AN ABSTRACT OF THE DISSERTATION OF

Nasir Alimardani for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on June 11, 2013.

Title: Investigation of Metal-Insulator-Metal (MIM) and Nanolaminate Barrier MIIM Tunnel Devices Fabricated via Atomic Layer Deposition

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John F. Conley, Jr.

Metal-insulator-metal (MIM) tunnel devices have been proposed for high speed applications such as hot electron transistors, IR detectors, optical rectennas for IR energy harvesting, and backplanes for LCDs. The majority of these applications require highly asymmetric and non-linear current versus voltage (I-V) behavior at low applied voltages and ultra-high frequencies. The objective of this work is to develop MIM tunnel devices with improved electrical properties including I-V asymmetry and non-linearity. The standard approach to achieving asymmetric operation in MIM devices is through the use of electrodes with different metal work functions. This approach is investigated using a variety of thin film dielectrics deposited by atomic layer deposition (ALD). To assess suitability for high speed operation, the physical mechanisms of electron transport in each dielectric are investigated. Next, as an alternative approach to achieving asymmetric and non-linear operation, pairs of dielectrics with different band-gaps and band-offsets are combined to form asymmetric tunnel barrier metal-insulator-insulator-metal (MIIM) diodes. MIIM diodes are fabricated using ALD to form nanolaminate pairs of Al_2O_3, HfO_2, ZrO_2, and Ta_2O_5 between asymmetric electrodes. It is found that the performance of the MIIM diodes is sensitive to the choice, relative thickness, and arrangement of the individual dielectric layers. It is shown that asymmetric dual-dielectric tunnel barriers can overwhelm the influence of asymmetric electrodes and it is demonstrated that MIIM structures can be designed to provide improved asymmetry at low electric fields. Low field asymmetry improvements are shown to be due to a step tunneling phenomenon. Finally, the formation and influence of interfaces, as a means for providing insight into engineering of nanolaminate barrier tunnel devices is examined by comparing different atomically smooth bottom electrodes.

Investigation of Metal-Insulator-Metal (MIM) and Nanolaminate Barrier MIIM Tunnel Devices Fabricated via Atomic Layer Deposition

By

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Nasir Alimardani, Author

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CONTRIBUTION OF AUTHORS

Wei Wang from Prof. Doug Keszler's research group helped with AFM characterizations in chapter 2 and 3. Cheng Tan assisted with electrical measurements in chapter 2. Dr. Dave Evans provided electron beam evaporated Ir and Pt used in devices reported in chapter 3. Prof. Brady Gibbons let us to use his research group spectroscopic ellipsometer for the studies of chapters 2, 3, 4, 5, and 6 for measuring thicknesses of dielectric films as well as analyzing optical dielectric responses of ALD films reported in chapter 4. Dr. Pete Eschbach helped greatly in TEM imaging and sample preparation of work in chapter 6 and 8. I would like to thank John McGlone, Bill Cowell, and Prof. John Wager for sputtered ZrCuAlNi films used as bottom electrodes for devices studied in chapters 6, 7, and 8.

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To my parents,

Mehdi and Mahdokht,

for their unwavering support

CHAPTER 1

Introduction

Thin film MIM based tunneling devices are seeing renewed interest for high speed applications.[1-11] Besides rectenna solar cells,[12-15] these applications include hot electron transistors,[16-18] and infrared (IR) detectors.[19-24] MIM diodes have also been proposed for macroelectronics applications[25] such as backplanes for liquid-crystal displays (LCDs).[26] Before any of these applications can be realized, a manufacturable process will be required that can produce uniform, high quality MIM tunnel devices with high asymmetry and non-linearity. Despite investigation by many groups over many decades,[27-34] progress towards commercialization of MIM based electronics has been hindered by a lack of a manufacturable process. In particular, inattention to electrode roughness along with the lack of a high quality deposited oxide appears to have slowed development of this technology - most experimental work to date on thin film MIM diodes has focused on the use of thin native dielectrics produced by oxidation or nitridation of an underlying rough polycrystalline metal electrode.[3,4,7-9,19-24,27-34] The operation of MIM diodes is based on quantum mechanical tunneling through a thin insulating film positioned between two metal electrodes.[35,36] The impact of roughness can be appreciated if it is remembered that the tunneling probability depends exponentially on the electric field in the thin dielectric film.[37,38] The tunneling current in a MIM tunnel diode should therefore depend strongly on the atomic scale roughness and the uniformity of the electrode-insulator interfaces.[39] Basic studies on electrode and interface roughness and their correlation with the tunneling current will therefore be very important for the advancement of MIM technology. In chapter 2 and 3, the performance of MIM tunnel diodes formed on bottom electrode materials with various levels of RMS roughness is compared. It is shown here that bottom electrode roughness can have a dominant impact on the electrical characteristics of MIM diodes, overwhelming the trends expected based on metal electrode work function differences. It is also shown that as electrode roughness decreases, the percentage yield of well-functioning devices trends higher.

As it will be discussed in chapter 4, for rectenna based solar cells as well as other potential applications of MIM diodes, highly asymmetric and non-linear current vs. voltage (I-V) behavior at low applied voltages is desired. Two potential dielectric candidates, Ta_2O_5 and Nb_2O_5, for low bias range performance of MIM tunnel diodes are investigated in chapter 4. Whereas previous MIM diode work has focused primarily on native oxides, the use of atomic layer deposition (ALD) in this work allows for deposition of high quality insulators, independent of the bottom metal electrode. In chapter 5, a variety of ALD dielectrics with narrow and wide band gaps including SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, and Nb_2O_5 are investigated as tunnel barriers in MIM tunnel diodes. The dominant conduction mechanism of electrons through these dielectrics is studied. I-V behavior of these diodes is analyzed regarding desired properties such as asymmetry and non-linearity in I-V response.

The standard approach to achieving asymmetric I-V characteristics in tunnel devices is the M_1IM_2 diode - the use of metal electrodes with different work functions ($\Phi_{M1} \neq \Phi_{M2}$) to produce a built-in voltage, $V_{bi} = (\Phi_{M1} - \Phi_{M2})/e$ (where e is the electronic charge) across the tunnel barrier.[38,40] However, even with low roughness electrodes, the amount of asymmetry achievable using this approach is limited by the V_{bi} ($\Delta\Phi_M$) that can be obtained using practical electrodes. An alternative approach to achieving asymmetric and non-linear operation is therefore needed. The approach investigated in chapters 6 and 7 involves engineering of the tunnel barrier so that electrons tunneling from one metal electrode to the other are presented with a different barrier shape depending on the direction of tunneling. Theoretically, formation of an asymmetric tunnel barrier can be accomplished using stacking of insulators,[41] with each insulator having different band-gaps (E_G) and electron affinities (χ), to produce metal-insulator-insulator-metal (MI_1I_2M) devices.[42,43] The *combined* effect of bilayer tunnel barriers and asymmetric ($\Phi_{M1} \neq \Phi_{M2}$) electrodes are investigated.[11] As illustrated in Fig. 1.1, for a pair of insulators, asymmetry may be enhanced through either resonant tunneling or step tunneling. Whereas most work in the literature has been concerned with resonant tunneling, here it is experimentally demonstrated that bilayer insulator tunnel barriers enable tuning of asymmetry (η) and non-linearity (f_{NL}) via step tunneling

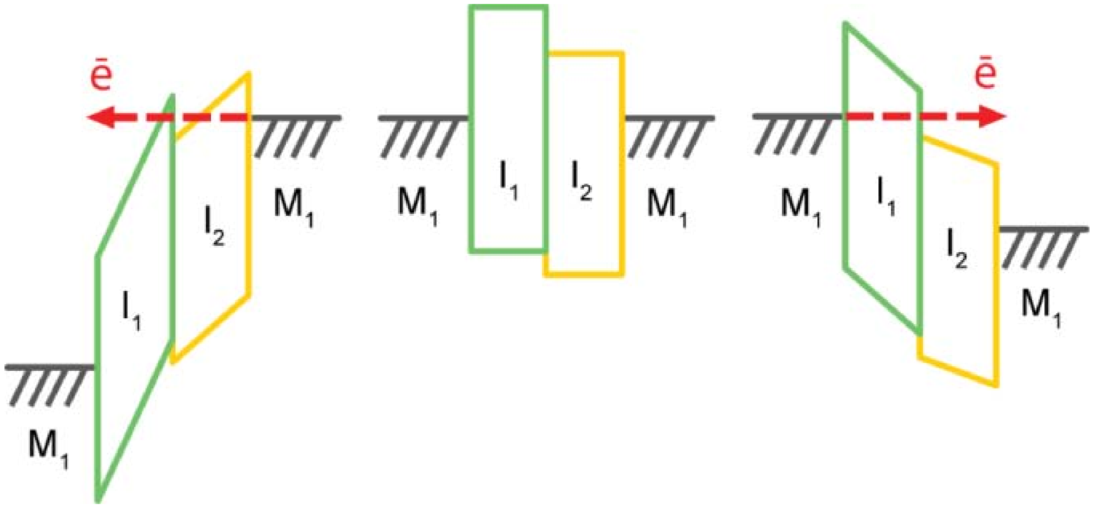

Fig. 1.1: Energy band diagrams of symmetric electrode $M_1I_1I_2M_1$ tunnel diodes, showing resonant tunneling (left) and step tunneling (right). In all band diagrams, the left electrode is grounded and voltage is applied to the right electrode.

Finally, the formation and influence of interfaces, as a means for providing insight into engineering of nanolaminate barrier tunnel devices is examined. It is discussed that interfacial layers form at the interfaces between electrodes and dielectrics, and nanolaminate dielectric layers can influence and change electrical behavior of MIM and MIIM tunnel devices.

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CHAPTER 2

Impact of Electrode Roughness on Metal-Insulator-Metal Tunnel Diodes with Atomic Layer Deposited Al_2O_3 Tunnel Barriers

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2.1 Introduction

Metal-insulator-metal (MIM) based tunneling devices, with very thin insulator layers compared to MIM capacitors, have been proposed for a variety of applications, including hot electron transistors,[1,2] infrared (IR) detectors,[3,4] liquid-crystal display (LCD) backplanes,[5] optical rectennas for IR energy harvesting,[6] and macroelectronics.[7] Despite investigation by many groups over many decades, progress towards commercialization of MIM based electronics has been hindered by the lack of a manufacturable process for fabrication of high quality MIM diodes. The operation of a MIM diode is based on quantum mechanical tunneling through a thin insulating film positioned between two metal electrodes.[8,9] The tunneling probability depends exponentially on the thickness of the insulator / insulator electric field; thus, the performance of a MIM tunnel diode should depend strongly on the atomic scale roughness and the uniformity of the electrode-insulator interfaces.[9-11] In fact, Miller et al.[12] have theoretically predicted that interfacial roughness should affect tunneling current in tunnel junctions. Inattention to electrode roughness along with the lack of a high quality deposited oxide appears to have slowed development of this technology. Most experimental work to date on MIM diodes has focused on the use of thin native dielectrics produced by oxidation or nitridation of the underlying polycrystalline metal electrode.[1-4,13-17]

Basic studies on electrode and interface roughness and their correlation with the tunneling current will be very important for the advancement of MIM technology. Recently, we demonstrated that sputter deposition of the amorphous metal ZrCuAlNi can be used to produce an ultrasmooth electrode (~0.3 nm root-mean-square (RMS) roughness).[18] While, the use of ZrCuAlNi as a bottom electrode in conjunction with high quality Al_2O_3 deposited via ALD allowed for reproducible fabrication of MIM tunnel diodes, we were unable to make any functioning devices on very rough Al bottom electrodes. Although it was hypothesized that the reason for good electrical characteristics on ZrCuAlNi versus the complete lack of functioning devices on Al was due to the large difference in roughness, our previous work did not discuss the case of intermediate electrode roughness – where the electrode roughness is not great enough to destroy all devices, but still large enough so that it might impact the electrical characteristics of functioning devices.

In the work presented herein, we compare MIM tunnel diode performance on low work-function (ZrCuAlNi and Al) and high work-function (Ir and two types of Pt) bottom electrode materials with various levels of RMS roughness. Whereas previous MIM diode work has focused primarily on native oxides, the use of atomic layer deposition (ALD) allows for deposition of the same high quality Al_2O_3 insulator on each of these bottom metal electrodes. We show that roughness can overwhelm the impact of metal work-function on the electrical characteristics of MIM diodes, in fact reversing the expected trends based on metal work-functions. We also find that that the percentage yield of functioning devices tracks higher with decreasing roughness. Finally, we find that even for nominally the same metal (Pt), the level of roughness dominates electrical characteristics and yield.

2.2 Experiment

MIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. First, blanket films of either Al, Pt, Ir, or ZrCuAlNi were deposited as bottom electrodes. A thin Ti adhesion layer was used for Pt and Ir. Al was deposited via thermal evaporation, Ir was deposited via electron-beam evaporation, and Pt was deposited using either DC sputtering (Pt-1) or electron-beam evaporation (Pt-2). ZrCuAlNi was deposited via DC magnetron sputtering with no intentional substrate heating using a 3-inch diameter, 0.25-inch thick vacuum arc-melted metal target (with an atomic composition $Zr_{40}Cu_{35}Al_{15}Ni_{10}$).[18] Next, a thin (≤ 10 nm) Al_2O_3 tunneling barrier was deposited via ALD using a Picosun SUNALE R-150B ALD reactor by alternating pulses of trimethlyaluminum (TMA) and deionized water at a temperature of 300 ºC. Finally, top electrodes were formed by evaporating Al dots (~0.8 mm^2) through a shadow mask.

Current density-electric field (J-ξ) characterization was conducted using an Agilent 4156C semiconductor parameter analyzer with samples at room temperature in the dark. Bottom electrode roughness (RMS and peak) was measured via atomic force microscopy (AFM) using a Digital Instruments 3 AFM with silicon-nitride tips. Work-functions of bottom electrodes were measured in air over an area of approximately 1 x 1 mm^2 using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip and calibrated against a gold standard. Work-functions of ZrCuAlNi and Al were measured to be approximately 4.8 eV and 4 eV, respectively. The thickness of Al_2O_3 films on ZrCuAlNi bottom electrodes was measured to be 9.5 ± 0.5 nm via TEM assessment,[18] and confirmed with a J.A. Woollam Co. WVASE32 spectroscopic ellipsometer using a Cauchy model.

2.3 Results and discussion

AFM micrographs, shown in Fig. 2.1, were used to establish the RMS and peak roughness of as-deposited ZrCuAlNi, Pt-1, Pt-2, and Ir bottom electrodes. Roughness values are averaged from a minimum of three images each. In order to assess any potential roughening as a result of the ALD thermal cycle or interaction of the TMA precursor with the electrodes, additional AFM images were also taken after deposition of a 10 nm Al_2O_3 layer (post ALD). As summarized in Table 2.1, the AFM images reveal a wide variation in both RMS average roughness and peak roughness, with ZrCuAlNi having the lowest roughness by a factor of 10. With the exception of Pt-2, the RMS and peak roughness tend to scale together. Following Al_2O_3 deposition, roughness values did not significantly change for the smoothest as-deposited electrodes, while the RMS roughness improved for the roughest as-deposited electrode, Ir. In contrast, the Al electrodes were found to roughen by about a factor of 5 after the Al_2O_3 deposition. This increase in roughness is not due to the ALD Al_2O_3 deposition itself. Rather, it is a consequence of the low melting point of Al and associated grain growth during the ALD thermal cycle.

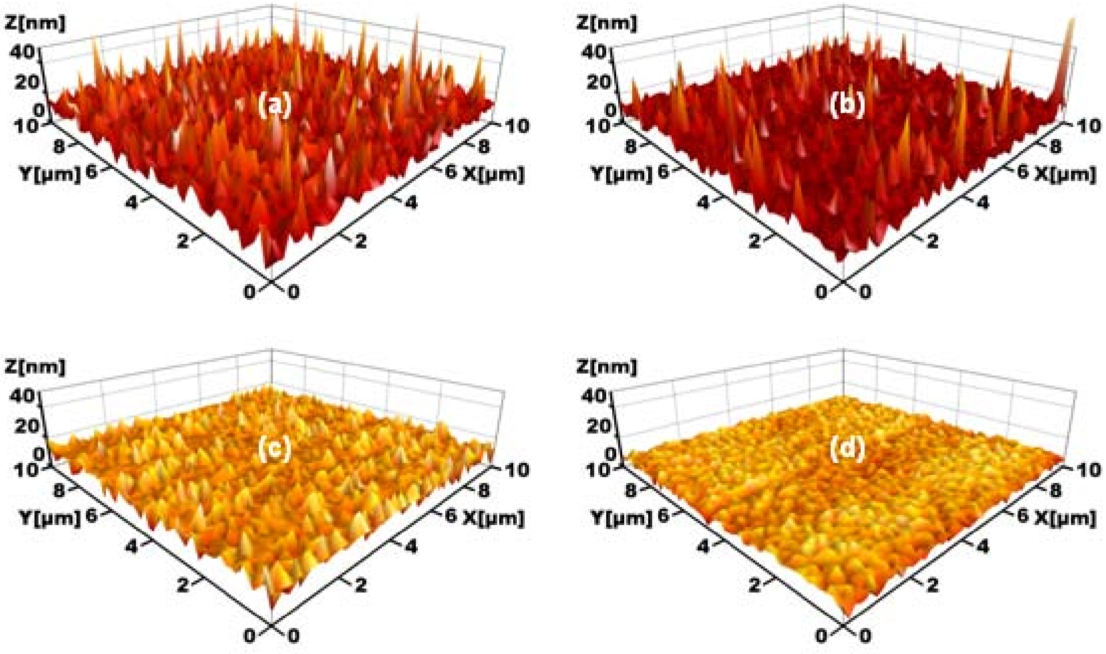

Fig. 2.1: AFM micrographs of as-deposited (a) Ir, (b) electron beam deposited Pt-2, (c) sputtered Pt-1, and (d) ZrCuAlNi blanket bottom electrodes.

Table 2.1: Work function, as-deposited and post-ALD RMS and peak rough-ness, and percentage of well functioning devices of metal bottom electrode / 10 nm Al2O3 / Al top electrode M1IM2 tunnel diodes.

Bottom Electrode	**Φ_M (eV)**	**Roughness (nm)**				**Functioning Devices (%)**
		As-deposited		Post ALD		
		RMS	Peak	RMS	Peak	
Al	4.2	4	43	21	468	0
Pt-2 (e-beam)	5.3	6 ± 1	220 ±5	5 ±1	210 ±10	< 10
Ir	5.1	11 ± 1	120 ±10	5 ±1	130 ±10	30 - 40
Pt-1 (sputtered)	5.3	2 ±0.5	22 ± 5	2 ±0.5	22 ± 10	30 - 50
ZrCuAlNi	4.8	0.3±0.1	3 ± 1	0.3±0.1	3 ± 1	65 - 80

Shown in Fig. 2.2(a) and (b), are simulated and representative measured J-ξ curves, respectively, for MIM devices with an Al top electrode (M_2), a ~10 nm thick Al_2O_3 tunnel barrier, and Ir, Pt, or ZrCuAlNi as bottom electrodes (M_1). The J-ξ curves are simulated using the Fowler-Nordheim (FN) tunneling equations of Simmons,[9,11]

$$J = \frac{1.1\, q^2}{4\pi h}\frac{1}{\varphi_b}\left(\frac{V+\Delta\varphi_b}{S}\right)^2 exp\left(\frac{-23\pi\sqrt{qm}}{6h}\ \varphi_b^{\frac{3}{2}}\left(\frac{S}{V+\Delta\varphi_b}\right)\right), \tag{1}$$

where q is the electron charge, h is Plank’s constant, V is the applied bias, φ_b is the barrier height of the electrode-insulator interface from which electrons are tunneling, $\Delta\varphi_b$ is the difference in barrier heights between the top and bottom electrode / insulator interfaces, m is the effective electron mass, and S is the tunnel barrier thickness. Simulations were performed with Matlab using an Al_2O_3 thickness of 10 nm, an electron affinity value of 2.58 eV for ALD-Al_2O_3,[19] and an electron effective mass of 0.79 of the free electron mass.[18] The only difference between the three simulated curves is the work-function of the bottom electrode (M_1), as given in Table 2.1. In order to understand the J-ξ trends of Fig. 2.2, it is necessary to consider MIM energy band diagrams. The equilibrium band diagram of a symmetric MIM tunnel device is shown in Fig. 2.3(a). The J-ξ characteristic of a symmetric MIM device is expected to be symmetric because the barrier to electron tunneling is the same in either direction. The diodes investigated in this work have asymmetric electrodes. The equilibrium band diagram of an asymmetric MIM tunnel diode is shown in Fig. 2.3(b). φ_{b1} and φ_{b2} indicate the barrier height of the bottom electrode metal M_1 (Ir, Pt, or ZrCuAlNi) and the smaller work-function top gate electrode metal M_2 (Al), respectively. Also shown are band diagrams of the asymmetric diode at the onset of FN tunneling for (c) positive and (d) negative bias applied to M_2 (assuming M_1 to be grounded).

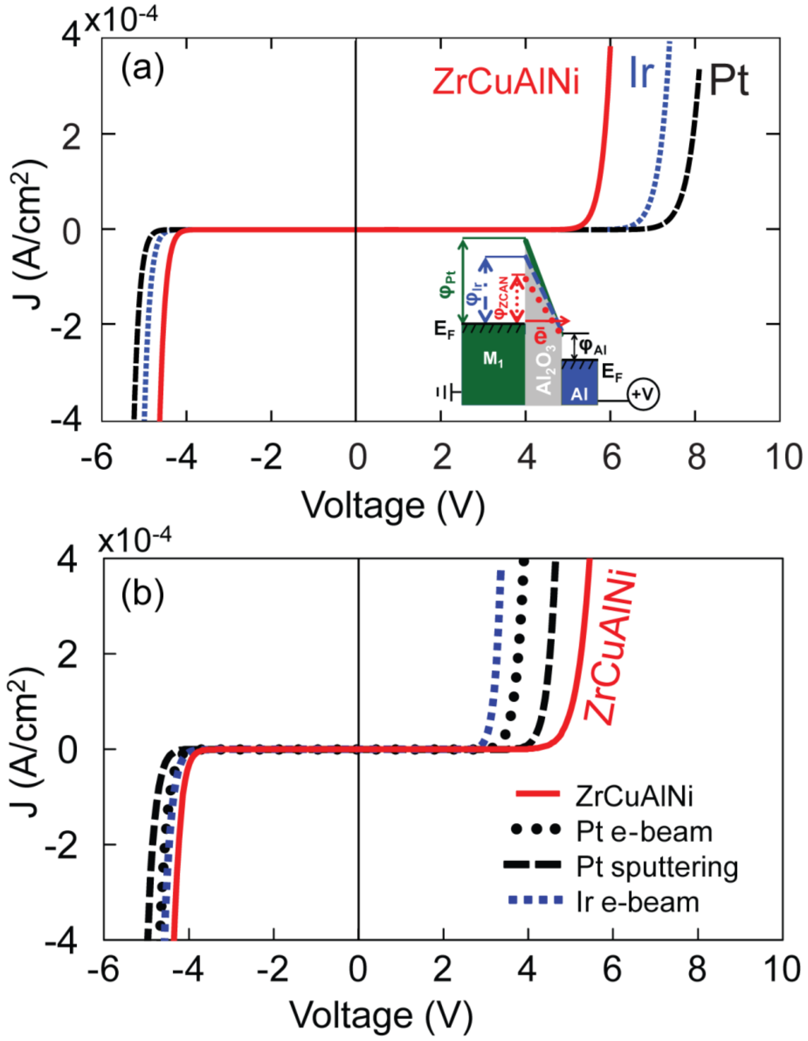

Fig. 2.2: (a) Plots of simulated current density vs. voltage (J-V) for M_1IM_2 diodes with either ZrCuAlNi, Ir, or Pt bottom (M_1) electrodes, a 10 nm thick Al_2O_3 tunnel barrier, and an Al top electrode (M_2). (b) Measured J-V for actual devices fabricated using ZrCuAlNi, Ir, sputtered Pt-1, and electron beam deposited Pt-2 bottom electrodes (M_1).

Considering first application of a sufficiently large *positive* bias to electrode M_2, FN tunnel emission occurs from the bottom electrode (M_1; Ir, Pt, or ZrCuAlNi), with different barrier heights as indicated in the energy band diagram given in the inset of Fig. 2.2(a). Note that the sketch is for the applied bias in which tunnel emission from electrode M_1 transitions from direct tunneling (across the entire insulator thickness) to FN tunneling (in which the tunnel distance decreases with increasing bias, because of the now triangular shape of the barrier). Since the insulator thickness used (10 nm) is sufficient to suppress direct tunneling, current conduction is dominated by FN tunneling. The probability of FN tunneling is exponentially dependent upon the insulator thickness and the barrier height presented to the tunneling electron (φ_{b1} for positive biases as shown in the inset in Fig. 2.2(a)). Thus, while the *onset* of FN tunneling for positive bias will be roughly the same for all bottom electrodes (as it involves overcoming the same barrier height, φ_{b2}, of the Al top electrode), the magnitude of the FN tunneling current at larger positive fields ($V_{app} >> \varphi_{b2}$) should be in reverse order of increasing work-function (increasing φ_{b1}). Based on relative barrier heights, the current density of the MIM diode with the ZrCuAlNi electrode (Φ_{ZCAN} = 4.8 eV) would be expected to be higher than that of the device with the Pt electrode (Φ_{Pt} = 5.3 eV), while the MIM diode with the Ir electrode (Φ_{Ir} = 5.1 eV) would be intermediate.[20] Although this trend is observed in the simulation (Fig. 2.2(a)), it is clearly not the trend witnessed in Fig. 2.2(b) by the experimental data.

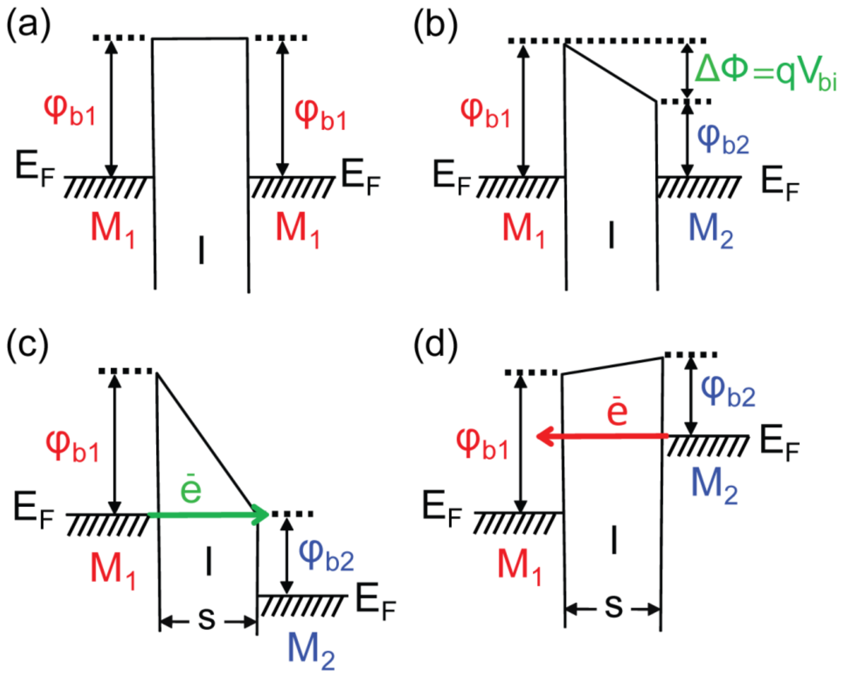

Fig. 2.3: Equilibrium band diagrams of (a) symmetric M_1IM_1 and (b) asymmetric M_1IM_2 tunnel diodes. φ_{b1} and φ_{b2} indicate the barrier height of the bottom (high work function M_1) and top (low work function M_2) metal electrodes, respectively. Energy band diagrams of the asymmetric tunnel diode under (c) positive applied bias showing the onset of FN tunneling and (d) an equivalent magnitude negative applied bias showing direct tunneling. In all band diagrams, M_1 is grounded and voltage is applied to M_2.

Assuming that the Al_2O_3 thickness for all devices is the same and that conduction is dominated by FN tunneling, a likely explanation for the unexpected trend shown in Fig. 2.2(b) is associated with the relative roughness of the bottom electrode. A rough bottom electrode could lead to electric field nonuniformity across the insulator due to field enhancement at sharp features which would decrease the effective insulator thickness. This field enhancement / decreased effective insulator thickness would tend to lead to increased conduction. As collected in Table 2.1 for the MIM structures measured in Fig. 2.2(b), Ir has the largest as deposited RMS roughness (11 nm) followed by e-beam deposited Pt-2 (6 nm), sputtered Pt-1 (2 nm), and finally ZrCuAlNi (0.3 nm). As evident from Fig. 2.2(b), the positive polarity current density trend correlates with bottom electrode roughness, while the curve of the device with ZrCuAlNi bottom electrode just matches with its simulation.

The RMS roughness for both Ir and Pt-2 are comparable to the overall dielectric thickness. Thus, it is not surprising that bottom electrode roughness overwhelms the expected influence of work-function. Perhaps the clearest indication of the impact of roughness can be seen by directly comparing MIM tunnel diodes made using the *same* bottom electrode (Pt) with two different levels of roughness. Despite having the same nominal work-function, the rougher e-beam evaporated Pt-2 (RMS = 6 nm) device shows a higher positive bias current density than the smoother DC sputtered Pt-1 (RMS = 2 nm) device (Fig. 2.2(b)).

Turning next to application of a sufficiently large *negative* bias to electrode M_2, electron tunnel emission now occurs from the top metal electrode (M_2; Al), as indicated in the energy band diagram in Fig. 2.3(d). The onset of FN tunneling should not occur until larger negative voltages for larger φ_{b1} and the simulation in Fig. 2.2(a) shows that the negative bias current density is expected to decrease slightly with increasing M_1 work-function. As shown in the measured data in Fig. 2.2(b), the devices made with ZrCuAlNi as a bottom electrode once again match fairly well with simulation. As compared with the simulation, the voltage required to achieve a given current density is reduced only slightly for both the Pt and Ir electrode devices. Ir shows the greatest deviation from simulation while the rougher Pt-2 once again deviates more than Pt-1.

The deviation between measured and simulated current density is much less on the negative bias side than on the positive bias side (Fig. 2.2). Additional FN tunneling simulations show that in an asymmetric MIM device, tunneling from the higher work-function side (in our case positive bias tunnel emission from M_1) is more sensitive to changes in the tunnel barrier (such as in thickness, electron effective mass, or electron affinity) than tunneling from the lower work-function side (in our case negative bias tunnel emission from M_2). The data in Fig. 2.2 suggests that tunneling from the higher work-function side (which occurs under positive bias in our experiments) is also more sensitive to roughness than tunneling from the smaller work-function side (which occurs under negative bias in our experiments). In addition, some smoothing of the roughest electrodes is observed after ALD (Table 2.1). While the roughness values did not change significantly for ZrCuAlNi and Pt-1, the smoothest as-deposited electrodes, the RMS roughness improved significantly for Ir (from 11 nm to 5 nm), and slightly for Pt-2 (from 6 nm to 5 nm).

Desired J-ξ characteristics for diodes include high non-linearity and asymmetry. Assuming that FN tunneling dominates, a larger work-function difference between electrodes should lead to more nonlinearity and asymmetry, as the simulation in Fig. 2.2(a) demonstrates. However, this is not the trend observed when roughness dominates, such as is the case for the Ir and two Pt electrodes in Fig. 2(b). The largest asymmetry for the experimental J-ξ curves shown in Fig. 2.2(b) belongs to the diode made with the smoothest electrode, in this case ZrCuAlNi. The full extent of work-function induced asymmetry is only evident when the bottom electrode roughness is minimized.

The percentage of functioning MIM diodes is also found to correlate with bottom electrode roughness. Diodes were considered non-functioning due to either electrical shorts or early breakdown under a low applied electric field. Smoother bottom electrodes are found to yield a greater percentage of functioning devices (Table 2.1). Devices fabricated using ZrCuAlNi, the smoothest bottom electrode investigated, have the highest fraction of functioning devices. At the opposite end of the roughness spectrum, no working diodes are obtained using Al bottom electrodes. The Al films are the roughest metal films investigated, with a post ALD RMS roughness of 21 nm (greater than the tunnel barrier thickness) and a peak roughness of more than 450 nm. Comparing the two types of Pt, use of the smoother Pt-1 results in a higher percentage of functioning devices than the rougher Pt-2 devices. Finally, despite lower as-deposited and roughly equivalent post ALD RMS roughness, Pt-2 bottom electrodes are found to yield a lower percentage of working devices than Ir bottom electrodes. This appears to be due to the larger peak roughness of the Pt-2 electrode devices.

Shown in Fig. 2.4(a) are J-ξ curves for seven Al top electrode (M_2) / ~10 nm thick Al_2O_3 tunnel barrier / ZrCuAlNi bottom electrode (M_1) diodes from five substrates produced in four different process runs. Using ultrasmooth ZrCuAlNi as a bottom electrode, we have been able to produce uniform and repeatable device characteristics with high yield that are well predicted by Fowler-Nordheim tunneling theory and the Simmons equations. Note that despite the inverse dependence of yield on bottom electrode roughness and non-agreement with Fowler-Nordheim theory for the rough bottom electrode devices, when *functioning* devices are obtained, even the devices with rough bottom electrode (Ir, Pt-1, and Pt-2) exhibit little variation in J-ξ characteristics. Finally, shown in Fig. 2.4(b) are 100 sequential J-ξ sweeps (-4.5 V to +6 V to -4.5 V) on a single Al top electrode (M_2) / ~10 nm thick Al_2O_3 tunnel barrier / ZrCuAlNi bottom electrode (M_1) device showing stable J-ξ response.

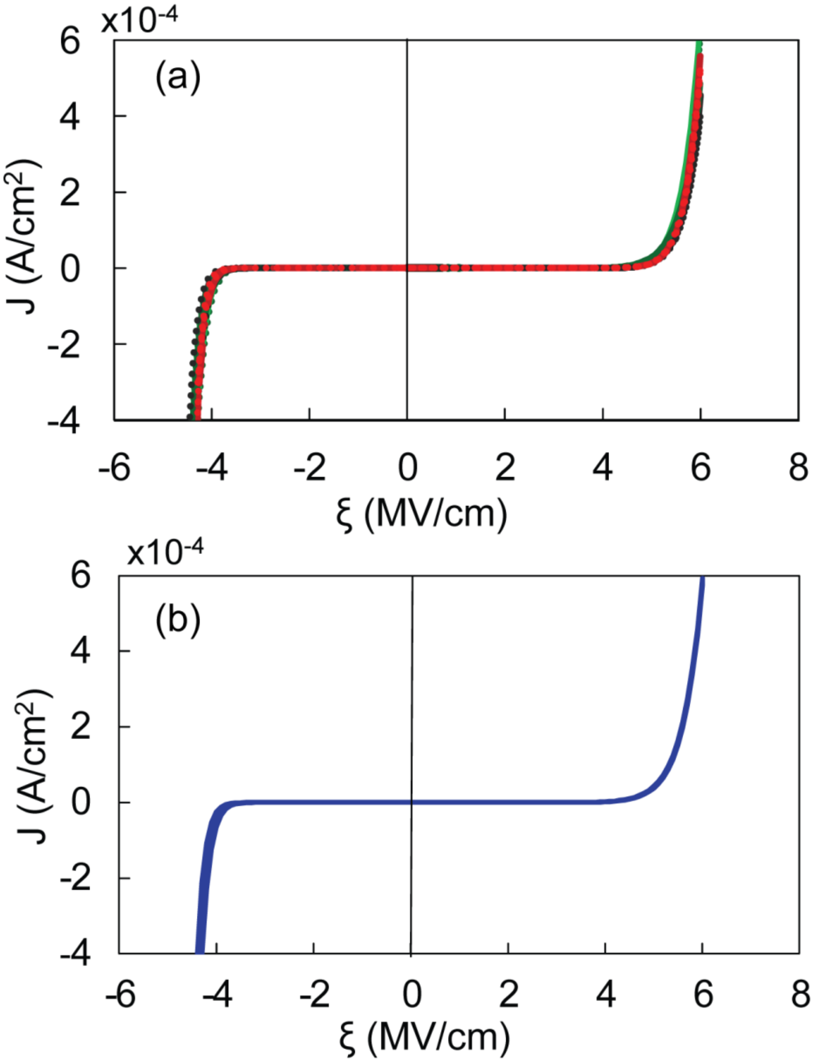

Fig. 2.4: (a) J-ξ sweeps for seven different MIM tunnel diodes taken from five different substrates fabricated in four different identical process runs. Different colors indicate different devices. The fact that the devices overlap and are barely distinguishable from one another is an indication of the run to run and device to device uniformity. (b) 100 sequential J-ξ sweeps on a single device. In all cases, the stack structure of the devices consists of ZrCuAlNi / ~10 nm Al_2O_3 / Al top electrode.

2.4 Summary

We compare MIM tunnel diode performance on low work-function (ZrCuAlNi and Al) and high work-function (Ir and two types of Pt) bottom electrode materials with

RMS roughness levels ranging from ~3% to greater than 100% of the insulator thickness. Most previous experimental work on MIM diodes has been conducted on native oxides produced by either oxidation or nitridation of the bottom metal electrode. Using ALD, we are able to deposit a high quality Al_2O_3 insulator, independent of the bottom metal electrode. We show (i) that roughness can overwhelm the impact of metal work-function on the electrical characteristics of MIM diodes, in fact reversing the expected trends based on metal work-functions, (ii) that the percentage yield of functioning devices tracks higher with decreasing roughness, and (iii) that even for the same nominal metal (Pt), the level of roughness dominates electrical properties and yield. Our results indicate that bottom electrode roughness levels of much less than 20% of the insulator thickness are necessary to achieve non-roughness dominated electrical behavior and suggest that it is likely that most prior MIM tunnel diode studies may have been compromised by uncontrolled bottom electrode roughness.[21] By using ultrasmooth (~0.3 nm RMS) bottom electrodes and uniform tunnel barriers deposited via ALD we have demonstrated highly non-linear and asymmetric MIM tunnel diodes with good device to device uniformity and stable J-ξ behavior. The good reproducibility and percentage of working devices, which have been a major challenge for MIM tunnel diodes reported to date, represent an important step towards commercialization of this technology.

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CHAPTER 3

Stability and Bias Stressing of Metal-Insulator-Metal Diodes

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3.1 Introduction

Metal/insulator/metal (MIM) based devices have been proposed as an alternate approach to high-speed (THz) hot electron transistors,[1] infrared (IR) detection, [2] liquid-crystal display (LCD) backplane electronics,[3] and optical rectennas for IR energy harvesting.[4] Commercialization of these applications has been hindered by the lack of manufacturable high quality MIM diodes. The operation of MIM diodes is based on quantum mechanical tunneling through the thin dielectric film placed between the two metal electrodes.[5] Desired current-voltage characteristics include high non-linearity and asymmetry. Since tunneling depends exponentially on the thickness of the barrier, reliable operation of these devices depends critically on electric field and device uniformity, which are dominated by electrode roughness and insulator thickness. Progress has been hampered by inattention to the smoothness of the electrodes and the lack of available highly uniform deposited oxides - most experimental work to date has been performed on oxidized crystalline metals.[6] In this work, we demonstrate that high-quality MIM tunnel diodes can be made using smooth bottom metal electrodes in combination with thin dielectrics deposited via atomic layer deposition (ALD) and begin to investigate the stability and bias stress reliability.

3.2 Experiment

MIM diodes were fabricated on Si/SiO_2 (100 nm of thermally grown SiO_2) substrates using either Al, Pt, Ir, or amorphous ZrCuAlNi (ZCAN) as a blanket lower electrode. A thin few nanometer thick Ti adhesion layer was used for the elemental metals. Al was deposited via thermal evaporation, Ir was deposited via electron-beam evaporation, and Pt was deposited via either sputtering (Pt(1)) or electron-beam evaporation (Pt(2)). ZCAN was deposited via DC magnetron sputtering with no intentional substrate heating using a 3-inch diameter, 0.25-inch thick vacuum arc-melted metal target (with an atomic composition Zr40Cu35Al15Ni10, manufactured by Kamis Inc.).[7] Next, thin (≤ 10 nm) blanket dielectric films of Al_2O_3 were deposited via ALD in a Picosun SUNALE R-150B ALD reactor using trimethlyaluminum (TMA) and deionized water at a temperature of 300°C. Finally, Al dots (~1 mm^2) were evaporated through a shadow mask to form the top electrode for all devices. The completed structure is shown in Fig. 3.1(a).

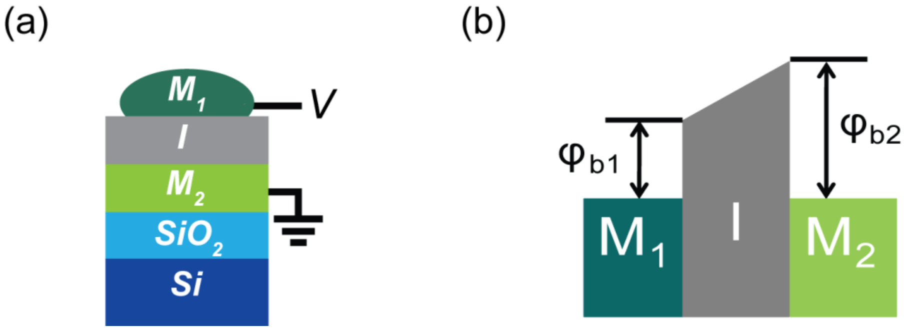

Fig. 3.1: (a) Schematic cross section of the asymmetric MIM devices used in this study and (b) band diagram of an asymmetric tunnel diode where φ_{b1} and φ_{b2} indicate the barrier height of the low and high workfunction metals, respectively.

Current density versus voltage (J-ξ) characterization was conducted using an HP 4156 semiconductor parameter analyzer and a probe station with samples at room temperature in the dark. Atomic force microscopy (AFM) images were obtained over 10 x 10 μm^2 with Digital Instrument 3 instrument with silicon-nitride tips. The workfunction of the bottom electrodes were measured in air over an area of approximately 1 x 1 mm^2 using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip calibrated against a gold standard. Al_2O_3 thickness on ZCAN was measured using a J.A. Woollam Co. WVASE32 spectroscopic ellipsometer.

3.3 Results and discussion

Shown in Fig. 3.2 are plots of current density vs. voltage (J-ξ) for MIM devices with a ~10 nm Al_2O_3 insulating layer and using either Ir, ZCAN, or sputtered Pt as a blanket bottom electrode. J-ξ characteristics for all devices are non-linear and asymmetric, as desired for diode operation. At *large* negative bias, all three devices have roughly same level of current density, as might be roughly expected for MIM devices with the same top electrode metal. The band structure of an asymmetric tunnel diode is shown in Fig. 3.1(b), where φ_{b1} and φ_{b2} indicate the barrier height of the top metal M1 (Al) and the higher workfunction bottom gate metal M2 (Ir, Pt, or ZCAN), respectively. At *large* positive biases, the magnitude of the conduction current (due to Fowler-Nordheim (F-N) tunneling) should be in reverse order of increasing workfunction. The workfunction of ZCAN was measured at 4.7 eV, Ir at 5.1 eV, and Pt(1) at 5.3 eV, so ZCAN should enter the FN regime first, followed by Ir and then Pt. It is seen, however, that Ir begins to show conduction at the lowest field, followed by Pt, and finally ZCAN. This is not consistent with what would be expected from the measured relative workfunctions. One possible explanation may be the relative roughness of the bottom electrodes. High bottom electrode roughness could cause field enhancement or effective thinning of the tunnel barrier, leading to higher current.

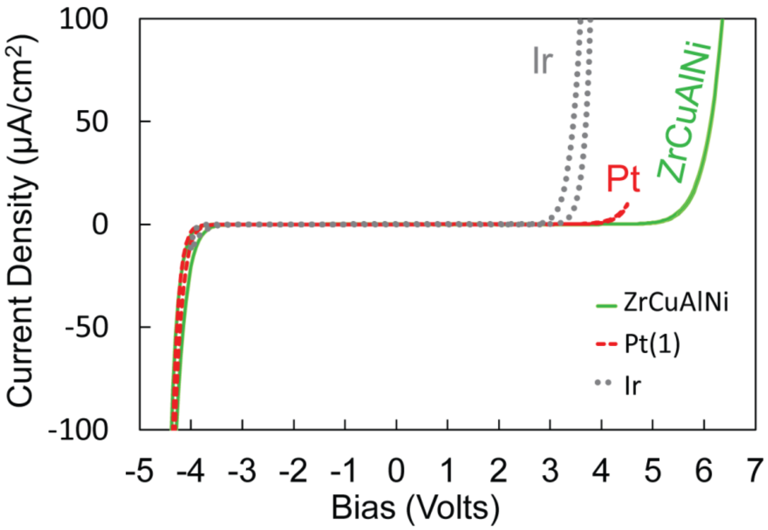

Fig. 3.2: Plot of current density vs. voltage (J-ξ) for MIM diodes fabricated on either Ir, ZCAN, or sputtered Pt bottom electrodes with 10 nm Al_2O_3 and Al top electrodes.

AFM micrographs (Fig. 3.3) of as-deposited ZCAN, Pt, Ir, and Al bottom electrodes reveal a wide variation in both RMS average roughness and peak roughness between the various metals. The AFM images of the electrodes were also taken after deposition of 10 nm Al_2O_3 to study the ALD thermal cycle as well as possible reaction of TMA precursor and the electrodes on roughness. The roughness values did not change after the Al_2O_3 deposition except for the Al electrodes. The Al electrodes were found to roughen by about a factor of 5. This is not due to the ALD Al_2O_3 deposition, but rather is expected due to the low melting point of Al and the likelihood of Al grain growth during the ALD thermal cycle. Roughness and yield are summarized in Table 3.1.

Referring again to Fig. 3.2, it is seen that Ir, the bottom electrode with the highest roughness (RMS = 11 nm), shows the highest conduction, followed by the sputtered Pt(1) (RMS = 2 nm), and finally ZCAN (RMS = 0.2 nm). These RMS values are considerable

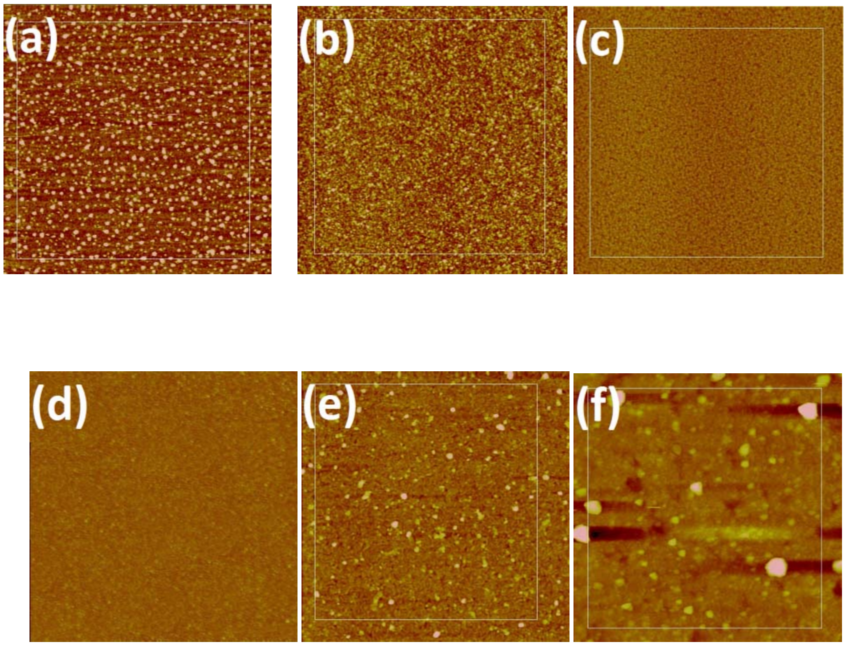

Fig. 3.3: AFM micrographs (10µm x 10µm) of as-deposited bottom electrodes. Shown are (a) Ir, (b) e-beam Pt(2), (c) sputtered Pt(1), (d) ZrCuAlNi, (e) Al, and (f) Al following 10 nm ALD Al_2O_3. The scale bar is not presented since the micrographs represent the uniformity of substrates.

in comparison to the film thickness and suggest that rougher bottom electrodes cause more FN tunneling through the insulator because of either enhanced field or an effectively thinner dielectric. It is also seen that forward bias hysteresis (ZCAN < Pt < Ir) follows bottom electrode roughness.

Table 3.1: Roughness of various blanket metal films and yield of samples made using the blanket metal / 10nm Al_2O_3 / Al top electrode devices.

Blanket	Yield (%)	RMS Roughness (nm)	Peak to Valley Height (nm)
ZrCuAlNi	65 to 80	0.3	5
Pt (1)	30 to 50	2.07	22
Ir	30 to 40	5.19	65
Pt (2)	<10	7.48	170
Al	0	13.86	190

In addition to leakage current density, it was found that device yield was anti-correlated with bottom electrode roughness – smoother electrodes were found to yield a greater percentage of working devices. For the Al bottom electrodes, the RMS roughness was greater than the dielectric thickness and all devices were shorted. Due to their amorphous nature, ZCAN bottom electrodes were the smoothest; devices fabricated using ZCAN electrodes were found to have the highest yield of working devices. (Using ZCAN as a bottom electrode, we are able to make working MIM diodes with an Al_2O_3 thickness down to 12 ALD pulse cycles.) The smoother Pt(1), deposited via sputtering, resulted in a much higher percentage of working devices than the rougher Pt(2) devices, deposited via evaporation. As shown in Fig. 3.4, a comparison of J-ξ sweeps for 10 nm Al_2O_3 MIM devices made with either Pt(1) or Pt(2) shows roughness has an important effect on the I-V characteristics of the devices. Devices made on Pt(1) and Pt(2) are might be expected

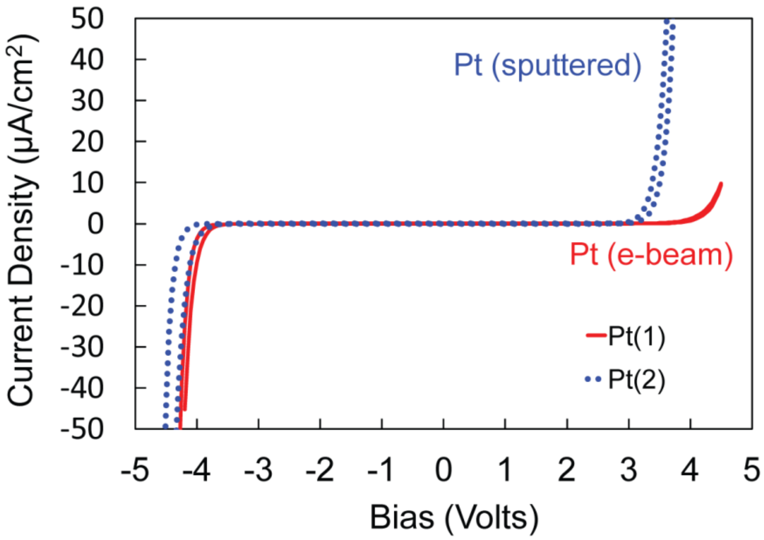

Fig. 3.4: Plots of back and forth J vs. ξ sweeps for sputtered (Pt(1)) and e-beam evaporated (Pt(2)) bottom electrode / ~10 nm Al_2O_3 / Al top gate diodes.

to exhibit similar characteristics but as it can be seen the device on the rougher Pt(2) has greater hysteresis as well as higher current density. The work function of Pt(2) was measured to be 5.1 eV, ~0.2 eV smaller than Pt(1), and would also account for some of the increased leakage.

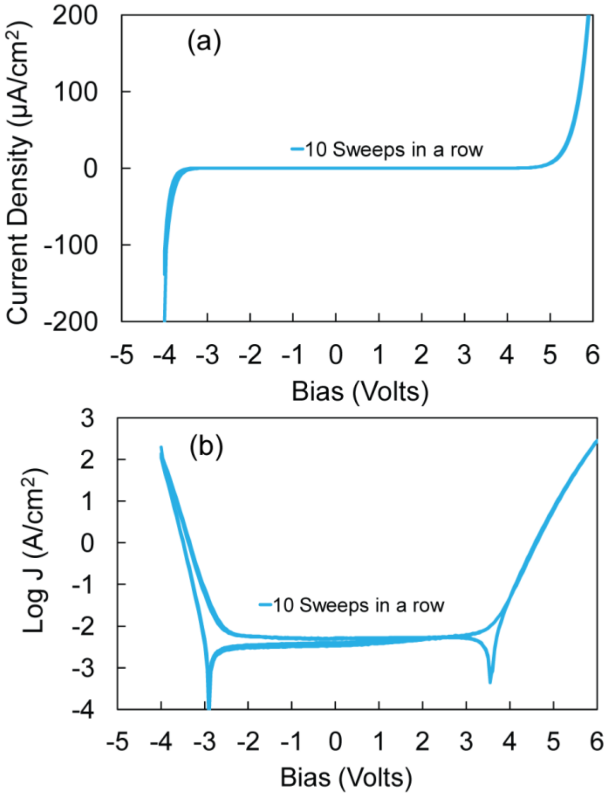

Fig. 3.5: Shown are 10 sequential J vs. ξ sweeps for a ZCAN / ~10 nm Al_2O_3 /Al device plotted on (a) linear, (b) log –linear scale

An important consideration for MIM diode applications is operational stability.[8] Shown in Fig. 3.5 are 10 sequential J-ξ sweeps for a ZCAN / ~10 nm Al_2O_3 / Al device plotted on a log-linear scale. The J-ξ behavior at low fields is dominated by displacement current, which causes the apparent reversal in leakage current polarity at non-zero fields. The devices show little shift, demonstrating that the short term stability of these unpassivated devices is quite good. The across sample uniformity of devices (not shown) is also quite good. The repeatability of this process, which is a big concern in tunneling devices that have been made to date, is unique and is a requirement for commercialization of this technology.

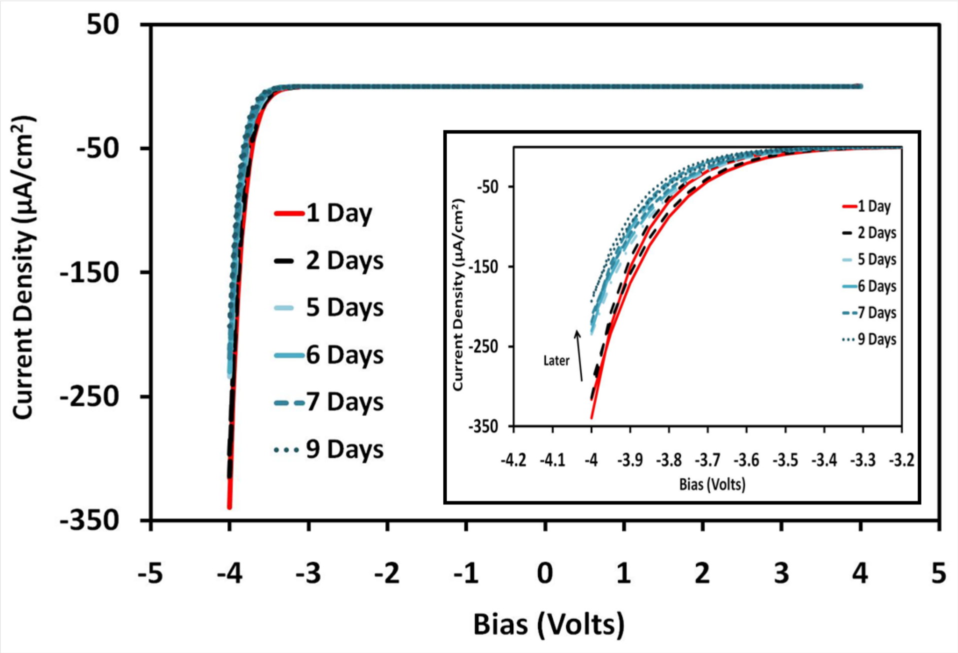

Fig. 3.6: Plots of J vs. ξ for the ZCAN / ~10 nm Al_2O_3 / Al device from Fig. 3.5 as a function of time after device fabrication.

Shown in Fig. 3.6 are J-ξ sweeps for the same device as a function of time. Over time, the onset of FN conduction is pushed out to higher voltages. Although not apparent in the plot, the displacement current was found to decrease by roughly 20% over nine days. Since identical sweep rates were used, this indicates that the capacitance of the device has decreased. A decrease in device capacitance suggests that either the effective dielectric thickness has increased or the dielectric constant has decreased, pointing to possible diffusion of species into the Al_2O_3. Alternatively, the metal electrode / Al_2O_3

barrier height may be changing over time so that electrons see a smaller energy barrier for tunneling through the insulator.

Shown in Fig. 3.7 are series of J vs. ξ sweeps taken on ZCAN / ~10 nm Al_2O_3 / Al devices after (a) +5 MV/cm and (b) -4 MV/cm DC bias stressing. The magnitude of DC bias stress was chosen to be larger than the metal/insulator barrier height required for FN tunneling but smaller than the instantaneous breakdown voltage. Due to the asymmetric nature of the diode structure (different top and bottom metal electrodes and thus different metal/insulator barrier heights) different stress fields were required. Although not obvious from the linear curves, the displacement current at zero bias increases with DC bias stressing time, indicating an increase in diode capacitance. This is opposite to what was observed for unstressed devices. It is also seen that bias stressing appears to accelerate the reduction of FN dominated current density. After 100 sec of +5 MV/cm stress, the current at -3.3 V has been reduced by 30% (0.15 $\mu A / cm^2$), equivalent to the reduction seen in Fig. 3.3(b) after 5 days unbiased. For 100 sec of -4 MV/cm stress, the reduction in current is even more pronounced, approximately 120%. The difference in positive and negative bias stress response may be attributed to the relative quality of the interfaces between the Al_2O_3 and the different top and bottom electrodes. For example, the results suggest that there may be more defects at or near the bottom metal / insulator interface than at the top interface.

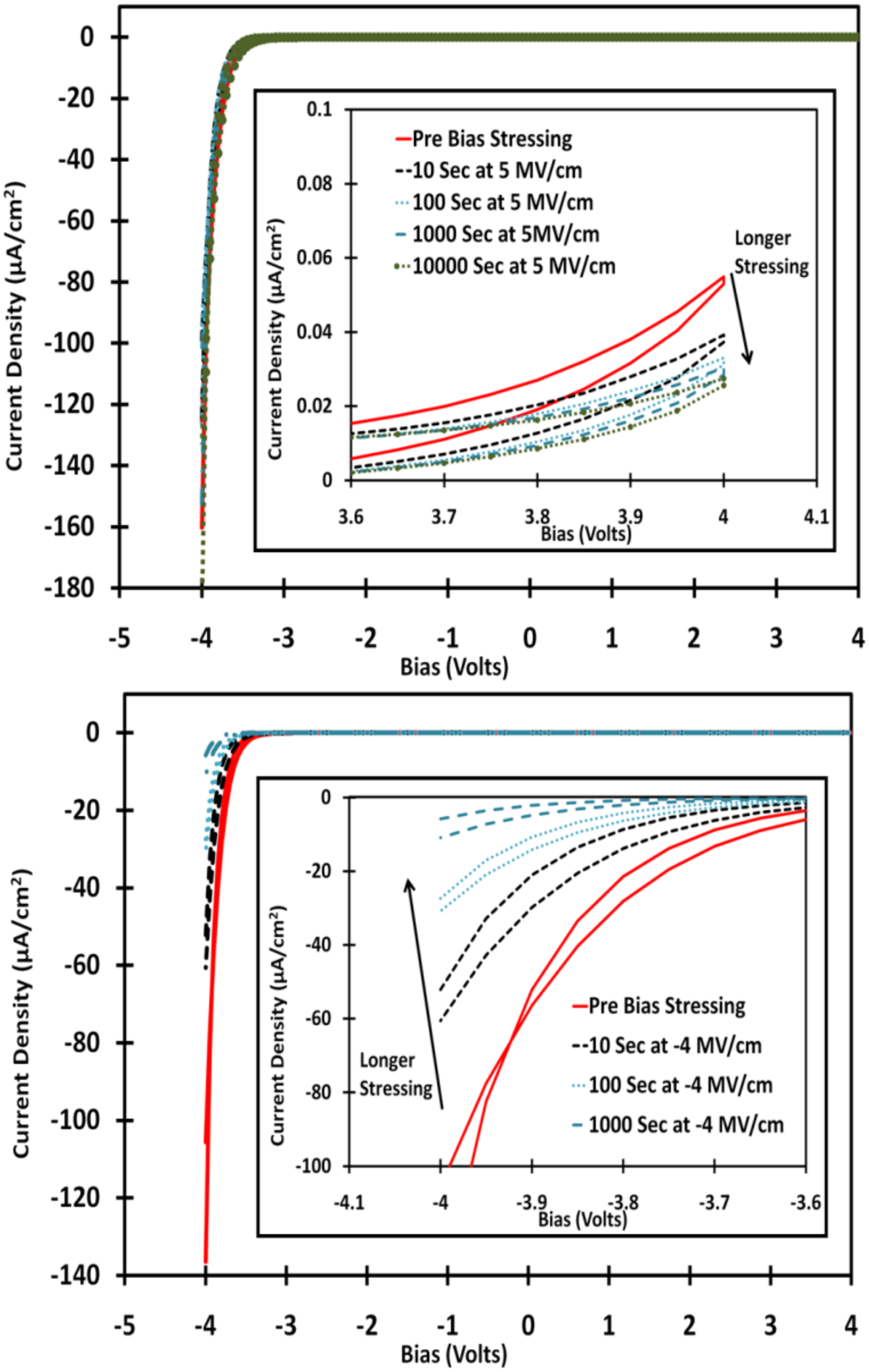

Fig. 3.7: J vs. ξ plots of a ZCAN / ~10 nm Al_2O_3 / Al device taken at intervals during +5 MV / cm (top), and -4 MV / cm DC bias stressing (bottom).

In order to assess the impact of roughness on DC bias stressing, a series of J vs. ξ sweeps taken on Ir / ~10 nm Al_2O_3 / Al devices after (a) +3 MV/cm and (b) -4 MV/cm DC bias stressing (Fig. 3.8). Ir devices were chosen for comparison to ZCAN since the Ir blankets were found to have the largest RMS roughness values of the working devices. The magnitude of DC bias stressing has been chosen as described for ZCAN devices. For (a) positive bias stressing, the reduction of current density is approximately 50% for 1000 sec stressing. For (b) negative bias stress, the device breaks down after 1000 sec of stress. Although a direct comparison is difficult due to the difference in workfunction between Ir and ZCAN, it appears that the greater roughness of the bottom Ir electrode plays a role in the DC bias stress response, particularly for negative bias stressing for which the bottom interface is critical.

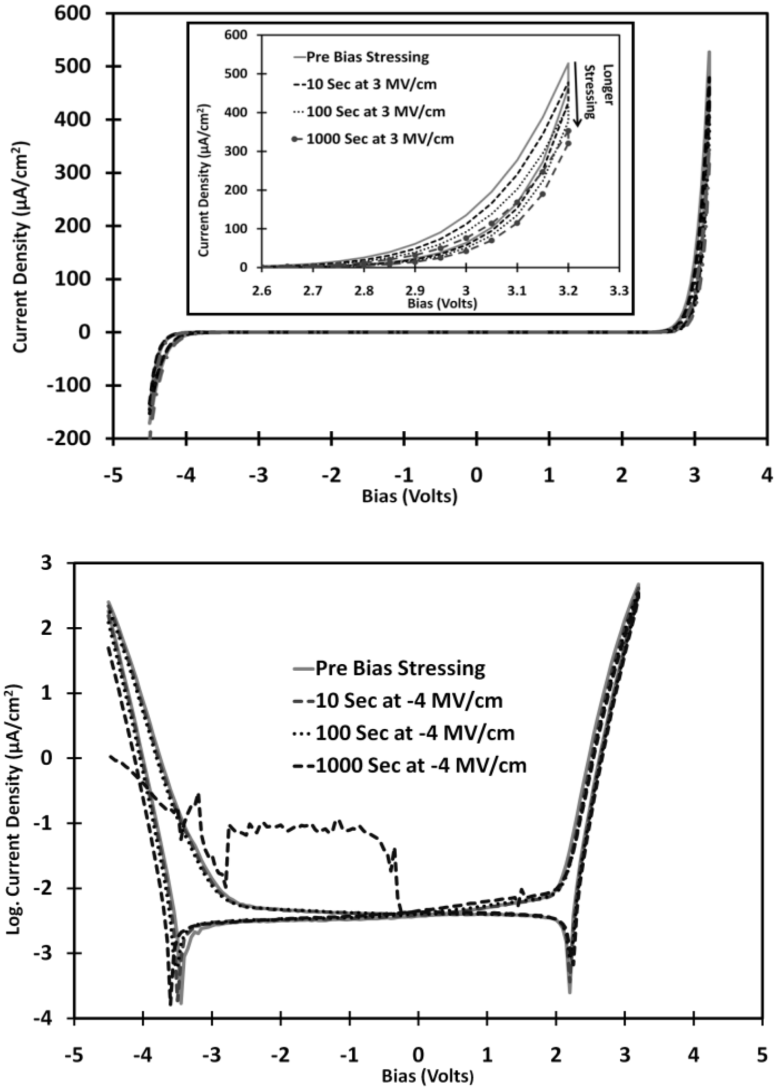

Fig. 3.8: J vs. ξ plots of an Ir / ~10 nm Al_2O_3 / Al device taken at intervals during +3 MV / cm (top), and -4 MV / cm (bottom), DC bias stressing.

2.4 Summary

We have demonstrated the fabrication of high-quality MIM tunnel diodes using smooth bottom electrodes and uniform ALD dielectrics. Both the J-ξ behavior and device yield were found to be a function of interfacial roughness. For example, it was found that bottom electrode roughness overwhelmed the influence of workfunction difference on the relative J-ξ behavior of Ir, Pt, and ZCAN devices. A preliminary investigation of DC bias stressed devices suggests that interfacial roughness plays a large role in stability and reliability as well.

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CHAPTER 4

Investigation of the Dominant Conduction Mechanism in Metal-Insulator-Metal Tunnel Diodes with Ta_2O_5 and Nb_2O_5 Dielectrics Deposited by Atomic Layer Deposition

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In preparation for submission

4.1 Introduction

Thin film metal-insulator-metal (MIM) tunnel diodes have recently attracted significant attention for a variety of low-power and high-speed applications such as hot electron transistors,[1,2] infrared (IR) detectors,[3-5] and optical rectennas for IR energy harvesting.[6, 7] The ultrahigh frequency (UHF) operation regime desired in these devices requires that the electron transport time between terminals be as short as a few femto seconds. Quantum mechanical tunneling through an ultrathin insulator is the only means of electron transport capable of achieving this time requirement. The standard way to achieve high speed rectification in tunnel diode is through the use of asymmetric work function metal electrodes to introduce different energy barriers for electrons tunneling under different polarities[9] with conduction dominated by Fowler-Nordheim (FN) tunneling,[8] An additional requirement for the MIM diodes used for rectenna and IR detector applications is a small turn-on voltage (V_{ON}) for a low zero bias resistance, and high asymmetry (η) and high non-linearity (f_{NL}) of the current density versus voltage (J-V) response of device at very low bias regimes.[10] Very recently, some research groups have theoretically predicted that Nb_2O_5 and Ta_2O_5 should be promising dielectric candidates for rectenna applications, [11-13] This is primarily due to their relatively large electron affinities, which should result in small energy barriers at the metal electrodes and allow FN tunneling to occur at small applied bias in diodes fabricated with either Nb_2O_5 or Ta_2O_5 as the tunnel barrier. However, the dominant conduction mechanisms have not yet been reported for actual MIM tunnel diodes made with Nb_2O_5 or Ta_2O_5.

Depositing high quality and pinhole free insulator layers with atomic scale thickness accuracy and choice of insulator layer independent of bottom electrode can be achieved by atomic layer deposition (ALD). Besides high quality dielectrics, smooth electrode-dielectric interfaces are also critical to achieve stable operation based on tunneling.[14,15] Using crystalline bottom metal electrode can overwhelm electron conduction through dielectric layer by introducing rough and defect rich electrode-dielectric interfaces. It has been shown that crystalline metal electrodes deposited with various advanced deposition techniques can have as deposited surface roughness many times larger than insulator layer thickness which can overwhelm work function of bottom electrodes, introduce a large amount of interface defect density, and deteriorate device yield.[14, 16] Using amorphous bottom electrode is also important to avoid work function non-uniformity due to different crystal orientations of grains. It should be noted that tunnel diode dimension is needed to be of order of nanometers for UHF applications to avoid large capacitive delays (RC values). For the rectenna application, nano scale diodes are also required for impedance matching to integrated antennas.[10]

In this work, we investigate in M_1IM_2 diodes fabricated with ZrCuAlNi amorphous bottom electrodes (M_1), Al top electrodes (M_2), and either Nb_2O_5 or Ta_2O_5 tunnel barriers (I) deposited via ALD. The J-V characteristics and rectification behavior are studied at temperatures ranging from 275° K to 375° K and the dominant conduction mechanism are identified in different bias regimes. For both dielectrics, it is found that Schottky emission dominates in the low bias regime whereas Poole-Frenkel emission dominates at larger biases. FN tunneling does not appear to play a significant role in device operation suggesting that MIM devices based on either Nb_2O_5 or Ta_2O_5 tunnel barriers may not be suitable for ultrahigh frequency operation. Trap depths are characterized

4.2 Experiment

MIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. A 150 nm thick ZrCuAlNi (ZCAN) bottom electrode was deposited directly on the SiO_2 via DC magnetron sputtering using a $Zr_{40}Cu_{35}Al_{15}Ni_{10}$ metal target. ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively.[14] Next, thin dielectric tunnel barriers were deposited via ALD using a Picosun SUNALE R-150B. Tantalum ethoxide and niobium ethoxide were used as the metal organic precursors for Ta_2O_5 and Nb_2O_5, respectively. Both ALD films were deposited at a chamber temperature of 250 ºC using deionized water as the oxidant. Finally, top electrodes were formed by evaporating Al dots (~0.2 mm^2) through a shadow mask.

The thickness and optical dielectric constant of the dielectrics was measured on Si with a J.A. Woollam WVASE32 spectroscopic ellipsometer using a Cauchy model. A dielectric thickness of 5 nm and 10 nm was chosen to facilitate distinguishing FN tunneling conduction from other conduction mechanisms - the 10 nm dielectric is thick enough to suppress direct tunneling while other mechanisms may still contribute to conduction at low applied voltages. All as-deposited ALD films were determined to be almost entirely amorphous via x-ray diffraction (XRD); however a low density of nanocrystalline seeds could be expected. Devices are studied without annealing treatments to avoid any possibility of crystallization of either the ALD films or the ZrCuAlNi bottom electrode. Crystalline phases in thin dielectric films may create alternate conduction paths for electrons[21] whereas crystallization of the bottom electrode increases electrode surface roughness which results in field enhancement[22] and increased defect density at the insulator-electrode interface.[23] An asymmetric electrode M_1IM_2 device structure is chosen for two main reasons. First, because different electrode-insulator interfaces are formed with different barrier heights, the influence of the interface on leakage current may be distinguished by comparing the current response at different polarities. Second, the ZrCuAlNi amorphous bottom electrode is deposited by DC magnetron sputtering. When used as a bottom electrode, it allows for high yield and high quality devices. However, if ZrCuAlNi is also used as the top electrode, the high energetic species introduced to dielectric surface during sputtering can cause damage to the dielectric, resulting in large hysteresis or electrical shorting for ultrathin devices.[15]

Two figures of merit are defined to characterize the devices: (i) I-V asymmetry, η, is defined as negative device current divided by positive current $|I_- / I_+|$ so that $\eta = 1$ indicates symmetric operation and (ii) non-linearity, f_{NL}, is defined as (dI/dV) / (I/V). All band diagrams were simulated using the Boise State University Band Diagram program.[17] Materials parameters used in simulations are: electron affinity (χ) = 4 eV, bandgap (E_G) = 4.3 eV and relative dielectric constant (κ) = 25 for Nb_2O_5;[18] χ = 3.75 eV, E_G = 4.5 eV and κ = 26 for Ta_2O_5.[19] The work function of the ZrCuAlNi and Al electrodes were determined to be 4.2 eV and 4.8 eV, respectively, which we have reported in previous work.[20]

4.3 Results and discussion

Shown in Fig. 4.1 are log (J) - V plots of M_1IM_2 diodes made with (a) 10 nm thick and (b) 5 nm thick layers of either Ta_2O_5 or Nb_2O_5. Plots of J-V asymmetry (η) vs. voltage and non-linearity (f_{NL}) vs. voltage for all devices are shown in Fig.1 (c) and Fig. 1(d), respectively. As expected, based on the relative barrier heights shown in the simulated energy band-diagrams insets in Fig. 4.1(a) and (b), the devices made with Nb_2O_5 show a larger current density than the devices made with Ta_2O_5. The Ta_2O_5 diodes, however, show slightly larger asymmetry. Although Ta_2O_5 and Nb_2O_5 devices demonstrate asymmetric J-V behavior with a small V_{ON}, the maximum asymmetry (η_{max}) is three orders of magnitude smaller than the η_{max} (up to 1400) which we have recently reported for diodes made the same electrode combination but with a 10 nm Al_2O_3 dielectric layer.[20] The asymmetry in M_1IM_2 tunnel diodes should be related to the work function difference between the electrodes ($\Delta\Phi = \Phi_{M1}-\Phi_{M2}$). If conduction is dominated solely by FNT, devices made with the same electrodes but different dielectrics should show the same value of η_{max}, but at different applied biases sorting by energy barrier height each dielectric makes with electrode. The poor asymmetric behavior shown in Fig. 4.1(c) suggests the dominance of non-FNT conduction mechanisms.

Besides FNT and direct tunneling, potential conduction mechanisms include Schottky emission (SE), Frenkel-Poole emission (FPE), and space-charge-limited (SCL) conduction.[21-25] In SE, conduction is limited by emission over a barrier and the current density, J, has the following relationship with electric field, E:[23,24]

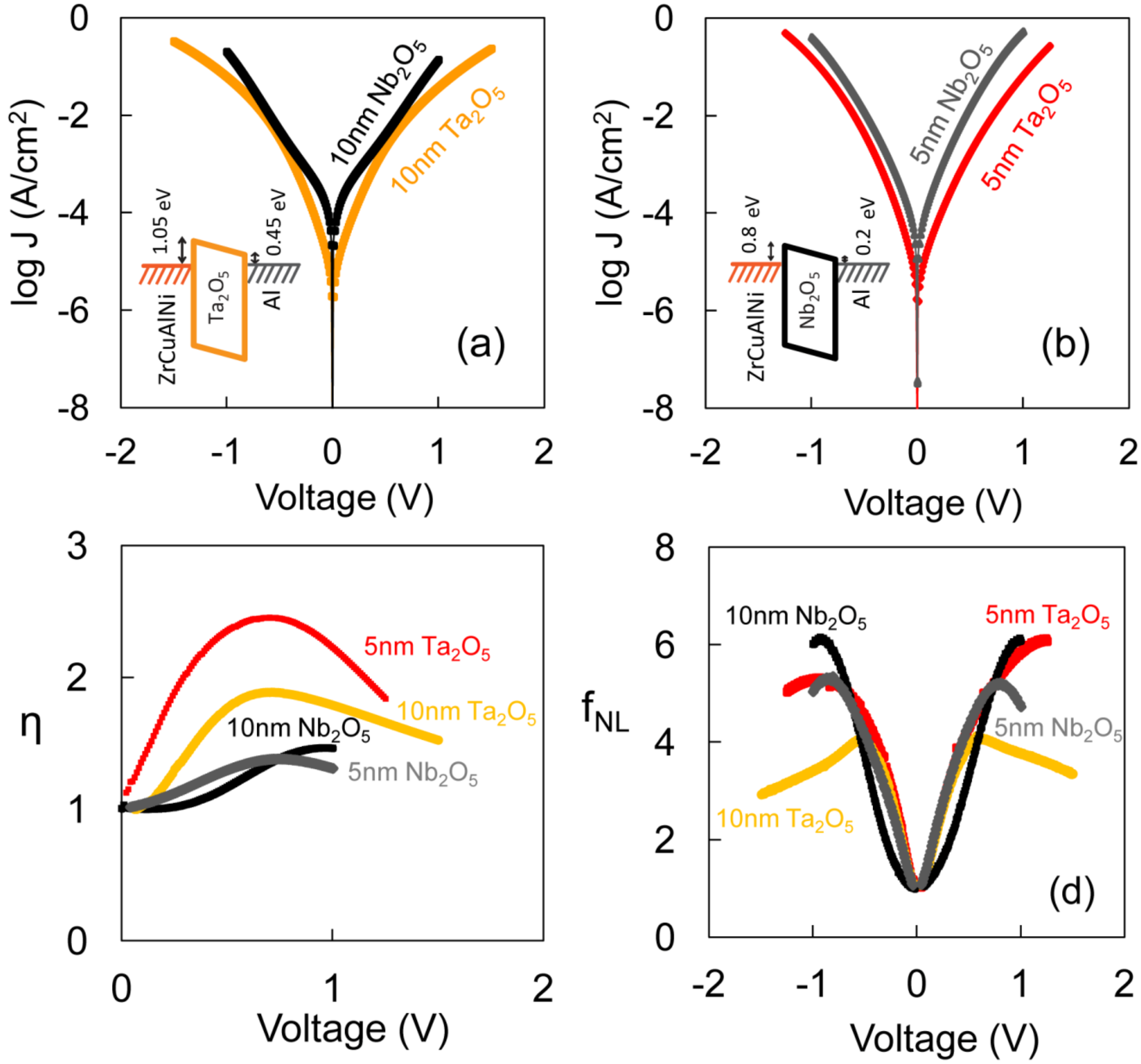

Fig. 4.1: Fig.1: Log J vs. V plots for M_1IM_2 diodes made with ZrCuAlNi bottom electrodes and Al top electrodes with (a) 10nm of Nb_2O_5 and Ta_2O_5 dielectrics, and (b) 5nm of Nb_2O_5 and Ta_2O_5 dielectrics. (c) Asymmetry (η) plots, and (d) non-linearity (f_{NL}) plots of diodes shown in (a) and (b).

$$J_{SE} = A^*T^2 \, exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/4\pi\kappa_r\epsilon_0}\right)}{kT}\right] \qquad (4.1)$$

where A^* is effective Richardson constant, T is temperature, q is elementary charge, Φ_B is the barrier height between the Fermi-level of the injecting metal, κ_r is the dynamic dielectric constant, ε_0 is the permittivity in vacuum, and k is Boltzmann's constant. For FPE, where conduction is limited by capture and emission from traps, the relationship between J and E is:[23,24]

$$J_{FPE} = E\ exp\left[\frac{-q\left(\phi_T - \sqrt{qE/\pi\kappa_r\epsilon_0}\right)}{kT}\right] \qquad (4.2)$$

where ϕ_T is the trap energy depth referenced to the conduction band edge.

To determine whether the dominant conduction mechanism is related to SE or FPE, the J-V data from Fig. 4.1(a) were replotted as ln (J_{TE}/T^2) vs. $V^{1/2}$ and ln (J_{FPE}/V) vs. $V^{1/2}$, respectively. Shown in Fig. 4.2, it was found that both the (a) Ta_2O_5 and the (b) Nb_2O_5 diodes produced linear ln (J/T^2) vs. $V^{1/2}$ curves ($R^2 > 0.999$) at both polarities in the low bias regime (0.1 V to 0.3 V), suggesting that Schottky emission dominates in the low bias regime. At higher biases (0.75 V to 1 V), also shown in Fig. 4.2, both the (c) Ta_2O_5 and (d) Nb_2O_5 diodes produced linear ln (J/V) vs. $V^{1/2}$ plots, suggesting that FPE dominates at higher biases. Note that space charge limited conduction was ruled out because J does not exhibit a V^2 dependence[26,27] and because these dielectrics are expected to exhibit high trap densities.[28,29] The change in the dominant conduction mechanism between low and high bias is in agreement with the observed asymmetry in these devices. Shown in Fig. 4.1(c), asymmetry first increases in the low bias regime where the electrode limited SE dominates and then decreases at the larger bias regime where the bulk limited FP emission dominates.

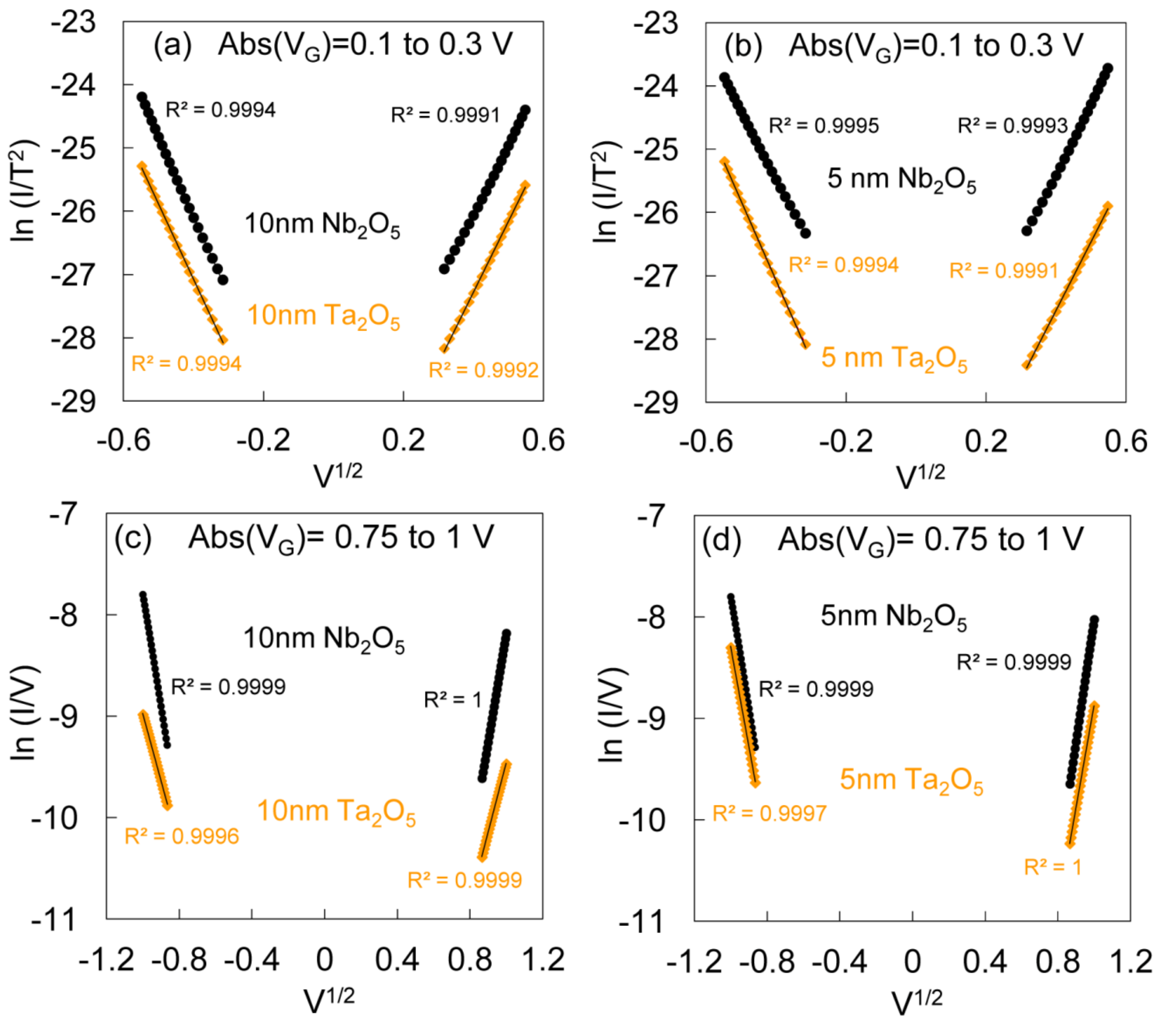

Fig. 4.2: J-V curves of 5nm and 10nm Nb_2O_5 and Ta_2O_5 fitted into conduction plots: (a) and (b) Schottky plots in the low voltage regime, and (c) and (d) Frenkel-Poole plots in the higher voltage regime show linear curves.

To further assess the validity of the conduction mechanism assignments, the relative dielectric constants, κ_r, of Nb_2O_5 and Ta_2O_5 may be extracted from the slopes of the plots in Fig. 4.2. For Nb_2O_5, $\kappa_r = 4.7 \pm 0.3$ was extracted from the SE plot in Fig. 4.2(a) and $\kappa_r = 5.5 \pm 0.1$ from FPE plot in Fig. 4.2(c). For Ta_2O_5, $\kappa_r = 4 \pm 0.3$ was extracted from the SE plot in Fig. 4.2(b) and $\kappa_r = 4.6 \pm 0.1$ from the FPE plot in Fig.

4.2(d). It is clear that all of these extracted dielectric constants are much smaller than the static dielectric constant expected for these high-κ dielectrics ($\kappa_{Ta2O5} > 20$, $\kappa_{Nb2O5} > 40$).[19,25]

Although the static or low frequency dielectric constant is sometimes considered for FPE, Frenkel used the high frequency dielectric constant to derive what is now called the Frenkel-Poole emission equation (Eqn. 2).[30] It is discussed in [28] that the dielectric constant associated with FPE current under relatively large electric field is expected to have the high frequency values as the hopping of the electrons from traps should occur in optical frequency range.[28] Ludeke *et al.* have discussed that the high frequency dielectric constant should be directly measured and compared to extracted values.[31] Finally, other researchers have also reported either the dynamic dielectric response, ε_{if}, or optical dielectric constant, ε_{∞}, for FPE in thin ALD films.[32-34] Optical dielectric constants were determined with spectroscopic ellipsomtery using 10 nm thick Nb_2O_5 and Ta_2O_5 films deposited on glass substrates. Shown in Fig. 4.3 are plots of the real part of the optical dielectric constant vs. wavelength for (a) Nb_2O_5 and (b) Ta_2O_5 films. For both Nb_2O_5 and Ta_2O_5 films, the κ_r values extracted from the FPE plots match very well with the range of values measured optically. The κ_r values extracted from the SE plots are somewhat below this range, but still match reasonably well.

To further investigate the conduction mechanisms, electrically measurements were performed over a range of temperature. Shown in Fig. 4.4 are (a) I-V, (b) η, and (c) f_{NL} plots for 10 nm Nb_2O_5 diodes along with (d) I-V, (e) η, and (f) f_{NL} plots for 10 nm

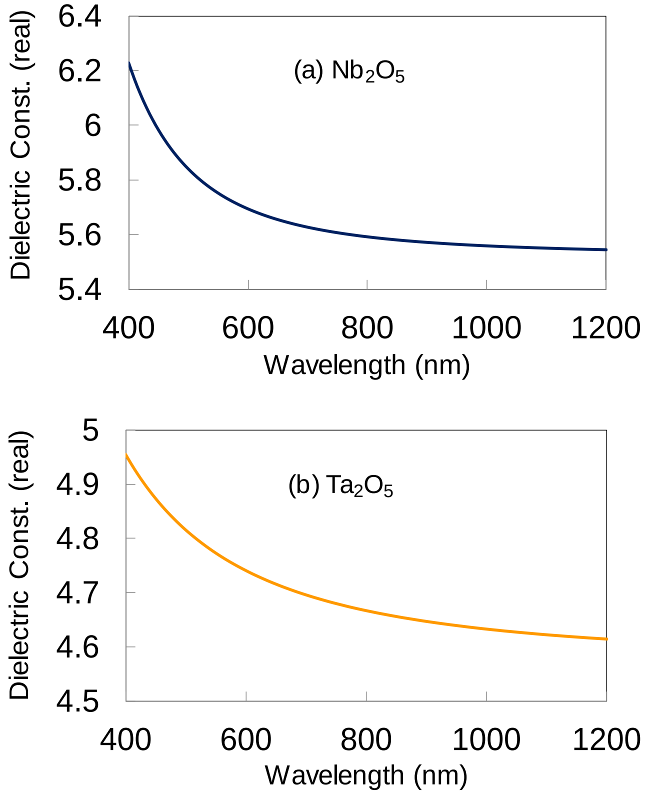

Fig.4.3: Optical dielectric constant measured by spectroscopic ellipsometry.

Ta_2O_5 diodes at temperatures ranging from 300°K to 375°K. The strong temperature dependence exhibited by the I-V characteristics of both the (a) Nb_2O_5 and (d) Ta_2O_5 devices provides additional evidence for the dominance emission mechanisms (SE and FPE) and further rules out FNT as a dominant conduction mechanism. The SE conduction (Eqn. 4.1) has a stronger temperature dependence than the FPE (Eqn. 4.2)). Therefore SE should become relatively easier than FPE as the temperature increases. Assuming both SE and FPE are present as series conduction mechanisms in the devices, this will lead to the devices becoming increasingly limited (dominated) by FPE as temperature increases. Whereas SE is dependent on the height of the barrier at the

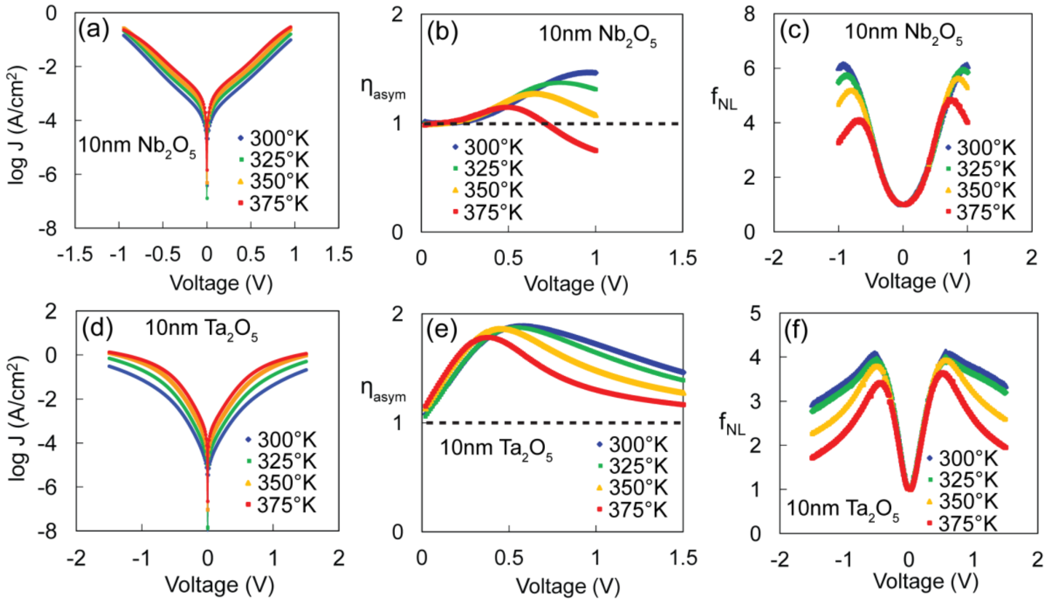

Fig.4.4: (a) Asymmetry (η) plots, and (b) non-linearity (f_{NL}) plots of 10nm Nb_2O_5 diodes at different temperatures. (c) Asymmetry (η) plots, and (d) non-linearity (f_{NL}) plots of 10nm Ta_2O_5 diodes at different temperatures.

metal/insulator interface and would be expected to be asymmetric with respect to voltage polarity for these devices, FPE is a bulk conduction mechanism and should be symmetric with respect to voltage polarity. An increased dominance of FPE with increasing temperature is consistent with the asymmetry trend observed for both the (b) Nb_2O_5 and (e) Ta_2O_5 devices, in which the maximum asymmetry, η_{max}, as well as the voltage at which η_{max} occurs is seen to decrease as temperature increases. A similar trend is observed for the f_{NL} plots for both devices.

Shown in Fig 4.5(a) are Frenkel-Poole plots of the extracted trap depth, ϕ_T, vs. the square root of the applied voltage for the large voltage region in which FPE appears to be dominant in both Nb_2O_5 and Ta_2O_5. The trap depth at each voltage, ϕ_T, was extracted from Arrhenius plots of ln(I/V) vs. 1/kT [34-36] shown in Fig 4.6 for the 10 nm thick Nb_2O_5

and Ta_2O_5 diodes. ϕ_T values are referenced to the conduction band edge of the dielectric. To account for barrier lowering of the trap depth when a field is applied across the dielectric, the zero field trap depth, ϕ_{T0}, is extracted by extrapolating the plots in Fig. 4.5(a) to V = 0. Considering first Ta_2O_5, ϕ_{T0} was determined to be 0.59 ± 0.02 eV below the conduction band edge. This value is in reasonable agreement with the ϕ_{T0} = 0.7 eV reported by Houssa *et al.* for ALD Ta_2O_5 deposited using $TaCl_5$ as the precursor.[37] The 0.1 eV difference could be due to the different ALD precursors used in the present study. Houssa *et al.* elsewhere reported ϕ_{T0} = 0.85 eV for Ta_2O_5 films deposited using metal organic chemical vapor deposition (MOCVD) precursor.[38] Recent ab-initio calculations predict an ϕ_{T0} of 0.2 eV for δ-Ta_2O_5.[39] For Nb_2O_5, the ϕ_{T0} was found to be 0.62± 0.05 eV below the conduction band. Reports on conduction mechanisms in thin film ALD Nb_2O_5 are very limited and no other trap depths could be found for comparison.

Shown in Fig. 4.5(b) are Schottky plots of the extracted metal-insulator energy barrier heights, Φ_B, vs. the square root of the applied voltage for the low voltage region in which SE appears to be dominant in both Nb_2O_5 and Ta_2O_5. The barrier height at each

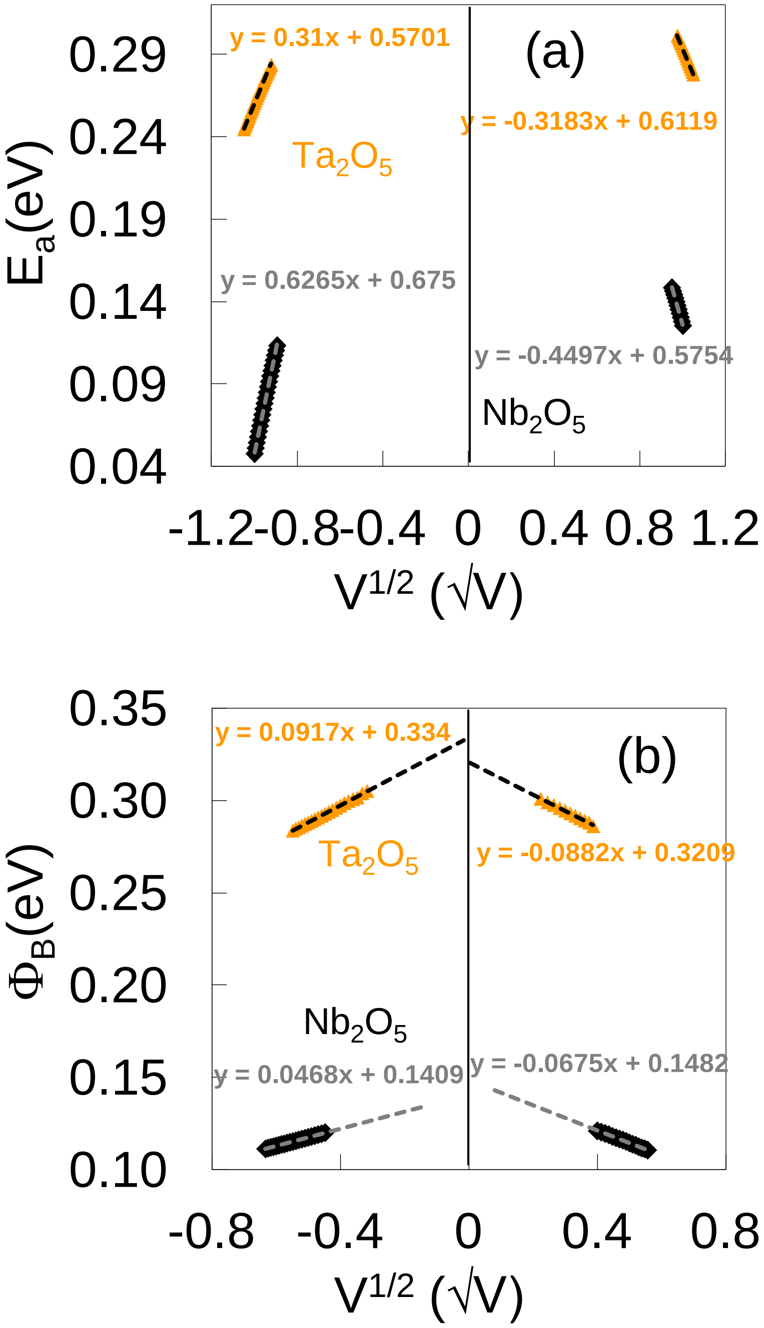

Fig.4.5: Arrhenius plots for Nb_2O_5 and Ta_2O_5 diodes. Trap energy ϕ_t is extracted by extrapolation of curves to zero bias in (a) Frenkel-Poole dominated bias regime. The energy barrier heights Φ_B is extracted by extrapolation of curves to zero bias in (b) Schottky emission dominated regime.

voltage, Φ_B, was extracted from the slope of Arrhenius plots of $\ln(I/T^2)$ vs. $1/kT$ for 10 nm thick Nb_2O_5 and Ta_2O_5 diodes. To account for Schottky barrier lowering of the barrier height when a field is applied across the dielectric, the zero field barrier height, Φ_{B0}, is extracted by extrapolating the plots in Fig. 4.5(b) to zero voltage.

Extrapolating the negative polarity curves to the zero bias point, Φ_{B0} were found to be 0.14 ± 0.02 eV for the Al-Nb_2O_5 interface and 0.33 ± 0.01 eV for Al-Ta_2O_5 interface, respectively. Both of these values are smaller than that expected based on ideal theory ($\Phi_B = \Phi_M - \chi_i$) and the limited reported values of electron affinity, χ_i, for ALD Nb_2O_5 and Ta_2O_5 (simulated band diagrams are shown in the Fig. 4.1 insets). Applying this technique to extract Φ_B is not as accurate as the similar method employed to extract ϕ_t mainly due to large non-linear influence of image force on Φ_B at different biases. However, it could serve as a lower estimate of the true Φ_B. Attempt to extract Φ_B for the ZrCuAlNi-Nb_2O_5 and the ZrCuAlNi-Ta_2O_5 interfaces resulted in unreasonably small values. We think the interfacial layer between ZrCuAlNi bottom electrode and dielectric layers which we have previously reported causes this discrepancy.[20] Zhuo et al. has also recently reported barrier height between ALD Ta_2O_5 and aluminum electrode to be approx. 0.08±0.2 due to Fermi level pining.[40] Further work is undergoing to measure barrier heights between these electrodes, and Ta_2O_5 and Nb_2O_5 ALD dielectrics.

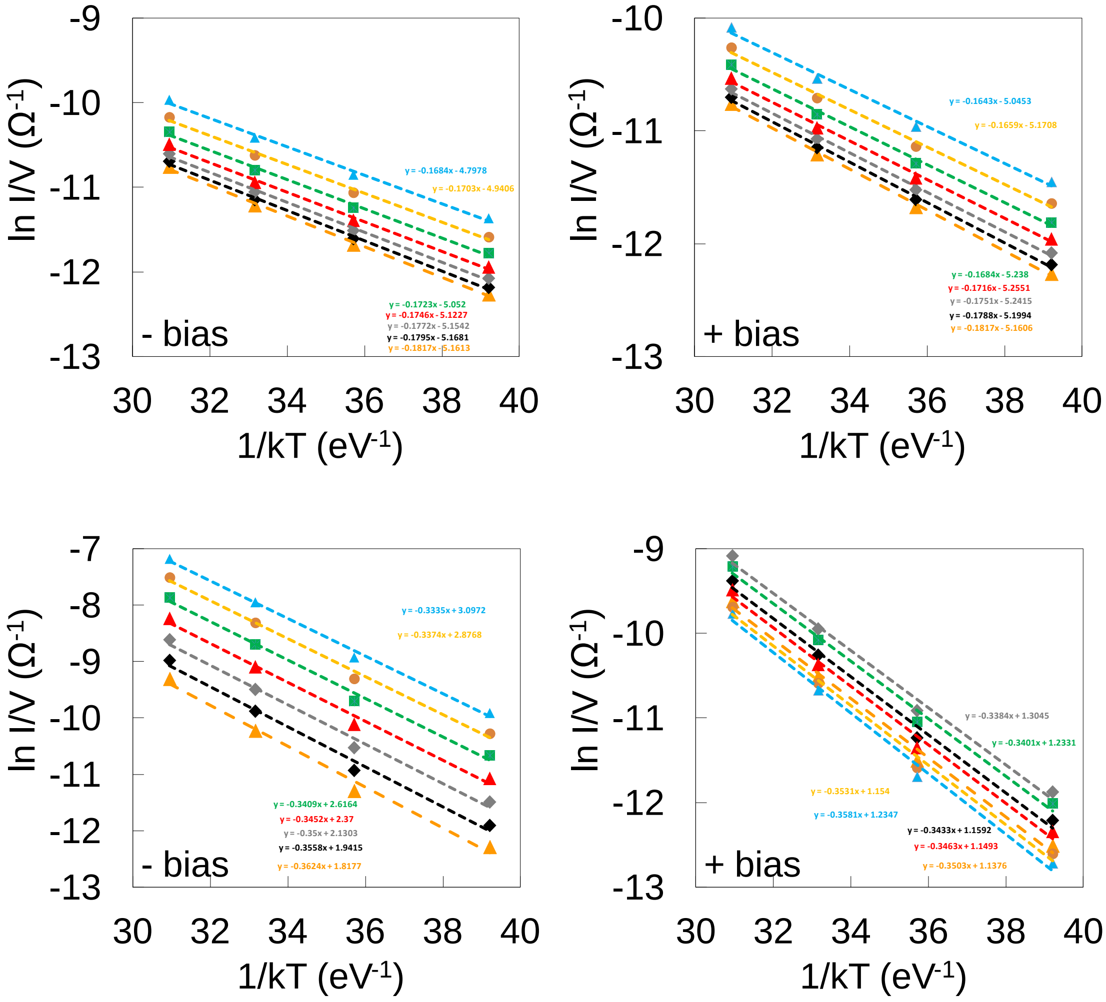

Fig.4.6: Top: Arrhenius plots to extract the activation energy (E_a) for 10nm Nb_2O_5. Bottom: Arrhenius plots to extract the activation energy (E_a) for 10nm Ta_2O_5.

4.4 Summary

In conclusion, two dielectrics, Nb_2O_5, and Ta_2O_5, with large electron affinity values as potential dielectric candidates in tunnel devices performing in low bias regimes were deposited by atomic layer deposition (ALD). Using MIM device structure with atomically smooth bottom electrodes, conduction mechanisms in these tunnel barriers were investigated by analyzing plots of current density (J) versus V, and J at different temperatures, ranging from 300° K to 375° K. It is demonstrated that although the desired conduction mechanism in MIM tunnel diodes is Fowler-Nordheim tunneling to achieve asymmetry in J-V response, tunneling is not the dominant conduction in the Nb_2O_5, and Ta_2O_5 dielectrics studied in this work. Schottky emission and Frenkel-Poole emission were found as the dominant conduction mechanisms in low bias regimes (0.1 to 0.3 V) and large bias regimes (0.75 to 1 V) for both these dielectrics; respectively. These results indicate that the choice of insulator layer is crucial in fabrication of tunnel devices and the dominant conduction mechanism should be assessed besides the formation of the energy barriers between electrodes and insulators in analyzing rectification performance of tunnel diodes at ultra high frequencies.

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CHAPTER 5

Metal-Insulator-Metal Tunnel Devices: Investigation of Dominant Conduction Mechanism in Dielectrics Deposited by Atomic Layer Deposition

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In preparation for submission

5.1 Introduction

Metal-insulator-metal (MIM) tunnel devices are recently attracting a significant attention for variety of ultra high-speed and low-power applications such as hot electron transistors,[1,2] infrared (IR) detectors,[3-5] and optical rectennas for IR energy harvesting.[6, 7] The ultra high frequency (UHF) operation regime desired in these devices requires transport of electrons between terminals as short as a few femto seconds. Quantum mechanical tunneling through an ultrathin insulator is the only means of electron transport capable of achieving this demanding high speed of operation. High quality dielectrics and smooth electrode-dielectric interfaces are critical to achieve stable operation based on tunneling.[8,9] Conduction mechanisms in tunnel diodes have been studied by many groups over the years. However, studies were affected by two main technological limitations at the time. First, studies have been mostly done on native oxides of electrodes which do not allow studying a wide range of dielectrics independent of bottom electrode. In addition, native oxides on multi crystalline metal electrodes do not show superior electrical properties due to large defect density. Second, use of crystalline bottom metal electrode can influence electron conduction through insulator layer. It has been shown that crystalline metal electrodes deposited with various advanced deposition techniques can have as deposited surface roughness many times larger than insulator layer thickness. This order of surface roughness can overwhelm work function of bottom electrodes, introduce a large amount of interface defect density, and deteriorate device yield.[8] Using amorphous bottom electrode is also important to avoid work function non-uniformity due to different crystal orientations of grains. It should be noted that tunnel diode dimension is needed to be of order of nanometers for UHF applications to avoid large capacitive delays (RC values). For the rectenna application, nano scale diodes are also required for impedance matching to integrated antennas.[10]

The classic way to achieve rectification in tunnel diodes, is through dominance of FN tunneling as conduction mechanism,[11] and the use of asymmetric work function metal electrodes to introduce different energy barriers to tunneling electrons based on polarity.[12] Very recently, we investigated a new approach to enhance rectification and have experimentally shown superior rectification properties through the use of a nanolaminate dielectric tunnel barrier in combination with asymmetric work function electrodes.[13] Periasamy et al. have recently investigated the role of the tunnel barrier on the rectification performance of MIM diodes through the energy barriers it makes with electrodes and its influence on turn-on voltage of MIM diodes.[14] It is not yet investigated that how choice of insulators can influence transport of electrons and if tunneling is the dominant conduction mechanism through promising dielectrics for use in MIM tunnel electronics.

In this work, we investigate the dominant conduction mechanism in MIM diodes fabricated with ALD deposited Nb_2O_5, Ta_2O_5, ZrO_2, HfO_2, Al_2O_3, and SiO_2. Depositing high quality and pinhole free insulator layers with atomic scale thickness accuracy and choice of insulator layer independent of bottom electrode can be achieved by ALD. These dielectrics are selected based on having a wide range of band-gaps and electron affinities. Dielectrics with large electron affinity such as Nb_2O_5 and Ta_2O_5 are potential candidate for rectenna applications as rectenna works in very low bias regime. A dielectric thickness of 10nm is chosen to be able to distinguish FN tunneling conduction from other conduction mechanisms because 10nm dielectric is thick enough to suppress direct tunneling to occur while other conduction mechanisms could contribute to conduction at low applied voltage. All as deposited ALD films were determined to be amorphous. Devices are studied without annealing treatments to avoid any possibility of crystallization of both ALD films and ZrCuAlNi amorphous bottom electrode. Crystalline phases in dielectric films may create conduction paths for electrons and thus facilitates defect-induced currents.[15] Crystallization of bottom electrode causes electrode surface roughness which generates field enhancement and large defect density at insulator-electrode interface.[8] An asymmetric electrode M_1IM_2 device structure is chosen due to two main reasons. First, different electrode-insulator interfaces are formed so interfacial induced leakage current could be distinguished by comparison of current response in different polarities. Second, ZrCuAlNi amorphous bottom electrode is deposited by DC magnetron sputtering. If ZrCuAlNi is also used as the top electrode, the high energetic species introduced to dielectric surface during sputtering could easily penetrate into dielectric layer and damage it. In fact, we have previously showed high trap density, evidenced by large hysteresis in J-V curves, at top electrode-insulator interface for diodes made with ZrCuAlNi top and bottom electrodes.[9] In case of diodes made with 3 nanometers dielectric layer, sputtering ZrCuAlNi top electrode produced electrically shorted devices.

5.2 Experiment

MIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. A 150 nm thick ZCAN bottom electrode was deposited directly on the SiO_2 via DC magnetron sputtering using a $Zr_{40}Cu_{35}Al_{15}Ni_{10}$ metal target. ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively. Next, thin oxide tunnel barriers were deposited via ALD using a Picosun SUNALE R-150B. Niobium ethoxide, tantalum ethoxide, tetrakis (ethylmethylamino) zirconium (TDMAZr), tetrakis (ethylmethylamino) hafnium (TDMAHf), and trimethylaluminum (TMA) were used as the metal precursors for Nb_2O_5, Ta_2O_5, ZrO_2, HfO_2, and Al_2O_3, respectively. The ALD films were deposited at a chamber temperature of 250 ºC using deionized water as the oxidant. 10nm SiO_2 films were deposited in Cambridge NanoTech Fiji PEALD tool using Tris (dimethylamino) silane ($[(CH_3)_2N]_3SiH$) Bis(T-Butylamino) Silane (BTBAS) and an O_2 remote plasam at a substarte temperature of 250 ºC. Finally, top electrodes were formed by evaporating Al dots (~0.8 mm^2) through a shadow mask. Insulator thickness on Si was measured with a J.A. Woollam WVASE32 spectroscopic ellipsometer using a Cauchy model. Metal workfunctions (Φ_M) were measured in air using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip and calibrated against a gold standard. Φ_{ZCAN} was measured to be approximately 4.8 eV. $\Delta\Phi$ ($\Phi_{ZCAN} - \Phi_{Al}$) was measured to be approximately 0.6 eV, confirmed by extraction from the slope of Fowler-Nordheim (FN) plots. I-V analysis was conducted at room temperature on a probe station in a dark box using an Agilent 4156C semiconductor parameter analyzer; the noise floor of this system is estimated to be on the order of 10^2 pA. The ZCAN bottom electrode (M_1) was always held at ground with bias applied to the Al top gate (M_2). To mitigate the impact of displacement current, all I-V curves were swept from zero bias to either the maximum positive or negative bias.

All band diagrams were simulated using the Boise State University Band Diagram program,[16] with the ZCAN electrode at ground and voltage applied to the top Al electrode (consistent with the electrical measurements). Materials parameters used in simulations are: electron affinity (χ) = 3.75 eV, band-gap (E_G) = 4.5 eV and relative dielectric constant (κ) = 26 for Ta_2O_5; χ = 4 eV, E_G = 4.35 eV and κ = 25 for Nb_2O_5; χ = 2.75 eV, E_G = 5.7 eV and κ = 25 for ZrO_2; χ = 2.5 eV, E_G = 5.8 eV and κ = 18 for HfO_2; χ = 1.3 eV, E_G = 6.4 eV and κ = 7.6 for Al_2O_3; and χ = 0.95 eV, E_G = 8.9 eV and κ = 3.9 for SiO_2. Two key figures of merit are defined to characterize the devices. First, I-V asymmetry, η, is defined as negative device current divided by positive current $|I_- / I_+|$ so that $\eta = 1$ indicates symmetric operation. Second, non-linearity, f_{NL}, is defined as (dI/dV) / (I/V).

5.3 Results and discussion

The I-V behavior of M_1IM_2 diodes is first investigated. Fig.5.1(a) shows log (J)-V plots of M_1IM_2 diodes made with 10nm of either SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, and Nb_2O_5. In Fig. 1(b), simulated energy band-diagrams of these dielectrics in conjunction with ZrCuAlNi and Al electrodes are illustrated. Simulations are performed based on reported values for ALD dielectrics deposited using the same precursors and process temperature. Looking at J-V curves in Fig.1(a), regarding energy band-diagrams; it is

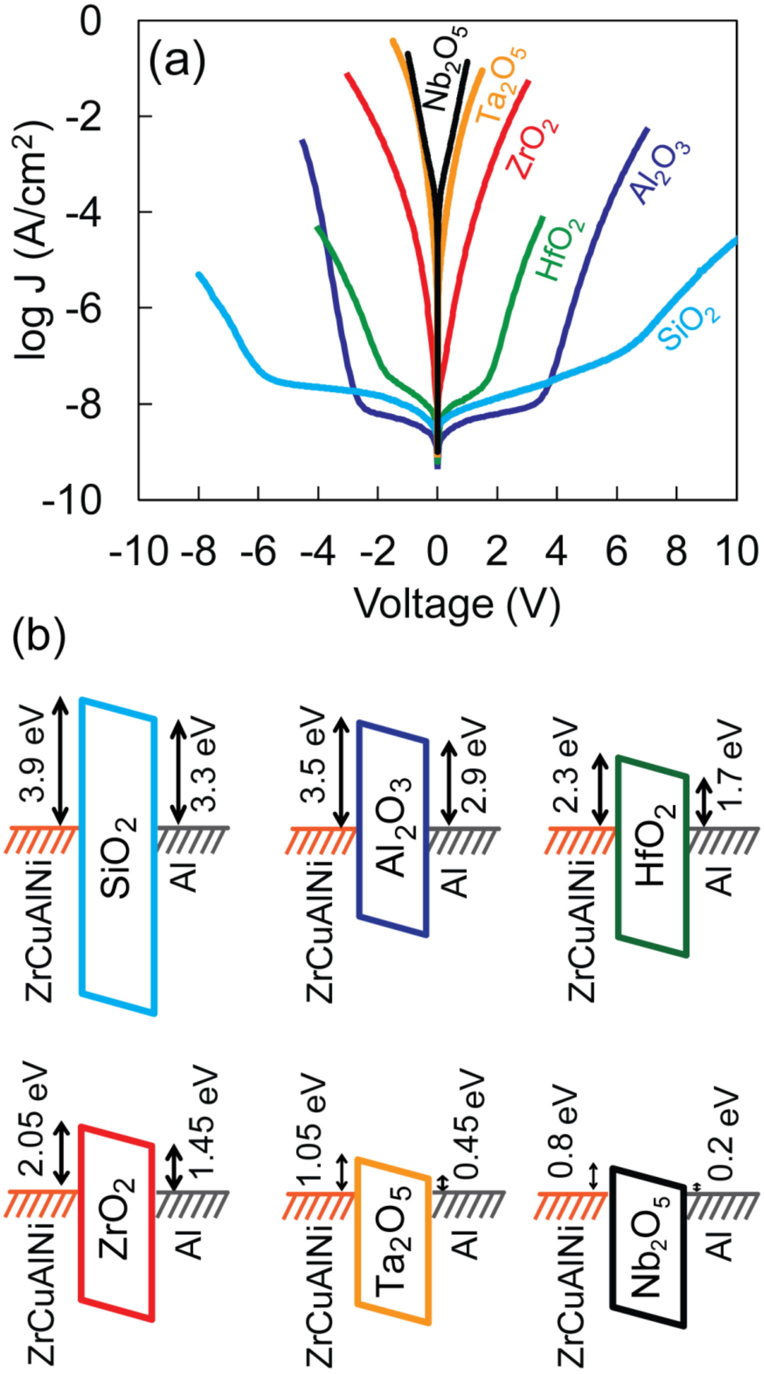

Fig. 5.1: (a) Plots of log (J) vs. V, for M_1IM_2 diodes made on ZrCuAlNi bottom electrodes with 10 nm of SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, and Nb_2O_5 ALD dielectrics and Al top electrodes. (b) Simulated band diagrams illustrating SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, and Nb_2O_5 MIM diodes in equilibrium bias condition.

evident that J-V response of devices is related very well to the height of the energy barriers these dielectrics make with the electrodes. It is seen that SiO_2, Al_2O_3, and HfO_2 diodes show a distinct knee at large electric field. This is an indication of an electric field dependent change in conduction mechanism. Following the appearance of the knee, the current response in these devices increases exponentially for about four orders of magnitude with a subtle increase in applied bias. The knees could be realized through FN tunneling. First, they occur at large applied bias regarding the barrier height of the diode, following with the breakdown of the devices after roughly a 2MV/cm rise of the applied electric field. Second, the appearance of a knee can be sorted regarding the energy barrier heights in diodes. In other words, the HfO_2 diodes which make the smaller energy barrier with electrodes, show knees in J-V curve at smaller bias, and the Al_2O_3 diodes with larger energy barrier display knees at larger bias. On the other hand, ZrO_2, Ta_2O_5, and Nb_2O_5 diodes do not show any knee in their current response. This difference could be explained due to the smaller energy barriers these dielectrics make which cause the onset of FN tunneling at lower bias range. However, a closer look specifically at the ZrO_2 diode which should form energy barriers very close to HfO_2 diode does not reveal any knee even at very small biases. Also, ZrO_2, Ta_2O_5, and Nb_2O_5 diodes show large leakage current at very low bias range as soon as electric field is applied.

Identification of the dominant conduction mechanisms at medium and large electric fields is typically performed by fitting J-V curves into Frenkel-Poole and tunneling plots.[17, 18] Conduction in MIM diodes is initially investigated through fitting of the room temperature J-V response. In Fig. 5.2, J-V curves of devices shown in Fig. 5.1

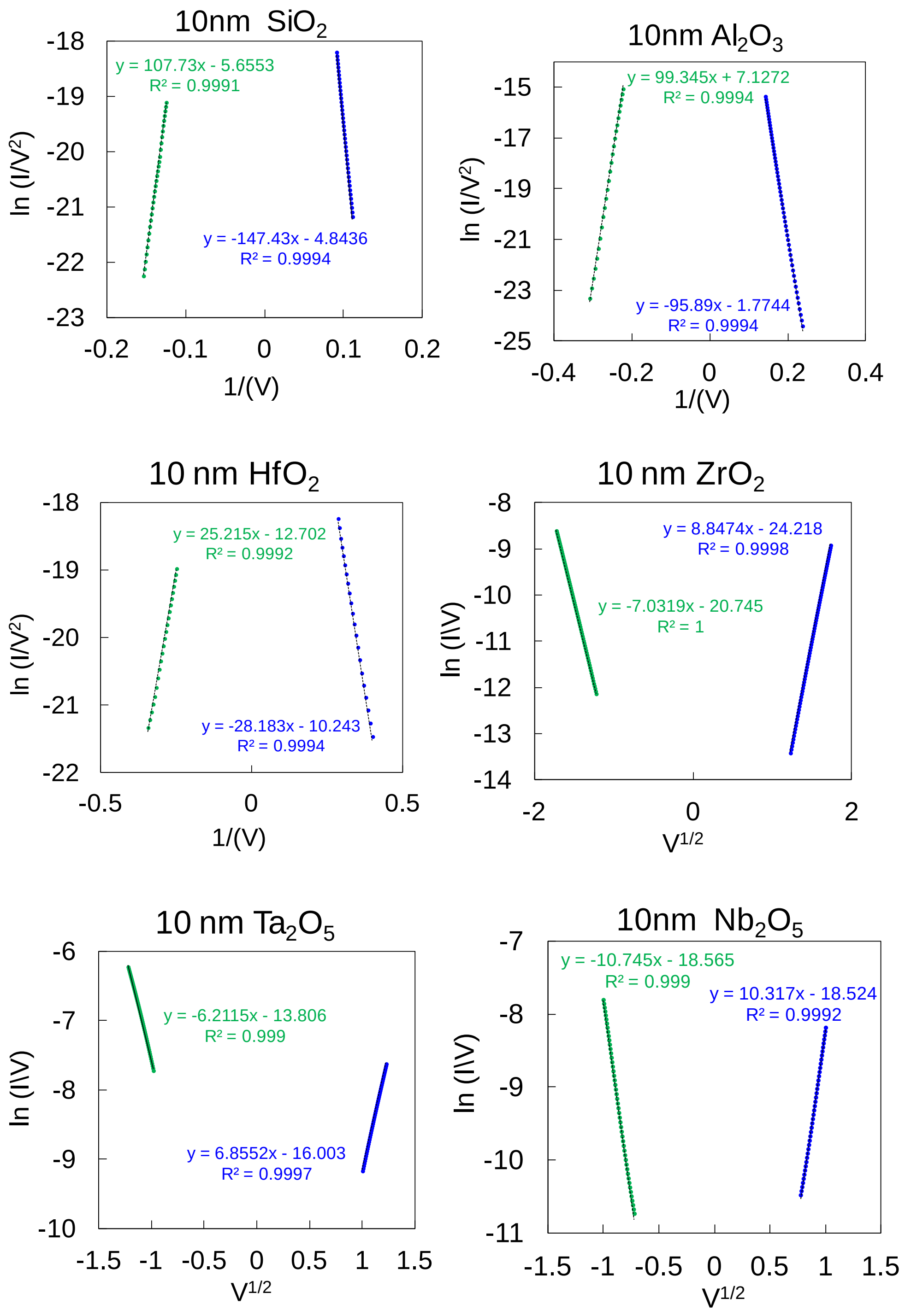

Fig. 5.2: Data shown in Fig. 5.1 is fitted into tunneling plots (ln (I/V^2) vs. V) and emission plots (ln (I/V^2) vs. $V^{1/2}$) to determine the dominant conduction mechanisms in different ALD dielectrics. Green and blue curves are representing negative and positive polarities respectively.

are fitted into conduction plots. Only plots showing well fitted curves are included in Fig. 5.2. the data is shown in the plot which is fitted well. J-V plots for SiO_2, Al_2O_3, and HfO_2 are fitted into ln (I/V^2) vs. V (tunneling plots), and ln (I/V^2) vs. $V^{1/2}$ (Frenkel-Poole plots), after the occurrence of the knee. As there is no knee in J-V plots of ZrO_2, Ta_2O_5, and Nb_2O_5 diodes, their J-V curves over the last four orders of magnitude increase in current response are analyzed. It can be seen that SiO_2, Al_2O_3, and HfO_2 produce highly linear curves in tunneling plots with R^2 value larger than 0.999. Whereas, ZrO_2, Ta_2O_5, and Nb_2O_5 diodes linearly fit in FP plots. This is representing tunneling as dominant conduction mechanism in SiO_2, Al_2O_3, and HfO_2, and FP emission as dominant conduction mechanism in ZrO_2, Ta_2O_5, and Nb_2O_5 diodes. This observation is in good agreement with previous studies performed on SiO_2,[18,19] Al_2O_3,[20, 21] HfO_2,[22, 23] ZrO_2, [24, 25]Ta_2O_5, [26, 27]and Nb_2O_5 [28, 29] ALD dielectrics. However studying conduction in thin film dielectrics solely based on J-V data acquired in room temperature can often produce misleading results. A more accurate way to investigate conduction in ultra thin dielectrics is accomplished by examining J-V behavior at different temperatures. J-V response of devices are measured at 300, 325, 350, and 375 K. Fig. 4 demonstrates temperature dependence of diodes.

Finally, it should be noted that ALD films are very sensitive to process parameters. Fully optimized deposition recipes would lead to ALD films with smaller defect densities. Utmost attention has been paid in process development employed to deposit ALD films studied in this work; however, there are always promises to use more adjusted deposition recipes and better precursor chemistries. Specifically in case of ZrO_2,

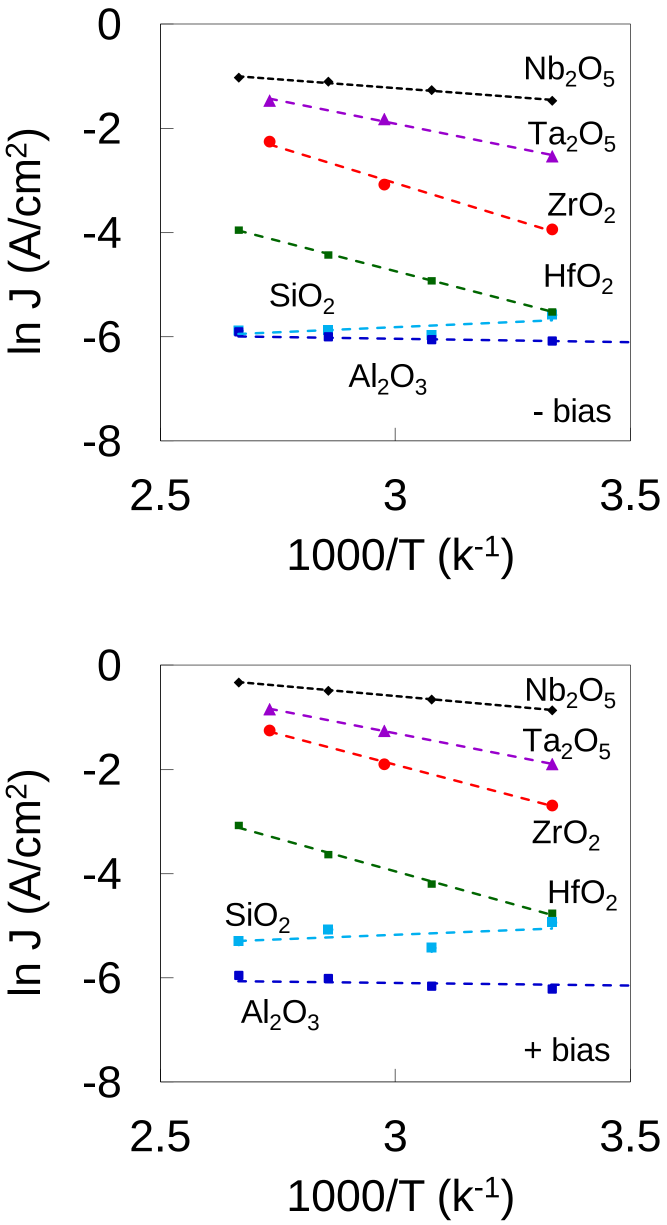

Fig. 5.3: Temperature dependence of current response for M_1IM_2 diodes made with with 10nm of either SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, or Nb_2O_5. Diode current responses under positive applied bias (electron injection from ZrCuAlNi bottom electrode) and negative applied bias (electron injection from Al top electrode) are shown in top and bottom plots respectively. Applied bias has chosen to be large enough so diodes are on (current density larger than 1 μ Amp/cm^2) in each measurement.

Ta_2O_5, and Nb_2O_5 dielectrics, developing better precursors and immaculate ALD processes could lead to formation of fewer defects in the bulk of films which could eventually transform itself to less contribution of defect based conduction currents.

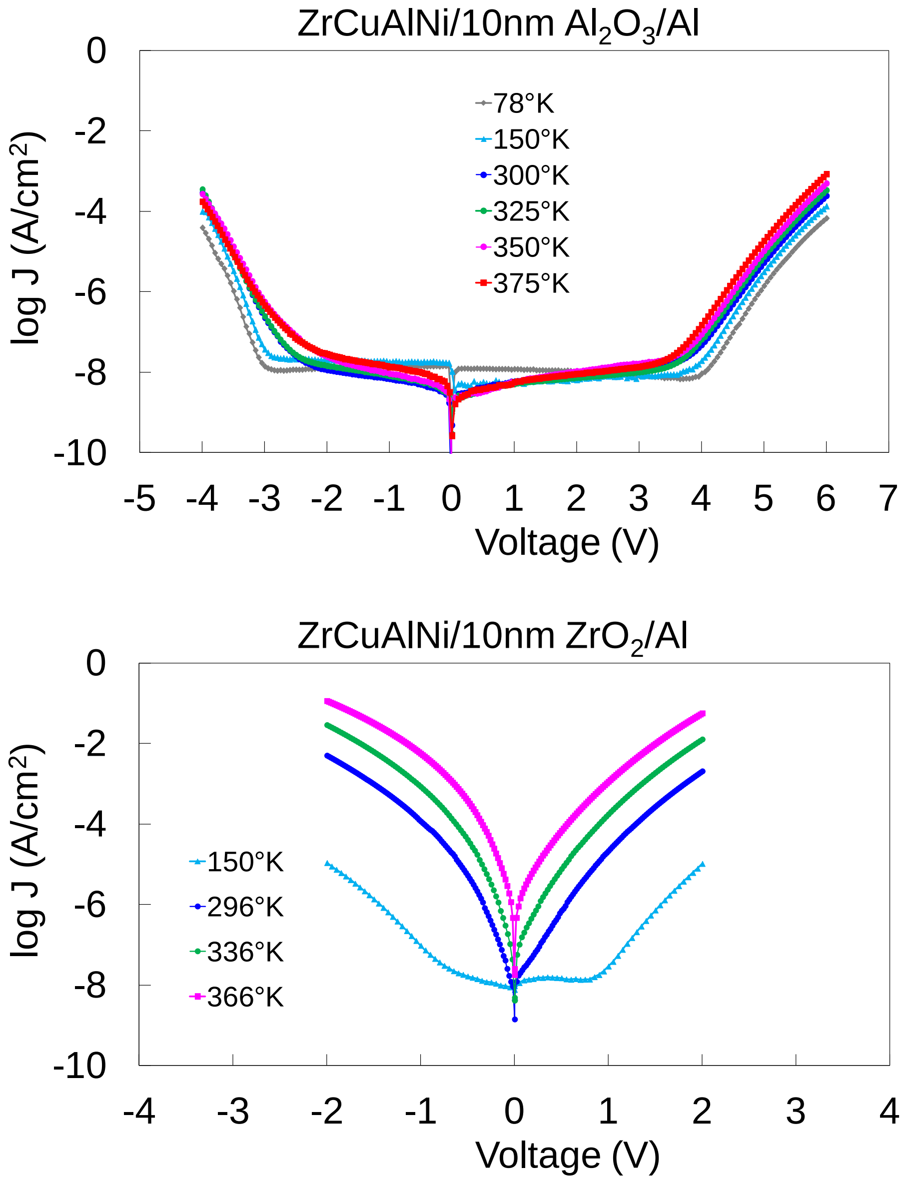

Fig. 5.4: Plots of current density (J) vs. V at different temperatures, ranging from 78° K to 375° K, for M_1IM_2 diodes made with ZrCuAlNi bottom electrodes, Al top electrodes, and either 10nm Al_2O_3 (top) or ZrO_2 (bottom).

5.4 Summary

In conclusion, a wide range of dielectrics (Nb_2O_5, Ta_2O_5, ZrO_2, HfO_2, Al_2O_3, and SiO_2) was deposited by atomic layer deposition (ALD) as the tunnel barrier in metal-insulator-metal (MIM) tunnel devices. Using MIM device structure with atomically smooth amorphous ZrCuAlNi bottom electrodes and Al top electrodes, conduction mechanisms in these tunnel barriers are investigated by analyzing plots of current density (J) versus V, and J at different temperatures, ranging from 78° K to 375° K. It is demonstrated that dominant conduction mechanism in the large bias regime in devices with less than 10nm tunnel barrier is not necessarily tunneling regardless of the choice of the insulator. Although the desired conduction mechanism in the majority of tunnel devices such as MIM diodes is Fowler-Nordheim (FN) tunneling to achieve asymmetry in J-V response, tunneling is dominant conduction only in the Al_2O_3, SiO_2, and HfO_2 dielectrics studied in this work. These results indicate that the choice of insulator layer is crucial in fabrication of tunnel devices and the dominant conduction mechanism should be assessed besides the formation of the energy barriers between electrodes and insulators in analyzing rectification performance of tunnel diodes at ultra high frequencies.

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CHAPTER 6

Step Tunneling Enhanced Asymmetry in Asymmetric Electrode Metal-Insulator-Insulator-Metal Tunnel Diodes

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6.1 Introduction

Thin film metal-insulator-metal (MIM) tunnel devices have seen renewed interest for high speed applications[1-3] such as infrared (IR) detectors,[4-6] optical rectennas for IR energy harvesting,[7-9] and hot electron transistors,[10] as well as for macroelectronic applications such as backplanes for liquid-crystal displays (LCDs).[11,12] For many of these applications, highly asymmetric and non-linear current vs. voltage (I-V) behavior at low applied voltages is desired. The standard approach to achieving asymmetric I-V characteristics in tunnel devices is to use metal electrodes with different workfunctions (Φ_M) to make M_1IM_2 diodes where $\Phi_{M1} \neq \Phi_{M2}$, to produce a built-in voltage, $V_{bi} = (\Phi_{M1} - \Phi_{M2})/e$ (where e is the electronic charge) across the tunnel barrier.[13,14] However, the amount of asymmetry achievable using this approach is limited by the $\Delta\Phi_M$ that can be obtained using practical electrodes. An alternative approach to achieving asymmetric and non-linear operation involves engineering of the tunnel barrier so that electrons tunneling from one metal electrode to the other are presented with a different barrier shape depending on the direction of tunneling/applied bias polarity.[15] Formation of an asymmetric tunnel barrier can be accomplished using nanolaminate pairs of insulators, each having different band-gaps and band-offsets, to produce metal-insulator-insulator-metal (MIIM) devices. Very recent work has shown that insulator heterojunctions can be used to produce asymmetric I-V behavior in symmetric metal electrode $M_1I_1I_2M_1$ diodes.[16-18] It has not been shown whether a bilayer insulator tunnel barrier can be combined with asymmetric workfunction metal electrodes to produce $M_1I_1I_2M_2$ diodes with superior I-V asymmetry. In addition, whereas asymmetry due to resonant tunneling has been studied, asymmetry due to step tunneling, a step reduction in tunnel distance in a bilayer insulator tunnel barrier, has not yet been experimentally demonstrated. In this work, we investigate the combined effect of bilayer tunnel barriers and asymmetric electrodes in $M_1I_1I_2M_2$ tunnel diodes.

Much previous work on MIM diodes has focused on native oxides of rough polycrystalline metals.[1-7,14,16,18,19] We recently showed that roughness at the bottom metal-insulator interface can dominate the I-V behavior of MIM diodes and that the use of atomically smooth bottom electrodes combined with high quality insulators deposited via atomic layer deposition (ALD) allowed for fabrication of high quality MIM diodes with well controlled quantum mechanical tunneling.[20,21] Therefore, we fabricate M_1IIM_2 diodes using smooth amorphous metal ZrCuAlNi (ZCAN) bottom electrodes [22] and nanolaminate insulator bilayers of HfO_2 and Al_2O_3 deposited via ALD. We demonstrate that bilayer insulator tunnel barriers enable tuning of the current vs. voltage (I-V) asymmetry and non-linearity via a step reduction in the minimum tunnel distance at the applied bias at which tunneling may begin to occur through only the wider band-gap insulator layer. We find that I-V asymmetry and non-linearity are sensitive to the arrangement of the individual insulator layers with respect to the larger and smaller workfunction electrodes (e.g. $M_1I_1I_2M_2$ vs. $M_1I_2I_1M_2$) and that bilayer tunnel insulators can be arranged to enhance or oppose the built in asymmetry of the asymmetric workfunction electrodes.

6.2 Experiment

MIM and MIIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. A 150 nm thick ZCAN bottom electrode was deposited directly on the SiO_2 via DC magnetron sputtering using a $Zr_{40}Cu_{35}Al_{15}Ni_{10}$ metal target. ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively. Next, thin oxide tunnel barriers were deposited via ALD using a Picosun SUNALE R-150B. Trimethylaluminum (TMA) and tetrakis (ethylmethylamino) hafnium (TDMAHf) were used as the metal precursors for Al_2O_3 and HfO_2, respectively. All ALD films were deposited at a chamber temperature of 250 ºC using deionized water as the oxidant. Nanolaminate bilayer barriers were deposited in one continuous run without breaking vacuum. Finally, top electrodes were formed by evaporating Al dots (~0.8 mm^2) through a shadow mask. Insulator thickness on Si was measured with a J.A. Woollam WVASE32 spectroscopic ellipsometer using a Cauchy model. Transmission electron microscopy (TEM) images were taken on a FEI Titan 80-200 using samples prepared with a Quanta 3D Dual Beam focused ion beam. Metal workfunctions (Φ_M) were measured in air using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip and calibrated against a gold standard. Φ_{ZCAN} was measured to be approximately 4.8 eV. $\Delta\Phi$ ($\Phi_{ZCAN} - \Phi_{Al}$) was measured to be approximately 0.6 eV, confirmed by extraction from the slope of Fowler-Nordheim (FN) plots. I-V analysis was conducted at room temperature on a probe station in a dark box using an Agilent 4156C semiconductor parameter analyzer; the noise floor of this system is estimated to be on the order of 10^2 pA. As shown in the schematic device cross section inset in Fig. 6.1(a), the ZCAN bottom electrode (M_1) was always held at ground with bias applied to the Al top gate (M_2). To mitigate the impact of displacement current, all I-V curves were swept from zero bias to either the maximum positive or negative bias.

Two key figures of merit are defined to characterize the devices. First, I-V asymmetry, η, is defined as negative device current divided by positive current $|I_- / I_+|$ so that $\eta = 1$ indicates symmetric operation. Second, non-linearity, f_{NL}, is defined as (dI/dV) / (I/V). All band diagrams were simulated using the Boise State University Band Diagram program.[23] Materials parameters used in simulations are consistent with values reported for similar ALD films: electron affinity (χ) = 1.3 eV, bandgap (E_G) = 6.4 eV and relative dielectric constant (κ) = 7.6 for Al_2O_3; $\chi = 2.5$ eV, $E_G = 5.8$ eV and $\kappa = 18$ for HfO_2; and $\Phi_{Al} = 4.2$ eV.

6.3 Results and discussion

The behavior of the individual insulators was first measured in single layer MIM diodes. Shown in Fig. 6.1 are plots of (a) log (J) vs. V and (b) log (η) vs. V for M_1IM_2 diodes where the bottom electrode M_1 is ZCAN, the top electrode M_2 is Al, and I is an approximately 3.5 nm or 10 nm thick single layer of either Al_2O_3 or HfO_2. As expected, the total current flow in Fig. 6.1(a) is a rough function of the relative barrier heights (see band diagrams shown as inset in Fig. 6.1(b)). In Fig. 6.1(a) the dominance of FN tunneling is apparent from the presence of the "knees" in the log (J) – V data at positive and negative bias which are followed by several orders of magnitude of exponentially increasing current. Not shown, FN plots of ln $(I/(V+\Delta\Phi)^2)$ vs. $1/(V+\Delta\Phi)$ confirm that

Al_2O_3 and HfO_2 devices are dominated by FN tunneling in the post turn on regime.[13] Due to the asymmetric workfunction electrodes, the devices are expected to show asymmetry. In Fig. 6.1(b), it is seen that the 10 nm Al_2O_3 diode shows a maximum η (η_{max}) of approximately 1350 at 4.1 V. Although the Al_2O_3 devices show excellent η at higher biases, asymmetric operation at low voltage is desirable for many applications, including energy harvesting. As seen in Fig. 6.1(b), decreasing the tunnel barrier thickness to 3.5 nm resulted in decreased turn on voltages and increased current. However η_{max} was not improved, most likely due to the increased influence of direct tunneling. Since decreasing the dielectric thickness in a single layer MIM diode does not improve asymmetry, another strategy is required.

Shown in Fig. 6.2 are cross sectional TEM images of ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ devices in (a) and (c), and ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ devices in (b). For each insulator bilayer, 56 ALD cycles were used to deposit Al_2O_3 and 65 cycles were used to deposit HfO_2, targeting a thickness of 5 nm for each layer. The TEM images in (a) and (b) reveal that while the top insulator layer is indeed approximately 5 nm thick, in each case the insulator layer deposited directly on the ZCAN bottom electrode is only approximately 3.5 nm thick. The reduced thickness is due to an inhibition of the ALD nucleation rate on ZCAN as compared to that on oxide. Also visible in the high resolution TEM images is the presence of an approximately 2 nm thick interfacial layer (IL) between the ZCAN and the insulator. This layer was previously determined to be composed of ZrO_x.[22] Fig. 6.2(c) is a lower magnification image of the device from (a), revealing the smooth nature of the ZCAN / Al_2O_3 border over an extended range. We previously found that a smooth interface is critical to achieving high yield, high quality MIM tunnel devices.[20,21]

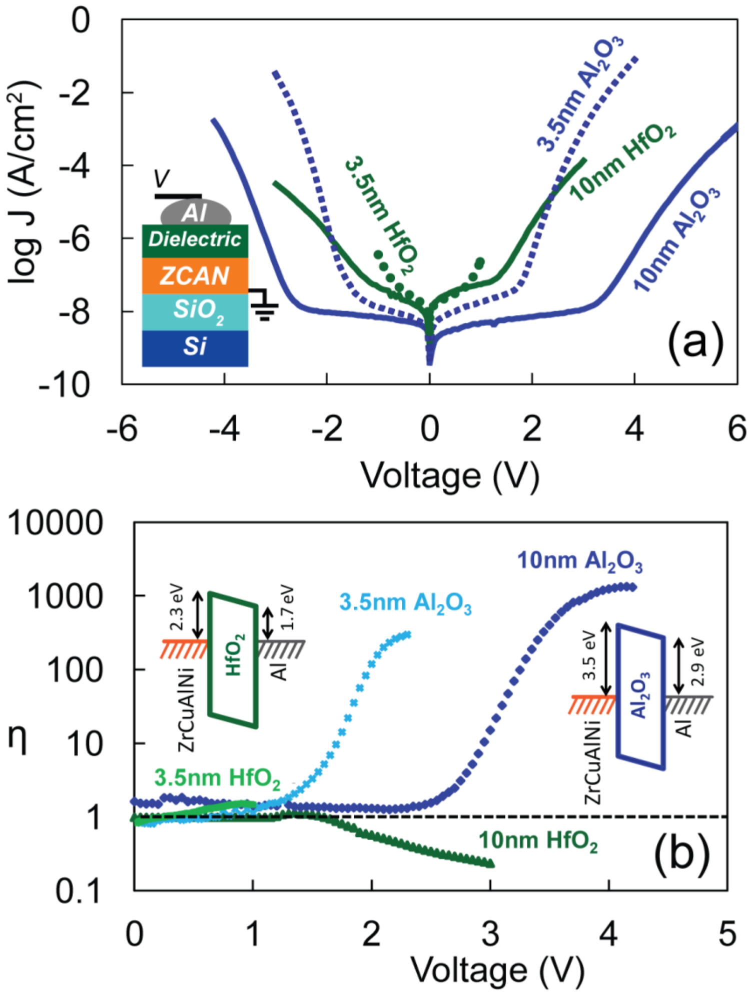

Fig. 6.1: Plots of (a) log (J) vs. V and (b) log(η) vs. V for single insulator MIM devices. Inset in (a) show a schematic device cross section. Inset in (b) shows equilibrium band diagrams.

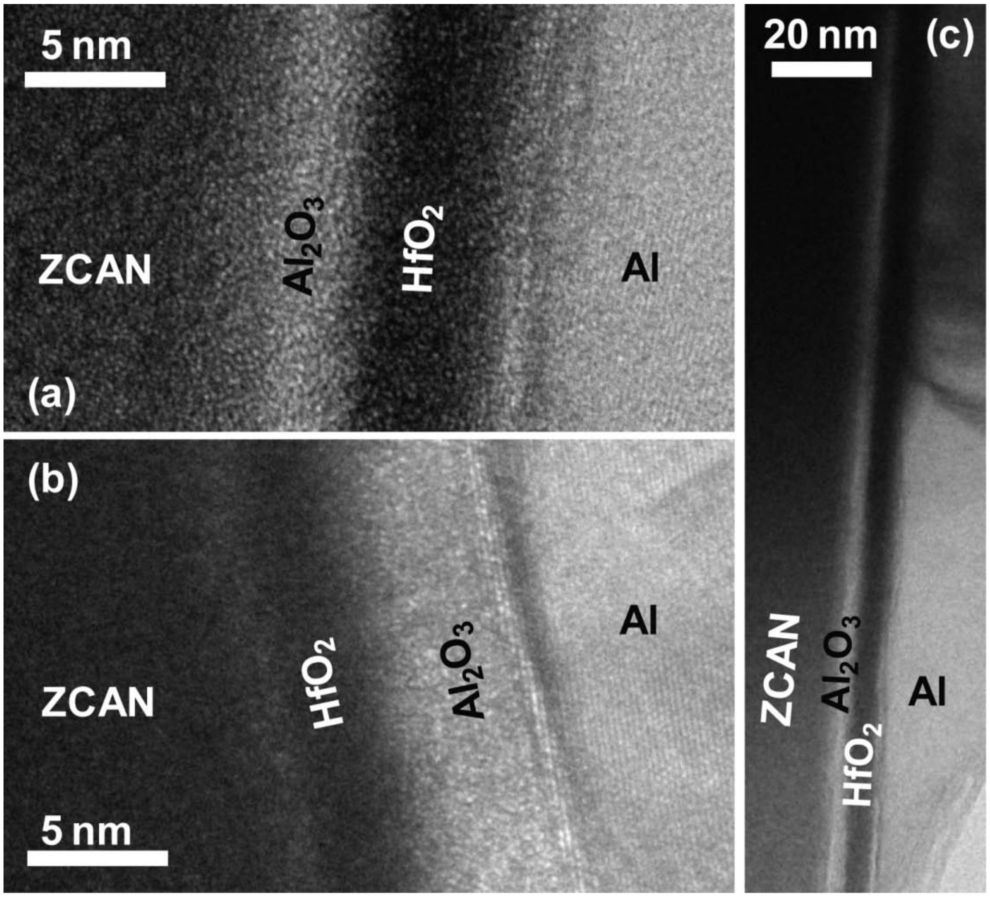

Fig. 6.2: Cross sectional TEM images of (a) and (c) ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ devices and (b) a ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ device. In each device, 56 ALD cycles were used to deposit Al_2O_3 and 65 cycles were used to deposit HfO_2.

Shown in Fig. 6.3 are (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V plots for ZCAN/3.5nm Al_2O_3/5nm HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/3.5nm HfO_2/5nm Al_2O_3/Al $M_1I_2I_1M_2$ diodes. For reference, also shown are the 10 nm thick single insulator Al_2O_3 and HfO_2 M_1IM_2 diodes from Fig. 6.1. The inherent asymmetry of the bilayer insulator barriers is evident in the equilibrium band diagrams shown in Fig. 6.3(d) and Fig. 6.3(e). Differences in the I-V and η characteristics are qualitatively explained by the band diagrams which illustrate the approximate onset of step tunneling, tunneling through only the wider band-gap Al_2O_3 layer, at positive and negative bias.

First we consider the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is adjacent to the larger workfunction ZCAN electrode. Application of approximately +3.1 V (Fig. 6.3(d), right) should bring the Fermi level of the ZCAN to just above the conduction band of the HfO_2 so that direct tunneling may occur through only the 3.5 nm thick Al_2O_3 layer, a step reduction in the required tunnel distance. For application of an opposite polarity -3.1 V bias (Fig. 6.3(d), left) electrons tunneling at the Fermi level must pass through both insulating layers. A larger current is thus expected at positive bias than at an equivalent magnitude negative applied bias so that $\eta < 1$ is expected. This is observed in Fig. 6.3(b). Note that the polarity of the asymmetry ($\eta < 1$) is reverse that of the single Al_2O_3 layer ($\eta > 1$), indicating that the asymmetry of the bilayer insulator barrier not only *opposes* that of the built-in voltage induced by the metal workfunction asymmetry ($\Delta\Phi$), but overwhelms its impact on device operation. Tunnel current is exponentially inversely dependent upon the barrier height ($I \propto \exp(\varphi_b^{-3/2})$).[13] Since $\varphi_{Al-HfO2} < \varphi_{ZCAN-Al2O3}$, for application of higher magnitude biases the negative bias current will begin to increase more rapidly than the positive bias current and it is expected that the slope of the η-V plot will decrease.[13] In Fig. 6.3(b) it is seen that for application of 4 V bias, the slope of the η-V plot has decreased.

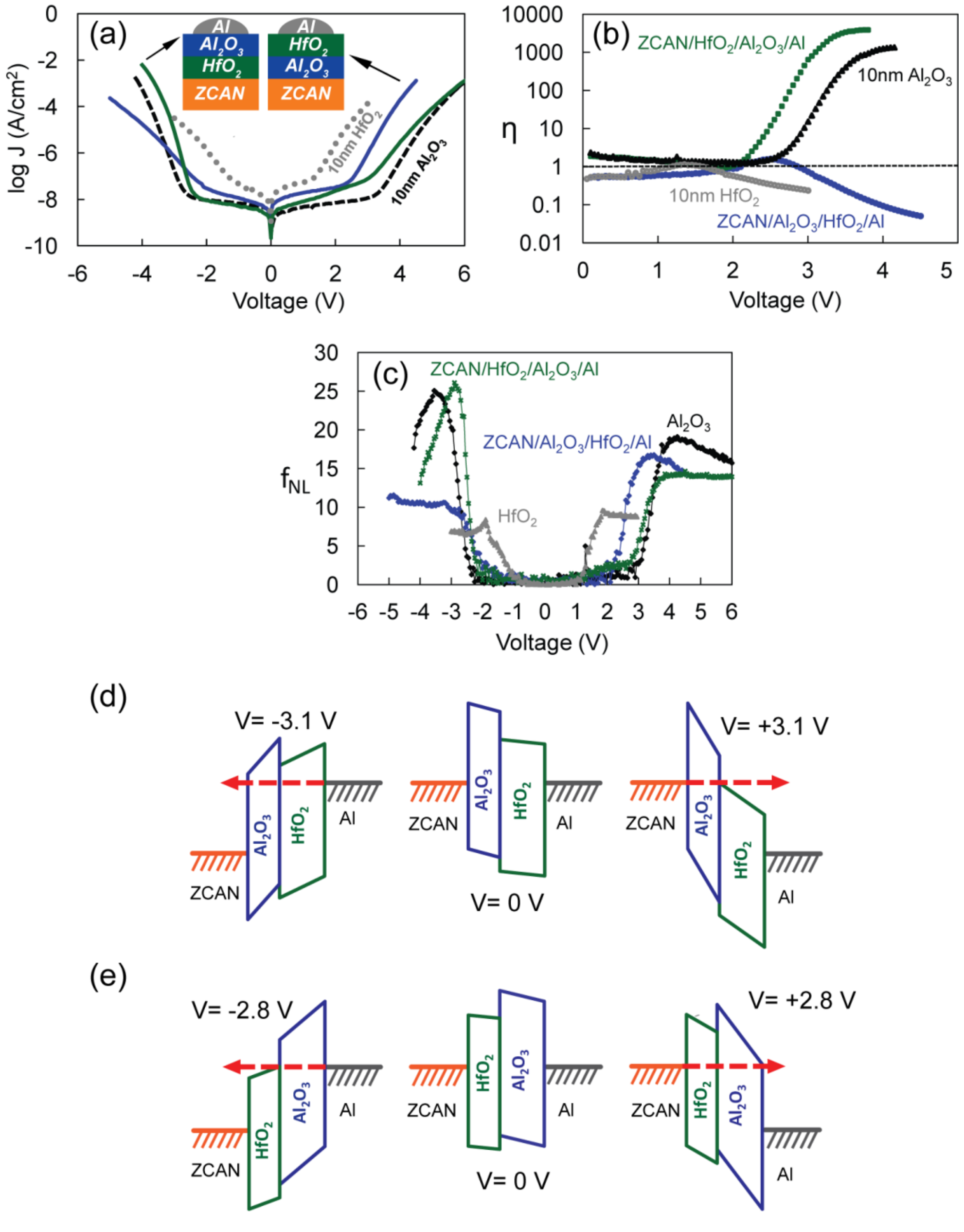

Fig. 6.3: Plots of (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V for ZCAN/3.5nm Al_2O_3/5nm HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/3.5nm HfO_2/5nm Al_2O_3/Al $M_1I_2I_1M_2$ diodes. M_1IM_2 diodes with single 10 nm layers of either Al_2O_3 or HfO_2 are included for comparison. In (d) and (e) are band diagrams illustrating MIIM diodes under negative bias (left), equilibrium (center), and positive bias (right).

Next consider the *reverse orientation* ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is now adjacent to the smaller workfunction Al electrode. Now with -2.8 V applied to the Al gate (Fig. 6.3(e),left), the Fermi level in the Al gate lies just above the conduction band of the HfO_2 and electrons injected from the Al may directly tunnel through only the Al_2O_3 layer (again representing a step reduction in tunnel distance). On the other hand, for +2.8 V applied to the Al gate (Fig. 6.3(e), right) electrons injected from the ZCAN electrode must pass through both insulator layers. Thus, a smaller current is expected at positive bias than at an equivalent magnitude negative bias so that $\eta > 1$ is expected, again confirmed in Fig. 6.3(b). In this case the asymmetry of the bilayer insulator barrier *enhances* the built-in asymmetry of the $\Delta\Phi$ and η is increased over that of the single Al_2O_3 layer M_1IM_2 diode. Note that since $\varphi_{Al\text{-}Al2O3} > \varphi_{ZCAN\text{-}HfO2}$, at higher magnitude applied biases the current density will begin to increase more quickly under positive bias than negative bias and the slope of the η-V plot will be expected to decrease. This behavior is confirmed in Fig. 6.3(b).

In Fig. 6.3(c), it is seen that all devices exhibit excellent f_{NL} with the bilayer ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diode showing the highest maximum non-linearity ($f_{NL\text{-}max}$ ~ 27). This device also shows enhanced f_{NL} at low negative bias exceeding that of single layer Al_2O_3 and HfO_2 devices, consistent with its enhanced η. The reverse insulator stack orientation ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device shows improved f_{NL} over the single layer Al_2O_3 M_1IM_2 diode at low positive bias and reduced f_{NL} at negative bias, consistent with the polarity of its η. Below ~|2V|, the single layer HfO_2 device shows the best f_{NL} consistent with its lower turn-on voltage.

Shown in Fig. 6.4 are (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V plots for *thinner* insulator bilayer ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. The HfO_2 and Al_2O_3 layers in these devices were deposited using 32 and 28 ALD cycles, respectively. The estimated thicknesses of the bottom and top insulator layers are ~1 nm and ~2.5 nm, respectively. For reference, also plotted are the approximately 3.5 nm thick single insulator layer Al_2O_3 and HfO_2 M_1IM_2 diodes from Fig. 6.1, which were deposited using 56 and 65 ALD cycles respectively. The behavior of these thinner bilayer devices is qualitatively the same as for the thicker devices. However, in all cases η_{max} is reduced, behavior that was also seen for the single layer MIM devices. Once again for the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device, the insulator bilayer *opposes* the $\Delta\Phi_M$ induced asymmetry. At voltages greater than about 2.5 V, $\eta < 1$ for the $M_1I_1I_2M_2$ device opposite to the $\eta > 1$ of the neat Al_2O_3 MIM device. For the reverse insulator orientation ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ device, the asymmetry induced by the $\Delta\Phi_M$ is once again *enhanced* by the bilayer insulator tunnel barrier, resulting in an η of higher magnitude than that of the neat Al_2O_3 MIM device.

As seen in Fig. 6.4(c), reducing the tunnel barrier thickness results in improved f_{NL} at small biases for all devices. This is due primarily to the lower turn on voltages and higher conductivity of these devices (see Fig. 6.4(a)). The relative improvement for the bilayer devices is even greater than for the single layer devices - as compared to single layer Al_2O_3, both of the thin MIIM devices show enhanced low bias f_{NL} for both polarities. Both MIIM devices have their highest f_{NL} for the bias polarity at which the step reduction in tunneling distance occurs. For the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$

devices f_{NL} is highest at positive bias, while for ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ devices f_{NL} is highest at negative bias, consistent with η data.

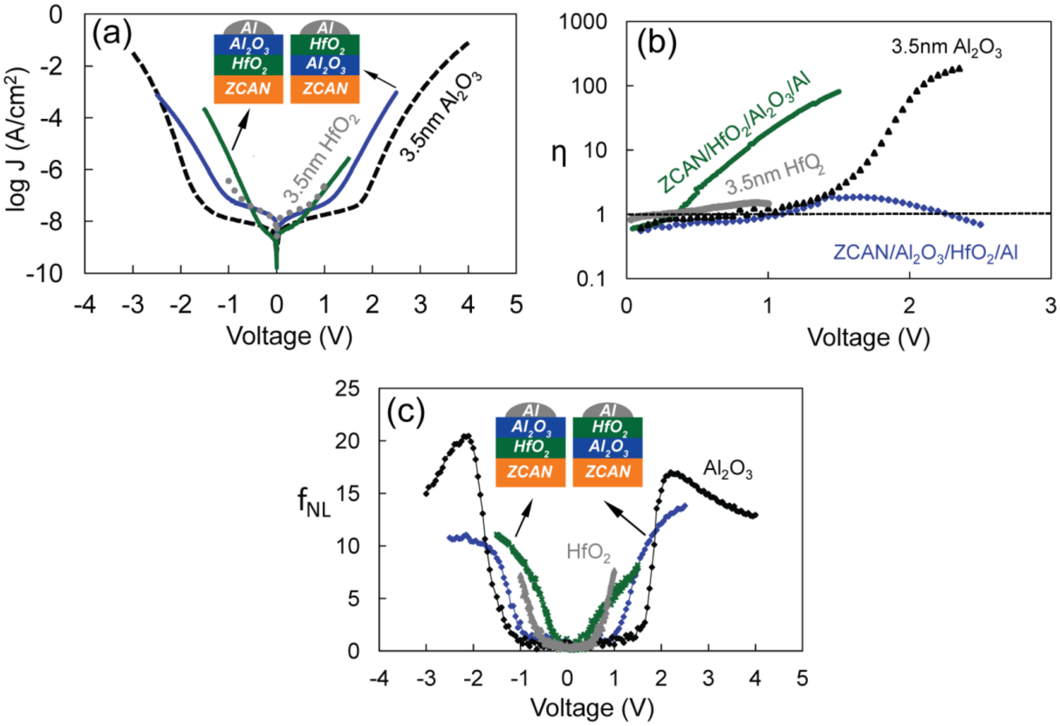

Fig. 6.4: Plots of (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V for ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. Al_2O_3 and HfO_2 layers were deposited using 28 and 32 ALD cycles, respectively, resulting in an estimated total stack thickness of 3.5 nm. M_1IM_2 diodes with approximately 3.5 nm thick layers of either Al_2O_3 or HfO_2 are included for comparison.

Overall, the thin bilayer ZCAN/HfO_2/Al_2O_3/Al device, despite reduced η_{max} and $f_{NL\text{-}max}$ as compared to the single layer Al_2O_3 device, shows excellent low voltage characteristics with $\eta > 10$ and $f_{NL} > 5$ at voltages as low as 0.8 V. For comparison, Maragechi et al.[16] recently reported η ~ 10 at 3 V and $f_{NL} < 5$ at 0.8 V for a symmetric electrode Cr/2nm HfO_2/2nm Al_2O_3/Cr diode.

It is clear that bilayer insulators can have a significant impact on M_1IIM_2 device operation. Examining more closely the ZCAN/Al_2O_3/Al band diagram inset in Fig. 6.1(b) and considering asymmetry due only to tunneling based conduction, the onset of FN tunneling should be roughly at the same voltage, independent of insulator thickness. However, in Fig. 6.1(b) it is seen that while significant asymmetry occurs above about 3 V in the 10 nm Al_2O_3 device, significant asymmetry occurs above about 1 V in the 3.5 nm Al_2O_3 device. While part of the reason for this may be the increased thickness of the Al_2O_3 reducing conduction below the noise floor of our measurement system, another possible explanation for this discrepancy could be the thin ZrO_x interfacial layer (IL) between the ZCAN electrode and the overlying insulator (see Fig. 6.2 as well as ref. [22]). Because of this IL, even the nominally single layer devices might be, in fact, bilayer devices. To model the potential impact of the ZrO_x IL, band diagrams similar to those in Fig. 6.3(e) may be used, if HfO_2 is replaced with 2 nm of ZrO_x and an Al_2O_3 thickness of approximately either 3.5 nm or 10 nm is used. For ZCAN/2 nm ZrO_x IL /Al_2O_3/Al bilayer devices, the minimum voltage for the step reduction in tunneling distance is simulated to be approximately -2.25 V. However, in the thicker device, the electrons must tunnel through a 10 nm thick Al_2O_3 layer while in the thinner device, the electrons tunnel through only an approximately 3.5 nm thick Al_2O_3 layer. Tunneling current is exponentially dependent upon the inverse of the barrier thickness ($I \propto \exp(1/d_{ox})$).[13] Thus in the presence of the ZrO_x IL, the onset voltage for tunneling based asymmetry is expected to be reduced as the thickness of the Al_2O_3 layer is reduced. Looking again at the single layer Al_2O_3 devices in Fig. 6.1, it seems evident that I-V characteristics and η were impacted by the presence of the ZrO_x IL, although it is also possible that emission based conduction mechanisms[24] or barrier lowering in the ultrathin device structure, not considered here, may play a role. The IL layer likely plays a role in the nominally single layer HfO_2 device as well, but since the E_G and χ of HfO_2 are likely similar to the E_G and χ of the ZrO_x IL, its impact is more difficult to predict.

6.4 Summary

In conclusion, we have experimentally demonstrated that ALD nanolaminate bilayer tunnel barriers add additional asymmetry and can be used to tune I-V asymmetry and non-linearity in asymmetric metal electrode M_1IIM_2 devices via step tunneling. I-V asymmetry and non-linearity were found to be sensitive to the arrangement of the individual insulator layers with respect to the asymmetric workfunction metal electrodes ($M_1I_1I_2M_2$ vs. $M_1I_2I_1M_2$). The bilayer insulators can be arranged to either enhance or oppose the built in asymmetric electrode workfunction induced asymmetry, depending on whether the smaller χ insulator is adjacent to the smaller or larger Φ_M electrode, respectively. By combining two methods of producing asymmetry, asymmetric metal electrodes and a bilayer insulator tunnel barrier, we were able to achieve excellent low voltage asymmetry and non-linearity in a ZCAN/HfO_2/Al_2O_3/Al diode exceeding both that of standard single insulator layer asymmetric electrode M_1IM_2 devices as well as symmetric electrode $M_1I_1I_2M_1$ devices. It is very likely that the relative thickness of the layers in the bilayer may be used to further enhance asymmetry. These results represent clear experimental demonstration that the asymmetry and non-linearity of MIIM diodes with asymmetric workfunction electrodes can be tuned by controlling step tunneling in the bilayer insulator, thus representing an advancement in the understanding necessary to engineer thin film MIIM tunnel devices for microelectronics applications.

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CHAPTER 7

Modulating Electrical Properties in MIM Tunnel Diodes by Stacking of Dielectrics

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In preparation for submission

7.1 Introduction

As discrete electronic devices are reaching to below 10 nm nodes, the quantum mechanical tunneling of carriers is inevitable through a few nanometer thick dielectrics. Thus, tunnel devices come to attention for microelectronic applications such as tunnel field effect transistors (FETs),[1] tunnel potential effect transistors (PETs) like hot electron transistors,[2] and magnetic tunnel junctions (MJTs) for memory applications.[3-5] Other applications include backplanes for liquid-crystal displays (LCDs),[6] infrared (IR) detectors,[7, 8] and optical rectennas for IR energy harvesting.[9, 10] These applications benefit from characteristics of tunneling phenomenon including ultra high frequency up to THz region operation, and low electric power consumption. For research studies on tunnel devices, thin film metal-insulator-metal (MIM) structures have been widely chosen due to the simple structure and planner compatibility to the current semiconductor processing technologies. MIM tunnel diodes are considered as the basic building blocks for tunnel electronics.

For majority of the mentioned applications, electrical properties requirement are, highly asymmetric and non-linear current vs. voltage (I-V) behavior at low applied voltages. These properties are defined via two figures of merits, the asymmetry (η) and the non-linearity (f_{NL}) in the I-V response. The standard approach to achieving asymmetric I-V characteristics in tunnel devices is the M_1IM_2 diode - the use of metal electrodes with different work functions ($\Phi_{M1} \neq \Phi_{M2}$) to produce a built-in voltage, $V_{bi} = (\Phi_{M1} - \Phi_{M2})/e$ (where e is the electronic charge) across the tunnel barrier.[11, 12] The amount of asymmetry achievable using this approach is limited by the V_{bi} ($\Delta\Phi_M$) that can be obtained using practical electrodes. An alternative approach to achieving asymmetric and non-linear operation is therefore needed. The approach investigated here involves engineering of the tunnel barrier so that electrons tunneling from one metal electrode to the other are presented with a different barrier shape depending on the direction of tunneling. Theoretically, formation of an asymmetric tunnel barrier can be accomplished using stacking of insulators,[13] with each insulator having different band-gaps (E_G) and electron affinities (χ), to produce metal-insulator-insulator-metal (MI_1I_2M) devices.[14, 15] As illustrated in Fig. 7.1, for a pair of insulators, asymmetry may be enhanced through either resonant tunneling or step tunneling (a step change in the tunneling distance through a bilayer tunnel barrier). We have recently reported superior electrical properties due to step tunneling in MIIM tunnel diodes made with HfO_2 and Al_2O_3 bilayer tunnel barriers, and ZrCuAlNi and Al asymmetric work function ($\Phi_{M1} \neq \Phi_{M2}$) electrodes.[16] It was demonstrated that bilayer tunnel barriers can be arranged to either enhance, oppose, or even reverse the asymmetry induced by the asymmetric work function electrodes. By

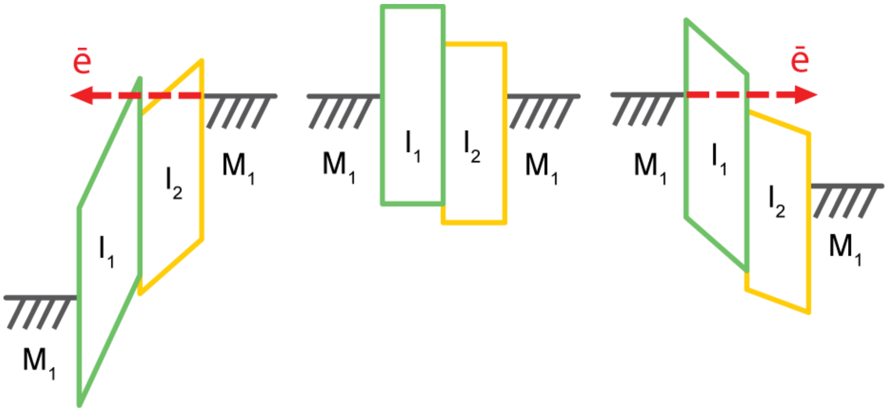

Fig. 7.1: Energy band diagrams of symmetric electrode $M_1I_1I_2M_1$ tunnel diodes, showing resonant tunneling (left) and step tunneling (right). In all band diagrams, the left electrode is grounded and voltage is applied to the right electrode.

combining bilayer tunnel barriers with asymmetric metal electrodes, devices are made with voltage asymmetry and non-linearity that exceed that of standard single layer asymmetric electrode M_1IM_2 devices as well as that of symmetric electrode $M_1I_1I_2M_1$ devices.

In this paper, the impact of a wide verity of small and large band gap dielectrics such as Al_2O_3, HfO_2, ZrO_2, and Ta_2O_5 as nanolaminate bilayer tunnel barriers on the performance of MIIM diodes is investigated experimentally. It is shown that the electrical properties of MIIM diodes can be modulated by the combination of the bilayer dielectrics and the relative thickness of each dielectric. Occurrence of step and resonant tunneling for these devices is simulated and experimentally examined. First, the importance of the choice of the electrodes is briefly discussed. Then the methodology for choosing bilayer dielectrics is described and band diagram simulations for different stacks are presented. After the description of the experiment, the experimental data is presented and discussed.

7.2 Brief notes on the importance of the electrodes

Before any of the mentioned applications can be realized, a manufacturable process will be required that can produce uniform, high quality MIM tunnel devices with high asymmetry and non-linearity. Despite investigation by many groups over many decades,[17-25] progress towards commercialization of MIM based electronics has been hindered by a lack of manufacturable processes. In particular, inattention to electrode roughness along with the lack of a high quality deposited oxide (which will be discussed in the next section) appears to have slowed development of this technology. The impact of electrode roughness can be appreciated if it is noted that the tunneling probability depends exponentially on the electric field in the thin dielectric film sandwiched between two electrodes.[26] In Fowler-Nordheim (FN) tunneling which is favored over direct tunneling to achieve asymmetry in tunnel devices, electrons tunnel through a triangular barrier into the conduction band of the dielectric. The current density attributed to FN tunneling is described as follows:[27, 28]

$$J = C_1 \frac{1}{\varphi_b} (\xi_{ox})^2 \exp\left(- \frac{C_2 \ \varphi_b^{\frac{3}{2}}}{\xi_{ox}} \right) \tag{7.1}$$

where

$$\xi_{ox} = \frac{V+\Delta\varphi}{S} \quad (V/cm), \tag{7.2}$$

$$C_1 = \frac{q^3}{16\pi\hbar}\left(\frac{m}{m_{ox}}\right) = 1.54 \times 10^{-6}\left(\frac{m}{m_{ox}}\right) \ (A/V^2), \tag{7.3}$$

and

$$C_2 = \frac{4\pi\sqrt{2m_{ox}}}{3q\hbar} = 6.83 \times 10^7 \left(\frac{m_{ox}}{m}\right)^{1/2} \ (V/cm) \tag{7.4}$$

φ_b is an effective energy barrier height between the dielectric and the electrode electrons tunneling from. Barrier height lowering is taken into account in φ_b. ξ_{ox} is electric field through the dielectric, V applied voltage, $\Delta\varphi$ the difference between barrier heights the dielectric makes with two electrodes, and S the dielectric thickness. q, $\hbar$, m, and m_{ox} are the elementary charge, reduced Plank constant ($h/2\pi$), the free electron mass, and the effective electron mass in the dielectric, respectively.

The tunneling current in a MIM tunnel diode should therefore depend strongly on the atomic scale roughness and the uniformity of the electrode-insulator interfaces.[29] Basic studies on electrode and interface roughness and their correlation with the tunneling current will therefore be very important for the advancement of MIM technology. We have previously studied the performance of MIM tunnel diodes formed on bottom electrode materials with various levels of RMS roughness.[30] It has been shown that bottom electrode roughness can strongly influence the I-V characteristics of M_1IM_2 diodes, overwhelming the metal work function difference induced asymmetry, and even reversing the trends expected based on $\Delta\Phi_M$. It has demonstrated that as electrode roughness decreases, the percentage yield of well-functioning devices trends higher. Further reliability investigations described in reference 31 have shown that devices with rougher bottom electrodes are more susceptible to failure due to bias stressing. It is observed that increased bottom electrode roughness is correlated with increased I-V hysteresis in these devices, suggesting that increased roughness may lead to increased charge trap density, which in turn could lead to energy barrier height variations.[31] Devices with smoother bottom electrodes are shown to produce I-V behavior with better agreement with Fowler-Nordheim tunneling phenomenon as well as yield a higher percentage of well-functioning devices. It should note that Fowler and Nordheim solved the Schrödinger equation using simplifications based on two considerations.[32] First the tunnel barrier has the exact triangular shape; second, the tunneling barrier is ideally smooth.[33] Both these issues are translated as the smoothness of the electrode-dielectric interface which is mainly governed by bottom electrode surface roughness. To overcome the mentioned non-idealities, the use of atomically smooth bottom electrodes is critical. Amorphous metal electrode ZrCuAlNi was proposed and studied due to its ultra smooth as deposited surface roughness.[34] In this work, amorphous ZrCuAlNi is used which have RMS and peak surface roughness below 0.3 nm and 3 nm, respectively. By combining high quality uniform tunnel barriers deposited by ALD with atomically smooth (≤ 0.3 nm RMS roughness) amorphous bottom electrodes, highly non-linear and asymmetric MIM tunnel diodes with good reproducibility and stable I-V behavior are produced.

7.3 Choosing nanolaminate dielectrics

Atomic layer deposition (ALD) was used to deposit high quality insulators independent of bottom metal electrodes. Whereas previous MIM diode work has focused primarily on native oxides, the use of ALD in this work allows for deposition of the same high quality insulator, independent of the bottom metal electrode. It should note that most experimental work to date on thin film MIM diodes has focused on the use of thin native dielectrics produced by oxidation or nitridation of an underlying rough polycrystalline metal electrode.[7,8,17-25] ALD enables depositing pinhole free dielectric films with atomic scale thickness accuracy. This is of utmost importance considering that tunneling current is exponentially dependent to the dielectric thickness.

M_1IM_2 structures using electrodes with different work functions are the standard approach to achieving asymmetric I-V characteristics in tunnel devices. Unfortunately, the amount of asymmetry achievable using the metal work function approach is limited by the $\Delta\Phi_M$ that can be obtained using practical electrodes. Note that ultrasmooth amorphous metals such as ZrCuAlNi, despite multiple metal components, typically do not easily allow a broad tuning of their electrical properties such as work function.[35,36] Thus, a better approach is needed to improve asymmetry in tunnel diodes. If the tunneling barrier consists of two or more dielectrics with different band-gaps and band-offsets, different energy barriers are introduced to tunneling electrons depending on the direction of tunneling; in other words the polarity of the applied bias. This makes turn-on bias of diodes polarity dependent and thus I-V response asymmetric. If dielectric layers are selected wisely, the asymmetry can increase by means of resonant or step tunneling beyond what can be achieved due to asymmetric turn-on bias contribution, see Fig. 7.1. In resonant tunneling, for one polarity quantized energy levels become available for tunneling electrons which increases tunneling probability and narrow down the energy distributions of tunneling electrons to those quantized energy levels. While for the same applied bias at opposite polarity, electrons have to tunnel through all the dielectric layers. The quantization occurs due to formation of a quantum well at the interface between two dielectrics. If there are more than two dielectric layers, the quantum wells should form the same polarity and quantized energy levels should accurately line up at all interfaces to enhance asymmetry; this is very hard to achieve. Thus, resonant tunneling can be mostly purposed and applicable for bilayer tunnel barriers. In step tunneling, a step reduction in the minimum tunnel distance occurs for one polarity. It occurs at the applied bias at which tunneling may begin to take place through only the wider band-gap insulator layer. As tunneling probability is exponentially dependent on tunneling distance, a step change would boost up tunneling current for one polarity. While, most theoretical work in the literature has been concerned with resonant tunneling; only step tunneling is of concern to this work. Using band-diagram simulations, it is found that resonant tunneling is not relevant for the majority of large and small band-gap dielectric pairs. It is discussed in another paper that the dominant conduction mechanisms through dielectrics should also be of main concern in choosing dielectric layers for nanolaminate tunnel barriers.[37] Simulations were performed for a variety of dielectric bilayer stacks with wide and narrow band-gaps. Shown in Fig. 7.2 are representative simulated band diagrams for various stacks showing the minimum voltage required for resonant tunneling and for step tunneling. To present a simplified picture, symmetric work function electrodes were assumed. It was found that for almost all bilayer stacks of SiO_2, Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, Nb_2O_5, and TiO_2, step tunneling occurs at a smaller absolute bias than resonant tunneling. The only exception was the Nb_2O_5 / Ta_2O_5 bilayer stack shown in Fig. 7.2 (d), in which resonant tunneling is predicted to occur at a slightly lower bias than step tunneling, consistent with recent simulation work on tunneling probability.[38,39] As it will be discussed, for the bilayer stacks used in this study, the electric field required to reach resonant tunneling exceeds the breakdown strength of the constituent Al_2O_3, HfO_2, Ta_2O_5 and ZrO_2 dielectrics.

One of the main advantages of using ALD is the capability of depositing nanolaminate dielectrics as the tunneling barrier. A wide range of dielectrics can be deposited in the nanolaminate order without breaking vacuum. Defects especially at the interfaces either at dielectric-electrode or dielectric-dielectric are minimum especially for thermal ALD because ALD is a very low-energy deposition technique. In this study four

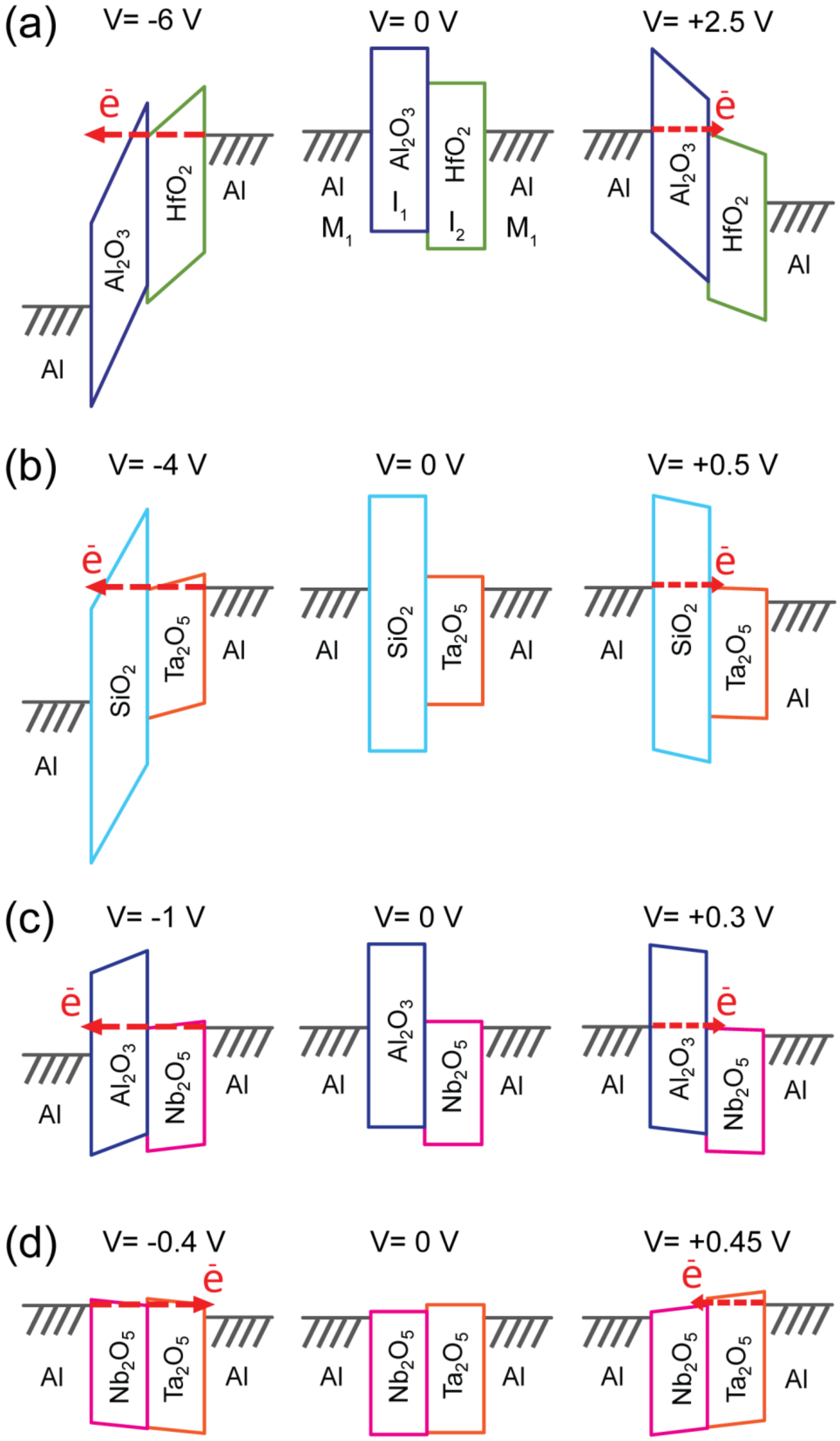

Fig. 7.2: Simulated energy band diagrams of $M_1I_1I_2M_1$ symmetric electrode tunnel diodes, showing step tunneling (right) and resonant tunneling (left) for a variety of dielectric stacks. In all band diagrams, left electrode is grounded and voltage is applied to right electrode.

metal oxide dielectrics, Ta_2O_5, ZrO_2, HfO_2, and Al_2O_3 are selected based on having a wide range of band-gaps and electron affinities. Nitride dielectrics have not used in this study to avoid potential chemical interactions between an oxide layer and a nitride layer, and cross contaminations in depositing oxides and nitrides in one chamber. Ta_2O_5 is chosen as it makes mall barriers with electrodes due to its large electron affinity which is close to the work functions of electrodes used in this study. Al_2O_3, a large band-gap dielectric, is useful to introduce a large energy barrier beside a low or medium energy barrier produced by a small or medium band-gap dielectric to increase asymmetry in nanolaminate structure tunnel barriers. SiO_2, a larger band-gap dielectric, is not used because a high quality ALD SiO_2 can be deposited by plasma-enhanced ALD (PEALD) which could damage dielectric-dielectric interfaces due to plasma radiations in PEALD. HfO_2 and ZrO_2 were chosen because they have band-gaps and electron affinity values in-between Ta_2O_5 and Al_2O_3; thus, they are useful to study how changing the band offset between dielectrics can influence diodes response. A total dielectric thickness of 10nm is chosen to favor FN tunneling conduction over direct tunneling because 10nm dielectric is thick enough to suppress direct tunneling to occur at low applied biases. Also, 10nm total dielectric thickness would enable easily studying how the relative thickness of the insulator layers can be used to further modulate electrical behavior. As discussed in our previous work, it is found that asymmetry and non-linearity reduce by decreasing tunnel barrier thickness. The impact of decreasing the total dielectric thickness is investigated in this study as well.

7.4 Experiment

MIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. A 150 nm thick ZrCuAlNi (ZCAN) bottom electrode was deposited directly on the SiO_2 via DC magnetron sputtering using a $Zr_{40}Cu_{35}Al_{15}Ni_{10}$ metal target. ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively.[30] Non-stoichiometry amorphous TaN electrodes with %10 nitrogen were deposited via physical vapor deposition (PVD) at the thickness of 40 nm. RMS and peak roughness of TaN films were measured to be 0.2 nm and 1 nm, respectively. Next, thin dielectric tunnel barriers were deposited via ALD using a Picosun SUNALE R-150B. Tantalum ethoxide, tetrakis (ethylmethylamino) zirconium (TDMAZr), tetrakis (ethylmethylamino) hafnium (TDMAHf), and trimethylaluminum (TMA) were used as the metal precursors for Ta_2O_5, ZrO_2, HfO_2, and Al_2O_3, respectively. The ALD films were deposited at a chamber temperature of 250 ºC using deionized water as the oxidant. All as deposited ALD films were determined to be almost entirely amorphous by X-ray diffraction (XRD). Devices are studied without annealing treatments to avoid any possibility of crystallization of either the ALD films or the amorphous bottom electrodes. Crystalline phases in thin dielectric films may create conduction paths for electrons and result non-tunneling currents.[40] Crystallization of the bottom electrode increases electrode surface roughness which results in field enhancement[41] and increased defect density at the insulator-electrode interface.[42] Finally, top electrodes were formed by evaporating Al dots (~0.2 mm^2) through a shadow mask. Thickness and optical dielectric constant of dielectrics on Si was measured with a J.A. Woollam WVASE32 spectroscopic ellipsometer using a

Cauchy model. Metal workfunctions (Φ_M) were measured in air using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip and calibrated against a gold standard. Φ_{ZCAN} was measured to be approximately 4.8 eV. $\Delta\Phi$ ($\Phi_{ZCAN} - \Phi_{Al}$) was measured to be approximately 0.6 eV, confirmed by extraction from the slope of Fowler-Nordheim (FN) plots. I-V analysis was conducted at room temperature on a probe station in a dark box using an Agilent 4156C semiconductor parameter analyzer; the noise floor of this system is estimated to be on the order of 10^2 pA. As shown in the schematic device cross section inset in Fig. 7.3, the bottom electrode (M_1) was always held at ground with bias applied to the Al top gate (M_2). To mitigate the impact of displacement current, all I-V curves were swept from zero bias to either the maximum positive or negative bias. An asymmetric electrode M_1IM_2 device structure is chosen for two main reasons. First, because different electrode-insulator interfaces are formed with different barrier heights, which enhances the asymmetry. Second, the ZrCuAlNi amorphous bottom electrode is deposited by DC magnetron sputtering. When used as a bottom electrode, it allows for high yield and high quality devices. However, if ZrCuAlNi is also used as the top electrode, the high energetic species introduced to dielectric surface during sputtering can cause damage to the dielectric, resulting in large hysteresis or electrical shorting for ultrathin devices.[34]

Two figures of merit are defined to characterize the devices. I-V asymmetry, η, is defined as negative device current divided by positive current $|I_- / I_+|$ so that $\eta = 1$ indicates symmetric operation. Non-linearity, f_{NL}, is defined as (dI/dV) / (I/V). All band diagrams were simulated using the Boise State University Band Diagram program.[43]

Materials parameters used in simulations are: electron affinity (χ) = 3.75 eV, band-gap (E_G) = 4.5 eV and relative dielectric constant (κ) = 26 for Ta_2O_5; χ = 2.75 eV, E_G = 5.7 eV and κ = 25 for ZrO_2; χ = 2.5 eV, E_G = 5.8 eV and κ = 18 for HfO_2; and χ = 1.3 eV, E_G = 6.4 eV and κ = 7.6 for Al_2O_3. ZrCuAlNi and Al electrodes work functions were considered 4.2 eV and 4.8 eV respectively which we have reported measurements and extractions in previous work.[16]

7.5 Results and discussion

The combined effect of bilayer tunnel barriers and asymmetric ($\Phi_{M1} \neq \Phi_{M2}$) electrodes are investigated on $M_1I_1I_2M_2$ diodes fabricated using atomically smooth ZrCuAlNi amorphous metal bottom electrodes and nanolaminate dielectric bilayers of HfO_2 / Al_2O_3, Ta_2O_5 / Al_2O_3, ZrO_2 / Al_2O_3, and HfO_2 / ZrO_2 deposited via ALD.

First in order to create an asymmetric tunnel barrier, Al_2O_3 and HfO_2 were stacked to form bilayer insulator MIIM devices. Initially for each dielectric bilayer, 56 ALD cycles were used to deposit Al_2O_3 and 65 cycles were used to deposit HfO_2, targeting a thickness of 5 nm for each layer. Previously reported high magnification TEM images revealed that the thickness of the top dielectric layer is indeed approximately equal to the 5 nm target. However, in each case, the thickness of the bottom dielectric layer deposited directly on the ZrCuAlNi bottom electrode was only approximately 3.5 nm.[16] This reduced thickness is likely due to an inhibition of the ALD nucleation rate on ZrCuAlNi as compared to that on oxide. In the first step in this study, the same thickness for each dielectric layer in the stack was desired to simplify analysis of I-V curves and band diagram simulations. Thus, nucleation curves of each dielectric layer on ZrCuAlNi bottom electrode were acquired and regarding the nucleation curves a larger number of ALD cycles was used if a dielectric layer is the first layer of the stack on the bottom electrode. 56 and 70 ALD cycles were used to deposit Al_2O_3 targeting a thickness of 5 nm on HfO_2 (first layer of the stack) and ZrCuAlNi; respectively. 66 and 85 ALD cycles were used to deposit HfO_2 targeting a thickness of 5 nm on Al_2O_3 (first layer of the stack) and ZrCuAlNi; respectively.

Shown in Fig. 7.3 are (a) log (J) vs. V, and (c) log (η) vs. V plots for ZCAN/5nm Al_2O_3/5nm HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/5nm HfO_2/5nm Al_2O_3/Al $M_1I_2I_1M_2$ diodes. For reference, also shown are the 10 nm thick single insulator Al_2O_3 and HfO_2 M_1IM_2 diodes. The inherent asymmetry of the bilayer insulator barriers is evident in the equilibrium band diagrams shown in Fig. 7.3(e). Differences in the I-V and η characteristics are qualitatively explained by the band diagrams which illustrate the approximate onset of step tunneling, tunneling through only the wider band-gap Al_2O_3 layer, at positive and negative bias.

First we consider the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is adjacent to the larger workfunction ZCAN electrode. Application of approximately +2.7 V (Fig. 7.3(e)) should bring the Fermi level of the ZCAN to just above the conduction band of the HfO_2 so that direct tunneling may occur through only the 5 nm thick Al_2O_3 layer, a step reduction in the required tunnel distance. For application of an opposite polarity -2.7 V bias electrons tunneling at the Fermi level

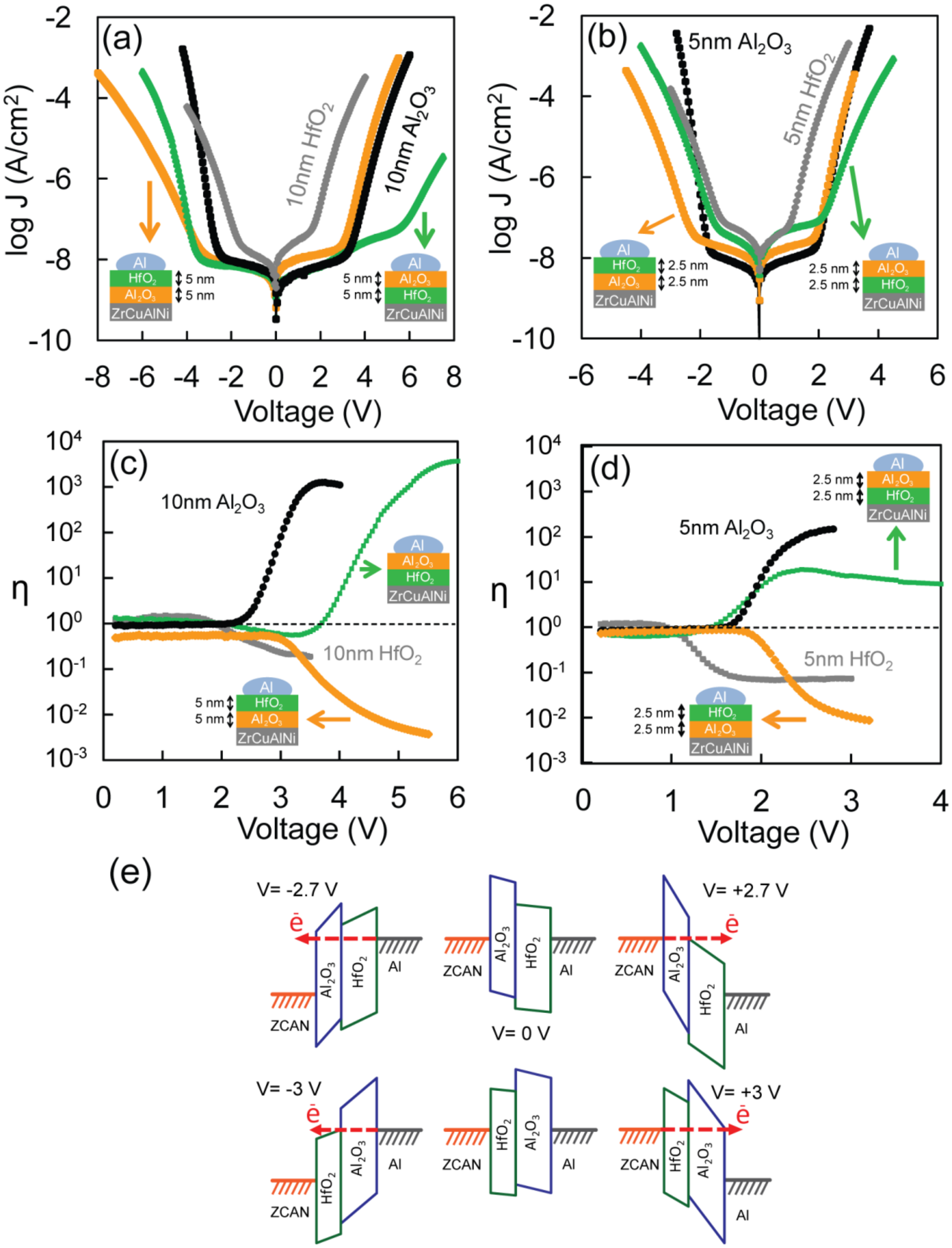

Fig. 7.3: Plots of log (J) vs. V, for ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes with (a) 5 nm and (b) 2.5 nm of each dielectric layer. Log (η) vs. V for the same devices (c) 5 nm, and (d) 2.5 nm of each dielectric. Data for M_1IM_2 diodes with single 10 nm or 5nm layers of either Al_2O_3 or HfO_2 are included for comparison. In (e) are band diagrams illustrating identical dielectric thickness MIIM diodes under negative bias (left), equilibrium (center), and positive bias (right).

must pass through 10nm thickness of both insulating layers. A larger current is thus expected at positive bias than at an equivalent magnitude negative applied bias so that $\eta < 1$ is expected. This is observed in Fig. 7.3(c). Note that the polarity of the asymmetry ($\eta < 1$) is reverse that of the single Al_2O_3 layer ($\eta > 1$), indicating that the asymmetry of the bilayer insulator barrier not only *opposes* that of the built-in voltage induced by the metal workfunction asymmetry ($\Delta\Phi$), but overwhelms its impact on device operation. Tunnel current is exponentially inversely dependent upon the barrier height ($I \propto \exp(\varphi_b^{-3/2})$).[11] Since $\varphi_{Al\text{-}HfO2} < \varphi_{ZCAN\text{-}Al2O3}$, for application of higher magnitude biases the negative bias current will begin to increase more rapidly than the positive bias current and it is expected that the slope of the η-V plot will decrease.[11] In Fig. 7.3(c) it is seen that for application of 5.5 V bias, the slope of the η-V plot has decreased.

Next consider the *reverse orientation* ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is now adjacent to the smaller workfunction Al electrode. Now with -3 V applied to the Al gate (Fig. 7.3(e)), the Fermi level in the Al gate lies just above the conduction band of the HfO_2 and electrons injected from the Al may directly tunnel through only the Al_2O_3 layer (again representing a step reduction in tunnel distance). On the other hand, for +3 V applied to the Al gate, electrons injected from the ZCAN electrode must pass through both insulator layers. Thus, a smaller current is expected at positive bias than at an equivalent magnitude negative bias so that $\eta > 1$ is expected, again confirmed in Fig. 7.3(c). In this case the asymmetry of the bilayer insulator barrier *enhances* the built-in asymmetry of the $\Delta\Phi$ and η is increased over that of the single Al_2O_3 layer M_1IM_2 diode. Note that since $\varphi_{Al\text{-}Al2O3} > \varphi_{ZCAN\text{-}HfO2}$, at higher magnitude applied biases the current density will begin to increase more quickly under positive bias than negative bias and the slope of the η-V plot will be expected to decrease. This behavior is confirmed in Fig. 7.3(c).

Shown in Fig. 7.3 are (b) log (J) vs. V, and (d) log (η) vs. V plots for *thinner* insulator bilayer ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ and ZCAN/HfO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. 29 and 49 ALD cycles were used to deposit Al_2O_3 targeting a thickness of 2.5 nm on HfO_2 (first layer of the stack) and ZrCuAlNi; respectively. 33 and 62 ALD cycles were used to deposit HfO_2 targeting a thickness of 2.5 nm on Al_2O_3 (first layer of the stack) and ZrCuAlNi; respectively. For reference, also plotted are the approximately 5 nm thick single insulator layer Al_2O_3 and HfO_2 M_1IM_2 diodes, which were deposited using 70 and 85 ALD cycles respectively. The behavior of these thinner bilayer devices is qualitatively the same as for the thicker devices. However, in all cases η_{max} is reduced, behavior that was also seen for the single layer MIM devices.[16] Once again for the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device, the insulator bilayer *opposes* the $\Delta\Phi_M$ induced asymmetry. At voltages greater than about 2 V, $\eta < 1$ for the $M_1I_1I_2M_2$ device opposite to the $\eta > 1$ of the neat Al_2O_3 MIM device.

Next Al_2O_3 and Ta_2O_5 dielectric stacks are studied in order to create asymmetric tunnel barrier MIIM devices. For each dielectric bilayer, 56 ALD cycles were used to deposit Al_2O_3 and 85 cycles were used to deposit Ta_2O_5, targeting a thickness of 5 nm for each layer. Shown in Fig. 7.4 are (a) log (J) vs. V, and (c) log (η) vs. V plots for ZCAN/5nm Al_2O_3/5nm Ta_2O_5/Al $M_1I_1I_2M_2$ and ZCAN/5nm Ta_2O_5/5nm Al_2O_3/Al

$M_1I_2I_1M_2$ diodes. For reference, also shown are the 10 nm thick single insulator Al_2O_3 and Ta_2O_5 M_1IM_2 diodes. The asymmetry of the bilayer insulator barriers is clear in the equilibrium band diagrams shown in Fig. 7.4(e). Differences in the I-V and η characteristics are qualitatively explained by the band diagrams which illustrate the approximate onset of step tunneling, tunneling through only the wider band-gap Al_2O_3 layer.

First we consider the ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is adjacent to the larger workfunction ZCAN electrode. For this stack, application of approximately +0.8 V (Fig. 7.4(e)) should bring the Fermi level of the ZCAN to just above the conduction band of the Ta_2O_5 so that direct tunneling may occur through only the 5 nm thick Al_2O_3 layer, a step reduction in the required tunnel distance. It is seen that the step tunneling occurs in the bias range 3 times smaller than that of Al_2O_3/HfO_2 stacks which is due to larger electron affinity of Ta_2O_5. So a dielectric with a large electron affinity value which makes smaller energy barriers with electrodes should be used besides a wider band-gap dielectric layer Al_2O_3 here in order to achieve step tunneling in lower bias ranges. For application of an opposite polarity -0.8 V bias, electrons tunneling at the Fermi level must pass through 10nm thickness of both insulating layers. A larger current is thus expected at positive bias than at an equivalent magnitude negative applied bias so that $\eta < 1$ is expected. This is not observed in Fig. 7.3(c). Note that the polarity of the asymmetry ($\eta > 1$) is reverse that of expected based on the band diagrams ($\eta < 1$). This could be due to dominance of other conduction mechanism rather than tunneling. As we have discussed elsewhere,[44] tunneling should be

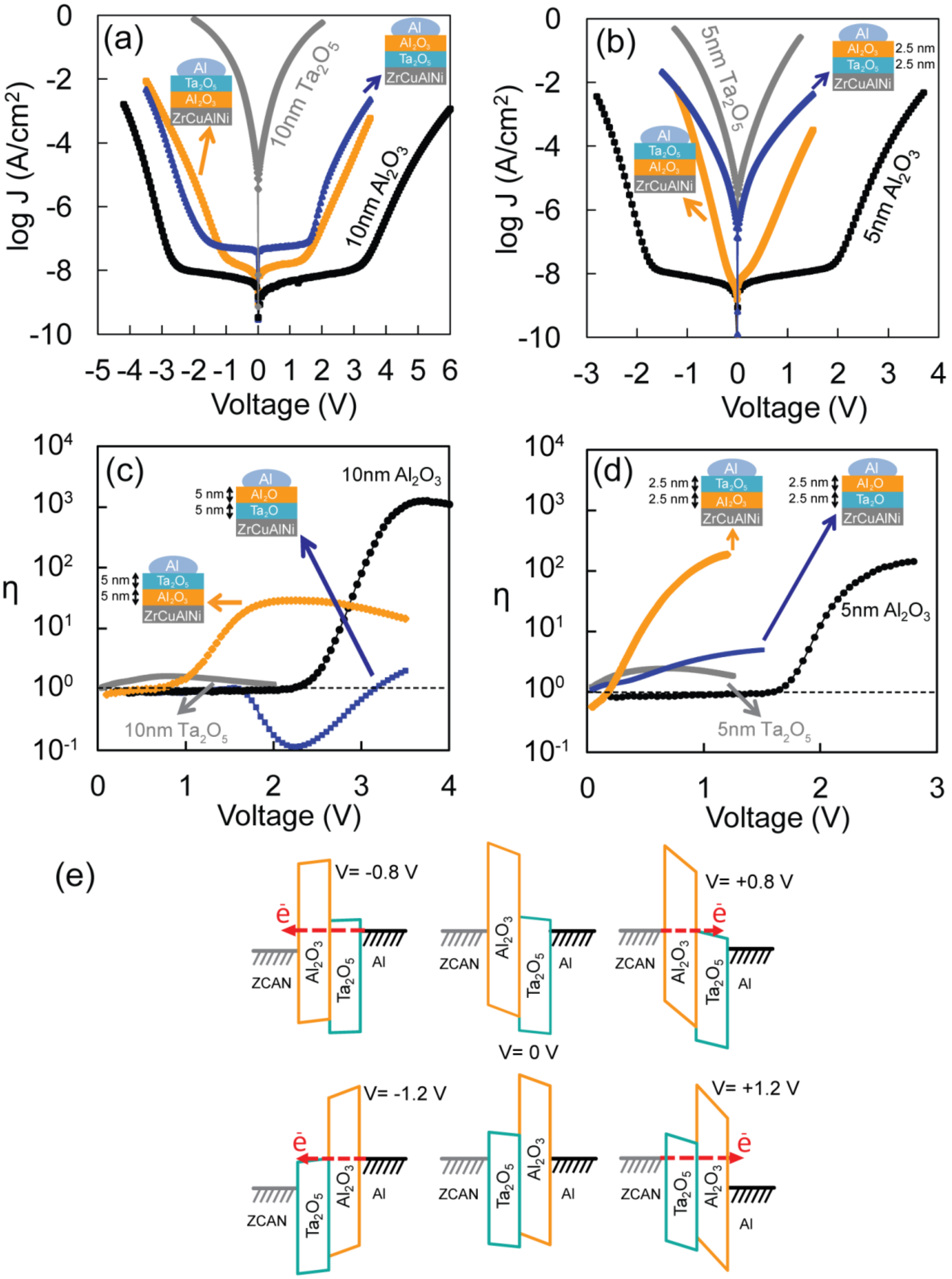

Fig. 7.4: Plots of log (J) vs. V, for ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ and ZCAN/Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ diodes with (a) 5 nm and (b) 2.5 nm of each dielectric; log (η) vs. V for the same devices (c) 5 nm, and (d) 2.5 nm of each dielectric. Data for M_1IM_2 diodes with single 10 nm or 5 nm layers of Al_2O_3 or Ta_2O_5 are included for comparison. In (e) are band diagrams illustrating identical dielectric thickness MIIM diodes under negative bias (left), equilibrium (center), and positive bias (right).

the dominant conduction mechanism in a dielectric layer to be used as a tunnel barrier. It was shown that tunneling is not the dominant conduction mechanism through 5 nm and 10 nm ALD Ta_2O_5 in diodes made with the same ZrCuAlNi and Al electrodes.[37]

Next consider the *reverse orientation* ZCAN/ Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is now adjacent to the smaller workfunction Al electrode. Now with -1.2 V applied to the Al gate (Fig. 7.4(e)), the Fermi level in the Al gate lies just above the conduction band of the Ta_2O_5 and electrons injected from the Al may directly tunnel through only the Al_2O_3 layer (again representing a step reduction in tunnel distance). On the other hand, for +1.2 V applied to the Al gate, electrons injected from the ZCAN electrode must pass through both insulator layers. Thus, a smaller current is expected at positive bias than at an equivalent magnitude negative bias so that $\eta > 1$ is expected; again it is not seen in Fig. 7.4(c). In this case the asymmetry of the bilayer insulator barrier *enhances* the built-in asymmetry of the $\Delta\Phi$ and η is increased over that of the single Al_2O_3 layer M_1IM_2 diode. However, the asymmetry increases to positive value for applied biases larger than 3 V, indicating current density is larger in negative polarity in comparison to positive polarity for applied biases larger than 3 V.

Shown in Fig. 7.4 are (b) log (J) vs. V, and (d) log (η) vs. V plots for *thinner* insulator bilayer ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ and ZCAN/Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. For each dielectric bilayer, 29 ALD cycles were used to deposit Al_2O_3 and 43 cycles were used to deposit Ta_2O_5, targeting a thickness of 2.5 nm for each layer. For reference, also plotted are the approximately 5 nm thick single insulator layer Al_2O_3 and

Ta_2O_5 M_1IM_2 diodes, which were deposited using 70 and 85 ALD cycles respectively. The behavior of these thinner bilayer devices is qualitatively the same as for the thicker devices. However, η_{max} is not reduced. Reduction of η_{max} for thinner insulator bilayer diodes is expected due to increase in probability of direct tunneling through thinner tunnel barriers. As mentioned above, it was also seen for the Al_2O_3/HfO_2 stacks.[16] For the ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ device, the insulator bilayer should *opposes* the $\Delta\Phi_M$ induced asymmetry. However, the $\eta > 1$ is seen, and η_{max} is even larger than the neat 5nm Al_2O_3 devices. The asymmetric response occurs in biases as small as 0.25 V which is not expected regarding the step tunneling predictions. For the reverse insulator orientation ZCAN/Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ device, the asymmetry induced by the $\Delta\Phi_M$ is observed in low bias range, but it seems that it is *not enhanced* by the bilayer insulator tunnel barrier, resulting in an η of smaller magnitude than that of the neat Al_2O_3 MIM device.

The anomalous observed asymmetry for ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ devices can be described due to different conduction mechanisms in each dielectric layer and a shift in the dominant conduction mechanism regarding the applied bias. Tunneling is the dominant conduction mechanism in Al_2O_3.[44] Whereas it is shown that Schottky emission and Frenkel-Poole emission are the dominant conduction mechanism at low bias regimes ($V_{appl.} < 0.4$ V) and large bias regimes ($V_{appl.} > 0.7$ V) through MIM diodes made with the same electrode combination and ALD Ta_2O_5. It should note that combining dielectrics having different dominant conduction mechanisms would make conduction of electrons in the MIIM diodes to be limited by the dielectric with lower conduction. In other words, I-V response of diodes cannot be only predicted by tunneling phenomenon. For ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ devices, the $\eta < 1$ is predicted based on tunneling and boosted current density under positive polarity due to step tunneling. However, $\eta > 1$ is observed for ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ devices which cannot be described by tunneling as the dominant conduction mechanism in these devices. However, the I-V responses can be explained by tunneling through Al_2O_3 and either Schottky emission or Frenkel-Poole emission through Ta_2O_5. If Al_2O_3 is adjacent to the electrode providing electrons, Al under negative applied bias for ZCAN/Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ device, and ZCAN under positive applied bias for ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ devices, the devices turn-on voltages and I-V responses can be explained by tunneling as electrons have to tunnel through Al_2O_3 layer first. If Ta_2O_5 is adjacent to the electrode providing electrons, ZCAN under negative applied bias for ZCAN/Ta_2O_5/Al_2O_3/Al $M_1I_2I_1M_2$ device, and Al under positive applied bias for ZCAN/Al_2O_3/Ta_2O_5/Al $M_1I_1I_2M_2$ devices, the devices turn-on voltages and I-V responses should be discussed by Schottky emission at smaller bias regimes because at small bias regimes conduction of electrons through Ta_2O_5 layer would be the limiting factor which is dominated by Schottky emission in Ta_2O_5. At the medium bias regimes (before the onset of Fowler-Nordheim tunneling through Al_2O_3 layer) tunneling of electrons through Al_2O_3 layer should limit conduction because electrons can conduct through Ta_2O_5 layer easier than Al_2O_3 layer. In other words, at medium bias regimes electrons conducting through Ta_2O_5, have to next conduct through Al_2O_3 layer by means of direct tunneling which is less likely at medium bias regimes. At larger bias regimes after reaching the onset of Fowler-Nordheim tunneling in Al_2O_3 the limiting factor again would be conduction of electrons through Ta_2O_5 layer which is dominated by Frenkel-Poole emission in large bias regimes.

Now, Al_2O_3 and ZrO_2 dielectric stacks are investigated in order to create asymmetric tunnel barrier in MIIM diodes. For each dielectric bilayer, 56 ALD cycles were used to deposit Al_2O_3 and 63 cycles were used to deposit ZrO_2, targeting a thickness of 5 nm for each layer. Shown in Fig. 7.5 are (a) log (J) vs. V, and (c) log (η) vs. V plots for ZCAN/5nm Al_2O_3/5nm ZrO_2/Al $M_1I_1I_2M_2$ and ZCAN/5nm ZrO_2/5nm Al_2O_3/Al $M_1I_2I_1M_2$ diodes. For reference, also shown are the 10 nm thick single insulator Al_2O_3 and ZrO_2 M_1IM_2 diodes deposited with 112 and 126 ALD cycles respectively. Again, the inherent asymmetry of the bilayer insulator barriers is evident in the equilibrium band diagrams shown in Fig. 7.5(e). Differences in the I-V and η characteristics are qualitatively discussed by the band diagrams which illustrate the approximate onset of step tunneling, tunneling through only the wider band-gap Al_2O_3 layer, at positive and negative bias.

First we consider the ZCAN/Al_2O_3/ZrO_2/Al $M_1I_1I_2M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is adjacent to the larger work function ZCAN electrode. Application of approximately +2.1 V (Fig. 7.5(e)) should bring the Fermi level of the ZCAN to just above the conduction band of the ZrO_2 so that direct tunneling may occur through only the 5 nm thick Al_2O_3 layer, a step reduction in the required tunnel distance. For application of an opposite polarity -2.1 V bias electrons tunneling at the Fermi level

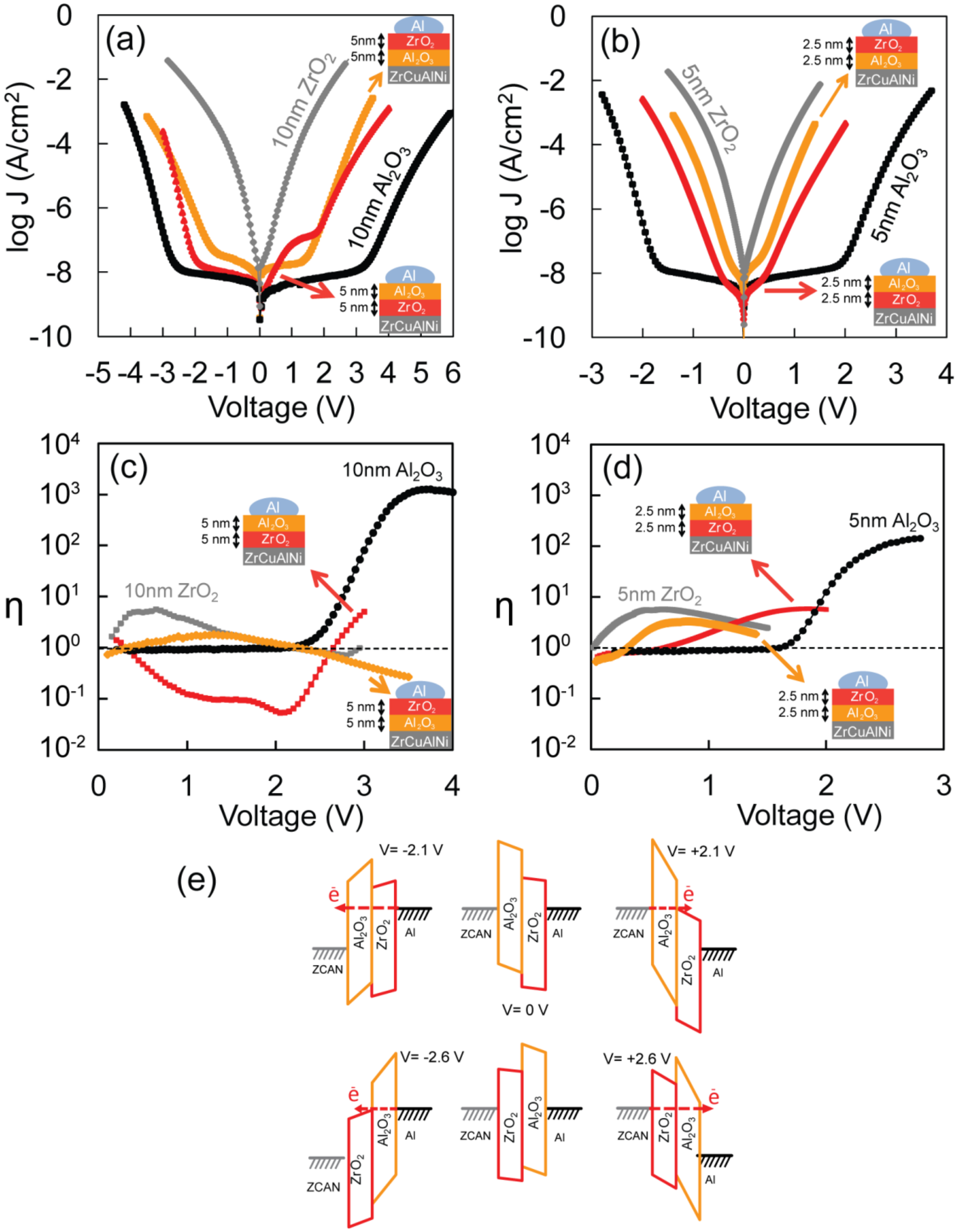

Fig. 7.5: Plots of log (J) vs. V, for ZCAN/Al_2O_3/ZrO_2/Al $M_1I_1I_2M_2$ and ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes with (a) 5 nm and (b) 2.5 nm of each dielectric; log (η) vs. V for the same devices (c) 5 nm, and (d) 2.5 nm of each dielectric. Data for M_1IM_2 diodes with single 10 nm or 5 nm layers of Al_2O_3 or Ta_2O_5 are included for comparison. In (e) are band diagrams illustrating identical dielectric thickness MIIM diodes under negative bias (left), equilibrium (center), and positive bias (right).

must pass through both insulating layers. A larger current is thus expected at positive bias than at an equivalent magnitude negative applied bias so that $\eta < 1$ is expected. This is observed in Fig. 7.3(c). Note that the polarity of the asymmetry ($\eta < 1$) is reverse that of the single Al_2O_3 layer ($\eta > 1$), indicating that the asymmetry of the bilayer insulator barrier not only *opposes* that of the built-in voltage induced by the metal work function asymmetry ($\Delta\Phi$), but overwhelms its impact on device operation.

Next we consider the *reverse orientation* ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ device, in which the larger band-gap Al_2O_3 layer (I_1) is now adjacent to the smaller work function Al electrode. Now with -2.6 V applied to the Al gate (Fig. 7.5(e)), the Fermi level in the Al gate lies just above the conduction band of the ZrO_2 and electrons injected from the Al may directly tunnel through only the Al_2O_3 layer (again representing a step reduction in tunnel distance). On the other hand, for +2.6 V applied to the Al gate, electrons injected from the ZCAN electrode must pass through both insulator layers. Thus, a smaller current is expected at positive bias than at an equivalent magnitude negative bias so that $\eta > 1$ is expected, again confirmed in Fig. 7.5(c). The asymmetry of the bilayer insulator barrier *enhances* the built-in asymmetry of the $\Delta\Phi$ and η should increase over that of the single Al_2O_3 layer M_1IM_2 diode. However, these devices break down at approximately -3.2 V and asymmetry values larger than that of neat Al_2O_3 devices was not reached. It is seen in Fig. 7.5(c) that $\eta < 1$ before the onset of the step tunneling at -2.6 V indicating larger current density for positive polarity. This is evident in a hump in Fig. 7.5(a) for ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ devices. It seems that if electrons are injected into ZrO_2 layer first, current density is larger than if electrons are first injected into Al_2O_3 layer from an electrode. This behavior can be expected if we consider the dominant conduction mechanism in each dielectric layer. It is discussed that the dominant conduction mechanism is tunneling throughout Al_2O_3 layer, while the dominant conduction mechanism could be Frenkel-Poole emission in ZrO_2.[44] Before current density at positive polarity takes over the current density at negative bias due to step tunneling, current density is larger for positive applied bias because electrons can conduct through ZrO_2 layer by means of Frenkel-Poole emission and then electrons see just 5nm of Al_2O_3 in front of them.

Shown in Fig. 7.5 are (b) log (J) vs. V, and (d) log (η) vs. V plots for *thinner* insulator bilayer ZCAN/Al_2O_3/ZrO_2/Al $M_1I_1I_2M_2$ and ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. For each dielectric bilayer, 29 ALD cycles were used to deposit Al_2O_3 and 33 cycles were used to deposit ZrO_2, targeting a thickness of 2.5 nm for each layer. For reference, also plotted are the approximately 5 nm thick single insulator layer Al_2O_3 and ZrO_2 M_1IM_2 diodes, which were deposited using 70 and 63 ALD cycles respectively. The behavior of these thinner bilayer devices is qualitatively the same as for the thicker devices. However, the expected $\eta > 1$ response for ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ devices occurs at biases as small as 0.6 V and the observed hump reported in the thicker insulator bilayer (5nm of each dielectric layer) is not seen here. It should note that for Al_2O_3 and ZrO_2 stacks, decreasing the total thickness is not found to produce devices showing either larger asymmetry or asymmetry in lower bias regime in comparison to neat Al_2O_3 or ZrO_2 diodes.

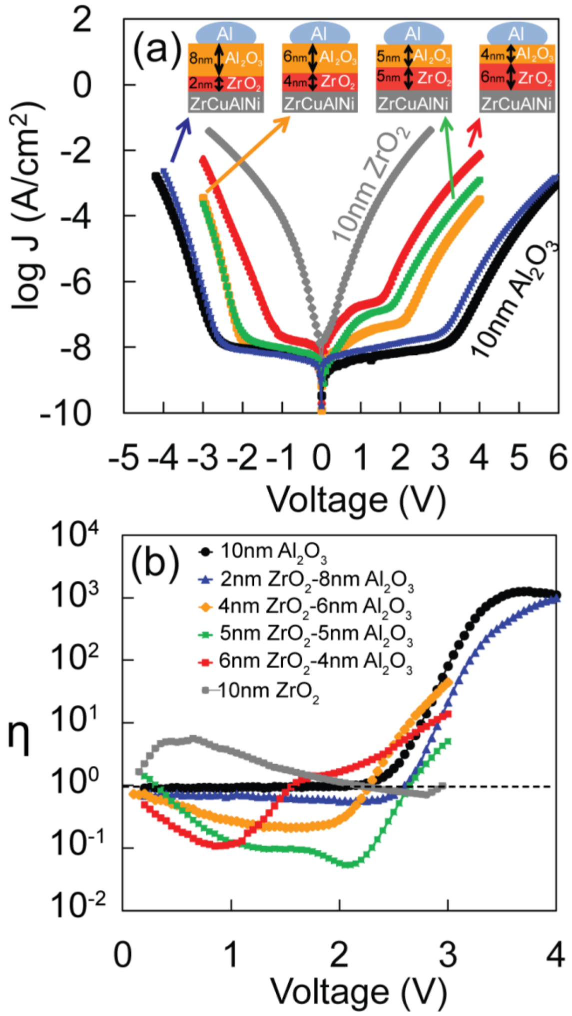

Fig. 7.6: Plots of (a) log (J) vs. V, (b) log (η) vs. V for ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes. The total thickness of the tunnel barrier is 10 nm and consists of either a single layer of Al_2O_3, a single layer of ZrO_2, or various Al_2O_3 I_1 /ZrO_2 I_2 bilayers.

ZCAN/ZrO_2/Al_2O_3/Al $M_1I_2I_1M_2$ diodes with total dielectric thickness of 10nm which showed a hump in positive polarities and a bias dependent in the polarity of asymmetry were furthermore investigated. Modulating I-V response of a tunnel device is critical to be able to broaden the applicability of tunnel devices. Here, we modulated the thickness of each dielectric layer without changing 10 nm total thickness of the tunnel barrier. Dielectric stacks with 2 nm ZrO_2/ 8 nm Al_2O_3, 4 nm ZrO_2/ 6 nm Al_2O_3, 5 nm

ZrO_2/ 5nm Al_2O_3, and 6nm ZrO_2/ 4nm Al_2O_3 were fabricated. Shown in Fig 7.6 are (a) log (J) vs. V, and (b) log (η) vs. V plots of these diodes. It is seen that the observed hump in ZCAN/5nm ZrO_2/5nm Al_2O_3/Al $M_1I_2I_1M_2$ diodes, repeats in all the stacks. The height of the hump and the bias it occurs at can be controlled by the relative thickness of the dielectric layer. Bipolar asymmetry as the function of the applied bias occurs for all of these devices too. It is seen that relative thickness of the individual insulator layers in the bilayer stack may be used to further tune electrical behavior.

Finally, HfO_2 and ZrO_2 dielectric stacks are investigated for creating asymmetric tunnel barrier in MIIM diodes. For each dielectric bilayer, 66 ALD cycles were used to deposit HfO_2 and 63 cycles were used to deposit ZrO_2, targeting a thickness of 5 nm for each layer. Shown in Fig. 7.7 are (a) log (J) vs. V, and (c) log (η) vs. V plots for ZCAN/5nm HfO_2/5nm ZrO_2/Al $M_1I_1I_2M_2$ and ZCAN/5nm ZrO_2/5nm HfO_2/Al $M_1I_2I_1M_2$ diodes. For reference, also shown are the 10 nm thick single insulator HfO_2 and ZrO_2 M_1IM_2 diodes deposited with 133 and 126 ALD cycles respectively. The asymmetric energy barriers of the bilayer insulator barriers are seen in the equilibrium band diagrams shown in Fig. 7.7(e), although due to relatively close electron affinities of HfO_2 and ZrO_2 dielectrics, the asymmetric barriers are not as distinct as the other stacks studied here. Differences in the I-V and η characteristics are qualitatively discussed by the band diagrams which illustrate the approximate onset of step tunneling, tunneling through only the wider band-gap Al_2O_3 layer, at positive and negative bias.

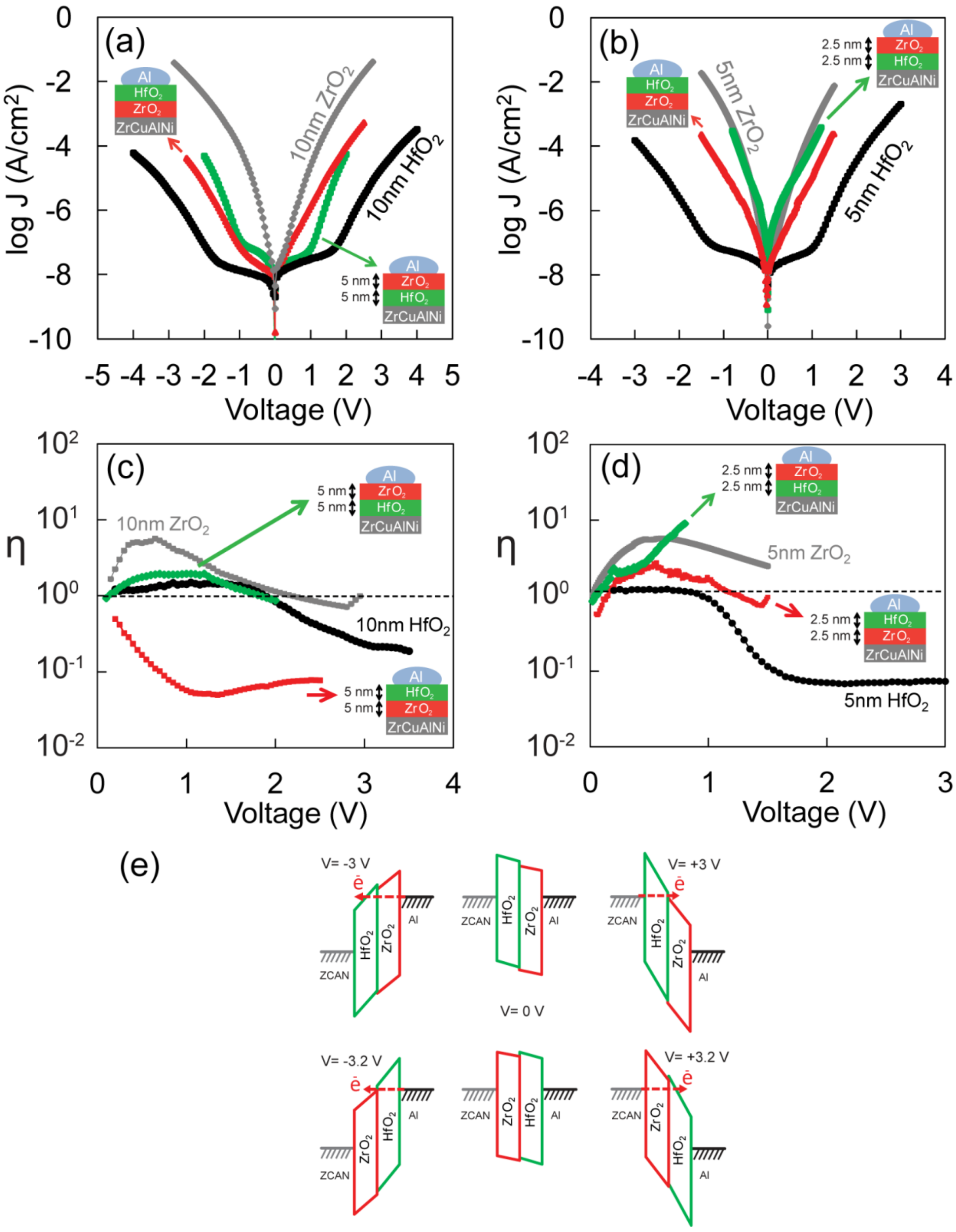

Fig. 7.7: Plots of log (J) vs. V, for ZCAN/HfO_2/ZrO_2/Al and ZCAN/ZrO_2/HfO_2/Al diodes with (a) 5 nm and (b) 2.5 nm of each dielectric; log (η) vs. V for the same devices (c) 5 nm, and (d) 2.5 nm of each dielectric. Data for M_1IM_2 diodes with single 10 nm or 5nm layers of HfO_2 or ZrO_2 are included for comparison. In (e) are band diagrams illustrating MIIM diodes under negative bias (left), equilibrium (center), and positive bias (right).

First we consider the ZCAN/ HfO_2/ZrO_2/Al $M_1I_1I_2M_2$ device, in which the larger band-gap HfO_2 layer (I_1) is adjacent to the larger work function ZCAN electrode. Application of approximately +3 V (Fig. 7.7(e)) should bring the Fermi level of the ZCAN to just above the conduction band of the ZrO_2 so that direct tunneling may occur through only the 5 nm thick HfO_2 layer, a step reduction in the required tunnel distance. Note that for HfO_2/ZrO_2 stacks due to relatively close electron affinities of HfO_2 and ZrO_2 dielectrics, step tunneling occurs at a larger bias. Remembering from the case of Al_2O_3/Ta_2O_5 stacks which have the largest difference in their electron affinity values, step tunneling should happen in the smallest voltage among stacks studied in this work. For application of an opposite polarity -3 V bias electrons tunneling at the Fermi level must pass throughout just the total thickness of ZrO_2 and a fraction of total thickness of HfO_2 as -3 V is larger than the onset bias for Fowler-Nordheim tunneling through HfO_2. Although a larger current is thus expected at positive bias than at an equivalent magnitude negative applied bias ($\eta < 1$), the difference between current under positive polarity and negative polarity would not be large. This could not be observed in Fig. 7.7(c) because the diodes break down before reaching to the onset of the step tunneling. ZCAN/ HfO_2/ZrO_2/Al $M_1I_1I_2M_2$ device showed relatively linear I-V response.

Next consider the *reverse orientation* ZCAN/ZrO_2/ HfO_2/Al $M_1I_2I_1M_2$ device, in which the larger band-gap HfO_2 layer (I_1) is now adjacent to the smaller work function Al electrode. Now with -3.2 V applied to the Al gate (Fig. 7.7(e)), the Fermi level in the Al gate lies just above the conduction band of the ZrO_2 and electrons injected from the Al may directly tunnel through only the HfO_2 layer (again representing a step reduction in tunnel distance). On the other hand, for +3.2 V applied to the Al gate, electrons injected from the ZCAN electrode must pass throughout just the total thickness of ZrO_2 and a fraction of total thickness of HfO_2 as +3.2 V is larger than the onset bias required for Fowler-Nordheim tunneling through HfO_2. Thus, a smaller current is expected at positive bias than at an equivalent magnitude negative bias so that $\eta > 1$ is expected. This is not seen in Fig. 7.7(c) because the devices break down before step tunneling occurs. However, in this case the asymmetry of $\eta < 1$ for the bilayer insulator barrier is seen which could be due to different conduction mechanisms in HfO_2 and ZrO_2. We have discussed elsewhere that while the dominant conduction mechanism in ZrO_2 is Frenkel-Poole, the dominant conduction mechanism in HfO_2 is defect assisted tunneling.[44] At low and medium bias ranges conduction by Frenkel-Poole emission is enhanced in comparison to defect assisted tunneling; thus larger current is expected in positive polarity for ZCAN/ZrO_2/ HfO_2/Al $M_1I_2I_1M_2$ device. This is seen in $\eta < 1$ for this devices in Fig. 7.7(c).

Shown in Fig. 7.7 are (b) log (J) vs. V, and (d) log (η) vs. V plots for *thinner* insulator bilayer ZCAN/HfO_2/ZrO_2/Al $M_1I_1I_2M_2$ and ZCAN/HfO_2/ ZrO_2/Al $M_1I_2I_1M_2$ diodes. For each dielectric bilayer, 33 ALD cycles were used to deposit HfO_2 and 32 cycles were used to deposit ZrO_2, targeting a thickness of 2.5 nm for each layer. For reference, also plotted are the approximately 5 nm thick single insulator layer HfO_2 and ZrO_2 M_1IM_2 diodes, which were deposited using 85 and 63 ALD cycles respectively. The behavior of these thinner bilayer devices should qualitatively be the same as for the thicker devices. However, it is seen that ZCAN/HfO_2/ ZrO_2/Al $M_1I_2I_1M_2$ diodes show relatively linear I-V response while they showed $\eta < 1$ for the thicker stacks (total thickness of 10 nm). In case of ZCAN/HfO_2/ZrO_2/Al $M_1I_1I_2M_2$ diodes with thinner bilayer stacks, they demonstrate $\eta > 1$ in small bias range ($V_{appl.} < 1$ V), whereas they show linear I-V response for thicker stack with total thickness of 10 nm (see Fig 7.7(c)). This unusual property could be due to the dominance of different conduction mechanisms for different thicknesses of ZrO_2 and HfO_2. It appears that for both of the thicknesses of these dielectrics studied here, tunneling is not the dominant conduction mechanism because the I-V curves of the diodes could not qualitatively describe based on the simulated band energy diagrams in Fig. 7.7(e).

7.6 Summary

In conclusion, it is demonstrated that the relative thickness of the layers in the bilayer could be used to modulate I-V response of devices and further enhance asymmetry. Nanolaminate bilayer tunnel barriers can be engineered to either increase the maximum asymmetry, $\eta_{max.}$, or asymmetry at small bias regimes. It showed that step tunneling occurs at smaller bias before resonant tunneling in all bilayer dielectrics studied in this work by simulation and fabrication.

It was experimentally shown that ALD nanolaminate bilayer tunnel barriers add additional asymmetry and can be used to tune I-V asymmetry and non-linearity in asymmetric metal electrode M_1IIM_2 devices via step tunneling. I-V asymmetry and non-linearity were found to be sensitive to the arrangement of the individual insulator layers with respect to the asymmetric work function metal electrodes ($M_1I_1I_2M_2$ vs. $M_1I_2I_1M_2$).

The bilayer insulators can be arranged to either enhance or oppose the built in asymmetric electrode work function induced asymmetry, depending on whether the smaller χ insulator is adjacent to the smaller or larger Φ_M electrode, respectively.

The combined effect of bilayer tunnel barriers were investigated on $M_1I_1I_2M_2$ diodes fabricated using nanolaminate dielectric bilayers of HfO_2 / Al_2O_3, Ta_2O_5 / Al_2O_3, ZrO_2 / Al_2O_3, and HfO_2 / ZrO_2 deposited via ALD. To enhance asymmetric I-V response in tunnel diodes via bilayer tunnel barriers, conduction should be tunneling in both dielectric layers. It was found that I-V behavior in Ta_2O_5 / Al_2O_3, ZrO_2 / Al_2O_3, and HfO_2 / ZrO_2 devices cannot be completely explained by means of simulated band diagrams considering tunneling as the dominant conduction mechanism through dielectric layers. Step tunneling enhanced asymmetric response was not observed for Ta_2O_5 / Al_2O_3, and HfO_2 / ZrO_2 devices.

I-V response of MIIM diodes with dielectric stacks having different conduction mechanism than tunneling was found to be complicated to predict and interpret. As it has explained for single dielectric layer MIM diodes before, the dominant conduction mechanism in ZrO_2 and Ta_2O_5 was found to vary regarding the applied electric field. Explanation of bilayer dielectric devices with either ZrO_2 or Ta_2O_5 was found even more complicated beacuse the dominant conduction mechanism through each layer changes as a function of applied bias.

These results represent clear experimental demonstration that the asymmetry and non-linearity of MIIM diodes with asymmetric work function electrodes can be tuned by controlling step tunneling in the bilayer insulator, thus representing an advancement in the understanding necessary to engineer thin film MIIM tunnel devices for microelectronics applications.

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CHAPTER 8

Metal Insulator Metal Tunnel Devices: Formation and Impact of Interfacial Layers

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In preparation for submission

8.1 Introduction

Metal-insulator-metal (MIM) tunnel devices are recently taken a significant attention for variety of high-speed and low-power application such as hot electron transistors,[1,2] infrared (IR) detectors,[3,4] and optical rectennas for IR energy harvesting.[5,6] Electrical behavior requirements are, highly asymmetric and non-linear current vs. voltage (I-V) behavior at low applied voltages. These properties are defined via two figures of merits, the asymmetry (η) and non-linearity (f_{NL}) in the I-V response. The standard way to achieveing asymmetric I-V respond in tunnel diodes, is through dominance of Fowler-Nordheim (FN) tunneling as conduction mechanism,[7,8] and the use of asymmetric work function metal electrodes to introduce different energy barriers to tunneling electrons based on polarity.[9] Unfortunately, the amount of asymmetry achievable using the metal work function approach is limited by the difference in electrodes' work functions $\Delta\Phi_M$ ($\Phi_{M1} \neq \Phi_{M2}$) that can be obtained using practical electrodes. Atomically smooth bottom electrodes have shown as a critical component in fabricating well-functioning and reliable tunnel diodes with superior electrical properties.[10,11] Note that ultrasmooth electrodes such as multi-component amorphous metal thin films (AMTFs), TaN, and TiN despite multiple components, typically do not allow a broad tuning of their electrical properties such as work function.[12,13] In addition, MIM diodes for rectenna and IR detector applications are required to operate at very low bias regimes.[14] The operation regime of MIM tunnel diodes is mainly ruled by the choice of the dielectric layer. Periasamy et al. have found that a dielectric with large electron affinity should be selected to make an MIM diode working in low bias regimes.[15] However, a very recent study on

Nb_2O_5 and Ta_2O_5 dielectrics having large electron affinities shows that these dielectrics are not good tunnel barriers as electrons can conduct through them by means of either Schottky emission or Frenkel-Poole emission through them.[16] Another study has also shown by reducing dielectric thickness in MIM structures while the turn-on voltage decreases, the asymmetry and noon-linearity of devices degrades.[17] Thus, an additional approach to achieving asymmetric and non-linear operation in low bias regimes has recently investigated theoretically [18,19] and experimentally [17,20] in which a nanolaminate pair of insulators (each with different E_G and χ) are used to create asymmetric tunnel barrier metal-insulator-insulator-metal (MIIM) devices.

In MIIM devices, electrons tunneling from one metal electrode to the other are presented with a different barrier shape depending on the direction of tunneling. It was demonstrated that high quality nanolaminate bilayer tunnel barriers deposited via ALD dominate the electrical characteristics of asymmetric metal electrode M_1IIM_2 devices.[17] I-V asymmetry and non-linearity were reported to be sensitive to the arrangement of the individual insulator layers with respect to the different metal electrodes ($M_1I_1I_2M_2$ vs. $M_1I_2I_1M_2$). Depending on whether the smaller χ insulator was adjacent to the smaller or larger Φ_M electrode, respectively, the bilayer dielectrics were found to either enhance or oppose (even reverse) the $\Delta\Phi_M$ induced asymmetry. Using band diagrams and assuming that conduction is dominated by tunneling mechanisms, these results are qualitatively well explained by step tunneling phenomenon. It has reported that by combining two methods of producing asymmetry, asymmetric metal electrodes and a bilayer dielectric tunnel barrier, excellent low voltage asymmetry and non-linearity have achieved in a

ZrCuAlNi/HfO_2/Al_2O_3/Al MIIM diode exceeding both that of standard single dielectric layer asymmetric electrode M_1IM_2 devices as well as symmetric electrode $M_1I_1I_2M_1$ devices.[17] It has also demonstrated that the relative thickness of the insulator layers could be used to further tune electrical behavior.[21]

Nanolaminate tunnel barriers can bring an exceptional opportunity to engineer tunnel devices. Hence, there is a calling need to investigate nanolaminate tunnel barriers from two perspectives. First, conduction mechanisms through nanolaminates of candidate dielectrics should be studied. Second, chemical and thermodynamical stability of layers, potential formation of interfacial layers, and electrical influence of interfaces should be investigated. In this work, the formation and influence of interfaces, as a means for providing insight into engineering of nanolaminate barrier tunnel devices is examined by comparing HfO_2/Al_2O_3 nanolaminate bilayer dielectric tunnel barriers on two different atomically smooth bottom electrodes, amorphous metal electrode ZrCuAlNi, and TaN.

8.2 Experiment

MIM and MIIM diodes were fabricated on Si substrates capped with 100 nm of thermally grown SiO_2. A 150 nm thick ZrCuAlNi (ZCAN) bottom electrode was deposited directly on the SiO_2 via DC magnetron sputtering using a $Zr_{40}Cu_{35}Al_{15}Ni_{10}$ metal target. ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively; the details were reported elsewhere.[11] ZCAN RMS and peak roughness were measured to be 0.3 nm and 3 nm, respectively; the details were reported elsewhere. Non-stoichiometry TaN bottom electrodes with %10 nitrogen concentration were deposited via physical vapor deposition (PVD) with the thickness of 40 nm. Next, thin oxide tunnel barriers were deposited via ALD using a Picosun SUNALE R-150B. Trimethylaluminum (TMA) and tetrakis (ethylmethylamino) hafnium (TDMAHf) were used as the metal precursors for Al_2O_3 and HfO_2, respectively. All ALD films were deposited at a chamber temperature of 250 ºC using deionized water as the oxidant. Nanolaminate bilayer barriers were deposited in one continuous run without breaking vacuum. Finally, top electrodes were formed by evaporating Al dots (~0.2 mm^2) through a shadow mask. Insulator thickness on Si was measured with a J.A. Woollam WVASE32 spectroscopic ellipsometer using a Cauchy model. Transmission electron microscopy (TEM) images were taken on a FEI Titan 80-200 using samples prepared with a Quanta 3D Dual Beam focused ion beam. Metal workfunctions (Φ_M) were measured in air using a KP Technology SKP5050 scanning Kelvin probe with a 2-mm tip and calibrated against a gold standard. Φ_{ZCAN} was measured to be approximately 4.8 eV. $\Delta\Phi$ ($\Phi_{ZCAN} - \Phi_{Al}$) was measured to be approximately 0.6 eV, confirmed by extraction from the slope of Fowler-Nordheim (FN) plots. I-V analysis was conducted at room temperature on a probe station in a dark box using an Agilent 4156C semiconductor parameter analyzer; the noise floor of this system is estimated to be on the order of 10^2 pA.

Two figures of merit are defined to characterize the devices. I-V asymmetry, η, is defined as negative device current divided by positive current $|I_- / I_+|$ so that $\eta = 1$ indicates symmetric operation. Non-linearity, f_{NL}, is defined as (dI/dV) / (I/V). All band diagrams were simulated using the Boise State University Band Diagram program.[22] Materials parameters used in simulations are consistent with values reported for similar

ALD films: electron affinity (χ) = 1.3 eV, bandgap (E_G) = 6.4 eV and relative dielectric constant (κ) = 7.6 for Al_2O_3; χ = 2.5 eV, E_G = 5.8 eV and κ = 18 for HfO_2; χ = 3.75 eV, E_G = 4.5 eV and κ = 26 for Ta_2O_5; χ = 2.75 eV, E_G = 5.7 eV and κ = 25 for ZrO_2; and Φ_{Al} = 4.2 eV.

A dielectric thickness of 5 nm and 10 nm is chosen to be able to distinguish FN tunneling conduction from other conduction mechanisms because 10 nm dielectric is thick enough to suppress direct tunneling to occur while other conduction mechanisms could contribute to conduction at low applied voltage. All as deposited ALD films were determined to be amorphous by XRD and electron diffraction under TEM. Devices are studied without annealing treatments to avoid any possibility of crystallization of both ALD films and amorphous bottom electrodes. Crystalline phases in dielectric films may create conduction paths for electrons and thus facilitates defect-induced currents.[23] Crystallization of bottom electrode causes electrode surface roughness which can generate field enhancement and large defect density at insulator-electrode interface.[24,25]

8.3 Results and discussion

I-V behavior of single dielectric layer MIM diodes is shown in Fig. 8.1. Plots are (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V, for devices made on ZrCuAlNi and TaN bottom electrodes and either 5nm or 10nm of Al_2O_3 or HfO_2 with Al top electrodes. Al_2O_3 and HfO_2 devices with TaN bottom electrode show very well agreement with band diagrams simulations illustrated in Fig 8.1(a) inset. As expected, HfO_2 diodes turn on earlier than Al_2O_3 diodes at both negative and positive polarities due to larger electron affinity of HfO_2 which makes smaller barrier heights with the electrodes. HfO_2 diodes show larger leakage before they turn on which is expected due to inherently smaller band gap and energy barriers with electrodes for HfO_2.

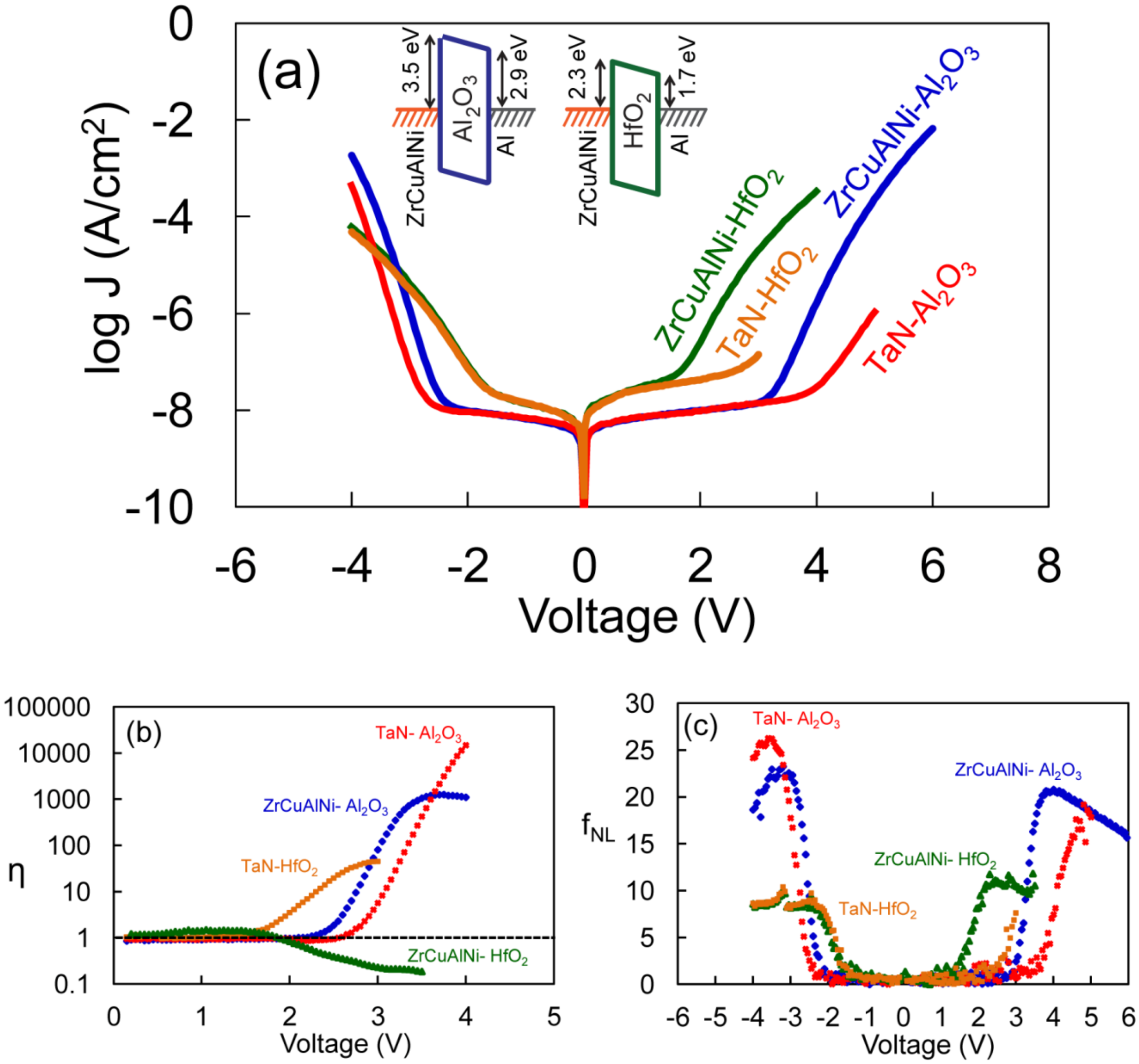

Fig.8.1: Plots of (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V for devices made on ZrCuAlNi and TaN bottom electrodes and either 5 nm or 10 nm of Al_2O_3 or HfO_2 with Al top electrodes.

Although diodes made with Al_2O_3 turn on at larger bias, it is seen that current response in these diodes increases more rapidly and eventually over come current for HfO_2 devices in negative polarity. This behavior is also in complete agreement with band diagram simulations and FN tunneling theory. After a tunnel diode turns on due to FN tunneling, the rate of exponential increase in current response (slope of I-V curve) due to FN tunneling is a function of energy barrier height between the electrode, electrons tunnel from, and the insulator layer. Thus slopes of I-V curves should be steeper for the device made with a dielectric having a small electron affinity and a large band gap, Al_2O_3 here, than that for the device made with a dielectric having a large electron affinity and a small band gap, HfO_2 here. Al_2O_3 and HfO_2 devices with TaN bottom electrode show larger turn on bias and smaller current density in positive polarity in comparison to devices made on ZrCuAlNi bottom electrodes. This is due to a larger work function for TaN electrodes. Kelvin probe measurements show TaN has approximately 0.5 eV larger work function; extraction from I-V plots also confirms ~0.5 eV larger work function for TaN.

Devices made on TaN should have larger asymmetry (η) due to larger $\Delta\varphi$ -top electrode is Al which is the same for both devices on TaN and ZrCuAlNi. This is evident in Fig.1 (b). However, a major discrepancy from simulations is observed for HfO_2 devices made on ZrCuAlNi bottom electrodes. The log (η) values for these devices are below 1 indicating larger current response at positive polarities. We have also reported it in our previous work.[17] Regarding the measurement set up, tunnel diodes show larger current density in negative polarity than positive polarity for the same amount of applied bias. As shown in f_{NL} vs. V plot in Fig. 8.1(a), an abrupt increase in f_{NL} occurs earlier in

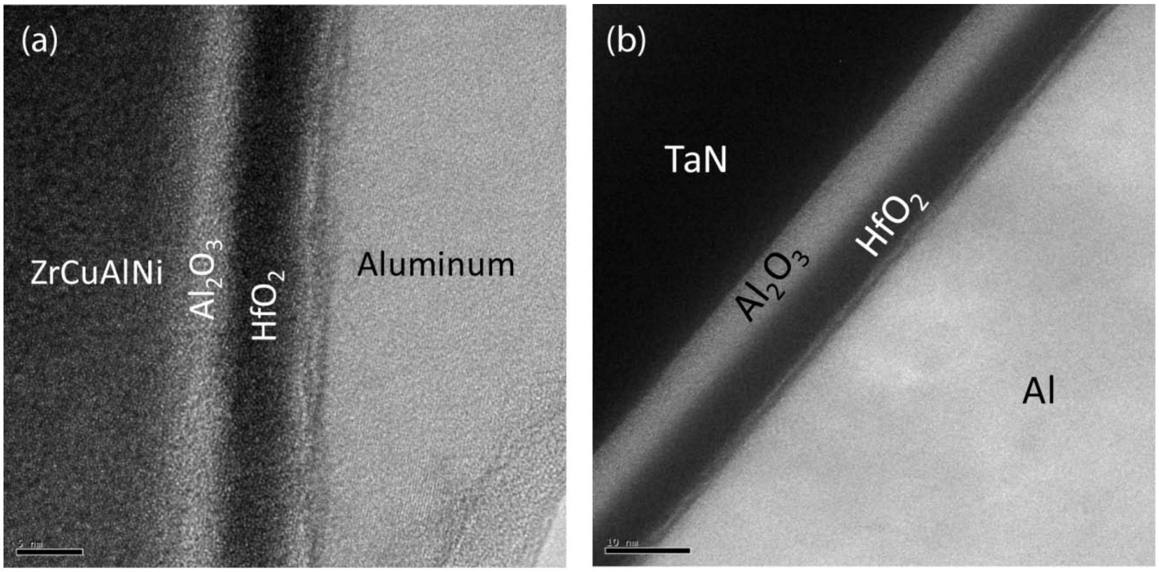

Fig.8.2: TEM cross section images of devices made with 5nm Al_2O_3-5nm HfO_2 dielectrics and aluminum top electrodes on (a) ZrCuAlNi bottom electrode, and (b) TaN bottom electrode.

positive polarity for HfO_2 confirming that HfO_2 devices on TaN turn on at smaller positive bias than expected from band diagram simulations. It should note that an abrupt increase in f_{NL} value indicates a change in conduction mechanism, turn-on bias here. This disagreement could be explained by studying the interfaces between the bottom electrode and HfO_2 and Al_2O_3 dielectrics. Shown in Fig. 8.2 are TEM cross section images of devices made with 5nm Al_2O_3-5nm HfO_2 dielectrics and aluminum top electrodes on (a) ZrCuAlNi bottom electrode, and (b) TaN bottom electrode. An approximately 2 nm interfacial layer between Al_2O_3 and ZCAN bottom electrode is seen in Fig. 8(a) while the interface between TaN bottom electrode and Al_2O_3 dialectic layer is clean without any interfacial layer.

To further study the nature of interfacial layer between ZCAN and TaN bottom electrodes and HfO_2 and Al_2O_3 dielectrics, X-ray photoemission spectroscopy (XPS) is employed. Shown in Fig 8.3 are XPS profiles for devices made with 10nm Al_2O_3 and 10nm HfO_2 on ZCAN and TaN bottom electrodes.

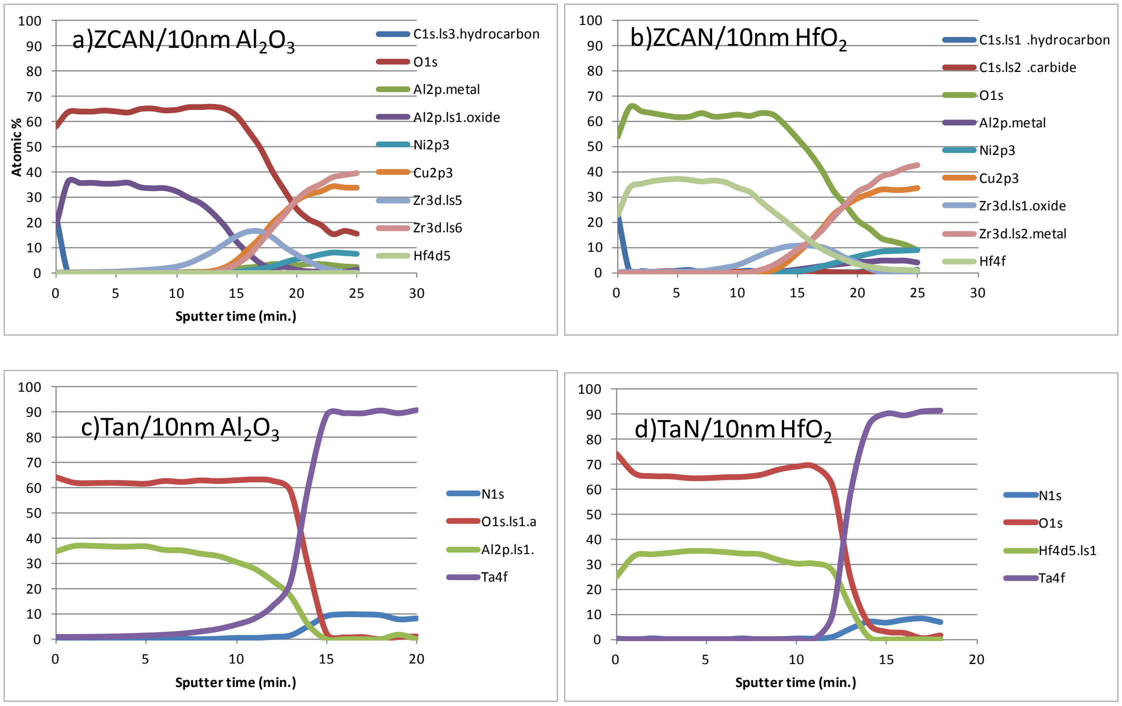

Fig.8.3: XPS profiles of (a) 10nm Al_2O_3 and (b) 10nm HfO_2 films on ZrCuAlNi bottom electrodes, and (c) 10nm Al_2O_3 and (d) 10nm HfO_2 films on TaN bottom electrodes.

Our thermodynamic simulations show Zr in ZrCuAlNi (% 40 atomic percentages) reduces HfO_2 to form ZrOx layer at ZrCuAlNi-HfO_2 interface. However Ta in TaN electrodes cannot reduce HfO_2. XPS investigations shown in Fig. 8.3 confirm the formation of ZrOx layer. Further thermodynamic simulations also reveal the formation of the ZrOx interfacial layer at ZrCuAlNi-Al_2O_3 interface as Zr reduces Al_2O_3 while there is no interfacial layer predicted by simulation at TaN-Al_2O_3 interface. However, I-V curves do not show evident influence of ZrOx IL in electrical properties for Al_2O_3 diodes on ZrCuAlNi. As shown in Fig. 8.4, XPS profiles of 10nm HfO_2 films on TaN bottom electrodes revealed that HfO_2 films are partially reduced by Ta in TaN bottom electrode to Hf in metallic state. To investigate the role of ZrOx IL in electrical properties of Al_2O_3 and HfO_2 devices, energy band diagram simulations are employed. Fig. 8.5 shows the energy band diagrams of devices made with 10 nm Al2O3 on either TaN, ZCAN, or Ta. The formation of ZrO_x and TaO_x interfacial layers on ZCAN and TaN bottom electrodes considered respectively. As shown in Fig. 8.5 (b), the zirconium rich IL could increase the asymmetric I-V response due to step tunneling which occurs in negative polarities.

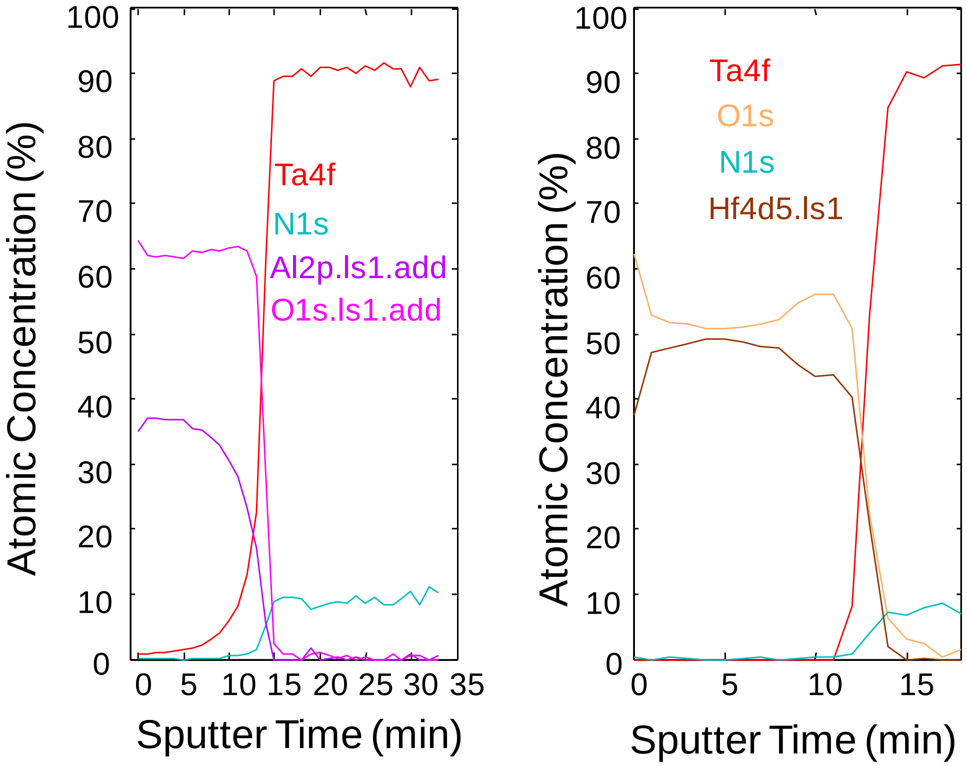

Fig.8.4: XPS profiles of 10nm HfO_2 films on TaN bottom electrodes.

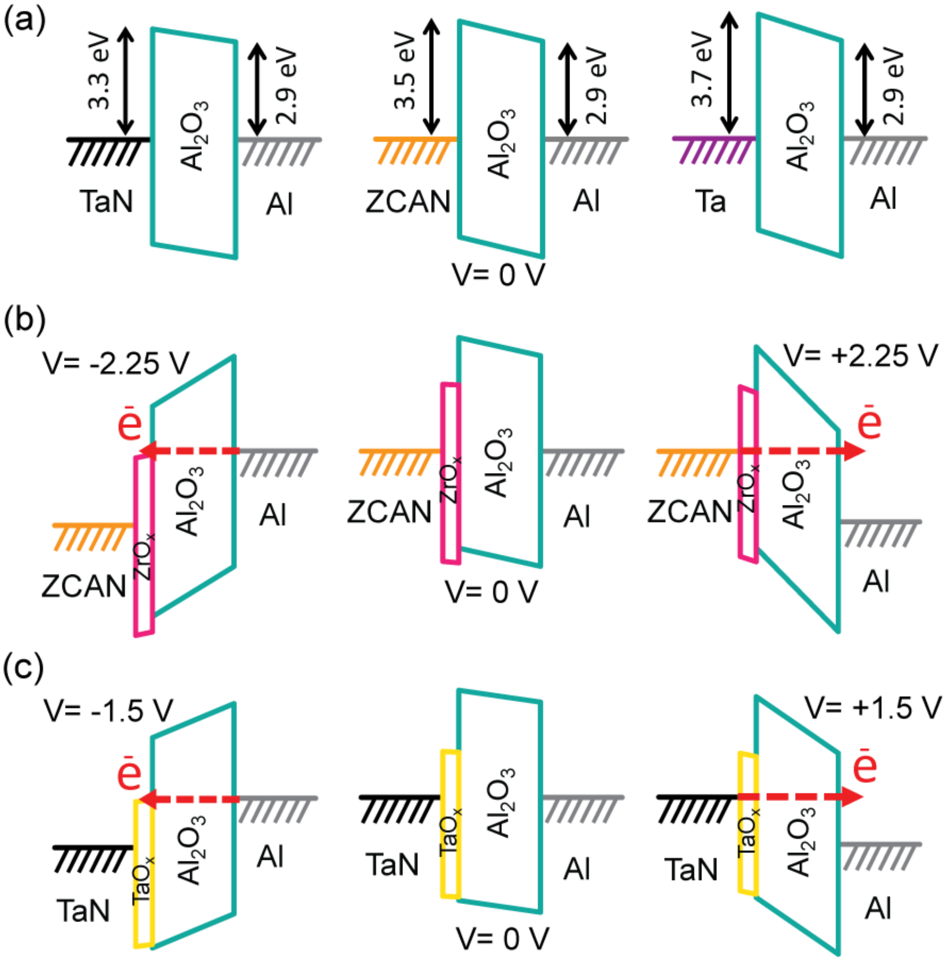

Fig. 8.5: (a) Band diagrams of MIM diodes having TaN, ZCAN, and Ta as bottom electrodes, 10nm Al_2O_3, and Al top electrode in equilibrium. (b) Band diagrams illustrating diodes consisting of ZCAN bottom electrode, 2nm native oxide rich in Zr, 10nm Al_2O_3, and Al top electrode under negative bias (left), equilibrium (center), and positive bias (right). (c) Band diagrams illustrating diodes consisting of TaN bottom electrode, 2nm native oxide rich in Ta, 10nm Al_2O_3, and Al top electrode under negative bias (left), equilibrium (center), and positive bias (right).

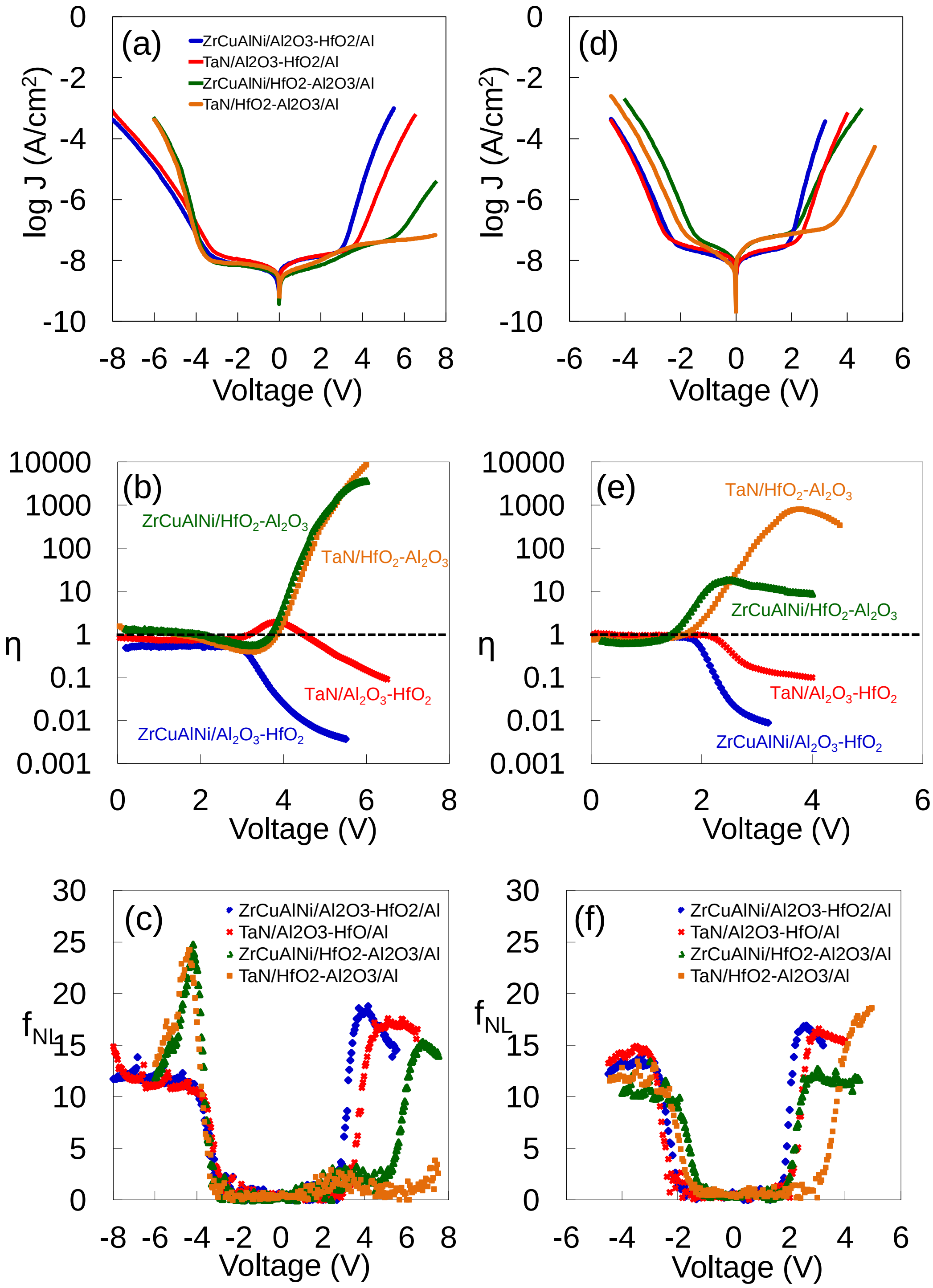

Fig. 8.6: Plots of (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V for 5nm Al_2O_3/5nm HfO_2 and 5nm HfO_2/5nm Al_2O_3 stacks deposited on ZrCuAlNi and TaN bottom electrodes with Al top electrodes. (d), (e), and (f) for 2.5nm Al_2O_3/2.5nm HfO_2 and 2.5nm HfO_2/2.5nm Al_2O_3 stacks.

Fig. 8.5 (c) illustrates the occurrence of step tunneling again in negative polarities due to the tantalum rich IL for devices made on TaN bottom electrode. This could increase the asymmetric I-V response in these devices.

Finally shown in Fig 8.6 are plots of (a) log (J) vs. V, (b) log (η) vs. V, and (c) f_{NL} vs. V for 5nm Al_2O_3/5nm HfO_2 and 5nm HfO_2/5nm Al_2O_3 stacks deposited on ZrCuAlNi and TaN bottom electrodes with Al top electrodes. (d), (e), and (f) for 2.5nm Al_2O_3/2.5nm HfO_2 and 2.5nm HfO_2/2.5nm Al_2O_3 stacks. The asymmetry plots clearly show the enhancement of asymmetry using HfO_2 and Al_2O_3 stacks for devices made on either TaN or ZCAN bottom electrodes.

8.4 Summary

The impact of interfaces on the performance of MIM and MIIM tunnel devices was investigated. The formation and influence of interfaces in MIM devices and especially when a nanolaminate tunnel barrier is employed in the structure, are of utmost importance. It was found that a few angstrom thick native oxide on bottom electrode can change and even overwhelm electrical properties of tunnel devices. The formation of a native oxide layer at electrode-dielectric interface would be inevitable regarding the thermodynamics between dielectric and electrode films. While no significant interactions or formation of unexpected interfaces were found between dielectric layers in nanolaminate structures studied in this work; TEM and XPS characterizations revealed a zirconium rich native oxide interfacial layer between ZrCuAlNi bottom electrodes and dielectrics. This zirconium reach native oxide at ZrCuAlNi-HfO_2 interface was found to reverse asymmetric response in MIM diodes made with HfO_2 dielectric layer. Further investigations on formation of interfacial layer between bottom electrodes and dielectrics studied in this work, showed that zirconium rich native oxide forming at electrode–dielectric interfaces for using ZrCuAlNi bottom electrode, does not affect or diffuse through dielectric films. For using TaN bottom electrodes, the interfacial TaOx can form on the surface of TaN bottom electrodes, and tantalum can diffuse through Al_2O_3 and HfO_2 dielectric films and get oxidized. It is found that tantalum in non-stoichiometry TaN bottom electrodes can reduce HfO_2 films and produce metallic hafnium.

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CHAPTER 9

Summary

9.1 Conclusions

The objective of this research work in this dissertation is to fabricate and investigate high quality, well-functioning tunneling devices. The feasibility and advantages of the atomic layer deposition (ALD) technique to deposit dielectric films independent of the choice of the electrodes were studied. Whereas most previous experimental work on MIM diodes has been conducted on native oxides produced by either oxidation or nitridation of the bottom metal electrode, the use of ALD in this work allowed deposition of high quality single layer and nanolaminate bilayer insulators. Using these high quality ALD dielectrics, the impact of bottom electrode roughness on MIM diode performance, the choice of the dielectric and the dominant conduction mechanism through the dielectric films, the impact of nanolaminate insulator bilayers on MIIM diode operation, and the role of interfaces were explored.

In the first part, chapters 2 and 3, the performance of MIM tunnel diodes with ALD Al_2O_3 insulator tunnel barriers on low work function (ZrCuAlNi and Al) and high work function (Ir and two types of Pt) bottom electrode materials with RMS roughness levels ranging from ~3% to greater than 100% of the insulator thickness was investigated. It was demonstrated that the roughness at the bottom metal interface can overwhelm the influence of metal work function on the electrical characteristics of M_1IM_2 diodes, even reversing the trends expected based on $\Delta\Phi_M$. It was also shown that the percentage yield of functioning devices tracks higher with decreasing roughness and that even for nominally the same metal (Pt), the level of roughness dominates electrical properties and yield. These results indicate that bottom electrode roughness levels of much less than 20% of the insulator thickness are necessary to achieve non-roughness dominated electrical behavior, suggesting that many previous MIM tunnel diode studies may have been compromised by uncontrolled bottom electrode roughness.[1-20] By combining uniform tunnel barriers deposited via ALD with ultrasmooth (~0.3 nm RMS) bottom electrodes, highly non-linear and asymmetric MIM tunnel diodes with good device to device uniformity and stable J-V behavior have been demonstrated. It was discussed that if rough bottom electrodes are used, the few functioning devices obtained do not exhibit ideal I-V characteristics and do not perform reliably- they do not show identical turn-on bias over time and large hysteresis in their I-V response. Bias stressing reliability investigations showed, a reliable operation of tunnel diodes cannot be met for diodes made on not atomically smooth electrodes. These devices made on rough bottom electrodes broke down in bias regimes much smaller than the breakdown bias expected the constituent dielectric films.

In the second part, chapters 4 and 5, the operation of MIM tunnel diodes is studied through the choice of the dielectric layer in the MIM structures. A broad range of dielectrics including Nb_2O_5, Ta_2O_5, ZrO_2, HfO_2, Al_2O_3, and SiO_2 films were deposited by ALD to study the impact of dielectric layer on the asymmetric operation of diodes as well as the turn-on bias of the devices. It is found that although dielectrics with large electron affinity such as Nb_2O_5 and Ta_2O_5 are promising candidates to achieving low bias asymmetric operation in tunnel diodes; they are not good choices a tunnel barrier because the dominant conduction mechanism of electrons through them is not tunneling. Schottky emission and Frenkel-Poole emission were found as the dominant conduction mechanism in Nb_2O_5 and Ta_2O_5 ALD films in small ($V_{appl.} < 0.5$ V) and large bias ranges ($V_{appl.} > 0.7$ V); respectively. Optical dielectric constants and trap energy levels for these dielectrics were extracted from appropriate conduction plots. ZrO_2 films were also found to be dominated by Frenkel-Poole conduction mechanism. Below room temperature measurements revealed that Folwer-Nordhiem tunneling conduction with characteristic knees in the I-V behavior is seen in temperatures as low as 150° K. The dominant conduction mechanism in Al_2O_3, and SiO_2 films were determined to be Fowler-Nordhiem tunneling. Although fitted conduction plots showed tunneling as the dominant conduction mechanism in HfO_2 films. Defect assisted tunneling was found to dominate electron conduction in HfO_2 MIM devices because Arrhenius plots display temperature dependency in HfO_2 I-V behavior. As expected for devices work based on Fowler-Nordhiem tunneling, Arrhenius plots showed that Al_2O_3 and SiO_2 devices are not sensitive to temperature. Characteristic knees in I-V response following with more than 10^3 rise in current response are observed for MIM devices made with HfO_2, Al_2O_3, and SiO_2 proving these dielectrics as proper choice for the tunnel barrier in tunneling devices.

In the third part of this dissertation, chapters 6 and 7, an additional approach to achieving asymmetric and non-linear operation is investigated in which a nanolaminate pair of insulators (each with different E_G and χ) are used to create asymmetric tunnel barrier MIIM devices. In MIIM devices, electrons tunneling from one metal electrode to the other are presented with a different barrier shape depending on the direction of tunneling. It was demonstrated that high quality nanolaminate bilayer tunnel barriers deposited via ALD dominate the electrical characteristics of asymmetric metal electrode M_1IIM_2 devices. I-V asymmetry and non-linearity were found to be sensitive to the arrangement of the individual insulator layers with respect to the different metal electrodes ($M_1I_1I_2M_2$ vs. $M_1I_2I_1M_2$). Depending on whether the smaller χ insulator was adjacent to the smaller or larger Φ_M electrode, respectively, the bilayer dielectrics were arranged to either enhance or oppose (even reverse) the $\Delta\Phi_M$ induced asymmetry. Using band diagrams and assuming that conduction is dominated by tunneling mechanisms, these results are qualitatively well explained by step tunneling phenomenon. By combining two methods of producing asymmetry, asymmetric metal electrodes and a bilayer dielectric tunnel barrier, we were able to achieve excellent low voltage asymmetry and non-linearity in a ZrCuAlNi/HfO_2/Al_2O_3/Al diode exceeding both that of standard single dielectric layer asymmetric electrode M_1IM_2 devices as well as recently reported symmetric electrode $M_1I_1I_2M_1$ devices. It was also demonstrated that the relative thickness of the insulator layers may be used to further tune electrical behavior.

Finally in the fourth part, chapter 8, the impact of interfaces on the performance of MIM and MIIM tunnel devices was investigated. The formation and influence of interfaces in MIM devices and especially when a nanolaminate tunnel barrier is employed in the structure are of utmost importance. It was found that a few angstrom thick native oxide on the bottom electrode can change and even overwhelm the electrical properties of tunnel devices. The formation of a native oxide layer at the electrode-dielectric interface would be inevitable regarding the thermodynamics between dielectric and electrode films. While no significant interactions or formation of unexpected interfaces were found between the nanolaminate dielectric layers studied in this work; TEM and XPS characterizations revealed a zirconium rich native oxide interfacial layer between ZrCuAlNi bottom electrodes and dielectrics. This zirconium reach native oxide at ZrCuAlNi-HfO_2 interface was found to reverse the asymmetric response in MIM diodes made with HfO_2 dielectric layer. Further investigations on the formation of interfacial layers between bottom electrodes and dielectrics studied in this work showed that a zirconium rich native oxide forming at ZrCuAlNi bottom electrode–dielectric interface, does not affect or diffuse through dielectric films. For using TaN bottom electrodes, an interfacial TaO_x can form on the surface of the TaN, and tantalum can diffuse through Al_2O_3 and HfO_2 dielectric films and get oxidized. It is found that tantalum in non-stoichiometry TaN bottom electrodes can reduce HfO_2 films and produce metallic hafnium.

Overall, it was shown that combining uniform tunnel barriers deposited via ALD with ultrasmooth bottom electrodes, allows for the fabrication of Fowler-Nordheim tunneling dominated MIM devices. It was also clearly experimentally demonstrated that nanolaminate insulator tunnel barrier MIIM devices are a powerful way to enhance or tune the asymmetry and non-linearity of asymmetric metal electrode. The importance of the interfacial layer formation on tunnel devices performance was reported. The good reproducibility, stable I -V behavior, and percentage of working devices along with the enhanced properties achieved combining insulator bilayers with asymmetric work function electrodes represent an advancement toward the understanding necessary to engineer thin film MIIM tunnel devices for commercial microelectronics applications.

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APPENDICES

Appendix A. Atomic Layer Deposition

Atomic layer deposition (ALD) is a gas phase thin film deposition method which can be considered as a special modification of chemical vapor deposition (CVD) technique.[1] ALD utilizes sequential precursor gas pulses to deposit a film one layer at a time. In ALD, the precursors are conducted into the reaction chamber in alternate pulses whereas in CVD, the precursors are simultaneously led into the reaction chamber. Fig. A.1 illustrates an ALD system.[2] As shown in Fig. A.1, the ALD process follows the flow of the precursors from the precursor source into the deposition chamber where the substrate is positioned and the deposition occurs. The alternate precursor pulses in ALD are separated by inert gas purging in flow type reactors which is used as thermal ALD in this work.[1] In high-vacuum type reactors, the alternate precursor pulses in ALD are separated by evacuation of the reactor which is widely used for plasma enhanced atomic layer deposition especially for metallic films.[3] Advantages of ALD deposition technique are including superior thickness uniformity over a substrate, excellent conformality for aspect ratios as large 200:1, dense films, sharp interfaces, low energy deposition, and stochiometric films.[1,3-5] As one monolayer of the ALD films is deposited at a time, a slower growth rate in comparison to other deposition techniques is the main disadvantage of ALD.

The precursors react with the surface groups on the substrates after releasing into the chamber. This surface reaction is often called “chemisorption” on the substrate surface.[5] If process conditions are perfectly chosen, the surface reactions are self-limiting,

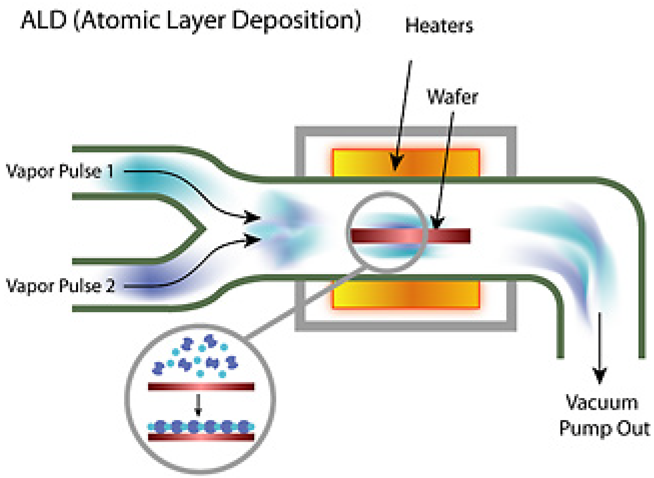

Fig. A.1: A simple illustration of an ALD system.[2] As shown precursors are introduced in vapor state into the deposition chamber from separate lines. Wafer substrates are positioned in a chamber which can be heated to adjust the deposition temperature.

which leads to highly controlled film growth.[4] The first precursor gas is introduced into the process chamber and produces a monolayer of gas on the substrate. Then, a second precursor gas is introduced into the chamber and reacts with the monolayer produced from the first gas. As each pair of gas pulses produces exactly one layer of the desired film in ideal growth condition, the thickness of the final film is precisely controlled by the number of precursor pulses. One ALD cycle means all the pulses required to produce one layer of the desired film. In this study, one atomic layer of the dielectric films deposited by one pulse of metal organic precursor and one pulse of water as the oxidant which make one ALD cycle.

The ALD precursors are kept in source vessels. Depending on the chemical, it can be either in gaseous, liquid, or solid form. A sufficient flow amount of the precursor material must feed into the deposition chamber to saturate the surface of the substrate and an ideal film deposition occurs. To deposit high quality films especially for electronic applications, self-limiting and saturated growth are critically required to achieve.[5] Saturated growth occurs if all the active bands available on the surface after each precursor pulse react with the next precursor. This leads to a uniform and dense ALD film. This is of utmost importance for electronic applications to minimize the amount of intrinsic defects such as vacancies and pin holes in the film.[4-6]

The precursor flux is very small compared to the gas flow required in CVD techniques as just one layer of atoms are deposited on the surface in each pulse of precursors into the chamber. In flow type reactors like the ALD tools used in this work, 1 m Torr of precursor is typically required to introduce into the chamber in each pulses of precursors.[5] Thus, the precursor flexibility is limited by the vapor pressure of the precursor material. If a precursor is in gaseous state in room temperature then it would easily provide 1 m Torr required vapor pressure in room temperature.[4] This is the case for trimethylaluminum (TMA) precursor used to deposit Al_2O_3 in this work. However, a majority of metal organic precursors used in this work are either in liquid or solid states. These precursors do not reach required vapor pressure in room temperature; thus, they are heated to higher temperatures to increase their vapor pressure. The vessels to keep low vapor pressure precursors are called solid sources. ALD manufacturers employ various techniques to heat these precursors and flow their vapor into the deposition chamber efficiently.

The precursors can thermally decompose either when they are heated in the sources or when they are introduced into the deposition chamber. Thermal selfdecomposition of the precursors is a very critical issue which has to be avoided as it destroys the self-limiting film growth mechanism, and the process can no longer be considered an ideal ALD process.[1,5] Two important issues should be considered. First, precursors should be carefully heated below their decomposition temperature so there is compensation between increasing the precursor temperature to increase its vapor pressure and keep the precursor below the decomposition temperature. As vapor pressure rises exponentially with increasing the temperature, the required vapor pressure can be achieved in a temperature below a precursor decomposition temperature. However, it is mostly preferred to introduce precursor vapor with a larger vapor pressure into the chamber to saturate the substrate more uniformly over a large area with shorter pulses of precursor and then shorter purge times. Short pulse and purges are desired to make the deposition faster and to avoid desorption of chemisorbed species from the surface.[4] As mentioned above, saturated film growth is highly desired and desorption of species from the surface can occur in long purges which lead to unsaturated growth. If the surface reactions become saturated, a constant growth rate of films is obtained over the whole substrate, and films with excellent electrical properties, conformality and uniformity can be deposited. Second, the deposition temperature should keep below the precursor decomposition temperature. The deposition temperature for metal oxides is normally desired to be higher than 200° C to obtain high quality as deposited films.[5] On the other hand, if the deposition temperature is too high, the precursor vapor can thermally decompose and the chemisorbed species on the substrate surface can desorbed from the surface. So ALD films should be deposited in a well- adjusted chamber temperature.

As mentioned above, a set of successive pulses of two or more precursors, separated by purges, is called an ALD cycle. The film growth rate is usually measured as the film thickness deposited during one ALD cycle. Hence the film thickness can be accurately controlled by the number of the ALD cycles. The pulse valves control the introduction of the precursors into the deposition chamber are often called ALD valves. To inhibit reactions between precursors in the deposition chamber ambient each precursor pulse into the chamber has separated by a purge period. During purge periods an inert gas flows into the chamber and purges out all the remaining vapor of a precursor in the chamber as well as all the byproducts of the ALD deposition reactions. Nitrogen is used as an inert gas in the ALD tools used in this study. The ALD valves have constant flow of nitrogen as well to transports the precursors to the deposition chamber. When an ALD valve is opened to the precursor line, the precursor diffuses into the nitrogen flow and then is transported to the deposition chamber. After the precursor is introduced into the chamber, the precursor ALD valve gets closed and chamber is purged by the nitrogen flow to remove excess precursor and deposition byproducts.

The chemical reactions responsible for film growth in an ALD system occur when a second precursor is introduced into the chamber. The second precursor completely saturates the surfaces of the substrate which have been already saturated by the first precursor. The deposition temperature in the chamber is set to ensure the reaction between the two precursors on the substrate occurs. Thus, the film growth in an ALD reactor is achieved through two or more alternating precursor pulses. The pulse and purge time of each precursor should be therefore adjusted to ensure that each precursor has fully saturated the substrate surface and any remaining precursor vapor and byproducts of deposition reactions have been evacuated from the chamber.

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Appendix B. Materials and Electrical Characterizations

The materials and electrical characterization techniques used to characterize MIM tunnel diodes are briefly discussed here. Material characterizations including atomic force microscopy (AFM), Kelvin probe analysis, transmission electron microscopy (TEM), and x-ray photoelectron spectroscopy (XPS), are reviewed firstly. Second, electrical characterization technique which is current versus voltage measurements in DC mode is reviewed.

Surface morphology studies of bottom electrodes investigated in this work has been done via atomic force microscopy (AFM). AFM analysis is able to measure root mean square (RMS) roughness as low as two angstroms. AFM analysis can be applicable to both insulating and conducting surfaces.[1] Roughness detection capability in the order of a few angstroms can be achieved by monitoring the deflection of a rigid cantilever possessing a sharp tip.[1] The deflection of the cantilever is quantified through the use of a laser focused on the cantilever surface. The laser light reflected by the cantilever is monitored via a photodiode. As the sample is moved under the cantilever, the sample surface morphology changes the position of the reflected light on the photodiode. Processing of the laser position on the photodiode allows for an assessment of the sample surface morphology. Contact mode and tapping mode are two common modes of AFM operation. Contact mode is used mainly for surface morphology characterizations. Hence, the contact mode is used to analysis the surface morphology of bottom electrodes studied in this work.

Kelvin probe analysis is a surface sensitive technique used to study the surface potential and eventually work function difference ($\Delta\Phi = \Phi_{M1}-\Phi_{M2}$) of electrodes used in MIM structures. The surface potential can be measured through the modulation of the electric field between the surface of the sample and a reference electrode.[2] As Kelvin probe systems work based on the sample, the reference electrode, and the air between them to make an MIM capacitor, the Kelvin probe analysis is very sensitive to the ambient of the measurements.[3] Surface effects can change the surface potentials witch influence the measured work function. Thus, relying solely on Kelvin probe analysis could be susceptible to false work function evaluation. To avoid this problem, work function analysis should be reexamined by I-V measurements. In the case of MIM devices that have FN tunneling as the dominant conduction mechanism, work function difference can be extracted from Fowler-Nordheim conduction plots. The Kelvin probe system used in support of this research is a KP Technology LTD SKP5050 operated under air ambient.

Although dielectric thicknesses of MIM diodes in this work have measured by ellipsometry, the thickness of the dielectric layer in some of the devices is also measured by transmission electron microscopy (TEM). This is specifically the case for MIIM devices with stacked dielectric layers. The TEM characterization is also a very powerful technique to investigate the interfacial layers between electrodes and dielectrics as well as two dielectrics in nanaolaminate structures. Transmission electron microscopy (TEM) employ electrons generated and detected in a vacuum system to achieve imaging resolution in the order of a few angstroms. TEM can take images of conducting and insulating materials with resolution less than 1 nm.[4] An electron beam is focused electrostatically onto the sample and is collected after passing through the sample under analysis. The beam is focused onto a sample surface via a series of electrostatic lenses, and then is applied over the analysis area. Electrostatic lenses located on the far side of the sample relative to the electron source focus the electrons passing through the sample to a detector for imaging.[4] The energy of the impinging electrons used in TEM analysis is approximately 200 keV.[5] The thickness of the material under analysis should be thin to allow for sufficient transmission of incident electrons. Hence, the uniformity of sample thickness in TEM analysis can directly influences the quality of analysis due to the contrast dependence on sample thickness. The tool used to prepare samples for TEM analysis is a Quanta 3D dual Beam focused ion beam tool (FIB). The TEM images were taken on a FEI Titan 80-200.

X-ray photoelectron spectroscopy (XPS) is a surface chemical analysis technique used to study the formation of interfacial layers in MIM devices.[6] XPS employs incident x-rays that excite photoelectrons from a surface. The photoelectrons analyzed in XPS have low kinetic energy, typically less than 2000 eV.[6] Low energy photoelectrons have short inelastic mean free paths in a solid material. Therefore, the photoelectrons that are analyzed in XPS originate very near the material surface, typically within 2 nm of the surface.[7] The kinetic energy spectra of emitted core photoelectrons are characteristic of the material’s surface composition. The oxidation states of surface atoms are determined through the analysis of photoelectron kinetic energy shifts away from the characteristic deoxidized spectra. Compositional and oxidation state analysis through the thickness of a sample is performed through depth profiling. The process of XPS depth profiling generally consists of sequential data collection and sputtering. XPS data is collected from the sample surface after which a controlled amount of the sample material is removed, revealing material below the initial surface. Chemical changes due to the sputtering process must be accounted for in depth profiling. Sequential material removal and XPS data collection provides compositional and oxidation state information through the thickness of a sample. XPS measurements of this work were performed in a Physical Electrons Quantera Scanning ESCA Microprobe with a focused monochromatic Al Kα Xray (1486.7 eV) source for excitation. The X-ray beam used was a 40 W, 200 μm X-ray beam spot on the sample.

The dynamic dielectric constant and optical dielectric constant of ALD dielectrics studied in this work are investigated via variable angle spectroscopic ellipsometry (VASE).[8] This technique is also used to measure the film thickness. The change in polarization state of incident polarized light reflected from or transmitted through the surface of a sample is measured in this characterization technique. The amplitude ratio (Ψ) and the phase difference (Δ) between orthogonal reflected polarized light are measured. The accuracy and the sensitivity of VASE measurement are defined by Ψ and Δ respectively.[8] The film and materials parameters such as thickness and the depth profile of the dielectric function are determined by modeling and fitting of the collected data. The intensity of the incident polarized light reflected from the sample surface is detected. Then, the materials dielectric response is determined by modeling the measured intensity data. The modeling of the dielectric response is improved in VASE as multiple angles of light incidence and multiple discrete wavelengths are employed. A J. A. Woolam variable angel spectroscopic ellipsometer was employed in this work. A wide spectrum xenon light source is used to generate the incident light. Ψ and Δ were acquired at wavelength from 300 nm to 1500 nm and incident angles of 60°, 65°, and 70°. The dielectric responds spectrum of films were modeled and calculated using a non-linear least squares fit of the polarized reflectance data.

MIM diodes in this work are characterized by their current-voltage (I-V) characteristics. The DC current-voltage characteristics presented are obtained using an Agilent 4155C Semiconductor Parameter Analyzer (SPA). The noise floor of the system is estimated to be on the order of 10^2 pA. The bottom electrode (M1) was always held at ground with bias applied to the Al top gate (M2). To mitigate the impact of displacement current, all I-V curves were swept from zero bias to either the maximum positive or negative bias. Displacement current is an artifact of measurements. Displacement current is a function of the capacitance of the device as well as sweep parameters. Sweep parameters influencing the displacement current are integration time, hold time, and the delay time. Integration time is the time the SPA tool integrates current response of a device to decrease the noise contribution to the measurement. The hold time is the time the first step of the sweep applied on the device without measuring the current response. Hold time can be used to stabilize the device under measurement before recording the measured data. The default testing parameters are hold time of 500 m seconds, delay time of 200 m seconds, and medium integration time of 62 m seconds.

Devices are contacted using tungsten probes on a BNC-based micromanipulator probe station. The electrical measurement technique for a MIM tunnel diode is similar to that used for a two terminal resistor. A voltage is applied and is swept between the two diode electrodes while a current is measured. The magnitude of the applied voltage is varied depending on the thickness and the choice of the tunneling dielectric. A diode with a thinner tunneling dielectric has a smaller voltage range applied than a diode with a thicker tunneling dielectric. A diode is considered functional when the measured I-V relationship is nonlinear, and a current magnitude of greater than 0.2 μA is achieved through the application of both positive and negative voltages. Contact to the bottom electrodes is made by scratching through the ALD dielectric layer with a diamond tip scriber, after which an indium solder is deposited. The indium solder melting point is approximately 160° C.

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Appendix C. Simulations

The I-V plot simulations of this work have been performed using Matlab software. General Fowler-Nordheim equation has been used to simulate the I-V characteristics of devices. We have performed tunneling based modeling of the I-V characteristics for MIM and MIIM devices. Shown in Fig. C.1 and Fig. C.2 are tunneling based simulations of the MIIM devices from Fig. 6.3 and Fig. 6.4, respectively. For the modeling, the equation developed by Simmons[1,2] was employed to describe FN tunneling between dissimilar (asymmetric work function) electrode M_1IM_2 structures:

$$J = C_1 \frac{1}{\varphi_b} (\xi_{ox})^2 \exp\left(- \frac{C_2 \ \varphi_b^{\frac{3}{2}}}{\xi_{ox}} \right), \tag{C.1}$$

where,

$$\xi_{ox} = \frac{V + \Delta\varphi}{S} \quad (V/cm), \tag{C.2}$$

$$C_1 = \frac{q^3}{16\pi\hbar} \left(\frac{m}{m_{ox}} \right) = 1.54 \times 10^{-6} \left(\frac{m}{m_{ox}} \right) \quad (A/V^2), \tag{C.3}$$

$$C_2 = \frac{4\pi\sqrt{2m_{ox}}}{3q\hbar} = 6.83 \times 10^7 \left(\frac{m_{ox}}{m} \right)^{1/2} \quad (V/cm), \tag{C.4}$$

φ_b is the energy barrier between the electrode electrons are tunneling from and the tunnel barrier. $\Delta\varphi$ is the difference in barrier heights between the interfaces of the insulators with the top and bottom electrodes. ξ_{ox} is the electric field through the dielectric layer. q is elementary charge, $\hbar$ is the reduced Planck constant. m and m_{ox} are electron rest mass and the unit-less tunneling effective mass for electrons tunneling through the dielectric layer; respectively. S is the tunnel barrier thickness.

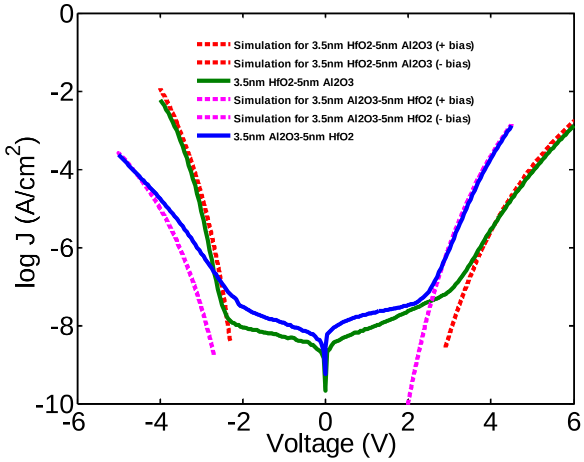

Fig. C.1: Experimental and simulated log (J) vs. V data for the thick $M_1I_1I_2M_2$ & $M_1I_2I_1M_2$ bilayer devices from Fig. 6.3(a).

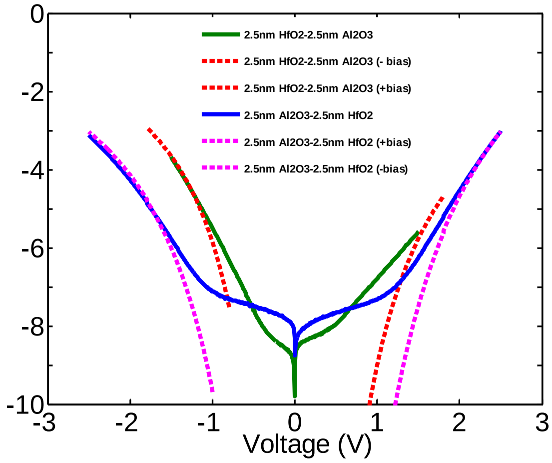

Fig. C.2: Experimental and simulated log (J) vs. V data for the thick $M_1I_1I_2M_2$ & $M_1I_2I_1M_2$ bilayer devices from Fig. 6.4(a).

It can be seen the tunneling simulations clearly predict the positive and negative bias post turn-on behavior of all thick (Fig. C.1) and thin (Fig. C.2) MIIM devices where tunneling is dominate conduction mechanism. The turn-on voltage at which the current rises sharply off of the baseline is also well predicted for the thicker bilayer devices in Fig. C.1, except at negative bias for the ZCAN/Al_2O_3/HfO_2/Al $M_1I_1I_2M_2$ device which turns on sooner than predicted. For the thinner devices in Fig. C.2, the turn-on voltages are fairly well predicted, but in all cases turn on occurs at lower voltages than predicted. Part of the reason for the departure of the simulations at low biases is that the low current levels cannot be measured by our experimental setup. However, since tunneling is the only conduction mechanism considered for these simulations, it is not surprising that the data does not always follow simulations in medium biases for all devices. Additional leakage conduction at low to medium biases can occur due to interface defects, "bulk" oxide defects, defect assisted tunneling, emission mechanisms such as Poole-Frenkel and Schottky, etc. The contributions of these other conduction mechanisms will be dependent upon the details of the device stack and insulator layer thicknesses. For example, the role of interface defects will be more important for thinner devices and indeed we see greater departure of our simulations at medium voltages for the thinner devices. In addition to the contribution of non-tunneling conduction mechanisms at low to medium biases, the reviewer should also appreciate that simulations of a dual-stack structure have additional complexities such as image force barrier lowering in the two barriers, potentially different effective masses for tunneling in the different insulator layers, the possibility of quantum-mechanical reflection at various interfaces.

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