AN ABSTRACT OF THE DISSERTATION OF

Yang Xu for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on March 16, 2017.

Title: Power-Efficient Design Techniques and Architectures for Scalable Submicron Analog Circuits.

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Un-Ku Moon

As the CMOS process scales down to submicron, digital circuit performance improves, while reduced supply voltage and lower transistor intrinsic gain make it difficult to implement analog circuits in a power efficient manner. Therefore, it has become advantageous to shift more analog signal processing functions conventionally realized in *voltage* (analog) domain into utilizing *charge* or *time* as the variable that can be processed by mostly digital/passive circuits. In this thesis, both circuit-level techniques and architectures are proposed that are inherently compatible with transistor scaling in submicron CMOS, meanwhile achieving state-of-the-art performance and optimizing power efficiency.

The first part focuses on a highly reconfigurable charge-domain switched-g_m-C biquad band-pass filter (BPF) topology that utilizes an interleaved semi-passive charge sharing technique. It uses only switches, capacitors, linearity-enhanced g_m-stages and digital circuitry for a 3-phase non-overlapping clock scheme. Flexible tunability in both center frequency and -3dB bandwidth is achieved with a scaling-compatible implementation. A 4^{th}-order BPF prototype operating at a 1.2GS/s sampling rate is designed with a cascade of two proposed biquads in a 65nm LPE CMOS process. A tunable center frequency of 35−70MHz is measured with programmable bandwidth and a maximum stop-band rejection of 72dB. The measured in-band IIP3 is +12.5dBm.

The filter prototype consumes 7.5mW total power from a 1.2V supply voltage, and occupies a core area of 0.17mm^2.

In the second part, a highly linear continuous-time low-pass filter (LPF) topology with source follower coupling is presented that achieves excellent power efficiency. It synthesizes a 3rd-order low-pass transfer function in a single stage using coupled source followers and three capacitors, and can be configured to 2nd-order by disconnecting a capacitor. A 5th-order Butterworth prototype is designed with a cascade of two proposed filter stages in a 0.18µm CMOS, and occupies a core area of 0.12mm^2. Operating with a 1.3V supply voltage, the filter consumes only 0.5mA current, and achieves a -3dB bandwidth of 20MHz with 82dB stop-band rejection. A total harmonic distortion (THD) of -39.5dB at the output is measured with a +6.6dBm (i.e. 1.35V_{pk-pk}) input signal at 2MHz. The measured in-band IIP3 is +28.8dBm. The dynamic range (at 1% THD) is 76.8dB, with 15.3nV/√Hz averaged in-band input-referred noise.

A pseudo-differential-VCO based 2nd-order continuous-time ΔΣ ADC with a residue self-coupling technique is proposed and implemented with mostly digital circuits in the third part. Two VCOs are arranged in a pseudo-differential manner. The digital output is obtained by comparing the sampled output phase of one VCO with that of the other. Passive subtraction is realized in current domain to obtain the residue at the VCO input. The residue self-coupling is implemented using a linear 1st-order transconductance low-pass filter (TCLPF). Moreover, a highly linear VCO topology is presented. The transistor-level simulations in a 65nm CMOS process show a 78dB SNDR over a 10MHz signal bandwidth with a power consumption of 2.9mW, which is 16dB improvement in contrast to the case with the TCLPF block powered off.

Power-Efficient Design Techniques and Architectures for Scalable Submicron Analog Circuits

by
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APPROVED:

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Yang Xu, Author

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I would like to dedicate this dissertation to my parents and wife. Again, I sincerely thank all who give me warm care and enthusiastic support in my life.

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POWER-EFFICIENT DESIGN TECHNIQUES AND ARCHITECTURES FOR SCALABLE SUBMICRON ANALOG CIRCUITS

CHAPTER 1. INTRODUCTION

With the rapid development of the Internet of Things (IoT), a flexible wireless receiver is desired to support multiple standards within a single radio. The block diagram of a typical receiver architecture [1-2] is shown in Fig. 1.1. The RF signal received at the antenna is firstly processed by a preselection band-pass filter to remove out-of-band signals. It is then amplified by a low noise amplifier (LNA) to suppress the noise contribution from the succeeding stages. The mixer down-converts the RF signal-band to intermediate frequency (IF). The IF filter, as one of the key analog baseband building blocks, is necessary to perform channel selection filtering. It is critical in determining the sensitivity and selectivity of a receiver. On the other hand, the analog-to-digital converter (ADC) plays an important role in digitizing the analog IF signal and generating its corresponding digital output that can be processed in a digital signal processor (DSP). Moreover, a variable gain amplifier (VGA) might be inserted to provide wide gain range and relax the dynamic range requirement on the ADC.

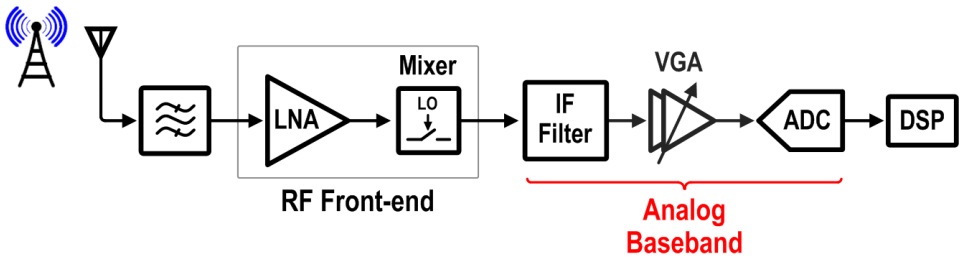


Figure 1.1: Block diagram of typical wireless receiver architecture.

The increasing popularity of portable electronic devices calls for a wireless receiver system with better sensitivity, more reconfigurability/programmability and decreasing power consumption for various applications. However, analog baseband blocks (i.e. IF filter to ADC) consume quite large power, for example 10.5−22.9mW in [3] accounting

for 34%−52% of the total power dissipation. What's more, as the CMOS process scales down to submicron, minimum transistor size decreases and the supply voltage reduces. While both RF and digital circuit performance improves with device scaling, analog circuits have not gained these benefits. As a result, it has become favorable to leverage increased digital circuit performance to mitigate analog circuit deficiencies. This thesis focuses on investigating new analog solutions in terms of circuit-level techniques and architectures that can be realized with a mostly digital/passive implementation. This allows compatibility with submicron scaling and high performance with improved power and area efficiency.

1.1 Research Motivation

Analog integrators are the fundamental building blocks in signal processing circuits with two examples being analog filters and ADCs. The three most commonly used circuit topologies to implement an analog integrator are depicted in Fig. 1.2.

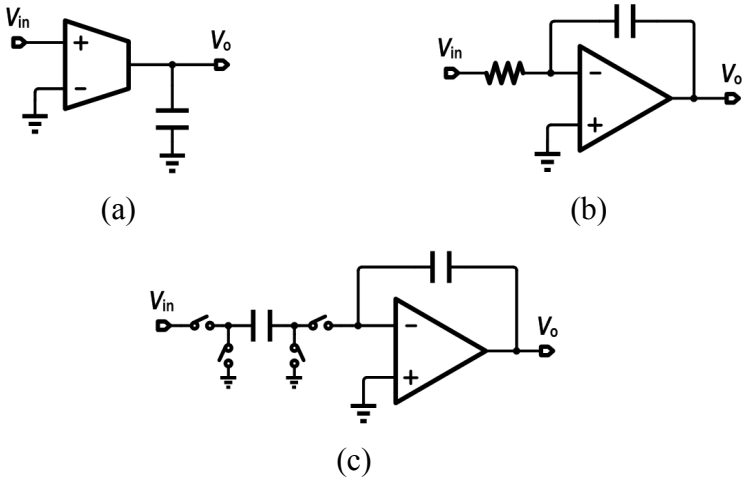


Figure 1.2: Conventional circuit topologies to implement an integrator: (a) g_m-C, (b) active-RC, and (c) active switched-capacitor.

The performance of such integrators depends on the operational transconductance amplifier (OTA). For example, a g_m-C integrator employs the OTA in an open loop to achieve high bandwidth, but suffers from poor linearity. Both active-RC and active switched-capacitor integrators use feedback to mitigate the OTA's nonlinearity but

result in much lower bandwidth compared to the g_m-C counterparts. In addition, limited OTA dc gain makes the integrator lossy, and the finite gain-bandwidth product (GBW) introduces a parasitic pole in the practical integrator transfer function that affects the response at high frequencies. Consequently, all types of analog circuits using the above integrator topologies require the OTA to have both high dc gain and wide GBW for desired system performance. However, in submicron CMOS processes, designing a high-quality OTA is increasingly challenging in a power efficient manner.

As the CMOS process rapidly scales down to submicron, the standard power supply voltage (V_{DD}) reduces to around 0.9V, while the transistor threshold voltage is about constant, as shown in Fig. 1.3. This would decrease the allowable signal swing, which consequently imposes a more stringent noise requirement for the same signal-to-noise ratio. Moreover, a smaller voltage headroom is resulted for each stacked transistor between V_{DD} and ground. On the other hand, shorter channel length lowers the transistor intrinsic gain, which further exacerbates the dc gain issue in conventional integrators. Techniques to increase the dc gain of the OTA include either cascoding or cascading multiple gain stages. Cascoding is generally more power efficient, but its effectiveness is negated by low supply voltage in submicron processes. A multi-stage OTA can achieve high gain but requires frequency compensation schemes which typically limit the OTA bandwidth and consume large power. Therefore, there is no clear solution to satisfying performance requirements in OTA-based analog circuits with little power penalty.

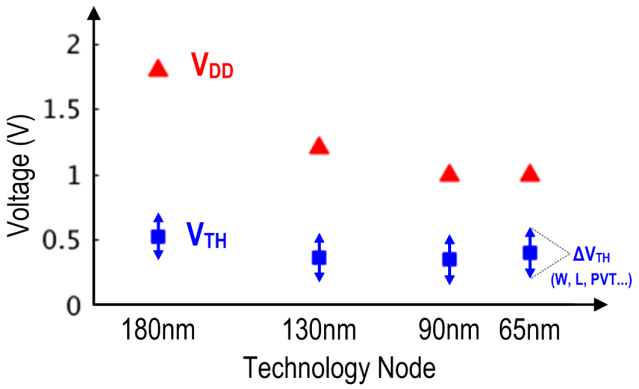


Figure 1.3: Power supply and threshold voltages vs. process scaling.

The major trend of emerging analog filters [4−5] and ADCs [6−8] is to shift more signal processing functions conventionally realized in *voltage* domain into utilizing *charge* or *time* as the variable that can be processed by mostly digital/passive circuits, as illustrated in Fig. 1.4. For example, the input voltage can be converted into current/charge that stores on a capacitor by using a transconductor. Passive charge-sharing operation [5] realizes a discrete-time IIR low-pass transfer function, in which capacitors, switches and a digital waveform generator are used. The *time* information has three types of representations which utilize different digital circuits to process. A pulse width modulator (PWM) generates a pulse whose width is proportional to the input voltage [9−10]. The pulse can be processed by a time-to-digital converter (TDC) to produce the corresponding digital code, or controls the charge pump to generate a voltage signal [4], [10]. A ring oscillator composed of delay cells converts the input voltage and generates an oscillator frequency that can easily processed by a counter to produce the digital code, and the oscillator phase can be digitized by a phase quantizer.

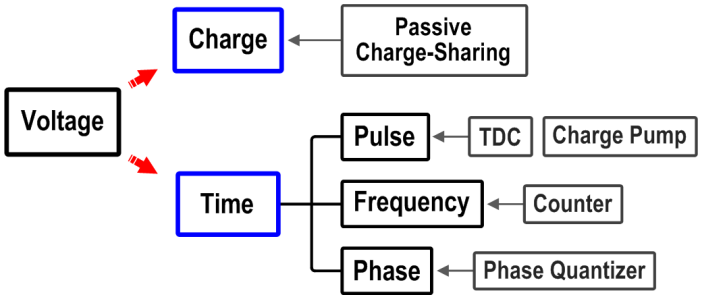


Figure 1.4: Utilization of *charge* or *time* as the variable instead of *voltage* for analog signal processing.

Analog signal processing circuit solutions using *charge* or *time* information with as many digital circuits as possible are desired, since they could operate faster, become smaller and consume less power. This thesis presents both circuit-level design techniques and architectures for analog circuits that are inherently compatible with submicron scaling, meanwhile achieving state-of-the-art performance and optimizing power efficiency.

1.2 Thesis Organization

The remainder of this thesis is organized as follows. Chapter 2 presents a highly reconfigurable charge-domain switched-g_m-C band-pass filter topology that utilizes an interleaved semi-passive charge-sharing technique. High in-band linearity is achieve with improved power efficiency in a scaling-compatible implementation. A highly compact continuous-time low-pass filter topology using source follower coupling is described in Chapter 3. The configurability of the proposed single-stage filter between 3^{rd}-order and 2^{nd}-order makes it a scalable topology to realize any order filters. In Chapter 4, a pseudo-differential-VCO based continuous-time ΔΣ ADC with a residue self-coupling technique is proposed and implemented with mostly digital circuits while achieving excellent power efficiency. Chapter 5 concludes this dissertation.

CHAPTER 2. CHARGE-DOMAIN SWITCHED-G_M-C BAND-PASS FILTER USING INTERLEAVED SEMI-PASSIVE CHARGE-SHARING TECHNIQUE

Band-pass filters (BPFs) with large flexibility in center frequency and bandwidth tuning are in demand, with decreasing power consumption, in multi-standard wireless receiver applications, such as super-heterodyne, etc. Moreover, the filter linearity is critical to the receiver performance, since the strong blocker signals can be modulated to generate undesired distortion products falling into the band-of-interest.

The BPF is typically implemented using either an active-RC [11] or a g_m-C [12] architecture, depending on frequency range and linearity requirements. The main focus in conventional designs is to improve the performance of OTAs used in the filter structure. For instance, a linearization technique is proposed for the transconductor (i.e. OTA) in [12]. However, the filter prototype still consumes large power.

In this chapter, a highly reconfigurable charge-domain switched-g_m-C band-pass filter topology utilizing an interleaved semi-passive charge-sharing technique is presented with improved power efficiency. Flexible tunability in both center frequency and -3dB bandwidth is achieved with a scaling-compatible implementation.

2.1 Overview of Prior Art

Passive switched-capacitor approaches to achieve band-pass filtering characteristic are presented in recent work with potentially low power consumption and more flexibility. Two filter architectures are briefly discussed in this section.

2.1.1 N-Path Band-Pass Filter

Fig. 2.1(a) shows the topology of a single-port N-path band-pass filter, implemented using RC low-pass filters and switches as passive mixers driven by a multi-phase non-overlapping clock scheme [13]. Since a resistor is a memory-less element, it is shared

by all paths. The mixing process results in a band-pass filtering characteristic around the switching frequency. The center frequency (f_C) is determined by the switching frequency, insensitive to filter component values. To intuitively understand the filter behavior, the input signal experiences down-conversion and low-pass filtering, and the same switches up-convert the filtered capacitor voltages to the output node.

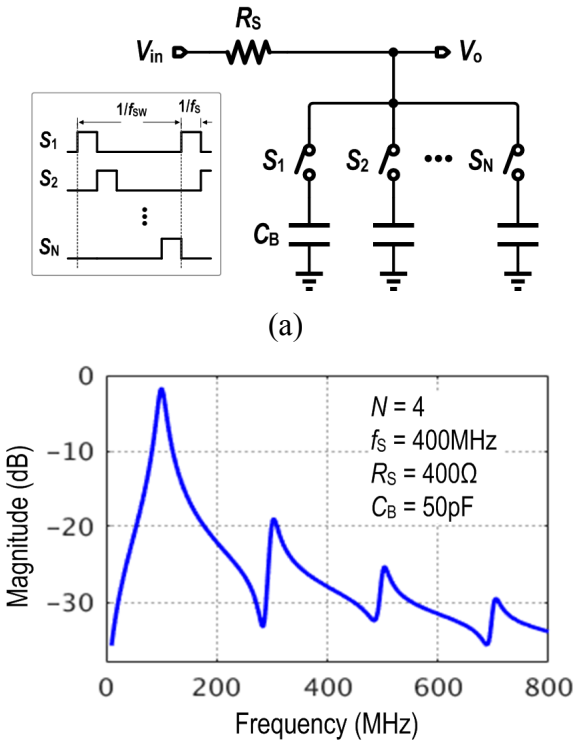


Figure 2.1: N-path band-pass filter: (a) topology, and (b) simulated frequency response of a differential 4-path filter at f_S = 400MHz.

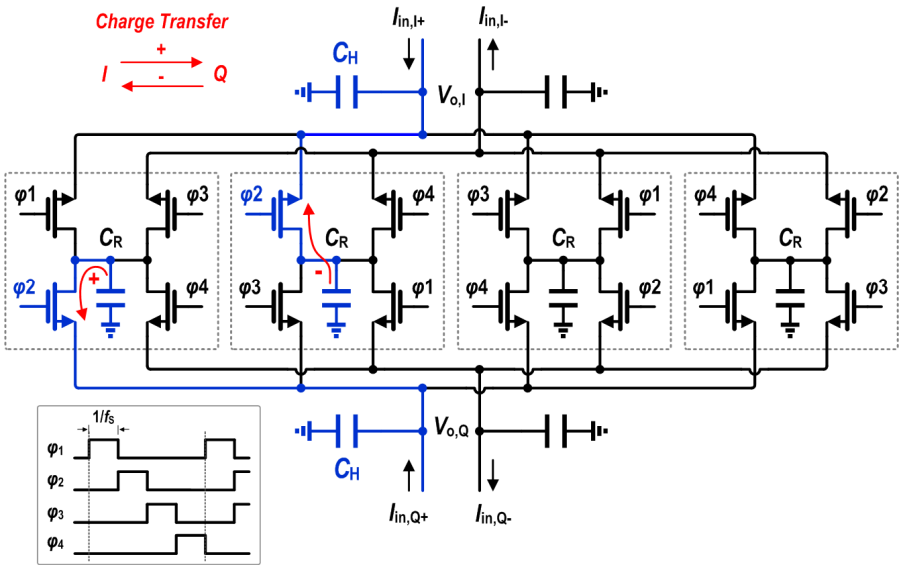
The N-path filter offers high-Q band-pass filtering with precise control of the center frequency through clock adjustment. However, this type of filter has a repetitive selectivity around harmonics of the switching frequency. It is noted that the differential structure could cancel the even harmonic responses. The simulated frequency response of a differential 4-path filter is plotted in Fig. 2.1(b). On the other hand, the N-path filter also shows folding-back from input frequencies around $(k{\cdot}N{+}1)f_C$ (where k = 0, ±1, …) to the desired band around f_C. For instance, for a 4-path architecture the first folding back will occur from $-3f_C$ to f_C (with frequency shift $4f_C$). In general, increasing

the number of paths will increase the distance between f_C and the first folded component around $(N\text{-}1)f_C$. Additionally, a low-pass pre-filter will be needed before the N-path filter to sufficiently suppress harmonic folding-back. Therefore, harmonic selectivity and harmonic folding-back issues limit the practical applicability of N-path filters for IF band-pass filtering.

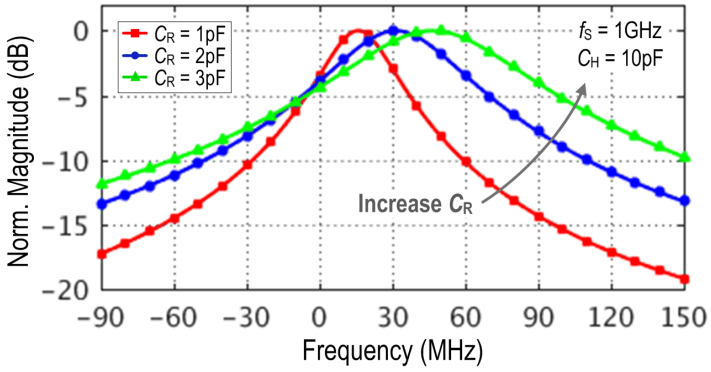
Despite of very high-Q filtering, N-path filters provide poor maximum achievable stop-band rejection due to non-zero switch on-resistance. In order to increase the maximum filter rejection, the switch resistance should be very small with respect to the source resistance R_S.

2.1.2 DT Charge-Sharing Complex BPF

There is an increased demand for highly integrated BPFs that would be free from response replicas around harmonics of the center frequency and still compatible with CMOS scaling. As illustrated in Fig. 2.2(a), a discrete-time complex BPF architecture using passive charge-sharing operation with 4-phase non-overlapping clock signals [14] avoids the undesirable harmonic selectivity and harmonic folding-back issues of N-path filters. The input signal in this topology is differential current that is obtained from a preceding transconductor.



(a)



(b)

Figure 2.2: Discrete-time charge-sharing complex BPF: (a) differential topology, and (b) simulated magnitude response.

During each of the phases φ1−4, the input current is integrated on the capacitor C_H. Meanwhile, each capacitor C_R containing a charge proportional to the previous charge packet on C_H (i.e. $C_R/C_H \cdot q_{H,I(Q)}[n-1]$) is passively charge-shared with C_H containing the present input charge packet and the "history" charge. Therefore, in each phase, a small portion of the charge stored on C_H is transferred by C_R between the in-phase (I) and quadrature (Q) channels. By defining the complex input charge as $q_{in} = q_{in,I}+jq_{in,Q}$ and the complex output voltage as $V_o = V_{o,I}+jV_{o,Q}$, the z-domain complex transfer function of the filter is given by [14]

$$\frac{V_{o,I}+jV_{o,Q}}{q_{in,I}+jq_{in,Q}} = \frac{k}{1-(\alpha+j(1-\alpha))\cdot z^{-1}} \tag{2.1}$$

where $q_{in,I(Q)}$ is the input charge packet in each channel, $k = 1/(C_H+C_R)$, and $\alpha = C_H/(C_H+C_R)$. It has a complex pole $z_p = \alpha+j(1-\alpha)$ defined by α. According to (2.1), the charge-sharing operation forms a first-order complex band-pass filter which has a center frequency (f_C) at

$$f_C = \frac{f_S}{2\pi}\arctan\left(\frac{C_R}{C_H}\right) \tag{2.2}$$

As illustrated in (2.2), f_C is determined by the capacitance ratio for a given sampling rate (f_S). However, the center frequency and -3dB bandwidth (f_{BW}) are correlated, and

there is always a relationship of $f_{BW} \approx 2f_C$ for $\alpha \approx 1$ (i.e. $C_R << C_H$). In other words, f_C and f_{BW} cannot be adjusted independently. Fig. 2.2(b) depicts the simulated magnitude response (normalized to maximum magnitude) with various C_R values. There are no response peaks around harmonics of the center frequency.

Another concern is that this IQ charge-sharing filter achieves a complex band-pass filtering characteristic with two quadrature input signals for the real and imaginary channels. Nonetheless, for many applications where only one input signal is available, a real band-pass filtering function is required. Moreover, it is not easy to generate the perfect I and Q signals from a single wideband input signal.

2.2 Proposed BPF Architecture

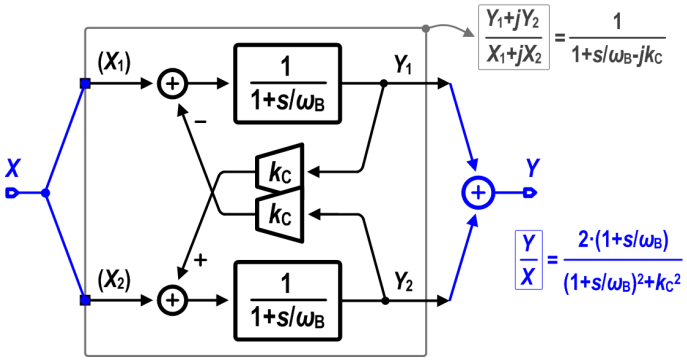
As discussed in Section 2.1.2, the IQ complex band-pass filter using passive charge-sharing operation is fully compatible with process scaling due to its passive nature. Furthermore, the constructed DT filter is more robust to mismatches than the active-RC and g_m-C type of filters because of excellent capacitor matching in advanced CMOS process. Despite of those advantages, two main problems, i.e. correlation in center frequency and bandwidth and not achieving real band-pass filtering with a single input, need to be further addressed.

In this work, a new switched-g_m-C biquad BPF topology utilizing an interleaved semi-passive charge-sharing technique is proposed with a highly passive/digital implementation. The center frequency and bandwidth can be digitally programmed by individually adjusting two different capacitors.

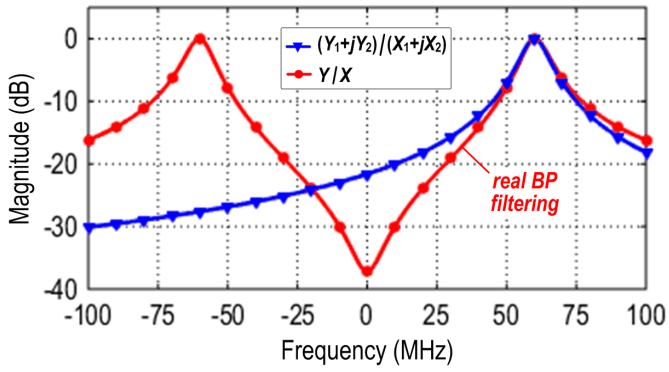
2.2.1 Derivation of Real Band-Pass Filtering

With cross-coupling between two identical paths, it frequency-shifts a 1st-order low-pass filter prototype to a complex band-pass filter. The strength of the cross-coupling paths determines the frequency of the shift. Therefore, it avoids the correlation between the center frequency and the -3dB bandwidth if introducing a degree of freedom in

implementing the cross-coupling paths. A biquad band-pass filtering characteristic is derived from a first-order complex band-pass filter topology by shorting the inputs and summing the outputs in the two paths [15], as shown in Fig. 2.3(a). The entire structure achieves a 2nd-order *real* band-pass transfer function with a single input. This solution to achieve real band-pass filtering is also applicable to a discrete-time realization. This prompts the feasibility of implementing a band-pass filter using passive charge-sharing operation. Fig. 2.3(b) depicts simulated magnitude response curves of the two transfer functions (e.g. f_C = 60MHz, f_{BW} = 10MHz). As illustrated, the two curves are quite close around the response peak. It can be proven that the resulting biquad BPF has about the same center frequency and -3dB bandwidth. Therefore, the filter parameters of the real BPF can be derived from the (mathematical) complex transfer function.



(a)



(b)

Figure 2.3: Proposed biquad real band-pass filtering derived from a 1st-order complex BPF topology: (a) block diagram, and (b) comparison of magnitude response.

2.2.2 Proposed Switched-g_m-C BPF

Fig. 2.4 shows the architecture of the proposed switched-g_m-C biquad BPF [15], in which a three-phase non-overlapping clock scheme is used. Main building blocks are switches, capacitors, g_m-stages, and digital circuitry for clock signals generation.

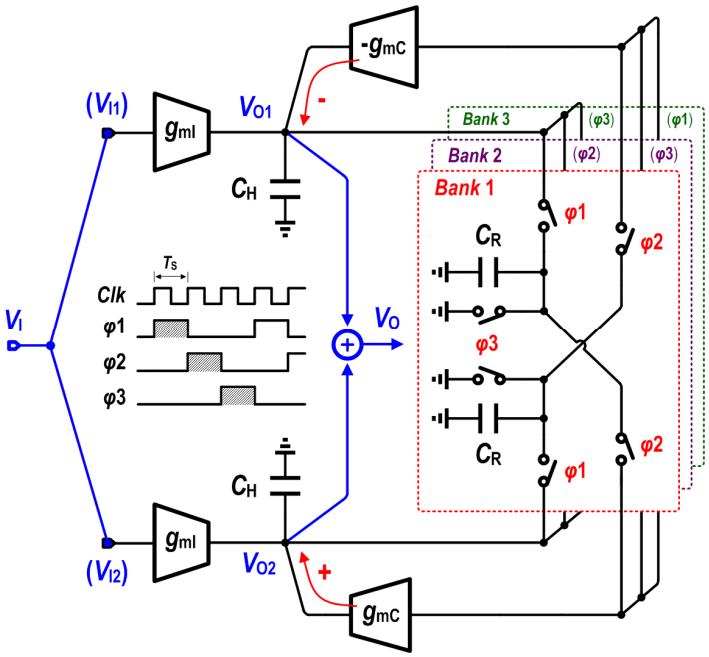


Figure 2.4: Architecture of the proposed switched-g_m-C biquad BPF (single-ended illustration for simplicity).

Two g_m-stages (g_{mI}) convert input voltage into current in each path. The capacitor C_H then integrates the current during each phase and stores the input charge packet. The input charge q_{in} from (n-1)T_S to nT_S (where T_S is one clock period) is defined as

$$q_{in}[n] = \int_{(n-1)T_S}^{nT_S} g_{mI} V_{in}(t)dt \tag{2.3}$$

This windowed current integration over a clock period creates a continuous-time *sinc* low-pass transfer function, given by

$$H_{CI}(s) = g_{mI} T_S \cdot \frac{1-e^{-sT_S}}{sT_S} \tag{2.4}$$

which has notches at integer multiples of sample frequency [16]. It enables an anti-aliasing filtering property for the biquad BPF.

Three identical banks of C_R and switches controlled by delayed clock signals are connected to C_H between the two paths. The filter configuration in one phase, for instance φ2, is shown in Fig. 2.5. In each path, the cross-coupling g_m-stage (g_{mC}) translates the held voltage (i.e. $q_{H1(2)}[n-1]/C_H$) on each capacitor C_R in *Bank* 1 into current/charge with opposite signs. It is noted that the "-1" operation is simply realized by cross-coupling the differential outputs of the g_{mC}-stage. The capacitor C_H that contains the input charge packet, the history charge from the previous phase and the injected charge from the cross-coupling g_m-stage is charge-shared with an empty capacitor C_R in *Bank* 2. This defines a semi-passive charge-sharing operation, since the charge transfer between the two paths is performed through both C_R and g_{mC}-stages. The capacitors C_R in *Bank* 3 are reset for the successive phase. From one phase to the next, these three operations are shifted sequentially in each bank. As a result of this interleaved semi-passive charge-sharing technique, the overall sampling throughput is at the full clock rate.

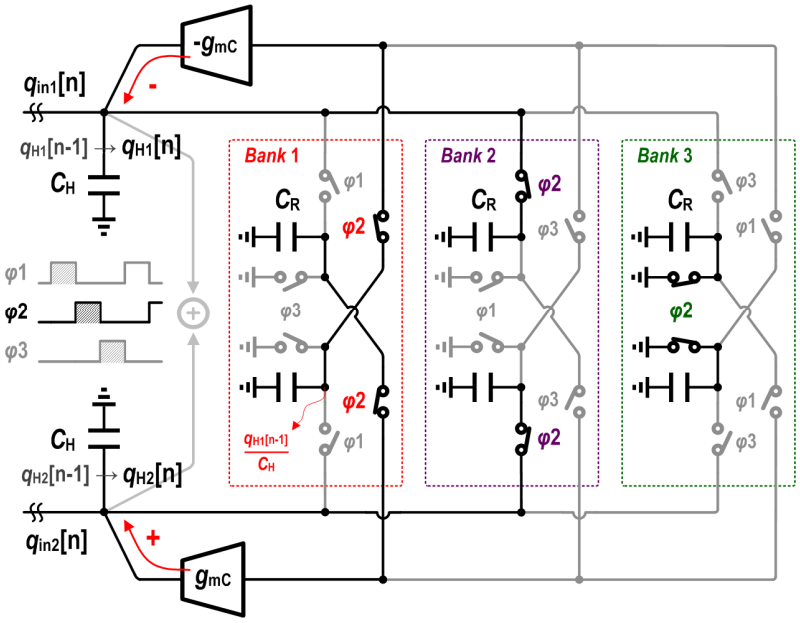


Figure 2.5: Filter configuration in φ2.

After the semi-passive charge sharing to acquire voltage equilibrium between C_H and C_R in each phase, the charge on C_H in each path is

$$\begin{cases} q_{H1}[n] = \dfrac{C_H}{C_H + C_R}\left(q_{in1}[n] + q_{H1}[n-1] - g_{mC}\dfrac{q_{H2}[n-1]}{C_H}T_S\right) \\ q_{H2}[n] = \dfrac{C_H}{C_H + C_R}\left(q_{in2}[n] + q_{H2}[n-1] + g_{mC}\dfrac{q_{H1}[n-1]}{C_H}T_S\right) \end{cases} \tag{2.5}$$

As discussed in Section 2.2.1, the center frequency and bandwidth of the proposed BPF topology can be approximately formulated from the charge-domain complex transfer function, given by

$$H_q(z) = \frac{q_{H1} + jq_{H2}}{q_{in1} + jq_{in2}} = \frac{\alpha}{1 - \alpha(1 + jk_C)\cdot z^{-1}} \tag{2.6}$$

where $\alpha = C_H/(C_H+C_R)$, and $k_C = (g_{mC}/C_H)T_S$. The filter transfer function has a complex pole $z_p = \alpha\cdot(1+jk_C)$. To maintain the filter stable, z_p needs to be located inside the unit circle. Therefore, a minimal capacitance ratio of C_R/C_H is determined for a desired center frequency.

Fig. 2.6 depicts the waveforms at different nodes from a transient simulation with a sinusoidal input signal at the center frequency (e.g. 50MHz). As shown, the voltage signals on each C_H (i.e. V_{O1}, V_{O2}) are not staircase because of the continuous-time input windowed integration.

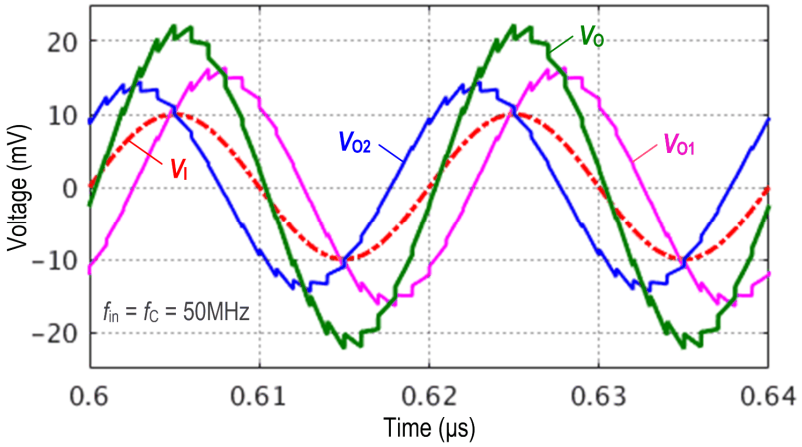


Figure 2.6: Waveforms at different nodes simulated with a sinusoidal input signal.

According to (2.6), the center frequency is derived as

$$f_C = \frac{f_S}{2\pi}\tan^{-1}(k_C) = \frac{f_S}{2\pi}\tan^{-1}(\frac{g_{mC}}{C_H}T_S) \tag{2.7}$$

As illustrated, f_C is only set by the g_{mC}/C_H ratio for a given sampling frequency. It is feasible to adjust the center frequency with a programmable C_H while g_{mC} is fixed to make the total power consumption constant.

The -3dB bandwidth of (2.6) is

$$f_{BW} = \frac{1-\alpha_C}{\sqrt{\alpha_C}}\cdot\frac{f_S}{\pi} \tag{2.8}$$

where $\alpha_C = \alpha\cdot\sqrt{1+k_C^2}$. Even though α_C is a function of both C_H and C_R, α_C has little dependency on C_H when $k_C << 1$ (e.g. $f_C < f_S/20$), thus f_{BW} remains nearly unchanged when adjusting C_H. The bandwidth monotonically reduces with a smaller C_R. On the basis of the analysis above, the proposed biquad BPF features independent tunability in center frequency and bandwidth. The principle of center frequency and bandwidth tuning in this filter topology is as follows: C_H is selected to obtain the desired f_C, then f_{BW} is adjusted by configuring C_R.

The signal flow diagram of the proposed filter is illustrated in Fig. 2.7. The entire filter transfer function has no replicas and image folding-back in the sampling frequency domain of $-f_S/2$ to $+f_S/2$. The overall voltage gain at the center frequency is the product of $H_{CI}(f_C)$, $H_q(f_C)$ and $1/C_H$. Based on (2.4), $|H_{CI}(f)| \approx g_{mI}T_S$ for $f << f_S$. Thus the voltage gain at f_C is approximately derived as

$$G_V(f_C) = \frac{g_{mI}T_S}{C_H}\cdot\frac{\alpha}{1-\alpha_C} \tag{2.9}$$

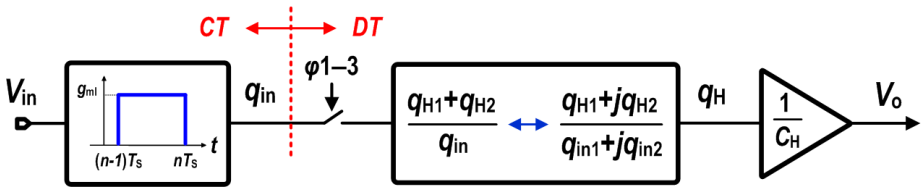
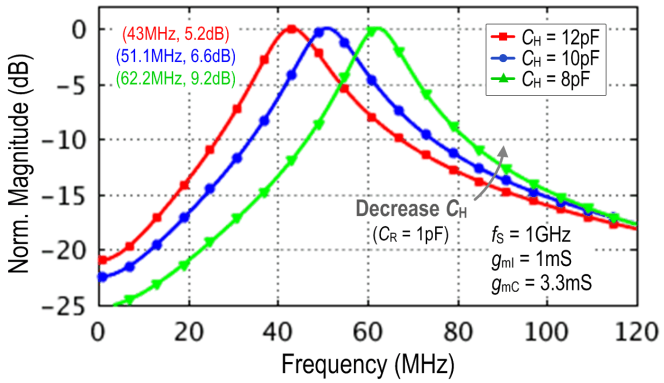


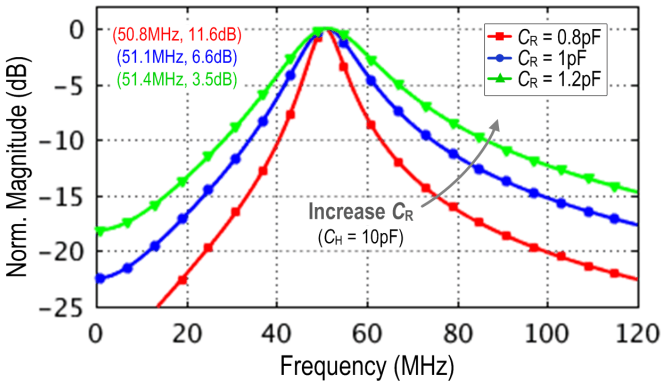
Figure 2.7: Signal flow diagram.

To demonstrate the feasibility of the proposed switched-g_m-C BPF, a behavioral-

model implementation using ideal components is simulated with a 1GS/s sampling rate. Fig. 2.8 shows the (normalized) magnitude response while individually adjusting the capacitor C_H and C_R. As shown in Fig. 2.8(a), the center frequency increases as C_H is decreased (e.g. C_R = 1pF), while the -3dB bandwidth is about constant at 13.5MHz. In addition, the peak voltage gain is slightly varied, as in agreement with (2.9). Fig. 2.8(b) illustrates the wide tunability of the filter bandwidth by only adjusting C_R (e.g. C_H = 10pF). The filter response shape becomes sharper when C_R is decreased, whereas the center frequency is nearly kept constant at 51MHz.



(a)



(b)

Figure 2.8: Simulated filter response while individually adjusting (a) C_H, and (b) C_R.

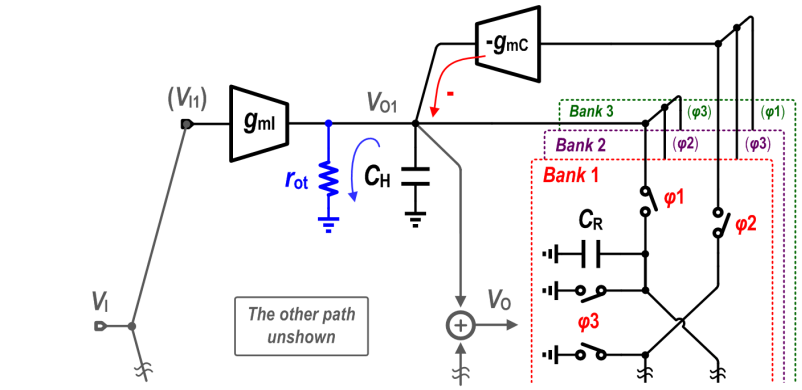
2.3 Design Considerations on Practical Non-Idealities

Practical non-idealities of building blocks affect the filter transfer function. In this section, finite output resistance of g_m-stages and non-zero switch on-resistance are

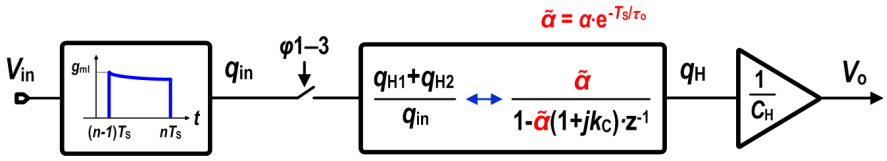
mainly analyzed and simulated to derive the design specifications.

2.3.1 Finite Output Resistance of g_m-Stages

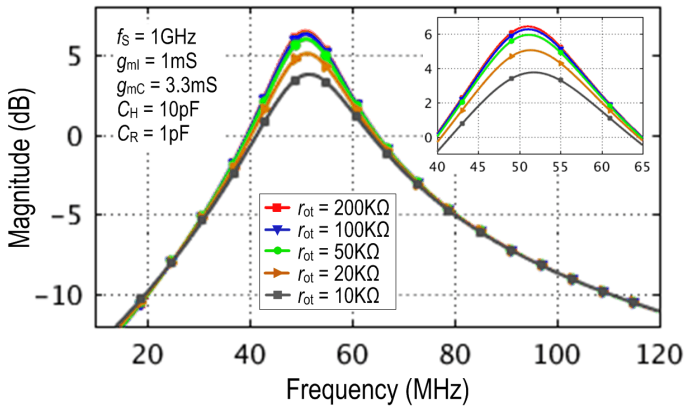
As shown in Fig. 2.4, the outputs of the input (i.e. g_{mI}) and cross-coupling (i.e. g_{mC}) transconductors in each path are connected. Therefore, a total output resistance of r_{ot} is considered here, as depicted in Fig. 2.9(a).



(a)



(b)



(c)

Figure 2.9: Impact of finite output resistance of g_m-stages: (a) equivalent circuit, (b) signal flow diagram, and (c) simulated magnitude response vs. r_{ot}.

The finite r_{ot} takes away some of the transconductor output current into ground in both the input windowed integration and charge-sharing operation. The input charge q_{in} over one T_S now becomes

$$q_{in}[n] = \int_{(n-1)T_S}^{nT_S} g_{mI} V_{in}(t) e^{-t/\tau_o} dt \tag{2.10}$$

where $\tau_o = r_{ot} \cdot (C_H + C_R)$ is the time constant of the circuit. This no longer results in an ideal *sinc* function, given by

$$H_{CI}(s) = g_{mI} T_S \cdot \frac{1 - e^{-(s+\tau_o^{-1})T_S}}{(s+\tau_o^{-1})T_S} \tag{2.11}$$

Comparing this new transfer function with the ideal one in (2.4), it illustrates that the zeros are shifted off the $j\omega$-axis by $1/\tau_o$.

On the other hand, during each phase charge sharing occurs between C_H and C_R to obtain voltage equilibrium, while the r_{ot} affects the settled voltage (or charge) on both capacitors. Therefore, (2.5) is modified by replacing $C_H/(C_H+C_R)$ with $\tilde{\alpha} = \alpha \cdot e^{-T_S/\tau_o}$, and then (2.6) becomes

$$H_q(z) = \frac{\tilde{\alpha}}{1 - \tilde{\alpha}(1 + jk_C) \cdot z^{-1}} \tag{2.12}$$

It turns out that the center frequency f_C is unchanged, as given by (2.7). But the filter pole is scaled down by e^{-T_S/τ_o}, increasing its -3dB bandwidth.

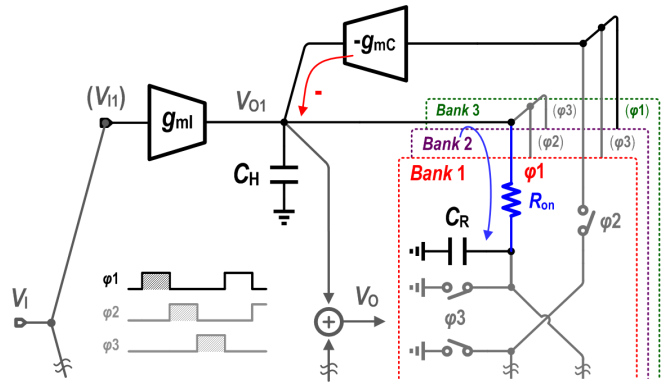
The modified signal flow diagram is shown in Fig. 2.9(b). The voltage gain at the center frequency is now modified to

$$G_V(f_C) = \frac{g_{mI} T_S}{C_H} \cdot \frac{\tilde{\alpha}}{1 - \tilde{\alpha} \cdot \sqrt{1 + k_C^2}} \tag{2.13}$$

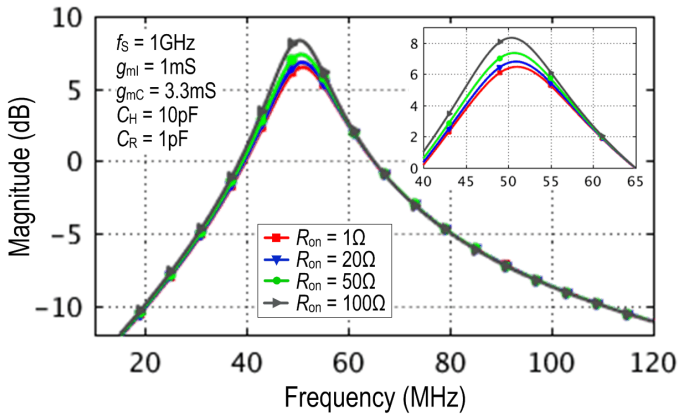
The voltage gain at f_C is decreased with a smaller r_{ot}. Intuitively, the switched capacitor C_R is equivalent a resistance of T_S/C_R, thus the voltage gain at f_C can be approximately derived as $g_{mI} \cdot (r_{ot} \,||\, (T_S/C_R))$. Fig. 2.9(c) plots the simulated magnitude response versus different r_{ot}, which is in agreement with the above analysis. In this work, $r_{ot} \geq 20\text{k}\Omega$ is desired when designing the g_m-stages for the proposed BPF.

2.3.2 Non-Zero Switch On-Resistance

During the charge-sharing operation in each phase (e.g. φ1), the non-zero on-resistance of the switch connecting C_H with C_R in each path, as shown in Fig. 2.10(a), makes the instant voltage on C_R (denoted as $V_{CR}(t)$) not perfectly track the voltage on C_H (denoted as $V_{CH}(t)$). The R_{on} and C_R form a low-pass filter, and the time constant in this circuit is equal to $\tau_{on} = R_{on} \cdot (C_H \,||\, C_R)$.



(a)



(b)

Figure 2.10: Impact of non-zero on-resistance of the switch connecting C_H with C_R: (a) equivalent circuit, and (b) simulated magnitude response vs. R_{on}.

Assuming there is enough time for C_R to be completely discharged in the reset phase, $V_{CR}(t) = V_{CH}(t) \cdot (1 - e^{-(t-(n-1)T_S)/\tau_{on}})$ during one T_S interval of [(n-1)T_S, nT_S]. Therefore, the sampled voltage at nT_S on the capacitors C_R and C_H in each path have a relationship of

$V_{CR}[n]=V_{CH}[n]\cdot(1-e^{-T_S/\tau_{on}})$. Applying Kirchhoff's current law (KCL) in terms of average current in each path,

$$\begin{cases} \dfrac{q_{in1}[n]}{T_S} - g_{mC} V_{CR2}[n-1] = C_H \dfrac{V_{CH1}[n]-V_{CH1}[n-1]}{T_S} + C_R \dfrac{V_{CR1}[n]}{T_S} \\ \dfrac{q_{in2}[n]}{T_S} + g_{mC} V_{CR1}[n-1] = C_H \dfrac{V_{CH2}[n]-V_{CH2}[n-1]}{T_S} + C_R \dfrac{V_{CR2}[n]}{T_S} \end{cases} \tag{2.14}$$

The modified complex transfer function of the filter becomes

$$\frac{V_{CH1}+jV_{CH2}}{q_{in1}+jq_{in2}} = \frac{1/C_H}{1+\dfrac{C_R}{C_H}(1-e^{-T_S/\tau_{on}})-(1+jk_C(1-e^{-T_S/\tau_{on}}))\cdot z^{-1}} \tag{2.15}$$

If $T_S >> \tau_{on}$, (2.15) is equivalent to (2.6) since $C_R/C_H = (1-\alpha)/\alpha$.

The center frequency and -3dB bandwidth can be derived from (2.15). For instance, the center frequency is expressed as

$$f_C = \frac{f_S}{2\pi}\tan^{-1}(k_C(1-e^{-T_S/\tau_{on}})) \tag{2.16}$$

The f_C is slightly decreased with a larger τ_{on} (i.e. increasing R_{on}), which is in good agreement with the simulated magnitude response, as plotted in Fig. 2.10(b). But the filter bandwidth is decreased as R_{on} is larger, which may compensate for the bandwidth increase caused by the finite output resistance of g_m-stages. In this work, $R_{on} \leq 50\Omega$ is desired when sizing this switch transistor.

The on-resistance requirement of the switch connecting C_R to the input of the cross-coupling g_{mC}-stage in the other path is much relaxed, since the time constant here is defined as R_{on} ($C_{in} || C_R$) where C_{in} is the input parasitic capacitance of the g_{mC}-stage. On the other hand, the switch transistor that connects C_R to ground in the reset phase is sized so that the complete discharge to zero is finished within one T_S.

2.4 Filter Prototype

In this work a 4th-order BPF prototype operating at a 1.2GS/s sampling rate is

designed by cascading two proposed biquad filter stages, as shown in Fig. 2.11. The center frequency and bandwidth of each biquad are independently adjusted to construct the overall filter frequency response. The g_{mC} is designed to be 3.3mS and 2.75mS in the first (i.e. BPF1) and second (i.e. BPF2) biquad stage, respectively. MoM capacitors are used for C_H and C_R. In both biquads, C_H is adjustable from 4.8pF to 11.7pF with a step size of 0.3pF, and used differentially to minimize the chip area. Similarly, C_R is digitally selected between 0.7−1.35pF in BPF1 and 0.6−1.05pF in BPF2, respectively, with a 3-bit binary-weighted realization.

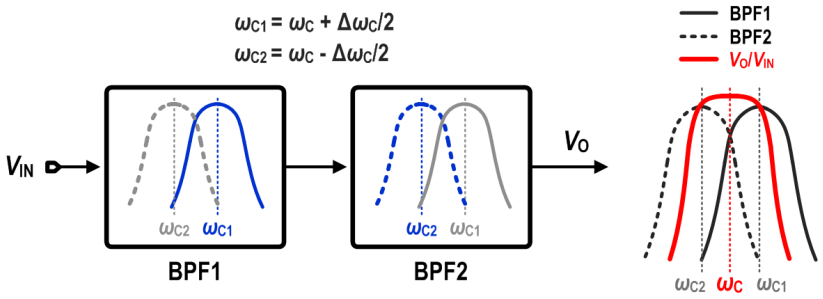


Figure 2.11: Diagram of the 4th-order BPF prototype.

Fig. 2.12 illustrates the complete diagram of the filter architecture, including the BPF core, current bias circuit, a switch multiplexer (MUX), an on-chip buffer amplifier and a series-parallel interface (SPI) module for measurements. The multiplexer is used to select the input of the test buffer (TB), thus the effect of the TB can be de-embedded to characterize the performance of the filter core. Furthermore, an open-drain amplifier topology is employed to implement the buffer, in which the differential outputs connect an off-chip transformer to drive the 50Ω load.

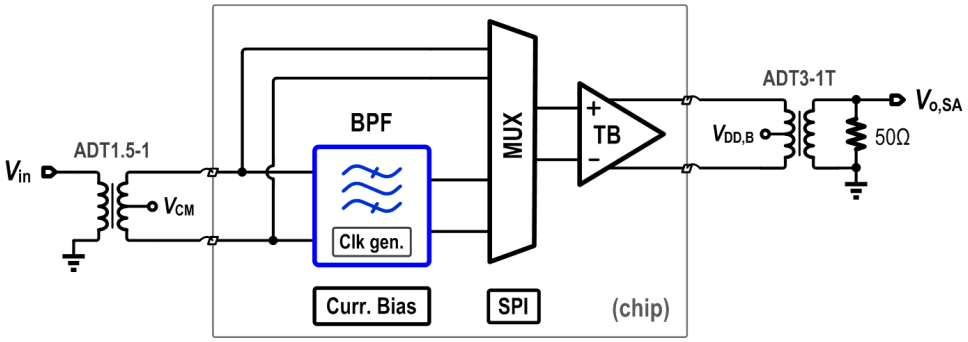


Figure 2.12: Filter architecture including an on-chip test buffer and SPI.

2.5 Circuit Implementation

The circuit implementation details of main building blocks in the proposed BPF architecture will be described in this section.

2.5.1 Linearity-Enhanced g_m-Stage

A new resistive source-degenerated transconductor with embedded local feedback is proposed to improve the linearity, as shown in Fig. 2.13. To reduce the input parasitic capacitance, NMOS differential pair is utilized. Transistors M_1−M_3 form a negative feedback loop that largely reduces the equivalent resistance looking into the node at the source of M_1 by the loop gain. As a result, the current flowing in the source degenerated resistor approximates to v_{id}/R_S (where v_{id} is the input differential voltage). This current is also equal to the small-signal current incremental in the transistor M_2, since the current of M_1 is (theoretically) unchanged. It assumes that the current incremental in M_2 should be less than its bias current. Moreover, the capacitor C_M is added as Miller compensation to improve the loop phase margin.

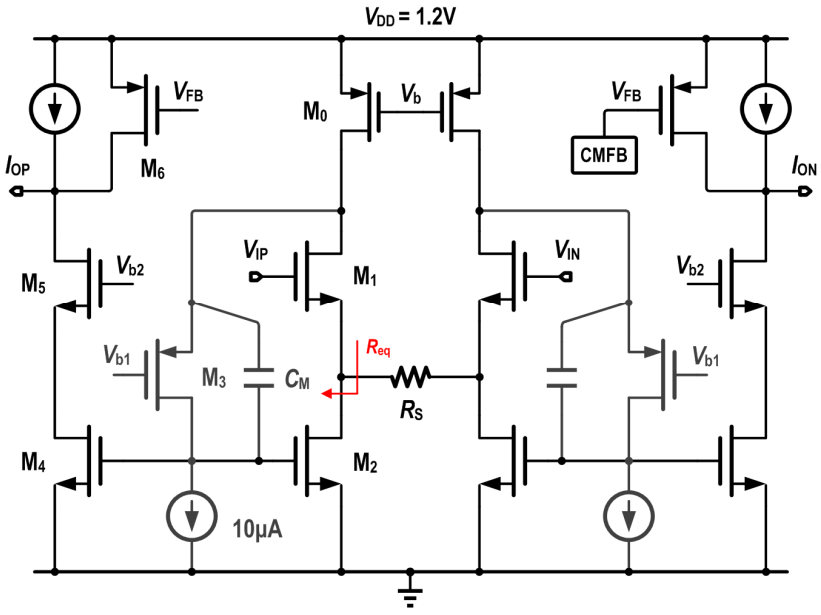


Figure 2.13: Schematic of the proposed source-degenerated transconductor with an embedded local feedback loop.

On the other hand, through the use of the current mirror M_2 and M_4, the linearized differential current (i.e. v_{id}/R_S) is copied to the output stage. In this way, the proposed transconductor achieves good linearity while drawing low current in each branch. A cascode structure of M_4 and M_5 is employed to increase the output resistance. A common-mode feedback (CMFB) circuit sets the output CM voltage by adjusting the voltage at node 'V_{FB}'. Since the outputs of g_{mI} and g_{mC} stages in each path are connected (Fig. 2.4), they share the same CMFB that connects to the node 'V_{FB}' in this work.

Fig. 2.14 shows the simulated transconductance versus input differential voltage in the proposed transconductor topology and the conventional source-degenerated topology (without a feedback loop). The proposed topology has much larger effective transconductance with the same source-degenerated resistor R_S (e.g. 640Ω in BPF1) and current consumption. Thus total power consumption can be minimized to achieve the desired g_m value in this proposed topology. As also illustrated, there is more flatness in the transconductance within a small input differential voltage (e.g. ±0.1V).

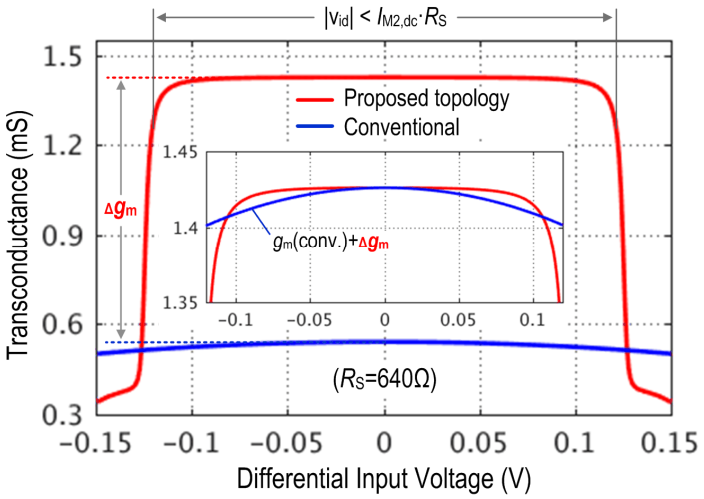


Figure 2.14: Simulated g_m vs. input differential voltage.

2.5.2 g_m-based Voltage Adder

The voltage signals (V_{O1}, V_{O2}) on C_H in the two paths (Fig. 4) are summed to obtain the overall biquad output V_O. This summation is realized using two transconductors with differential outputs connected to the same load resistor R_L, as shown in Fig. 2.15.

Each transconductor cell here converts V_{O1} (or V_{O2}) into current. The output currents from the two g_m cells flow through the load resistor, and therefore the voltage across the resistor is V_O.

The g_m cell in Fig. 2.15 employs a similar source-degenerated transconductor topology (Fig. 2.13) for g_{mI} and g_{mC} stages, except that the NMOS transistor M_3 is employed to realize a level shifter. In this way, the dc voltage at the drain of M_1 is set to $V_{GS2}+V_{GS3}$. The loop gain is decreased, and a good phase margin (e.g. >65°) can be obtained even without the Miller compensation. In addition, the resistor R_S is chosen relatively larger to meet the desired linearity due to a reduction of the loop gain. On the other hand, the effective transconductance is decreased. As a result, the input-referred noise performance gets worse. The design of this g_m cell used to implement the voltage adder should be optimized in view of the linearity, input-referred noise and total current consumption.

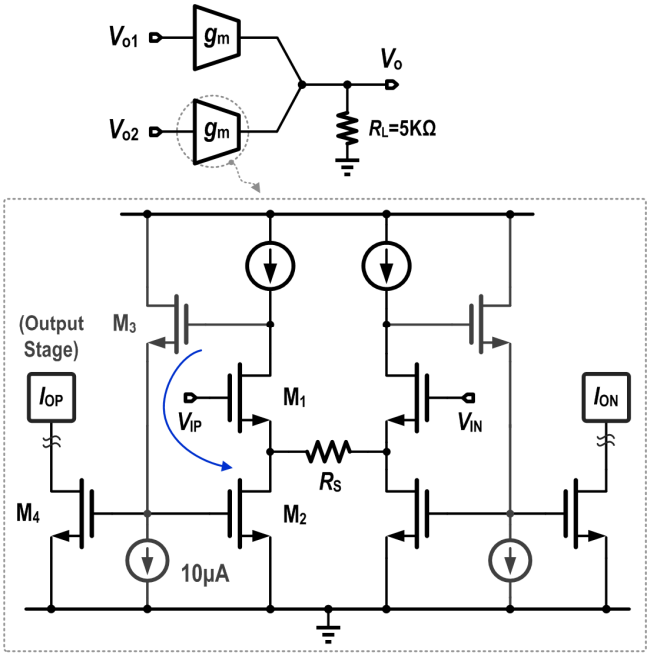


Figure 2.15: Diagram of the voltage adder using two transconductors.

2.5.3 3-Phase Non-Overlapping Clock Generator

Fig. 2.16 shows the block diagram of the 3-phase non-overlapping clock generator.

A D-flip-flop (DFF) based divider divides the external input clock (i.e. *Clk*) by three, in which a NOR gate is used to generate a clock signal with ⅓ duty cycle at node 'A'. Next, a shift register implemented with three DFFs produces 3-phase clock signals *Ck*1−3 whose pulse width is one clock period T_S. However, there might be some overlap period between two adjacent clock signals of *Ck*1−3. Therefore, a non-overlapping monitor (Fig. 2.16), simply designed using a NOR gate with explicitly inserted delays, is proposed to guarantee the non-overlap between two adjacent clock signals of φ1−3. The inverter-based buffers that drive the switches in Fig. 2.4 are sized to achieve steep rise and fall transitions. The current consumption of the clock generator including driving buffers is proportional to the sampling clock rate f_{Clk}. In this work, the entire clock generator consumes 1.3mW power from a 1.2V supply voltage while operating at f_{Clk} = 1.2GHz.

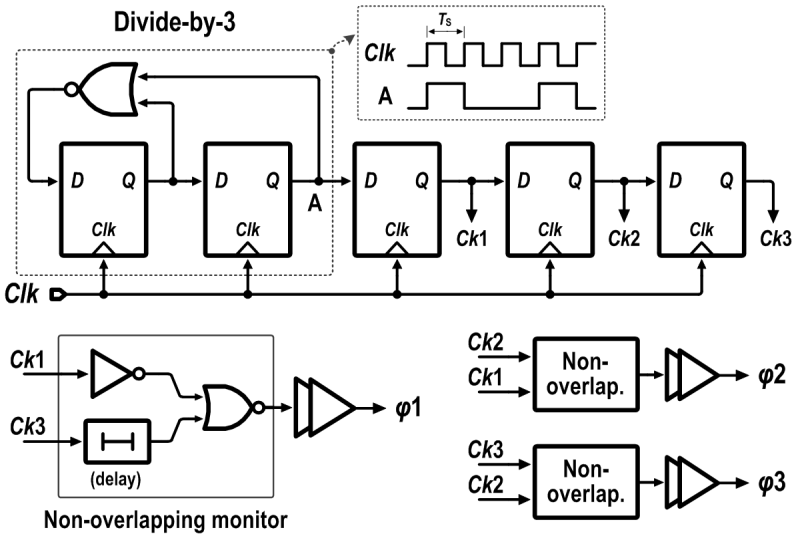


Figure 2.16: Diagram of the 3-phase non-overlapping clock generator.

2.6 Measurement Results

The filter prototype is fabricated in a 65nm LPE CMOS process, and Fig. 2.17 shows the die micrograph. As shown, the core area is dominated by capacitors. The filter core occupies an active area of 0.17mm^2 (excluding the test buffer and pads). The chip is mounted in a 24-pin QFN package for measurement.

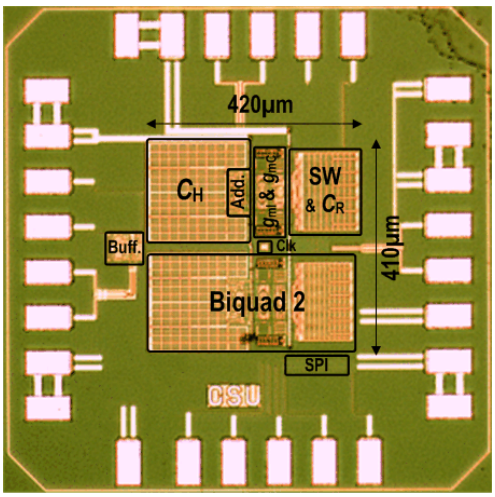
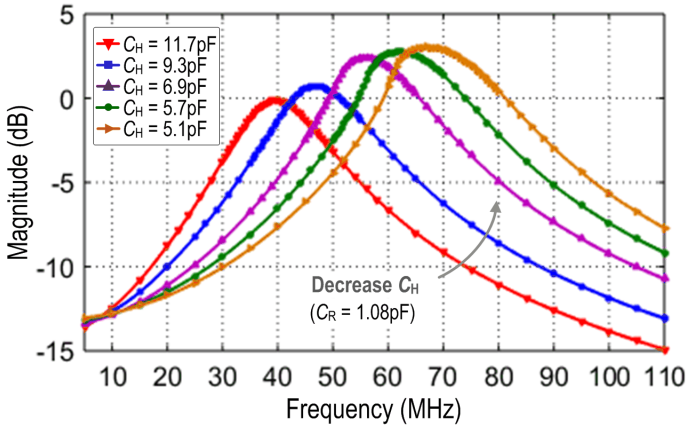
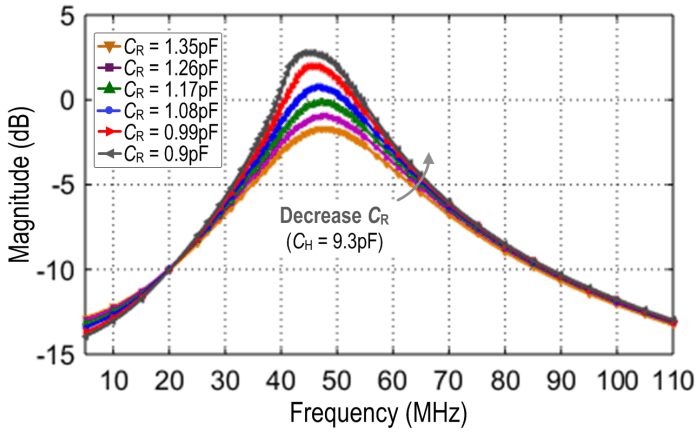


Figure 2.17: Chip die micrograph.

The filter is operating at a 1.2V supply voltage, and consumes 7.5mW total power. Fig. 2.18 depicts the measured magnitude response of the 1st biquad BPF stage (i.e. BPF1) with different C_H and C_R values. As shown in Fig. 2.18(a), the center frequency increases as C_H is decreased (e.g. C_R = 1.08pF), and is tunable from 38MHz to 68MHz. The -3dB bandwidth is about constant (e.g. 18.5−20MHz). Meanwhile, the voltage gain at the center frequency is varied. Fig. 2.18(b) illustrates the wide tunability of -3dB bandwidth by only adjusting C_R (e.g. C_H = 9.3pF). The filter shape becomes sharper when C_R is decreased. The -3dB bandwidth is programmable from 16MHz to 27.5MHz, whereas the center frequency is nearly kept constant (e.g. 45.5−47MHz).



(a)



(b)

Figure 2.18: Measured magnitude response of the 1st biquad BPF (i.e. BPF1) vs. adjustable (a) C_H and (b) C_R.

The magnitude response of the complete 4th-order filter is shown in Fig. 2.19, while C_R in each biquad is set to 1.17pF/0.98pF and the capacitors C_H are adjusted. A tunable center frequency of 35−70MHz is measured with the -3dB bandwidth varying between 12.5−18MHz. The maximum stop-band rejection is 72dB. In addition, no harmonic selectivity issue is observed. On the other hand, the filter bandwidth can be accordingly configured by adjusting the capacitors C_R.

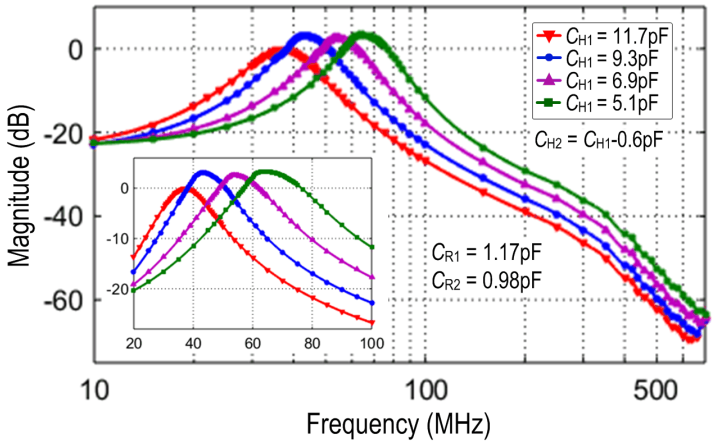


Figure 2.19: Measured magnitude response of the 4th-order BPF.

Configuring the capacitors (e.g. C_H = 9.3pF/8.7pF, C_R = 1.08pF/0.91pF in each biquad) to set the mode with f_C at 48MHz, the input 1dB compression point (CP_{1dB}) is measured at -0.5dBm. The in-band linearity of the entire filter (including the test buffer)

is evaluated by feeding two input tones at 48MHz and 48.2MHz. The measured output spectrum for the two-tone input signals with 0.11V_{pp} amplitude for each tone is shown in Fig. 2.20. Under this condition, the 3rd-order intermodulation (IM3) measures at 47.6dB. Fig. 2.21 shows the IM3 term versus input power. The resulting input intercept point (IIP3) is +12.5dBm.

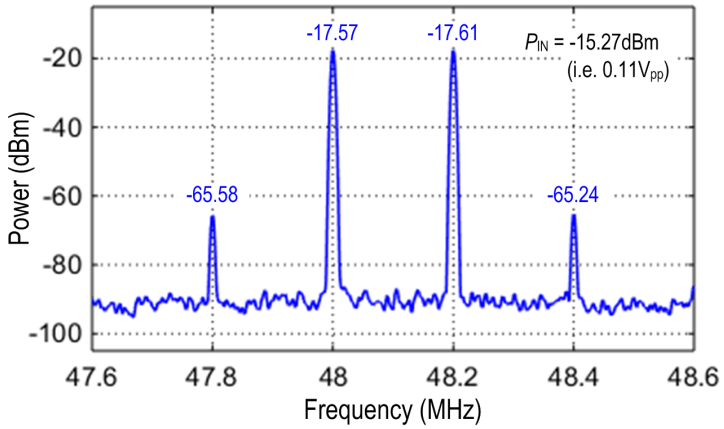


Figure 2.20: Measured output spectrum with feeding two input tones.

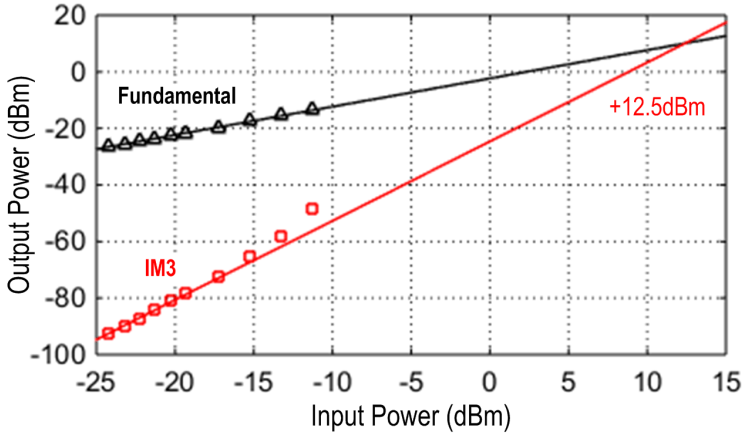


Figure 2.21: In-band IIP3 measurement.

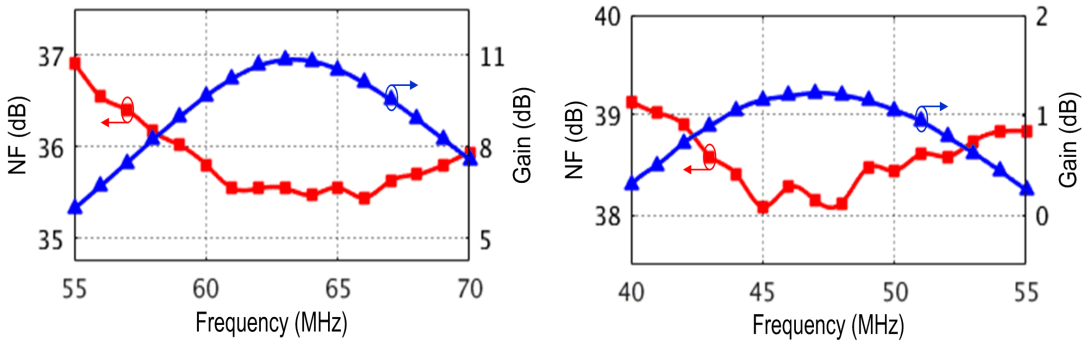
The noise figure (NF) is measured through a two-step experiment using a spectrum analyzer. The input port is terminated with the characteristic impedance (e.g. 50Ω), and then 1) measure the output noise power spectral density (PSD) of the direct path (i.e. configuring the MUX to connect the input port to the test buffer); 2) measure the total output noise PSD of the filter path including the BPF core and the test buffer. Since the noise of the filter core and the test buffer are uncorrelated, the filter noise is calculated

by subtracting the buffer noise PSD in step 1) from the total noise PSD in step 2). The formula to calculate the NF is

$$NF = P_{\text{ND,out}} + 174\text{dBm/Hz} - G_{\text{BPF}} \tag{2.17}$$

where $P_{\text{ND,out}}$ is the filter noise PSD, G_{BPF} is the gain at a specific frequency, and each term is in log (dB) scale.

Fig. 2.22 shows the measured NF in two different modes. The NF (at the center frequency) ranges from 35.5dB to 38dB, while the voltage gain at center frequency varies between 10.8dB and -0.1dB. According to post-simulations, the noise figure is limited by the voltage adders.



(a) (b)

Figure 2.22: Measured noise figure in two different modes.

Table 2.1 summarizes the performance of the filter prototype, and compares with other state-of-the-art BPFs [11−12], [17−18]. The presented BPF using an interleaved semi-passive charge-sharing technique favorably compares to other work with a reduced power consumption. It achieves superior stop-band rejection and attenuation at $3f_C$, and competitive in-band linearity performance.

Table 2.1: Performance summary and comparison

	This work	[12] JSSC′10	[17] ISSCC′12	[18] ISSCC′13	[11] ASSCC′09
Technology	65nm LPE	65nm	65nm LP	65nm LP	65nm
Architecture	SW-g_m-C, charge-sharing	g_m-C	SW g_m-C, N-path	SC+g_m, N-path	active-RC
V_{DD} (V)	1.2	1.2	1.2/2.5	1.2	1
Filter Order	4^{th}	4^{th}	4^{th}	6^{th}	10^{th}
f_C (MHz)	35−70	80	300−1200	100−1200	60
f_{BW} (MHz)	12−28	10	21	8	8
Power (mW)	7.5	13.2	13−21.4	18−57.6	23.5
Gain (dB)	-0.1−10.8	2	3.5	25	0
Stop-band Rej. (dB)	67−72	28	55	59	60
Harmonic Selectivity	Yes	CT	No	No	CT
Rejection @3f_C (dB)	32	27	20	N/A	60
In-band CP_{1dB} (dBm)	-1.8−-0.5	N/A	-4.4	-23	N/A
In-band IIP3 (dBm)	9.7−12.5	-2	9	-12	N/A
NF (dB)	35.5−38	21.5	9.5	2.8	51
Area (mm^2)	0.17	0.25	0.13	0.27	0.5

2.7 Further Discussions

A generalized topology to achieve high-order filtering characteristic is shown in Fig. 2.23, by internally cascading a series of 1^{st}-order complex BPF (CBPF) cells and then shorting the inputs and summing the outputs in the two paths. It is noted that the CBPF cell is implemented using the proposed switch-g_m-C architecture in Fig. 2.4. To achieve N^{th}-order filtering, only one voltage adder is required, in contrast to N adders used in the previous high-order filter diagram in Fig. 2.11. In this way, the power consumption is minimized. Moreover, the noise figure performance can be improved.

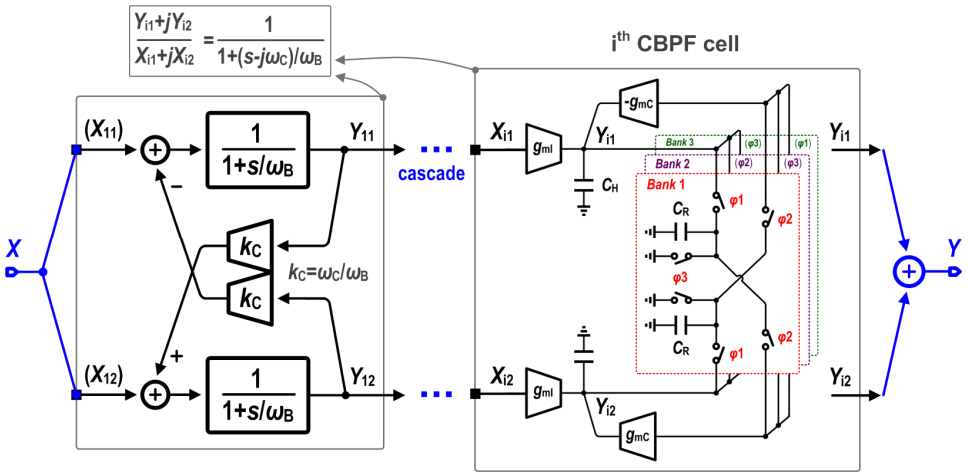


Figure 2.23: New method to achieve high-order filtering characteristic by an internal cascade of the proposed complex BPF cells.

A 4th-order BPF is designed using the internal cascade of two complex BPF cells. Fig. 2.24 depicts the simulated magnitude response curves for different topologies. As illustrated, the constructed BPF in Fig. 2.23 demonstrates a 4th-order real band-pass filtering characteristic. It achieves higher voltage gain at center frequency and more stop-band rejections at higher frequencies compared to the previous 4th-order BPF structure in Fig. 2.11.

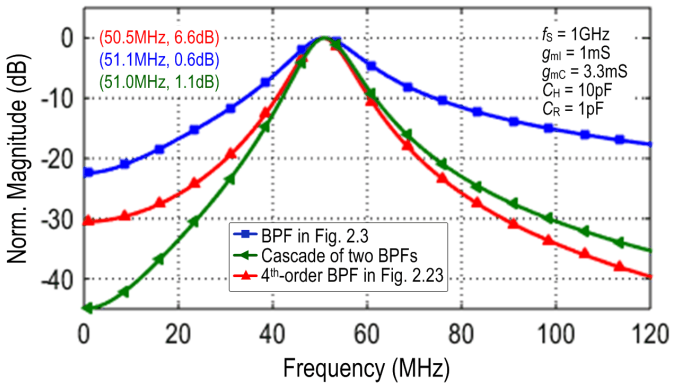


Figure 2.24: Comparison of simulated magnitude response for different topologies.

2.8 Summary

In this chapter, a new charge-domain switched-g_m-C band-pass filter topology that utilizes an interleaved semi-passive charge-sharing technique is proposed and

experimentally verified. The center frequency and bandwidth of the proposed biquad filter stage are independently programmable. A 4^{th}-order BPF prototype is designed using a cascade of two reconfigurable biquad stages with a 1.2GS/s sampling rate. A tunable center frequency of 35−70MHz is achieved with a total power consumption of 7.5mW. The proposed filter topology is highly reconfigurable and compatible with submicron scaling due to a passive/digital implementation.

CHAPTER 3. HIGHLY COMPACT LOW-PASS FILTER WITH SOURCE FOLLOWER COUPLING

Low-pass filters (LPFs) are essential building blocks in analog signal processing systems which require high linearity and decreasing power consumption. Typically, active-RC [19−20] or g_m-C [21−22] topologies are used to implement LPFs. The performance of such filters depends on the OTA used to realize the integrator. As discussed in Section 1.1, reduced supply voltage and lower transistor intrinsic gain in submicron CMOS processes make it difficult to implement a high-gain and wide-bandwidth OTA in a power efficient manner. The main focus in conventional LPF designs is to improve the performance of OTAs used in the filter topology.

This chapter presents a highly linear OTA-free continuous-time LPF topology with source follower coupling that achieves excellent power efficiency. It synthesizes a 3^{rd}-order low-pass transfer function in a single stage using coupled source followers and three capacitors, and can be easily configured to 2^{nd}-order by disconnecting a capacitor. The configurability of the proposed single-stage $3^{rd}/2^{nd}$-order filter makes it a scalable topology to realize any order filter.

3.1 Prior Solutions

Other than active-RC and g_m-C topologies using OTAs, new techniques that are compatible with process scaling have been proposed to overcome the limitations of conventional OTA-based filters. One of the major goals is to further minimize the power consumption. This section describes some circuit techniques and architectures to implement power-efficient low-pass filters.

3.1.1 Using Ring Oscillator based Integrators

The ring oscillator based integrator (ROI) is an alternative to implement the filter

instead of an OTA-based integrator [4], due to the integral relationship of the oscillator output phase to the input signal. Fig. 3.1 shows the diagram of a ROI with current input and current output. The current-controlled oscillator (CCO) converts the input current and generates multiple output phases. The phase detector (PD) compares one phase of the CCO with a reference phase to generate a pulse-width modulated (PWM) signal. The PD output is converted to a PWM current using a charge pump. The transfer function of this integrator is defined as

$$H_{\mathrm{ROI}}(\mathrm{s}) = \frac{I_{\mathrm{out}}}{I_{\mathrm{in}}} = \frac{K_{\mathrm{CCO}} K_{\mathrm{PDCP}}}{s} \tag{3.1}$$

in which K_{CCO} is the oscillator gain, and K_{PDCP} is the gain of the combination of the PD and the charge pump.

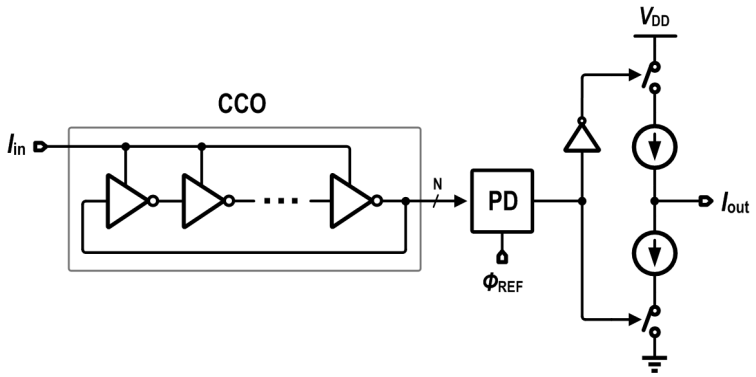


Figure 3.1: Diagram of the ring oscillator based integrator with current input and current output.

The ROI transfer function reveals that the dc gain is infinite as long as the CCO oscillates, and is independent of the transistor intrinsic gain and supply voltage. It is this property of the ROI that offers an alternative way to implement an analog filter in submicron CMOS processes. However, the current-to-frequency transfer curve of a practical CCO is nonlinear, which severely limits the linearity performance of the ROI. When implementing the biquad using two ROIs, each ROI is embedded in a feedback loop that forces the oscillator input to a small swing. In addition, the ROI suffers from spurious tones in the output spectrum caused by pulse-width modulation, and additional phase shift caused by parasitic poles.

This ROI based filter is implemented using highly digital circuits, which makes it compatible with process scaling and capable of operating under low supply voltage. The 4th-order filter using ROIs in [4] achieves comparable performance in terms of linearity and power efficiency.

3.1.2 DT Charge-Sharing IIR Filter

A simple 1st-order discrete-time (DT) IIR low-pass filter [5] is depicted in Fig. 3.2. A g_m-stage converts the input voltage to current. In each phase, the history capacitor C_H integrates this current and stores the input charge packet $q_{in}[n]$. The total charge, containing the input charge and the history charge on C_H from the last phase, is shared between C_H and an empty sampling capacitor C_S to obtain a voltage equilibrium. As a result, this passive charge-sharing operation forms a 1st-order low-pass filter. The bandwidth is determined by the capacitors ratio of C_S/C_H and sampling frequency, making it insensitive to PVT variations.

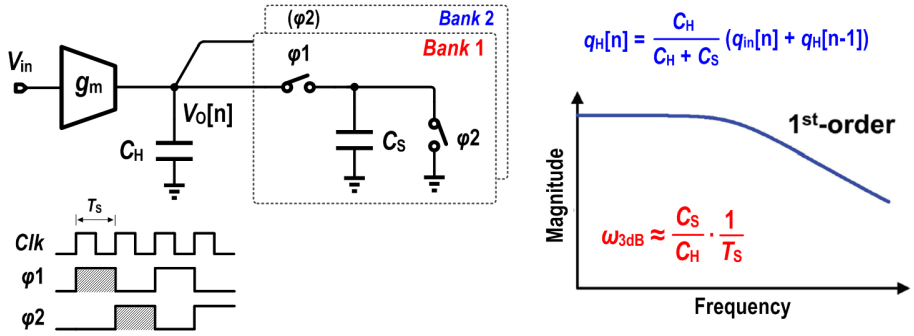


Figure 3.2: The 1st-order DT IIR low-pass filter with charge-sharing operation.

A high-order IIR filter can be realized by using only one sampling capacitor that shares total charge with several history capacitors at different phases [5]. Using this method, a 7th-order DT IIR filter is implemented in [5] with an 8-phase non-overlapping clock scheme. On φ1, the charge stored on C_{H1} is shared with the empty sampling capacitor C_S. Then on φ2, the charge on C_S is shared with C_{H2}. In the same way, C_S charge is shared with other history capacitors C_{H3}–C_{H7} on φ3 to φ7. Finally, on φ8, C_S is discharged to zero and gets ready for the next cycle.

Main building components in this charge-sharing IIR filter are capacitors, T-gate switches, inverter-based g_m-stage and digital circuitry for waveform generation. All of these blocks are friendly to the nanoscale CMOS technology. Also, they are improving from one process node to the next: faster switches, higher capacitor density and lower-power digital circuits. In contrast, conventional OTA-based analog filters [19−22] suffer from lower voltage headroom, lower gain and more process variation in more advanced technologies.

However, this charge-sharing IIR low-pass filter only creates real poles located at the same frequency in the filter transfer function, therefore it cannot achieve a flat pass-band response.

3.1.3 Source-Follower-based Biquad

A source follower driving a capacitor realizes a first-order low-pass filter, in which good linearity may be obtained with the use of local feedback. A source-follower-based biquad filter topology in [23], as shown in Fig. 3.3, allows the synthesis of a pair of complex conjugate poles by using positive feedback in the transistor M_2. The "-1" operation is realized by cross-coupling M_2 in a pseudo-differential structure.

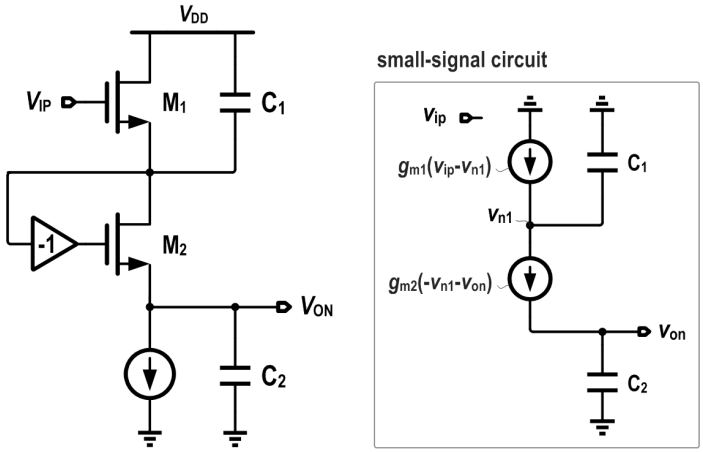


Figure 3.3: Schematic of the source-follower-based biquad filter.

The equivalent small-signal circuit is also shown in Fig. 3.3, assuming that the transistor's output conductance is much smaller than its transconductance. Transistors

M_1−M_2 are designed with the same sizes and draw the same current, therefore they exhibit the same transconductance, i.e. $g_{m1} = g_{m2} = g_m$. The filter transfer function is

$$H(s) = \frac{V_{on}}{V_{ip}} = -\frac{1}{s^2 \frac{C_1 C_2}{g_m^2} + s\frac{C_1}{g_m} + 1} \tag{3.2}$$

The pole frequency ω_0 and quality factor Q are respectively given by

$$\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}},\ Q = \sqrt{\frac{C_2}{C_1}} \tag{3.3}$$

No common-mode feedback (CMFB) circuit is needed in this biquad filter topology, since the output CM voltage is fixed to be V_{GS1}+V_{GS2} lower than the input CM voltage. Supposing that the previous PMOS-type stage presents at least a V_{DD}-V_{dsat} (where V_{dsat} = V_{GS}-V_{TH}) output CM voltage, the minimum required supply voltage is

$$V_{DD,min} = 4 \cdot V_{dsat} + 2 \cdot V_{TH} + V_{swing} \tag{3.4}$$

A $V_{DD,min}$ = 1.8V is used in [23]. To reduce the $V_{DD,min}$ of the stacked structure, a folded structure can be instead realized. However, it draws double current because two branches are used.

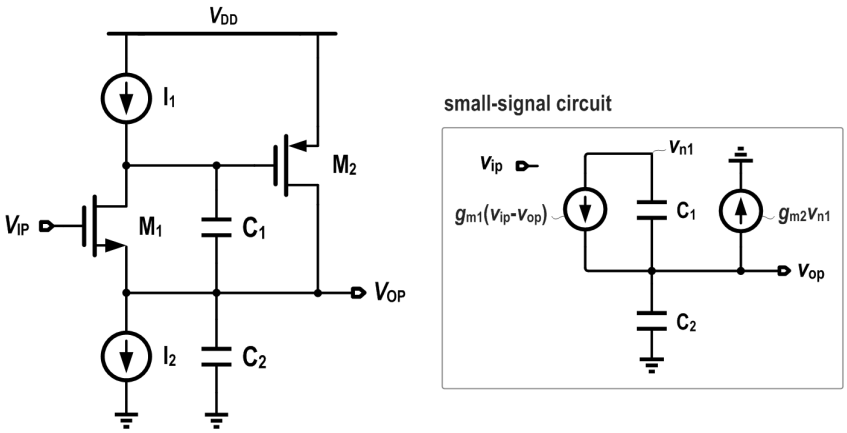


Figure 3.4: Schematic of the biquad LPF using a super source follower.

In [24], a biquad LPF topology exploiting a super source follower is presented, as shown in Fig. 3.4. A smaller output impedance is achieved due to the negative feedback in the super source follower. However, it consumes double current compared to [23],

because transistors M_1 and M_2 providing the transconductance (i.e. g_{m1} and g_{m2}) in the 2nd-order filter transfer function are in two branches. In addition, M_1 and M_2 are implemented using different types of transistors (e.g. M_1: NMOS and M_2: PMOS), which makes the quality factor vulnerable to PVT variations.

A self-coupled source follower based biquad LPF topology in [25], achieving a 2nd-order low-pass transfer function, demonstrates improved power efficiency, higher linearity and smaller output impedance. Transistors M_1 and M_2 employ the same type devices (e.g. NMOS), reuse the same current, and provide the same transconductance while designed with the same size. In this way, the quality factor is determined by the capacitor ratio of C_2/C_1, as shown in (3.3), making it insensitive to PVT variations.

A high-order filter can be implemented with a cascade of the above biquad stages. However, only even-order filter transfer function can be realized.

3.2 Proposed LPF Topology

In this work, a highly compact OTA-free low-pass filter topology with source follower coupling is proposed that can be configured to a 3rd- or 2nd-order transfer function in a single stage. A 5th-order Butterworth filter is designed with a cascade of two proposed filter stages in a 0.18μm CMOS process, achieving 76.8dB dynamic range (DR) while dissipating 0.65mW total power.

Fig. 3.5 shows the single-stage LPF topology, composed of two coupled source followers and three capacitors. The capacitors C_1 and C_2 are connected across the drain and source of M_1 and M_2 in the main source follower (MSF, consisting of I_{B1}, M_1 and M_2), respectively; and C_3 in series with a switch is placed at the source of M_3 to ground the auxiliary source follower (ASF, composed of M_3 and I_{B2}). The gate of M_2 in the MSF is connected through the ASF to the drain of M_1, forming a negative feedback loop. A high linearity is obtained due to this embedded feedback loop. The output signal is delivered at the output node of the MSF, and the output CM voltage is set by the input CM voltage with a gate-source voltage drop of M_1, therefore no CMFB circuit is needed in this filter topology. Additionally, with the use of the ASF with M_3, a larger

input signal swing can be achieved, further improving the in-band linearity and peak signal-to-noise ratio (or dynamic range).

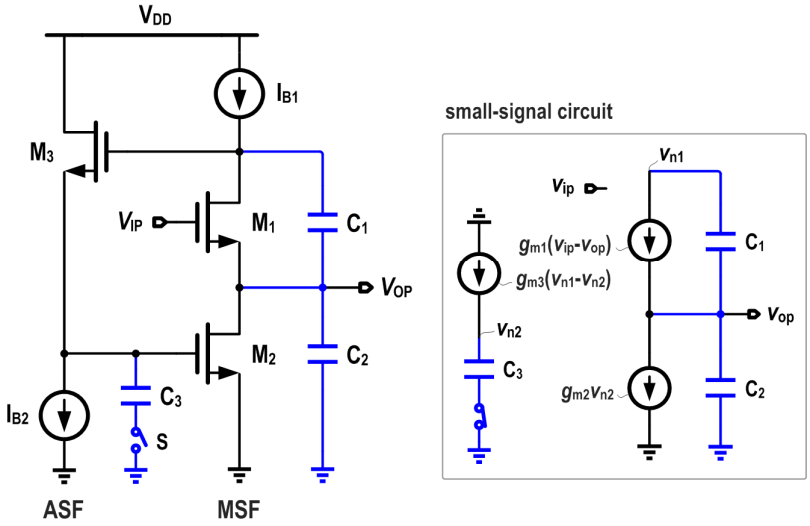


Figure 3.5: Proposed single-stage LPF topology with source follower coupling.

Transistors M_1–M_3 employ the same type devices (e.g. NMOS), and are sized in a ratiometric way (i.e. unit transistors in parallel). Transistors M_1 and M_2 reuse the same current and are designed with the same size, therefore they exhibit the same transconductance (i.e. $g_{m1} = g_{m2} = g_m$, and $g_{m3} = k \cdot g_m$ where $k = I_{B2}/I_{B1}$). Since no circuital parasitic poles are present in the proposed filter topology, there is no need of extra current to push parasitic poles to higher frequencies.

3.2.1 Transfer Function

The equivalent small-signal circuit is also shown in Fig. 3.5, assuming the transistor's output conductance is much smaller than its transconductance. In the mode when the switch is turned on, the filter transfer function is derived as

$$H_{Son}(s) = \frac{1}{s^3 \frac{C_1 C_2 C_3}{g_{m1} g_{m2} g_{m3}} + s^2 \frac{C_1 C_2}{g_{m1} g_{m2}} + s \frac{C_1}{g_{m1}} + 1} \tag{3.5}$$

As illustrated, the proposed filter topology achieves a 3rd-order low-pass transfer function that has one real pole and a pair of complex conjugate poles.

Define the prototyped 3rd-order low-pass transfer function as

$$H_{\mathrm{N}}(s)=\frac{F_{\mathrm{o1}}}{s+F_{\mathrm{o1}}}\cdot\frac{F_{\mathrm{o2}}^{2}}{s^{2}+s\dfrac{F_{\mathrm{o2}}}{Q_{2}}+1} \tag{3.6}$$

in which F_{o1} and F_{o2} are the normalized pole frequencies (with respect to the cut-off frequency $\omega_{\text{cut-off}}$), and Q_2 is the quality factor of the pair of conjugate poles. Map (3.5) with (3.6), and let each coefficient of H_{Son}(s) and H_{N}(s) equal with respect to 's' terms,

$$\begin{cases}\dfrac{C_1C_2C_3}{g_{\mathrm{m1}}g_{\mathrm{m2}}g_{\mathrm{m3}}}=\dfrac{1}{F_{\mathrm{o1}}F_{\mathrm{o2}}^{2}}\cdot\dfrac{1}{\omega_{\text{cut-off}}^{3}}\\[2ex]\dfrac{C_1C_2}{g_{\mathrm{m1}}g_{\mathrm{m2}}}=\left(\dfrac{1}{F_{\mathrm{o1}}F_{\mathrm{o2}}Q_2}+\dfrac{1}{F_{\mathrm{o2}}^{2}}\right)\cdot\dfrac{1}{\omega_{\text{cut-off}}^{2}}\\[2ex]\dfrac{C_1}{g_{\mathrm{m1}}}=\left(\dfrac{1}{F_{\mathrm{o1}}}+\dfrac{1}{F_{\mathrm{o2}}Q_2}\right)\cdot\dfrac{1}{\omega_{\text{cut-off}}}\end{cases} \tag{3.7}$$

From the Butterworth response, $F_{\mathrm{o1}}=F_{\mathrm{o2}}=1$. According to (3.7), for given transistors M_1–M_3 transconductance the capacitor values are then determined by

$$C_2=\frac{g_{\mathrm{m}}}{\omega_{\text{cut-off}}},\ C_1=\left(1+\frac{1}{Q_2}\right)\cdot C_2,\ C_3=k\cdot\frac{C_2^{2}}{C_1} \tag{3.8}$$

As illustrated, the quality factor Q_2 is well defined by the capacitors ratio of C_1/C_2, which is insensitive to PVT variations. Moreover, the cut-off frequency can be properly adjusted via either digital setting of capacitor arrays or the transconductance of M_1–M_3, performing widely programmable bandwidth. It is noted that the above mapping procedure is also applicable for implementing other filter types, such as Chebyshev.

On the other hand, in the mode when the switch is turned off, i.e. $C_3=0$ in (3.5), the filter topology is simply reconfigured to achieve a 2nd-order low-pass transfer function, as given by

$$H_{\mathrm{Soff}}(s)=\frac{1}{s^{2}\dfrac{C_1C_2}{g_{\mathrm{m}}^{2}}+s\dfrac{C_1}{g_{\mathrm{m}}}+1} \tag{3.9}$$

In this case, the pole frequency ω_0 and quality factor Q are respectively derived as

$$\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}},\ Q = \sqrt{\frac{C_2}{C_1}} \tag{3.10}$$

3.2.2 In-Band Linearity Analysis

The negative feedback loop formed by source follower coupling allows to largely suppress the M_1 gate-source voltage swing at low frequency. Therefore, the proposed LPF topology exhibits high in-band linearity.

The filter dc gain is

$$H_{dc} = \frac{g_{m1} r_{o1} (g_{m2} + g_{ds,IB1}) r_{o2}}{g_{m1} r_{o1} (g_{m2} + g_{ds,IB1}) r_{o2} + g_{ds,IB1} r_{o1} + 1} \simeq 1 \tag{3.11}$$

where $g_{ds,IB1}$ is the drain-source conductance of the current source I_{B1}. The suppression to the M_1 gate-source voltage swing is in the order of magnitude of $(g_m r_o)^2$, which is much larger than that in [23]. On the other hand, the voltage buffering is significantly improved while consuming little power with respect to a simple source follower.

Fig. 3.6 plots the simulated magnitude response of v_{op}/v_{ip} and $v_{M1,gs}/v_{ip}$, in which $v_{M1,gs}$, representing the M_1 gate-source voltage incremental, is the difference between the output and input signals. As illustrated, the M_1 gate-source voltage swing is largely suppressed at low frequency. Therefore, high linearity at low frequency is expected. On the other hand, since the suppression to the $v_{M1,gs}$ tends to decrease, the linearity is reduced at higher frequency, as in any closed-loop analog circuit.

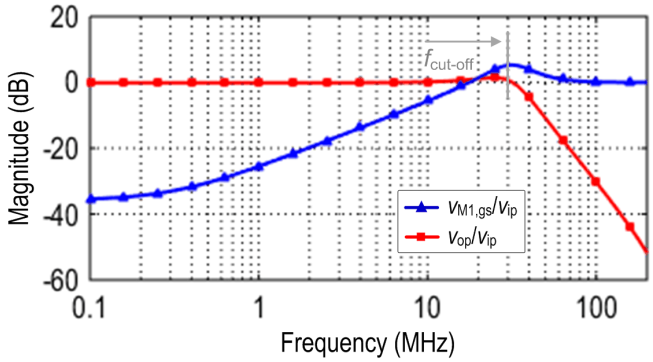


Figure 3.6: Simulated magnitude response of v_{op}/v_{ip} and $v_{M1,gs}/v_{ip}$.

To quantitatively evaluate the in-band linearity, an analysis on IIP3 at low frequency is made assuming the same overdrive voltage (V_{OV}) and channel-length modulation parameter (λ) for each transistor. According to the Taylor series expansion of v_{op} in terms of v_{ip}, the IIP3 is approximately derived as

$$IIP3 = \sqrt{\frac{4}{3}\cdot(\frac{\partial v_{op}}{\partial v_{ip}})/(\frac{1}{6}\cdot\frac{\partial^3 v_{op}}{\partial v_{ip}^3})} \simeq \frac{16}{\sqrt{3}}\cdot\frac{1}{\lambda^3 V_{ov}^2} \tag{3.12}$$

in which $\partial v_{op}/\partial v_{ip} = H_{dc}$, as given in (3.11). Therefore, IIP3 can be improved by decreasing V_{OV}, which differs from what generally occurs in g_m-C filters. In fact, smaller V_{OV} increases the loop gain and consequently the in-band linearity. Thus, for a fixed bias current, decreasing V_{OV} while designing the transistors M_1–M_3 with a larger size ratio can increase the transconductance, offering a power-efficient way to optimize the noise and linearity at low frequency.

3.2.3 Loop Gain

Since the feedback loop reduces the output impedance and the output-referred noise density, the loop gain analysis versus frequency is described. Assuming the output impedance of I_{B1} (denoted as R_{IB1}) is close to $r_{o1,2}$, the loop gain at low frequency is derived as

$$G_{loop,dc} = -g_{m2}\cdot(R_{IB1} \,||\, (g_{m1}r_{o1}r_{o2})) \approx -g_{m2}R_{IB1} \tag{3.13}$$

The loop gain can be increased with either a higher output impedance of I_{B1} (e.g. cascode) or a larger transconductance of M_2. As a result, the proposed source follower coupled topology can be optimized in view of the filter dc gain, in-band linearity and noise without affecting the input transistor M_1.

The loop gain transfer function is derived as

$$G_{loop}(s) \simeq \frac{-g_{m2}R_{IB1}\cdot(1+s\frac{C_1}{g_{m1}})}{1+s\frac{C_1}{g_{m1}}(1+\frac{R_{IB1}}{r_{o1,2}})(1+\frac{C_2}{C_1})+s^2\frac{R_{IB1}}{g_{m1}}C_1C_2}\cdot\frac{1}{1+s\frac{C_3}{g_{m3}}} \tag{3.14}$$

As illustrated, it has a left half plane zero $z_1 = g_{m1}/C_1$, a real pole $p_3 = g_{m3}/C_3$, and a pair of complex conjugate poles whose natural frequency ω_n and quality factor Q_c are respectively defined by

$$\begin{cases} \omega_n = \sqrt{\dfrac{g_{m1}}{R_{IB1}} \cdot \dfrac{1}{C_1 C_2}} \\ Q_c = \dfrac{1}{(1+\dfrac{R_{IB1}}{r_{o1,2}})(1+\dfrac{C_2}{C_1})} \sqrt{g_{m1} R_{IB1} \dfrac{C_2}{C_1}} \end{cases} \tag{3.15}$$

Fig. 3.7 plots the simulated frequency response of the loop gain, and the component parameters in the filter topology are also given. The loop gain is 35dB at low frequency, and degrades from 3MHz due to the conjugate pole pair.

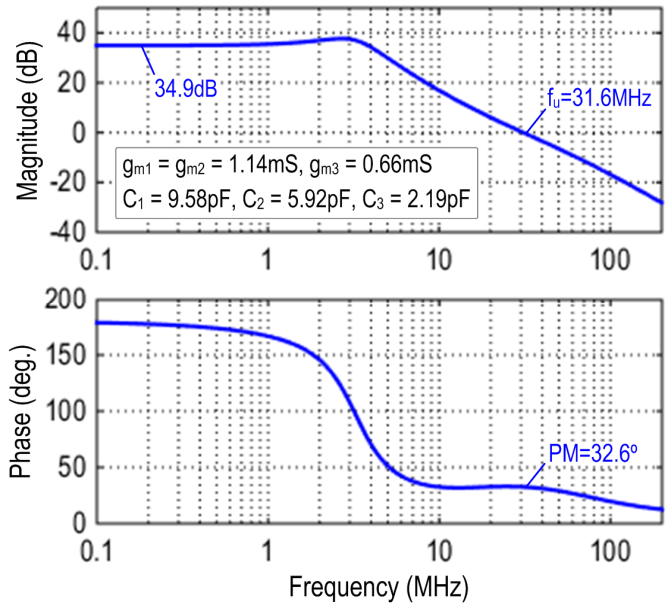


Figure 3.7: Simulated frequency response of the loop gain.

3.2.4 Output Impedance

The output impedance at low frequency is significantly reduced by the loop gain, and is derived as

$$R_{\text{out,dc}} = \left(\frac{R_{\text{IB1}} + r_{\text{o1}}}{1 + g_{\text{m1}} r_{\text{o1}}} \,||\, r_{\text{o2}}\right) / (1 + G_{\text{loop}}) \simeq \frac{1}{g_{\text{m1}} g_{\text{m2}} r_{\text{o1}}} \tag{3.16}$$

The output impedance $R_{\text{out,dc}}$ in this proposed topology with source follower coupling is much smaller compared to a simple source follower that has an equivalent output impedance of $1/g_{\text{m}}$. As a result, it is capable of driving a resistive or capacitive load without substantially affecting the overall linearity.

Fig. 3.8 shows the simulated frequency response of the output impedance R_{out}. The R_{out} increases in the frequency range below 30MHz (i.e. cut-off frequency) since the loop gain tends to degrade, and it then decreases due to the capacitor C_2.

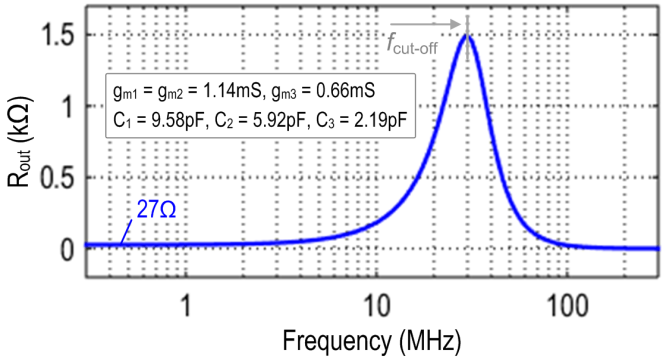


Figure 3.8: Simulated frequency response of the output impedance.

3.2.5 Noise Analysis

The negative feedback loop allows a small output impedance and consequently low input-referred noise (IRN) power spectral density (PSD), since the noise current of M_2 flows into the output node. Furthermore, the noise current of M_3 and I_{B2} is band-passed to the output and therefore largely suppressed at low frequency. The output noise PSD with respect to each noise source in the filter topology is plotted in Fig. 3.9. As expected, the output noise density at low frequency is dominant by M_1 and I_{B1}. In addition, some peaks are present either in M_2, I_{B1} and M_3+I_{B2} terms around the cut-off frequency as the output impedance also peaks.

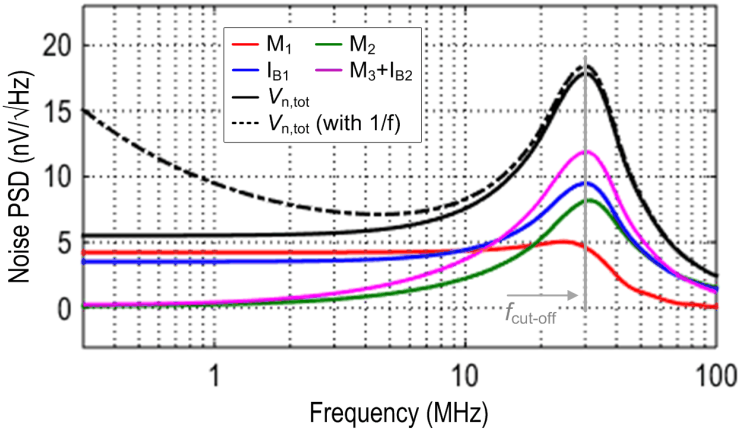


Figure 3.9: Simulated output noise power spectral density w.r.t. each noise source.

Neglecting flicker noise, the output noise density at low frequency is approximately expressed as

$$\upsilon_{\text{n,out}}^2 \simeq \frac{4kT\gamma}{g_{\text{m1}}} + \frac{4kT\gamma g_{\text{m,IB1}}}{g_{\text{m2}}^2} \tag{3.17}$$

where $g_{\text{m,IB1}}$ is the transconductance of the current source I_{B1}, and should be minimized for better noise performance.

This gives an integrated input-referred noise $V_{\text{in,noise}}$, given by

$$V_{\text{in,noise}}^2 \simeq \upsilon_{\text{n,out}}^2 \cdot f_{\text{cut-off}} = \frac{2kT\gamma}{\pi C_2} \cdot (1 + \frac{g_{\text{m,IB1}}}{g_{\text{m}}}) \tag{3.18}$$

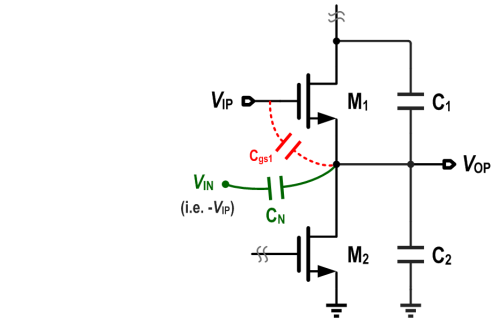
in which $f_{\text{cut-off}}$ is the cut-off frequency, and its expression is obtained from (3.8). The $V_{\text{in,noise}}$ gets smaller when all capacitors (i.e. C_1–C_3) are proportionally increased. Meanwhile, to maintain the same cut-off frequency, the transconductance of transistors M_1–M_3 should be increased by proportionally increasing the transistor channel width and the bias current.

3.2.6 Effect of M_1 Gate-Source Capacitance

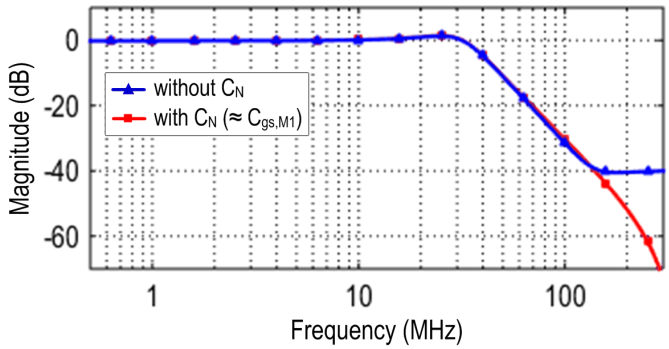
When the gate-source capacitance ($C_{\text{gs,M1}}$) of the input transistor M_1 is considered, the filter transfer function is derived as

$$\hat{H}(s) = H_{\text{Son}}(s) \cdot (s^2 \frac{C_1 C_{\text{gs,M1}}}{g_{\text{m1}} g_{\text{m2}}} + 1) \tag{3.19}$$

As illustrated, $C_{\text{gs,M1}}$ creates a conjugate pair of imaginary zeros in the filter transfer function, which affect the frequency response at high frequencies and limit the stop-band rejection. Negative capacitance realized by cross-coupling two capacitors (ideally equal to $C_{\text{gs,M1}}$) between the differential input and output nodes is employed to eliminate the effect of $C_{\text{gs,M1}}$, as shown in Fig. 3.10(a). The simulated magnitude response without and with C_N is plotted in Fig. 3.10(b).



(a)



(b)

Figure 3.10: Eliminating the effect of M_1 gate-source capacitance: (a) realizing negative capacitance, and (b) simulated magnitude response.

3.3 Implementation of 5th-Order Filter

The proposed single-stage low-pass filter is implemented in a pseudo-differential structure, as shown in Fig. 3.11. Current sources I_{B1} and I_{B2} are designed using a single

transistor. All transistors employ low threshold devices, and are designed with 3× minimum channel length (except M_S) to improve the transistor output impedance. A pair of MOS capacitors are added as transistors M_4 (same type as M_1) with drain and source shorted, and they are cross-coupled between the differential input and output nodes. The size of M_4 is set to about ⅔ of M_1, therefore the MOS capacitance is closely equal to M_1 gate-source capacitance $C_{gs,M1}$. As discussed in Section 3.2.5, they mitigate the effect of $C_{gs,M1}$ at high frequencies. Moreover, no CMFB circuit is required in this filter implementation.

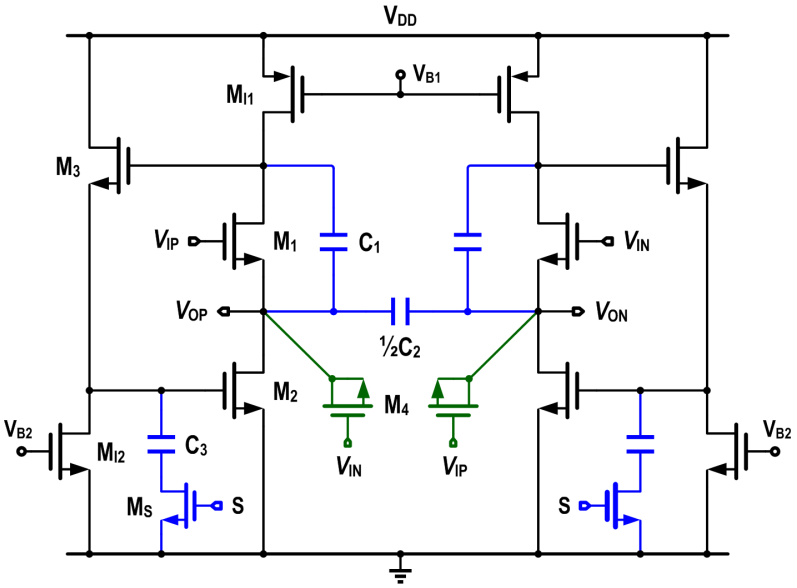


Figure 3.11: Pseudo-differential implementation of the proposed single-stage 3rd/2nd-order low-pass filter.

A 5th-order Butterworth filter prototype is designed using a cascade of two proposed filter stages, as shown in Fig. 3.12. The component parameters in each filter stage are also illustrated targeting a 30MHz nominal bandwidth. The first filter stage (STG1) employs NMOS-type source followers and achieves a 3rd-order transfer function by configuring the switch on. The second filter stage (STG2) uses PMOS-type and achieves a 2nd-order transfer function by not placing a capacitor at the gate of M_{2b} (to save area). The use of cascading NMOS and PMOS structures makes the input and output CM voltages of the entire 5th-order filter almost the same, balancing out the gate-source level shift in each filter stage.

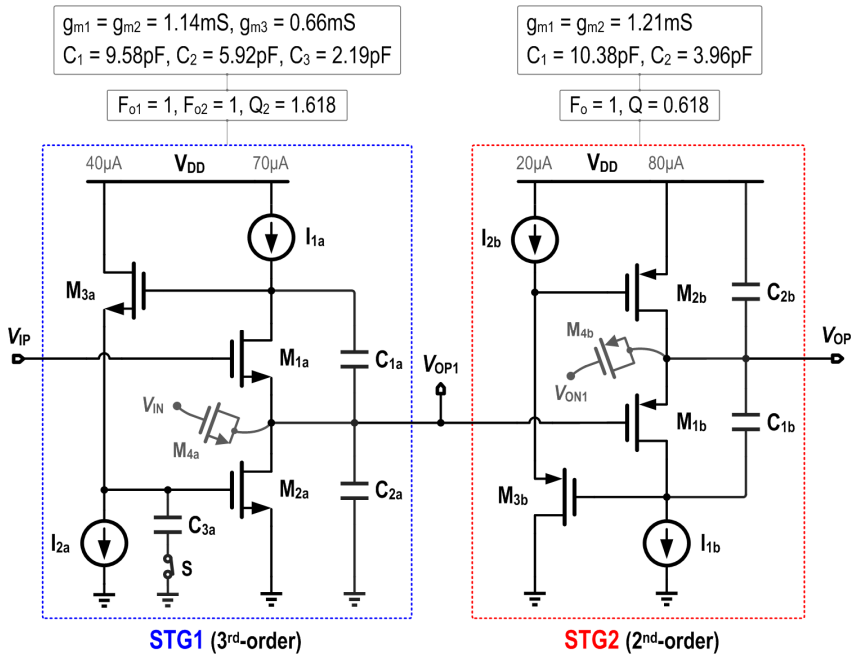
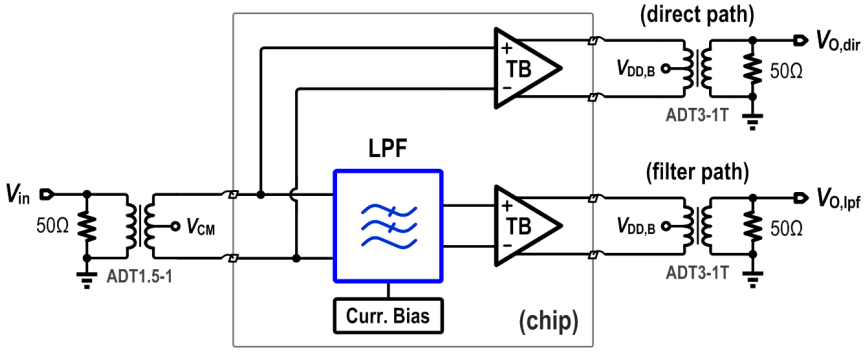
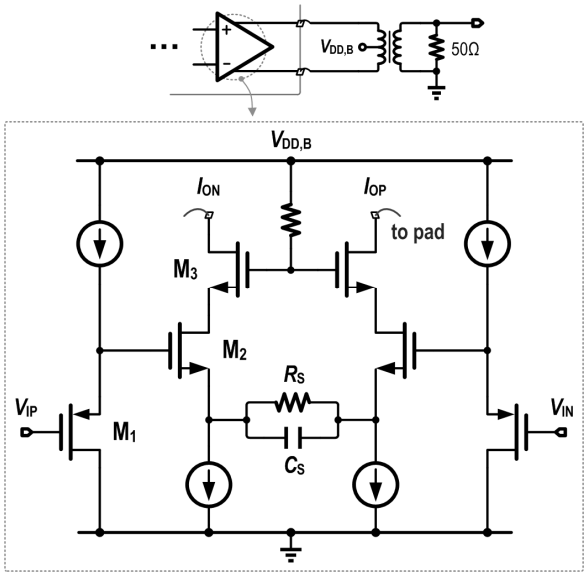


Figure 3.12: 5th-order Butterworth filter prototype (single-ended illustration).

Fig. 3.13(a) illustrates the complete diagram of the filter architecture, in which the LPF core, current bias circuit and two test buffers (TBs) are integrated on-chip. The direct path is measured to de-embed the effect of test buffers when evaluating the filter frequency response and output-referred noise. The test buffer, as shown in Fig. 3.13(b), is comprised of a cascade of a source follower and a source-degenerated open-drain amplifier topology for high linearity. The capacitor C_S in parallel with R_S is employed as source degeneration to extend the bandwidth. The buffer output is differential current that is terminated with an off-chip transformer to drive the 50Ω load. In this way, the effects of pads and bonding wires are mitigated.



(a)



(b)

Figure 3.13: Filter architecture including two on-chip test buffers: (a) measurement setup, and (b) schematic of the test buffer.

3.4 Measurement Results

The prototyped filter (including two on-chip test buffers) is fabricated in a 0.18µm CMOS process, and occupies an active area of 0.12mm^2. The die micrograph is shown in Fig. 3.14. As shown, the core area is dominated by capacitors. The layout is placed symmetrically to minimize the mismatch between differential half-side circuits.

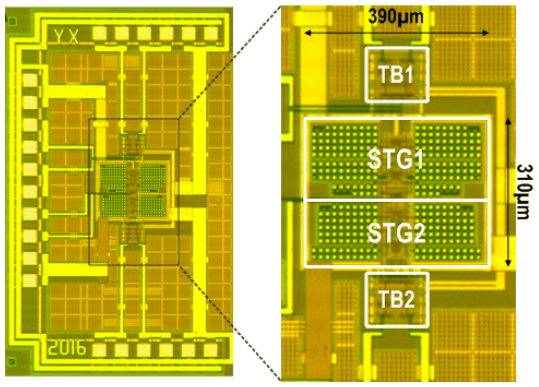
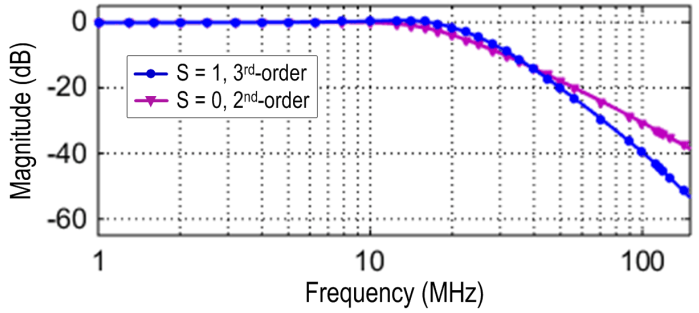


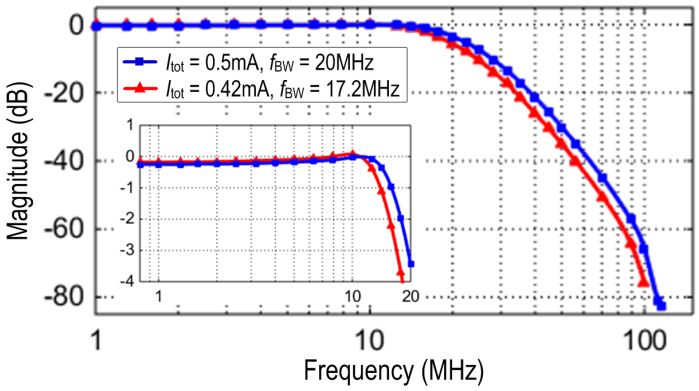
Figure 3.14: Die micrograph.

Operating with a 1.3V supply voltage, the filter consumes 0.65mW total power and

achieves a -3dB bandwidth of 20MHz. The measured magnitude response of the first filter stage (i.e. STG1), for two modes of operation via the switch, is depicted in Fig. 3.15(a). As illustrated, the proposed single-stage filter topology can be easily configured to either 3rd-order or 2nd-order while configuring the switch on or off, respectively. The magnitude response of the complete 5th-order filter for two different bias currents is shown in Fig. 3.15(b). The feasibility of finely tuning the filter bandwidth by adjusting the bias current (to vary transistors M_1−M_3 transconductance) is demonstrated. Moreover, the stop-band rejection of 82dB is measured.



(a)



(b)

Figure 3.15: Measured magnitude response of (a) the first filter stage (i.e. STG1), and (b) the complete 5th-order filter for two different bias currents.

Fig. 3.16 shows the output spectrum measured with a +6.6dBm (i.e. $1.35V_{pk\text{-}pk}$) input signal at 2MHz. It creates -40.2dBc 3rd-order harmonic distortion (i.e. highest spurious tone) at the output, meanwhile the total harmonic distortion (THD) is -39.5dB. The 1dB compression point (CP_{1dB}) is defined as the power level that causes the gain

to drop by 1dB from its small-signal value. Fig. 3.17 plots the 1dB compression point measurement with a 2MHz input signal. The measured input CP_{1dB} is +10.1dBm (with respect to 50Ω).

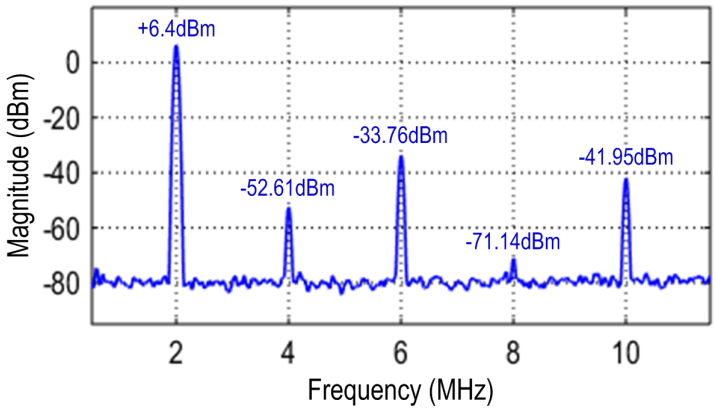


Figure 3.16: Output spectrum with 0.675m$V_{0\text{-}pk}$ input signal at 2MHz.

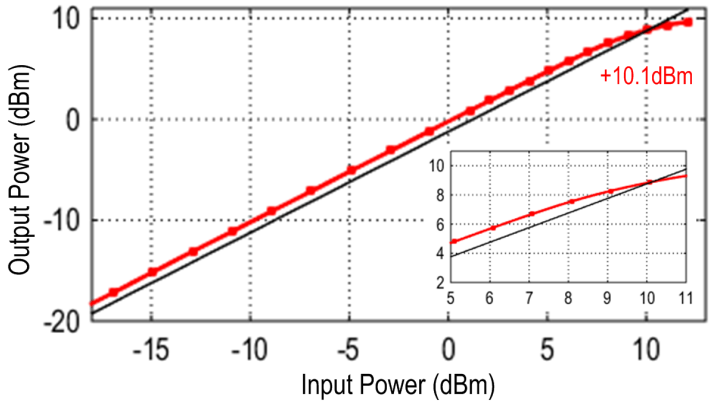


Figure 3.17: Measured 1dB compression point with a 2MHz input signal.

The in-band linearity of the filter (including the test buffer) is evaluated by feeding two input tones at 1.9MHz and 2.1MHz. The measured output spectrum for the two-tone input signals with 0.15$V_{0\text{-}pk}$ amplitude for each tone is shown in Fig. 3.18. Under this condition, the 3rd-order intermodulation (IM3) measures at 63.5dB. Fig. 3.19 shows the in-band 2nd- and 3rd-order intermodulation terms versus input power. The resulting IIP2 and IIP3 are +58.5dBm and +28.8dBm, respectively.

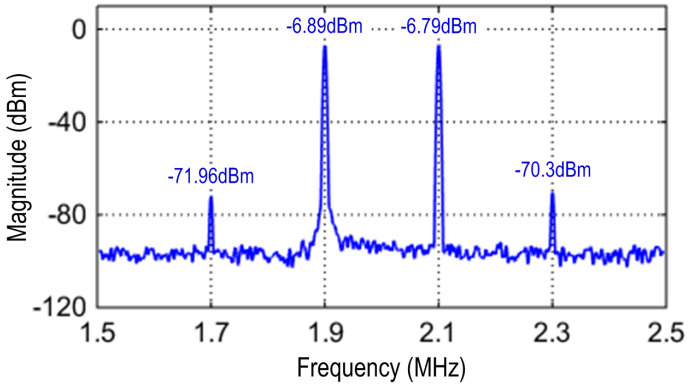


Figure 3.18: Measured output spectrum for two-tone input signals.

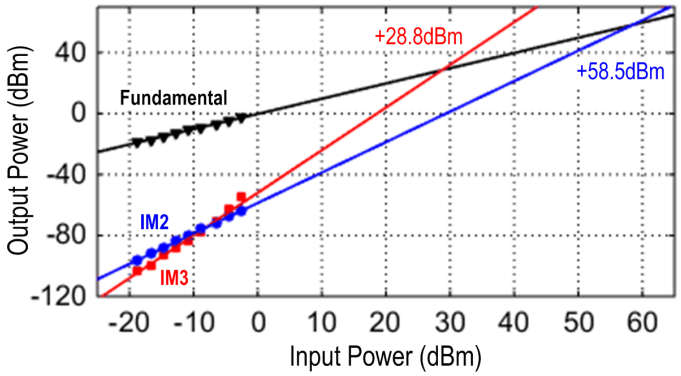


Figure 3.19: In-band IIP2 and IIP3 measurement.

To measure the output noise PSD of the low-pass filter, the input port is grounded. A two-step experiment is carried out: 1) measuring the output noise density of the direct path (i.e. only the test buffer), 2) measuring the total output noise density of the filter path including the LPF core and test buffer. Then, since the noise of the filter core and the test buffer are uncorrelated, the filter noise is calculated by subtracting the buffer noise PSD in step 1) from the total noise PSD in step 2). The measured output noise power spectral density of the de-embedded filter is plotted in Fig. 3.20. For frequencies lower than 1MHz, flick noise is dominant. Around the cut-off frequency (i.e. 20MHz), the peak is present since the output impedance of the single-stage filter topology also peaks. Integrating the noise PSD from 100kHz to 20MHz gives 68.4μV_{rms}, and the averaged IRN over the bandwidth is 15.3nV/$\sqrt{Hz}$. It is noted that the minimum spot noise density in the signal-band is around 11.7nV/$\sqrt{Hz}$. The DR (at 1% THD) is 76.8dB.

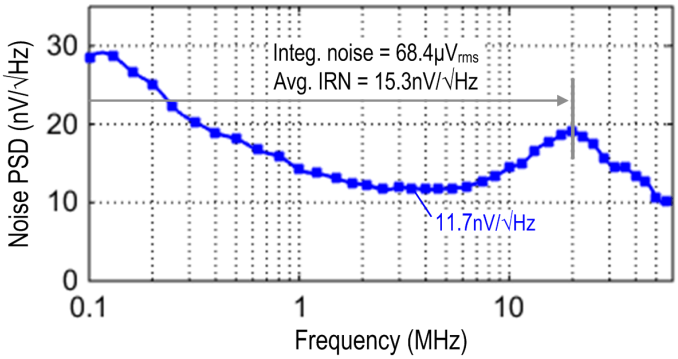


Figure 3.20: Measured output noise spectral density of the de-embedded filter.

Table 3.1 summarizes the filter performance and compares with recent state-of-the-art LPFs [4−5], [19−25]. The presented filter with source follower coupling in this work achieves competitive power-per-pole/bandwidth efficiency and excellent in-band linearity while dissipating little power.

A figure-of-merit (FoM) expression taking into account the spurious-free dynamic range (SFDR) is used to evaluate the filter performance, as defined by [21−22]

$$FoM = \frac{P_{\text{tot}} / N}{f_{\text{BW}} \cdot SFDR \cdot N^{4/3}} \tag{3.20}$$

where P_{tot} is the total power consumption, N is the number of poles (i.e. filter order), f_{BW} is the -3dB bandwidth, and $SFDR \cdot N^{4/3}$ is the normalized spurious-free dynamic range with $SFDR = (IIP3/P_{\text{N}})^{2/3}$ (where P_{N} is the input-referred noise power). In order to better evaluate the filter performance in large signal amplitude condition, another type of FoM is defined that utilizes the DR (1% THD) in the expression [27−28], as given by

$$FoM_{\text{DR}} = \text{DR} + 10 \cdot \log_{10}\left(\frac{f_{\text{BW}}}{P_{\text{tot}} / N}\right) \tag{3.21}$$

in which $(P_{\text{tot}}/N)/f_{\text{BW}}$ is the power-per-pole/bandwidth efficiency.

As illustrated in Table 3.1, the presented filter in this work achieves the best FoMs in both definitions compared with other state-of-the-art LPFs.

Table 3.1: Filter performance summary and comparison with state-of-the-art

	This work	[25] VLSI'16		[24] JSSC'15	[23] ISSCC'06	[5] ISSCC'13
Technology	0.18µm	0.18µm		0.18µm	0.18µm	65nm
Architecture	source follower coupling	self-coupled source follower		super source follower	source follower	DT IIR
V_{DD} (V)	1.3	1.35		1.8	1.8	1.2
Filter Order	5^{th}	4^{th}	6^{th}	4^{th}	4^{th}	7^{th}
Bandwidth (MHz)	20	30.8	21.4	33	10	0.4−30
Power (mW)	0.65	0.62	0.93	1.38	4.1	1.96
Power-per-pole/BW (mW/MHz)	0.0065	0.005	0.0072	0.011	0.103	0.7−0.009[b]
$V_{in,THD=-40dB}$ ($V_{0\text{-}pk}$)	0.675	0.605	0.54	0.225	0.3	0.21
Input CP_{1dB} (dBm)	10.1	8.6	10	8	5	0.7
In-band IIP3 (dBm)	28.8	29.1	28.2	18	17.5	16[c]
IRN ($nV_{rms}/\sqrt{Hz}$)	15.3	22.6	31.6	7.83	7.6	4.57[d]
(1% THD) DR (dB)	76.8	71	68.5	70	79	80.7[d]
FoM ($dB(J^{-1})$)[a]	187.2	183.7	183.0	179.1	172.5	184.2[c]
FoM_{DR} (dB)	188.7	184.0	179.9	179.8	178.9	185.8
Core Area (mm^2)	0.12	0.1	0.14	0.14	0.26	0.42

[a] calculated with $10 \cdot \log_{10}(1/FoM)$ [b] same order of filter BW [c] for 2.9MHz BW [d] avg. for 9MHz BW [24]

Table 3.1: Filter performance summary and comparison (Continued)

	[4] ISSCC'12	[22] JSSC'11	[21] JSSC'09	[27] JSSC'06		[20] JSSC'07	[19] JSSC'06
Technology	90nm	90nm	0.18µm	0.13µm		0.13µm	0.12µm
Architecture	ring osc. integrator	g_m-C	g_m-C	active-g_m-RC		active-RC	active-RC
V_{DD} (V)	0.55−0.9[b]	1.0	1.2	1.2		1.5	1.0
Filter Order	4^{th}	6^{th}	3^{rd}	4^{th}		5^{th}	5^{th}
Bandwidth (MHz)	7−30	8.1−13.5	0.5−20	2.11	11	19.7	5−10
Power (mW)	2.9−19.1[b]	4.35	4.1−11.1[b]	3.4	14.2	11.25	4.6
Power-per-pole/BW (mW/MHz)	0.104−0.16[b]	0.09−0.054[b]	2.7−0.185[b]	0.403	0.323	0.114	0.18−0.092[b]
$V_{in,THD=-40dB}$ ($V_{0\text{-}pk}$)	N/A	0.47	N/A	0.56	0.56	0.53[h]	0.16−0.36
Input CP_{1dB} (dBm)	N/A	7.6	N/A	11	10.6	5	3.6
In-band IIP3 (dBm)	16.7[e]	21.7−22.1	22.3−19	21	21	18.3	18.8−21.3
IRN ($nV_{rms}/\sqrt{Hz}$)	23.7−32.8[b]	75	425−12	24.78	10.85	30	143−85.4
(1% THD) DR (dB)	65.5	63	N/A	80.8	80.8	69	N/A
FoM ($dB(J^{-1})$)[e]	166.4[e]	166.1[f]	167.5[g]	166.5	167.5	163.9	162.1[f]
FoM_{DR} (dB)	165.3	164.4	N/A	174.8	175.8	168.4	N/A
Core Area (mm^2)	0.29	0.24	0.23	0.9		0.2	0.25

[e] for 7MHz BW [f] for 10MHz BW [g] for 20MHz BW [h] THD = -49.1dB

Fig. 3.21 plots the FoM_{DR} (from Table 3.1) versus the filter bandwidth. The FoM_{DR} in this work is even above 20dB improvement over the least ones [4], [22], [20].

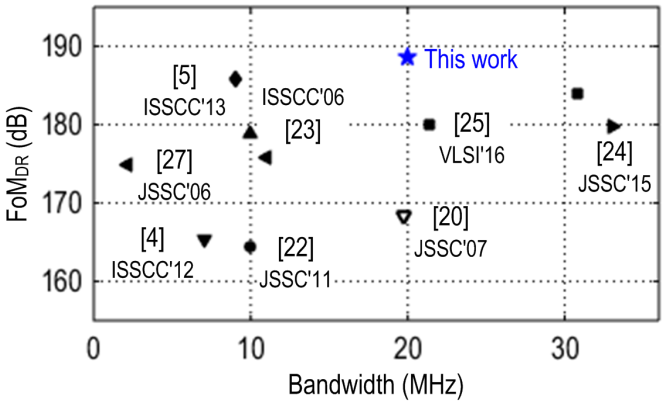


Figure 3.21: FoM_{DR} plot versus bandwidth.

3.5 Summary

In this chapter, a highly compact single-stage $3^{rd}/2^{nd}$-order low-pass filter topology with source follower coupling is proposed that requires no OTAs. This filter topology exhibits inherently high in-band linearity due to the source follower coupled negative feedback while consuming little power. A 5^{th}-order Butterworth prototype is designed with a cascade of two proposed filter stages in a 0.18µm CMOS process. A cut-off frequency of 20MHz and a dynamic range (at 1% THD) of 76.8dB are measured with a total power consumption of 0.65mW from a 1.3V supply voltage. The presented filter with source follower coupling in this work favorably compares with other state-of-the-art LPFs.

CHAPTER 4. PSEUDO-DIFFERENTIAL-VCO BASED CT ΔΣ ADC WITH RESIDUE SELF-COUPLING TECHNIQUE

Continuous-time (CT) ΔΣ ADCs have been widely employed in wireless receiver applications due to their inherent anti-aliasing filtering characteristic. By incorporating a CT ΔΣ ADC into the receiver, it could largely simplify analog baseband circuits (Fig. 1.1) and therefore reduce the total power consumption from the system level [29]. For the targeted signal bandwidth, conventional ΔΣ ADCs combine multi-bit quantization, a high-order loop filter with an appropriate oversampling ratio to achieve the desired resolution. However, amplifiers used to implement the loop filter incur a large power penalty, and designing precise analog comparators in submicron CMOS processes is also a challenging task.

Voltage-controlled oscillator (VCO) based ΔΣ ADCs have recently emerged as an alternative to conventional ΔΣ architectures. The VCO-based quantizer [30] achieves first-order noise shaping in an open-loop manner with neither an active integrator nor a feedback digital-to-analog converter (DAC). Furthermore, it is implemented using mostly digital circuits such as CMOS inverters, flip-flops and logic gates. Therefore, it benefits from process scaling and is capable of operating with a GHz sampling clock frequency. However, the performance of VCO-based ΔΣ ADCs is severely limited by the nonlinearity of the VCO's voltage-to-frequency (V-to-F) transfer curve.

A pseudo-differential-VCO based continuous-time ΔΣ ADC with a residue self-coupling technique is described in this chapter, which is implemented with mostly digital circuits while achieving excellent power efficiency.

4.1 Overview of VCO-based Quantizer

An efficient high-speed implementation of a VCO-based quantizer (VCOQ) [30] is depicted in Fig. 4.1(a). An inverter-based ring VCO converts the input voltage into a proportional oscillation frequency. The key idea is to observe whether a given VCO

delay cell undergoes a transition within a given sampling clock period by comparing samples of its current and previous states with an XOR operation [30]. The number of VCO delay cells that have experienced a transition within a given clock period is a function of the delay through each stage as set by the input voltage V_{IN}, which yields the digital output code. This topology assumes that the number of edges traveling through the ring oscillator during one sampling clock period never exceeds the number of oscillator stages. Stated a different way, the VCO frequency range should be designed such that it remains less than half of the sampling frequency.

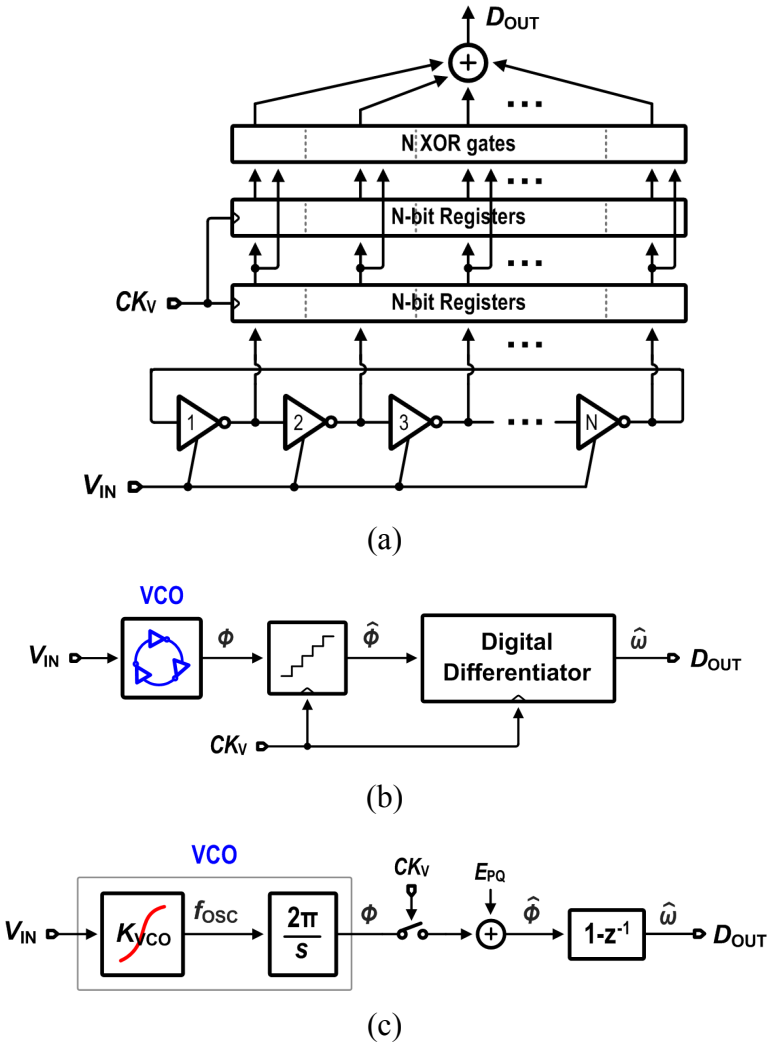


Figure 4.1: VCO-based quantizer: (a) an efficient high-speed implementation, (b) block diagram, and (c) linearized frequency-domain model.

To better understand the properties of the VCO-based quantizer, Fig. 4.1(b) and (c) shows the block diagram and linearized frequency-domain model. The ring oscillator is represented as a phase-domain integrator that is expressed as $2\pi K_{VCO}/s$ (where K_{VCO} is the VCO's V-to-F conversion gain). The phase quantizer block corresponds to the first set of registers that sample and digitize the oscillator output phase, which is modeled as a sampler that adds quantization noise. The sampled phase is then digitally differentiated to generate the quantized frequency output by comparing the register values to their previous sample values with the XOR operation. In this way, the digital differentiator block is seen as a $(1-z^{-1})$ transfer function.

According to the model in Fig. 4.1(c), the phase-domain quantization noise E_{PQ} is first-order noise shaped. In another word, the noise transfer function (NTF) is

$$NTF(z) = \frac{D_{OUT}}{E_{PQ}} = 1 - z^{-1} \tag{4.1}$$

For an N-stage VCO, there are $2N$ quantized levels of the VCO phase, and each phase tap is delayed from the previous one by π/N. It is also noted that the VCO input voltage is integrated over a clock period, and the quantized output is ready on the next positive edge of the sampling clock. Therefore, there is a delay in the signal path of the VCO-based quantizer. The signal transfer function (STF) is derived as

$$STF(z) = \frac{D_{OUT}}{V_{IN}} = 2NK_{VCO}T_S \cdot z^{-1} \tag{4.2}$$

where T_S is the sampling clock period. As illustrated in (4.2), the low-pass magnitude response of the STF provides implicit anti-aliasing filtering characteristic.

4.1.1 Theoretical SQNR

To obtain the signal-to-quantization-noise ratio (SQNR), the input signal is assumed to be $x(t) = A \cdot \cos(\omega_{in} t)$ (where A is the amplitude, and ω_{in} is the signal frequency). The sampled VCO phase output is

$$\phi[n] = \int_{0}^{nT_S} 2\pi(K_{VCO}x(t) + f_{fr})dt \tag{4.3}$$

where f_{fr} is the free-running oscillation frequency. The phase-domain input signal $\phi_x[n]$, i.e. the phase incremental within one clock period, can be described as

$$\phi_x[n] = \int_{(n-1)T_S}^{nT_S} 2\pi K_{VCO}x(t)dt = A_\phi \cdot \cos(\omega_{in} \cdot (n - \frac{1}{2})T_S) \tag{4.4}$$

in which $A_\phi = 2\pi K_{VCO} A T_S \,\mathrm{sinc}(f_{in}T_S)$ (where sinc(x) = sin(πx)/(πx)). At low frequencies (i.e. $f_{in} << f_S$), $|\mathrm{sinc}(f_{in}T_S)| \simeq 1$, therefore $A_\phi \simeq 2\pi K_{VCO} A T_S$. Hence, the phase-domain input signal power can be represented as

$$P_{\phi_x} = \frac{1}{2} A_\phi^2 = 2(\pi K_{VCO} A T_S)^2 \tag{4.5}$$

Since there is no correction between the VCO output phase and the sampling clock edge, phase-domain quantization noise can be assumed to be random and uniformly distributed between ±½·(π/N). Therefore, the phase-domain quantization noise power over a signal bandwidth of f_B can be obtained using a similar method to that of a conventional first-order ΔΣ ADC, given by

$$P_{qn} = \frac{1}{12}(\frac{\pi}{N})^2 \frac{\pi^2}{3}(\frac{1}{OSR})^3 \tag{4.6}$$

where $OSR = f_S/(2f_B)$ is the oversampling ratio.

From (4.5) and (4.6), the theoretical SQNR can be derived as [31]

$$SQNR = 10 \cdot \log_{10}(\frac{P_{\phi_x}}{P_{qn}}) = 6.02M_q - 3.41 + 30 \cdot \log_{10}(OSR) \tag{4.7}$$

where M_q is the quantizer resolution, which can be represented as

$$M_q = \log_2(4NK_{VCO}AT_S) = \log_2(\frac{2Nf_{tune}}{f_S}) \tag{4.8}$$

in which f_{tune} is the tuning range of the VCO (i.e. $f_{tune} = 2K_{VCO}A$). Doubling the OSR in the conventional first-order ΔΣ ADC gives 9dB improvement in SQNR. According to

(4.7), keeping K_{VCO} fixed and doubling the *OSR* improves the SQNR of the VCO-based quantizer by only 3dB. Therefore, to keep the performance the same, K_{VCO} needs to be doubled. As illustrated, the gain factor of $2f_{tune}/f_S$ in (4.8) provides another degree of freedom in this ADC design to optimize the SQNR.

4.1.2 VCO Phase noise

The VCO phase noise is modeled to be added at the VCO output. As illustrated in Fig. 4.1(c), the VCO phase noise is first aliased due to sampling and then shaped by the high-pass filter of $(1-z^{-1})$. If assuming that the VCO has a phase noise of L at a frequency offset of f_{offset} and a slope of -20dB/decade, the frequency-domain noise power spectral density can be expressed as

$$S_{\phi_{pn}}(\Omega) = \frac{L}{2\pi}\left(\frac{2\pi f_{offset}}{\Omega}\right)^2 \tag{4.9}$$

The noise power in the signal band is derived as [31]

$$P_{\phi_{pn}} = 2\int_0^{\omega_B} |1-e^{-j\omega T_S}|^2 \cdot S_{\phi_{pn}}(\omega)d\omega \simeq 8\pi^2 L T_S^2 f_{offset}^2 f_B \tag{4.10}$$

Therefore, the SNR due to the VCO phase noise can be derived as

$$SNR_{pn} = \frac{P_{\phi_x}}{P_{\phi_{pn}}} = \frac{(K_{VCO}A)^2}{4Lf_{offset}^2 f_B} \tag{4.11}$$

4.1.3 Prior Solutions to Combat VCO Nonlinearity

In the discussion thus far, we assumed that the VCO frequency is a linear function of the input voltage, leading to a constant gain K_{VCO}. However, in most practical VCO implementations, the VCO suffers from a nonlinear voltage-to-frequency transfer curve that causes the VCO-based ADC performance to be severely distortion limited. Several techniques to mitigate VCO nonlinearity have been proposed, some of which will be briefly discussed in the following.

A digital background calibration technique is illustrated in Fig. 4.2, which employs a calibration unit to cancel the 2nd- and 3rd-order distortion terms caused by the VCO nonlinear V-to-F transfer curve [32]. The calibration unit uses a replica VCO to measure the nonlinearity coefficients. The estimated distortion is stored in a look-up table and used to correct the main VCOQ output. While this work demonstrates improved linearity, the effectiveness replies on the matching between the replica and the main VCO for good cancellation of the nonlinearity. Moreover, the calibration algorithm is complex and takes very long time to converge.

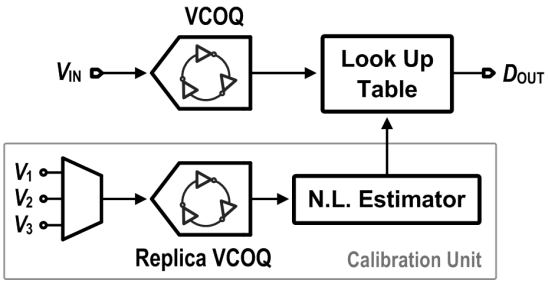


Figure 4.2: Coefficient estimation based digital background calibration technique.

The magnitude of distortion terms also depends on the input signal amplitude, therefore, the impact of VCO nonlinearity on the ADC performance can be mitigated by not exercising the nonlinear region of the VCO's V-to-F transfer curve. The VCO-based residue cancelling quantizer [33], as shown in Fig. 4.3, seeks to minimize the voltage swing at the VCO input.

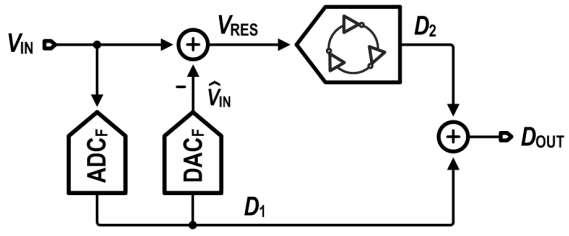


Figure 4.3: Block diagram of the VCO-based residue cancelling quantizer.

Analogous to a classical two-step ADC structure, the input voltage V_{IN} is firstly digitized by a flash ADC (ADC_F), and a coarse estimate of the input voltage, $\hat{V}_{IN}$, is obtained using a digital-to-analog converter (DAC_F). The residue V_{RES}, is generated by

subtracting $\hat{V}_{IN}$ from the input voltage V_{IN}. The V_{RES}, equal to the quantization error of ADC_F, is subsequently digitized by a VCO-based quantizer. When the two digital outputs are added to produce the overall output, the residue, i.e. the quantization error of ADC_F, is cancelled. Therefore, D_{OUT} contains only first-order shaped quantization noise from the VCO-based quantizer. Because VCO processes only a small residue voltage, it spans only a small region of its nonlinear V-to-F transfer curve, thus mitigating the impact of VCO nonlinearity on the ADC performance. In [34], the ADC_F is replaced by a VCO-based quantizer, further improving the power efficiency.

4.2 ΔΣ ADC Using VCO-based Integrator and Quantizer

A closed-loop ΔΣ ADC architecture that uses the VCO phase rather than its frequency (Fig. 4.1) as the output variable [35] is shown in Fig. 4.4. The sampled VCO output phase is measured by comparing it with a reference phase derived from the sampling clock using XOR gates. The resulting digital output is fed back through a DAC to the input of the feedback loop. The VCO acts as a phase-domain integrator, which largely suppresses the signal swing at the VCO input. Therefore, the VCO spans only a small region of its nonlinear V-to-F transfer curve, mitigating the impact of VCO nonlinearity on the ADC performance.

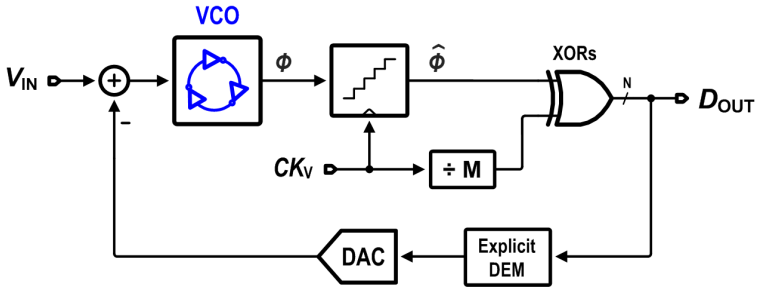


Figure 4.4: Voltage-to-phase VCO-based 1st-order ΔΣ ADC.

However, the intrinsic dynamic weighted averaging (DWA) capability, which the VCO-based quantizer has due to the digital differentiation at the VCO output [30], is lost in this phase-output ΔΣ ADC architecture. To shape the DAC mismatch, an explicit dynamic element matching (DEM) block is inserted which leads to increased design

complexity and power. On the other hand, analogous to a phase-locked loop in which phase error is quantized, the VCO nominal oscillation frequency has to be equal to the reference clock frequency (i.e. the sampling frequency divided by *M*).

To simultaneously use the VCO as an integrator and maintain an intrinsic DEM capability, a first-order ΔΣ ADC architecture using a pseudo-differential VCO-based integrator and phase quantizer is described in [36], as shown in Fig. 4.5. The two VCOs are arranged in a pseudo-differential manner. The digital output is resulted by comparing the sampled output phase of one VCO with that of the other using an array of XOR gates. Then the digital output is fed back through a DAC to the input of the VCOs. The feedback loop operates only on the difference between the two VCO output phases, and does not control the VCO center frequency. As a result, unlike [35], the VCO nominal oscillation frequency can be freely chosen to optimize the power. Moreover, the common-mode phase of the two VCOs simply accumulates and wraps around 2π at a speed of twice the VCO center frequency. Consequently, this results in a natural rotation of the middle point of the DAC element selection pattern. This effectively realizes a data-independent DEM scheme of clock averaging (CLA) that shapes the DAC mismatch errors [36]. In a transistor-level simulation with a 15-stage VCO, Fig. 4.6 depicts the selection pattern of the 15 DAC elements. It is noted that the VCO center frequency is designed to be around a quarter of the sampling frequency, therefore the middle point of the selected DAC elements in each sample is shifted by 9 from that in the previous sample.

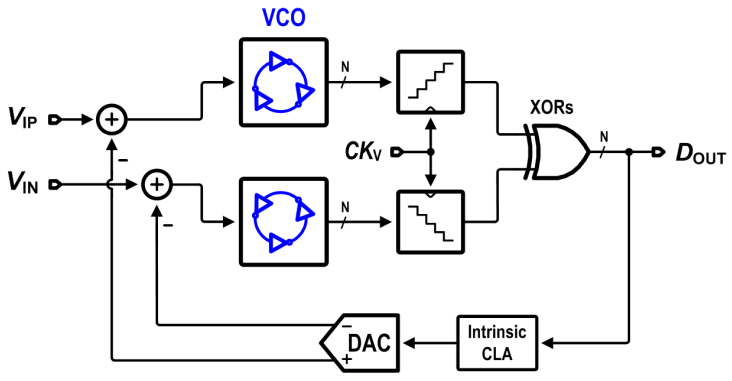


Figure 4.5: The 1st-order ΔΣ ADC using a pseudo-differential VCO-based integrator and phase quantizer.

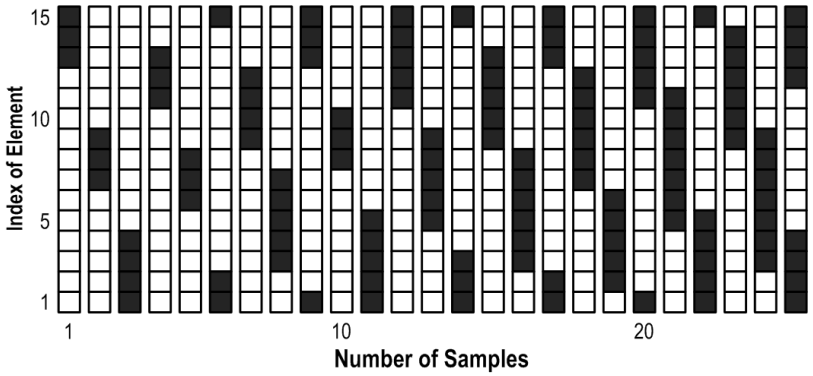


Figure 4.6: DAC element selection pattern.

Fig. 4.7 shows the linearized model of the 1st-order ΔΣ ADC architecture in Fig. 4.5. Denoting $\pm V_{REF}$ as the reference voltages of the feedback DAC, $2V_{REF}/(N+1)$ is the DAC conversion gain. Analogous to a conventional first-order ΔΣ ADC in which the loop transfer function is f_S/s,

$$\frac{2\pi K_{VCO}}{s}\cdot\frac{N}{\pi}\cdot\frac{2V_{REF}}{N+1}=\frac{f_S}{s} \tag{4.12}$$

Therefore, the desired VCO V-to-F conversion gain K_{VCO} is derived as

$$K_{VCO}=\frac{N+1}{N}\cdot\frac{f_S}{4V_{REF}} \tag{4.13}$$

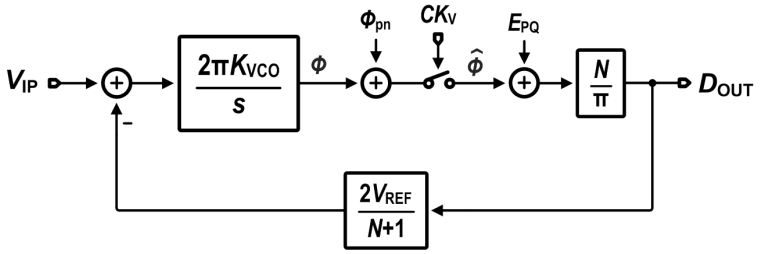


Figure 4.7: Linearized model of the 1st-order ΔΣ ADC in Fig. 4.5.

Substituting (4.13) into (4.7) with $A = V_{REF}$, the theoretical SQNR is derived as

$$SQNR=6.02\cdot\log_2(N+1)-3.41+30\cdot\log_{10}(OSR) \tag{4.14}$$

Since the phase noise of the two VCOs are uncorrelated, according to (4.11), the signal-to-phase-noise ratio (SPNR) is derived as

$$SNR_{\text{pn}} = \frac{P_{\phi_x}}{2P_{\phi_{\text{pn}}}} = \left(\frac{N+1}{N}\right)^2 \cdot \frac{OSR^2 f_B}{32Lf_{\text{offset}}^2} \tag{4.15}$$

4.3 Proposed ΔΣ ADC Architecture

Conventional ΔΣ ADCs incorporate the 1st-order ΔΣ ADC topology using VCO-based integrator and quantizer as the back-end stage to achieve high-order noise shaping with a preceding loop filter [35], as shown in Fig. 4.8. However, it turns out that the voltage swing at the VCO input (V_{R2}) becomes larger compared to the 1st-order ΔΣ ADC with the same input signal V_{IN}. Though the loop filter $L(s)$ suppresses the VCO nonlinearity to the extent of its gain in the signal bandwidth, the large voltage swing of V_{R2} makes it difficult to implement the driver stage that controls the VCO. For instance, in [37] a power-hungry operational amplifier is used to realize the subtraction at the VCO input and directly drive the control terminal of the VCO.

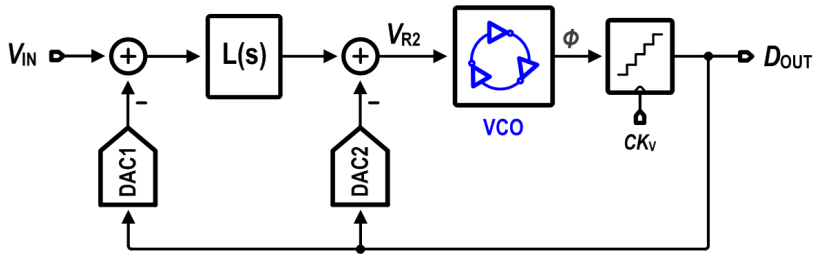


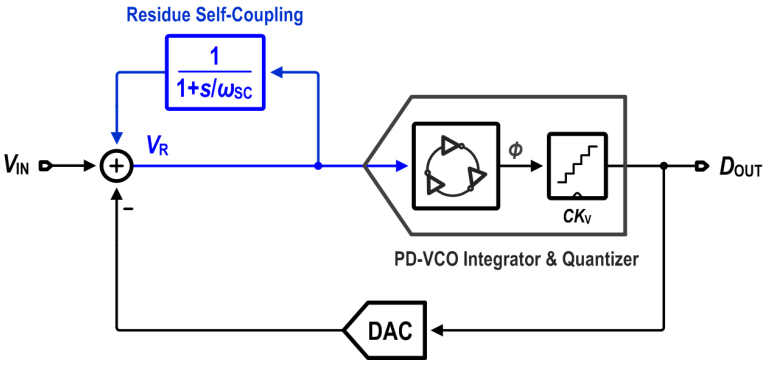
Figure 4.8: High-order ΔΣ ADC incorporating the VCO-based integrator and quantizer as the back-end stage.

In this work, a pseudo-differential-VCO based 2nd-order continuous-time ΔΣ ADC with a residue self-coupling technique is proposed and implemented with mostly digital circuits. Passive subtraction is realized in current domain to obtain the residue at the VCO input. Moreover, a highly linear VCO topology is presented.

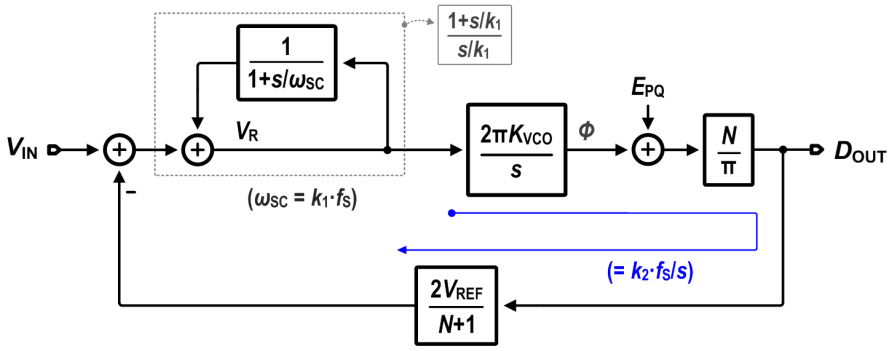
4.3.1 Proposed Architecture

Fig. 4.9(a) shows the proposed pseudo-differential-VCO based 2nd-order ΔΣ ADC architecture with a residue self-coupling technique. A pseudo-differential (PD)-VCO

based integrator and the phase quantizer are employed in the ΔΣ loop. The digital output is fed back through a DAC to generate the residue. The integral relationship of the VCO output phase to its input voltage enables a small residual signal swing at the VCO input. As a result, the VCO nonlinearity is mitigated. On the other hand, a local positive feedback path with a first-order low-pass transfer function is incorporated at the residue node. This residue self-coupling (RSC) operation forms an additional integrator (Fig. 4.9(b)). The overall architecture achieves 2nd-order noise shaping.



(a)



(b)

Figure 4.9: Proposed 2nd-order ΔΣ ADC architecture: (a) block diagram, and (b) linearized model.

The linearized model is shown in Fig. 4.9(b) to derive the coefficients. Assuming the transfer function of the VCO-based integrator and feedback DAC is represented as $k_2 f_S/s$, similar to (4.12), the K_{VCO} is then defined as

$$K_{VCO} = \frac{N+1}{N} \cdot \frac{k_2 f_S}{4V_{REF}} \tag{4.16}$$

The *s*-domain NTF (normalized to f_S) of the proposed ΔΣ ADC is derived as

$$NTF(s) = \frac{s^2}{s^2 + k_2 s + k_1 k_2} \tag{4.17}$$

While 2nd-order noise shaping is obtained in the proposed ΔΣ ADC architecture, the number of VCO delay cells and the oversampling ratio can be optimized to achieve the desired SQNR performance. For example, with a 15-stage VCO and an oversampling ratio of 30, an SQNR of 82dB can be achieved in a 10MHz signal bandwidth. Using the 'Delta-Sigma Toolbox' with a maximum NTF out-of-band gain of 2.5, the synthesized *z*-domain NTF is given by

$$NTF_{\text{syn}}(z) = \frac{(z-1)^2}{z^2 - 0.4676z + 0.1324} \tag{4.18}$$

Based on the impulse invariance transformation (corresponding to a rectangle DAC pulse shape) to the loop transfer function $L(z)$ (where $L(z) = 1/NTF_{\text{syn}}(z)\text{-}1$) [38], after design centering $k_1 = 0.554$ and $k_2 = 1.2$.

4.3.2 Behavioral-Model Simulations

Behavioral-model simulations are performed to quantify the effects of the non-idealities of building blocks in the proposed ΔΣ ADC architecture (Fig. 4.9). In the simulations, the nonlinearity coefficients of the VCO V-to-F transfer curve are obtained from the transistor-level simulation of the VCO used in this ΔΣ ADC. The simulated signal-to-quantization-noise-plus-distortion ratio (SQNDR) is plotted as a function of the gain error in the RSC path, as shown in Fig. 4.10(a). With a gain error of ±10% in the RSC path, the SQNDR degradation is less than 2dB. Fig. 4.10(b) depicts the SQNDR versus the relative variation in K_{VCO}. As K_{VCO} increases, the suppression to the in-band quantization noise is improved, therefore a better SQNDR is expected. As shown in Fig. 4.10(b), the SQNDR is still above 80dB with a relative variation of -20% in K_{VCO}.

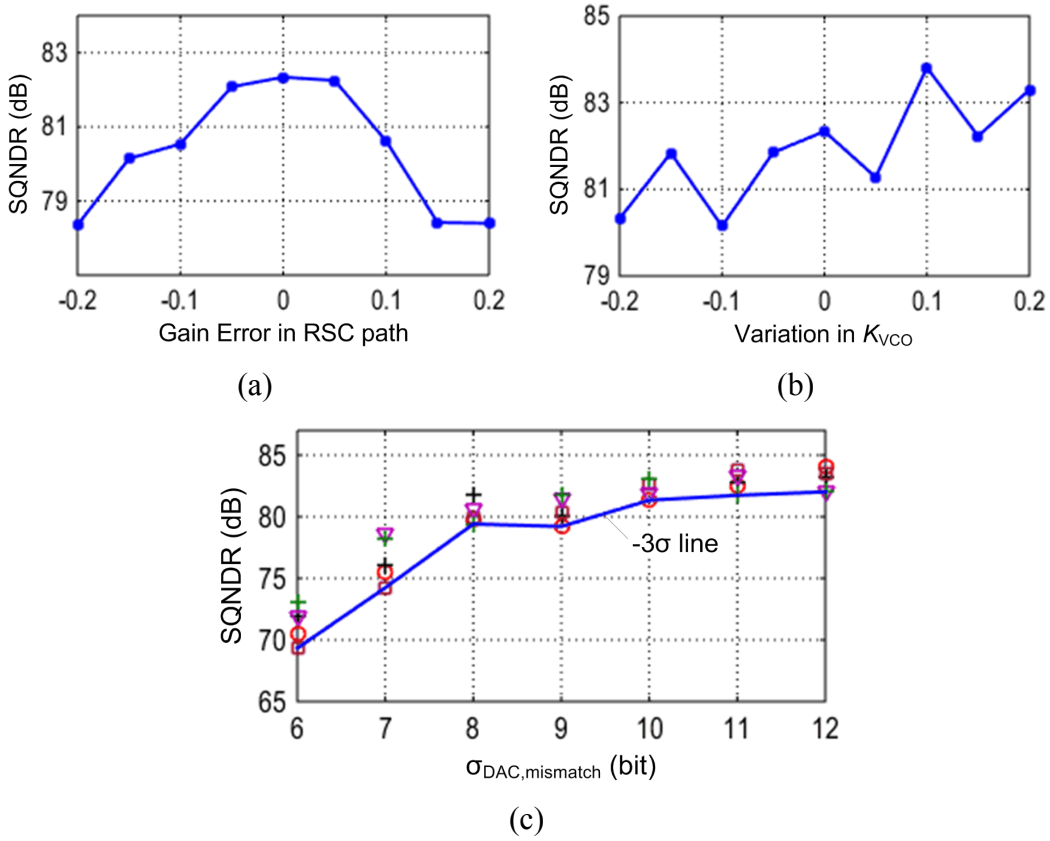


Figure 4.10: SQNDR of the ΔΣ ADC plotted versus: (a) gain error in the RSC path, (b) relative variation in K_{VCO}, and (c) standard deviation of DAC mismatch.

As illustrated in Fig. 4.6, the way of implementing the phase quantization results in a clock averaging capability to the digital output code that shapes the DAC mismatch errors. Therefore, the DAC matching requirement can be relaxed. The DAC elements selection pattern is modeled in the simulations. A plot of SQNDR versus the DAC mismatch, shown in Fig. 4.10(c), reveals that 9.5b 1-σ matching is needed to achieve a 3σ SQNDR of greater than 80dB.

4.4 Circuit Implementation

The circuit implementation details of the prototyped ΔΣ ADC will be described in this section. Design trade-offs are also discussed to optimize the performance.

4.4.1 ΔΣ Modulator

Fig. 4.11 shows the schematic diagram of the 2nd-order ΔΣ modulator operating at a sampling frequency of 600MHz. Two VCOs are arranged in a pseudo-differential manner. The output phase of each VCO is sampled by an array of sense amplifier flip-flops (SAFFs), introducing phase-domain quantization noise. The digital output is obtained by comparing the sampled phase of one VCO with that of the other using an array of XOR gates. Then the digital output is fed back through a current DAC to the input of the VCOs. To allow enough settling time for the phase quantizer (composed of SAFFs and XORs), a delay of about $0.1T_S$ is introduced between the sampling clock and the clock of feedback DAC. On the other hand, the residue self-coupled path is implemented using a 1st-order transconductance low-pass filter (TCLPF) whose transfer function is defined by

$$G_m(s) = \frac{(R_1 \,||\, R_2)^{-1}}{1 + s/\omega_{SC}} \tag{4.19}$$

The product of the transconductance at dc and the equivalent resistance at the residue node should be equal to one.

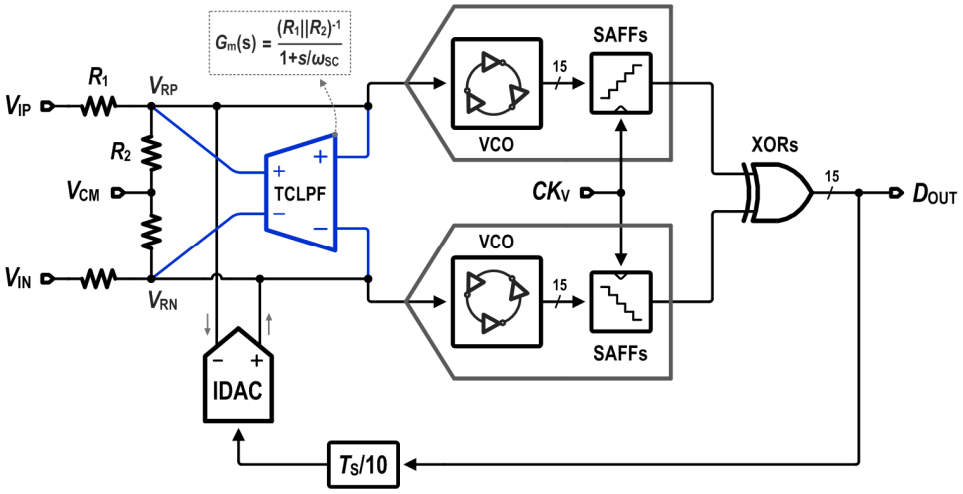


Figure 4.11: Schematic diagram of the 2nd-order ΔΣ modulator.

Passive resistors R_1 are used to perform the subtraction of the input signal path, feedback DAC path and the self-coupled TCLPF path in current domain. The voltage generated across R_1 by the output currents from the feedback DAC and the self-coupled

TCLPF is subtracted from the input voltage to generate the residues (i.e. V_{RP} and V_{RN}) at the two VCOs input. In addition, the resistor R_2 is added to realize a resistive divider that further decreases the signal swing at the residue nodes. Then the VCO V-to-F conversion gain (i.e. K_{VCO}) is designed to compensate for this scaling factor.

4.4.2 Linear VCO

The schematic of the linear VCO is shown in Fig. 4.12. The VCO is comprised of 15 stages of delay cells in a ring. Each delay cell is implemented using two main CMOS inverters and two small inverters cross-coupled between the differential output nodes. A new VCO input stage that connects between the input voltage V_I and the control terminal of the delay cells is proposed that is implemented by a resistor R_C along with a fixed current source (transistor M_0). In this way, it improves the linearity of the V-to-F transfer curve.

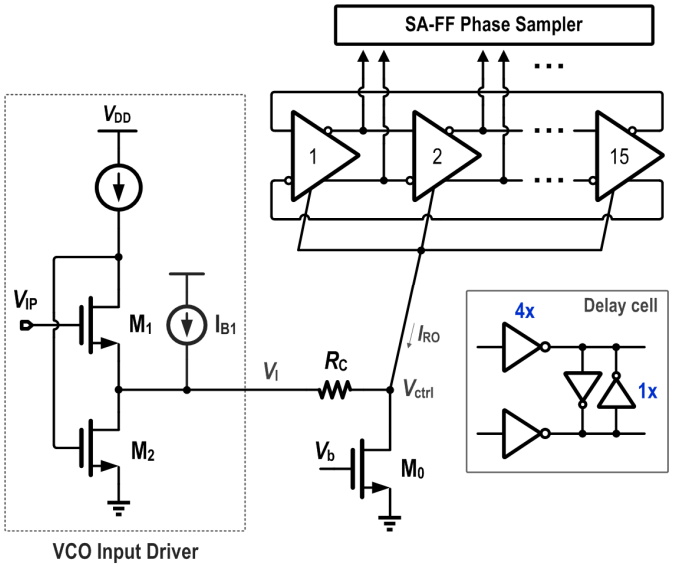


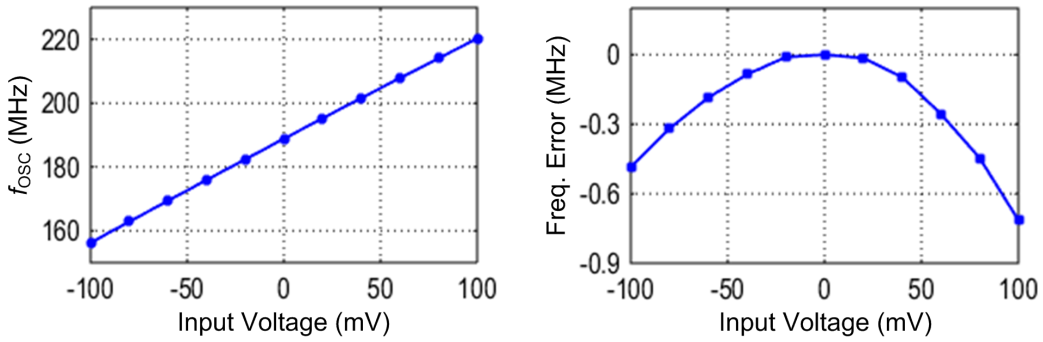
Figure 4.12: Schematic of the linear VCO.

The control current flowing into the ring oscillator is given by

$$I_{RO} = -\frac{V_I}{R_C} + \frac{V_{ctrl}}{R_C} + I_{M0} \tag{4.20}$$

where V_{ctrl} is the voltage at the control terminal of the delay cells. Similar to [39], the

transistor-level simulations show that the tuning curve of oscillation frequency versus the control current I_{RO} exhibits a negative curvature; the curve of V_{ctrl} against the input voltage V_I exhibits a positive curvature. According to (4.19), both nonlinear effects on the overall V-to-F transfer curve will get mitigated. As a result, the VCO linearity can be improved. Fig. 4.13 depicts simulated V-to-F transfer curve of the VCO. After deviating the V-to-F transfer curve from a best-fit line, the worst-case frequency error over the input voltage from -0.1V to 0.1V is -0.7MHz, corresponding to 1.1% of the full tuning range.



(a) (b)

Figure 4.13: (a) Simulated V-to-F transfer curve of the VCO, and (b) frequency error after deviating from a best-fit line.

To drive the resistive input stage of the VCO and provide a high input impedance, a self-coupled source follower [25] is employed as the VCO input driver. In addition, the current source I_{B1} connected at the driver output node provides the nominal current flowing through R_C under dc operation conditions.

Fig. 4.14 plots the simulated phase noise of the VCO, which is about -108dBc/Hz at a 1MHz frequency offset. According to (4.15), the calculated signal-to-phase-noise ratio is about 73dB, which is 8dB larger than the calculated SQNR from (4.14). It is clear that the VCO phase noise does not limit the overall ADC performance.

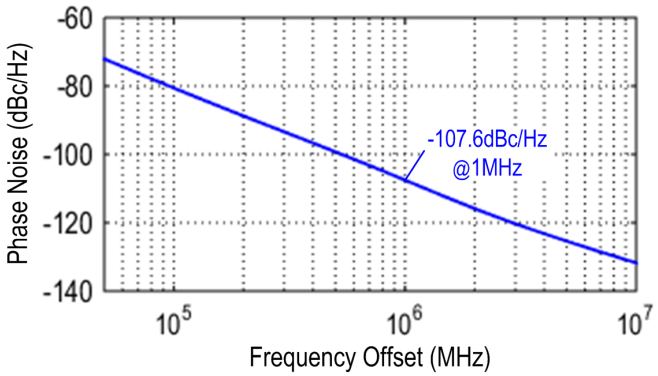


Figure 4.14: Simulated phase noise of the VCO.

4.4.3 Transconductance Low-Pass Filter

The schematic of the 1st-order TCLPF is shown in Fig. 4.15. A resistive source-degenerated transconductor topology with embedded local feedback is employed to achieve good linearity [15]. Transistors M_1 and M_2 form a negative feedback loop that largely reduces the equivalent resistance looking into the node at the source of M_1. As a result, the current flowing in the source degenerated resistor approximates to v_{id}/R_S (where v_{id} is the input differential voltage). This current is also equal to the small-signal current incremental in the transistor M_2, since the current of M_1 is unchanged.

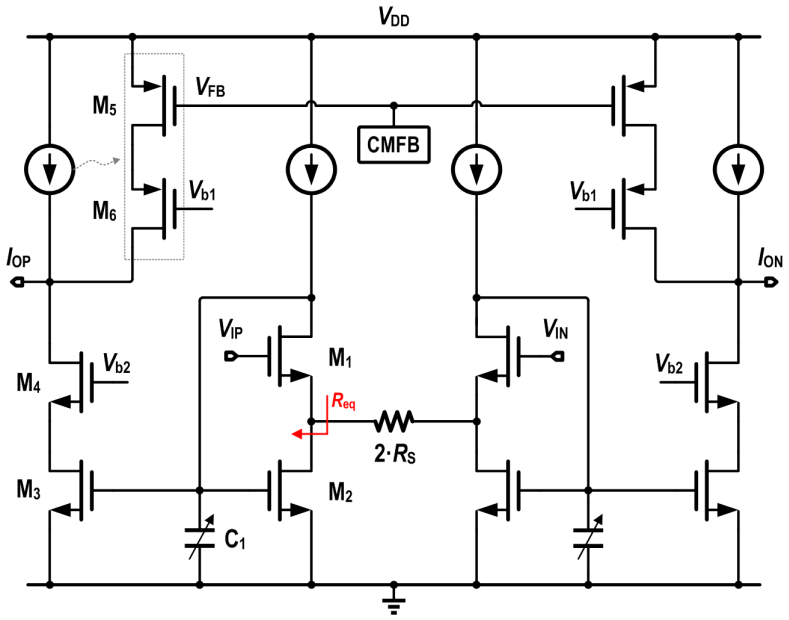


Figure 4.15: Schematic of the 1st-order TCLPF.

On the other hand, through the use of the current mirror M_2 and M_3, the linearized differential current (i.e. v_{id}/R_S) is copied to the output stage. In this way, the proposed transconductor achieves good linearity while drawing low current in each branch. The cascode structure is used in the output stage to provide high output resistance. A common-mode feedback (CMFB) circuit sets the output CM voltage by adjusting the voltage at node 'V_{FB}'.

The capacitor C_1 is placed at the gate of the current mirror M_2 and M_3 to result in a 1st-order low-pass transfer function. To derive the transfer function of the TCLPF, the small-signal half circuit of the first stage is shown in Fig. 4.16. The voltage incremental v_x at the gate of transistors M_2 and M_3 is given by

$$v_x = -\frac{v_{ip}}{g_{m2}R_S} \cdot \frac{1}{s\frac{C_1}{g_{m2}}\left(\frac{1}{g_{m1}R_S}+1\right)+1} \tag{3.21}$$

As illustrated, it has a pole whose frequency is approximately defined as g_{m2}/C_1. In this work, C_1 is adjustable to cover PVT variations.

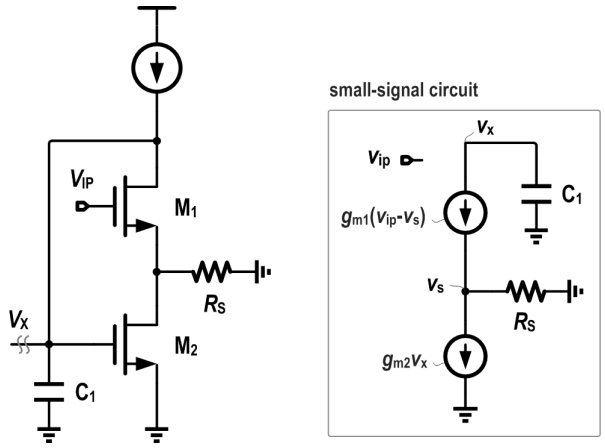


Figure 4.16: Small-signal half circuit of the first stage in the TCLPF.

4.4.4 Current DAC

The feedback DAC in the ΔΣ modulator is implemented using a non-return-to-zero (NRZ) topology. In contrast to a return-to-zero topology, an NRZ DAC is less sensitive to clock jitter but is more susceptible to inter-symbol interference (ISI). The unary

current steering architecture is used to achieve fast switching and reduce the distortion caused by ISI. To make the full scale of the feedback DAC equivalent to $\pm V_{\mathrm{REF}}$, the current in the DAC unit cell is determined by

$$I_{\mathrm{u,DAC}} = \frac{V_{\mathrm{REF}}}{2(N+1)R_{\mathrm{I}}} \tag{4.22}$$

Fig. 4.17 shows the schematic of the DAC unit current cell. The current source is cascoded to increase the output impedance, and the cascode transistor that is designed with 2× minimum channel length provides shielding from the switching node. Furthermore, voltage glitch at the drain of the cascode transistor is minimized by using input signals with high crossover point that are generated using cross-coupled NOR gate latches. The DAC current source transistors are sized to achieve better than 9.5-b matching in the DAC. To minimize the noise contribution, they are designed with a large overdrive voltage.

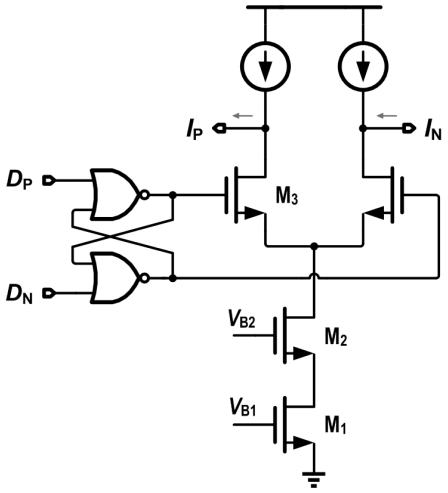


Figure 4.17: Schematic of the DAC unit current cell.

4.5 Simulation Results

The prototyped ΔΣ modulator is designed in a 65nm CMOS process. Operating with a 600MHz sampling frequency, the ΔΣ modulator consumes 2.9mW power, of which 1.6mW is consumed by the analog blocks (including TCLPF, DAC and VCO driver) and 1.3mW by the digital blocks. Among the digital blocks, the two VCOs consume

0.66mW from a 1.2V supply voltage. For a 1.2V_{pp} (-2.5dBFS) sinusoidal input signal at 2.894MHz with a 0.8V common-mode voltage, Fig. 4.18 shows the simulated (4096-point FFT) spectrum of the ΔΣ modulator with the TCLPF block powered off and on. The ΔΣ modulator achieves 78dB SNDR over a 10MHz bandwidth, which is 16dB improvement compared to the case with the TCLPF block powered off.

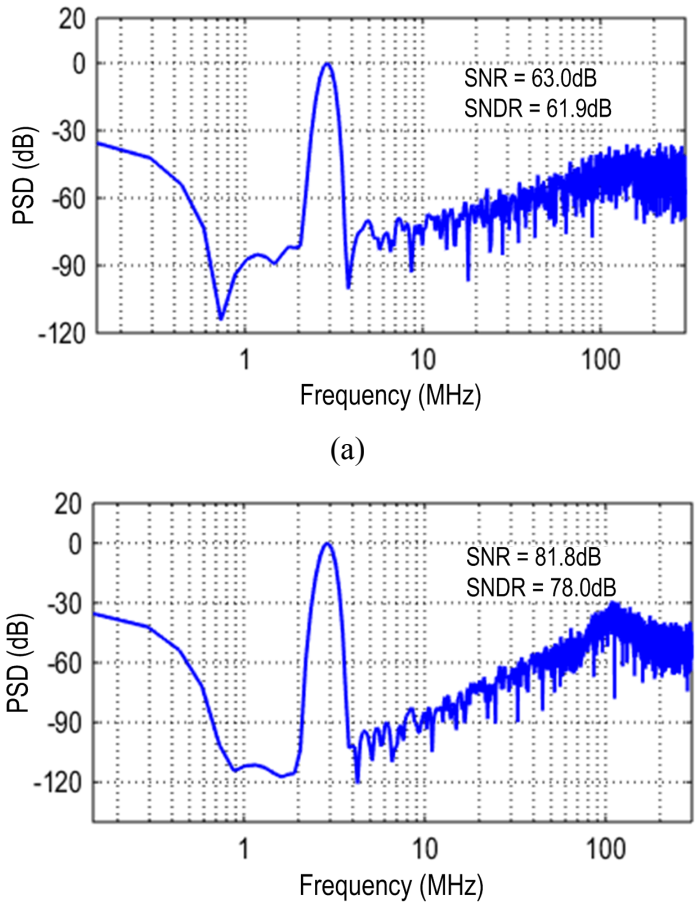


Figure 4.18: Simulated spectrum of the prototyped ΔΣ modulator with the TCLPF block powered (a) off and (b) on.

4.6 Summary

A pseudo-differential-VCO based continuous-time ΔΣ ADC with a residue self-coupling technique is presented and implemented with mostly digital circuits. Two VCOs are arranged in a pseudo-differential manner. The digital output is obtained by

comparing the sampled output phase of one VCO with that of the other. The digital output is fed back through a DAC, and passive subtraction is realized in current domain to obtain the residue at the VCO input. The residue self-coupling is implemented using a linear 1st-order transconductance low-pass filter. The transistor-level simulations in a 65nm CMOS process show a 78dB SNDR over a 10MHz signal bandwidth.

CHAPTER 5. CONCLUSIONS

The increasing popularity of portable electronics devices calls for a wireless receiver system with better sensitivity, more reconfigurability/programmability and decreasing power consumption. As the CMOS process scales down to submicron, reduced supply voltage and lower transistor intrinsic gain make it difficult to implement analog circuits in a power efficient manner. It has become advantageous to shift more analog signal processing functions conventionally realized in voltage (analog) domain into utilizing charge or time as the variable that can be processed by mostly digital/passive circuits. In this thesis, both circuit-level techniques and architectures are proposed that are inherently compatible with transistor scaling in submicron CMOS, meanwhile achieving state-of-the-art performance and optimizing power efficiency.

In Chapter 2, a highly reconfigurable charge-domain switched-g_m-C biquad band-pass filter (BPF) topology is presented that utilizes an interleaved semi-passive charge sharing technique. It uses only switches, capacitors, linearity-enhanced g_m-stages and digital circuitry for a 3-phase non-overlapping clock scheme. Flexible tunability in both center frequency and -3dB bandwidth is achieved with a scaling-compatible implementation. A 4^{th}-order BPF prototype operating at a 1.2GS/s sampling rate is designed with a cascade of two proposed biquads in a 65nm LPE CMOS process. The filter prototype consumes 7.5mW total power from a 1.2V supply voltage, and occupies a core area of 0.17mm^2. A tunable center frequency of 35−70MHz is measured with programmable bandwidth.

Chapter 3 presents a highly linear continuous-time low-pass filter (LPF) topology with source follower coupling that achieves excellent power efficiency. It synthesizes a 3^{rd}-order low-pass transfer function in a single stage using coupled source followers and three capacitors, and can be configured to 2^{nd}-order by disconnecting a capacitor. A 5^{th}-order Butterworth prototype is designed with a cascade of two proposed filter stages in a 0.18μm CMOS process, and occupies a core area of 0.12mm^2. Operating with a 1.3V supply voltage, the filter consumes only 0.5mA current, and achieves a -

3dB bandwidth of 20MHz and a dynamic range (at 1% THD) of 76.8dB.

A pseudo-differential-VCO based continuous-time ΔΣ ADC with a residue self-coupling technique is described in Chapter 4, which is implemented with mostly digital circuits while achieving excellent power efficiency. Two VCOs are arranged in a pseudo-differential manner. The digital output is obtained by comparing the sampled output phase of one VCO with that of the other. The digital output is fed back through a current-steering DAC, and passive subtraction is realized in current domain to obtain the residue at the VCO input. The residue self-coupling is implemented using a linear 1^{st}-order transconductance low-pass filter (TCLPF). The transistor-level simulations in a 65nm CMOS process show a 78dB SNDR over a 10MHz signal bandwidth.

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