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A fast-settling CMOS operational amplifier using the folded-cascode topology has been designed. The design is based on a theory developed by Yang et al for the optimum settling time of two-pole systems for switched-capacitor applications. The theory states that the two poles are separated by a given factor in order to obtain a minimum small-signal settling time. The design is achieved by performing a complete small-signal analysis to gain a better understanding of the frequency and time responses of the folded-cascode op-amp. SPICE simulation results are in good agreement with the theoretical predictions.

A Fast-Settling Folded-Cascode CMOS Operational Amplifier

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

A FAST-SETTLING FOLDED-CASCODE CMOS OPERATIONAL AMPLIFIER

1 INTRODUCTION

The electronic component known as the operational amplifier (op-amp) is a basic building block in analog systems. In the past before the development of integrated circuit technology, the operational amplifier was used primarily in analog computers to implement the mathematical operations of addition, integration and differentiation. However, in recent years, and after the progress that has been made in the monolithic circuit technology, a great number of op-amps may be fabricated on a single chip thus greatly reducing cost. Consequently, the range of applications has broadened enough to make the op-amp the most well-known device used in signal conditioning.

In one form, the op-amp consists of a differential input stage, a single-ended output stage, and has the following ideal characteristics [1] :

1) Infinite input impedance,
2) zero output impedance, and
3) infinite gain.

A schematic diagram of such an ideal op-amp is shown in figure 1. In practice, op-amps do not behave ideally,

but their performance can be approximated by the ideal op-amps.

In the past few years, the technology of metal-oxide-semiconductor (MOS) has been established as an efficient fabrication process. The MOS technology, when compared with the bipolar technology, is more desirable. The MOS technology uses relatively simple fabrication techniques, providing high-packing density and low power consumption. These features make the MOS technology attractive for large-scale integrated digital circuits. Recently, there was a need to use MOS technology in analog circuits where bipolar technology was previously dominating. This was necessary to realize analog-digital subsystems on the same integrated circuit using the same technology.

The performance of the MOS op-amp does not challenge that of the bipolar op-amp [2]. MOS op-amps have higher offset voltage, higher input noise, especially the 1/f component, and lower transconductance per stage. However, improvements in the control of the MOS process have lowered the offset voltage. Also, higher gain is obtained by using cascode stages, depletion load devices and the complementary MOS (CMOS) process.

CMOS op-amps can be implemented in different topologies. The two-stage topology shown in figure 2 [3] is widely used. The two-stage op-amp performance is well understood. It provides high voltage gain, wide output swing, high CMRR, and wide input common-mode range.

A second topology is the class-AB op-amp as shown in figure 3 [1]. The quiescent currents in the input transistors are determined by the bias voltages V_{B1} and V_{B2}. The class-AB op-amps do not show any slew-rate limiting since they can deliver to and source from a load, a current that is much larger than the quiescent current.

Another topology is the common-source common-gate or the folded-cascode op-amp shown in figure 4 [3]. It is a cascade of a common-source stage and a common-gate stage, whereas the two stage op-amp is a cascade of two common-source stages. The folded-cascode op-amp consists of a p-channel source-coupled pair M1 and M4 with the drains connected to the sources of the n-channel cascode devices M3 and M6. This technique is known as the current folding circuit technique [4]. The folded-cascode op-amp has a small-signal voltage gain comparable to that of the two-stage op-amp due to the cascode transistors at the output. One of the advantages of the folded-cascode topology is that the dominant pole is determined by the

load capacitance. Thus, no compensation capacitor needs to be added since the load and the compensation capacitors are the same. This leads to improved frequency response and to large phase margin (compared to a two-stage topology) since increasing the load capacitance reduces the bandwidth and increases the phase margin.

In this thesis, the folded-cascode topology is used to design a minimum settling time op-amp to be used in high-frequency switched-capacitor (SC) circuits, thus increasing the maximum operating frequency of SC filters and other SC circuits.

The settling time consists of two distinct periods [5]. The first is the slewing period which is determined by the amount of current available to charge or discharge the load capacitor. During that period, the op-amp behaves nonlinearly and the output makes the transition from the original output voltage to the vicinity of the new value. The second part is the settling period or the small-signal settling time. In this period, the op-amp behaves quasi-linearly and settles to the final value. The small-signal settling time is the significant part when working with SC circuits and will be thoroughly discussed in this thesis.

A simplified cross section of the silicon-gate 3-um n-well CMOS process used in this thesis is shown in figure 5.

The design is initiated by providing background material in chapter II.

Chapter III gives the frequency and time responses of the folded-cascode op-amp.

Chapter IV presents the small-signal settling behavior of the op-amp.

Chapter V describes the actual implementation of the design.

Chapter VI gives further improvements on the design.

Chapter VII provides summary and conclusions.

2 BASIC CIRCUITS ANALYSIS

2.1 Introduction

Although the folded-cascode op-amp is widely used, apparently it has never been fully analyzed. The architecture of the op-amp is complex, so to understand better the operation and the structure of the op-amp, some basic circuits which constitute the building blocks of the op-amp are analyzed. These circuits include :

1) Common-source amplifier with passive load.

2) Cascode common-source amplifier with passive load.

3) Cascode common-source amplifier with cascode active load.

The presentation includes small-signal analysis and computer verification.

2.2 Common-source amplifier with passive load (figure 6a.)

A. AC equivalent circuit

The AC equivalent circuit shown in figure 6b is obtained by [7] :

1) replacing all DC current sources with open circuits, and

2) replacing all DC voltage sources with short circuits.

B. Small-signal model

The small-signal model of a MOS transistor is shown in figure 7 [7]. Replacing the active device of the circuit in figure 6b with the small-signal model, the circuit becomes as shown in figure 8a. With $v_{bs}=0$, and with C_{gs} directly loading the input source, v_{in}, this circuit can be simplified as shown in figure 8b,

where

$$C = C_L + C_{db}, \tag{1}$$

$$g_L = g_{ds}, \tag{2}$$

and

$$g_{L\uparrow} = 1/R_L. \tag{3}$$

C. Transfer function

The voltage transfer function is obtained by applying Kirchoff's Current Law (KCL) at node 1 in figure 8b :

$$v_{out}[s(C_{gd1}+C)(g_{L\downarrow}+g_{L\uparrow})]+v_{in}(g_m-sC_{gd1}) = 0, \tag{4}$$

or

$$\frac{v_{out}}{v_{in}} = \frac{-(g_m-sC_{gd})}{s(C_{gd}+C)+g_{L\downarrow}+g_{L\uparrow}}. \tag{5}$$

As shown in figure 8c, the transfer function has a right-half plane (RHP) zero at a radian frequency of

$$W_z = \frac{g_m}{C_{gd}}, \tag{6}$$

and a left-half plane (LHP) pole at

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C+C_{gd}}, \tag{7}$$

or approximately,

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C_L}, \tag{8}$$

with $C_L >> C_{gd}+C_{db}$.

Equation (7) shows the fundamental principle that the pole frequency at a node is determined by the inverse of the RC product at that node, or

$$\text{LHP pole} = \frac{g_{out}}{C_{out}} = \frac{1}{r_{out}C_{out}}. \tag{9}$$

The small-signal low-frequency voltage gain, a_o, is obtained from equation (5) with s --→ 0, and is given by:

$$a_o = \frac{-g_m}{g_{L\downarrow}+g_{L\uparrow}}. \tag{10}$$

D. Computer simulation

The circuit of figure 8a was simulated using SPICE2 [8] with the resulting frequency response shown in figure 9.

E. Summary of results

Table 1a shows a comparison between hand analysis and SPICE results. As shown, the error percentages are very small, indicating that hand calculations are in good agreement with SPICE results.

2.3 Cascode common-source amplifier with passive load (figure 10a.)

Following the same procedure as in section 2.2, the simplified small-signal model of the amplifier is shown in figure 10b,

where

$$C_1 = C_{db2}+C_{gd2}+C_L, \tag{11}$$

and

$$C_2 = C_{db1}+C_{gs2}+C_{bs2}. \tag{12}$$

Applying KCL at nodes 1 and 2, the following voltage transfer function is obtained :

$$\frac{v_{out}}{v_{in}} = \frac{-g_{s2}(g_{m1}-sC_{gd1})}{As^2+Bs+D}, \tag{13}$$

where

$$A = C_2(C_1+C_{gd1}), \tag{14}$$

$$B = (C_{gd1}+C_1)(g_{ds2}+g_{L\uparrow})+C_2(g_{s2}+g_{ds1}-g_{ds2}g_{s2}), \tag{15}$$

$$D = (g_{ds2}+g_{L\uparrow})(g_{s2}+g_{ds1}-g_{ds2}g_{s2}), \tag{16}$$

and

$$g_{s2} = g_{m2}+g_{mbs2}+g_{ds2}. \tag{17}$$

$G_{L\downarrow}$ and $g_{L\uparrow}$ are the conductances at the output node and are given by:

$$g_{L\downarrow} = \frac{g_{ds1}g_{ds2}}{g_{s2}+g_{ds1}}, \tag{18}$$

and

$$g_{L\uparrow} = 1/R_L. \tag{19}$$

The transfer function shows a RHP zero given by :

$$W_z = \frac{g_{m1}}{C_{gd1}}, \tag{20}$$

and using the results from section 2.2, the two LHP poles are :

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C_1}, \tag{21}$$

or

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C_L}, \tag{22}$$

for

$$C_L >> C_{db2}+C_{gd2},$$

and

$$W_2 = \frac{-(g_{s2}+g_{ds1})}{C_2}, \tag{23}$$

or

$$W_2 = \frac{-g_{m2}}{C_2}, \tag{24}$$

for

$g_{m2} >> g_{ds1}+g_{mbs2}+g_{ds2}$.

The $g_{L\downarrow}$ expression is obtained by carrying-out the following derivation : The small-signal model of the cascode devices is shown in figure 10c. Applying KCL at nodes 1 and 2, the following equations are obtained :

$$v_s = \frac{i}{g_{ds1}}, \tag{25}$$

and

$$i = g_{ds2}v_{out} - g_{s2}v_s. \tag{26}$$

Substituting equation (25) into (26),

$$g_{L\downarrow} = \frac{i}{v_{out}} = \frac{g_{ds1}g_{ds2}}{g_{s2}+g_{ds2}+g_{ds1}}. \tag{27}$$

The small-signal low frequency voltage gain is given by :

$$a_o = \frac{- g_{m1}g_{s2}}{(g_{L\downarrow}+g_{L\uparrow})(g_{s2}+g_{ds1}-g_{ds2}g_{s2})}, \tag{28}$$

or

$$a_o = \frac{- g_{m1}}{g_{L\downarrow}+g_{L\uparrow}}, \tag{29}$$

for $g_{s2} >> g_{ds1}-g_{ds2}g_{s2}$.

The frequency response of the amplifier obtained by computer simulation is shown in figure 11. Also, table 1b shows a comparison between hand analysis and SPICE results. As shown, the error percentages are small,

indicating that hand calculations are in good agreement with SPICE results.

2.4 Cascode common-source amplifier with cascode active load (figure 12a.)

Using nodal analysis, the voltage transfer function of the cascode common-source circuit in figure 12b is :

$$\frac{v_{out}}{v_{in}} = \frac{-\,g_{s2}(g_{s3}+sC_3+g_{ds4})(g_{m1}-sC_{gd1})}{K_1s^3+K_2s^2+K_3s+K_4}, \tag{30}$$

where

$$K_1 = (C_1+C_{gd1})C_2C_3, \tag{31}$$

$$K_2 = C_3(C_{gd1}+C_1)g_{ds2}+C_3C_2(2g_{s2}+g_{ds1}) +C_2(C_{dg1}+C_1)(g_{s3}+g_{ds4}), \tag{32}$$

$$K_3 = g_{s2}(g_{s3}+2g_{ds2})C_3+g_{ds2}(g_{s3}+g_{ds4})(C_{gd1}+C_1) +g_{ds2}(2g_{s2}+g_{ds1})C_3, \tag{33}$$

and

$$K_4 = g_{ds2}(g_{s3}+g_{ds4})(2g_{s2}+g_{ds1})+g_{ds3}g_{s3}g_{s2} -g_{s2}(g_{ds3}+2g_{ds2})(g_{s3}+g_{ds4}). \tag{34}$$

As expected, the transfer function has three LHP poles, with one pole at each node :

$$W_1 = \frac{-\,g_{L\downarrow}+g_{L\uparrow}}{C_1}, \tag{35}$$

$$W_2 = \frac{-\,g_{s2}+g_{ds1}}{C_2}, \tag{36}$$

$$W_3 = \frac{-\,g_{s3}+g_{ds4}}{C_3}, \tag{37}$$

and a RHP zero :

$$W_{z1} = \frac{g_{m1}}{C_{gd1}}, \tag{38}$$

and a LHP zero :

$$W_{z2} = \frac{-(g_{s3}+g_{ds4})}{C_3}. \tag{39}$$

As shown in figure 12c, there is (fortunately) a pole-zero cancellation;

$$W_{z2} = W_3. \tag{40}$$

Using the results from the previous sections, the small-signal gain can be approximated by :

$$a_o = \frac{-g_{m1}}{g_{L\downarrow}+g_{L\uparrow}}, \tag{41}$$

where

$$g_{L\downarrow} = \frac{g_{ds1}g_{ds2}}{g_{s2}+g_{ds1}}, \tag{42}$$

and

$$g_{L\uparrow} = \frac{g_{ds3}g_{ds4}}{g_{s3}+g_{ds4}}. \tag{43}$$

The frequency response of the amplifier is shown in figure 13. Also, table 1c shows a comparison between hand analysis and SPICE results. As shown, the error percentages are small, indicating that hand calculations are in good agreement with SPICE results.

3 FREQUENCY AND STEP RESPONSES

The folded-cascode op-amp has been used in a wide range of applications, mainly high-frequency SC circuits. One advantage of this op-amp, as mentioned before, is that the dominant pole is contributed by the load capacitor. Thus, no compensation capacitor is needed providing a good phase margin and a fast settling time [9].

In this chapter, the folded-cascode op-amp is analyzed. The small-signal analysis is necessary to realize expressions for the most dominant poles and to develop an optimum two-pole model. Then applying the theory developed in [10], an optimum design is realized to obtain small-signal settling time for a given load capacitance.

The op-amp shown in figure 14 is computer simulated to obtain the frequency response which shows that the op-amp has two poles and a pole-zero doublet (a doublet occurs when a pole and a zero do not cancel exactly) as shown in figure 15. The doublet is located far from the unity-gain frequency so it has a negligible effect on the transfer function. The op-amp can then be well-approximated by a simple two-pole model. The open-loop

transfer function of the model for small-signal analysis can be approximated by a second-order system,

$$a(s) = \frac{a_o}{(1+s/W_1)(1+s/W_2)}, \tag{44}$$

where a_o is the DC gain of the op-amp, W_1 and W_2 are the frequencies of the LHP poles.

To determine W_1 and W_2, the cascode common-source circuit in figure 12a is used. The frequency responses of both circuits 12a and 14 are shown in figure 16. As shown, except at very high frequencies not of interest, the phase responses are in good agreement with each other (the unity-gain phase margins of the op-amp and the cascode common-source amplifier are 87.6^o and 87.4^o respectively.) For the magnitude responses, the response of the op-amp is shifted down because it has a lower DC gain. However, the locations of the poles will not be affected. Then, the frequency response of the op-amp can be well-approximated by that of the cascode common-source amplifier in figure 12a. Thus W_1 and W_2 can be determined by the equations derived in chapter 2 :

$$W_2 = \frac{-(g_{s3}+g_{ds1}+g_{ds2})}{C_2}, \tag{45}$$

or

$$W_2 = \frac{-g_{s3}}{C_2}, \tag{46}$$

for

$$g_{s3} >> g_{ds1}+g_{ds2},$$

and

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C_1}, \tag{47}$$

or

$$W_1 = \frac{-(g_{L\downarrow}+g_{L\uparrow})}{C_L}, \tag{48}$$

for

$$C_L >> C_{db3}+C_{gd3}+C_{db8}+C_{gd8},$$

where

$$C_2 = C_{gd1}+C_{gs1}+C_{gb1}+C_{db1}+C_{gd2}+C_{db2}+C_{gs3}+C_{bs3}, \tag{49}$$

$$C_1 = C_L+C_{gd3}+C_{db3}+C_{gd8}+C_{db8}, \tag{50}$$

$$g_{L\uparrow} = \frac{g_{ds10}\ g_{ds8}}{g_{ds10}+g_{s8}}, \tag{51}$$

and

$$g_{L\downarrow} = \frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{ds1}+g_{ds2}+g_{s3}}. \tag{52}$$

The transfer function in the unity-gain closed-loop configuration (figure 17) is given by :

$$A(s) = \frac{A_o}{(s/W_o)^2+2k(s/W_o)+1}, \tag{53}$$

where

$$A_o = \frac{a_o}{1+a_o}, \tag{54}$$

$$W_o = (W_1W_2(1+a_o))^{1/2}, \tag{55}$$

and k, the damping factor, is given by :

$$k = \frac{W_1+W_2}{2W_o}. \tag{56}$$

Defining the pole separation factor as

$$\beta = W_2/W_1, \tag{57}$$

equation (56) becomes :

$$k = \frac{1+\beta}{2((1+a_o))^{1/2}}. \tag{58}$$

It is well-stated [11] that the second-order system possessing two poles in the LHP has three possible responses to a step input. Each response is directly related to the damping factor k. Equation (53) is solved for the inverse Laplace transform to obtain the following analytical expressions for the normalized responses [10] :

1) k > 1, overdamped (exponentially approaching the steady-state value):

$$v_o(t) = 1 - \frac{1}{2(k^2-1)^{1/2}} [1/k_1 \exp(-k_1 W_o t) - 1/k_2 \exp(-k_2 W_o t)], \tag{59}$$

where

$$k_1 = k - (k^2 - 1)^{1/2}, \tag{60}$$

and

$$k_2 = k + (k^2 - 1)^{1/2}. \tag{61}$$

2) k = 1, critically damped (exponentially approaching the steady-state value):

$$v_o(t) = 1 - (1+W_o t)\exp(-W_o t). \qquad (62)$$

3) $k < 1$, underdamped (overshoot followed by damped response) :

$$v_o(t) = 1 - [k/(1-k^2)^{1/2} \sin((1-k^2)^{1/2} W_o t) + \cos((1-k^2)^{1/2} W_o t)]\exp(-kW_o t). \qquad (63)$$

4 SETTLING BEHAVIOR

Settling time is a very important characteristic in analog sampled-data system applications, especially in high-frequency SC circuits. The settling time affects the speed of analog signal processing, since the amplifier has to settle within a predetermined error bound of the final value of the applied signal to avoid errors in processing that signal. Thus the settling time, t_s, can be defined [12] as the time required for the output voltage to settle within a specified input step excitation region as shown in figure 18.

The minimum settling time is obtained when the system response is underdamped. This is illustrated in figure 19. As shown, the overdamped response takes longer time to rise and intersect the lower error bound. In the case of the underdamped response, the minimum settling time is obtained when the first peak of the response just intersects the upper error bound. The position of the first peak is obtained by differentiating equation (63) with respect to $W_o t$, and the derivative is set equal to zero. The first peak is found to occur at

$$W_o t = \frac{\pi}{(1-k^2)^{1/2}}. \qquad (64)$$

The value of the first peak is obtained when equation (64) is substituted into (63),

$$v_o = 1+\exp(-k\,\pi/(1-k^2)^{1/2}). \tag{65}$$

Setting that value equal to the upper error bound, 1+D, equation (65) becomes :

$$1+D = 1+\exp(-k\,\pi/(1-k^2)^{1/2}). \tag{66}$$

Substituting equation (58) into (66) gives [10] :

$$\beta = \frac{4\ (1+a_o)}{1+(\pi/\ln\ D)^2}, \tag{67}$$

where β is the pole separation factor.

5 ACTUAL IMPLEMENTATION

The frequency and time responses of the folded-cascode op-amp are now well understood. The theory established in [10] is applicable to the folded-cascode op-amp after it was well-approximated by a two-pole system. The theory states that for any two-pole system, a minimum settling time is obtained when the two poles are separated such that equation (67) is satisfied for given a_o and D, or

$$W_2 = \beta W_1, \tag{68}$$

or equivalently from equations (46) and (48),

$$\frac{g_{s3}}{C_2} = \frac{(g_{L\downarrow}+g_{L\uparrow})}{C_L}. \tag{69}$$

The folded-cascode topology is used to design an op-amp optimized for a given specific load capacitor value to obtain a minimum small-signal settling time. The biasing currents and device sizes are determined by satisfying equation (69) for a given load capacitance (C_L = 5 pF). The circuit schematic and device sizes are shown in figure 20 and table 2 respectively.

It is clearly evident from the previous analysis that the small-signal settling time of the op-amp is a strong function of the load capacitance. This is demonstrated by the graph in figure 21. The graph is

obtained by applying a small-signal step (20 mV) to the op-amp in the unity-gain configuration. Also, it is clearly evident from the graph that increasing or decreasing C_L beyond the optimum value (C_L = 5 pF) would slow the response speed of the op-amp. This is in agreement with the discussion in chapter 4 about the settling time and the type of response. The minimum settling time occurs when the response is underdamped and the first peak of the response just intersects the upper error bound.

6 FURTHER IMPROVEMENT

The type of layout technique has a significant effect on the small-signal settling time and the load capacitance plot. This can be easily observed when equation (69) is rewritten as :

$$C_L = \frac{(g_{L\downarrow}+g_{L\uparrow})C_2}{g_{s3}}, \tag{70}$$

where C_2 is the parasitic capacitance at node 2. C_2 depends among other things on the layout technique. The plot in figure 21 was obtained by assuming the typical rectangular layout shown in figure 22. By selecting a layout technique that reduces C_2, the plot can be shifted to the right, driving larger load, thus further improving the previous optimized design. One technique is the horseshoe layout shown in figure 23. Transistors M1, M2, and M3 are laid out using that technique. C_2 was reduced by 5%, indicating that some improvement on the plot is possible.

7 CONCLUSION

The small-signal analysis of the folded-cascode operational amplifier is complete. The op-amp possessed several poles and zeros but an optimum two-pole model was realized representing the two most dominant left-half-plane poles. Using this model, a fast settling op-amp, to be used in high-frequency switched-capacitor circuits, was designed. The design was based on a simple relationship that specifies the separation between the two poles. By satisfying that relationship, a minimum small-signal time is obtained for an optimum load capacitance (C_L = 5 pF). The specifications of the optimized op-amp are shown in table 3.

Parameter	SPICE Results	Hand Calculation	Error Percentage
a_o	-35.91	-35.89	0.06
f_p	38.02E3 Hz	37.97E3 Hz	0.13
f_z	97.72E7 Hz	98.89E7 Hz	1.20

(a)

Parameter	SPICE Results	Hand Calculation	Error Percentage
a_o	-38.08	-39.05	2.55
f_{p1}	31.80E3 Hz	32.98E3 Hz	3.71
f_{p2}	32.50E6 Hz	33.60E6 Hz	3.38
f_z	96.72E7 Hz	90.16E7 Hz	6.78

(b)

Parameter	SPICE Results	Hand Calculation	Error Percentage
a_o	-33.74E3	-34.07E3	0.98
f_{p1}	34.67 Hz	33.66 Hz	2.91
f_{p2}	30.60E6 Hz	31.70E6 Hz	3.60
f_z	90.10E7 Hz	85.01E7 Hz	5.55

(c)

Table 1 A comparison between hand calculation and SPICE results for the (a) common-source amplifier, (b) cascode common-source amplifier with passive load, (c) cascode common-source amplifier with cascode active load.

M1	280/6	M10	280/6
M2	280/10	M11	280/6
M3	140/10	M12	279/10
M4	280/6	M13	558/10
M5	280/10	M14	1645/6
M6	140/10	M15	140/10
M7	280/6	M16	95/6
M8	280/6	M17	410/6
M9	280/6	M18	63/10

Table 2 The optimized folded-cascode operational amplifier device sizes (um.)

AC gain	71.6 dB
Load capacitance	5 pF
Unity-gain bandwidth	8 MHz
Phase margin	69 ^{o}
Gain margin	40 dB
Slew rate	18 V/uS
Settling time	41 nS
DC offset voltage	1 mV
Power dissipation	8.85 mW
Power Supplies	± 5 V

Table 3 The optimized folded-cascode operational amplifier specifications.

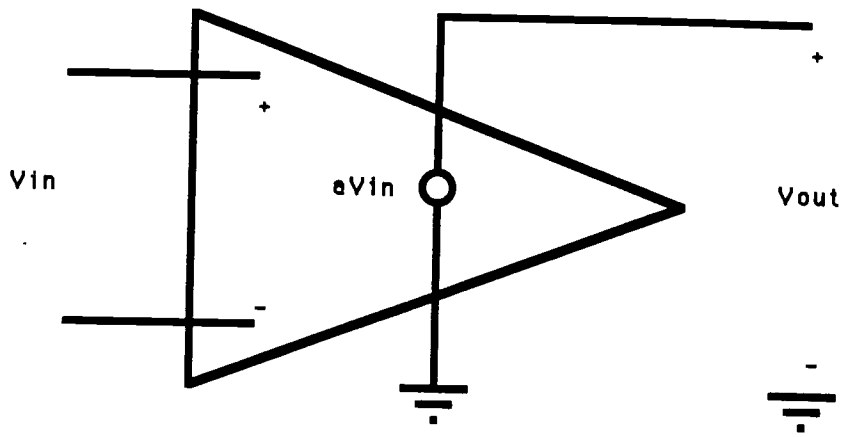


Fig. 1 An ideal operational amplifier schematic diagram.

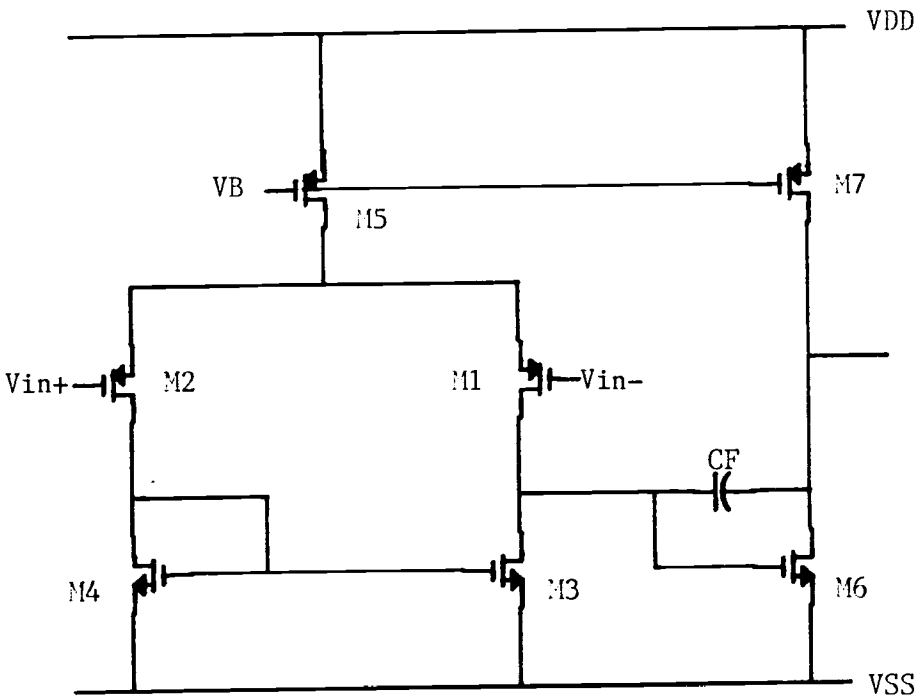


Fig. 2 A two-stage CMOS operational amplifier.

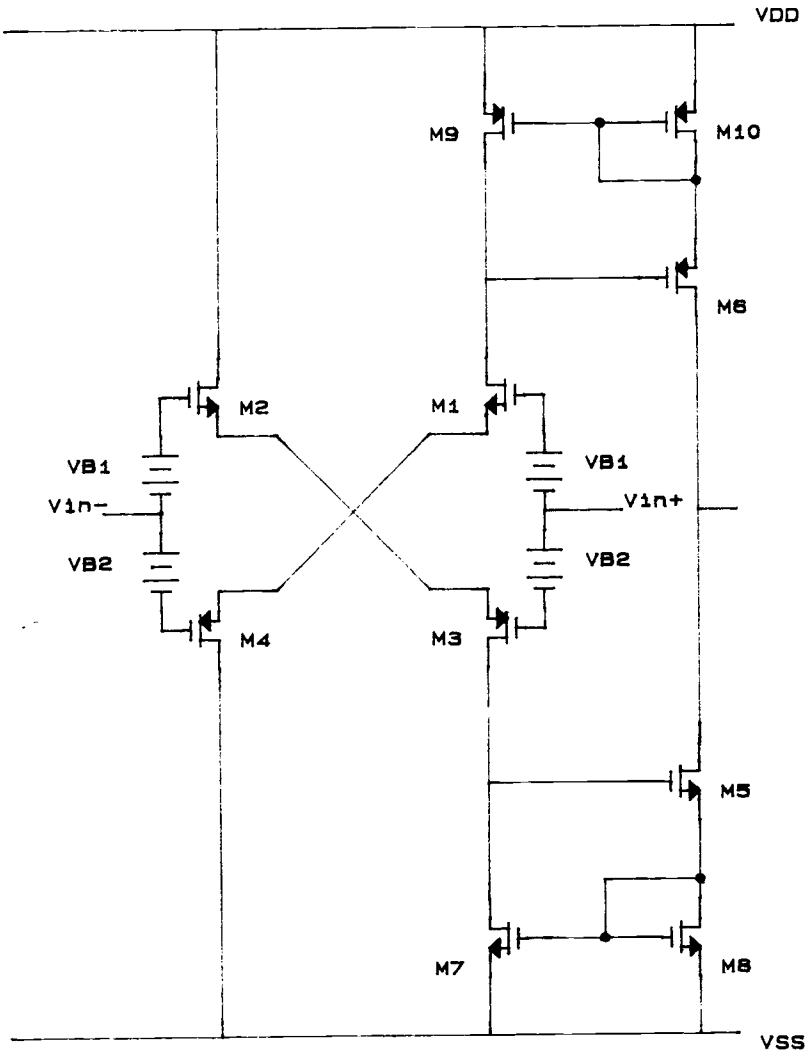


Fig. 3 A class-AB CMOS operational amplifier.

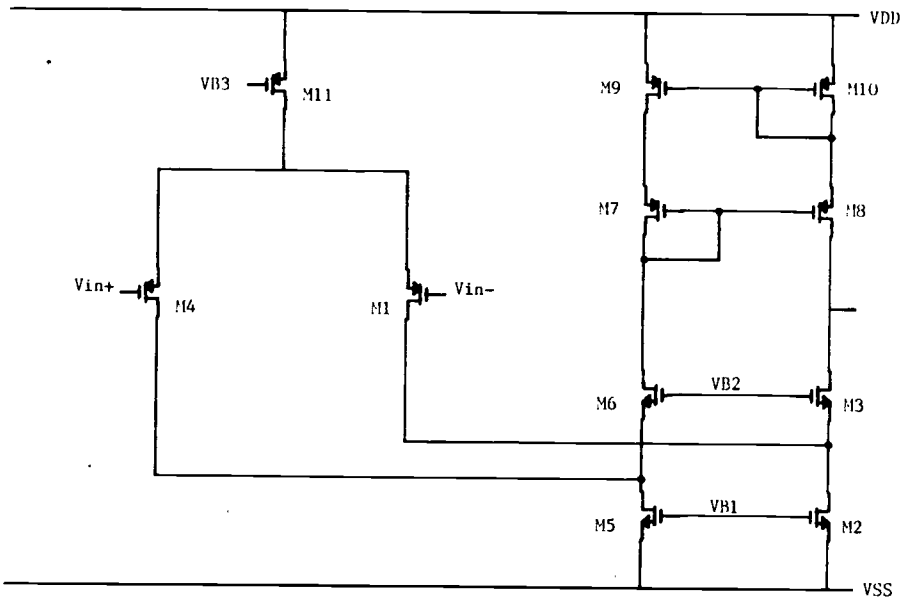


Fig. 4 A folded-cascode CMOS operational amplifier.

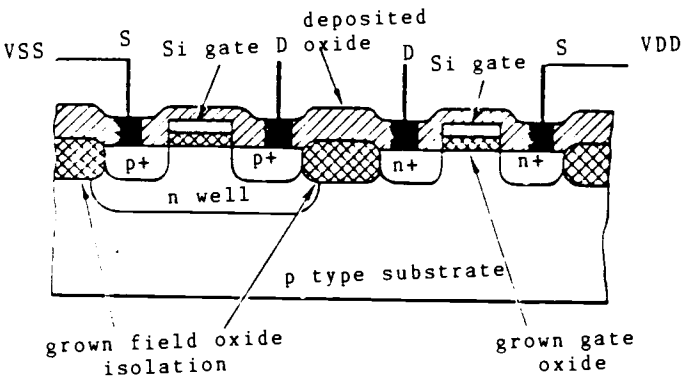
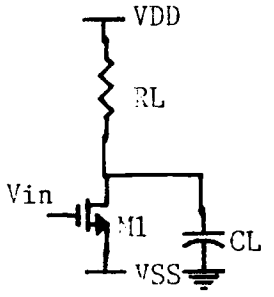
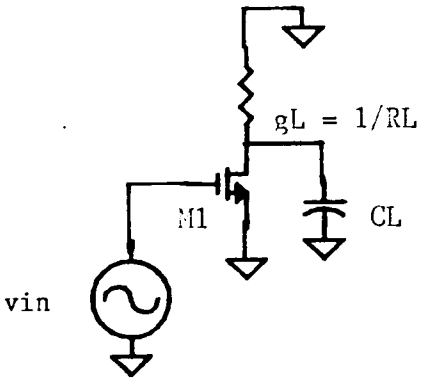


Fig. 5 A cross section of an n-well CMOS process [6].



(a)



(b)

Fig. 6 (a) A common-source amplifier with passive load, (b) The AC equivalent circuit of the amplifier.

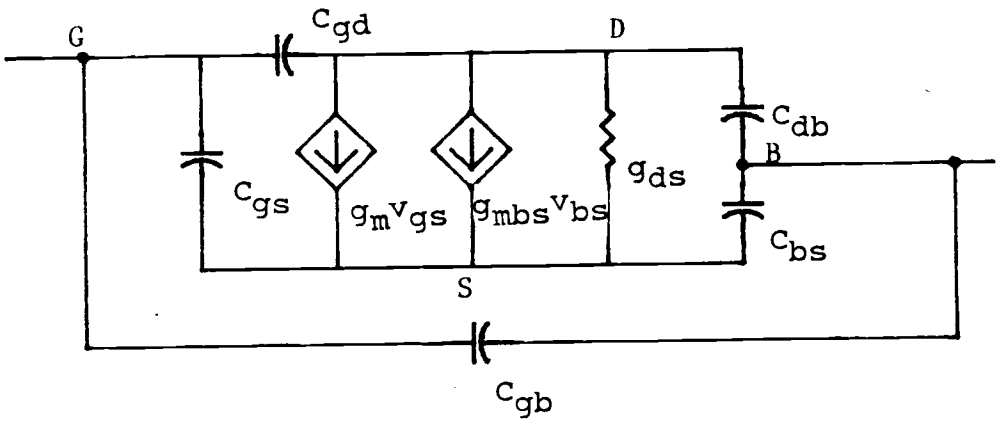


Fig. 7 The small-signal model of a MOS transistor.

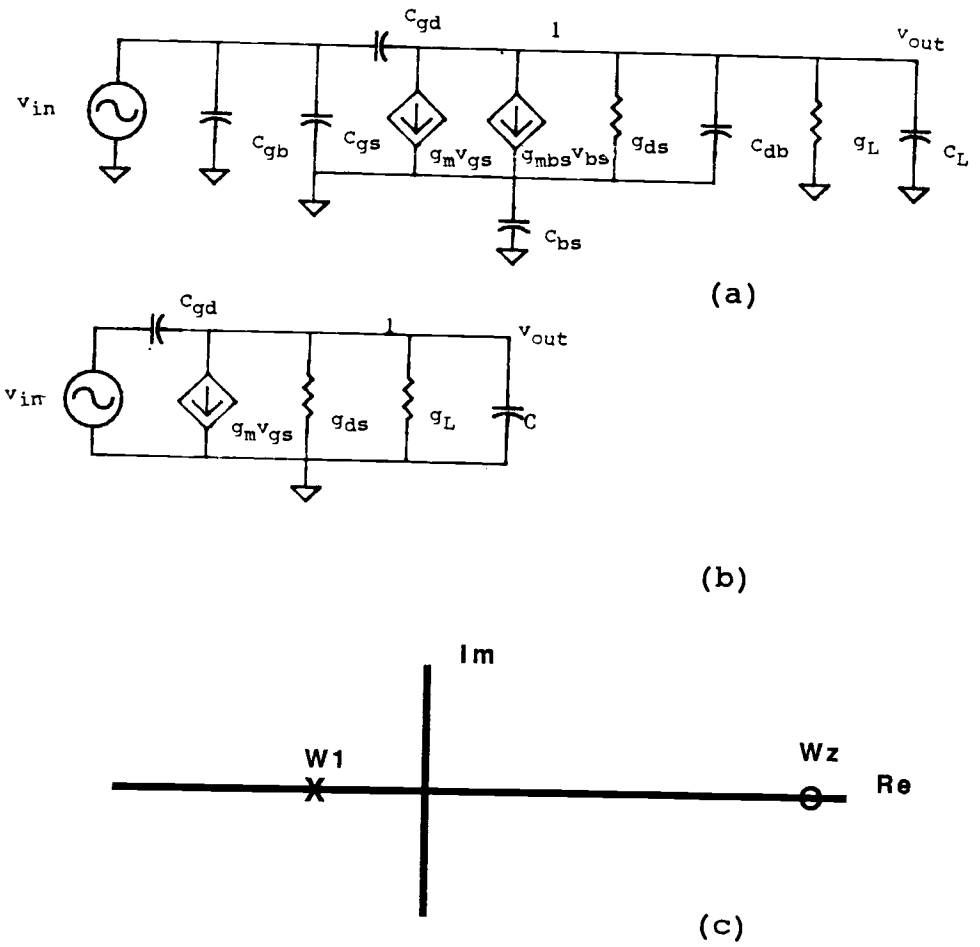


Fig. 8 (a) The small-signal model of the amplifier in fig. 6a; (b) a simplified model; (c) the pole-zero locations of the amplifier.

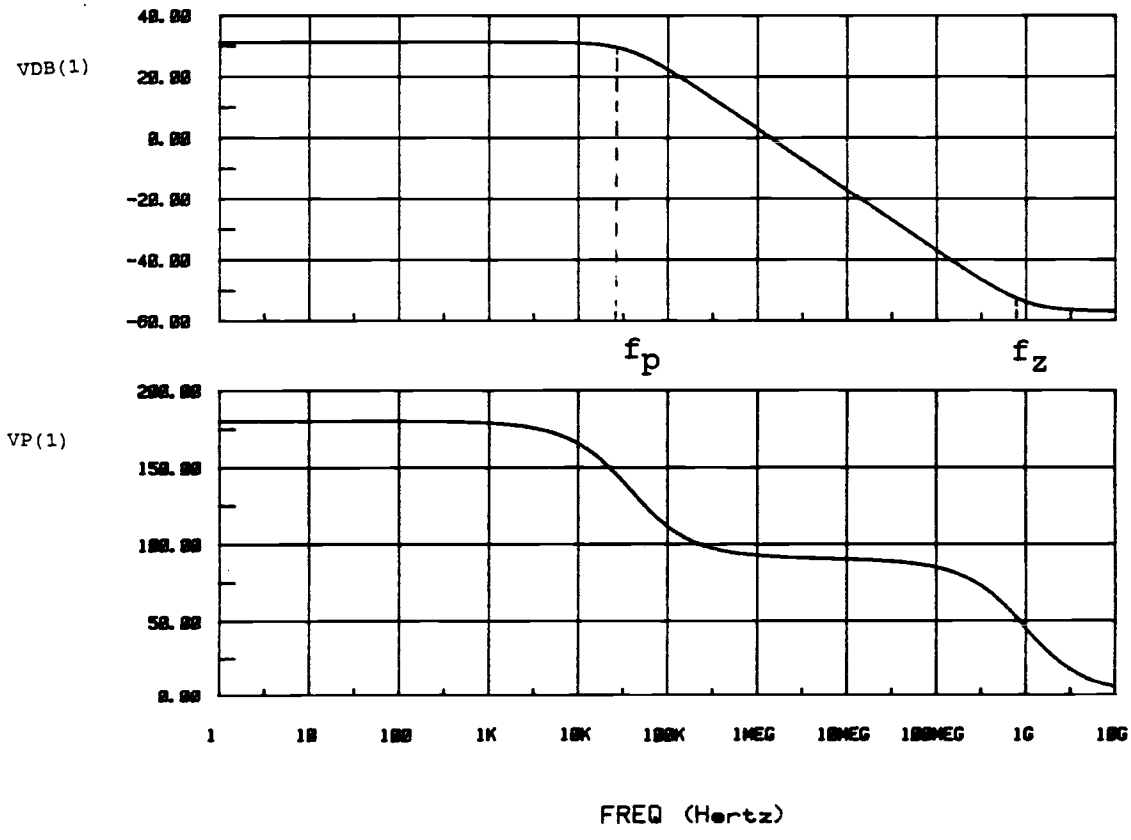
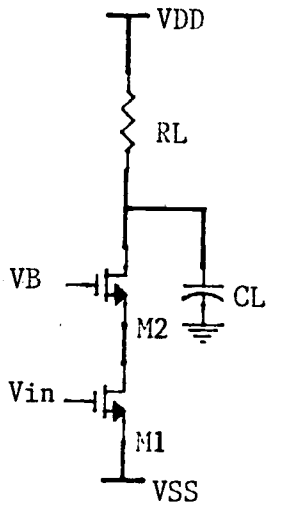
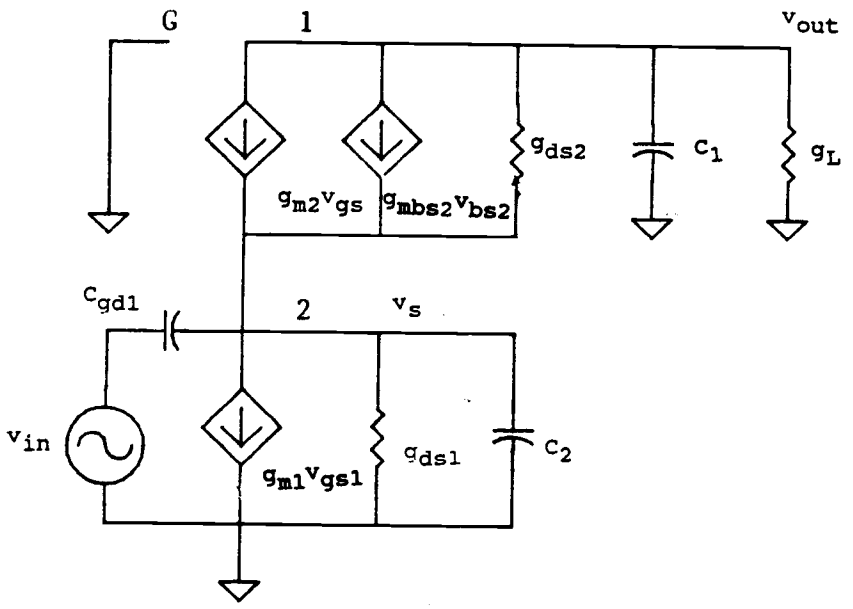


Fig. 9 The simulated frequency response of the amplifier in fig. 6a.

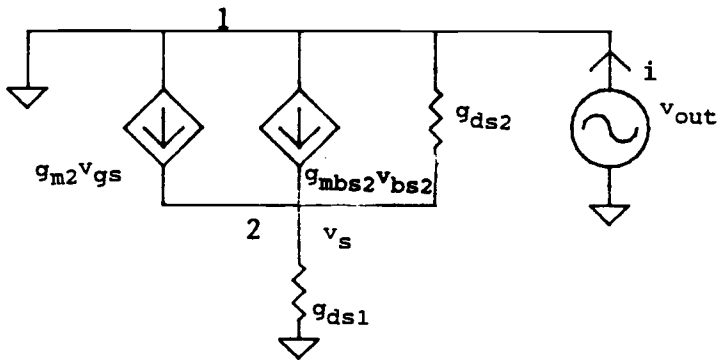


(a)



(b)

Fig. 10 (a) A cascode common-source amplifier with passive load, (b) the small-signal model of the amplifier.



(c)

Fig. 10 A (c) The small-signal model of the cascode transistors, M1, M2.

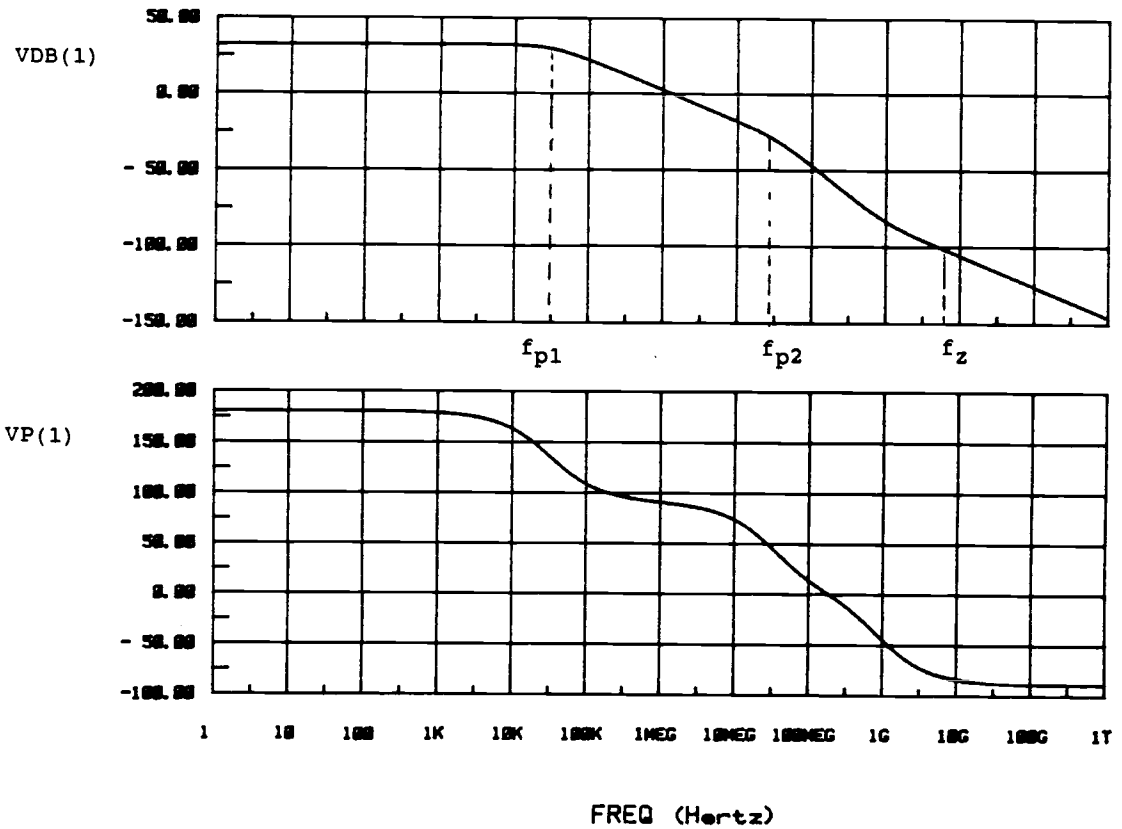
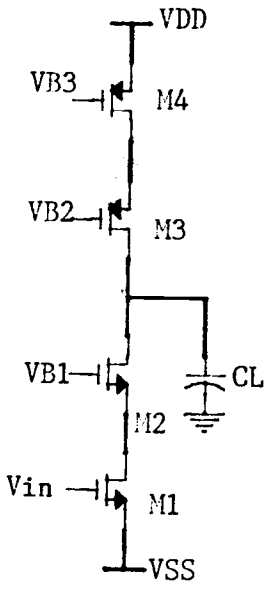


Fig. 11 The simulated frequency response of the amplifier in fig. 10a.



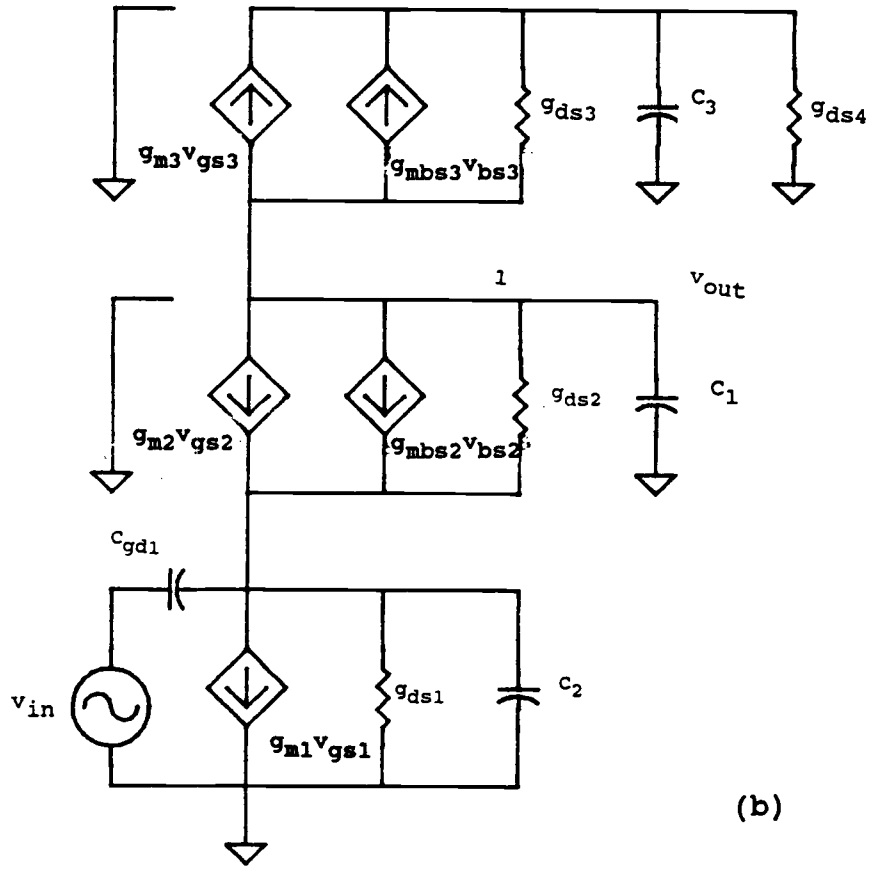
(a)

Fig. 12 (a) A cascode common-source amplifier with cascode active load.

$$C1 = CL + Cgd2 + Cdb2 + Cgd3 + Cdb3$$

$$C2 = Cdb1 + Cbs2 + Cgs2$$

$$C3 = Cgs3 + Cbs3 + Cgd4 + Cdb4$$



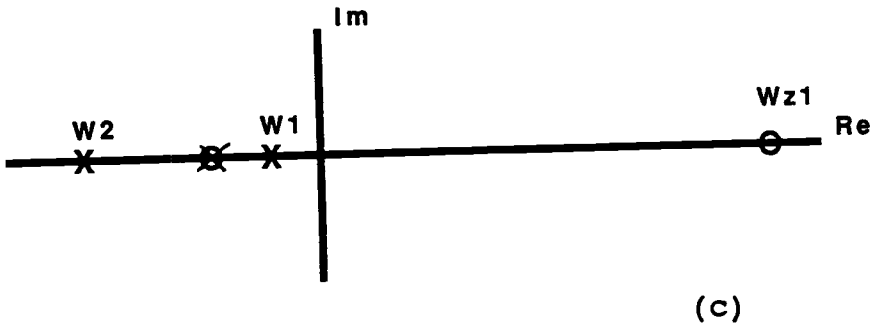


Fig. 12 A (b) The small-signal model of the amplifier, (c) the poles and zeros locations of the amplifier.

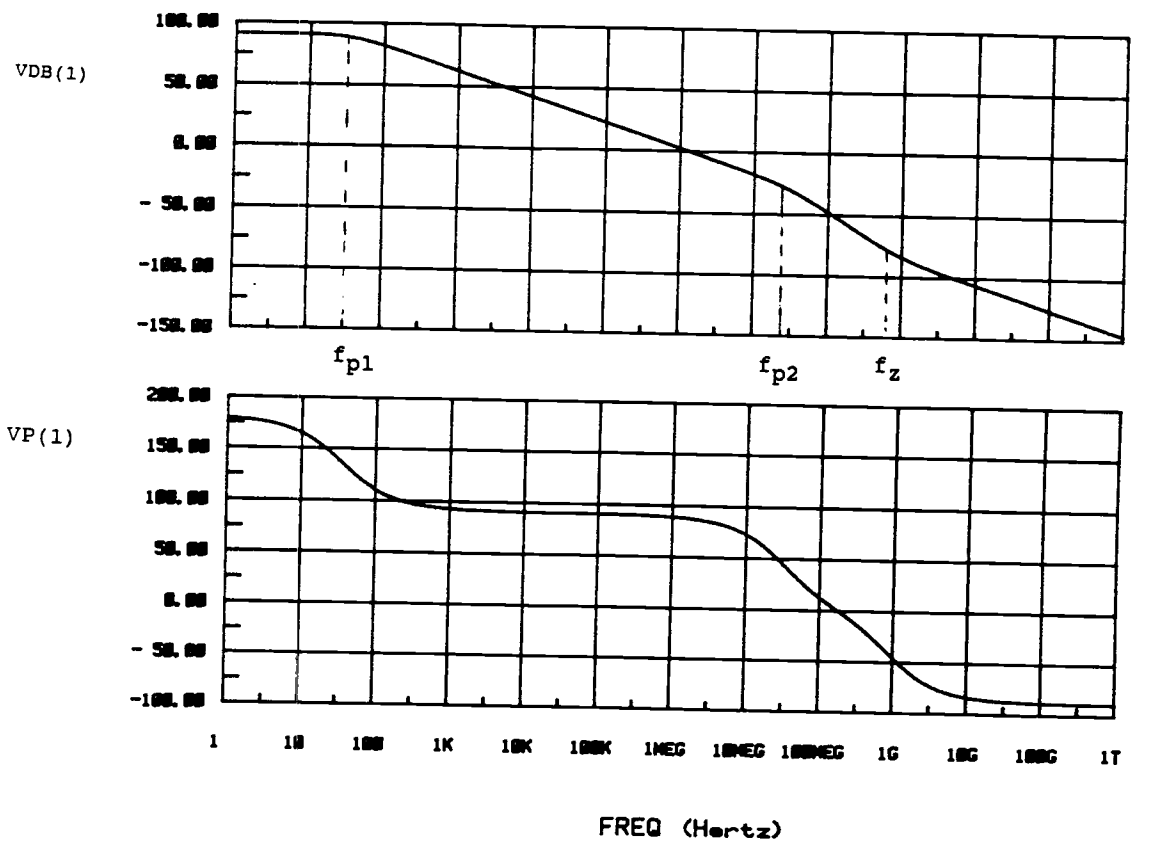


Fig. 13 The simulated frequency response of the amplifier in fig. 12a.

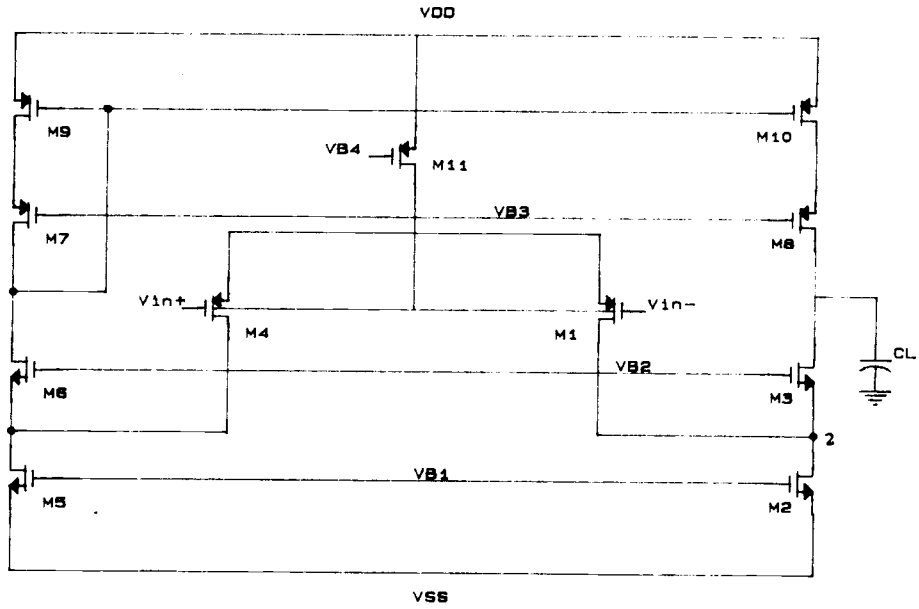


Fig. 14 A folded-cascode operational amplifier.

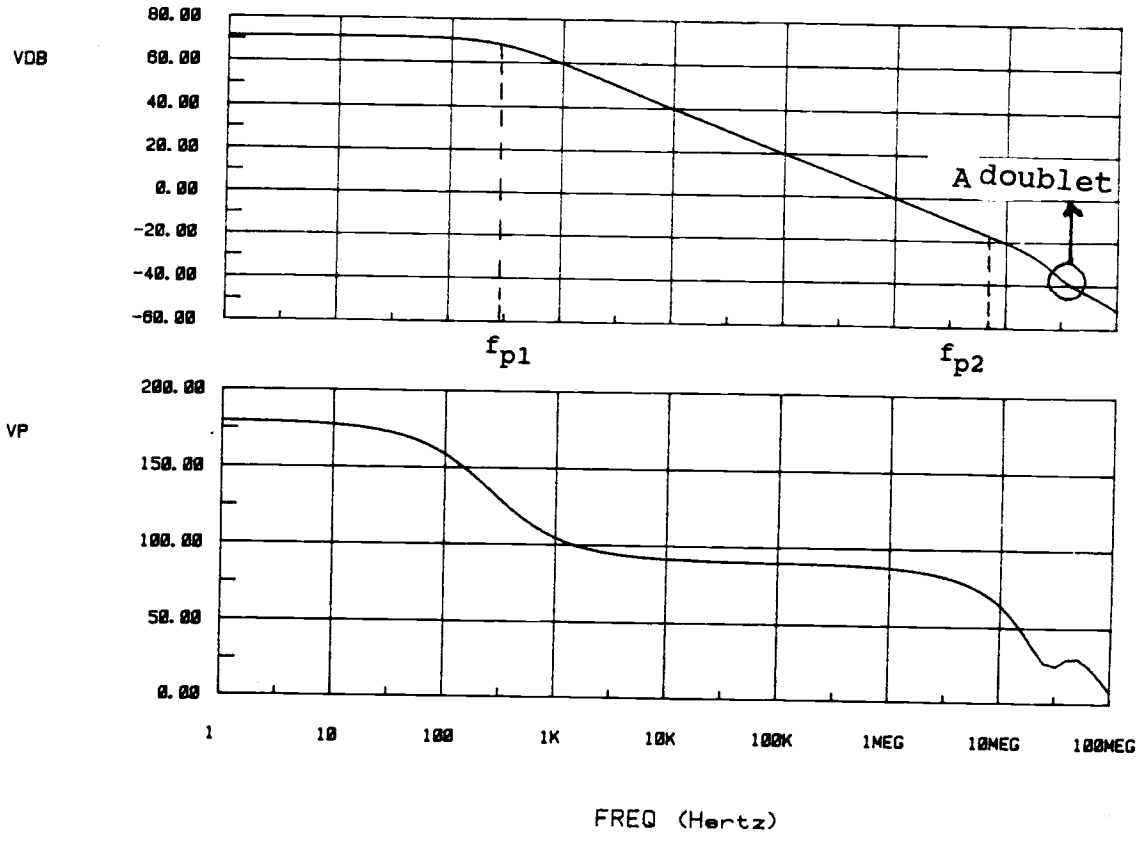


Fig. 15 The simulated frequency response of the amplifier in fig. 14.

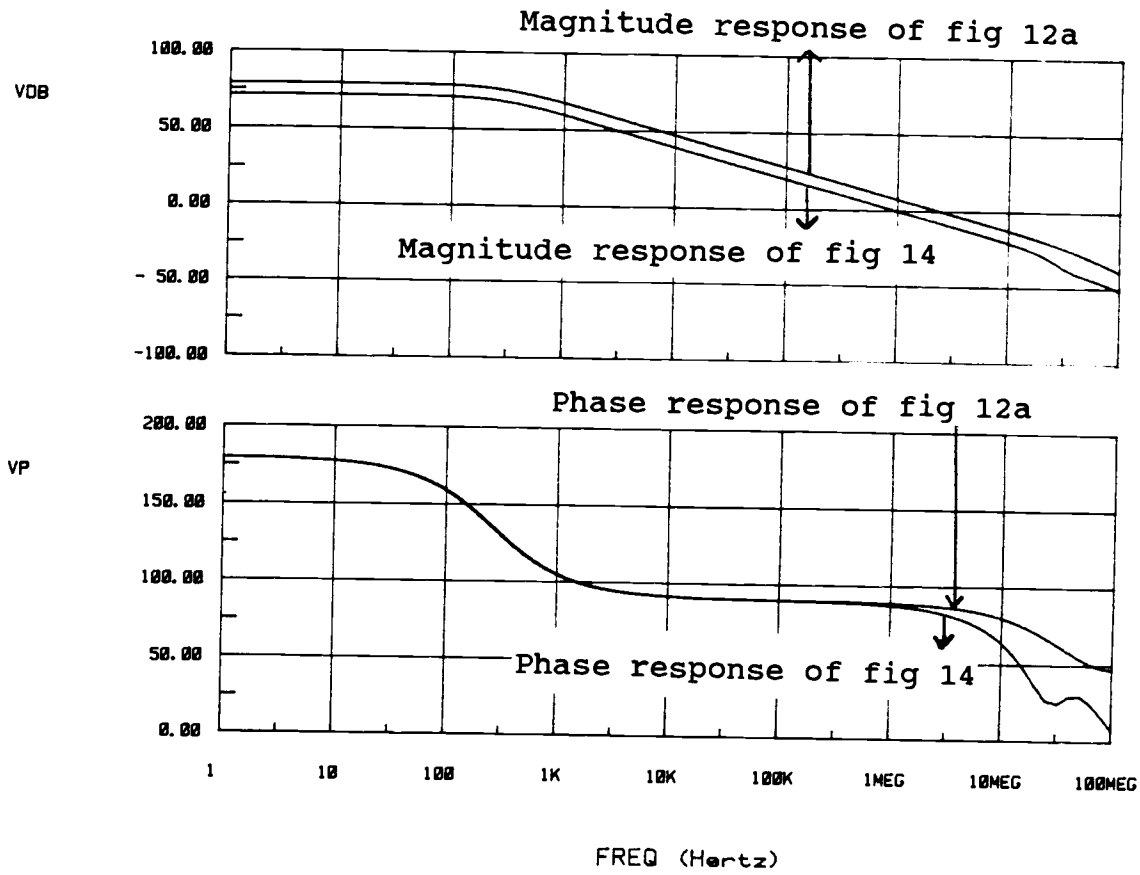


Fig. 16 The simulated frequency responses of the circuits in figures 12a and 14.

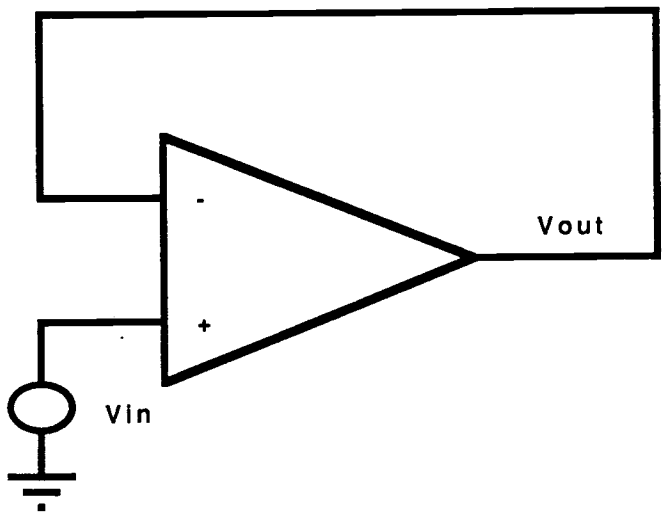


Fig. 17 An op-amp in unity-gain closed-loop configuration.

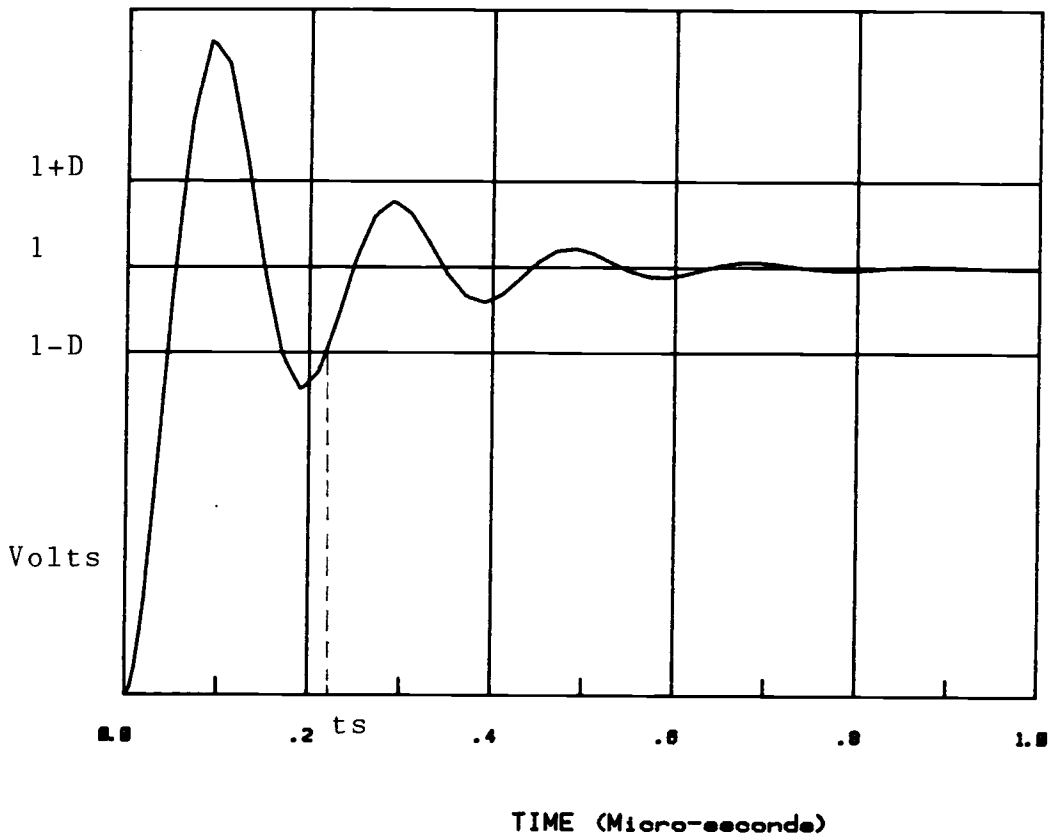


Fig. 18 An underdamped response with an error bound, D. The settling time is t_s.

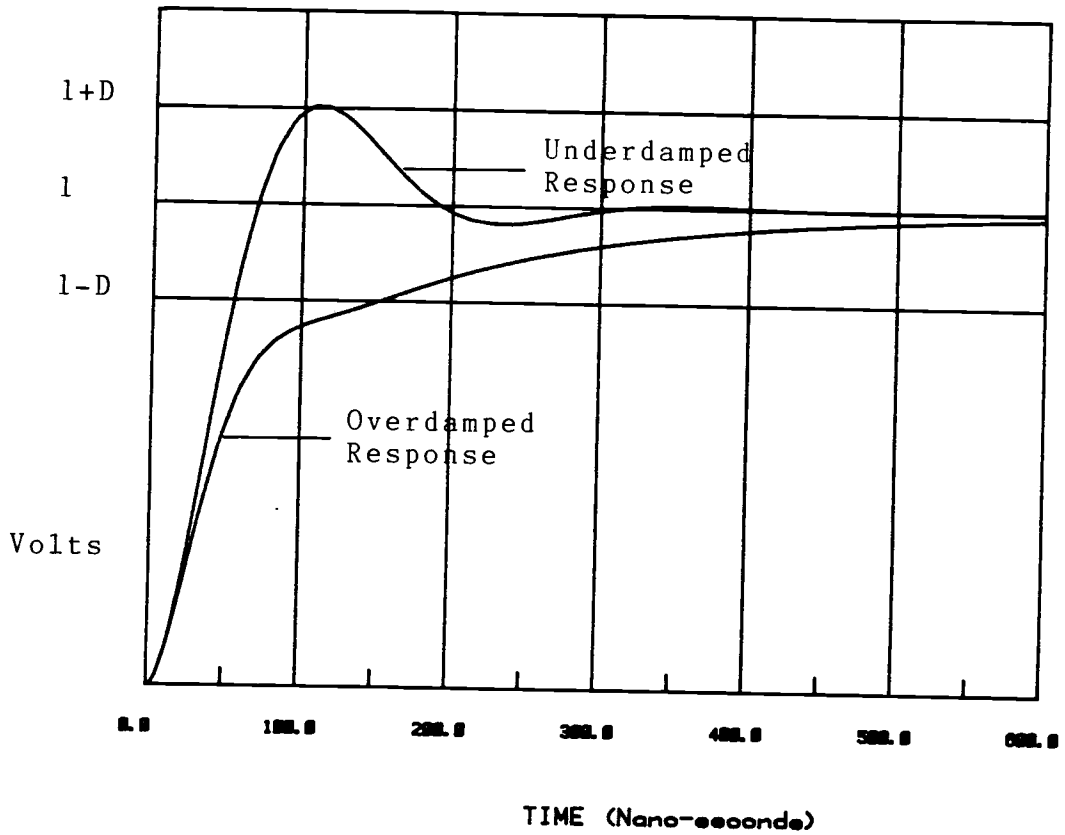


Fig. 19 An underdamped response just intersecting the upper error bound and an overdamped response.

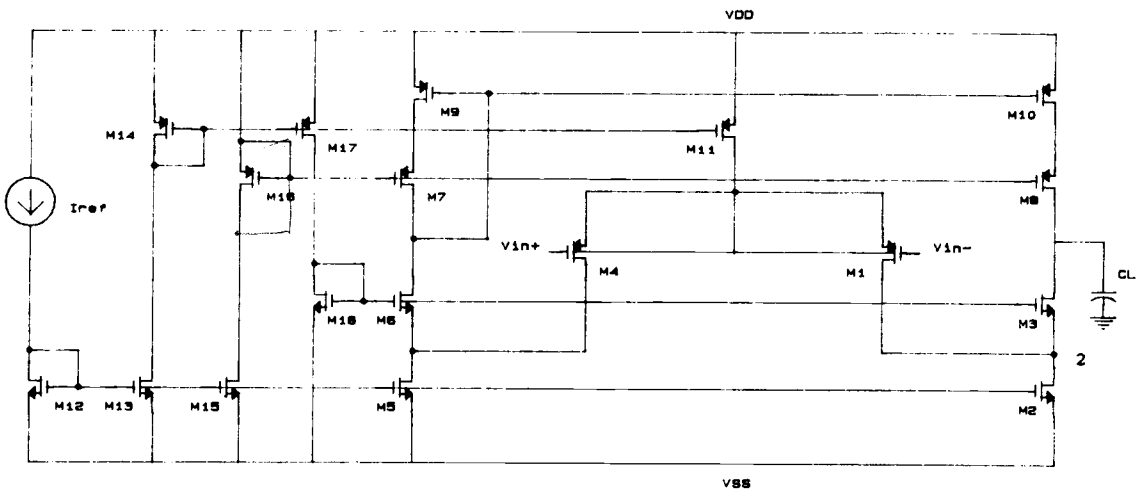


Fig. 20 The optimized folded-cascode op-amp with bias circuitry.

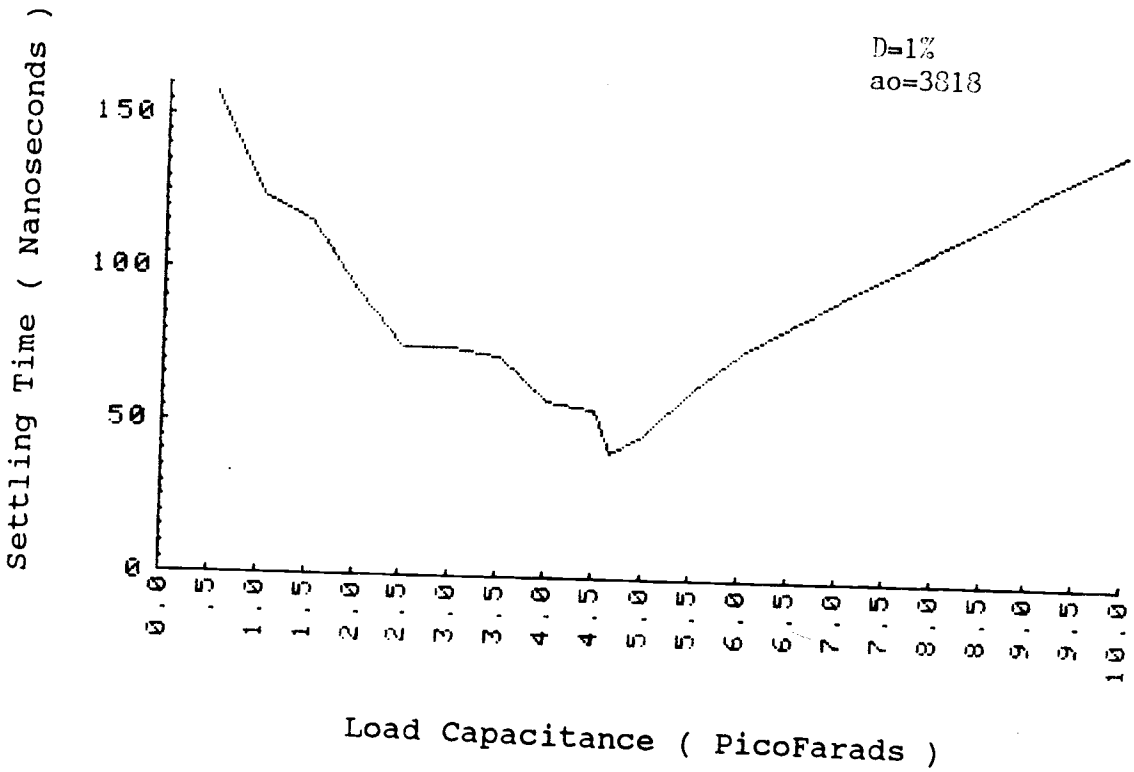


Fig. 21 A plot of the settling time vs. the load capacitance.

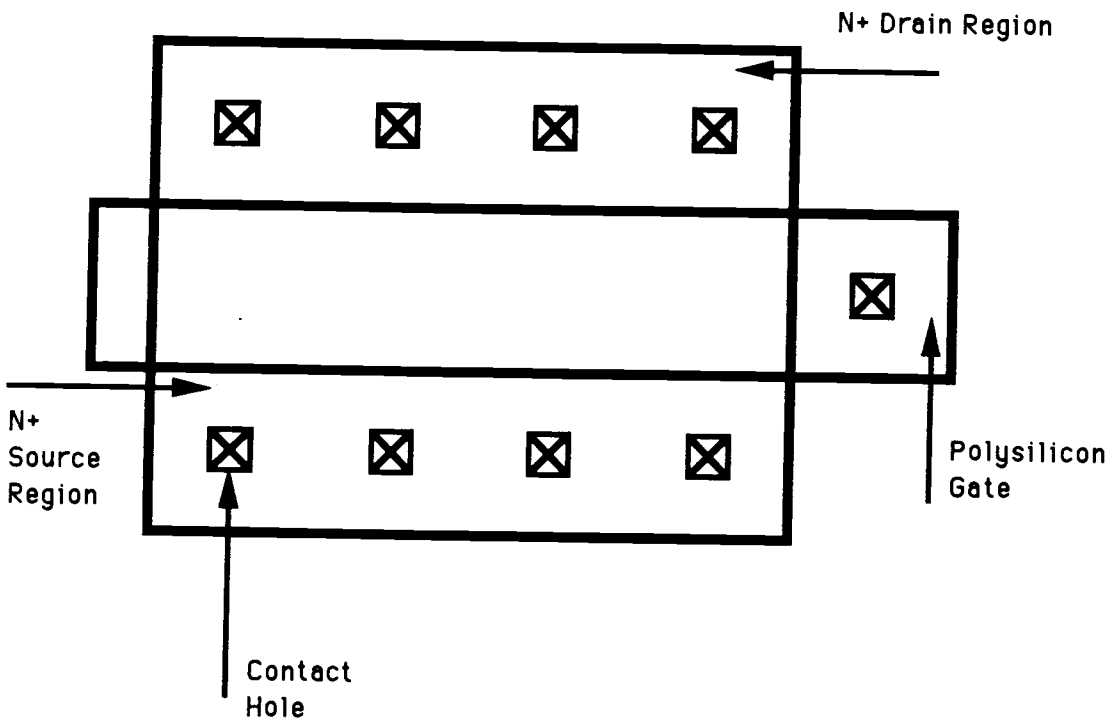


Fig. 22 A rectangular layout of a MOS transistor.

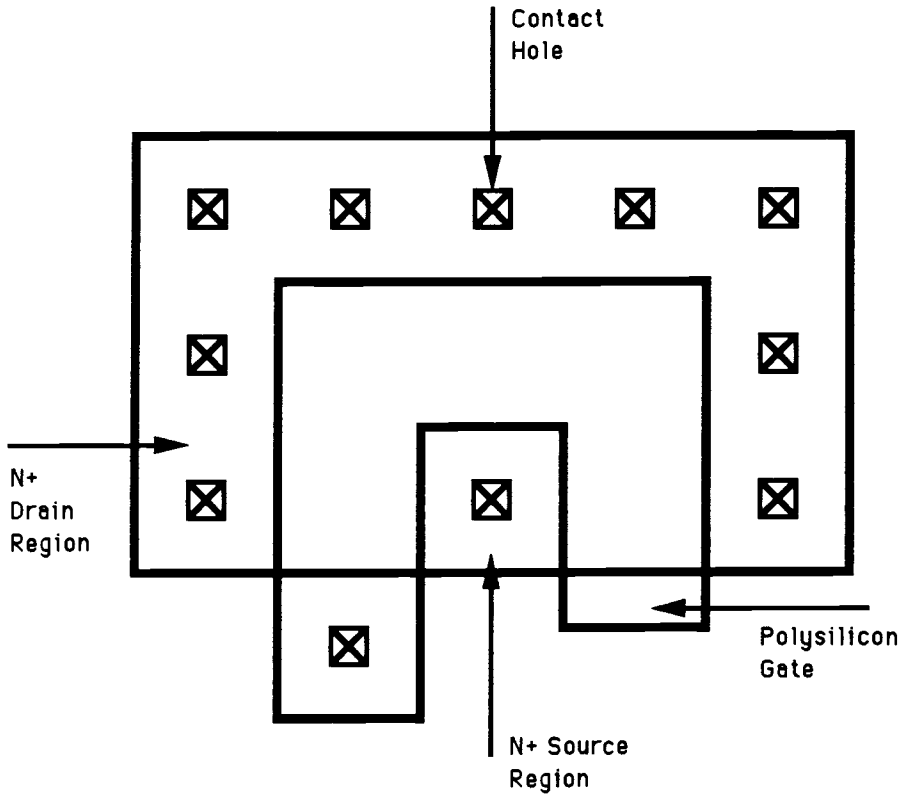


Fig. 23 A horseshoe layout of a MOS transistor.

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APPENDIX

Appendix A. Simulation programs

SPICE input file for the circuit in Fig. 6a.

```
COMMON-SOURCE AMPLIFIER ( RESISTIVE LOAD )
*
.MODEL N10 NMOS LEVEL=2 VTO=0.75 KP=40U GAMMA=0.17 PHI=0.52
+TOX=100N UCRIT=40000 UEXP=0.1 XJ=0.5U LD=0.3U PB=0.82
+CJSW=0.3N CGDO=0.173N CGSO=0.173N CGBO=0.1N JS=10U AF=1.25
+KF=1E-27 MJ=0.5 MJSW=0.5 LAMBDA=0.033 CJ=0.055M
*
.OPTIONS NOMOD
*
M1 2 1 5 5 N10 W=40U L=10U AS=360P AD=360P PS=58U PD=58U
*
VDD 10 0 DC 5
VSS 5 0 DC -5
VIN 1 0 DC -4.016 AC 1
*
CL 2 0 5P
R 2 10 1MEG
*
.TF V(2) VIN
.AC DEC 10 1 10G
*.DC VIN -4.05 -4 0.00025
*.PLOT DC V(2)
*.GRAPH DC V(2)
*.PRINT DC V(2)
.PRINT AC VDB(2) VP(2)
.PLOT AC VDB(2) VP(2)
.GRAPH AC VDB(2) VP(2)
.END
```

SPICE input file for the circuit in Fig. 10a.

```
CASCODE COMM-SOUR AMP ( RESISTIVE LOAD )
*
.MODEL N10 NMOS LEVEL=2 VTO=0.75 KP=40U GAMMA=0.17 PHI=0.52
+TOX=60N UCRIT=40000 UEXP=0.1 XJ=0.5U LD=0.3U PB=0.82
+CJSW=0.3N CGDO=0.173N CGSO=0.173N CGBO=0.1N JS=10U AF=1.25
+KF=1E-27 MJ=0.5 MJSW=0.5 LAMBDA=0.033 CJ=0.055M
*
.OPTIONS NOMOD
*
M1 2 1 5 5 N10 W=40U L=10U AS=360P AD=360P PS=58U PD=58U
M2 4 3 2 5 N10 W=40U L=10U AS=360P AD=360P PS=58U PD=58U
*
VDD 10 0 DC 5
VSS 5 0 DC -5
VIN 1 0 DC -3.9968 AC 1
VB 3 0 DC -3.75
*
CL 4 0 5P
R 10 4 1MEG
*
.TF V(4) VIN
.AC DEC 10 1 1T
*
.PRINT AC VDB(4) VP(4)
.PLOT AC VDB(4) VP(4)
.GRAPH AC VDB(4) VP(4)
.END
```

SPICE input file for the circuit in Fig. 12a.

```
CASCODE COMM-SOUR AMP ( CASCODE LOAD )
*
.MODEL N10 NMOS LEVEL=2 VTO=0.75 KP=40U GAMMA=0.17 PHI=0.52
+TOX=60N UCRIT=40000 UEXP=0.1 XJ=0.5U LD=0.3U PB=0.82
+CJSW=0.3N CGDO=0.173N CGSO=0.173N CGBO=0.1N JS=10U AF=1.25
+KF=1E-27 MJ=0.5 MJSW=0.5 LAMBDA=0.033 CJ=0.055M
*
.MODEL P6 PMOS LEVEL=2 VTO=-0.75 KP=12U GAMMA=0.45 PHI=0.62
+TOX=60N UCRIT=40000 UEXP=0.2 XJ=0.5U LD=0.3U PB=0.87
+CJSW=0.6N CGDO=0.173N CGSO=0.173N CGBO=0.1N JS=10U AF=1.25
+KF=1.5E-27 MJ=0.5 MJSW=0.5 LAMBDA=0.033 CJ=0.14M
*
.OPTIONS NOMOD
*
M1 2 1 5 5 N10 W=40U L=10U AS=360P AD=360P PS=58U PD=58U
M2 4 3 2 5 N10 W=40U L=10U AS=360P AD=360P PS=58U PD=58U
M3 4 6 7 10 P6 W=80U L=6U AS=720P AD=720P PS=98U PD=98U
M4 7 8 10 10 P6 W=80U L=6U AS=720P AD=720P PS=98U PD=98U
*
VDD 10 0 DC 5
VSS 5 0 DC -5
VIN 1 0 DC -4.011414 AC 1
VB2 3 0 DC -3.75
VB3 6 0 DC 3.75
VB4 8 0 DC 4.0
CL 4 0 5P
*
.TF V(4) VIN
*
.AC DEC 10 1 1T
.PRINT AC VDB(4) VP(4)
.PLOT AC VDB(4) VP(4)
.GRAPH AC VDB(4) VP(4)
.END
```