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Title: Design Techniques for Wideband Low-Power Delta-Sigma Analog-to-Digital Converters.

Abstract approved:

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Gábor C. Temes Pavan Kumar Hanumolu

Delta-Sigma (ΔΣ) analog-to-digital converters (ADCs) are traditionally used in high quality audio systems, instrumentation and measurement (I&M) and biomedical devices. With the continued downscaling of CMOS technology, they are becoming popular in wideband applications such as wireless and wired communication systems, high-definition television and radar systems. There are two general realizations of a ΔΣ modulator. One is based on the discrete-time (DT) switched-capacitor (SC) circuitry and the other employs continuous-time (CT) circuitry. Compared to a CT structure, the DT ΔΣ ADC is easier to analyze and design, is more robust to process variations and jitter noise, and is more flexible in the multi-mode applications. On the other hand, the CT ΔΣ ADC does not suffer from the strict settling accuracy requirement for the loop filter and thus can achieve lower power dissipation and higher sampling frequency than its DT counterpart.

In this thesis, both DT and CT ΔΣ ADCs are investigated. Several design innovations, in both system-level and circuit-level, are proposed to achieve lower power consumption and wider signal bandwidth.

For DT ΔΣ ADCs, a new dynamic-biasing scheme is proposed to reduce opamp bias current and the associated signal-dependent harmonic distortion is minimized by using the low-distortion architecture. The technique was verified in a 2.5MHz BW and 13bit dynamic range DT ΔΣ ADC. In addition, a second-order noise-

coupling technique is presented to save two integrators for the loop filter, and to achieve low power dissipation. Also, a direct-charge-transfer (DCT) technique is suggested to reduce the speed requirements of the adder, which is also preferable in wideband low-power applications.

For CT ΔΣ ADCs, a wideband low power CT 2-2 MASH has been designed. High linearity performance was achieved by using a modified low-distortion technique, and the modulator achieves higher noise-shaping ability than the single stage structure due to the inter-stage gain. Also, the quantization noise leakage due to analog circuit non-idealities can be adaptively compensated by a designed digital calibration filter. Using a 90nm process, simulation of the modulator predicts a 12bit resolution within 20MHz BW and consumes only 25mW for analog circuitry. In addition, the noise-coupling technique is investigated and proposed for the design of CT ΔΣ ADCs and it is promising to achieve low power dissipation for wideband applications.

Finally, the application of noise-coupling technique is extended and introduced to high-accuracy incremental data converters. Low power dissipation can be expected.

Design Techniques for Wideband Low-Power Delta-Sigma Analog-to-Digital Converters

by
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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

Design Techniques for Wideband Low-Power Delta-Sigma Analog-to-Digital Converters

CHAPTER 1. INTRODUCTION

High performance delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are desirable in applications where high input bandwidths (> 1 MHz) and medium-to-high resolutions (above 12bits) are required. With oversampling and noise-shaping characteristics, ΔΣ ADCs can achieve high dynamic range without the need for high-precision analog circuits, and thus can achieve good power efficiency compared with Nyquist-rate ADCs. The thesis describes the challenges and limitations associated with the ΔΣ ADCs design. It presents several techniques which can help overcome the limitations and achieve improved performance. The proposed techniques have been validated by system or circuit level simulations, post-layout simulations and the experiment chip evaluation.

1.1 Motivation

ΔΣ ADCs were traditionally and are still widely used for low-frequency high resolution applications, such as consumer electronics and instrumental measurement. In the last decade, the expanding market for wired and wireless communication systems, driven by more and more advanced technology and circuit design techniques, increases the demand for wideband low-power data converters with high resolution. For signal bandwidths within a 20 MHz range, ΔΣ ADCs have often been used in these systems [1-4]. Fig.1.1 [5] shows the relationship between the input bandwidth and the required dynamic range (DR) of the ΔΣ ADCs used in up-to-date wireless standards.

To date, most commercial ΔΣ ADCs use discrete-time (DT) architectures due to many reasons. A DT ΔΣ ADC can be easily analyzed and designed in z-domain and the design procedure is well developed. In addition, the loop filters of DT ΔΣ

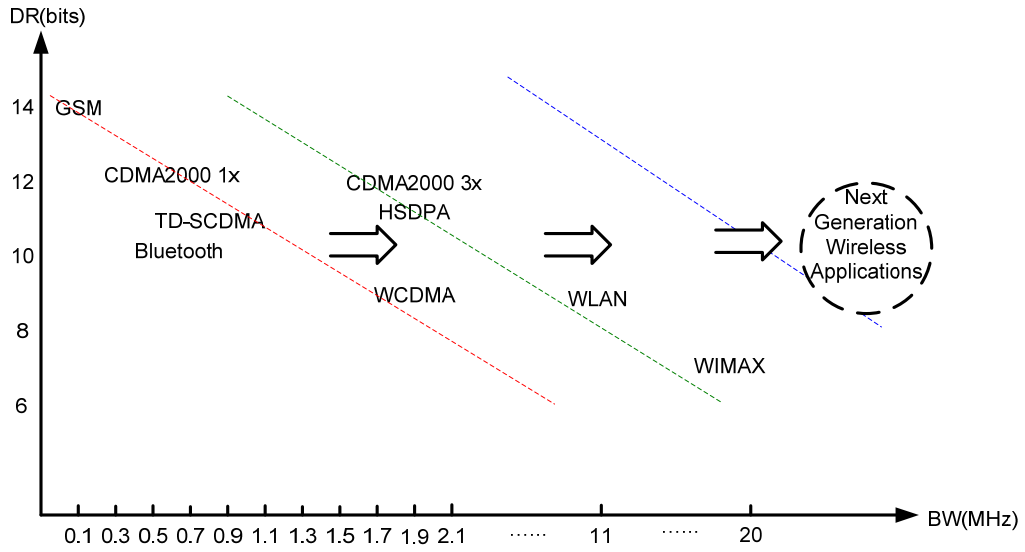

Figure 1.1: ΔΣ ADC performance requirement in some wireless applications.

ADCs are implemented using switched-capacitor (SC) circuits and the integrator gain relies on the ratio of capacitors, which can be very accurate and insensitive to process variation. Moreover, the performance is robust and scalable with clock frequency, which is particularly attractive for multi-mode applications. However, the sampling frequency of DT ΔΣ ADCs is usually limited by the settling requirements of the operational amplifiers (opamps), which usually becomes a bottleneck for wideband applications.

On the other hand, continuous-time (CT) ΔΣ ADCs have become popular in transceiver systems for two important advantages. First, the sampling operation of the CT ΔΣ ADCs is executed at the input of the quantizer, and the aliased out of band noise will be attenuated by the loop gain of the modulator. It can reduce the design requirement of the front-end anti-aliasing filter and hence reduce the power consumption of the system. Second, the loop filters are implemented using Active-RC or Gm-C filters and there is no stringent settling requirement for the operational amplifiers in CT ΔΣ ADCs. It enables sampling frequencies of CT ΔΣ ADCs up to several hundred MHz, which is still not possible for their DT

counterparts. Fig.1.2 shows an audit result of published papers for DT and CT ΔΣ ADCs.

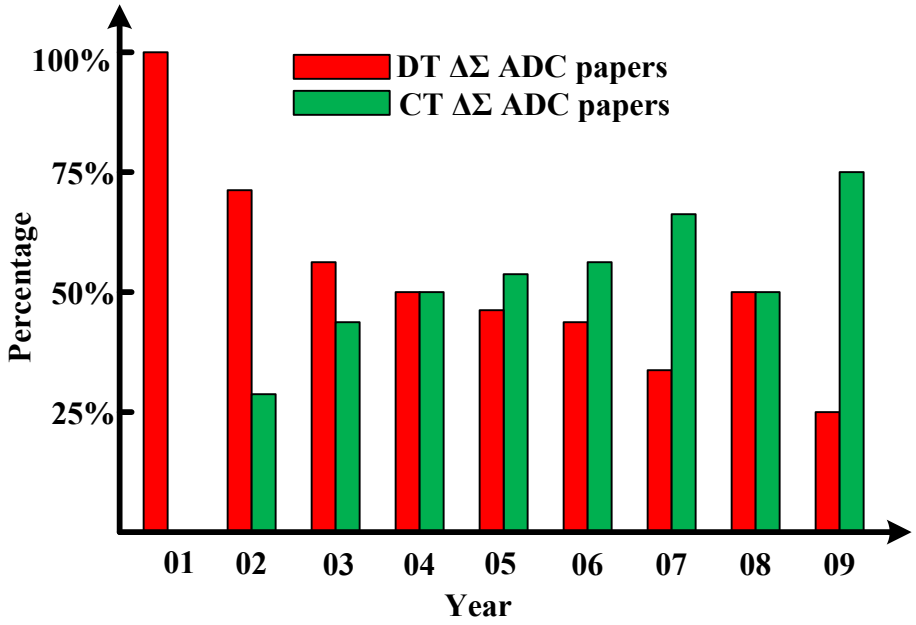

Figure 1.2: The comparison of DT and CT ΔΣ ADCs in ISSCCs.

in recent years' International Solid-State Circuit Conference (ISSCC). It demonstrates the increasing interest and efforts that CT ΔΣ ADCs have received.

Compared with DT ΔΣ ADCs, the design of CT ΔΣ ADCs is more challenging. The converters are sensitive to clock jitter noise and suffer from the large coefficient uncertainty of the loop filter due to process variations of resistors and capacitors. The excess feedback loop delay will increase the order of the loop filter and thus degrade stability performance.

This research work investigates new design techniques for both DT and CT ΔΣ ADCs. First, a 2.5MHz BW, 78dB SNDR DT ΔΣ modulator was realized. A new dynamic-biasing technique was proposed to reduce opamp power dissipation. Second, a 20MHz BW, 12bit resolution CT cascade ΔΣ modulator was designed. The analog circuit design requirement, as well as the power dissipation, is reduced by using an adaptive background calibration technique. Third, the first-order

noise-coupling technique for DT ΔΣ ADCs was extended to be used for CT ΔΣ ADCs. Then the second-order noise-coupling technique was introduced to further reduce the active components, and new circuit blocks were used to simplify the modulator complexity. Power dissipation reduction can be expected. After that, a direct-charge-transfer (DCT) technique was proposed to reduce the speed requirement of the adder for a ΔΣ modulator using a feed-forward structure, and can be useful for wideband low-power applications. Finally, a noise-coupled low-power incremental ADC is proposed, and the corresponding design methodology is introduced.

1.2 Contributions

The major contributions of this research can be summarized as fellows:

- New dynamic-biasing technique for wideband low-power switch-capacitor circuit design.
- New architecture for CT cascade ΔΣ modulator (MASH)
- Improved low-distortion technique for CT ΔΣ ADCs.
- New background calibration technique for CT MASH ADCs.
- New CT ΔΣ ADCs using noise-coupling technique.
- New ΔΣ ADCs architectures with second-order noise-coupling technique.
- New delay-cell circuit blocks for noise-coupled ΔΣ ADCs.
- New direct-charge-transfer (DCT) adder for wideband low-power ΔΣ ADCs.
- New noise-coupled incremental data converters.

1.3 Thesis Organization

This thesis covers the theoretical analysis and circuit implementations for both DT ΔΣ ADCs and CT ΔΣ ADCs. It is organized as follows:

Chapter 2 provides fundamental background knowledge about ΔΣ ADCs to help understand the rest of the thesis.

Chapter 3 presents a 2.5MHz BW 78dB SNDR DT ΔΣ modulator using dynamically-biased amplifiers. The operation principle of proposed dynamic-biasing scheme, corresponding circuit design and chip measurement results are all described.

Chapter 4 introduces a novel CT 2-2 MASH ADC with 20MHz BW and 12bit resolution. Several new design techniques are proposed, and the details of the modulator, from system level and circuit level to the layout, are described.

Chapter 5 proposes noise-coupled CT ΔΣ ADCs. The noise-coupling technique for DT ΔΣ ADC is extended to CT ΔΣ ADC. Operation principle and circuit realization are discussed.

Chapter 6 discusses the high-order noise-coupled ΔΣ ADCs. Second-order noise-coupling technique is presented. New single-delay cell and double-delay cell are introduced to simplify the analog coupling circuit.

Chapter 7 presents the direct-charge-transfer adder for wideband low-power ΔΣ ADCs.The operation principle and implementations are introduced. Its application in double-sampling ΔΣ ADCs is also discussed.

Chapter 8 extends the application of the noise-coupling technique to incremental data converters. The proposed idea is verified by an example second-order noise-coupled incremental ADC using extended counting technique.

Chapter 9 concludes the thesis, summarizes the research work and suggests some future works.

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CHAPTER 2. OVERVIEW OF ΔΣ A/D CONVERTERS

In this chapter, the basics of ΔΣ A/D converters will be reviewed. The concepts of quantization noise, oversampling and noise shaping are illustrated. Different architectures for ΔΣ A/D converters are described and compared.

2.1. Delta-Sigma A/D Converter Basics.

2.1.1 Sampling and Quantization.

The analog-to-digital converter (ADC) is an interface between the real analog world (composed of continuous-time and continuous-amplitude signals) and the digital world (composed of discrete-time and discrete-amplitude signals). As is shown in Fig. 2.1, the operation can be described by two characteristics: Sampling and Quantization.

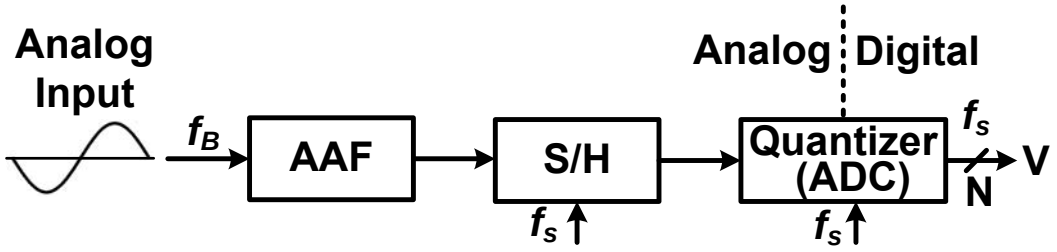


Figure 2.1: Block diagram of Nyquist rate Analog-to-Digital Converter.

The sampling process converts an analog signal to discrete time steps. The frequency f_s of the discrete-time steps is called the sampling frequency and should be at least twice the signal bandwidth f_B to avoid the aliasing of undesired high frequency signals (Nyquist sampling theorem).Therefore, a front-end anti-aliasing filter (AAF) is usually required to limit the input signal bandwidth. The sampled signal should also be held for a sufficient time to be represented by a set of

discrete-time values, so the sampling operation is actually realized by a sample and hold circuit.

Although the sampled signal is represented in discrete-time values, the amplitude is still in analog domain. The quantizer can then convert the sampled signal into discrete digits. For an ideal quantizer with N-bit resolution, there are 2^N-1 uniform quantization steps. Its transfer function is defined by the static input-output characteristics. Assuming the full-scale (V_{FS}) input signal range of $\pm V_{REF}$, the step size of the quantizer, or the value of the least-significant-bit (LSB), is $\Delta = \frac{2V_{REF}}{2^N - 1}$. An ideal 2-bit quantizer is shown in Fig.2.2 (a).The corresponding quantization error, or quantization noise, is shown in Fig.2.2 (b). If input signal y is within $-(V_{REF}+V_{LSB}/2)$ and $V_{REF}+V_{LSB}/2$, the quantization error varies between $-V_{LSB}/2$ and $+V_{LSB}/2$ and quantizer locates at the linear (non-saturated) region. For input signal beyond the linear region, the quantizer output value will not change with increased input signal. The quantizer enters the overload (saturation) region, which is undesirable because of the increased harmonic distortion.

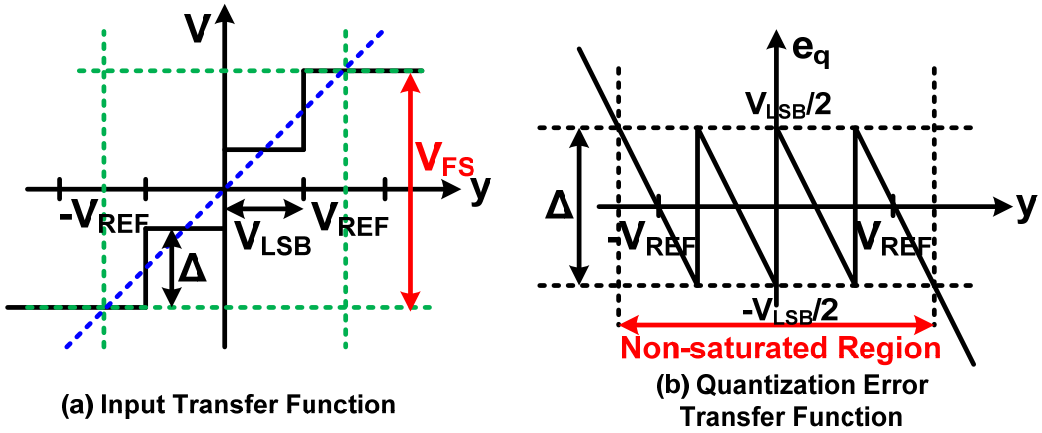


Figure 2.2: Ideal 2-bit quantizer.

The ideal quantizer is deterministic and the quantization error e_q is completely defined by the input. However, if the input signal changes randomly from sample to sample by the amount comparable with or greater than the step size, without

causing saturation, then the error is mostly uncorrelated between samples and has equal probability within the range ±Δ/2. If the error is statistically independent of the input signal, which is feasible under most cases, then it can be represented as a random white noise. The average noise power, or mean square value, is given by

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.1}$$

When a signal is quantized at frequency f_s, the quantization noise is uniformly distributed within the Nyquist frequency band, which means between dc and half of the sampling frequency f_s . For a sinusoidal input signal with amplitude A_u, the maximum signal to quantization noise ratio (SQNR) of an *N*-bit quantizer is thus given by

$$SQNR_{\max} = \frac{A_{u,\max}^2 / 2}{e_{rms}^2} = \frac{2^{2N-3}\Delta^2}{\Delta^2/12} = \frac{3}{2}2^{2N} \tag{2.2}$$

Expressed in dB, the performance of an ideal Nyquist-rate ADC is given by

$$SQNR_{\max}[dB] = 6.02N + 1.76 \tag{2.3}$$

2.1.2 Oversampling

In a sampled system, the quantization noise equally distributes within half of the sampling frequency band and total quantization noise power is equal to $\frac{\Delta^2}{12}$. To reduce the passband quantization noise and improve the SNR, one straight-forward way is “Oversampling”. Fig 2.3 shows the block diagram of an oversampling ADC system. The analog input signal is sampled by the rate f_s, which is much faster than the Nyquist frequency f_N, and then it is digitized by the quantizer to generate a digital output. For a complete A/D Converter, a subsequent decimation filter is used to filter the out-of-band noise and convert the oversampled digital output data to a high-resolution digital signal at a rate of f_N. The oversampling ratio (OSR) is defined as OSR=f_s/f_N .

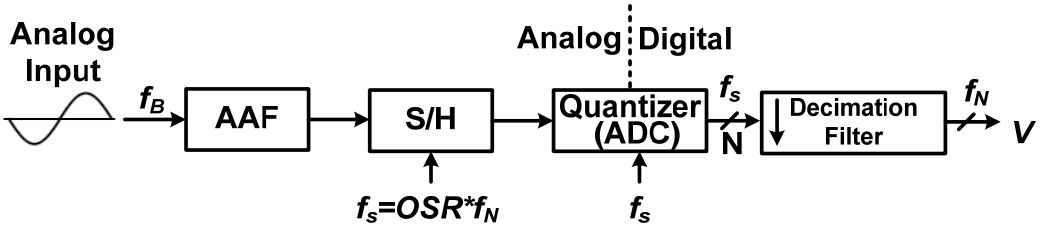


Figure 2.3: Block diagram of oversampled Analog-to-Digital Converter.

There are two main advantages of oversampling ADCs. First, the oversampling creates a wider transition band between the pass-band and its first alias band. Then the design requirement of the front-end anti-aliasing filter is relaxed and usually a simple passive low pass filter is good enough. The reduced filter order and gentler roll-off means smaller die area and lower power dissipation in an IC implementation. Second, as is shown in Fig. 2.4, the quantization noise spreads out to $f_s/2$, and the amount of quantization noise in the passband f_B is reduced to Eq. 2.4.

$$e_{rms,OSR}^2 = \frac{2}{f_s}\int_0^{f_B} e_{rms}^2 df = \frac{e_{rms}^2}{OSR} \tag{2.4}$$

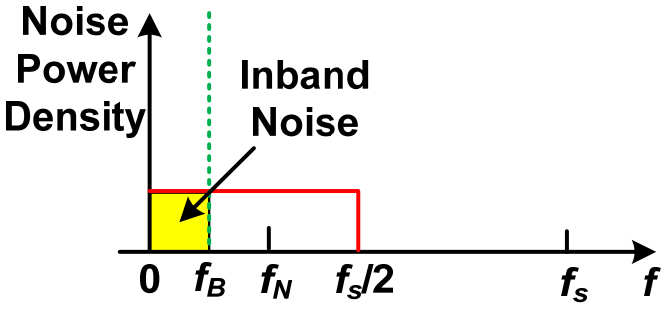


Figure 2.4: Quantization noise spectra for oversampling ADCs.

So, oversampling ADC trades resolution in time with resolution in amplitude to ease the demands on precision with which the signal must be quantized. The maximum achievable SQNR is given by Eq. 2.5.

$$SQNR_{max}[dB] = 6.02N+1.76+10\log_{10}OSR \tag{2.5}$$

2.1.3 Noise Shaping

As explained in Eq. 2.5, the SNR of oversampling ADCs can gain 3dB improvement by doubling the sampling frequency. However, the oversampling alone is not an effective means to achieve high resolution, especially for wideband applications. For a 4-bit quantizer and 10MHz signal bandwidth, an oversampling ratio of OSR=4^6 is required to obtain 10 bits of resolution. It means that the required minimum sampling frequency is 82GHz, which is impractical using modern CMOS process. To further improve the SNR, "noise shaping" is employed with oversampling in ΔΣ ADCs.

Fig. 2.5 shows the block diagram of a single stage DT ΔΣ modulator (excluding the decimation filter). It normally contains three key circuit blocks: a loop filter H(z),a quantizer and one feedback DAC. The quantizer working within the non-saturation region behaves as a linear adder for the loop filter output and the quantization error. So the modulator has two inputs (analog input signal U and quantization error E) and one output (modulator output V). The signal transfer function (STF) from U to V and the noise transfer function (NTF) from E to V are given by

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{2.6}$$

$$NTF(z) = \frac{1}{1+H(z)} \tag{2.7}$$

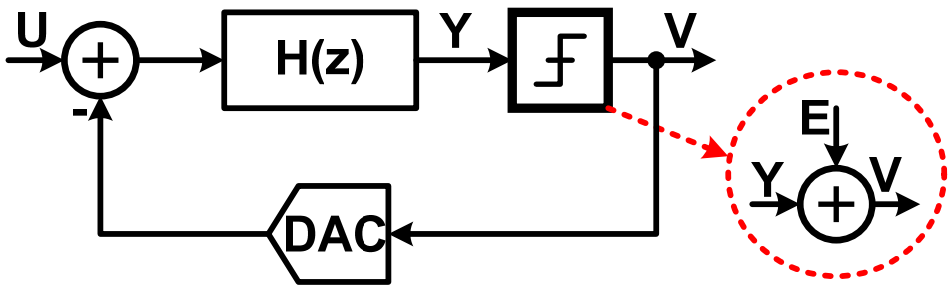


Figure 2.5: The general block diagram of a DT ΔΣ modulator.

For the simple case of $H(z)=\frac{z^{-1}}{1-z^{-1}}$,STF(z)=$z^{-1}$ and NTF(z)=1-z^{-1}, the input signal U is delayed and appears at the modulator output without attenuation, while the quantization error E is first-order high pass shaped. By properly designing the loop filter H(z), *L*-th order high pass shaping of the quantization error can be achieved and the squared magnitude of the noise transfer function, NTF(z)=(1-z^{-1})^L, is given by

$$|NTF(e^{j\omega})|^2=|1-e^{-j\omega}|^{2L}=(2-2\cos\omega)^L=\left(2\sin(\pi\frac{f}{f_s})\right)^{2L} \tag{2.8}$$

So, the power spectral density of the quantization noise will be shaped by the squared magnitude of NTF(z) and the quantization noise power within the signal band is given by

$$e_q^2=\frac{2}{f_s}\int_0^{f_B} e_{rms}^2\,|NTF(e^{j\omega})|^2\,df=\frac{2^{2L+1}e_{rms}^2}{\pi}\int_0^{\pi\cdot f_B/f_s}\sin^{2L}(\pi\frac{f}{f_s})d(\pi\frac{f}{f_s}) \tag{2.9}$$

If the sampling frequency f_s is much larger than the pass band frequency f_B, $\sin(x)\approx x$, and the total inband quantization noise power is

$$e_q^2=e_{rms}^2\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{2.10}$$

Expressed in dB, the performance of an ideal oversampled ΔΣ ADC with *L*-th order noise-shaping is given by

$$SQNR_{\max}[dB]=6.02N+1.76+20L\times\log_{10}^{\frac{OSR}{\pi}}+10\log_{10}^{(2L+1)OSR} \tag{2.11}$$

Besides the original resolution *N*, the SQNR increases with the OSR at a rate of 6*L*+3 dB/octave or *L*+0.5 bit/octave. Assuming a 4-bit quantizer, Fig. 2.6 shows the illustrative plot for noise shaping order from *L*=0 to *L*=5.

Again, for a 4-bit quantizer and 10MHz signal bandwidth, a 2nd order noise-shaping and oversampling ratio of OSR=10 are sufficient to achieve 10bit

resolution. The required sampling frequency is only 200MHz, which is greatly reduced and becomes practical in modern processes.

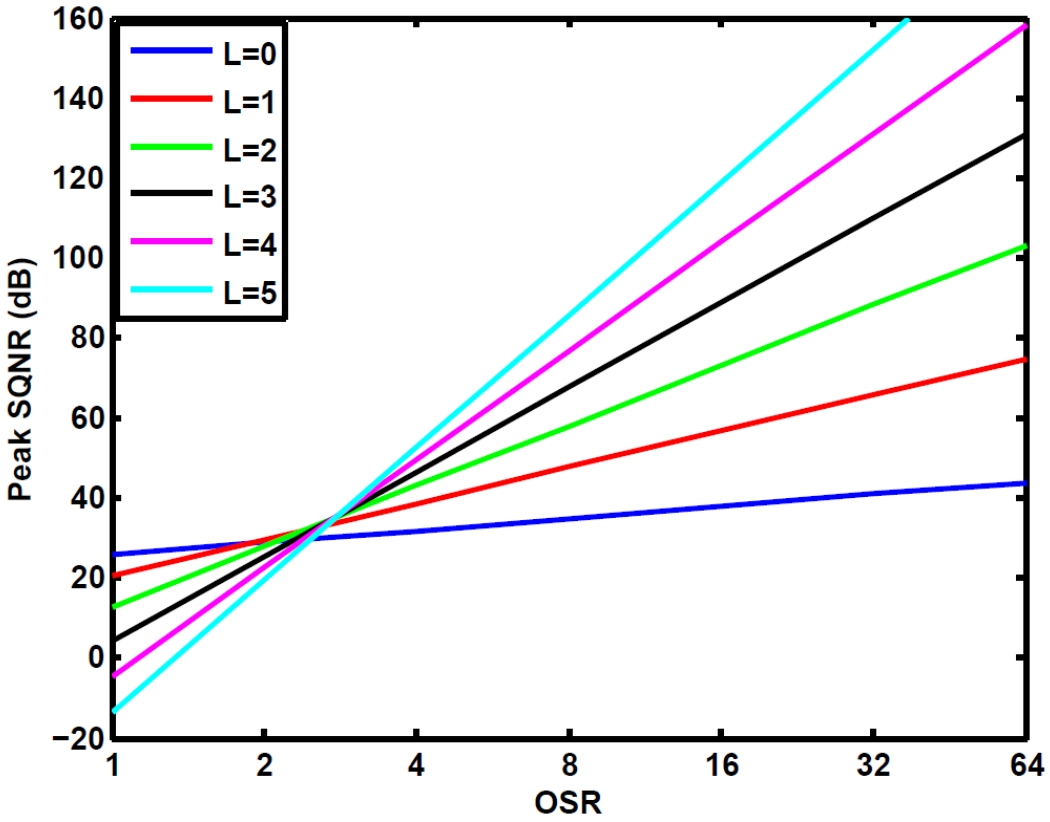


Figure 2.6: SQNR improvement with OSR and noise shaping order (N=4).

2.2. Delta-Sigma A/D Converters Architectures

There are different architectures for ΔΣ ADCs and classification is usually based on the number of modulators and the circuit realization of the loop filter. In general, ΔΣ ADCs are grouped as single-stage or multi-stage (MASH), and discrete-time (DT) or continuous-time (CT).

2.2.1 Single-Stage vs. Multi-Stage ΔΣ ADCs [1]

2.2.1.1 Single-stage topology

There is only one quantizer in single-stage ΔΣ ADCs. The quantizer output is the input of the feedback DAC and the DAC output is subtracted from the input signal, filtered by the loop filter and then fed back to the quantizer input. Based on the loop filter configuration, there are two generalized single-stage topologies .

a. Fig. 2.7 shows a 4th order single-stage ΔΣ modulator containing the loop filter with distributed feedback and input coupling (CIFB).The loop filter contains 4 integrators, with the input signal as well as the feedback signal being fed to each integrator input terminal with weight factors a_i and b_i.The local resonator feedback coefficients g_1 and g_2 are used to intentionally shift the poles of the loop filter (the zeros of NTF) from DC to some in-band frequencies. This can further reduce in-band quantization noise power, which is very desirable for wideband high resolution applications.

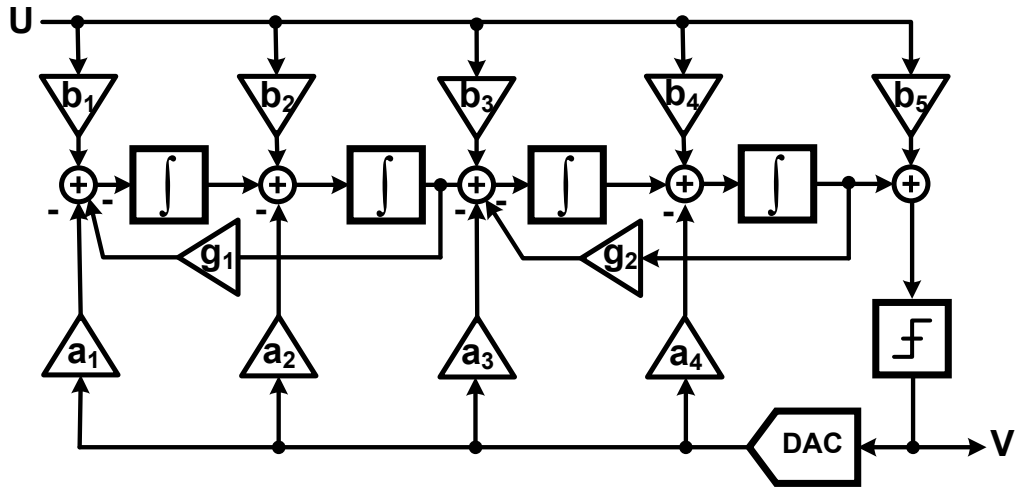


Figure 2.7: Cascade integrators with distributed feedback and input coupling.

In the CIFB structure, the input signal and feedback signal have different loop transfer functions. For a DT ΔΣ modulator using CIFB structure, the signal transfer function STF(z) and noise transfer function NTF(z) can be given as :

$$STF(z) = \frac{G(z)}{1 + H(z)} \tag{2.12}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{2.13}$$

By setting all feed-in branches except the first to zero, the ΔΣ modulator with CIFB structure has the maximally-flat all-pole signal transfer function. It means that the modulator can easily achieve low-pass filtering STF, and then it is more robust to out-of band interferences. However, all integrators need to deal with shaped quantization noise as well as the input signals. This increases integrator output swing and harmonic distortion. In addition, the multiple feedback DACs consume considerable area and power, especially when a multi-bit quantizer is used.

b. The NTF in single-stage ΔΣ modulator can also be designed using feed-forward, rather than feedback, signal paths to realize the loop filter. The example 4^{th} order structure is depicted in Fig. 2.8. It contains the chain of integrators with weighted feed-forward branches a_i for summation (CIFF). The local resonator feedback coefficients g_1 and g_2 are again used to shift zeros of the NTF from DC to in-band frequencies. Since the input signal and feedback signal go through the same loop filter, for a DT ΔΣ modulator using CIFF structure, the signal and noise transfer function can be given as :

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{2.14}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{2.15}$$

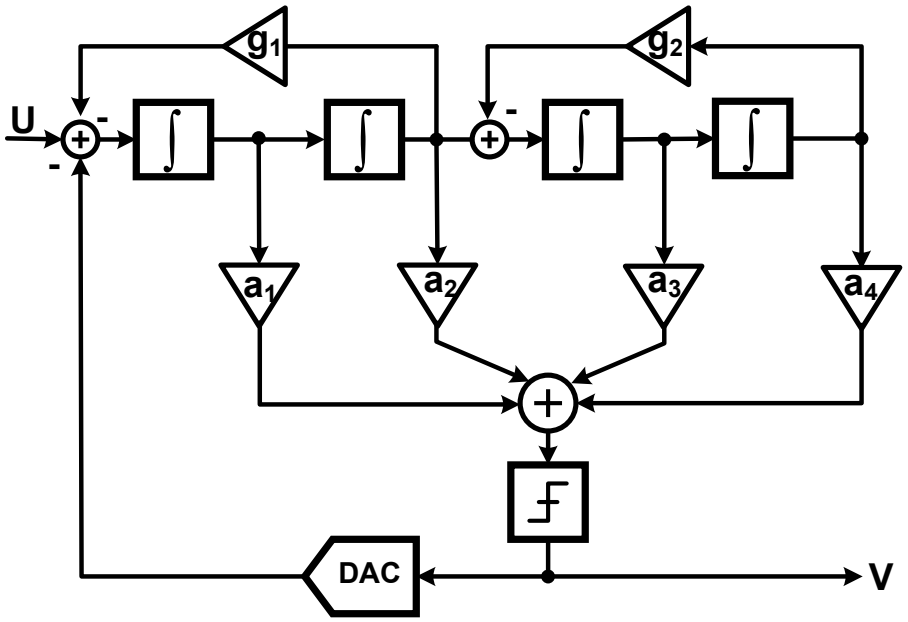


Figure 2.8: Chain of integrators with weighted feed-forward summation (CIFF).

Compared to the ΔΣ modulator using CIFB topology, the modulator using CIFF architecture requires only one feedback DAC, which can reduce the power consumption and area. On the other hand, the STF(z) of ΔΣ modulator using CIFF topology shows out-of band peaking and in some cases results in loop instability if there exists large out-of band interferences.

For DT ΔΣ ADCs with zero optimization, if the local resonator is designed using two delayed switched-capacitor integrators, the poles of the resonator will be outside the unit circle and the resonator itself will be unstable. To keep the poles of the resonator on the unit circle, one of the integrators needs to be a delay-free integrator. The feed-forward architecture using this configuration is called the cascade of resonators with feed-forward summation(CRFF) structure and the feed-back architecture using this configuration is called the cascade of resonators with distributed feedback (CRFB) structure.

c. "Silva-Steensgaard structure", is another specific structure using CIFF topology. Fig. 2.9 shows the modified Fig. 2.7 using this structure. The corresponding NTF(z) is the same as Eq. 2.15 while the corresponding STF(z) is changed to

$$STF(z) = \frac{1 + H(z)}{1 + H(z)} = 1 \tag{2.16}$$

So, by adding a direct feed-in branch from the input signal to the quantizer, the input signal can be directly transferred to the modulator output without any delay and attenuation. It means that the loop filter only needs to deal with shaped quantization noise and thus signal dependent harmonic distortion can be greatly reduced. Since this topology greatly improves a modulator's linearity performance, it is also named the "**low-distortion**" architecture and is extensively used for wideband low-power applications.

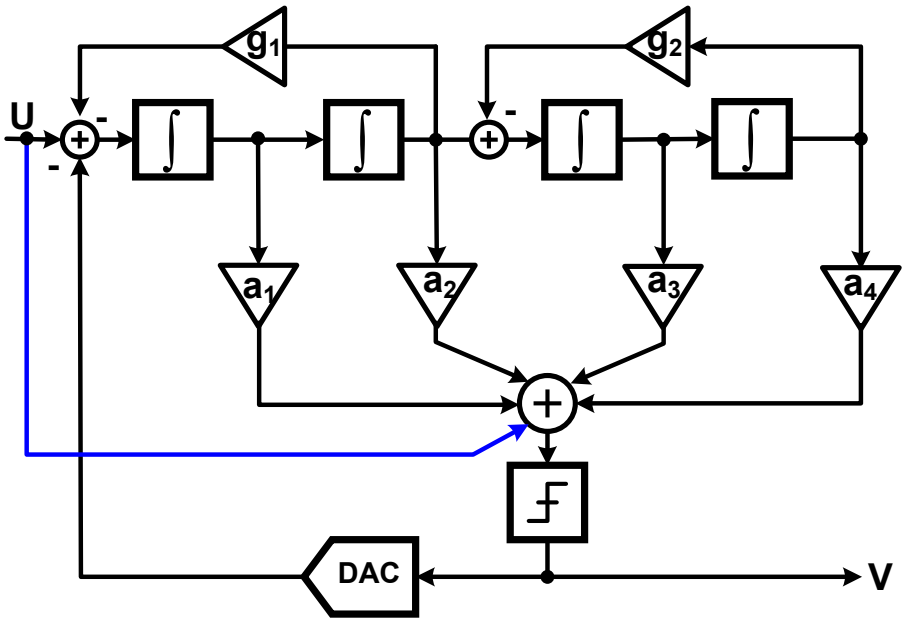


Figure 2.9: The low-distortion ΔΣ modulator using CIFF topology.

2.2.1.2 Multi-stage topology

To analyze and design the ΔΣ ADC, the quantizer is usually modeled as a linear summation block with constant gain. The gain, *k*, can be defined as:

$$k = \frac{< v, y >}{< y, y >} \tag{2.17}$$

However, when the nonlinearity of the quantizer is taken into account, the gain of the quantizer is actually not well defined. The issue becomes even worse for a single-bit quantizer, where the input signal can be any value but the output is limited to two levels. As is shown in the root-locus plot of Fig. 2.10, the variations of *k* will shift the poles of NTF away from original. For the first and second-order systems, the poles can still stay within the unit-circle in z-plane when *k* changes between 0 and 1, so stability is guaranteed. However, for third and higher order systems, some poles will move outside the unit-circle when the quantizer gain is smaller than a certain value, and then the ΔΣ ADC becomes unstable. In this case, the internal states of the ΔΣ ADC (the integrator outputs) will continue growing until they become saturated.

To maintain the stability of high order ΔΣ ADCs, the gain has to be limited within certain ranges. Table. 2.1 summarizes the required minimum *k* values for different noise-shaping orders. It is easy to conclude that k_{min} is required to be closer to the ideal gain value of 1 with higher-order noise shaping, and the corresponding ΔΣ ADC stability suffers more from circuit non-idealities.

Table 2.1: The quantizer gain requirement for ΔΣ ADCs.

	NTF(z)=$(1-z^{-1})^L$					
Order(*L*)	1	2	3	4	5	6
Gain(k_{min})	0	0	0.5	0.8	0.917	0.964

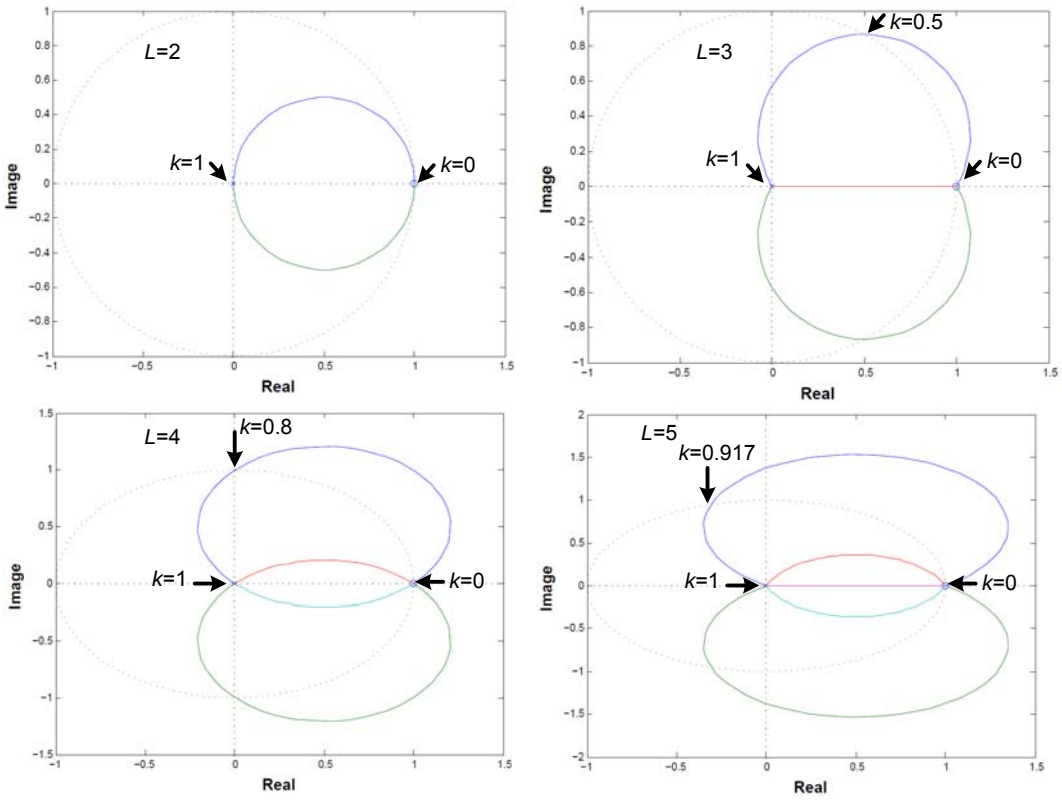


Figure 2.10: The root-locus plots for ΔΣ ADCs with different noise shaping orders.

In general, the gain *k* depends on the quantizer input *y* and the output signal *v*. If the input signal *y* is too large and the quantizer enters saturation region, the gain *k* will be reduced and the ΔΣ ADC becomes unstable. Different techniques can improve the stability of high-order ΔΣ ADCs. First, by limiting the out-of-band magnitude of the NTF(z), the likelihood of instability can be reduced. For a single-bit quantizer, Lee's empirical rule [2] requires that the maximum gain of NTF (z) should be less than 2.The disadvantage is that this will degrade the in-band noise-shaping performance. Another way to mitigate the stability issue is to use a multi-bit quantizer. This can reduce the quantization error and improve the linearity of the quantizer, and then the gain of the quantizer is much more constant compared to a single-bit structure. In reality, the stability is still limited by the resolution of quantizer, comparator offset, comparator mismatches and other non-ideal effects.

Since the first and second-order ΔΣ ADCs are very robust against quantizer gain variations, another way to avoid the stability issue for high-order ΔΣ ADCs is to cascade low-order ΔΣ loops to achieve the equivalent high order noise-shaping. The cascade modulator is also called a multi-stage or MASH (for Multi-stAge-noise-SHaping) modulator [3-5].

Fig.2.11 shows the block diagram of a two-stage modulator. The principle can be described by Eq. 2.18 - Eq. 2.20. The first stage is a ΔΣ modulator with corresponding $STF_1(z)$ and $NTF_1(z)$, and the second stage can also be a ΔΣ modulator or a Nyquist-rate ADC. The first stage quantization error, E_1, is extracted and digitized by the second stage ADC. After being filtered by the noise cancellation filters $NCF_1(z)$ and $NCF_2(z)$, two sub-ADCs outputs are summed together to cancel out the first stage quantization noise at the overall modulator output V. Therefore, the overall accuracy of the converter can be increased. Since all the sub-ADCs in a MASH structure can be implemented using low-order structures, stability can be greatly improved.

$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z) \tag{2.18}$$

$$V_2(z) = -STF_2(z)E_1(z) + NTF_2(z)E_2(z) \tag{2.19}$$

$$V(z) = V_1(z)NCF_1(z) + V_2(z)NCF_2(z) \tag{2.20}$$

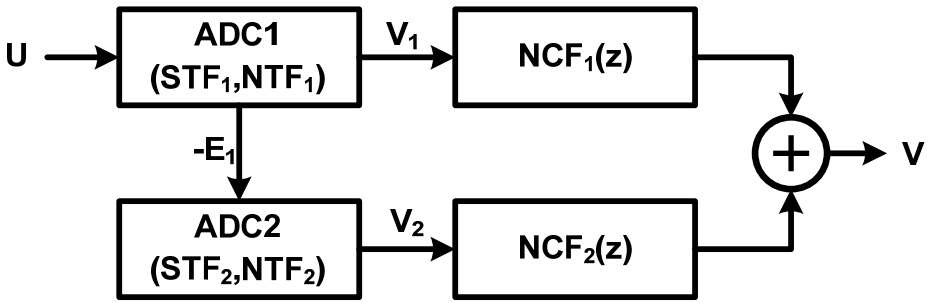


Figure 2.11: The block diagram of two stage modulator.

In order to cancel $E_1(z)$ and achieve high-order noise shaping at the MASH output, the $NCF_1(z)$ and $NCF_2(z)$ should satisfy:

$$NCF_1(z) = STF_2(z) \tag{2.21}$$

$$NCF_2(z) = NTF_1(z) \tag{2.22}$$

Then $$V(z) = STF_1(z)STF_2(z)U(z) + NTF_1(z)NTF_2(z)E_2(z) \tag{2.23}$$

One limitation of the MASH structure is the quantization noise leakage. Ideal cancellation of the first stage quantization noise requires perfect matching between $NCF_1(z)$ and $STF_2(z)$ as well as between $NCF_2(z)$ and $NTF_1(z)$. However, $STF_2(z)$ and $NTF_1(z)$ are implemented in analog-domain, while $NCF_1(z)$ and $NCF_2(z)$ are realized in digital-domain. If the analog circuit is not perfectly designed, Eq. 2.21 and Eq. 2.22 won't match, and $E_1(z)$ will be presented at the output. To minimize noise leakage, the analog and digital circuits need to be matched as closely as possible; otherwise digital calibration techniques must be applied [6-8].

2.2.2 Discrete-time Vs. Continuous-time ΔΣ ADCs

In the previous section, ΔΣ ADCs are classified as single-stage or multi-stage structures. Based on the loop filter circuit implementation, ΔΣ ADCs can also be grouped as discrete-time (DT) or continuous-time (CT). Compared to the CT topology, DT ΔΣ ADCs have been extensively discussed. So, after a brief overview of these two structures, this section will focus the discussion on CT ΔΣ ADCs.

2.2.2.1 Comparison of DT and CT ΔΣ ADCs

For a DT ΔΣ ADC,the CT input signal is sampled before it is applied to the modulator input and the loop filter H(z) is realized using switched-capacitor integrators. Since the whole system is a sampled-data system, it can be analyzed completely in z-domain. However, for a CT ΔΣ ADC, the CT input signal is

applied to the modulator with a CT loop filter H(s), whose output is denoted as y(t), and the quantizer samples y(t) and periodically produces DT output signal V[n], which is fed back through a DAC. So, the CT ΔΣ ADC is in fact a hybrid system. Fig. 2.12 shows the general block diagram of DT and CT ΔΣ modulators.

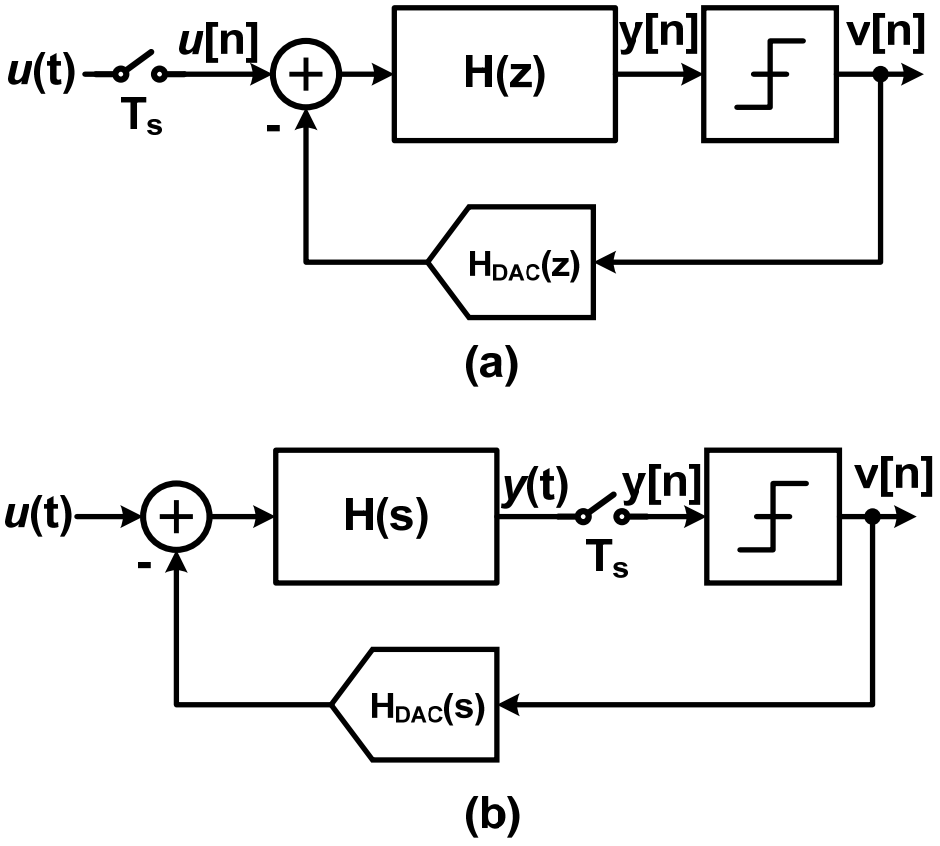


Figure 2.12: The general block diagram of (a) DT (b) CT ΔΣ modulators.

Both DT and CT ΔΣ ADCs have their own pros and cons. For DT ΔΣ ADCs, the design methodology is well developed. The loop filter coefficients depend on the capacitor ratios and can be very accurate, so the performance is robust and no additional tuning circuit is required. Also, the signal bandwidth is automatically scalable with sampling clock and is very flexible for multi-mode applications for different wireless communication systems. The clock jitter sensitivity is also low in DT structures. On the other hand, for high resolution applications, the maximum achievable signal bandwidth of a DT ΔΣ ADC is limited by the settling accuracy

of switched-capacitor stages, and it is difficult to go above 20MHz, even when the double-sampling or time-interleaved technique has been applied [9-10].

Compared to DT ΔΣ ADCs, there are more challenges in the design of CT ΔΣ ADCs. The loop filter coefficients of CT ΔΣ ADCs depend on the product of resistors and integrating capacitors, which have large variations over fabrication process. A tuning circuit is necessary to stabilize the ADC and optimize the performance. Besides the thermal noise and flicker noise, the jitter noise [11-12], which is usually negligible in DT ΔΣ ADCs, can considerably increase the noise floor of CT ΔΣ ADCs and has to be made negligible [13]. For Non-Return to Zero feedback DAC, excess-loop delay compensation is usually required to stabilize CT ΔΣ ADCs [14-15]. On the other hand, CT ΔΣ ADCs are superior to DT structures in terms of power dissipation and speed. First, the sampling of a CT ΔΣ ADC is executed at the input of the quantizer, so both sampling error and the out of band noise aliased into the signal band are suppressed by the high loop gain in the passband. The inherent anti-aliasing filtering can eliminate the need (or at least reduce the requirements) for a front-end anti-aliasing filter. The quiet resistive input also couples less noise to the whole system and reduces the requirements of ADC driver circuits, saving system power dissipation. Also, by continuously integrating the signals, the settling requirement of a CT loop filter is greatly relaxed, and the opamp unity-gain bandwidth requirement can be reduced. So, higher signal bandwidth can be achieved using CT structures. For example, one year ago, National Semiconductor delivered the industry's first 25MHz BW,12bit resolution low power CT ΔΣ ADC [16], which is still unbeatable using DT topologies.

2.2.2.2 Synthesis of CT ΔΣ ADCs

For a DT ΔΣ ADC, the loop filter can be directly synthesized in z-domain because it is a sampled data system. However, the CT ΔΣ ADC is a DT/CT hybrid system, and the loop filter has to be synthesized using different methods. One way

is to directly synthesize the loop filter in the s-domain [17-18], but it may require extensive simulations to ensure the stability and noise shaping performance. The other scheme is to design the CT loop filter by referring to its equivalent DT loop filter model using impulse-invariant transformation (*IIT*) [19]. Here, the *IIT* mapping is preferable to the bilinear transformation because it does not suffer from the frequency wrapping issue for low OSR applications, and thus the synthesized CT modulator preserves the stability and dynamic behavior of its equivalent DT model. Furthermore, since the DT model can be efficiently evaluated using well-developed tools, such as Richard Schreier's ΔΣ toolbox [20], the majority of the CT ΔΣ ADCs use impulse invariant transformation technique.

To find the equivalent DT loop filter H(z) for a given CT loop filter H(s), it is useful to understand the concept of impulse invariant transformation. The block diagrams of CT and DT ΔΣ modulators are re-drawn in Fig. 2.13. The quantizer is replaced with a linear summation block of loop filter output and quantization error. For a ΔΣ modulator, the stability and noise-shaping ability are mostly determined by the feedback loop behavior, so it is illustrative to set both inputs to zeroes, and break the loops around the quantizers.The open-loop diagrams are shown at the bottom of Fig.2.13.

In the CT open-loop diagram, the quantizer output v[n] is a DT quantity, and the DAC converts the DT output sample v[n] to a CT pulse $v_{dac}(t)$. The DAC can be realized using different kinds of waveforms, and NRZ feedback waveform is used here as an example. The pulse is then filtered by CT loop filter H(s) and generates y(t) at the quantizer input, which is then sampled to produce the DT quantizer input y[n]. Therefore, the input and output of both the CT and DT open-loop diagrams are DT quantities. For any input sequences of v[n], if the open loop

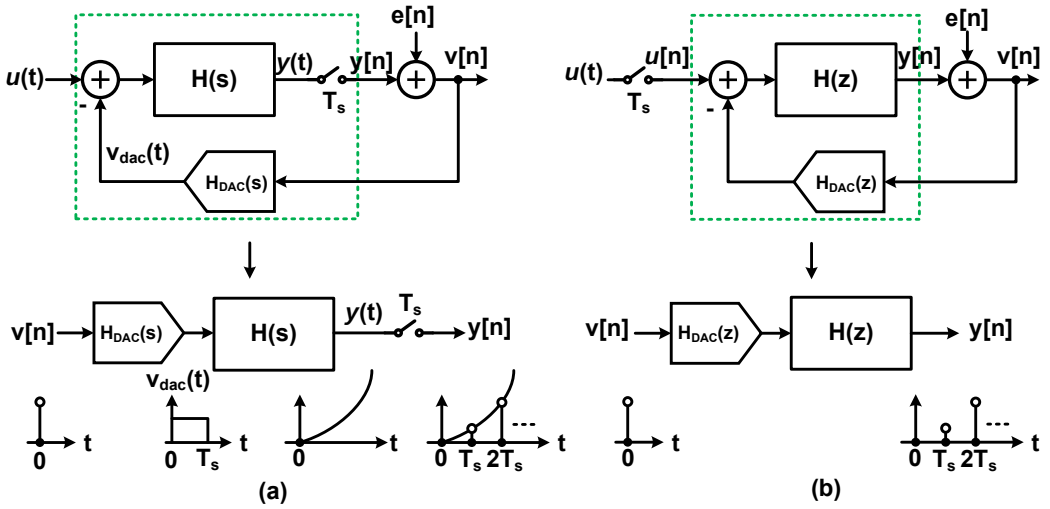


Figure 2.13: (a) CT ΔΣ modulator (b) DT equivalent.

responses of y[n] are identical at the sampling instances:

$$y[n] = y(t)\,|_{t=nT_s} \tag{2.24}$$

then the given CT ΔΣ modulator would have the same response as the corresponding DT ΔΣ modulator. The assumption can be satisfied only if the impulse responses of the open-loop diagrams are identical at each sampling instance. Since $H_{DAC}(z)$ is equal to 1, it comes to the condition:

$$h(n) = L^{-1}\{H_{DAC}(s)H(s)\}|_{t=nT_s} = Z^{-1}\{H(z)\} \tag{2.25}$$

Here, L^{-1} denotes the inverse Laplace transform and Z^{-1} means the inverse z-transform. In the time domain, the impulse response h[n] for the CT open-loop diagram can be given by:

$$h(n) = \left[h_{DAC}(t) * h(t)\right]|_{t=nT_s} = \int_{-\infty}^{+\infty} h_{DAC}(\tau)h(t-\tau)d\tau\,|_{t=nT_s} \tag{2.26}$$

Here, $h_{DAC}(t)$ is the impulse response of $H_{DAC}(s)$, and $h(t)$ is the impulse response of CT loop filter H(s). Since Eq. 2.25 requires the CT and DT open-loop system impulse responses to be the same, the mapping between them is called the

impulse-invariant transformation [21], and the noise transfer function for the CT ΔΣ modulator is given by

$$NTF(z) = \frac{1}{1 + z\left\{L^{-1}\left\{H_{DAC}(s)H(s)\right\}\big|_{t=nT_s}\right\}} \tag{2.27}$$

To achieve the desired *NTF(z)*, the DT loop filter H(z) is readily derived. Using *IIT* mapping, the CT loop filter *H*(*s*) for a given type of DAC waveform can be synthesized to implement the CT ΔΣ modulator with identical behavior. The s-domain equivalents *H*(*s*) for z-domain *H*(*z*) can be found by solving Eq. 2.25 using the modified-z-transform [22] [23], the state-space representation [24], the pole-zero equivalent representation [19] using symbolic math program Maple [25], or by solving the linear equations using the Simulation-Based approach [26].

2.2.2.3 Signal Transfer Function of CT ΔΣ ADCs

The synthesis of a CT ΔΣ ADC from its DT model using *IIT* mapping only keeps the equivalence of the noise transfer function. The signal transfer function is usually not the same. Since the input signal and loop filter output are both continuous signals, it is reasonable to evaluate the STF in s-domain. Fig. 2.14 shows the general block diagram of a CT ΔΣ modulator. L_0(s) denotes the transfer function from U(s) to the input of quantizer Y(s), and L_1(s) the transfer function from modulator output V(z) to Y(s). In the feed-forward structure $L_0(s) = -L_1(s)$.

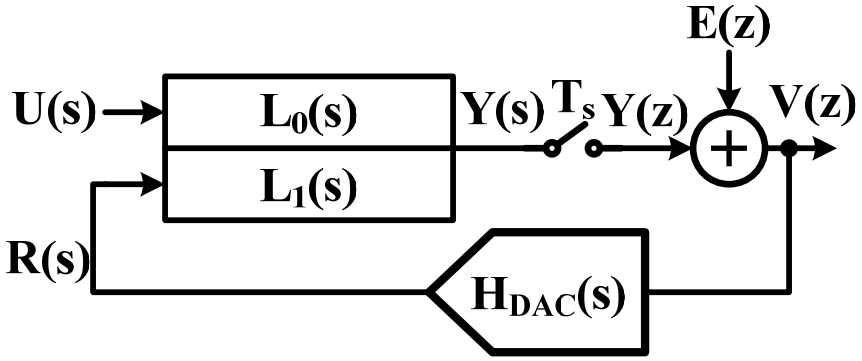


Figure 2.14: General block diagram of a CT ΔΣ modulator.

At the input of the quantizer,

$$Y(s) = U(s)L_0(s) + R(s)L_1(s) \tag{2.28}$$

$$y(t) = L^{-1}(Y(s)) = L^{-1}\{U(s)L_0(s) + R(s)L_1(s)\} \tag{2.29}$$

For simplicity, assuming the quantizer has infinite resolution and so E(z)=0

$$v(t) = \sum_{n=-\infty}^{+\infty} y(t)\delta(t - nT) \tag{2.30}$$

$$V(s) = \int_0^{+\infty} v(t)e^{-st}dt = \sum_{n=0}^{+\infty} y(nT)e^{-nsT} \tag{2.31}$$

$$V(s) = V(z)\big|_{z=e^{sT}} \tag{2.32}$$

For feedback DAC output signal *r*(t),

$$r(t) = h_{dac}(t) * v(t) = \sum_{n=0}^{+\infty} y(nT)h_{dac}(t - nT) \tag{2.33}$$

And $$Y(s) = U(s)L_0(s) + Y(z)\big|_{z=e^{sT}} \cdot H_{DAC}(s)L_1(s) \tag{2.34}$$

Assuming *U*(s) is band-limited and there is negligible aliasing at *Y*(s) due to sampling, which is usually valid because of *DAC*'s low-pass filtering effect, then within the Nyquist frequency

$$Y(s) \approx Y(z)\big|_{z=e^{sT}} = V(z)\big|_{z=e^{sT}} \tag{2.35}$$

Combined with Eq. 2.34,

$$V(s) = Y(s) \approx \frac{L_0(s)}{1 - H_{DAC}(s)L_1(s)}U(s) \tag{2.36}$$

$$STF(s) = \frac{V(s)}{U(s)} = \frac{L_0(s)}{1 - H_{DAC}(s)L_1(s)} \approx L_0(s)NTF(z)\big|_{z=e^{sT}} \tag{2.37}$$

Here, $$NTF(z) = \frac{1}{1 - z\left\{L^{-1}\{H_{DAC}(s)L_1(s)\}\big|_{t=nT_s}\right\}} \tag{2.38}$$

2.2.2.4 Design Issues of CT ΔΣ ADCs

As is mentioned in section 2.2.2.1, the successful design of CT ΔΣ ADCs, with good robustness and high resolution, requires carefully dealing with many issues, such as time-constant variation, high jitter sensitivity and excess-loop delay etc. These issues will be discussed in this section, and corresponding solutions or design guidelines are provided.

2.2.2.4.1 Integrator Time-Constant Variation Effect

In general, there are three fundamental circuit blocks in a ΔΣ ADC, including the loop filter, the quantizer and the feedback DACs. The loop filter usually contains the integrators and the adder (in the feed-forward structure). Figs. 2.15. a and b show the commonly used integrator circuit diagrams of CT and DT ΔΣ ADCs.

For DT ΔΣ ADCs, the integrator is realized as a delayed or non-delay switched-capacitor integrator. The sampling clock frequency has little effect on the integrator transfer function, and the integration gain depends on the ratio between C_{in} and C_f. 10-12bit matching accuracy can be easily achieved by most up-to-date processes, so the integrator gain variation is usually not an issue. However, this is not the case in CT ΔΣ ADCs. The loop filter is implemented using active-RC or

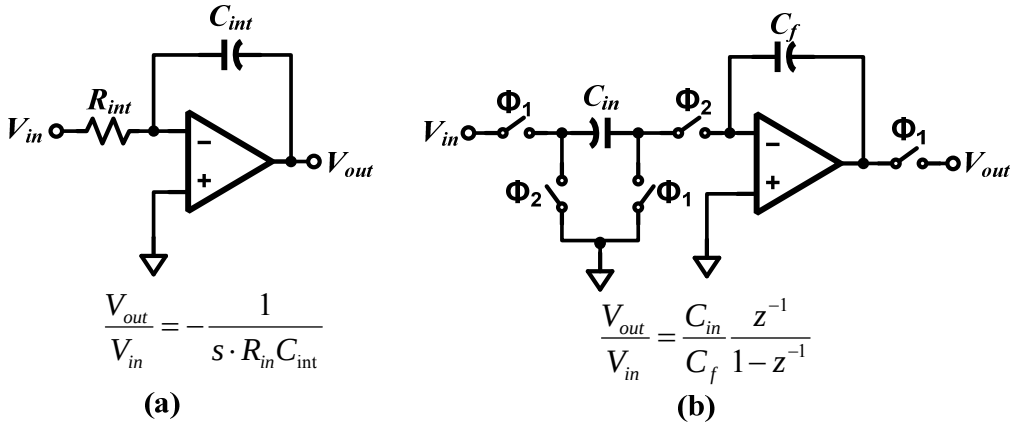


Figure 2.15: (a) Active-RC integrator for CT ΔΣ ADC (b) Switched-capacitor delayed integrator for DT ΔΣ ADC.

Gm-C integrators and the transfer function is given as

$$\frac{V_{out}}{V_{in}} = -\frac{k_{\text{int}}}{s \cdot T_s} \tag{2.39}$$

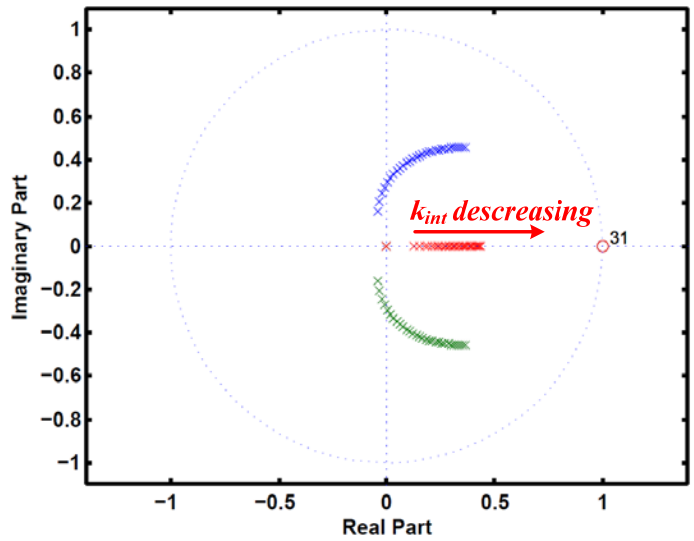
Here, T_s represents the update period of the modulator output, and the gain of the integrator is

$$k_{\text{int}} = \frac{T_s}{R_{in} C_{\text{int}}} \tag{2.40}$$

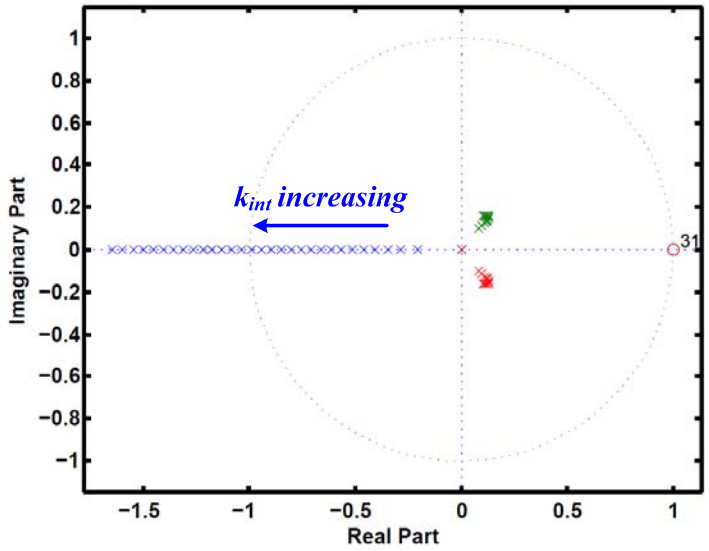
T_s is usually deterministic in a mono-rate ΔΣ ADC, while the values of R_{in} and C_{int} are uncorrelated and widely spread, which thus induces big variations in k_{int}.

The ΔΣ modulator performance degradation due to the k_{int} deviation can be analyzed in two ways. First, the integrator gain determines the coefficients of the loop filter. The gain of the loop filter will also change with k_{int}. Since both the input signal and feedback signal pass through the loop filter, the signal transfer function, as well as the noise transfer function, will also be changed with the variation. Usually, a smaller time constant means more aggressive noise-shaping and thus higher SQNR, but the input signal dynamic range is also reduced because of the increased signal gain. The overall dynamic range is decreased. On the other hand, a larger time constant reduces the loop gain, and the noise-shaping ability. SQNR is also decreased because of the increased inband quantization noise and reduced signal power at the modulator output. The second effect of integrator gain variation is the reduced modulator stability. Since the CT loop filter is changed, the equivalent DT NTF(z) is also changed. Using a 3rd order CT modulator as an example, the DT NTF(z) pole and zero trajectories within ±30% RC time constant variation have been checked and plotted in Figs. 2.16. a and b. When the RC time constant is larger than the desired value, the poles will move from the origin to the right part of the unit-circle, but they still keep within the unit-circle, so the modulator maintains stability with reduced noise shaping ability.However,if the RC time constant is smaller than the desired value, which means k_{int} is greater than

ideal value, then the two poles will move from the origin but still keep within the unit-circle, while the other pole will move along the negative real axis and finally out of the unit-circle when k_{int} is 16% higher than the ideal value. The modulator becomes unstable. By checking a higher order modulator, the critical value of k_{int} for stability is even smaller.



(a) $k_{int} < k_{int,ideal}$



(b) $k_{int} > k_{int,ideal}$

Figure 2.16: NTF pole/zero trajectory with k_{int} (a)0 to -30%(b)0 to 30% variation.

To optimize the modulator performance and maintain robustness at the same time, different tuning schemes [27][28], by tuning capacitor or resistor, have been successfully applied in CT ADC design to adjust the time constant to the desire value.

2.2.2.4.2 Clock Jitter Sensitivity

Compared to DT ΔΣ ADCs, CT ΔΣ ADCs are very sensitive to the sampling clock uncertainties. The clock jitter appears at the output data stream as a noise whose spectral density can surpass the quantization noise and even wideband thermal noise, limiting the overall SNR in high performance modulators. For a general single-loop CT structure, as is shown in Fig. 2.17, the sampling is executed at the input of the quantizer and the feedback DAC. The sampling error at the input of the quantizer will be attenuated by the loop gain, and hence it is usually negligible for moderate jitter levels. However, the timing uncertainties of DAC will generate a wrong position of feedback pulse and also inaccurate duration time. The resulting errors will directly present at the modulator output, and significantly degrade the SNR.

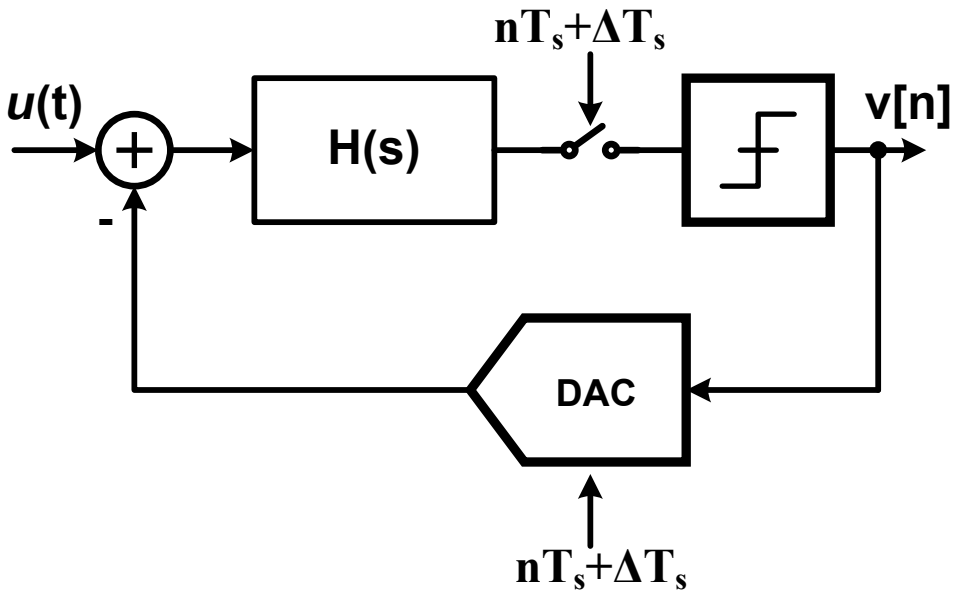


Figure 2.17: Single-loop CT ΔΣ modulator with clock timing uncertainties.

In general, feedback DAC waveform represents the way of charge transferring from modulator output to the loop filter H(s).The pulse will be integrated at least once in the loop filter before sampling. So, the error in the area of the feedback pulse for every sampling period is meaningful and determines the jitter sensitivity.

Compared to CT ADCs using switched-capacitor feedback DAC [29] or pulse-shaped feedback DAC [30], CT ADCs using switched-current feedback DAC, such as NRZ or RZ feedback pulse, have more critical jitter sensitivity requirement. Therefore, discussion here focuses on the switched-current DACs.

For a NRZ feedback DAC, the error area during each cycle is

$$\Delta A[n] = (V[n] - V[n-1]) \cdot \Delta T_s[n] \tag{2.41}$$

If it is normalized to the ideal sampling period T_s, the equivalent error voltage $e_n[n]$ is

$$e_n[n] = \frac{\Delta A[n]}{T_s} = (V[n] - V[n-1]) \cdot \frac{\Delta T_s[n]}{T_s} \tag{2.42}$$

If the clock jitter and modulator output are statistically independent, the error voltage variance is

$$\sigma_{e_n}^2 = \frac{1}{T_s^2} \sigma_{\Delta T}^2 \cdot \sigma_{dV}^2 \tag{2.43}$$

Here, $\sigma_{\Delta T}^2$ is the clock jitter noise power and σ_{dV}^2 represents the variance of dV[n] in Eq. 2.41. Since the modulator output contains the input signal filtered by the signal transfer function and the quantization noise filtered by noise transfer function, the jitter is clearly related to the input signal. But in low pass ΔΣ ADCs with high oversampling ratio, the input signal varies slowly and clock jitter noise introduced by the quantization noise is more dominant than by the input signal, especially with low resolution quantizer. For simplicity, let

$$dV(z) \approx \mathrm{NTF}(z)(1-z^{-1})\mathrm{E_q}(z) \tag{2.44}$$

and the variance is

$$\sigma_{dV}^2 = \frac{\sigma_{E_q}^2}{2\pi}\int_0^{2\pi} |1-e^{-j\omega}|^2 |NTF(e^{j\omega})|^2 d\omega \tag{2.45}$$

Here, $\sigma_{E_q}^2$ represents the quantization noise power. The jitter noise power at modulator output is

$$\sigma_{e_n,NRZ}^2 = \frac{\sigma_{\Delta T}^2}{T_s^2}\cdot\frac{\sigma_{E_q}^2}{2\pi}\int_0^{2\pi} |1-e^{-j\omega}|^2 |NTF(e^{j\omega})|^2 d\omega \tag{2.46}$$

For a RZ or HRZ feedback DAC, the DAC is switched on only half cycle at each sampling period and then reset to zero, so both clock rising and falling edges contribute to the error area and is

$$\Delta A[n] = V[n]\frac{T_s}{T_{RZ}}\left(\Delta T_r[n] + \Delta T_f[n]\right) \tag{2.47}$$

T_{RZ} is the duration time for RZ waveform in each cycle, if it is normalized to ideal sampling period T_s, the equivalent error voltage $e_n[n]$ is

$$e_n[n] = \frac{\Delta A[n]}{T_s} = V[n]\frac{\Delta T_r[n] + \Delta T_f[n]}{T_{RZ}} \tag{2.48}$$

Again, if clock jitter and modulator output are statistically independent, the error voltage variance is

$$\sigma_{e_n}^2 = \frac{2}{T_{RZ}^2}\sigma_{\Delta T}^2 \cdot \sigma_V^2 \tag{2.49}$$

Under this case, the variance σ_V^2 depends on both filtered input signal power and quantization noise power. In the passband, the signal transfer function is usually approximately equal to 1.Assume the input signal is uncorrelated to quantization noise, then the jitter noise at modulator output is

$$\sigma_{e_n,RZ}^2 = 2\frac{\sigma_{\Delta T}^2}{T_{RZ}^2}\left(P_{sig} + \frac{\sigma_{E_q}^2}{2\pi}\int_0^{2\pi} |NTF(e^{j\omega})|^2\, d\omega\right) \tag{2.50}$$

Eq. 2.46 and Eq. 2.50 suggests some guidelines for jitter noise reduction: First, a cleaner clock source and multi-bit quantizer can reduce the jitter sensitivity for the modulator; Second, by modifying the *NTF(z)* to minimize the variance of σ_{dV}^2 [31], the jitter requirement for modulator using NRZ DAC can be further relaxed ; Third, a more conservative NTF(z) is also helpful to reduce the jitter noise for RZ and HRZ DAC, but they also generate considerable large signal-dependant jitter noise, which can even become dominant for large input signal. So, for wideband high-performance CT ΔΣ ADC design, a NRZ DAC is preferable to a RZ or HRZ DAC for introducing less jitter noise to the modulator.

2.2.2.4.3 Excess Loop Delay

As discussed in section 2.2.2.2, for a given feedback DAC waveform, the CT loop filter can be synthesized from its equivalent DT loop filter using *IIT* mapping. The assumption is that there is no any delay at the feedback path. However, it is impossible in the real circuit due to the finite speed of transistors. The overall delay in the feedback path, also named as excess loop delay, is usually introduced by the quantizer, dynamic element matching (DEM) logics, DAC switches and loop filter.

In a CT ΔΣ ADC, the loop filter continuously integrates the feedback signal, and the synthesized loop filter coefficients become inaccurate when the excess loop delay is considered. The deviation from ideal loop filter will degrade the noise-shaping ability and stability. It is even worse for wideband applications, where the half-cycle or full-cycle delay is usually introduced ahead of the feedback DAC to absorb the signal-dependent delay of the quantizer and the dynamic element matching (*DEM*) logic delay. A high-order modulator becomes unstable if the excess loop delay is not compensated. For a 2nd order CT ΔΣ ADC, Fig. 2.18 shows the loop filter impulse responses with zero delay, $0.1T_s$ and $0.5T_s$ loop delay. The excess loop delay postpones the output response of CT loop filter

and generates sampling error at the end of each cycle, which thus increases the inband noise of the modulator. The corresponding output spectrums are shown in Fig. 2.19.

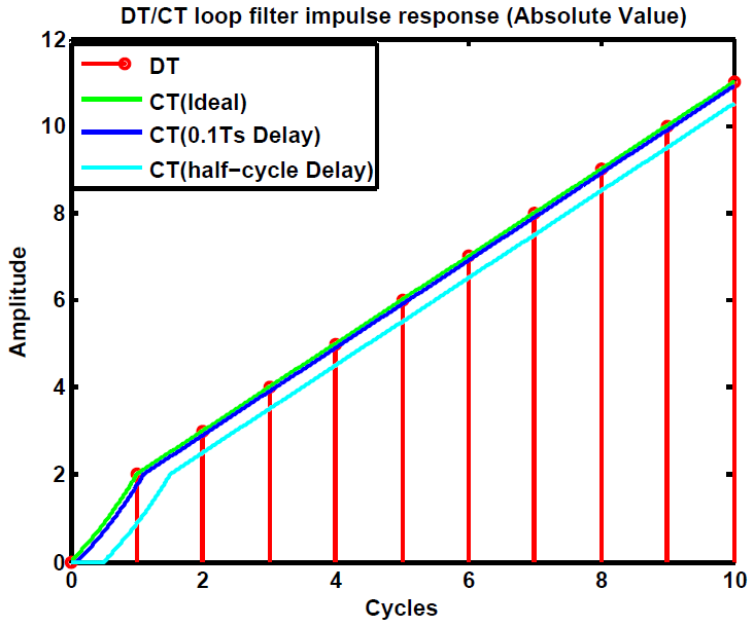


Figure 2.18: Excess loop delay effect on CT loop filter impulse response.

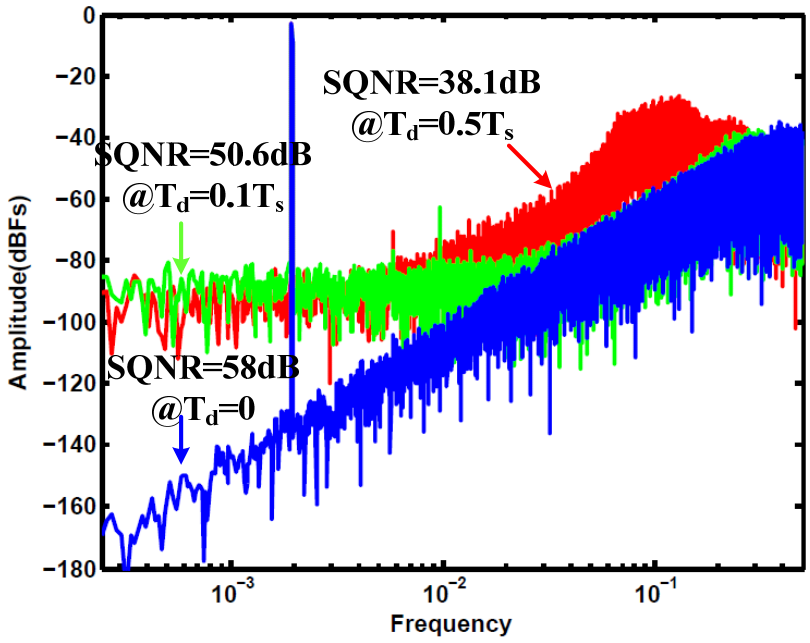


Figure 2.19: Simulated spectrum with excess loop delay (*OSR*=16, *nLev*=5, *L*=2).

To compensate the excess loop delay, the loop filter coefficients should be tuned [19] to match the desired response. For *RZ* or *HRZ* DAC, the loop filter order doesn't change within half-cycle excess loop delay, and hence directly tuning the coefficients is enough to satisfy the requirement. However, for the *NRZ* feedback DAC, the excess loop delay increases the order of equivalent DT loop filter by one. Therefore, additional independent feedback branch should be applied for the tuning [15]. After the half cycle loop delay is compensated, the correct loop filter impulse responses using *RZ* and *NRZ* DAC are shown in Fig. 2.20. Although output responses are different, the sampling values at the end of each cycle are the same. Close-loop stability and noise-shaping ability are guaranteed.

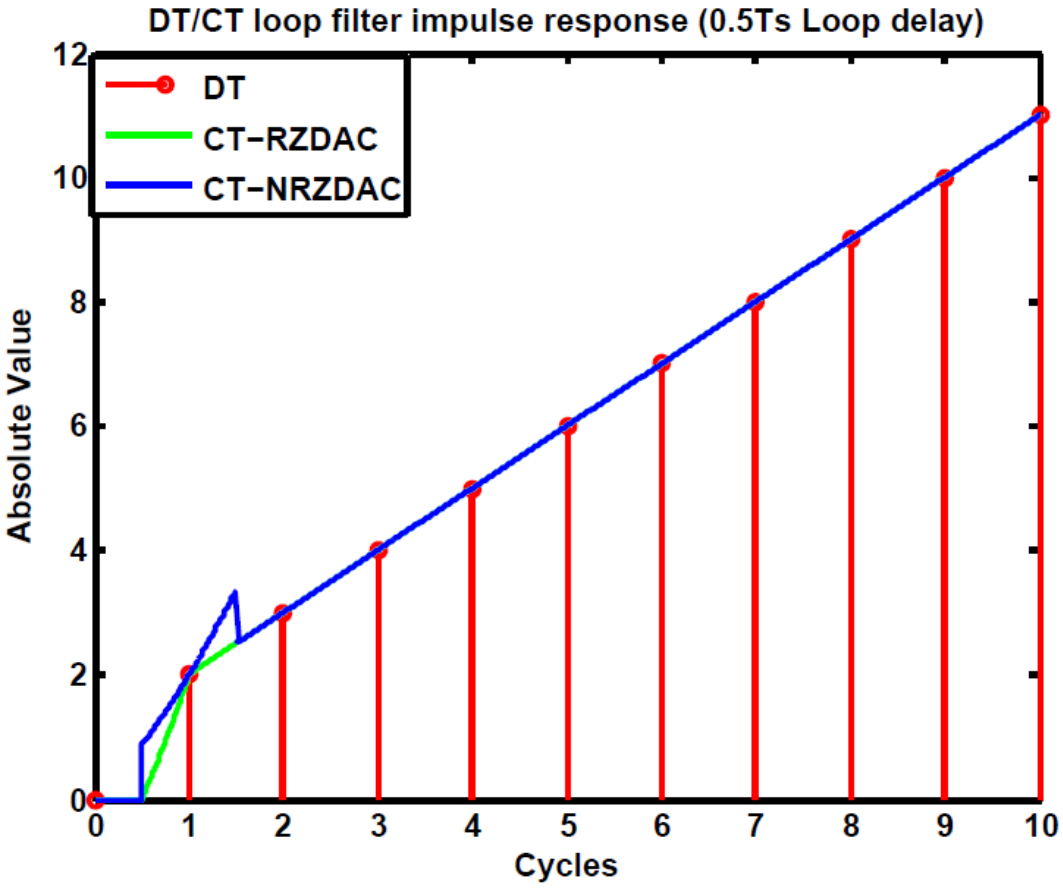


Figure 2.20: The loop filters impulse responses with compensated excess loop delay.

Besides above system-level design issues, many other circuit non-ideal effects also degrade modulator performance, such as amplifier finite gain and bandwidth, feedback DAC mismatch and quantizer delay, hysteresis and metastability,etc. All of them require careful circuit and layout design techniques.

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CHAPTER. 3 A 2.5 MHz BW, 89 dB SFDR AND 78 dB SNDR DELTA-SIGMA MODULATOR USING DYNAMICALLY BIASED AMPLIFIERS

A new dynamically biased circuit is proposed to implement a 13-bit delta-sigma modulator with a 2.5 MHz signal bandwidth. It uses the low-distortion architecture, and hence the amplifier linearity requirements are greatly relaxed. Its noise-coupled and time-interleaved structure further decreases the power consumption. The prototype chip was fabricated in a 0.18 um CMOS technology. Experimental results show 89 dB SFDR and 78 dB SNDR for a 60 MHz clock rate. With a 1.6 V supply, the power dissipation is 19.2 mW.

3.1 Introduction

Discrete-time delta-sigma (ΔΣ) A/D converters with 12 to 14 bits resolution and 1 to 5 MHz signal bandwidth find many applications in xDSL, wireless and wire-line communication systems. Switched-capacitor (SC) circuits are often used to realize the fundamental blocks of discrete-time ΔΣ ADCs. In conventional design, each opamp in the switched-capacitor circuits is biased with a constant current source, which is dimensioned to satisfy the slew rate and settling accuracy requirement under worst-case conditions. This is wasteful under other operation conditions. To achieve low power consumption, various dynamically biased schemes [1]-[3], such as tail-biased dynamic stages, clocked-current dynamic scheme and switched-capacitor sampling network dynamic biased scheme, etc., have been proposed. However, the applications of these schemes are limited by their narrow signal bandwidth or large harmonic distortion.

In this chapter, we present a 2.5 MHz bandwidth, 89 dB SFDR, 78 dB SNDR low power ΔΣ modulator using a new dynamically biased telescopic amplifier for the input integrator [4], [5]. Using the proposed dynamic biasing technique, the bias current of the stage will increase with the square of the differential input

signal. Noise coupling [6] and time interleaving, combined with the low-distortion architecture [7], have been used to achieve good linearity performance with wide signal bandwidth.

This chapter is organized as follows. Section 3.2 describes the operation principle of the proposed dynamic biasing scheme and shows its implementation in a ΔΣ ADC. Section 3.3 discusses the low-distortion ΔΣ modulator architecture using the proposed dynamic biasing scheme. Section 3.4 describes the detailed circuit realization of the prototype modulator. Section 3.5 presents the measurement results, and section 3.6 contains the conclusions.

3.2 The proposed dynamic biasing scheme

3.2.1 Dynamically Biased Integrator

Fig. 3.1 shows the partial circuit diagram of a single-ended dynamically-biased switched-capacitor integrator. During the input sampling phase (Φ_1=1), the input capacitor C_s is charged to input signal level V_{in}, while during the following integration phase (Φ_2=1), C_s is discharged, and its charge is transferred to the integration capacitor C_{int}. The bias current of the opamp is the sum of a fixed bias current I_{bias} and the variable bias current flowing through M_3, which is controlled by V_{in} during the sampling phase, and held constant during the integration phase. If V_{in} is large, and hence the transferred charge into C_{int} is large, M_3 will dynamically increase the total bias current. Since the current detection path is very fast, the process is suitable for high clock frequency applications.

A straightforward extension of Fig. 3.1 to differential operation is illustrated in Fig. 3.2. For differential input signals represented by

$$V_{IP} = V_{cmi} + V_{diff} \tag{3.1}$$

$$V_{IN} = V_{cmi} - V_{diff} \tag{3.2}$$

Assume that V_{IP} and V_{IN} swing significantly from their common-mode level $V_{cmi,}$ but the associated transistors still stay in their saturation regions. Assuming

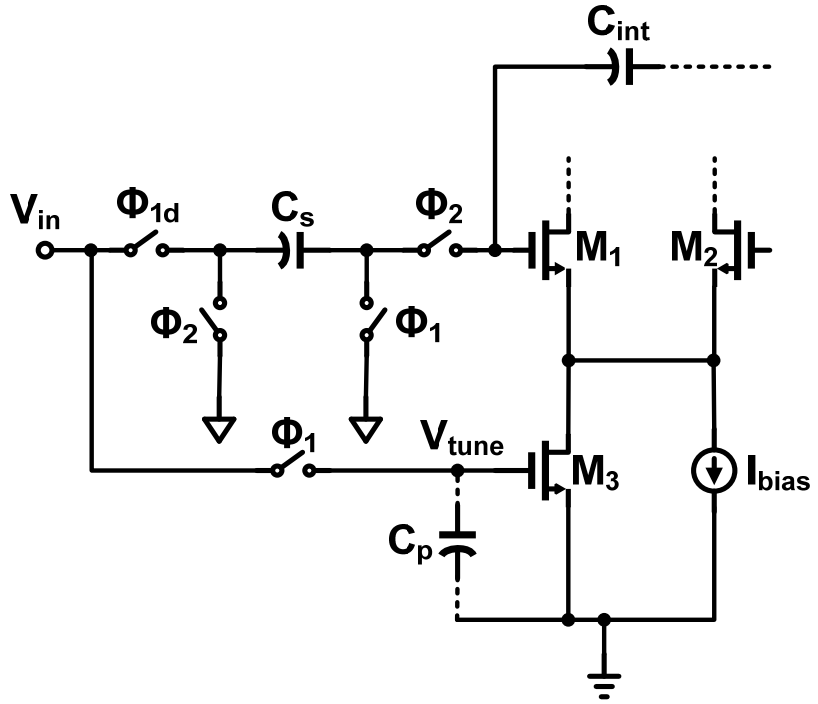

Figure 3.1: Partial circuit diagram of a single-ended dynamically-biased integrator.

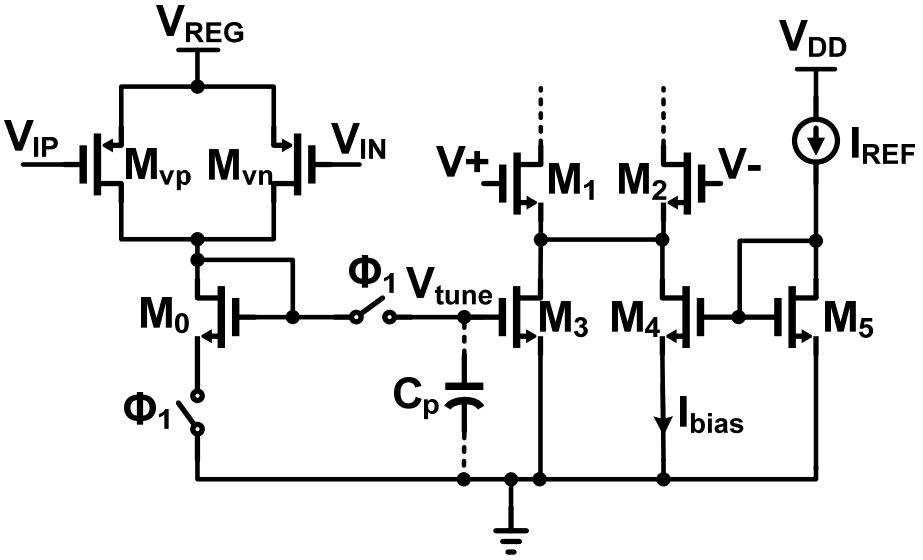

Figure 3.2: Dynamic biasing scheme for a differential input stage.

square-law characteristics, the current flowing through M_0 and M_3 can be expressed as

$$I = K \times (V_{REG} - V_{cmi} - V_{th})^2 + K \times V_{diff}^2 \tag{3.3}$$

Here, $K = \mu C_{ox} \frac{W}{L}$ and V_{diff} is the signal swing of the input signals V_{IP} or V_{IN} from the common-mode level V_{cmi}, as shown in Eqs. 3.1-3.2. I contains a constant term and a signal-dependent tuning current. Both can be chosen so as to meet the specifications of the stage. If $V_{REG} = V_{cmi}+V_{th}$, the fixed current will be much smaller than the tuning current, and the tuning range is extended. For a slew-rate limited opamp, the total bias current at integration phase should be large enough to provide the slew current into the opamp's load capacitor C. This gives the condition

$$I_{bias} + \frac{K}{2} \times V_{diff}^2 > \frac{2C \times V_{diff}}{t_{slew}} \tag{3.4}$$

Here, t_{slew} is the allocated slew time for the opamp. Inequality of Eq. 3.4 can be satisfied by a real value of V_{diff} only if I_{bias} and K meet the condition

$$KI_{bias} > 2C^2 / t_{slew}^2 \tag{3.5}$$

This is the basic design equation for the stage.

3.2.2 *Dynamic biasing implementation for a ΔΣ modulator*

In the input integrator of a delta-sigma modulator, as shown in Fig. 3.3, the total charge transferred during the integration phase depends not only on the input signal, but also on the *DAC* feedback voltage. Hence, the current detection circuit is required to extract the difference between these two voltages. Fig. 3.4 shows the circuit realization for this task. When Φ_1=1, the differential input signals from the ADC input and the feedback DAC are subtracted at nodes A and B by capacitors *C1*-*C4*. The voltages at node A and B can be expressed as

$$V_A = \frac{V_{SIGP} - V_{DACP}}{2 + r} + V_{cmi} \tag{3.6}$$

$$V_B = \frac{V_{SIGN} - V_{DACN}}{2 + r} + V_{cmi} \tag{3.7}$$

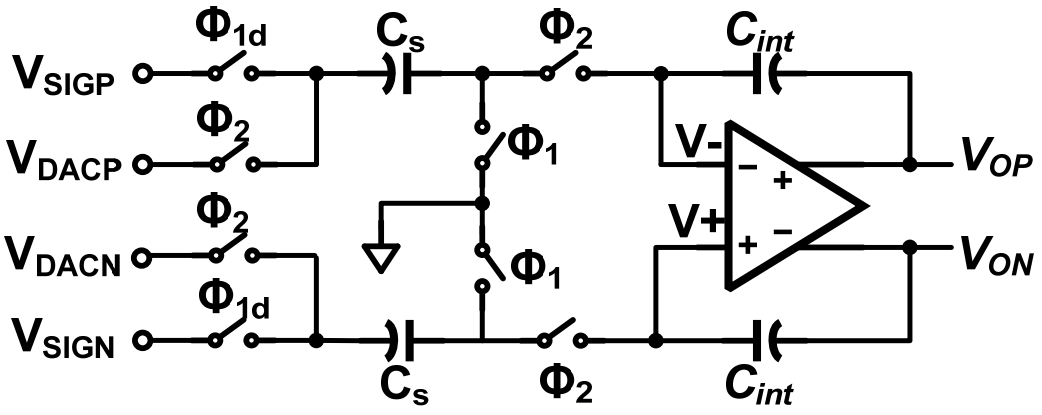

Figure 3.3: The input integrator circuit of a ΔΣ modulator.

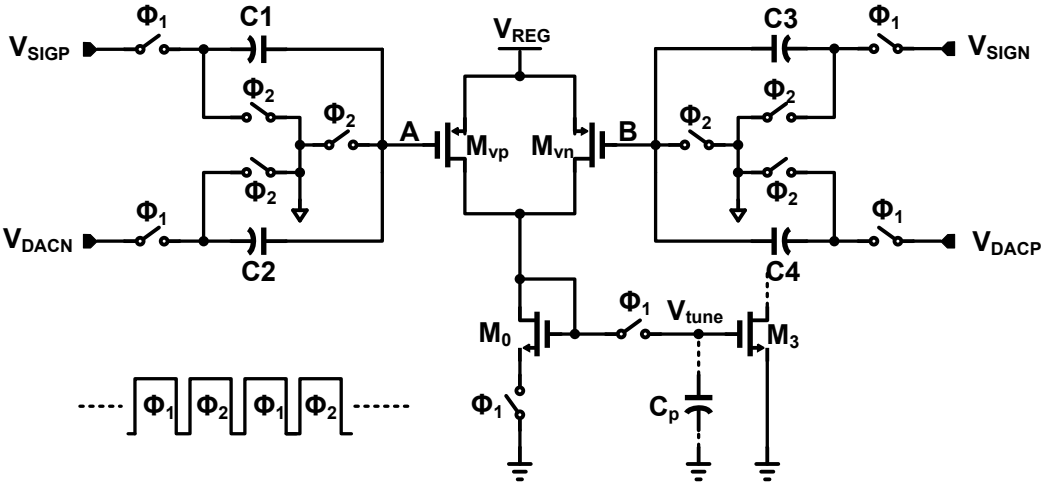

Figure 3.4: The dynamic biasing circuit for an integrator with two input branches.

Here, $r = Cp/2C$, and Cp is the parasitic capacitance at nodes A and B. The current flowing through M_0 and M_3 will track the voltage variation at nodes A and B, and the input signal attenuation can easily be compensated by adjusting the current ratio between M_0 and M_3. When Φ_2=1, C_1 through C_4 are reset to prevent memory effects. The voltage V_{tune} is held by the M_3 transistor's parasitic capacitance, and hence the opamp's bias current keeps constant.

The dynamic current detection circuit shown in Fig. 3.4 requires that the input signal and the DAC feedback signal be available at the same time. A practical structure of ΔΣ modulator is the CIFB topology described in [8]. An example

circuit realization is shown in Fig. 3.5. (For different modulator architectures, the clock timing for the summation capacitors of current detection circuit might need to be changed.)

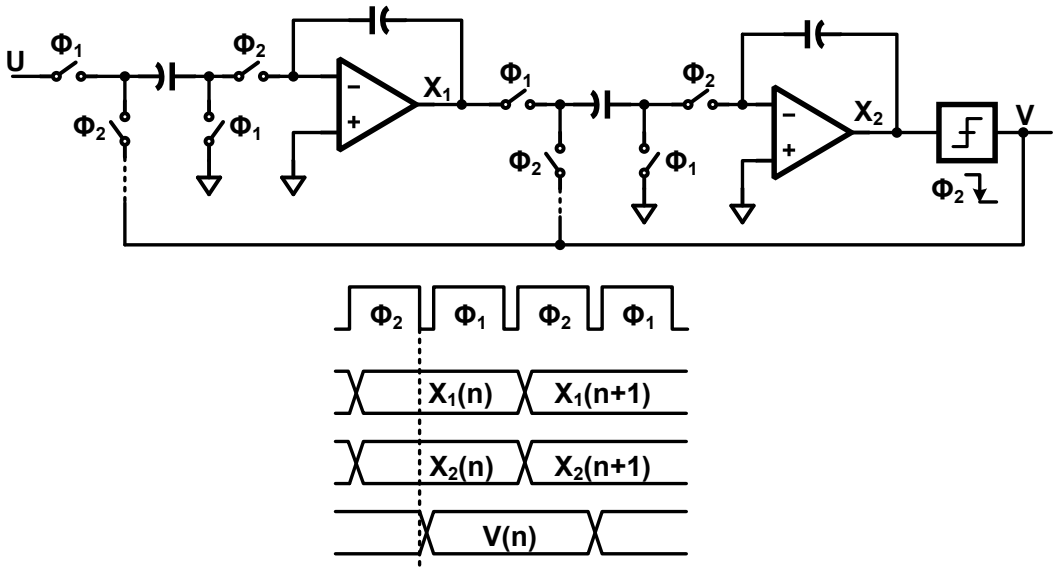

Figure 3.5: A second-order dynamic-biasing ΔΣ modulator.

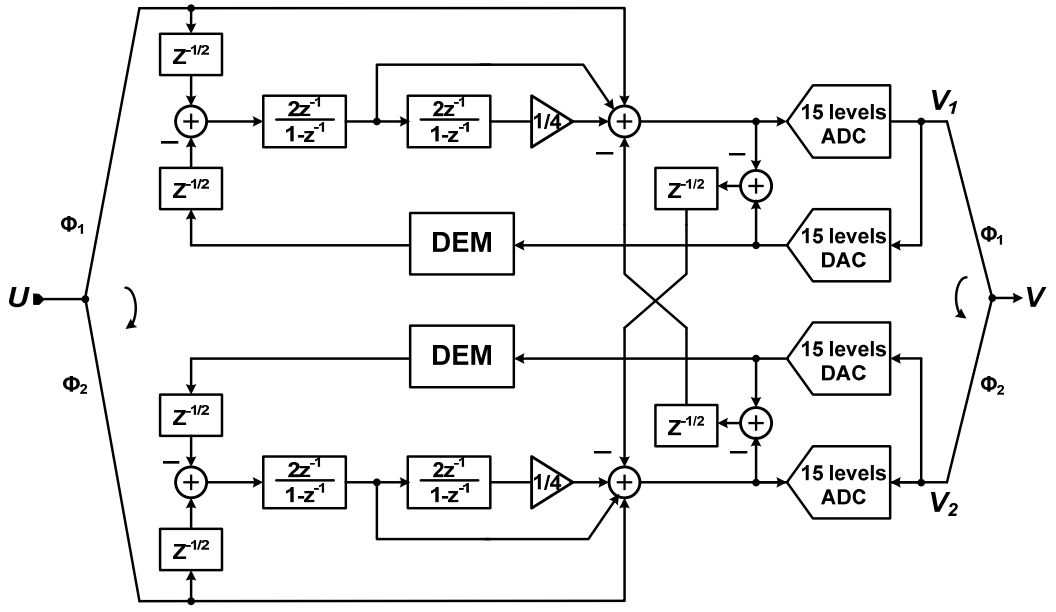

Figure 3.6: The block diagram of the prototype ΔΣ ADC.

3.3 Modulator Architecture

The proposed dynamic-biasing scheme was applied to a two-channel noise-coupled time-interleaved delta-sigma modulator [9]. Fig. 3.6 shows the system-level block diagram. Each channel contains a second-order low-distortion modulator with a multi-bit quantizer. The time-interleaved sampling doubles the effective sampling rate to 120 MSample/s for the 60 MHz clock rate, and introduces two notches at the Nyquist frequency in the noise transfer function. Hence, the quantization noise power at the Nyquist frequency is greatly attenuated, and the noise folding into the signal band due to the channel mismatches is negligible. The second-order modulator's quantization noise at each channel is extracted and injected into the loop of the other channel's modulator. This cross-coupling between the two channels raises the effective noise-shaping order from two to three, without affecting the loop stability. In addition, the injected noise acts as a dither signal, and reduces the in-band idle tones and harmonic distortion. The bias current of the telescopic opamp in the input integrator is dynamically controlled using the proposed scheme. By introducing a half-cycle delay into both the input signal path and the DAC feedback path, the low distortion characteristic is maintained. The extra phase is used for the current detection to dynamically bias the input integrator. Thus, the bias current depends only on the shaped quantization noise, and the linearity requirement of the loop filter is greatly relaxed. The dynamic element matching (DEM) timing, which is critical for conventional low-distortion multi-bit architecture, is also relaxed with the introduced half-cycle delay.

3.4 Circuit Implementation

Fig. 3.7 shows the block diagram of the input integrator for a single-channel ΔΣ modulator. It contains two sets of alternating sampling capacitor circuit blocks to realize the half-cycle delay required in the proposed modulator architecture. Both

the sampling and integration operations of the integrator are executed during Φ_1 phase by alternating between the two identical switched-capacitor blocks.

The dynamic-biasing current sensing (DBCS) circuit is shown in Fig. 3.8. The current sensing block extracts the signal difference between the ADC input and the DAC feedback paths during Φ_2 phase. The operation of current sensing block starts from the reset state. Nodes A and B are reset to clear up the memory during Φ_1 phase and to get ready for the next cycle of operation. At the same time, the

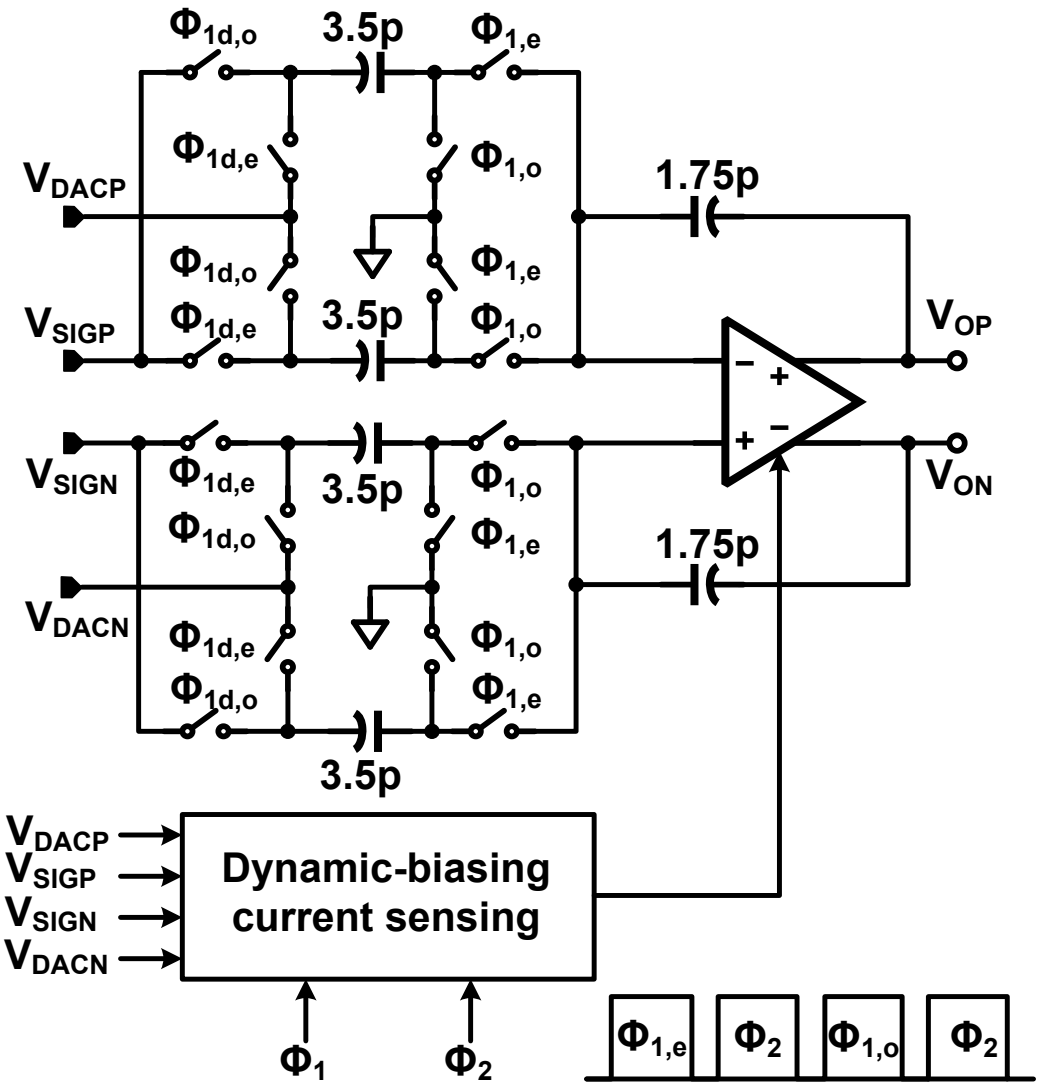

Figure 3.7: The block diagram of the dynamically-biased integrator.

input signal is sampled during the Φ_1 phase, and then a half-cycle delay is introduced before the charge transfer during the Φ_2 phase in this current detection branch. During the next Φ_2 phase, the DAC feedback signal is applied to the delay-free current detection branch to get the proper signal difference between the two paths. Thus, when the M_{SW1} and M_{SW2} switches open at the falling edge of Φ_2 phase, the signal difference information is sampled on the gate of M_3, and the current flowing through M_3 is held to dynamically bias the input integrator during the next Φ_1 phase.

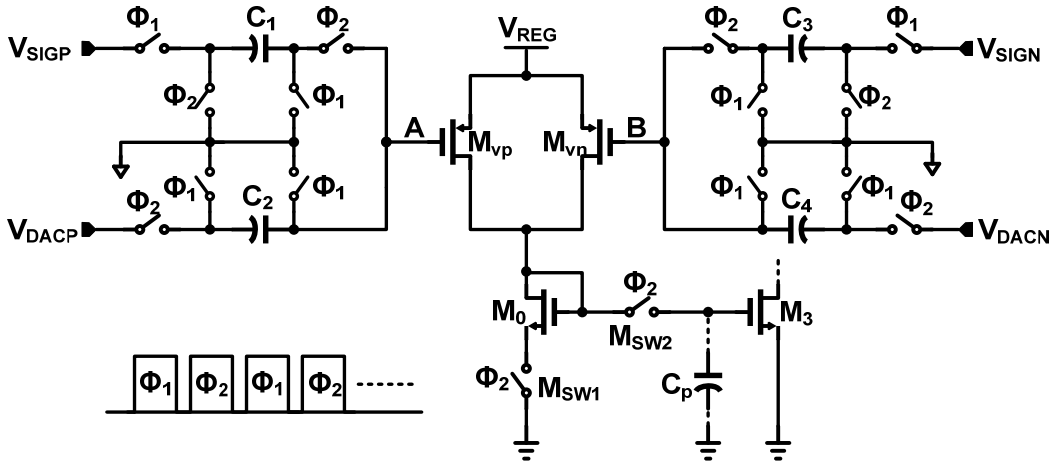

Figure 3.8: The dynamic-biasing current sensing circuit for the time-interleaved low-distortion ΔΣ modulator.

The circuit diagram of the dynamically-biased telescopic opamp is illustrated in Fig. 3.9. To balance the nMOS tail current and the pMOS source current, two additional pMOS current sources, controlled by $M_{6,\,7}$ and $M_{10,\,13}$, are added. Thus, the current flowing through M_{14} and M_{17} can also track the integrator input, and it balances the current through M_3. By properly sizing the transistors, the output common-mode voltage variation due to the unbalanced current in the dynamically-biased opamp can be minimized, and the bandwidth requirement for the common-mode feedback loop is relaxed.

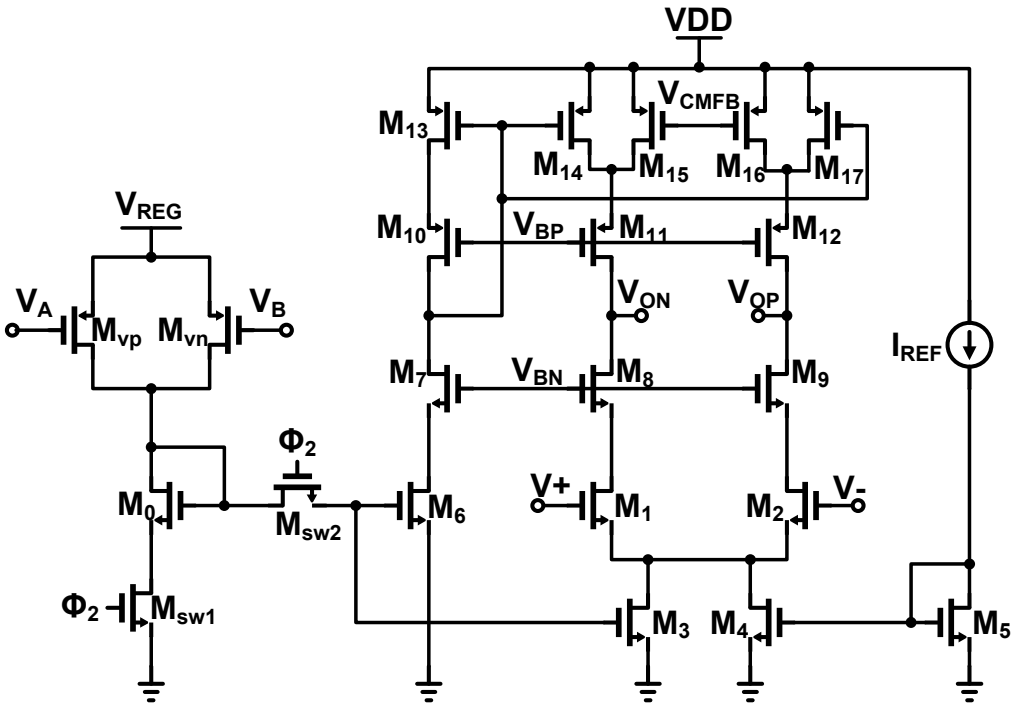

Figure 3.9: The dynamically-biased telescopic amplifier.

For the other channel modulator, the circuit implementation of the integrator is identical, except that the operations during the Φ_1 and Φ_2 phases are interchanged. So, the dynamic biasing current is detected during the Φ_1 phase, while the input signal sampling and integration are executed during the Φ_2 phase. Fig. 3.10 shows the switched-capacitor circuit implementation of the whole modulator. The dynamic biasing scheme was applied to the first integrator only, to prove the effectiveness of the proposed scheme. A conventional telescopic opamp with fixed bias was employed for each second integrator and offset-compensated active adder. Bootstrapped switches [10] were used for the critical input sampling switches to achieve linear sampling. The quantizer is composed of two-stage preamplifier, a track and latch, and an SR latch [11], [12]. The two-stage preamplifier with input offset cancellation speeds up the signal amplification, suppresses the kick-back noise, and reduces the offset of the following stages by its gain. The quantizer thresholds for both modulators were generated with a resistor string. Conventional data-weighted averaging (DWA) [13] with a 4-stage

logarithmic shifter was applied to dynamically shape the mismatch errors of the 15-level DAC. Fig. 3.11 illustrates the non-overlapped clock signal generator. Even and odd phase clock signals were used to realize the required delay to accommodate the proposed dynamic biasing scheme. A more detailed circuit description of the circuit blocks (without dynamic biasing) can be found in [9].

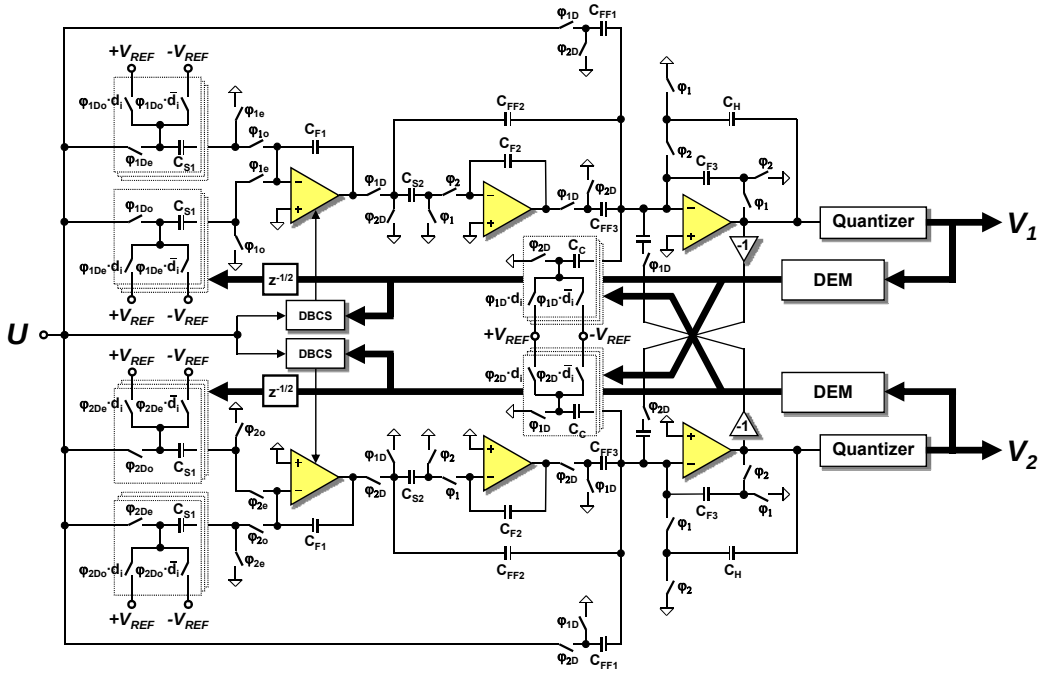

Figure 3.10: The switched-capacitor circuit implementation of the modulator.

3.5 Measurement Results

The prototype chip was fabricated in a double-poly four-metal 0.18 μm CMOS technology. The die photograph is shown in Fig. 3.12. The core area is around 3.66 mm^2. The supply voltage of the chip was set to 1.6 V, the supply voltage of the dynamic-biasing current sensing circuit (V_{REG}) was set to 1.25 V, the input common-mode voltage of the signal was set to 0.9 V and the output common-mode level of the circuit was set to 0.955 V. External voltages V_{REFP} and V_{REFN} generated by on-board drivers were used as the reference voltages of the internal

DAC. The sampling clock frequency of each channel modulator was 60 MHz, and the output data rate after time-interleaving was 120 MSample/s

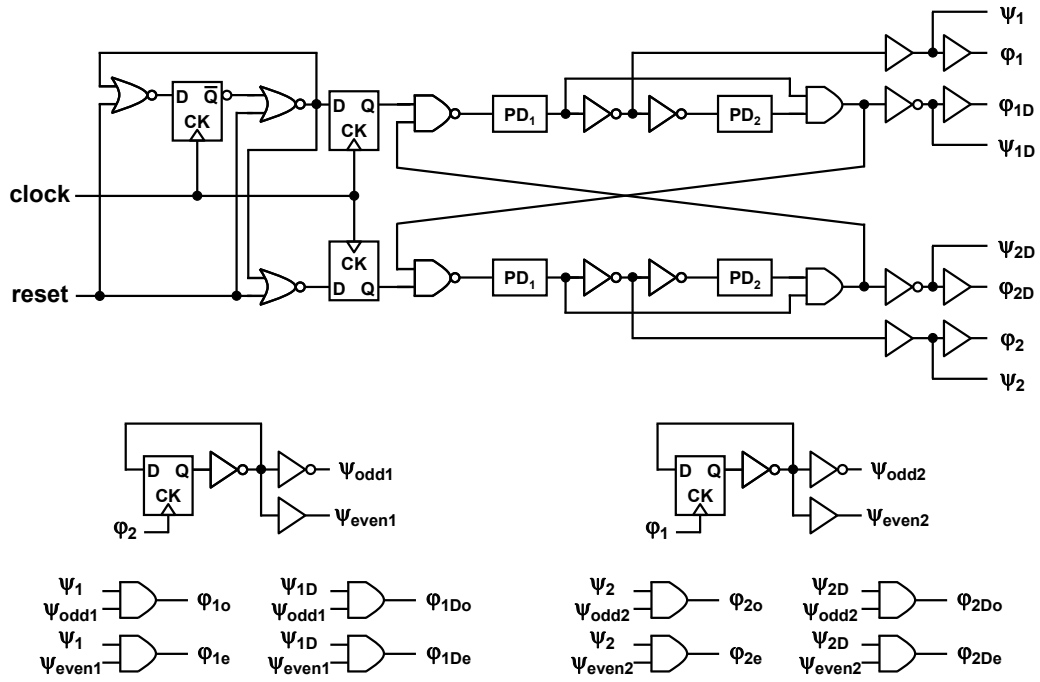

Figure 3.11: Non-overlapped clock signal generator.

The modulator's performance was evaluated by driving it with a fully differential sinusoidal signal, and capturing the output data through a logic analyzer. Then, the output spectrum of the modulator was evaluated by performing the Fast Fourier transform (FFT) with Matlab.Fig. 3.13 shows the measured output spectrum for a -1.25 dBFS 100-kHz sine-wave input signal and 60 MHz clock signal. With a 131,072-point FFT, a 78 dB SNR was achieved within the 2.5 MHz signal bandwidth. The SNDR degradation caused by the third harmonic tone was 0.4 dB, which is negligible. The measured SFDR was around 89.2dB. The input dynamic range was measured by sweeping the input signal level and observing the corresponding SNR and SNDR performance variation of the prototype modulator. Fig. 3.14 shows the measured result with a 100-kHz input sine wave. The prototype showed almost unchanged SNR and SNDR performance over the whole input range; the DR was 77 dB. Fig. 3.15 shows measured peak SNR and SNDR

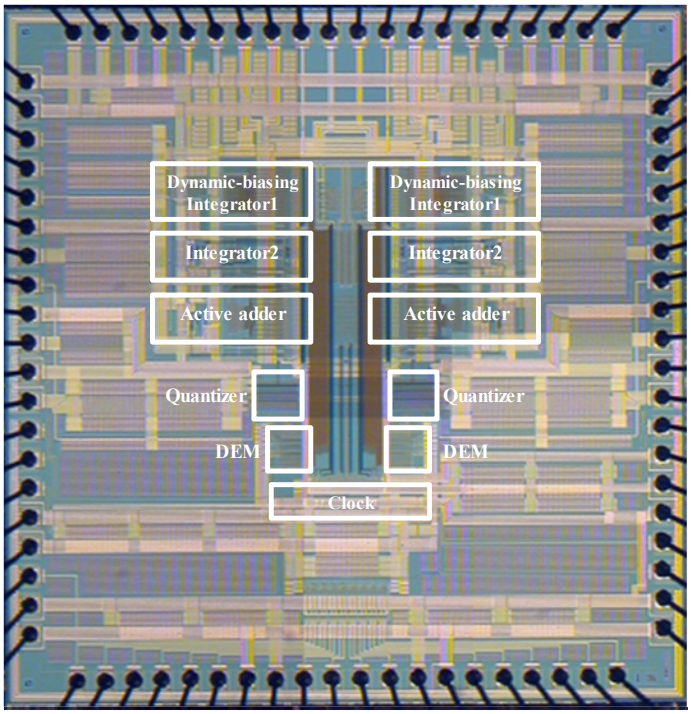

Figure 3.12: The die photograph of the modulator.

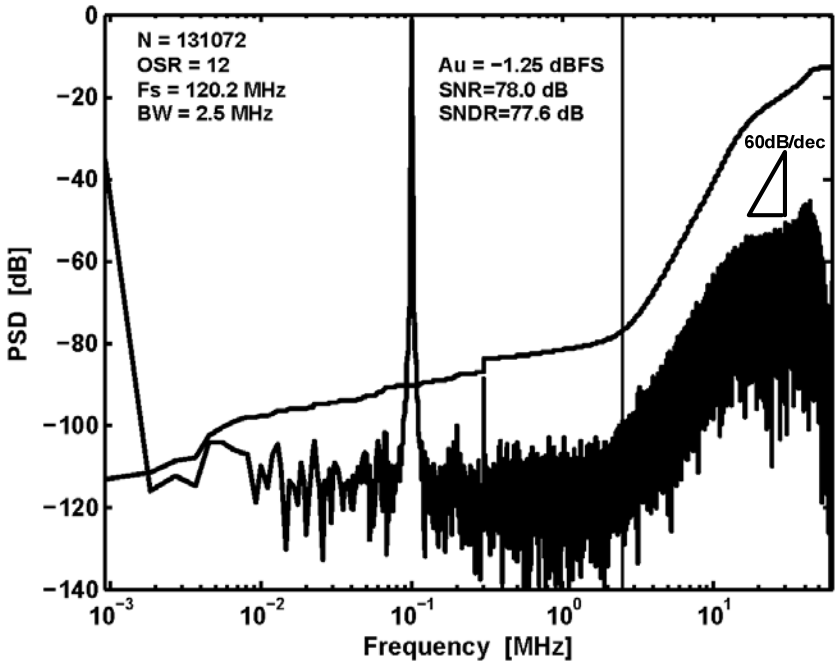

Figure 3.13: The measured output spectrum of the proposed modulator.

for different input signal frequencies from 100 kHz to 2 MHz. The second-order harmonic increases with higher input frequency, and the worst-case SNDR is around 74.3 dB with 1 MHz input signal. The total power dissipation is around 19.2 mW (11.2 mW for the analog circuitry, and 8 mW for the digital circuits). The overall performance is summarized in Table 3.1.

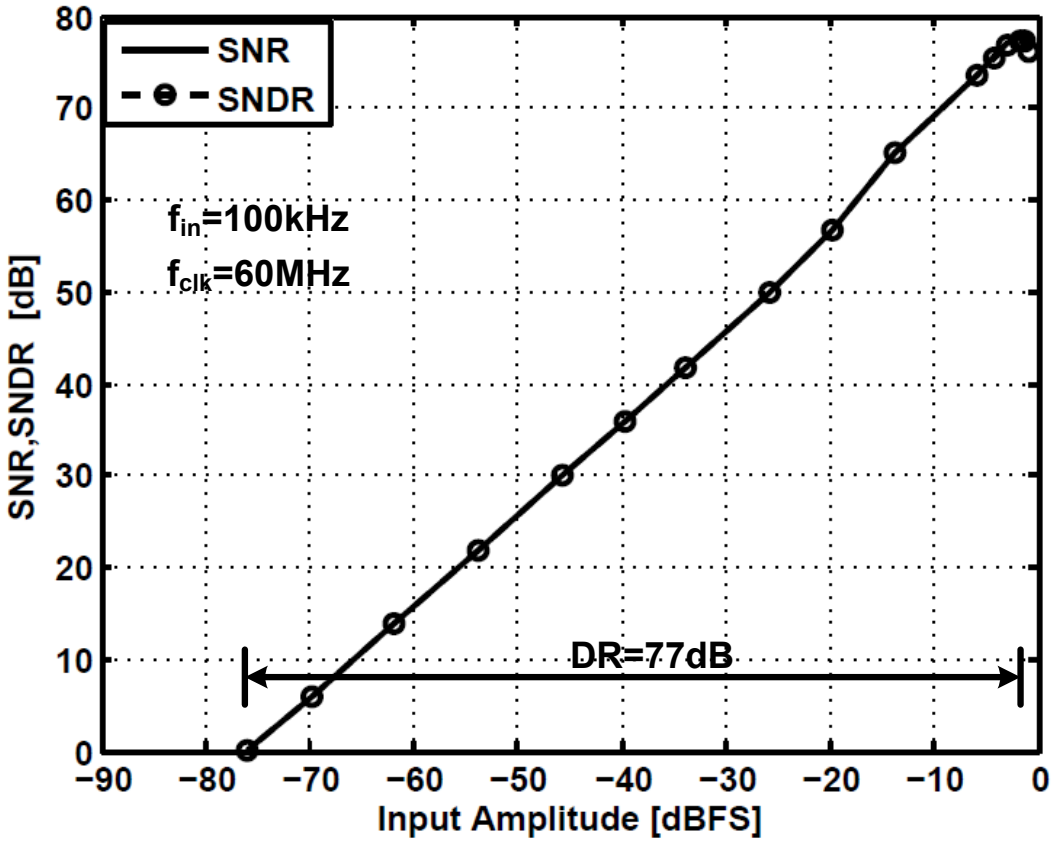

Figure 3.14: Measured SNR/SNDR with different input levels.

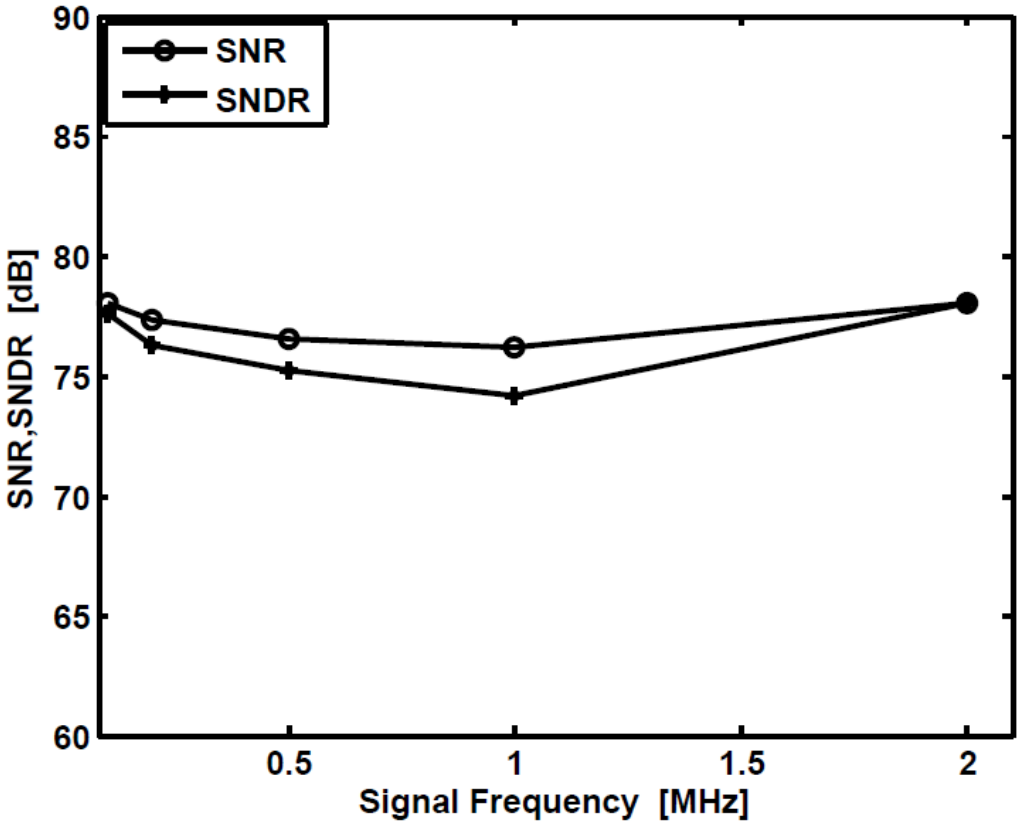

Figure 3.15: The variation of the measured SNR/SNDR with input frequency.

Table 3.1: Measured performance summary.

Process	0.18 um 2P4M CMOS
Sampling frequency	120 MHz
Clock frequency	60 MHz
Signal bandwidth	2.5 MHz
OSR	12
C_{in} and C_{DAC}	Shared
Power supply	1.6 V
Dynamic range	77 dB
SNDR / SFDR	77.6 dB / 89.2 dB
THD	-88.7 dB
FOM	0.59 pJ/conversion
Power consumption	11.2 mW (A), 8 mW (D)
Core area	3.66 mm^2

3.6 Conclusions

A signal-dependent dynamic biasing scheme was proposed. The operation principle and its circuit implementations were discussed in detail. Combined with noise coupling and low-distortion technique, the effectiveness of the proposed scheme has been verified by a high-performance time-interleaved ΔΣ ADC.

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CHAPTER. 4 A 20MHz BW, 12 BIT CONTINUOUS-TIME CASCADE DELTA-SIGMA MODULATOR WITH ADAPTIVE DIGITAL CALIBRATION

A new CT cascade ΔΣ ADC is presented to achieve 12 bit resolution within a 20 MHz signal bandwidth. The low-distortion technique, which has been effectively used in discrete-time ΔΣ modulators, has been modified to compensate for the excess-loop delay effect, and thus made applicable in continuous-time structures. The out-of band peaking issue in CT ΔΣ ADCs with feed-forward architecture is eliminated by a front-end passive low-pass filter. The MASH 2-2 architecture is used for its good stability and high inter-stage gain. Finally, a background digital compensation filter is designed to correct the quantization noise leakage due to the analog circuit non-idealities. With a 90-nm CMOS technology, the power dissipation is around 25 mW.

4.1 Introduction

High accuracy and wideband ΔΣ analog-to-digital data converters with low power dissipation are key building blocks in many applications, such as communication systems [1]-[5], consumer electronics[6][7] and radar systems[8]. In wireless and wire-line communication systems, the CT ΔΣ A/D converters become more and more popular because they have inherent anti-aliasing effects [9] and also can achieve higher bandwidth or lower power dissipation compared to the DT counterparts[10]-[14]. Compared to single stage high order ΔΣ ADC, the equivalent cascaded structure (MASH) has much better stability performance because the high-order quantization noise-shaping characteristic can be achieved with cascaded low-order modulators. The SQNR can be further increased by the inter-stage gain. Although the MASH structure has been successfully applied in the DT ΔΣ ADCs, there are only few publications on the CT MASH [15][16]. The synthesis methodology for the CT MASH is not as straight-forward as that for the

single stage modulator; Due to the excess loop delay in the feedback DAC, the low-distortion technique effective in DT structures is not applicable in CT MASH because there exists large signal power in the integrators output. Also an effective method needs to be found to correct the quantization noise leakage due to analog circuit non-idealities.

In this chapter, a new CT MASH has been presented to deal with above mentioned problems. The low-distortion-enhancement technique is developed for CT ΔΣ ADC using NRZ current DAC; the adaptive digital calibration scheme, which was developed for discrete-time ADC, is also applied successfully in CT MASH for noise leakage correction. To verify the structure, a 20 MHz, 12bits CT cascade ΔΣ modulator has been designed and the power dissipation is less than 25mW.

This chapter is organized as follows. Section 4.2 discusses two synthesis methodologies for CT MASH and an efficient synthesis flow combining these two schemes is introduced as follow. After that, section 4.3 describes the system-level design of proposed CT MASH. The circuit realization details are discussed in section 4.4. Section 4.5 presents the simulation results, and section 4.6 draws the conclusions.

4.2 The Synthesis of CT Cascade ΔΣ Modulators

A cascade DT ΔΣ modulator contains two or more low-order modulators in a series configuration. The quantization noise of each stage is passed through the following stage. Then, the digital noise cancellation filters remove the quantization noise of all stages other than the last one. Although the CT MASH topology is quite similar to the DT structure, synthesis of a CT MASH is more complicated because of its hybrid CT/DT characteristic. The inter-stage network *ITF(s)* and digital noise cancellation filter *NCF*(z), as well as each low-order modulator, need to be designed. And it is impossible to keep the loop filter topology and corresponding *NCF*(z) exactly the same as its DT version. In general, two

synthesis schemes are practical for the design: The first scheme is to design the inter-stage loop filter and keep the *NCF(z)* unchanged by referring to an equivalent DT model[17][18], while the other scheme is to directly synthesize the whole CT loop filters, including the interconnection network, and then design the matched *NCF*(z)[19].

4.2.1 Equivalent DT MASH Model

Fig. 4.1 shows a DT 2-2 MASH block diagram and the corresponding CT 2-2 MASH using the first synthesis scheme. The principle is consistent with single-stage CT modulator. The noise-shaping and stability of a ΔΣ modulator depend on the feedback loop behavior. Each low-order modulator can be directly synthesized using impulse invariant transformation (*IIT*) mapping described in chapter. 2. In order to achieve the exact mapping between the CT and DT MASH and keep the *NCF(z)* unchanged, the inter-stage loop filter transfer function, the response from first stage DAC output to the second stage quantizer input, should be the same between the two modulators. The inter-stage transfer function of DT modulator is

$$ITF_d(z) = -\left[\left(\frac{z^{-1}}{1-z^{-1}}\right)^{-2} + d_{11}\left(\frac{z^{-1}}{1-z^{-1}}\right)^{-3} + d_{12}\left(\frac{z^{-1}}{1-z^{-1}}\right)^{-4}\right] \tag{4.1}$$

With a certain feedback DAC waveform, for example the NRZ current DAC, the equivalent inter-stage loop filter transfer function in the s-domain is a fourth-order loop filter after the *IIT* mapping [20]

$$ITF_{IIT}(s) = k_1\frac{1}{s\cdot T_s} + k_2\left(\frac{1}{s\cdot T_s}\right)^2 + k_3\left(\frac{1}{s\cdot T_s}\right)^3 + k_4\left(\frac{1}{s\cdot T_s}\right)^4 \tag{4.2}$$

Here, k_1-k_4 stands for the coefficients of the equivalent *ITF*(s) for the DT modulator. So, with only two independent branches, g_1 and g_2 paths, it is not possible for CT MASH to match its ITF_a(s) with ITF_{IIT}(s), additional two independent paths g_3 and g_4 are required. The ITF_a(s) of CT MASH is

$$ITF_a(s) = g_3 \frac{1}{s \cdot T_s} + (g_1 - a_{12} g_4)\left(\frac{1}{s \cdot T_s}\right)^2 - (a_{12} g_2 + a_{11} g_4)\left(\frac{1}{s \cdot T_s}\right)^3 - a_{11} g_2 \left(\frac{1}{s \cdot T_s}\right)^4 \quad (4.3)$$

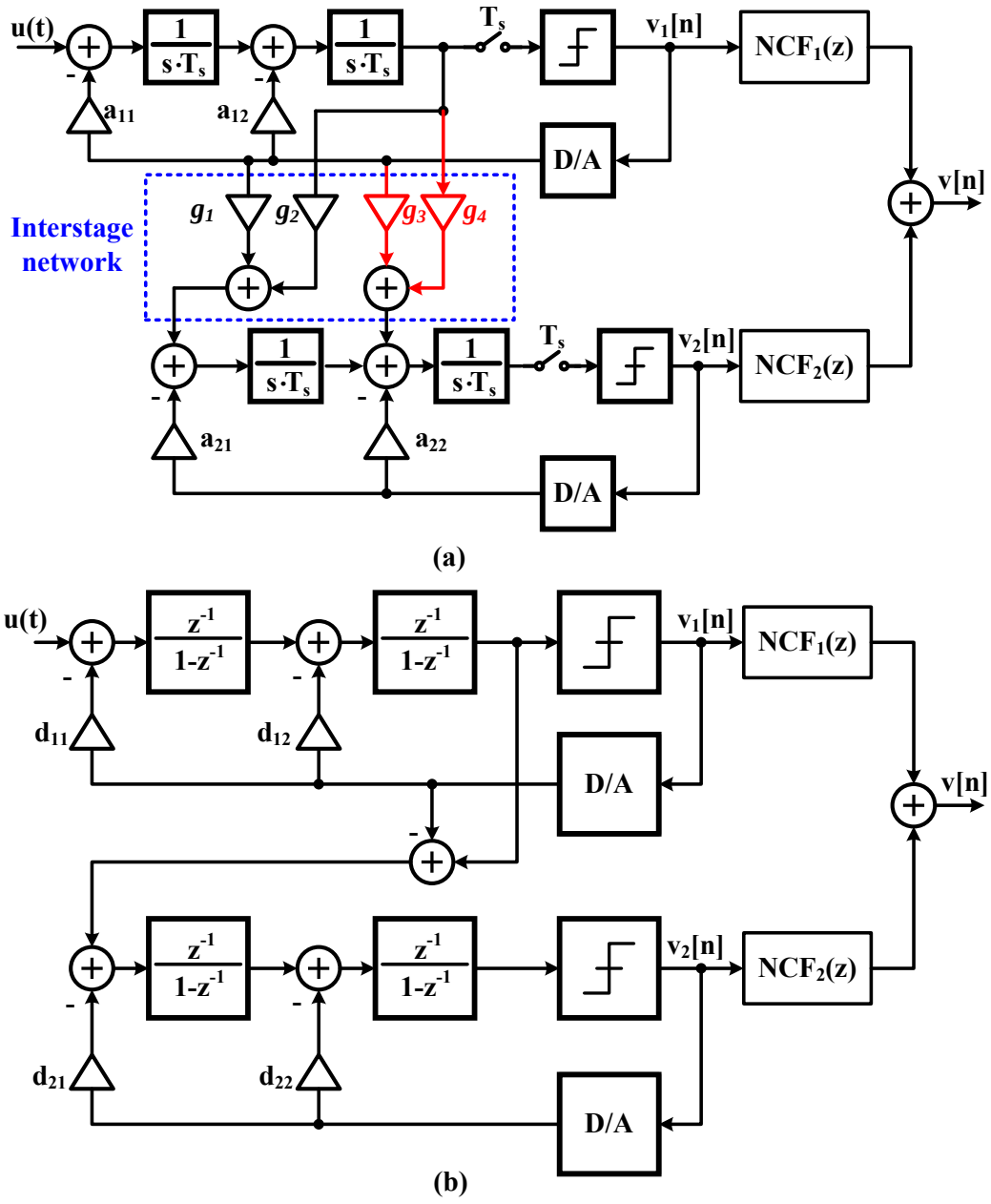

Figure 4.1: Block diagram of (a) CT 2-2 MASH (b) Equivalent DT 2-2 MASH.

There are four linear equations equivalent to Eq. 4.2 and Eq. 4.3. Then, the unique solution of g_1-g_4 can be obtained by solving the linear equations.

$$\begin{bmatrix} g_1 \\ g_2 \\ g_3 \\ g_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & -a_{12} \\ 0 & -a_{12} & 0 & a_{11} \\ 0 & -a_{11} & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} k_1 \\ k_2 \\ k_3 \\ k_4 \end{bmatrix} \tag{4.4}$$

The advantage of this scheme is that it can easily achieve the optimized NTF (z) as the discrete-time modulator [21]; the NCF (z) design is also simplified. The disadvantage of this method is that additional branches should be provided to make the exact mapping between CT and DT's loop transfer functions. With high-order noise shaping characteristic and more cascaded stages, the inter-stage loop filter requires more inter-stage branches compared to its discrete-time prototype. Taking a CT MASH with 2-1-1 topology as an example, seven independent inter-stage branches are needed. This will increase the analog circuit complexity with large silicon area, higher power consumption and more sensitivity to parameter tolerances.

4.2.2 Direct Synthesis Methodology

The alternative methodology of designing the CT cascaded delta sigma modulator dispenses with the DT-to-CT transformation, and directly synthesizes the loop filter in continuous-time domain [22]. The noise cancellation logics for each stage are designed based on the synthesized loop filters' transfer functions [23]. Fig 4.2 is a CT 2-1-1 example using this scheme. For the *k*-th stage modulator output $V_k(z)$, it can be written as

$$V_k(z) = \frac{Z\left\{L^{-1}[L_{0k}(s)U(s)]|_{nT_s}\right\} + E_k(z) + \sum_{i=1}^{k-1} Z\left\{L^{-1}[H_{DAC}(s)ITF_{ik}(s)]|_{nT_s}\right\} V_i(z)}{1 - Z\left\{L^{-1}[H_{DAC}(s)ITF_{kk}(s)]|_{nT_s}\right\}} \tag{4.5}$$

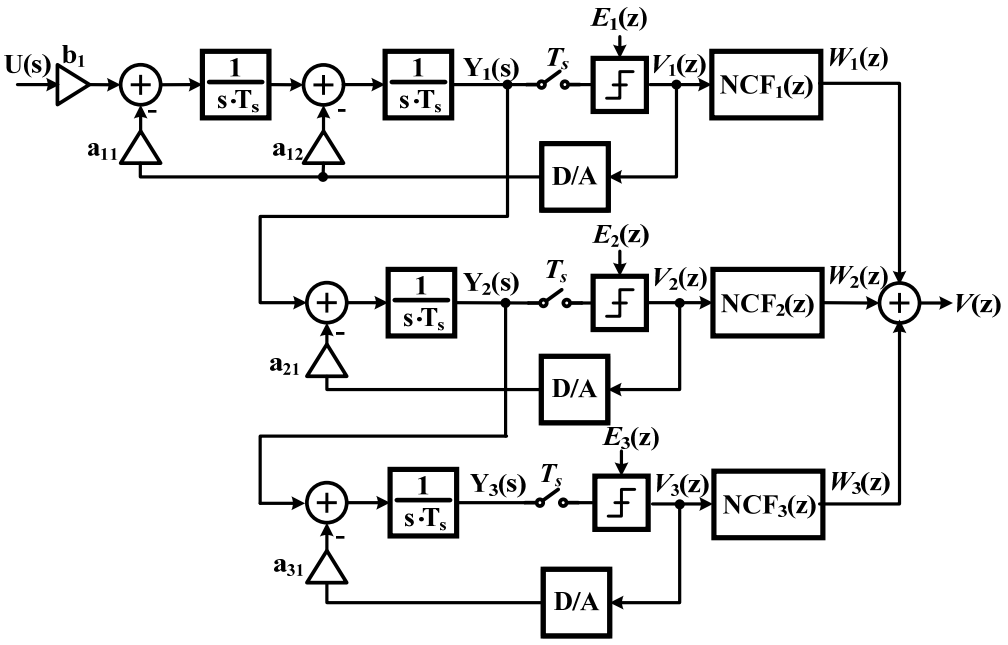

Figure 4.2: CT cascade 2-1-1 ΔΣ modulator.

Here, $L_{0k}(s)$ is the transfer function from input signal to the input of *k*-th stage quantizer, $H_{DAC}(s)$ is the transfer function of feedback DAC in *k*-th stage, *Z* stands for the *Z*-transform, L^{-1} is the inverse *Laplace* transform and $ITF_{ik}(s)$ represents the transfer function from *i*-th stage *DAC* output to *k*-th stage quantizer input. The overall output is given by

$$V(z) = \sum_{k=1}^{3} V_k(z) NCF_k(z) \tag{4.6}$$

Since the last stage modulator output, $V_3(z)$, contains all previous stages outputs, the previous stage noise cancellation filters can be designed by imposing the cancellation of the transfer function of the previous two stage modulators' output $V_k(z)$ in Eq. 4.6. This gives

$$NCF_k(z) = \frac{-Z\left\{L^{-1}[H_{DAC}(s)ITF_{k3}(s)]|_{nT_s}\right\}}{1-Z\left\{L^{-1}[H_{DAC}(s)ITF_{33}(s)]|_{nT_s}\right\}} NCF_3(z) \tag{4.7}$$

The last stage noise cancellation filter can be chosen to preserve the required noise shaping.

This scheme makes the inter-stage network design simplified, and very flexible compared to previous scheme. However, since the loop filter is designed entirely in the CT domain and doesn't refer to an equivalent DT modulator; the overall performance *NTF*(z) might not be optimized and requires extensive simulation and even some iterations for performance verification.

By combining the above two schemes, a more efficient synthesis method can be used here to synthesize a CT MASH with both optimized *NTF*(z) and simplified inter-stage loop filters. For a specific design, the optimized *NTF*(z) can be easily synthesized using the ΔΣ Toolbox [24]. Then the poles/zeros pairs can be grouped into each low-order modulators with expected loop filter structures. With designed sub-stage modulators, the whole modulator can be simply cascaded connected as Fig 4.2.

Thus, each low order modulator output can be written as:

$$\begin{aligned} V_i(z) &= Z\left\{L^{-1}[L_{0i}(s)U(s)]\,|_{nT_s}\right\}NTF_i(z) + E(z)NTF_i(z) \\ &+ \sum_{m=1}^{i-1} Z\left\{L^{-1}\left[H_{DAC}(s)ITF_{mi}(s)\right]|_{nT_s}\right\}NTF_i(z)\times V_m(z) \end{aligned} \tag{4.8}$$

and the last stage noise cancellation filter is chosen to be:

$$NCF_k(z) = \prod_{i=1}^{k-1} NTF_i(z) \tag{4.9}$$

So W_k (z), the last stage modulator output after NCF_k (z) is

$$W_k(z) = STF(z)U(z) + NTF(z)\times\left(\sum_{m=1}^{k-1} Z\left\{L^{-1}[H_{DAC}(s)ITF_{mk}(s)]\,|_{nT_s}\right\}V_m(z) + E_k(z)\right) \tag{4.10}$$

Here,

$$STF(z)U(z) = NTF(z)\times Z\left\{L^{-1}[L_{0k}(s)U(s)]\,|_{nT_s}\right\} \tag{4.11}$$

$$NTF(z) = \prod_{i=1}^{k} NTF_i(z) \tag{4.12}$$

If the *i*th (*i*<*k*) stage noise cancellation filter is chosen as

$$NCF_i(z) = -Z\left\{L^{-1}[H_{DAC}(s)ITF_{ik}(s)]|_{nT_s}\right\}NTF(z) \tag{4.13}$$

the modulator outputs of all proceeding stages other than the last one are cancelled. The overall output can be written as:

$$V(z) = STF(z)U(z) + NTF(z)E_k(z) \tag{4.14}$$

Each $NCF_i(z)$ is the linear combination of

$$NCF_i(z) = \sum_{j=1}^{k} c_j \frac{z^{j-1}}{D(z)} \tag{4.15}$$

$D(z)$ is the denominator of $NTF(z)$. Similar to the Eq. 4.4, by using *IIT* mapping in each ITF_{ik}, we can get the equivalent $ITF_{ik}(z)$. Combined with $NTF(z)$, all the coefficients of c_j can be derived.

Once the CT MASH structure is decided, the $NTF(z)$ and each stage $NCF(z)$,as well as CT loop filter coefficients, can all be directly synthesized using on hand ΔΣ toolbox and *Matlab* simulation tools. The system-level design and verification become very efficient. Noise-shaping and stability are also well predicted and guaranteed. Also, no complicated inter-stage network is needed. Thus low power, small silicon area and low sensitivity to parameter tolerance can be expected.

4.3 System-level design of CT 2-2 MASH

In this section, the low-distortion technique for CT ΔΣ ADC is first described, followed by the introduction of adaptive digital calibration scheme of CT MASH. After that, the system-level design of proposed CT MASH, including system parameters selection, modulator architecture consideration and noise-budget allocation, etc. is illustrated.

4.3.1 Low-Distortion Technique for CT ΔΣ ADC

For a DT ΔΣ ADC with feed-forward architecture, the low distortion topology [25] is a favorite for wideband low-power applications. By adding a direct feed-in path to the quantizer input, the modulator achieves a unity STF for all frequencies

and the input signal can be transmitted to the modulator output without any filtering and delay. Therefore, at the loop filter input, signal component can be ideally cancelled. Since the loop filter just needs to deal with the random errors, the amplifier's linearity requirement is greatly relaxed.

The low-distortion technique can be extended to the CT ΔΣ ADCs, which is depicted in Fig. 4.3. Referred to Eq. 2.37,

$$H(s) = L_0(s) = -L_1(s) \tag{4.16}$$

So the signal transfer function in s-domain is

$$STF(s) \approx \frac{1 + H(s)}{1 + H_{DAC}(s)H(s)} \tag{4.17}$$

For a NRZ feedback DAC, it is essentially a low-pass Sinc filter with 0dB DC gain. The transfer function can be given as

$$H_{DAC}(s) = H_{DAC}(j\omega) = \frac{\sin(\omega T_s/2)}{\omega T_s/2} e^{-j\omega T_s/2} \tag{4.18}$$

T_s denotes the sampling period of the modulator. With increased frequency, the gain of $H_{DAC}(s)$ decreases with a linear phase shift. Fig. 4.4 shows the gain and phase responses of a *NRZ DAC* from DC to the sampling frequency. When OSR=8, the gain drop is -0.056dB at the edge of pass band and the phase drop is 11.3^o, both of them negligible. They are even smaller for higher OSRs. So, within the pass band of a low-pass ΔΣ modulator, $STF(s) \approx 1$.

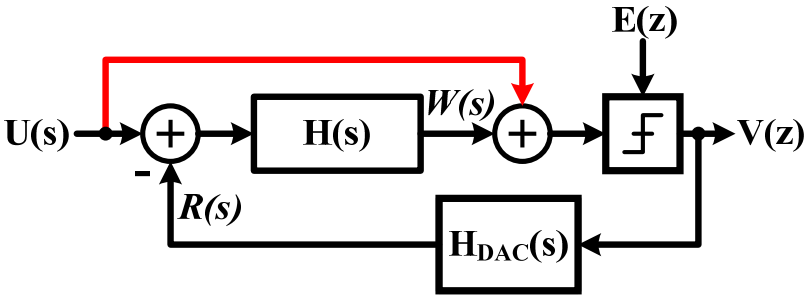

Figure 4.3: The block diagram of the low-distortion CT ΔΣ ADC.

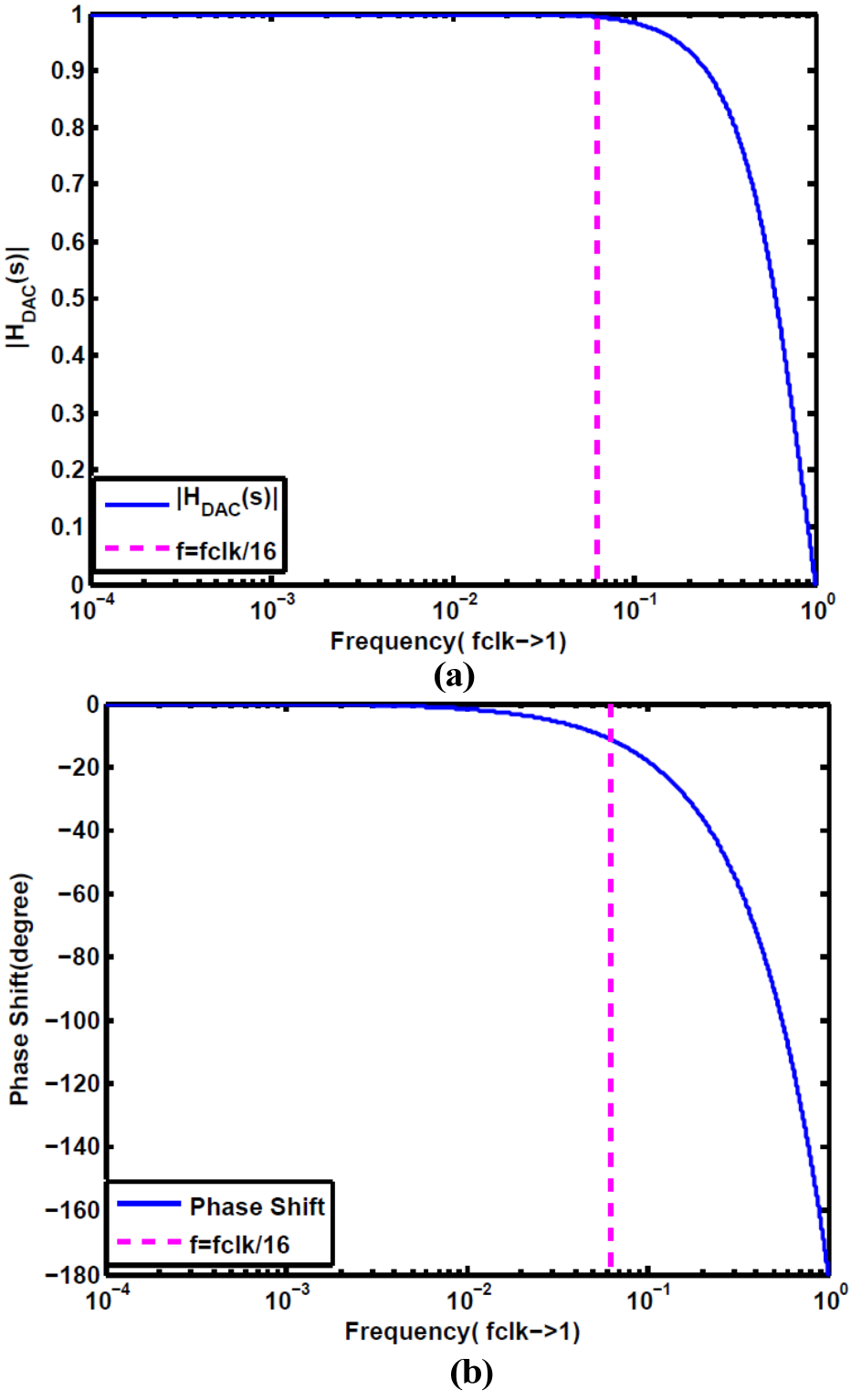

Figure 4.4: (a)Magnitude response (b) Phase response of $H_{DAC}(s)$.

Hence, as in a DT modulator, by adding a direct input branch to the quantizer, the STF(s) is roughly equal to 1 within the pass band and the signal will be mostly cancelled at the loop filter input. Fig. 4.5 shows a simple 2nd order modulator example. With a 0 dBFS input, there are only -23 dBFS and -17 dBFS signal components at first and second integrator output at fclk/16 (Fig. 4.6). So, the low-distortion condition is achieved in the signal band.

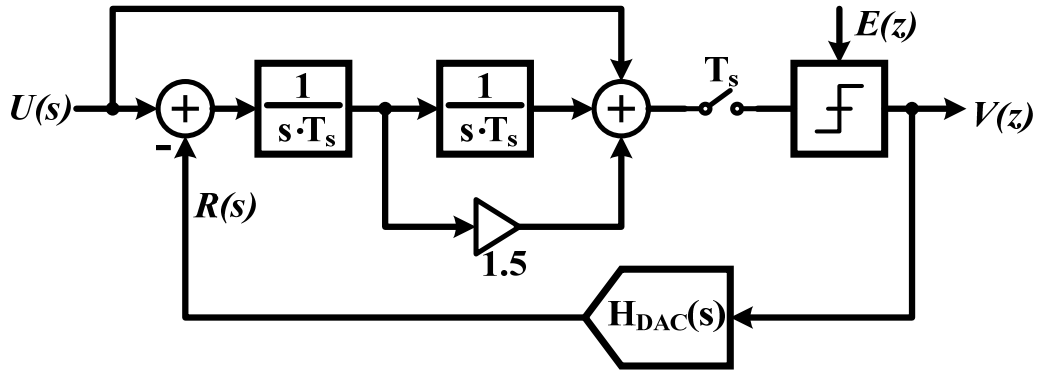

Figure 4.5: Block diagram of 2nd-order low-distortion CT ΔΣ modulator.

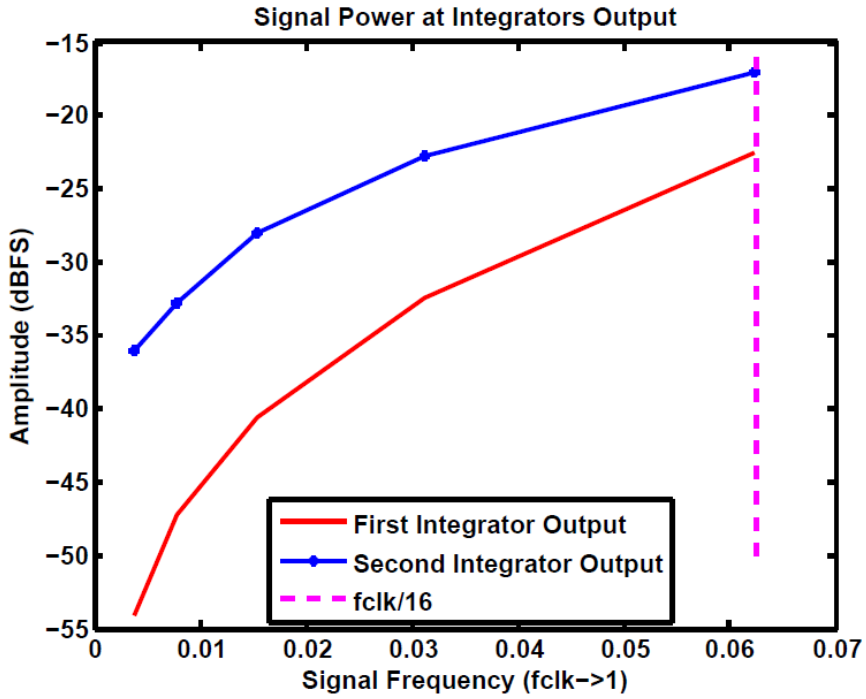

Figure 4.6: Signal power at the integrators' output (0 dBFS input).

However, for a wideband CT ΔΣ ADC, fixed half-cycle or full-cycle delay is usually applied in the feedback DAC to reduce the signal dependent jitter noise and to relax the timing for the *DEM* logic blocks. This excess loop delay increases the loop filter order by one and may induce instability. To stabilize the loop, another independent feedback path has to be added [20], and we have to match the new loop filter transfer function to the desired DT loop filter function, using impulse-invariant-transformation (IIT). The general block diagram with a half-cycle delay is shown as Fig. 4.7. The adder output Y(s) is now

$$Y(s) = H(s) \times \big(U(s) - R(s)\big) - K_C \times V(s) \tag{4.19}$$

The signal transfer function for the new modulator is approximately

$$STF(s) = \frac{H(s)}{1 + K_C + H_{DAC}^{'}(s)H(s)} \tag{4.20}$$

Here, $H_{DAC}^{'}(s)$ denotes the DAC transfer function with the added half-cycle delay

$$H_{DAC}^{'}(s) = H_{DAC}^{'}(j\omega) = \frac{\sin(\omega T_s/2)}{\omega T_s/2} e^{-j\omega T_s} \tag{4.21}$$

Compared to Eq. 4.18, the magnitude response is unchanged but the phase lag is twice as large as for the non-delayed *DAC*. Due to oversampling, the input signal is in the low frequency range and the approximation of $H_{DAC}^{'}(s) \approx 1$ still holds.

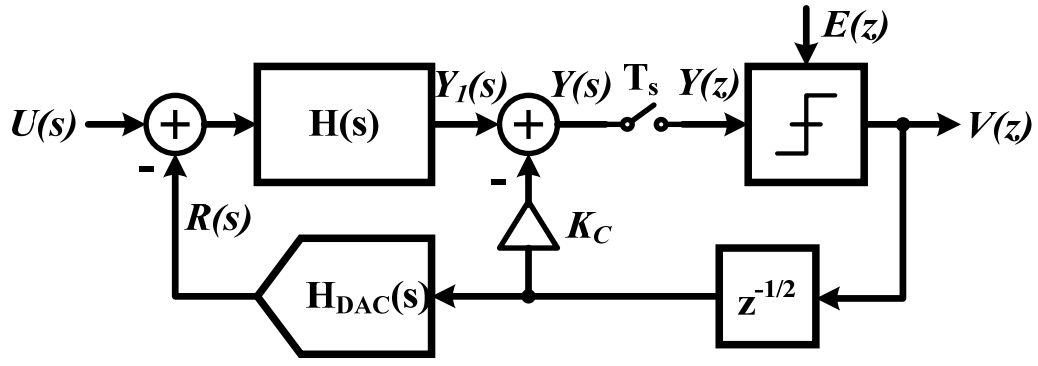

Figure 4.7: The block diagram of a CT ΔΣ modulator with excess-loop-delay compensation.

Adding a direct input branch to the quantizer with a gain of 1, the STF becomes

$$STF(s) = \frac{1 + H(s)}{1 + K_C + H(s)} \tag{4.22}$$

So, $|STF| < 1$ even at very low frequency and signal cannot be perfectly cancelled at the loop filter input. Since $H(s)$ is realized by integrators, which have large gain at low frequency, the signal component at loop filter output $Y_1(s)$,

$$\frac{Y_1(s)}{U(s)} \approx \frac{K_C H(s)}{1 + K_C + H(s)} \approx K_C \mid_{s \to 0} \tag{4.23}$$

So a large signal component is present at the loop filter output. Its power is directly related to the gain of the additional feedback path. The low-distortion technique becomes invalid.

In order to retrieve the low-distortion technique, the direct input branch should be modified, and the resulting block diagram is shown in Fig. 4.8. So, the gain of direct input branch is increased from 1 to $1+K_c$. The new signal transfer function at low frequency becomes

$$STF(s) = \frac{1 + K_c + H(s)}{1 + K_c + H(s)} = 1 \tag{4.24}$$

Therefore, the low-distortion is achieved.

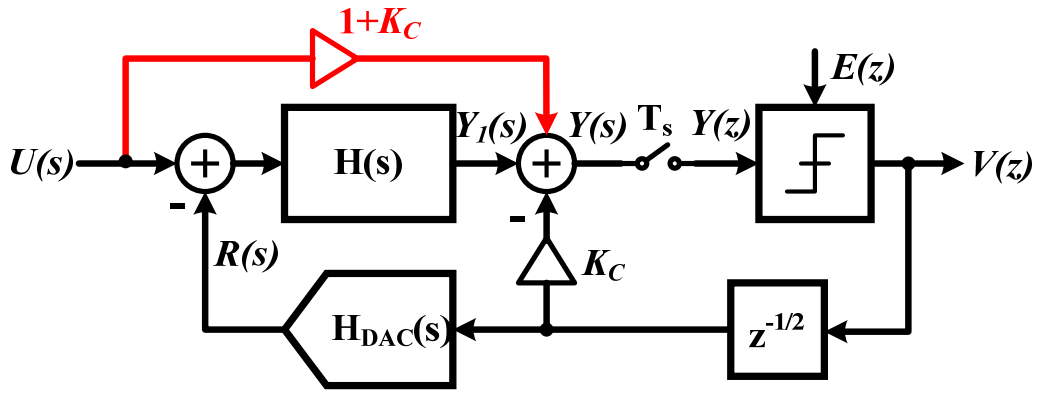

Figure 4.8: Low-distortion CT ΔΣ modulators with half-cycle excess-loop delay.

In addition to the feed-forward compensation structure, the low-distortion can also be achieved by using the feedback compensation technique, the resulting block diagram is shown in Fig. 4.9. And for low frequency input signal, the signal transfer function at modulator output is

$$STF(s) = \frac{1 + H(s)/(1 + K_C)}{1 + K_C + H(s)} = \frac{1}{1 + K_C} \tag{4.25}$$

So, low frequency input signal will be attenuated by $1/(1+K_C)$ at modulator output. But it will again be cancelled at loop filter input.

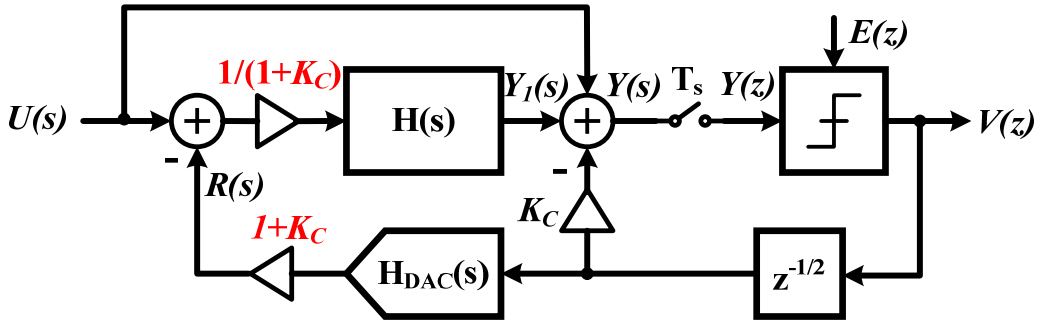

Figure 4.9: Low-distortion CT ΔΣ modulators using feedback compensation.

To verify the proposed topologies, both feed-forward and feedback compensation techniques were applied to the second-order CT ΔΣ modulator with a half-cycle excess loop delay. The block diagram is shown in Fig. 4.10. Since K_C is equal to 0.875 in this case, the optimum K_T is also equal to 0.875. Assume OSR=8 and a 3bit quantizer for the modulator, with 0dBFS input signal, the signal amplitudes at the loop filter output before and after compensation are plotted in Fig. 4.11 for comparison. Without any compensation, the signal amplitude at the loop filter output is around -1.2dBFS, which is well predicted by Eq. 4.23. After compensation, signal amplitude can be greatly reduced, especially for low frequency signals. At the edge of the pass band, 6.5dB and 12dB attenuation are obtained with feed-forward and feedback compensation, respectively. Due to the input signal attenuation by $1/(1+K_T)$, the feedback compensation technique has 5.46dB lower signal amplitude at loop filter output. Meanwhile, the signal

amplitude decreases by 6dB/Octave with signal frequency. Thus, loop filter linearity requirement can be further relaxed.

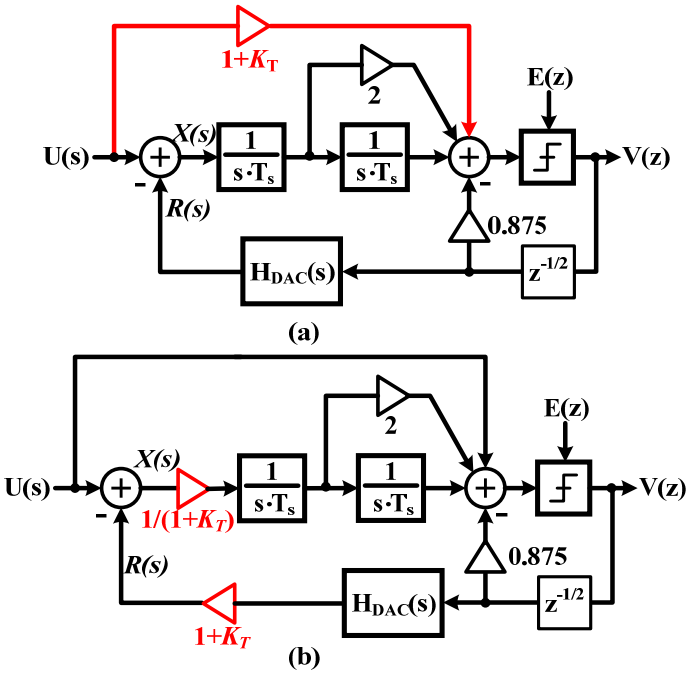

Figure 4.10: Second order low-distortion ΔΣ ADC with (a) Feed-forward (b) Feedback compensation.

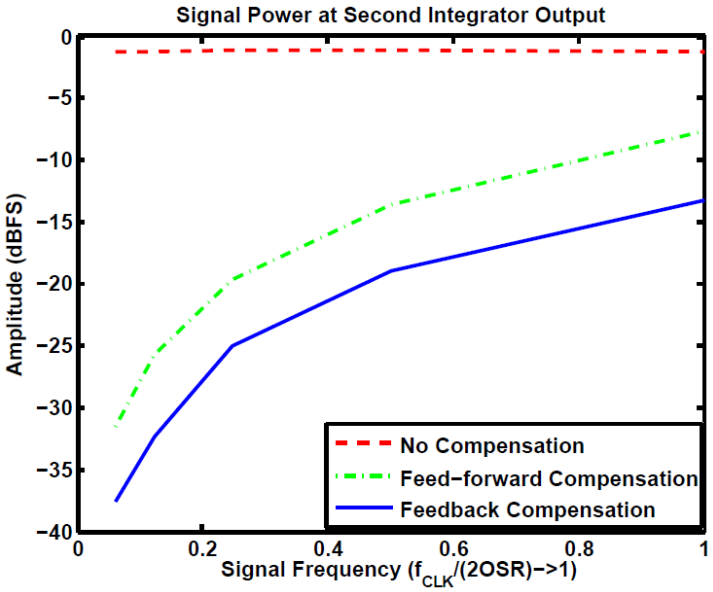

Figure 4.11: Signal amplitudes at 2nd integrator output W/WO compensation.

For a signal frequency at the edge of the pass band, the optimum value of K_T, and its sensitivity to varying OSR values have been checked. With a 0 dBFS input signal, Fig. 4.12 shows the signal amplitudes at the loop filter output with different K_T values. The optimum K_T is unchanged at 0.875 when OSR is high, and decreases only slightly with OSR. For higher OSRs, the signal amplitude is more sensitive to K_T, but is much lower around the optimum K_T value. So modulators with higher OSR have lower linearity requirements for the loop filter. Furthermore, if the modulator is used as the first stage for a CT MASH, an inter-stage gain can be applied to increase the overall SQNR, when the second integrator output is directly used as the input of following stage modulator. The maximum inter-stage gain depends on the OSR and the quantizer resolution. For an OSR of 8, the inter-stage gain can be 4 using the feedback compensation scheme, if the quantizer has a 3 bit or higher resolution. For higher OSR, even larger inter-stage gain can be applied.

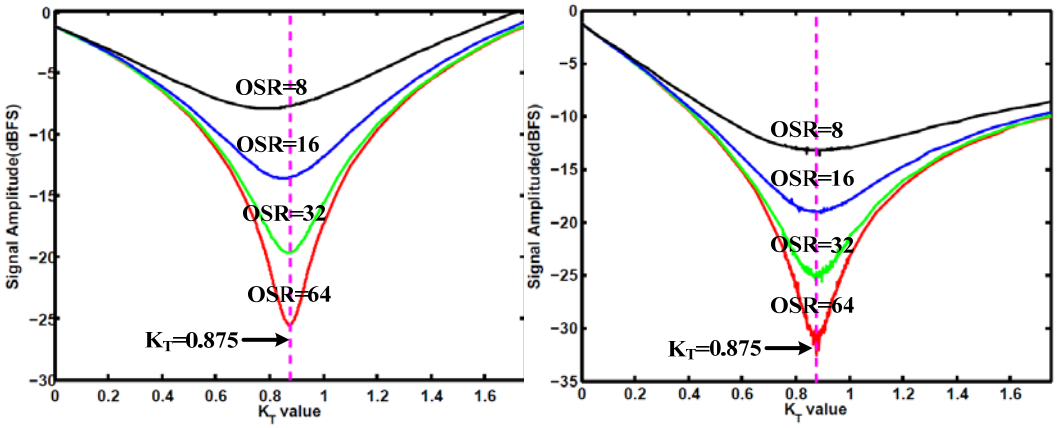

Figure 4.12: Optimum K_T values with different OSRs.

4.3.2 Adaptive Digital Calibration for CT Cascaded ΔΣ ADCs

4.3.2.1 Noise-leakage for CT Cascaded ΔΣ ADCs

As is mentioned in Chapter 2, the performance of cascaded ΔΣ ADCs suffers from the noise leakage caused by the mismatch between the analog realization of

the NTFs and the digital noise cancellation logics. For a CT cascaded ΔΣ ADC, analog circuit imperfections are mainly caused by opamp finite dc gain, finite bandwidth and integrator RC time constant variation, etc.

Fig. 4.13 shows the block diagram of two stage CT ΔΣ modulator. The overall modulator output $V(z)$ is

$$V(z) = V_1(z)NCF_1(z) + V_2(z)NCF_2(z) \tag{4.26}$$

Using the direct synthesis scheme described in section 4.2.2,

$$NCF_1(z) = -Z\left\{L^{-1}[H_{DAC1}(s)LTF(s)]|_{nT_s}\right\}NTF_1(z)NTF_2(z) \tag{4.27}$$

$$NCF_2(z) = NTF_1(z) \tag{4.28}$$

Here, *LTF(s)* denotes inter-stage loop filter transfer function and $NTF_i(z)$ the noise transfer function at *i-th* stage

$$LTF(s) = -H_1(s)H_2(s) \tag{4.29}$$

$$NTF_1(z) = \frac{1}{1 + Z\left\{L^{-1}\left[H_{DAC1}(s)H_1(s)\right]|_{t=nT_s}\right\}} \tag{4.30}$$

$$NTF_2(z) = \frac{1}{1 + Z\left\{L^{-1}\left[H_{DAC2}(s)H_2(s)\right]|_{t=nT_s}\right\}} \tag{4.31}$$

The first stage modulator output $V_1(z)$ contains the filtered input signal and shaped quantization error $E_1(z)$. Ideally, $V_1(z)$ is cancelled at the overall modulator output. However, due to the analog circuit imperfections, the inter-stage transfer function *LTF(s)*, $NTF_1(z)$ and $NTF_2(z)$ are all deviated from ideal values, the $V_1(z)$ cannot be completely cancelled and the residue presenting at the output is equal to

$$\frac{V_{1,res}(z)}{V_1(z)} = Z\left\{L^{-1}\left[H'_{DAC1}(s)LTF'(s)\right]|_{t=nT_s}\right\}NTF_2'(z)NTF_1(z) - NCF_1(z) \tag{4.32}$$

$H'(*)$, $LTF'(*)$ and $NTF'(*)$ represent the realistic transfer function of feedback *DAC*, loop filter and noise transfer function. Since $V_1(z)$ contains $E_1(z)$, quantization noise also leaks to the modulator output.

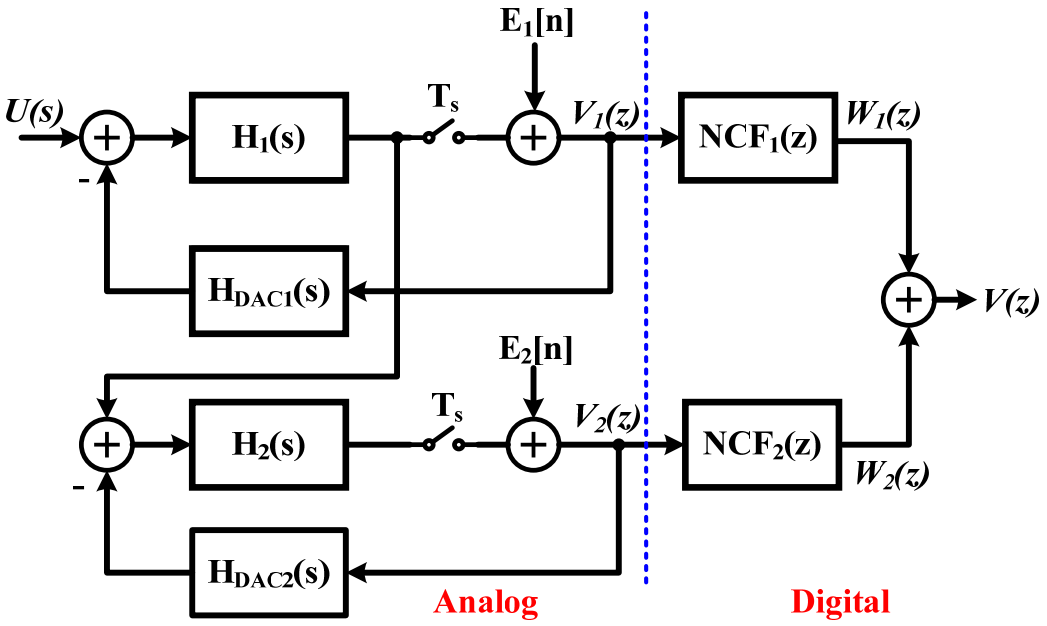

Figure 4.13: The CT ΔΣ modulator block diagram without calibration.

4.3.2.2 Adaptive Calibration Using Test-Signal Injection

To mitigate the quantization noise leakage issue, a multi-bit quantizer can be used in the first stage modulator. It can ideally provide 6dB improvement with every extra bit. On the other hand, the number of comparators and then the power dissipation increases exponentially for a multi-bit quantizer, therefore the quantizer resolution is usually limited up to 5bit in real ΔΣ ADC. By designing the analog blocks as perfect as possible, the analog NTFs can match closely with the digital NCFs, and thus the leakage noise is reduced. However, the analog circuitry has to be very robust against the process and environment variations, and usually ends up with large power dissipation and increased production cost, especially for wideband application. The alternative solution is to use an adaptive digital compensation filter matching with the analog counterparts; it requires more complicated digital circuit, but it becomes trivial when considering the significant improvement of the effective analog precision. The environment drift and aging can also be adaptively tracked and compensated. Different off-line and on-line calibration schemes have been investigated and verified successfully [26-29].

In this work, the test-signal injection approach [30] is chosen to do the on-line calibration. Fig. 4.14 shows the block diagram using proposed technique. A well defined (pseudo-random and uniformly distributed) test signal is injected to the input of first-stage quantizer where it is added to the quantization noise E_1. Since the test signal behaves similarly to the E_1 and goes through the same parasitic leakage path to the output V, $V = f\{u, test, e_1, e_2\}$ .On the other hand, the test signal is independent with input signal U, and quantization noise e_1 and e_2, the correlation result between $V(z)$ and test signal only contains test signal. $corr(V, test) \approx f\{test\}$ .Appling the correlation information with a robust *LMS* algorithm, test signal at the modulator output can be minimized by adding a digital compensation filter L_c (z). Since the test signal has the same leakage path as the quantization error E_1, minimization of the test signal can minimize the leakage of E_1 at the same time.

The modulator output becomes

$$V(z) = V_1(z)\left[NCF_1(z) + L_C(z)\right] + V_2(z)NCF_2(z) \tag{4.33}$$

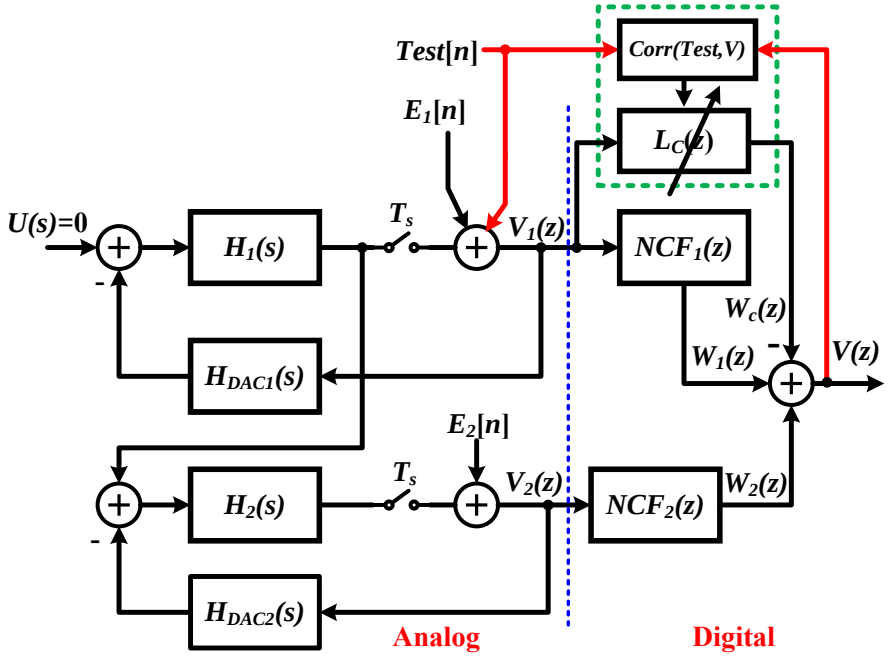

Figure 4.14: The modulator block diagram with adaptive digital calibration.

Based on Eq. 4.32, in order to cancel the residue component of $V_1(z)$ in the modulator output, the digital compensation filter $L_c(z)$ should be

$$L_c(z) = \frac{Z\left\{L^{-1}\left[H'_{DAC1}(s)H'_1(s)H'_2(s)\right]|_{t=nT_s}\right\}}{1+Z\left\{L^{-1}\left[H'_{DAC2}(s)H'_2(s)\right]|_{t=nT_s}\right\}} NTF_1(z) - NCF_1(z) \qquad (4.34)$$

$H'(*)$ denotes the realistic transfer function of analog blocks.

Fig. 4.15 shows the example block diagram of a six-order *FIR* digital calibration filter. The filter's coefficients are updated based on the correlation results between modulator output *V*(z) and the injected test signal. Sign-Sign Block-Least-Mean-Square (SS-BLMS) algorithm [31] is used here for its efficient circuit structure. To make sure that the correlation result is dominated by test signal, the coefficient update cycle L is set to 2^{20}, and a flexible step size is also used to optimize the calibration performance in terms of speed and resolution.

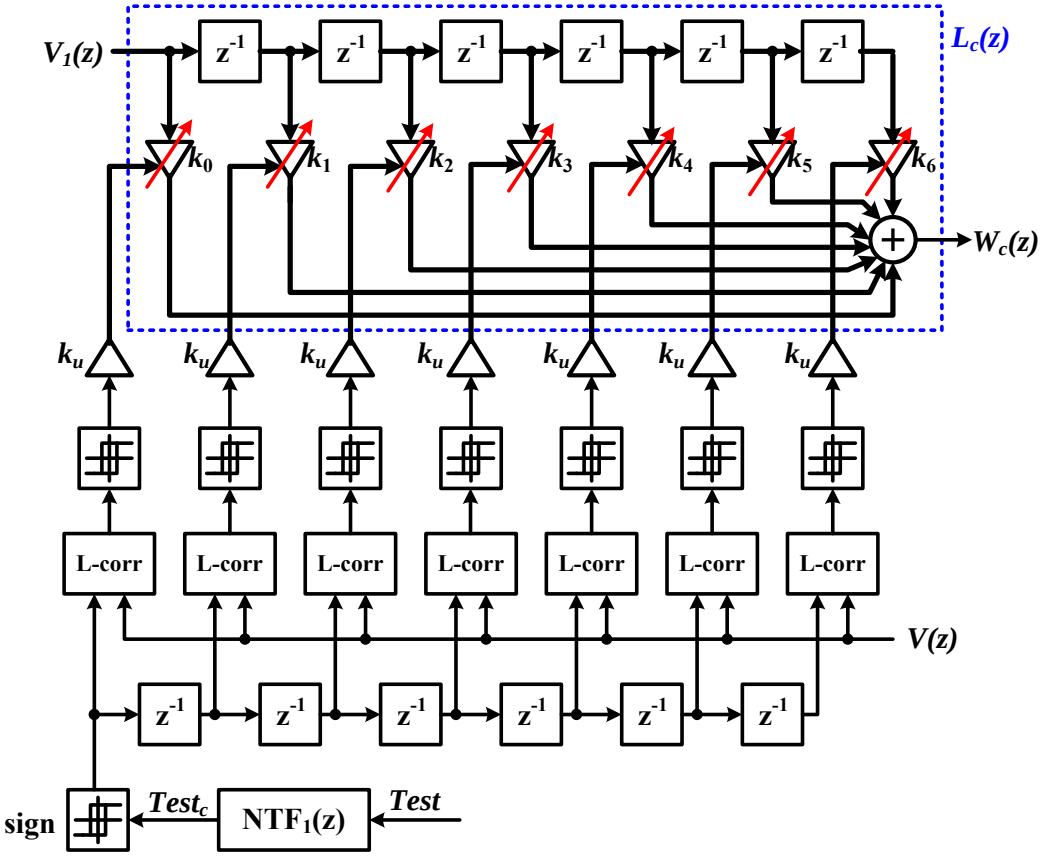

Figure 4.15: Adaptive digital calibration filter block diagram.

From Eq. 4.32, the calibration filter $L_c(z)$ is actually used to compensate the residue of $V_1(z)$, where the test signal has already been shaped by $NTF_1(z)$, so it is better to first shape the test signal by $NTF_1(z)$ before it is used in the correlation operation. The update algorithm is

$$\vec{k}[(j+1)L] = \vec{k}[jL] - k_u sign\left\{\sum_{i=0}^{L-1} V(jL+i) \times sign\left[\overrightarrow{Test_C}(jL+i)\right]\right\} \tag{4.35}$$

Here, $\vec{k} = [k_0\ k_1\ k_2\ k_3\ k_4\ k_5\ k_6]^T$ and

$$Test_C(z) = NTF(z) \times Test(z) \tag{4.36}$$

Detail description of the adaptive calibration can be found at Refs [32-33].

4.3.3 System-level Parameters Consideration

After the discussion of new design techniques for CT cascade ΔΣ ADC, the key system parameters (OSR, loop filter order L and quantization levels *nLev*, etc) need to be decided based on the design requirement. The target design specification is summarized in Table 4.1.

Table 4.1: CT MASH Design Specifications.

Process	90nm CMOS Logic
BW	20MHz
Resolution	12bit
Dynamic Range	72dB
THD	<-74dB
Power Dissipation(Analog circuit)	<25mW

For a cascade ΔΣ modulator, the inter-stage gain k_{int} can further increase the noise-shaping ability and the maximum SQNR is given as

$$SQNR_{\max}[dB] = 6.02N + 1.76 + 20\log_{10}\prod_{i=1}^{k-1} k_{\text{int},j} + 10\log_{10}(OSR/\pi)^{2L} + 10\log_{10}[(2L+1)OSR] \quad (4.37)$$

$k_{\text{int},j}$ means the inter-stage gain between the j-th stage and (j+1)-th stage modulator. For a low-distortion DT ΔΣ ADC, the inter-stage gain is determined by the quantizer resolution, and usually set to 2^{N-1} for an N-bit quantizer. However, in a low-distortion CT ΔΣ ADC, the inter-stage gain depends not only on the quantization levels but also the oversampling ratio, which usually requires k_{int} no more than OSR/4. Therefore, the maximum k_{int} is limited by OSR or quantization levels in different structures.

In general, CT ΔΣ ADC performance is determined by many noise sources, such as thermal noise, jitter noise, integrator gain error and quantization error etc. For a low-power design, the in-band quantization noise should occupy only a very small portion in the total noise and the noise floor is dominated by thermal noise and jitter noise. So, designing a CT ΔΣ ADC with 12bit resolution requires more than 14bit SQNR. Using the low-distortion technique discussed in Chapter 4.3.1, Table 4.2 summarizes four different topologies that can achieve the design target.

Table 4.2: Different system-level parameter combinations for design target.

OSR	Architecture	Quant. Bits	Inter-stage Gain	SQNR
16	2-2	2-2	2	>86
12	2-2-1	2-2-2	2-2	>86
16	2-1	3-2	4	>86
8	2-2	4-4	2	>86

By inspection, the third scheme is superior to the first two combinations in terms of the power dissipation, jitter sensitivity and circuit complexity. The first scheme has the highest jitter sensitivity with only 2-bit quantizer and oversampling ratio equal to 16. The circuit implementation of the second scheme is more

complicated compared to others. And the quantization noise leakage has to be calibrated at both the first stage and the second stage modulator output, resulting a more complicated digital calibration filter.

On the other hand, the last two schemes have their own pros and cons when they are compared to each other. In general, the third solution has simpler circuit structure. It uses only 3 integrators and 12 comparators. The inter-stage gain is optimized because the limitation of k_{int} is the same considering both sampling rate and quantizer resolution. In the last scheme, 4 integrators and 32 comparators are required and the effective k_{int} is limited by OSR and can not be greater than 2. On the other hand, OSR is 8 in the last scheme and the sampling frequency is only half of previous scheme. Speed requirement of the amplifiers and comparators can be greatly reduced, as well as the clock jitter sensitivity. The more accurate quantizer further reduces the jitter noise and increases the input signal range.

Since jitter noise can significantly degrade the performance for wideband CT ΔΣ ADC, an integrated clock generator is usually necessary to provide clean clock source with sub-ps jitter performance [14], which is unfortunately impossible in our design. Therefore, the last scheme becomes the best solution to compromise jitter performance, circuit realization and power dissipation, etc.

Fig. 4.16 shows the proposed CT 2-2 MASH block diagram. Low-distortion feed-forward structure is used in the first stage modulator for its excellent linearity performance and good power efficiency. The feedback compensation technique is used here to maintain low-distortion characteristic with half-cycle loop delay. So, an inter-stage gain of 4 can be used with OSR=8. The unit-element mismatch of feedback DAC generates harmonic tones at the modulator output, so a simple but fast DWA circuit is used to shape the harmonic tone out of signal band. On the other hand, the CT ΔΣ ADC using feed-forward structure suffers from out-of band peaking issue, and then a front-end low-pass filter is added to prevent the modulator from saturation . In the second stage modulator, the linearity requirement is much relaxed with 2^{nd} order noise-shaping, so the feedback

architecture is chosen for its attractive low-pass filtering characteristic. Pole and Zero optimization are used to further increase the SQNR. To minimize the quantization noise leakage at the modulator output, the adaptive calibration filter using test signal injection approach is designed. And the test signal behaves also as a dither signal, which prevents DWA block from the tone issue. Two stage modulator outputs are both filtered by the noise cancellation filters, and the noise leakage is cancelled with the digital calibration filter.

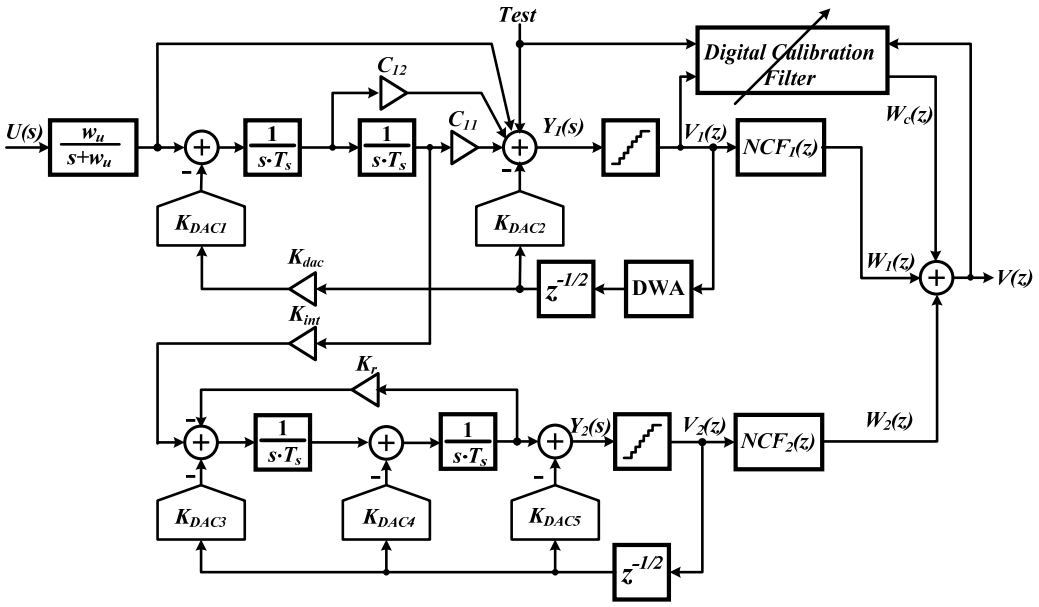

Figure 4.16: The CT 2-2 MASH block diagram.

To verify the proposed structure, extensive simulations have been run using the SIMULINK toolbox. Fig.4.17 shows the ideal output spectrum with -0.45dBFs input signal, 86.7dB SQNR can be achieved. Meanwhile, assuming the 60dB DC gain and 1GHz UGBW for the opamp, as well as 20% RC time constant variation, Fig. 4.18 shows the modulator output spectrums before and after digital calibration. Around 28dB improvement can be achieved. The effectiveness of digital calibration scheme is verified. On the other hand, although the noise leakage due to the time-constant variation can be compensated by the background

calibration, signal transfer function is still affected. To keep STF unchanged at the modulator output, RC time constant tuning circuit is still necessary.

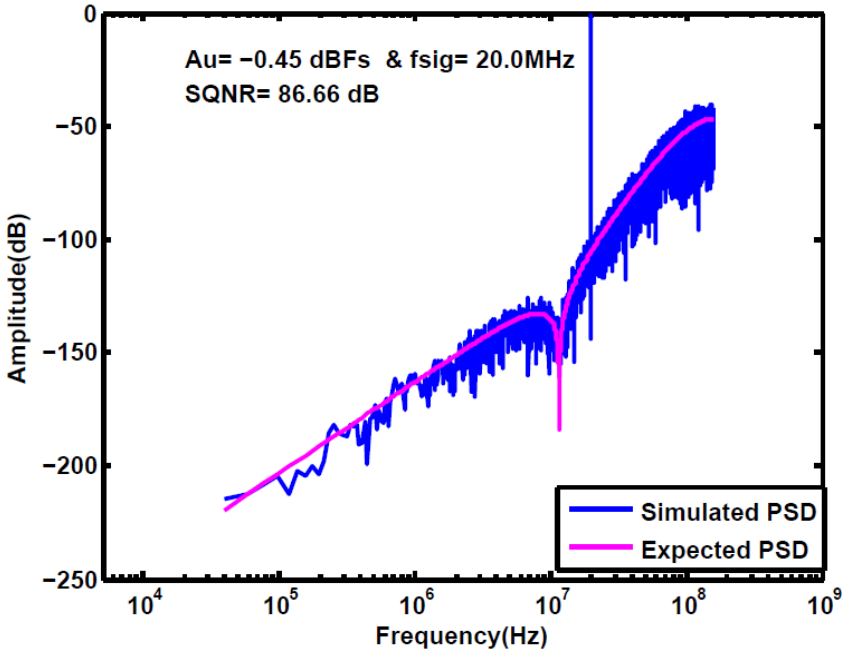

Figure 4.17: Ideal SQNR simulation result.

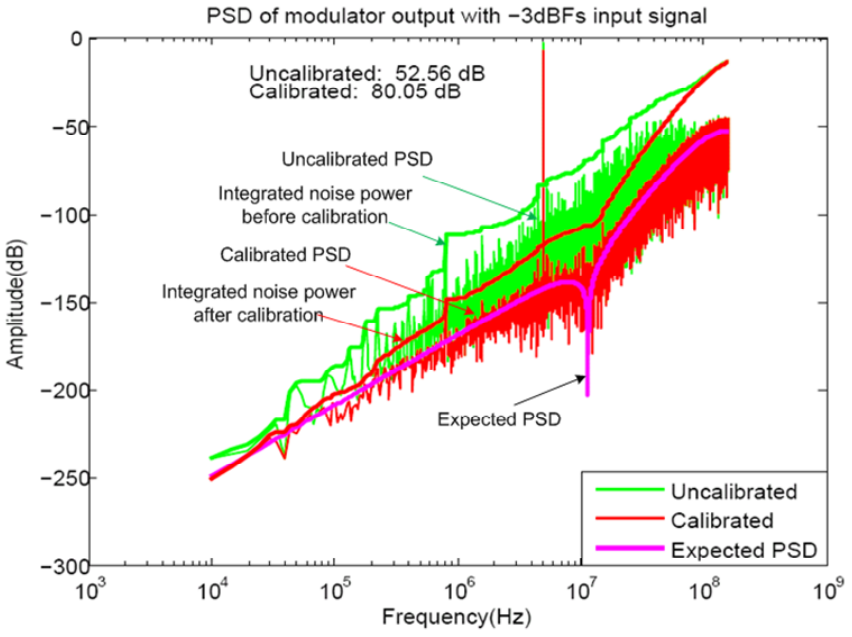

Figure 4.18: The modulator output spectrum with/without background calibration.

4.3.4 Noise Budget

After choosing the modulator architecture and system parameters, the noise specification of each building block has to be decided for targeted signal-to-noise ratio (SNR) and input dynamic range (DR). In the proposed MASH 2-2 structure, each low-order modulator is very stable, and can accommodate input signals approaching to 0dBFs, so the peak SNR should be at least 72dB for a higher than 12bit resolution requirement.

Besides the quantization noise, there are many other noise sources that limit the modulator performance, such as jitter noise, thermal noise, flicker noise, DAC mismatch error and some other non-ideal effects. Since noises generated after the first integrator will be noise shaped and are usually negligible compared to the noise of input stage, noise analysis is then focused on the first integrator input.

By including the tuning circuit and digital calibration filter in the modulator, performance degradation due to integrator RC time-constant variation can be negligible. However, the mismatch error among main feedback *DAC* unit-cells increases the noise floor as well as the harmonic-tones. By including the *DWA* block [34] in the feedback DAC, both the harmonic tones and noise are shaped out of the pass band, and then the DAC matching requirement can be much relaxed. Assuming a 0.1% DAC mismatch, Fig. 4.19 shows the simulation results before and after *DWA* correction.

Also, the DAC mismatch depends heavily on the transistor size and layout technique. Improving its accuracy is much easier than reducing the uncontrollable external jitter noise and it won't increase power dissipation. The noise budget for DAC mismatch error is then set to 4%. The first DAC mismatch error is less than 0.1%, while others are less than 1% to save chip area.

For a DT ΔΣ ADC, the noise floor is usually dominated by wideband thermal noise for low power design. However, for a stand-alone CT ΔΣ ADC, the noise floor is often limited by two noise sources: jitter noise and thermal noise. Since the

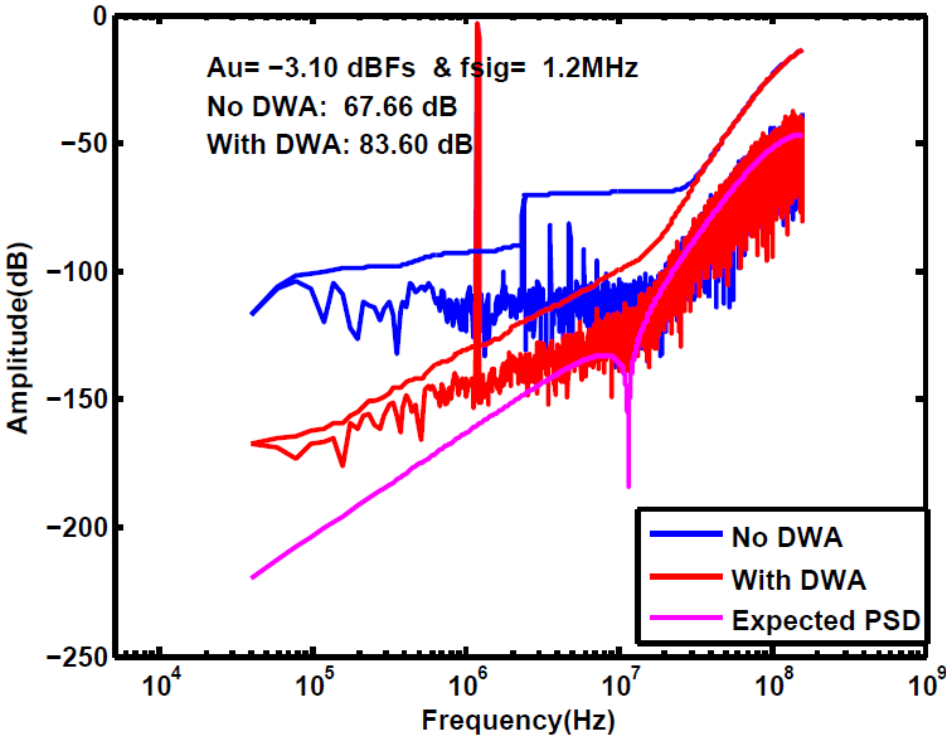

Figure 4.19: Simulated output spectrum with 0.1% DAC mismatch.

clock jitter relies on the quality of the external clock source and the following driving circuitry, careful selection of clock generator and a safe noise budget become necessary. In our design, 36% total noise is allocated to clock jitter ($\sigma_{jitter} < 2.5\,ps$), and 46% total noise to wideband thermal noise and flicker noise. Another 10% of the noise budget is left for other non-ideal effects, such as comparator offset and hysteresis effect, integrator and adder finite bandwidth effects, etc. The noise budget is summarized in Table 4.3.

Table 4.3: Noise budget for the CT modulator.

Noise source	Noise Budget	Simulated SNR	Design Parameter
Quantization Noise	4%	>86dB	-0.5dBFs input
Quantization Noise + DAC Mismatch	8%* (4%)	>83dB	$\sigma_{DAC1}(I) = 0.1\%$

Quantization Noise + Jitter noise	40% (36%)	>76dB	$\sigma_{jitter} < 2.5ps$
Quantization Noise + thermal/flicker noise	50% (46%)	>75dB	Input resistor + DAC + 1st Opamp
Other Noises	10%		Comparator offset and hysteresis effect, et al.

* The numbers outside the parenthesis in the noise budget column refer to the total noise in consideration.

4.4 Circuit-level Implementation

With the proposed architecture and system parameters, the CT 2-2 MASH was designed using a 90nm CMOS logic process. For a 1.2V power supply voltage, the full-scale input signal range was set to 1V.

The whole circuit diagram is shown in Fig. 4.20. In the first stage modulator, the loop filter is realized with active-RC integrators for better linearity performance, and a first-order low-pass filter is merged with the input of the first integrator to solve the STF out-of-band peaking issue. For the first stage modulator output and the MASH output, the STF simulation results before and after adding the LPF are shown in Fig. 4.21. By choosing a 3.125ns RC time constant, both STFs exhibit low-pass filtering characteristic. The attenuation at the edge of signal band is less than 1dB, and thus negligible. Also, the open-loop current summation scheme is used for the adder to reduce the extra delay in the loop. The test signal is generated by the on-chip Pseudo-Random Bit Generator (PRBG) and injected into the adder. In the second stage modulator, linearity requirement of the loop filter is much relaxed and then the Gm-C integrators are used for fast operation. The integrator time constant variation is manually controlled by tuning the integration capacitor value, and all the feedback DACs are realized using NRZ current DACs for a good compromise between jitter noise and integrator slew-rate requirement.

To simplify the design, the digital processing blocks, such as noise cancellation filters and digital calibration filter, are only realized with MATLAB. Therefore, the follow discussions will focus on the design of analog building blocks.

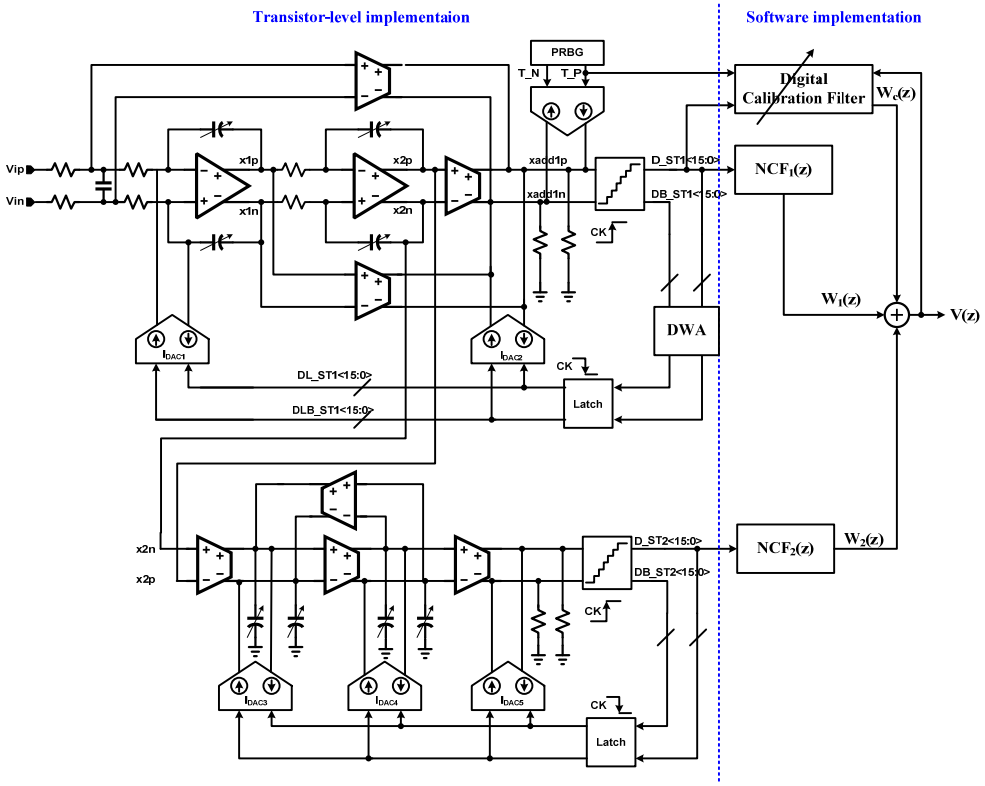

Figure 4.20: Circuit diagram of the CT 2-2 MASH.

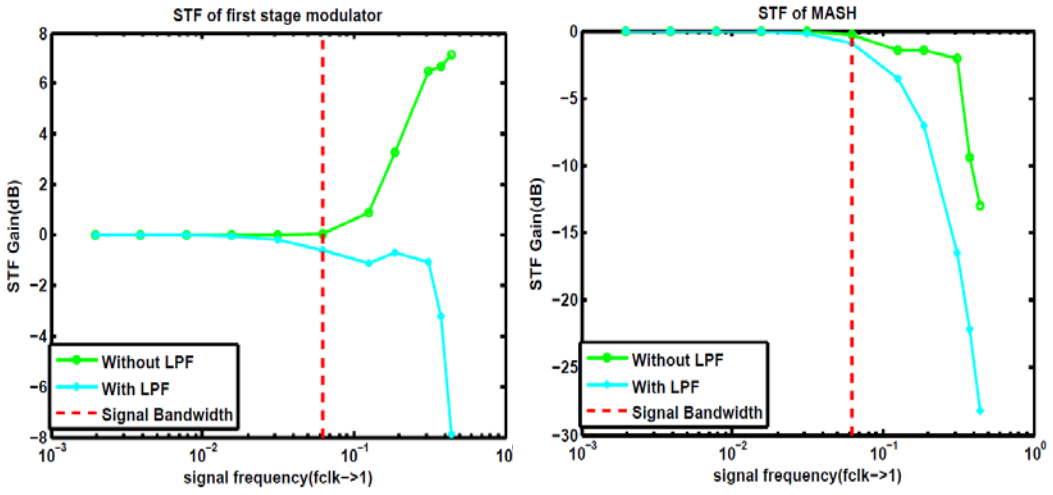

Figure 4.21: STFs of the 1st stage modulator and MASH.

4.4.1 The Input Stage Circuit

The input stage circuitry is the most critical part of the modulator. Any error generated by these circuit blocks (noise, integrator gain variation and insufficient opamp gain bandwidth etc) will transmit to the modulator output without any noise shaping. As is shown in Fig. 4.22, the input stage contains input resistors with filtering capacitor, current feedback DAC (IDAC), fully-differential amplifier and the integration capacitor with 4bit tuning accuracy etc.

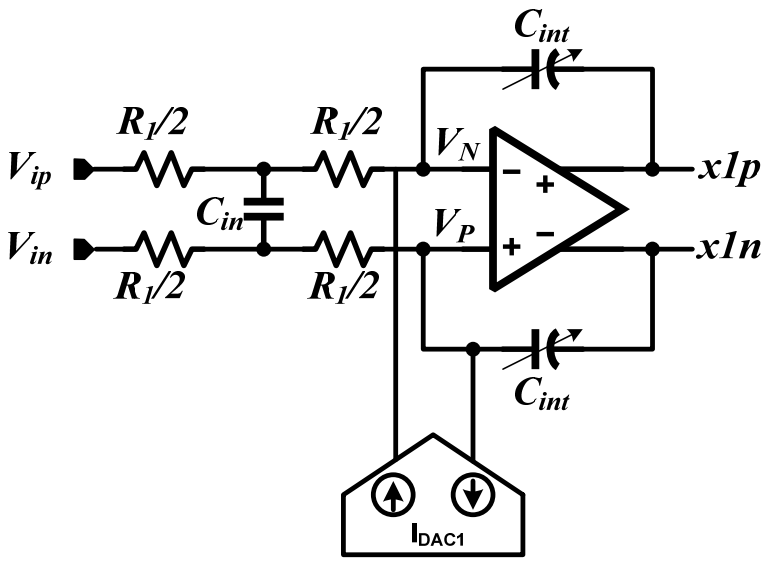

Figure 4.22: The diagram of input stage circuit.

4.4.1.1. Current Feedback DAC

Fig. 4.23 shows the circuit diagram of the current feedback *DAC* and its biasing circuit. The M_{CN} and M_{CP} transistors are used to compensate for the gate leakage current in deep-submicron transistors. C_P and C_N are two off-chip capacitors which can filter out the noise generated by the voltage and current reference circuits and biasing circuit itself. There are 16 identical unit-cells for the *IDAC*. In each unit-cell, the cascode transistor is used to increase the output resistance of current

mirror. Meanwhile, *PMOS* and *NMOS* current sources are controlled by the complementary switches to charge or discharge the integrator capacitor.

The sizing of *IDAC* current source transistors ($MN_{0\sim15}$ and $MP_{0\sim15}$) is determined by the matching requirement. For two *MOS* transistors with same dimension and biasing conditions, the relative drain current mismatch error is given by [35]

$$\sigma^2_{\Delta I/I} = \sigma^2_{\Delta\beta/\beta} + \left(\frac{2}{V_{gs} - V_{th}}\sigma_{\Delta V_{th}}\right)^2 \tag{4.38}$$

Here, $\Delta\beta/\beta$ and ΔV_{th} are the current factor β and the threshold voltage V_{th} mismatches between these two transistors. These mismatch errors are process dependent, and inversely proportional to the active device area. For a given process, they can be empirically estimated as

$$\sigma^2_{\Delta\beta/\beta} = \frac{A^2_\beta}{WL} \qquad \text{and} \qquad \sigma^2_{\Delta V_{th}} = \frac{A^2_{V_{th}}}{WL} \tag{4.39}$$

A_β and $A_{V_{th}}$ are process dependent coefficients.

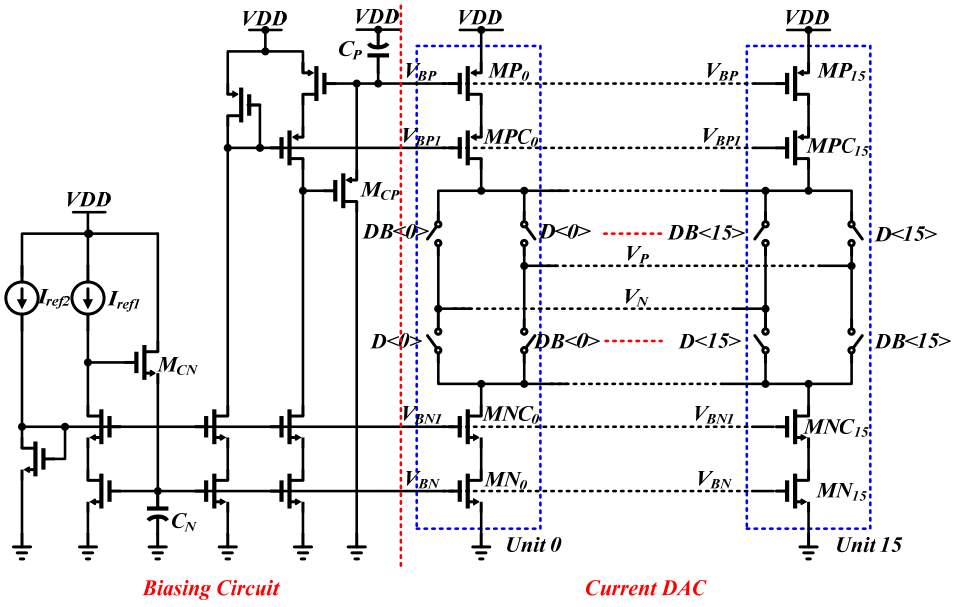

Figure 4.23: The circuit diagram of current feedback DAC.

With Eq. 4.38 and Eq. 4.39, the size of transistors for a given matching requirement, $\sigma(I)/I = 0.1\%$ in our case, should satisfy [36][37]

$$WL \geq \frac{1}{2}\frac{A_\beta^2 + 4A_{V_{th}}^2 \big/ (V_{GS} - V_{th})^2}{\left(\sigma(I)/I\right)^2} \tag{4.40}$$

To estimate the noise *PSD* at the output of *IDAC*, the noises generated by the complementary switches and the cascode transistors (MNC_0-MNC_{15} and MPC_0-MPC_{15}) are often negligible because they are attenuated by the large output resistance of the current mirror transistors (MP_0-MP_{15} *and* MN_0-MN_{15}). The noise current of biasing circuit are also negligible because of the filtering capacitors C_P and C_N. Therefore, noises at *IDAC* output mostly come from MN_0-MN_{15} and MP_0-MP_{15}. A simplified circuit diagram for noise analysis is drawn in Fig. 4.24. During every clock cycle, the noise currents from *PMOS* and *NMOS* current sources will be transmitted to the *DAC* output V_P and V_N, and the total output noise current PSD is

$$i_{dac}^2(f) = \sum_{k=1}^{16} i_{d,n}^2(f) + \sum_{k=1}^{16} i_{d,p}^2(f) \tag{4.41}$$

Here,

$$i_d^2(f) = \frac{8}{3}kTg_m + g_m^2\frac{k_f}{2\mu C_{ox}^2 WL}\frac{1}{f} \tag{4.42}$$

For exacting matching requirements and wide signal band, the minimum size of *WL* is large, and then the corner frequency of flicker noise is very low compared to the signal bandwidth. So, in a wideband application, the thermal noise is usually the dominant component for the current DAC. The output noise current *PSD* can be simplified as

$$i_{dac}^2(f) = 16\times\frac{8}{3}kTg_{m,p} + 16\times\frac{8}{3}kTg_{m,n} \tag{4.43}$$

Since all current source transistors work at saturation region, $g_m = \frac{2I}{V_{dsat}}$ and the Eq. 4.43 can be re-written as

$$i_{dac}^2(f) = \frac{32kT}{3} I_{FS} \left(\frac{1}{V_{dsat,P}} + \frac{1}{V_{dsat,N}}\right) \tag{4.44}$$

Here, I_{FS} is the *DAC* feedback current when V_{DAC} is equal to the reference voltage of quantizer, V_{ref}. For the fully-differential circuit, V_{ref}=V_{FS}/2 and I_{FS} can be calculated as

$$I_{FS} = \frac{V_{FS}}{4R_1} \times k_{dac} \tag{4.45}$$

If $V_{dsat,p}$=$V_{dsat,n}$, the equivalent input noise voltage *PSD* of *IDAC* is

$$v_{n,dac}^2(f) = i_{dac}^2(f) \frac{\left|\frac{1}{sC}\right|^2}{\left|-\frac{1}{sR_1C}\right|^2} = \frac{16}{3} kT \times \frac{V_{FS}}{V_{dsat}} \times k_{dac} \times R_1 \tag{4.46}$$

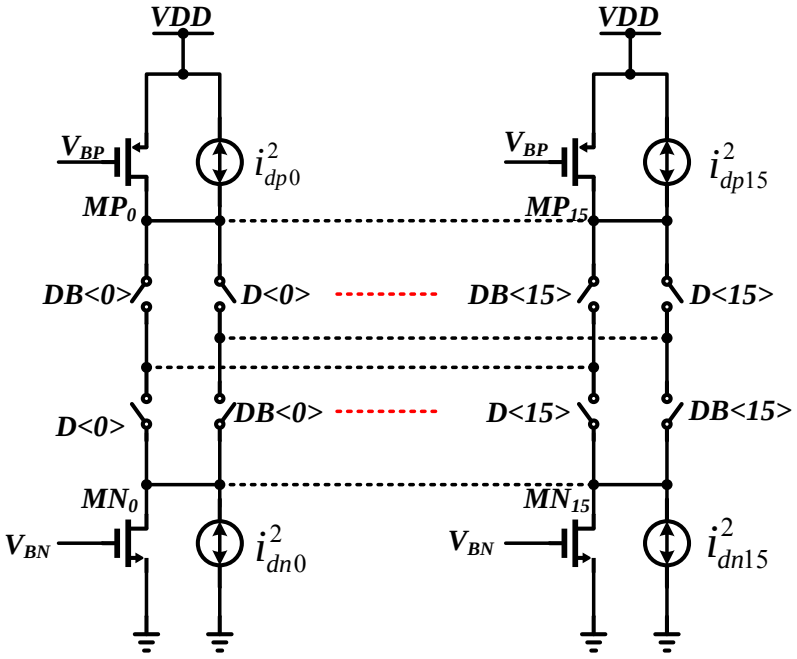

Figure 4.24: *IDAC* diagram for noise analysis.

4.4.1.2. Operational Amplifier

For a multi-stage ΔΣ modulator, the operational amplifier (opamp) for the integrator should have high dc gain as well as wide bandwidth to reduce the quantization noise leakage. By using the digital calibration filter, opamp design requirement can be much relaxed. With a 320MHz sampling clock, the 60dB dc gain and 1GHz UGBW are required for the opamp. For the 90nm CMOS process, it is hard to fulfill the dc gain requirement with a conventional single-stage telescope opamp or folded-cascode opamp, especially with the resistive loading at the integrator output. Therefore a two-stage opamp is designed. Fig. 4.25 shows the schematic of the amplifier. The first stage opamp is a folded-cascode amplifier, which provides suitable input common-mode voltage as well as 50dB dc gain; the second-stage common-source amplifier with miller compensation further increases the dc gain of the amplifier and maintains good phase margin for fast close-loop response. The output common-mode voltage is then sensed by resistor R_c. With the common-mode feedback circuit, the integrator output common-mode voltage is set to a reference voltage V_{CMO}, 0.7V.

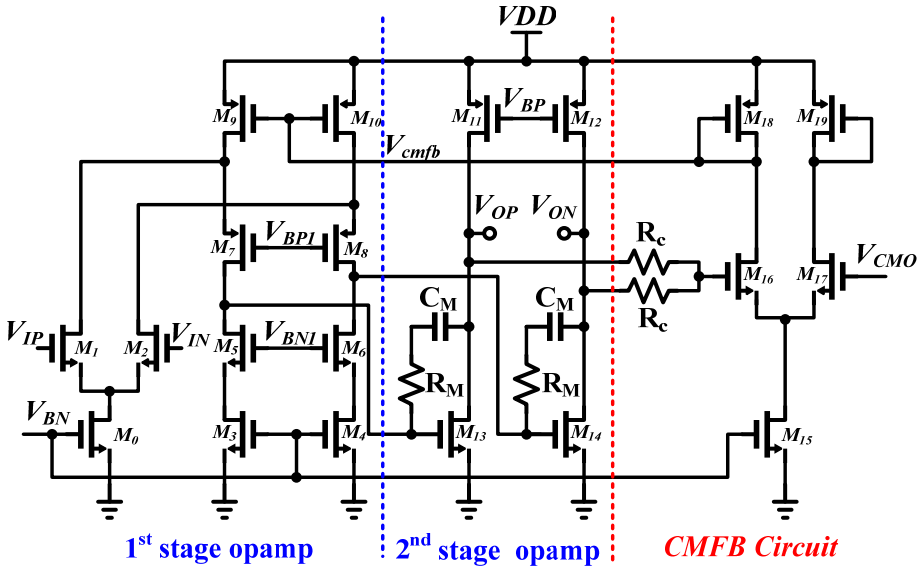

Figure 4.25: The amplifier schematic.

Noise generated by the opamp is also a limiting factor for modulator performance, and the dominant component comes from the first stage because the noises generated at following stage are shaped out of band and thus negligible. For a fully-differential input stage, the noise of M_0 is negligible because of the high input common-mode rejection ratio , noises of cascode transistors $M_{5,6}$ and $M_{7,8}$ are also greatly attenuated by the source degeneration transistors. Therefore, the equivalent input noise *PSD* of the opamp can be expressed as

$$v_{n,op}^2(f) = 2v_{n,M1}^2(f) + 2(\frac{g_{m3}}{g_{m1}})^2 v_{n,M3}^2(f) + 2(\frac{g_{m9}}{g_{m1}})^2 v_{n,M9}^2(f) \tag{4.47}$$

Here,
$$v_{n,i}^2(f) = \left(\frac{8kTg_{m,i}}{3} + \frac{k_f I_{ds}}{C_{ox} L^2} \frac{1}{f} \right) \Big/ g_{m,i}^2 \tag{4.48}$$

To achieve 1GHz bandwidth and low power dissipation, M_1 and M_2 work in the weak inversion region with minimum channel length, while others transistors work at the saturation region and use larger channel length for better matching accuracy and larger dc gain, so g_{m1} is often much higher than g_{m3} and g_{m9}. The equivalent input noise is dominated by the differential input pair, M_1 and M_2. On the other hand, the corner frequency of flicker noise can be in the order of sub-GHz, especially when minimum channel length is used. Increasing the size of transistor can reduce the flicker noise corner frequency but at the penalty of increased parasitic capacitance and thus reduced closed-loop feedback factor. So a design optimization has to be made among sizing, speed and power for the opamp. In our design, the flicker noise corner frequency of input transistor is set to around 6MHz. The equivalent input noise power of the opamp is actually dominated by flicker noise, which is six times larger than the thermal noise.

The opamp circuit structure in the second integrator is the same as the opamp of first integrator but the current at each branch is scaled down to reduce power dissipation. Since the noise of this opamp will be first order shaped, the noise contribution is negligible.

4.4.1.3 Detailed Noise Analysis

Fig. 4.26 shows a simplified block diagram of for the input stage with different noise sources, and the total noise power spectrum density (*PSD*) is the linear combination of independent noise sources:

$$v_{n,total}^2 = v_{n,R1}^2 + v_{n,dac}^2(f) + v_{n,op}^2(f) \tag{4.49}$$

For the input resistor R_1, the noise *PSD* can be simply expressed as $4kTR_1$ and the total input-referred noise PSD in differential circuit is

$$v_{n,R1}^2(f) = 8kTR_1 \tag{4.50}$$

Combined Eq. 4.46-4.50, the inband noise power can be given by

$$v_{rms}^2 = BW \times v_{n,R1}^2(f) + BW \times v_{n,dac}^2(f) + \int_0^{BW} v_{n,op}^2(f)df \tag{4.51}$$

and

$$\int_0^{BW} v_{n,op}^2(f)df \approx BW \times \frac{16}{3}\frac{kT}{g_{m1}} + 2\frac{k_f I_{ds}}{C_{ox}L^2}\frac{1}{g_{m1}^2}\ln\left(BW/f_L\right) \tag{4.52}$$

Here, f_L =0.1 is the lower bound frequency for flicker noise integral and $g_{m1} \approx I_{ds}/(2V_T)$ is the M_1 transistor input transconductance in sub-threshold region.

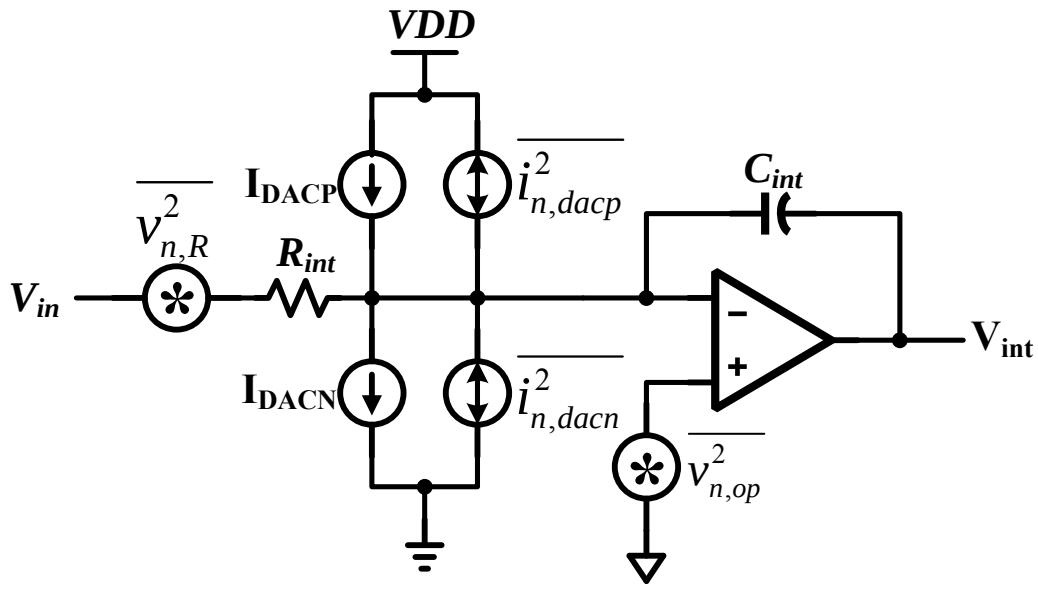

Figure 4.26: Block diagram of noise sources for the input integrator.

In the design, opamp noise contribution to the modulator is set to 10% of total noise, so the minimum input stage current of the opamp can be calculated by Eq. 4.52. Also, the noise generated by input resistor R_1 and feedback *IDAC* should be smaller than 36% of total noise, which means

$$\frac{V_{FS}^2/8}{\left(8kTR_1+\frac{16}{3}kTR_1\times\frac{1}{V_{dsat}}\times k_{dac}\right)\times BW}\geq 10^{7.644} \tag{4.53}$$

Since the Boltzmann constant k=1.38×10^{-23} JK^{-1}, for V_{FS}=1V, V_{dsat}=0.3V, k_{dac}=1.9 and BW=20MHz, the maximum input resistor R_1 at room temperature is 820 Ω. So R_1=625 Ω is chosen and the input filtering capacitor C_{in} is then equal to 5pF.

4.4.2 The Summation Circuit

As is shown in Fig. 4.20, a summation circuit is needed to add the integrators' output together with the direct feed-in signal, *DAC* feedback signal and dither signal. The adder has to be very fast because any delay of the adder increases the overall loop delay and thus degrades the noise-shaping and stability performance. A passive adder is fast but sensitive to the parasitic capacitances and kickback noise. The active adder with an opamp in closed-loop configuration has a small closed-loop feedback factor because of the multiple input branches, and the opamp should have very wide bandwidth and consume large power. Therefore, an open-loop low power active adder is used to realize the summation. Fig. 4.27 shows the circuit diagram of the adder. The summation operation is done in the current domain. The analog voltages (the modulator input signal and integrator output signals) are first converted into currents by transconductance cells (Gm1-Gm3), and the DAC feedback and dither signals are transformed from logic levels to currents by the current DACs. These currents are added together at the low impedance nodes *A* and *B*, and then converted back to voltage with resistor output loading. Since the *V-I* and *I-V* conversions are both realized with open-loop circuits, the adder can be very fast.

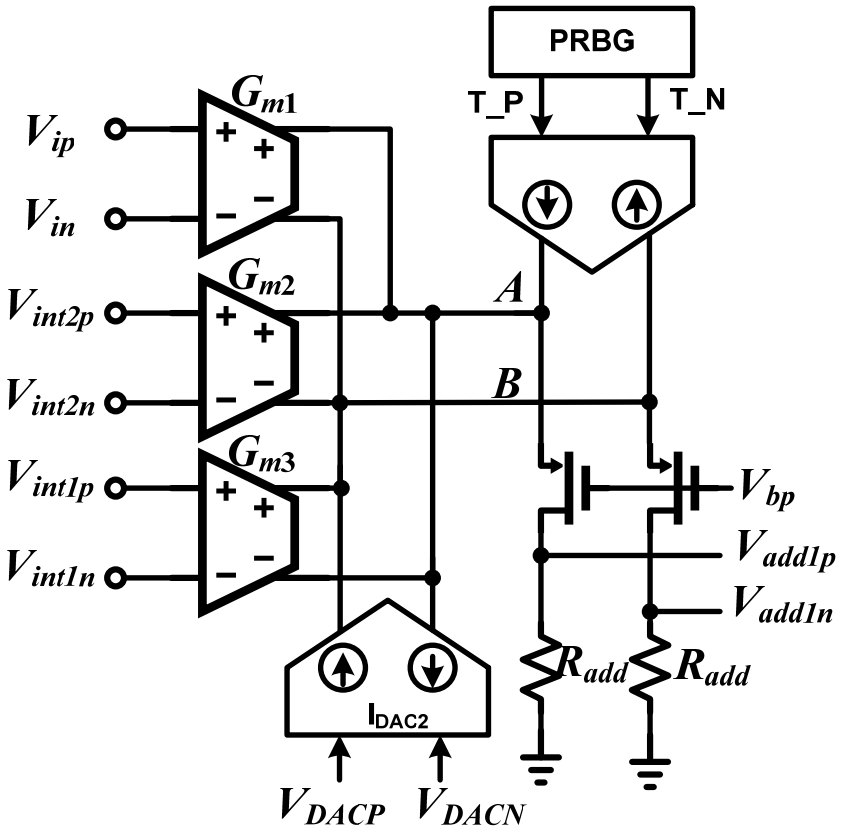

Figure 4.27: The circuit diagram of the current summation circuit.

4.4.2.1 Gm Cells

The schematic of *Gm* cell is shown at Fig. 4.28. The signal-related current is first generated by applying the input signals V_{IP} and V_{IN} to the resistor R through the source follow transistors M5 and M6, and the current will be transmitted to the current summation nodes (V_{OP} and V_{ON}) and then the adder output. By choosing the resistor ratio between R and R_{add}, the gain of each gm cell k_c can be set:

$$k_c = \frac{R_{add}}{R} \tag{4.54}$$

By using cascode transistors as the current sources, good linearity can be achieved for the Gm cells.

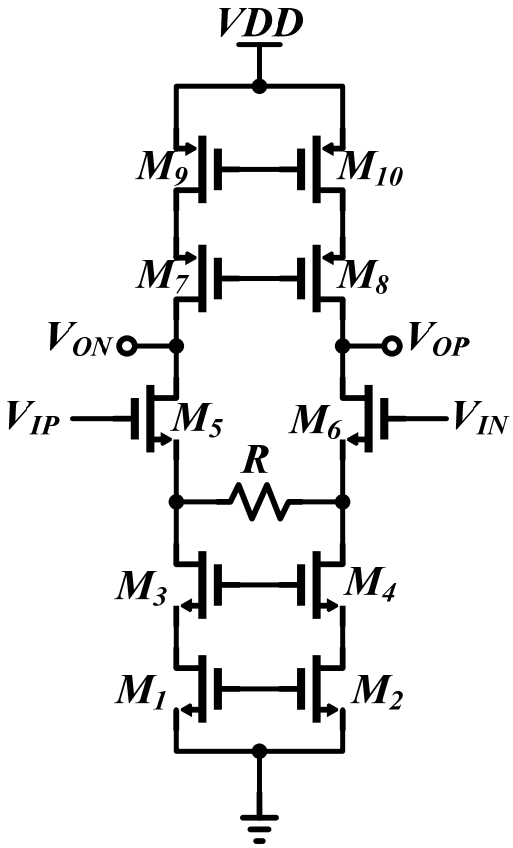

Figure 4.28: The schematic of Gm cell.

4.4.2.2 Dither Generator

To apply the digital calibration technique in the modulator, a pseudo-random and uniformly distributed dither signal has to be generated and applied to the adder through the current *DAC*. The pseudo-random bit stream generator can be realized using linear feedback shift register (LFSR) [38], which can modify itself on each rising edge of clock using feedback. Generally, there are two kinds of implementation for the LFSRs, Fibonacci type and Galois type. With only a few taps, the Fibonacci implementation generally achieves a faster clock speed than Galois counterpart. The maximum unrepeated sequence length is determined by the size of LFSR. For a LFSR with *N* registers, the maximum sequence is (2^N-1). Fig. 4.29 shows the designed LFSR, a Fibonacci-type implementation with 28

registers is used. The maximum sequence length is 268435455, which well fulfill the digital calibration filter requirement.

To prevent the designed LFSR from locking at all zero state, the preset and initiation operation has been done by an additional simple logic block.

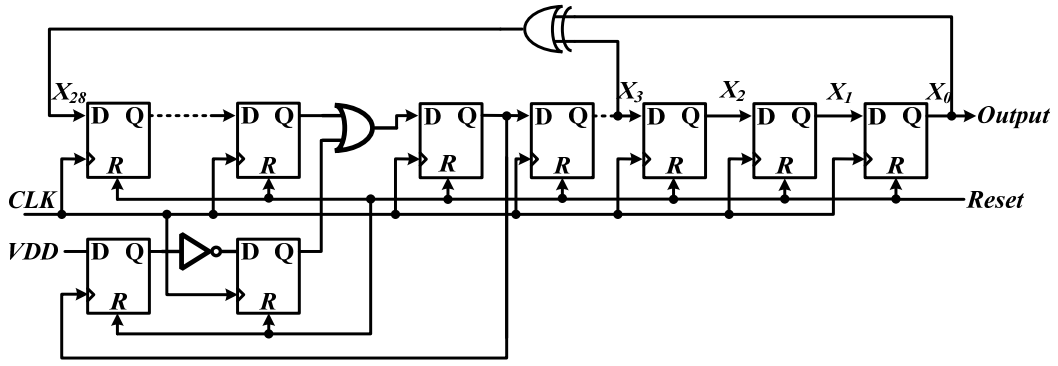

Figure 4.29: The block diagram of Fibonacci-type 28-bit LFSR.

4.4.3 Quantizer

The circuit diagram of the 4-bit quantizer is shown in Fig. 4.30. The comparators are realized as the pre-amplifier with S/H function, followed by the regeneration latches. To reduce the input parasitic capacitance of the quantizer, an interpolator [39][40] circuit is inserted between S/H circuit and the latches. So, the number of preamplifier can be reduced from 16 to 6, which reduces the input parasitic capacitance by 62.5%.

The schematic of S/H gain stage is shown at Fig. 4.31. The CK_2 (CK_{2D}) phase is the reset phase and CK_1 phase is the amplification phase. During CK_2 phase, the preamplifier is reset and opamp offset voltage is stored at the sampling capacitor. At the falling edge of CK_2, the differential input signal is sampled. At the rising edge of CK_1, the sampled signal is subtracted by the differential reference voltage and the residue voltage is amplified by a gain equal to 5. With this gain stage, the offset voltage of following regenerative latch is much reduced.

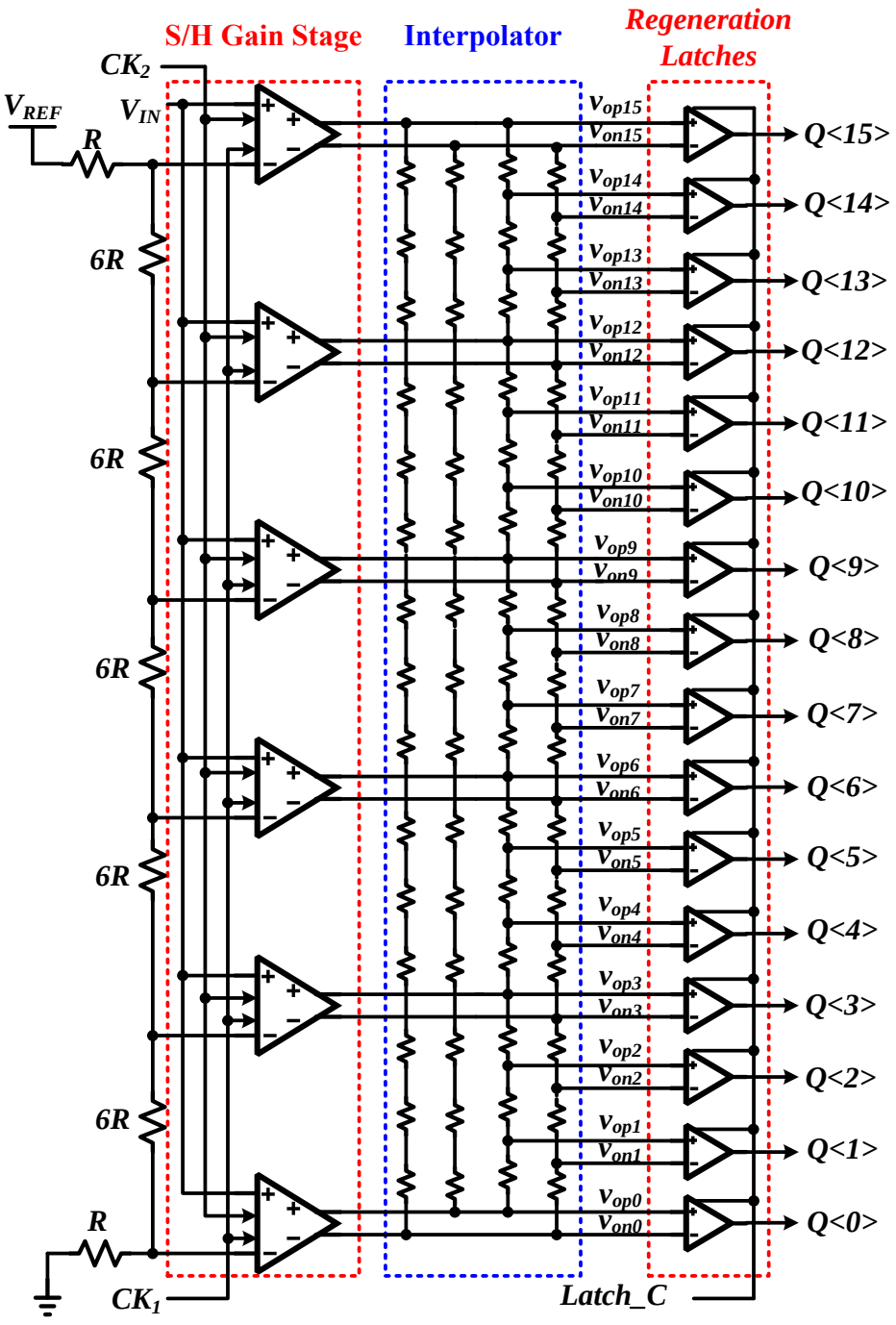

Figure 4.30: The circuit diagram of 4bit quantizer.

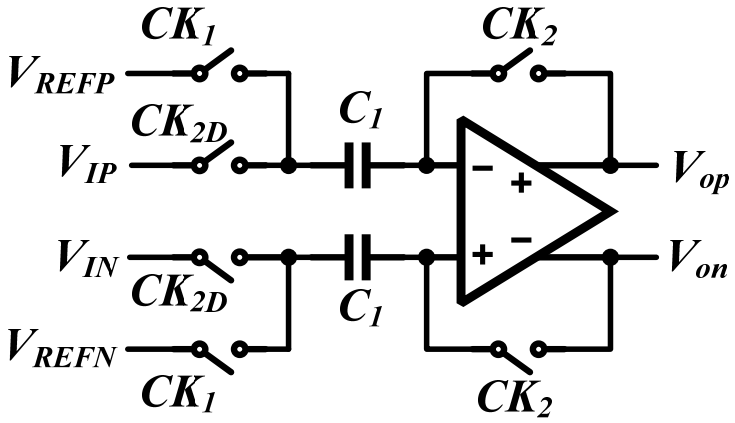

Figure 4.31: The schematic of S/H gain stage.

Fig. 4.32 shows the schematic of dynamic latch circuitry. It contains a clock controlled regenerative dynamic latch stage followed by a *RS* latch. The *Latch_C* is the enable signal for regenerative latch. When the CK_1 signal keeps high for a while, interpolator output voltages are settled and ready for comparison; the *Latch_C* signal becomes low and turns on M_5 and M_6 transistors. The latch input signals are amplified further to logic levels by the *PMOS* and *NMOS* regeneration

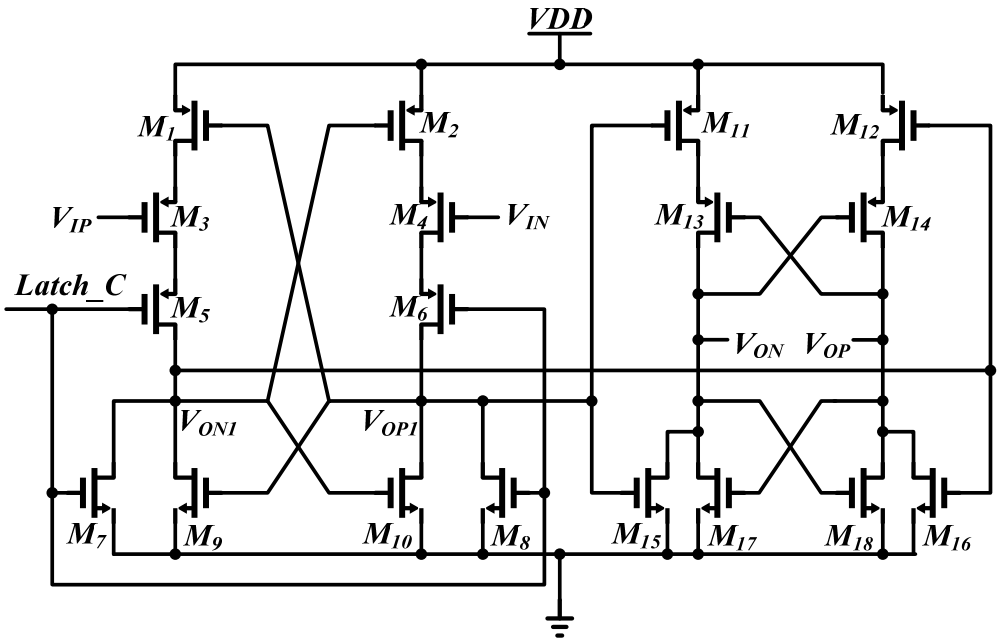

Figure 4.32: The schematic of regeneration latch.

pairs and the next stage *RS* latch. Meanwhile, M_1 or M_2 will be cut off when V_{OP1} or V_{ON1} becomes *VDD*, and there is no static current after the latch makes its decision. Power can thus be saved. When *Latch_C* becomes high, M_5 and M_6 are cut-off and nodes V_{ON1} and V_{OP1} are discharged to ground. The decision voltages are then held by the *RS* latch.

4.4.4 Data-Weighted Averaging (DWA) Circuit

The basic idea of DWA algorithm [34] is to select the DAC elements sequentially. Fig. 4.33 shows an example of element selection in a 2-bit DAC for a given input sequence V(n). It uses a pointer to keep track of the end point that previous element selections and then starts from next point as new element selection. Thus the DAC mismatch error can be first-order high-pass shaped out of the signal band. Some tones might still show up in the output spectrum for certain input dc values and frequencies. However, the injected test signal at the quantizer input behaves as a dither signal for the modulator, and the tone issue using DWA scheme is greatly improved.

The implementation of a fast DWA technique [41] is shown in Fig. 4.34 and the corresponding timing diagram is shown in Fig. 4.35. At the falling edge of *Latch_C*, the quantizer generates the new output signals Q<15:0>. The updated value will be barrel shifted a certain value based on the addressing pointer *SEL*<3:0>. At the same time, the new pointer location is calculated by adding the addressing pointer *SEL*<3:0> with the shifting information V_B<3:0>, which is extracted from the quantizer output by the Thermal-to-Binary (T2B) decoder. At the falling edge of CK_1, the feedback DAC signals V<15:0> are generated from the barrel-shifter output and fed back to the input integrator and the adder. When CK_1 returns to high, V<15:0> is hold and then PTR registers are trigged with rising edge of PTR signal, the pointer *SEL*<3:0> is then updated for next cycle barrel-shifter addressing. Also, the first stage modulator output ADC_ST1<4:0>

will be updated at the falling edge of CK_2. Except the DWA block, similar timing and operation are used for the second stage modulator.

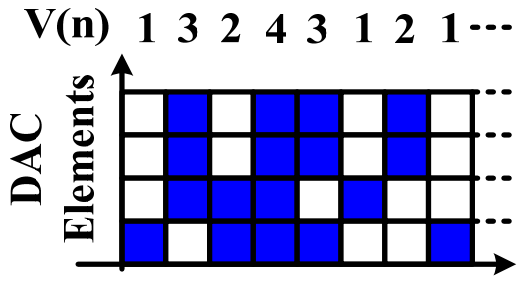

Figure 4.33: The unit-element selection example for the DWA algorithm.

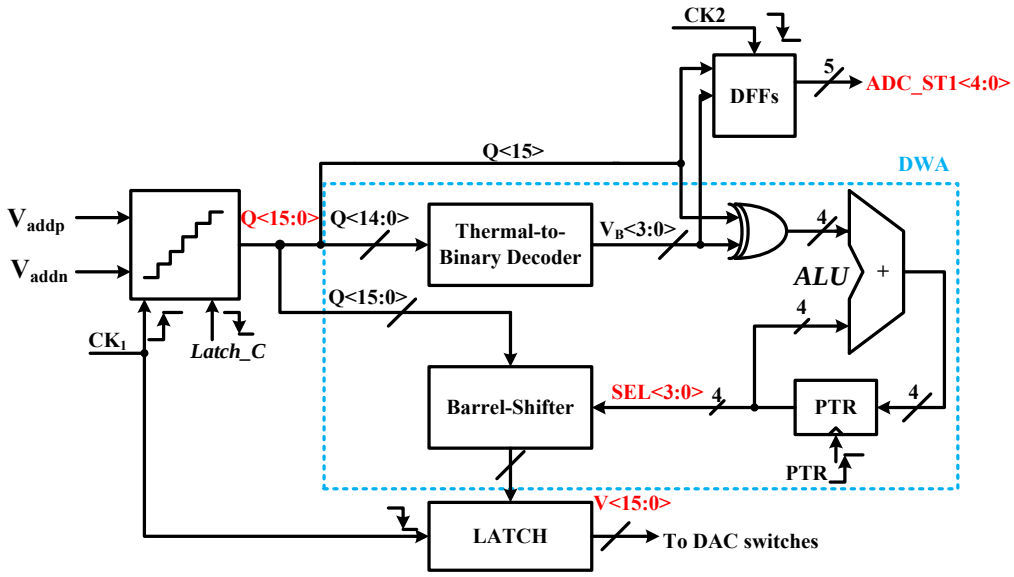

Figure 4.34: The block diagram of DWA circuitry.

Since the T2B decoding, *ALU* calculation and pointer registers are located out of the modulator loop and can be done within one clock cycle, the *DWA* timing is much relaxed. Meanwhile, the barrel-shifter delay is small in 90nm process and can be easily absorbed during the quantization phase, so no DWA-related loop delay is introduced to the modulator.

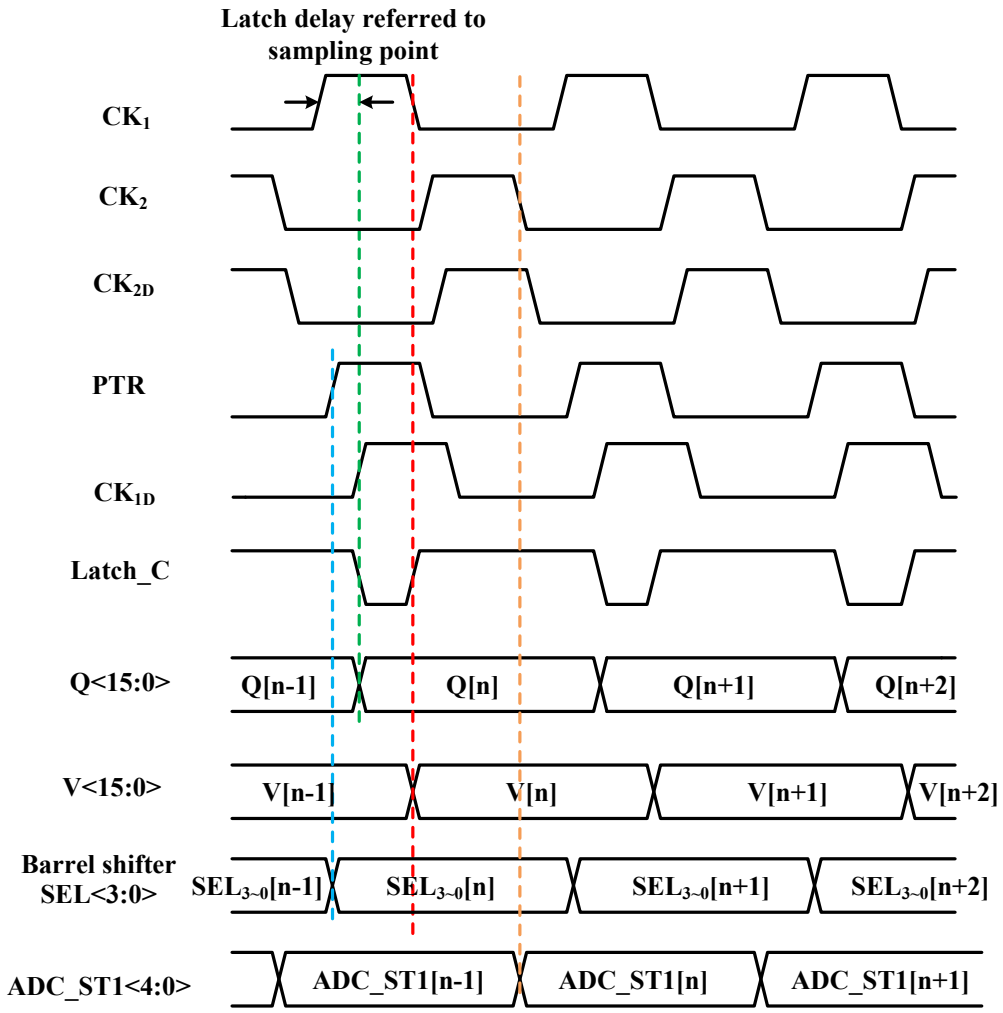

Figure 4.35: Timing diagram of the Quantizer and DWA circuitry.

Fig. 4.36 shows T2B block diagram realized using *Wallace-Tree* topology, which has highest hardware efficiency and can effectively kill the "bubbles" in the quantizer output.

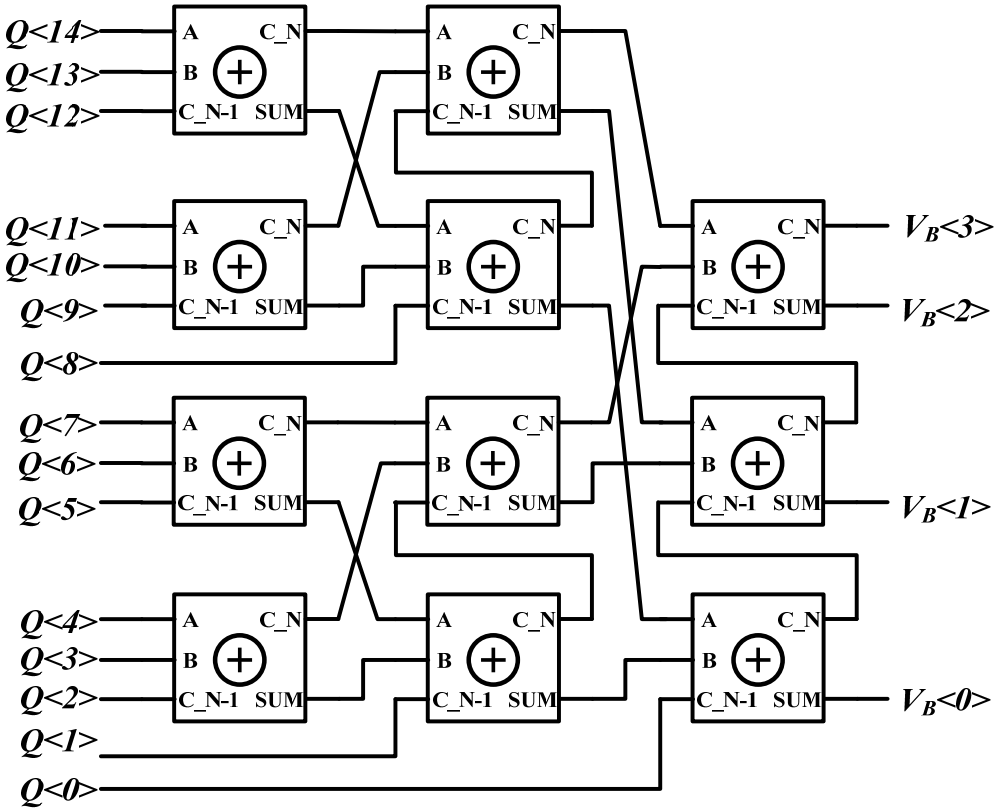

Figure 4.36: Block diagram of T2B encoder.

4.4.5 Clock Generator

The block diagram of clock generator circuit is shown in Fig. 4.37. A 640MHz clock signal is first divided by two and generates two complementary clocks CK_A

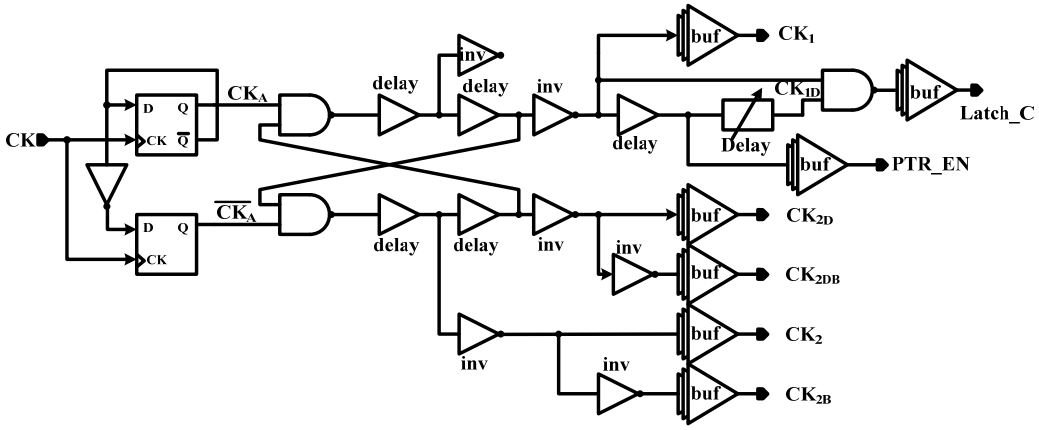

Figure 4.37: Block diagram of clock generator circuit.

and $\overline{CK_A}$ with 50% duty cycle. Different clock signals used in the modulator are then produced with these two clocks. A variable delay cell (Fig. 4.38) is inserted in the clock generator to adjust the delay time between CK_1 and *Latch_C*.

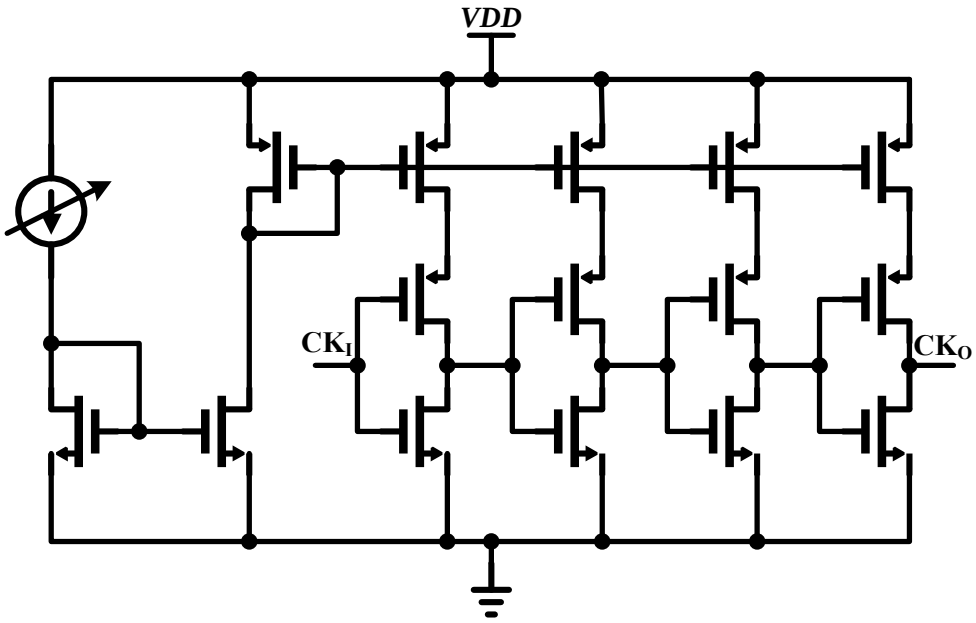

Figure 4.38: Schematic of the variable delay cell.

4.4.6 Gm-C Integrators

In second stage modulator, the integrator linearity requirement is greatly relaxed. Therefore, the loop filter is implemented using the Gm-C integrators for fast operation. Fig. 4.39 shows the circuit diagram of Gm-C integrators. Similar to the summation circuit, the input voltages are first converted into currents and then added together at node A and B. The summation current will then again transform to integrator output voltage by charging or discharging the output capacitors. Since the output nodes are now high-impedance nodes, the common-mode feedback circuit is necessary to stabilize the output common-mode voltage.

Fig. 4.40 shows the schematic of common-mode feedback circuit. The output common-mode voltage is extracted by a simple RC network and then compared

with a reference voltage V_{CMO} using a simple one-stage opamp. The level-shifting circuit (M_1-M_4) is used to isolate integrator outputs from common-mode sensing *RC* network, which sinks ac current and increases additional parasitic capacitance. Meanwhile, the capacitor C_f is placed between the input and output of single-stage opamp and this additional feed-forward path can compensate for the high frequency phase lag for the opamp. Better phase margin and then better stability and settling behavior can be achieved.

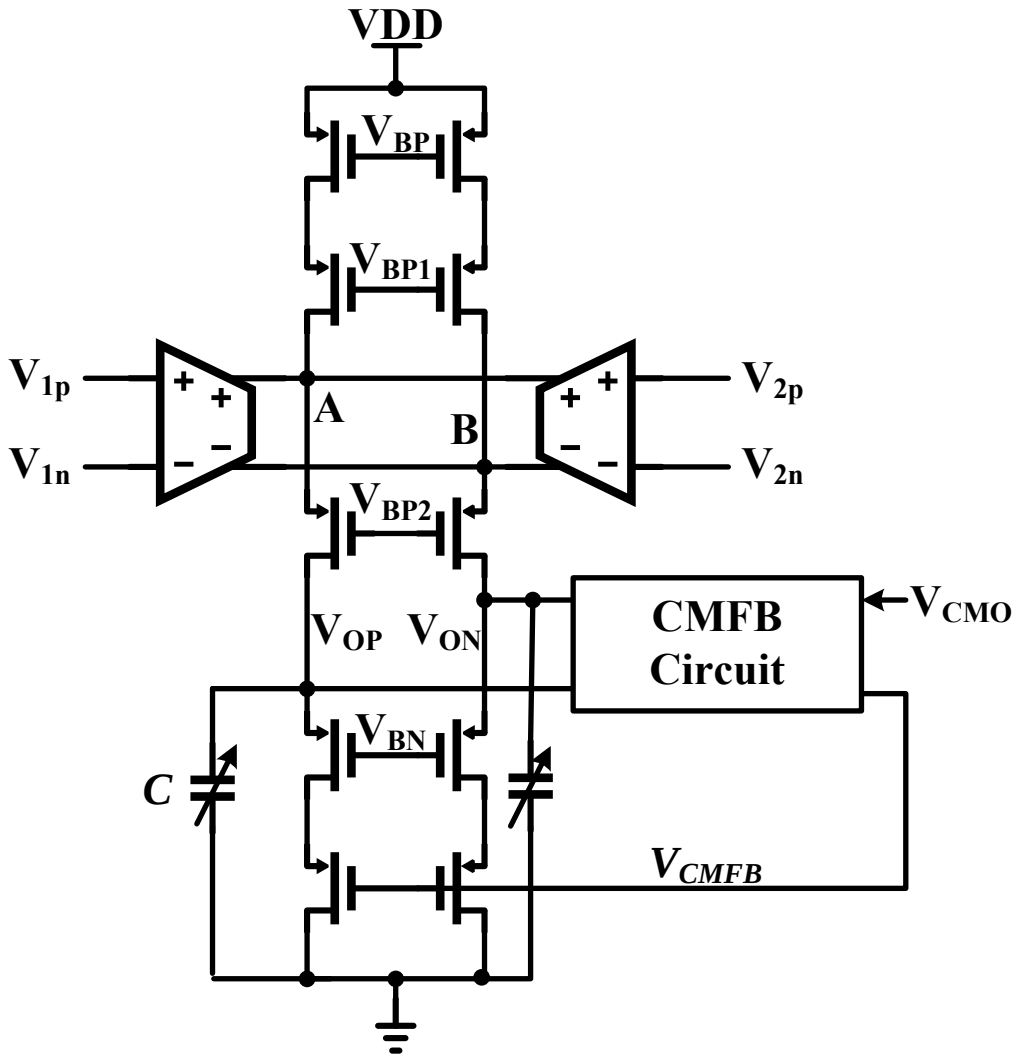

Figure 4.39: Circuit diagram of Gm-C integrator.

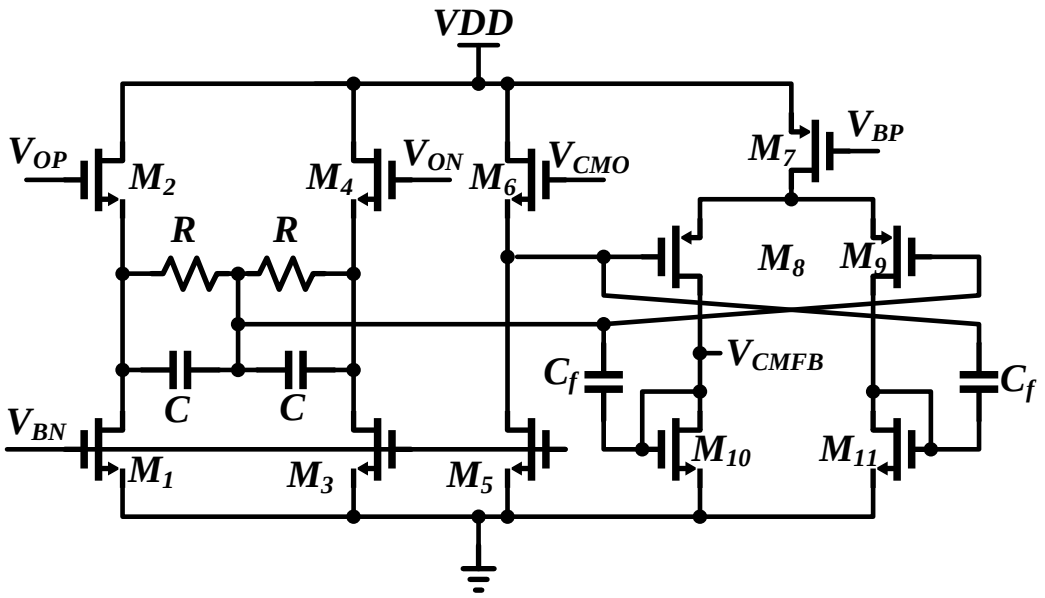

Figure 4.40: The schematic of CMFB circuit.

4.4.7 Timing Constant Tuning.

As is discussed at Chapter 2, the integrator *RC* time constant variation will degrade noise-shaping ability and in some cases make the modulator unstable. So, a time-constant tuning circuit is necessary to optimize modulator performance. In our design, the capacitor tuning scheme is used. Fig. 4.41 shows the 4-bit capacitor

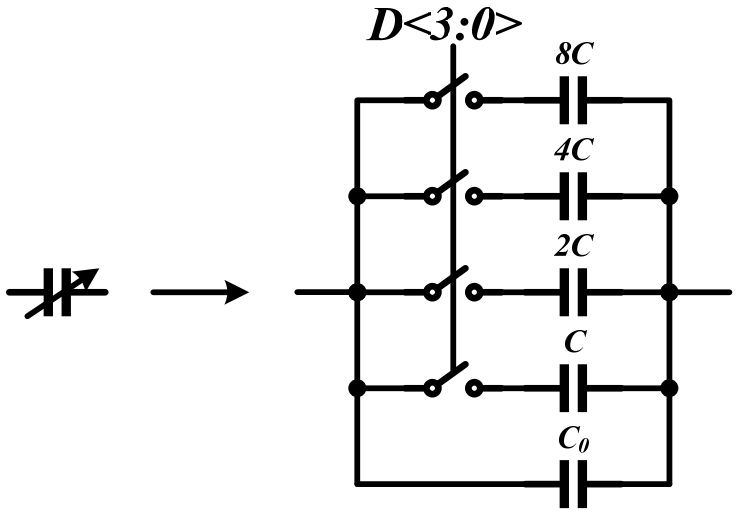

Figure 4.41: The 4-bit capacitor tuning array.

tuning circuit diagrams. The capacitor C_0 sets the minimum capacitor value and the other binary weighted capacitors are controlled by 4 bit digital word. So the total in-use capacitor value is equal to

$$C_{\text{int}} = C_0 + \sum_{i=0}^{3} D_i C_i \tag{4.55}$$

The integrator time constant is the product result of resistor and capacitor, so the minimum capacitor value is required when both R and C have the same largest variations, +15% in our case.

$$1.15C_{\min} \times 1.15R = RC_{ideal} \tag{4.56}$$

Similarly, the maximum capacitor value is required when R and C have -15% variations

$$0.85C_{\max} \times 0.85R = RC_{ideal} \tag{4.57}$$

Therefore, the tuning range of capacitor should satisfy

$$0.75C_{ideal} < C_{\text{int}} < 1.384C_{ideal} \tag{4.58}$$

With 4-bit binary tuning scheme, the tuning accuracy is around 4% and can satisfy our design requirements.

4.5 Layout Design and Simulation Results

The proposed wideband CT 2-2 MASH is a mixed-signal system, which contains not only the analog blocks (e.g., the loop filters) but the sampled blocks (e.g., the DACs and quantizers) and digital blocks (e.g., DWA, PRBG and Interface circuit etc.), and hence the layout design is very challenging. To achieve high linearity and high resolution, many undesirable issues such as the device and wiring mismatch, well proximity and STI stress effect [42], signal path parasitic and cross-talk digital noises, etc. have to be carefully considered. Fig. 4.42 shows the finalized floor plan of the modulator and the corresponding layout is shown in Fig. 4.43. The active area excluding I/O pads is around 0.7mm^2.

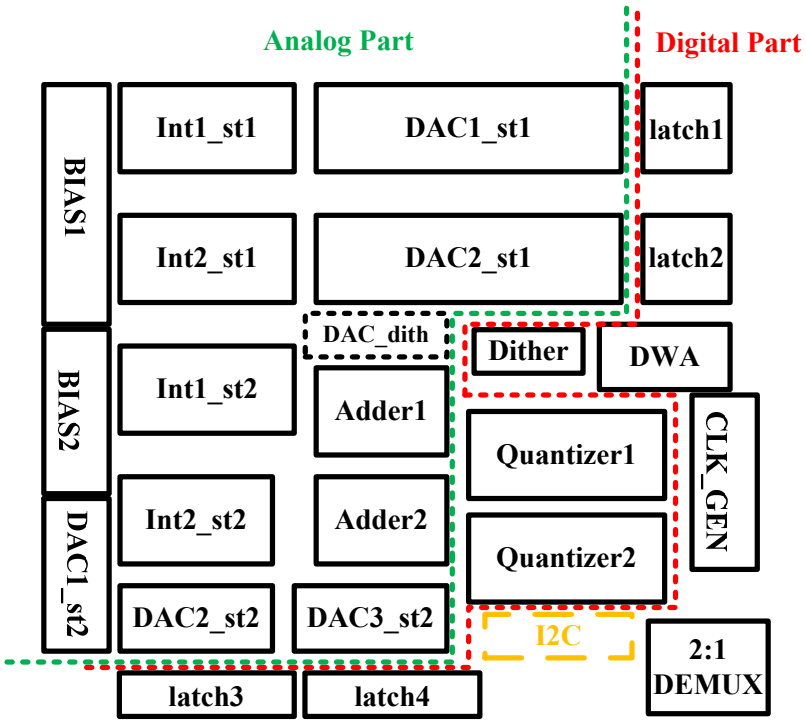

Figure 4.42: Floor plan of CT 2-2 MASH.

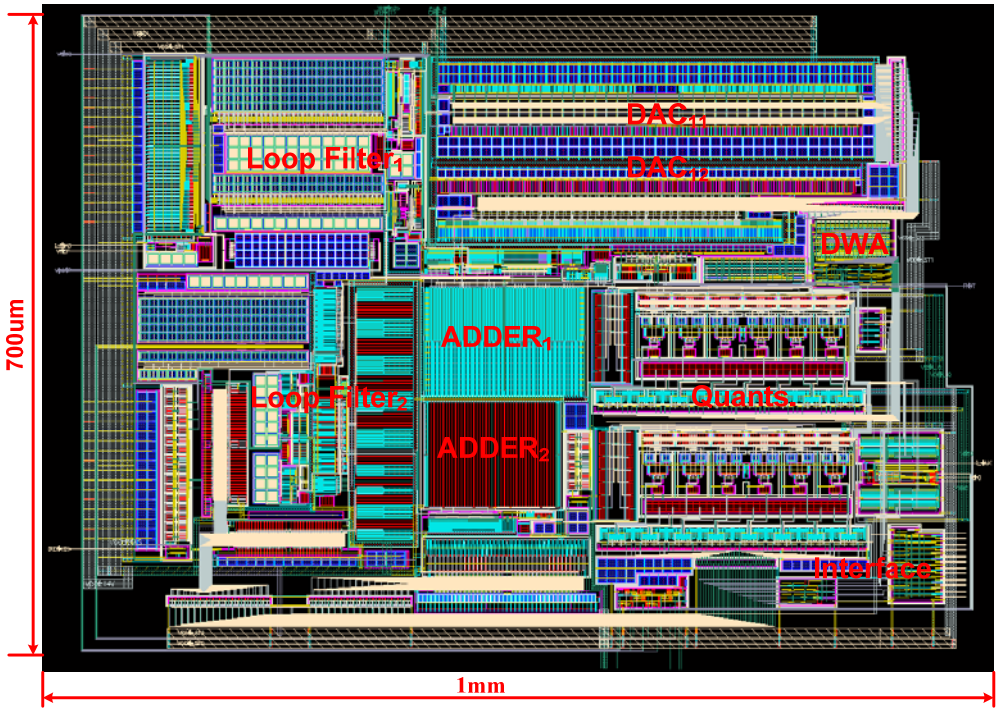

Figure 4.43: The core layout of CT 2-2 MASH.

For performance verification, the post-layout simulation results have been checked. With a 0dBFs, 1.1MHz sine-wave input signal, Fig. 4.44 shows the simulated output spectrum of overall modulator. More than 11bit resolution can be achieved before the digital calibration filter is applied. Due to the extremely long simulation time, the calibration technique has to be verified with the measurement results.

The second integrator output spectrum simulation result is shown in Fig. 4.45. Again, for the 0dBFs, 1.1MHz sine-wave input, the signal amplitude is attenuated by around 28dB, which validates the proposed low-distortion technique.

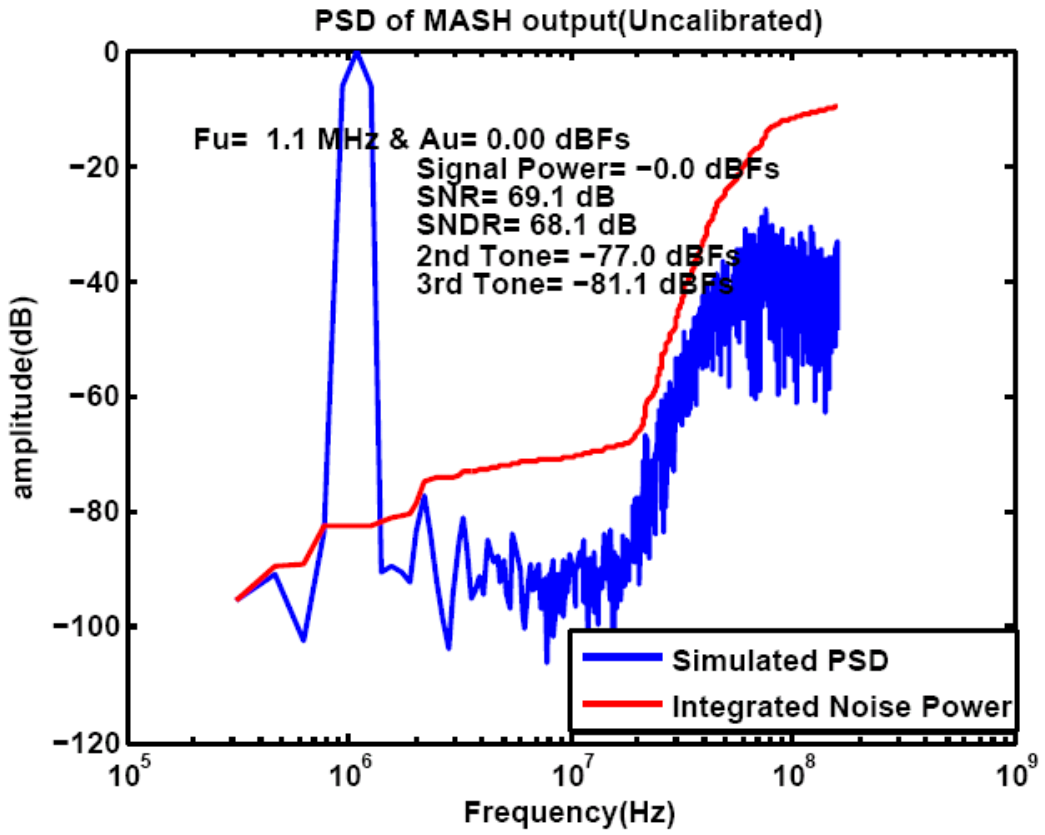

Figure 4.44: Simulated output spectrum of CT 2-2 MASH (Before calibration).

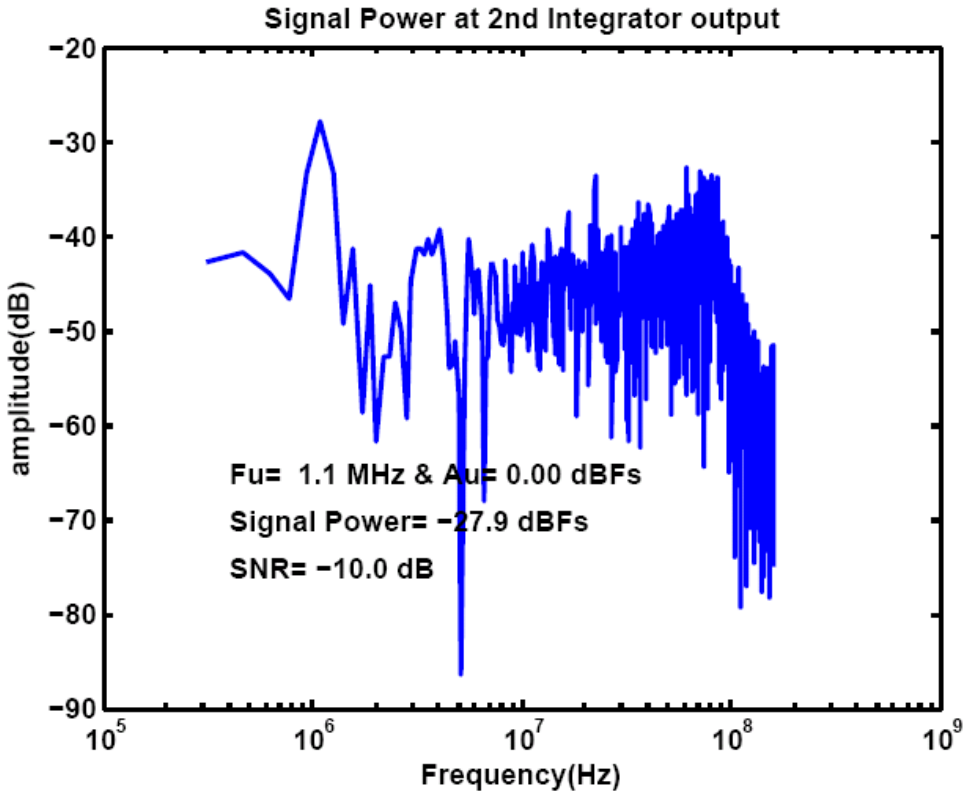

Figure 4.45: Simulated output spectrum at 2nd integrator output.

4.6 Conclusions

A 20MHz BW, 12 bit resolution CT cascade ΔΣ modulator has been described in this chapter. A new low-distortion technique and new adaptive digital calibration topology are proposed to improve the performance of the CT 2-2 MASH. Detailed circuit implementations are also described. The whole modulator is designed in a 90nm CMOS Logic process, and simulation results verify the proposed ideas.

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CHAPTER. 5 NOISE COUPLED CONTINUOUS-TIME ΔΣ A/D CONVERTERS [1]

The noise-coupling technique successfully used in discrete-time delta-sigma ADCs is extended to the realization of continuous-time delta-sigma ADCs, resulting in improved quantization noise shaping. The operation and design of these circuits is discussed in detail. To verify the proposed design methodology, a second-order continuous-time delta-sigma modulator with noise coupling was designed and simulated.

5.1 Introduction

High-accuracy wide-band delta-sigma (ΔΣ) analog-to-digital converters with low power dissipation are key components used in wired and wireless communication systems, consumer electronics, radar systems and medical applications. There is much ongoing effort to find novel architectures and circuit design techniques that can efficiently deal with these design requirements. Recently, the noise-coupling technique was introduced by K. Lee et al. [2] to enhance quantization noise shaping in discrete-time (DT) delta-sigma modulators. As is shown in Fig. 5.1, if the quantization noise is extracted and then coupled to the loop filter output after a one-cycle delay, a first-order noise-shaping enhancement can be achieved. Combined with the low-distortion topology [3], the noise-coupled technique has been applied to several chips and the resulting ADCs [4-6] demonstrate excellent linearity and good power efficiency. Currently, there is increasing interest in building ΔΣ modulators using continuous-time (CT) circuitry for the loop filter, because of their inherent anti-aliasing filtering performance and lower bandwidth requirements. These properties are particularly important in low-power and wide-band applications. Further improvements in the power efficiency and performance can be expected if the noise-coupling technique can also be used for CT ΔΣ ADCs.

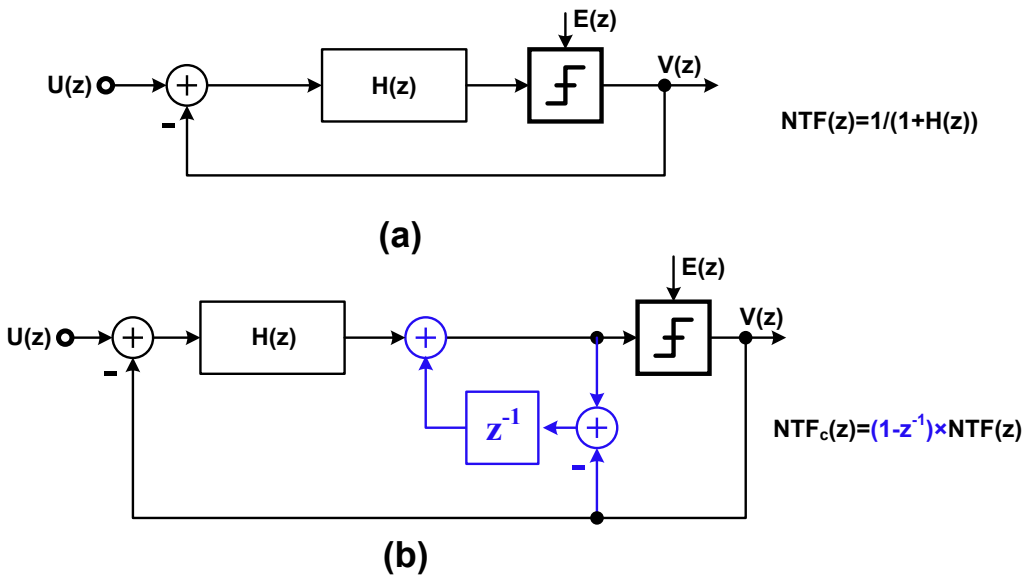

Figure 5.1: The block diagram of (a) conventional ΔΣ modulator (b) noise-coupled ΔΣ modulator.

The chapter is organized as follows. Section 5.2 introduces the noise-coupling technique for continuous-time ΔΣ ADC, and its operation principle and circuit realization are discussed. In Section 5.3, a design example is described to verify the effectiveness of the proposed scheme. Section 5.4 summarizes the conclusions.

5.2 The Continuous-Time Noise-Coupled ΔΣ ADC

5.2.1. Noise-Coupling Principle in CT ΔΣ ADC

The block diagram of a continuous-time ΔΣ modulator is illustrated in Fig. 5.2a, and its equivalent discrete-time model is shown in Fig. 5.2b .These two kinds of modulators process the input signal in different ways. For the DT ΔΣ modulator, the input signal is sampled prior to entering the modulator loop, and its out-of-band noise is aliased into the signal band after sampling. It will go through the same path as the desired input signal, without any filtering in the signal band. Hence, a front-end anti-aliasing filter is usually required. By contrast, the CT ΔΣ modulator carries out the sampling just before the quantizer. As a result, the aliased high-frequency components will be treated just as the quantization noise,

i.e. attenuated by the loop gain, and hence the loop performs an anti-aliasing filtering. On the other hand, the CT ΔΣ modulator is not as simple to design as DT ΔΣ modulator, because it contains both CT and DT blocks, and hence the design must be performed in the s- and z-domains. However, the noise-shaping ability for a ΔΣ modulator is determined solely by the feedback loop characteristics. If the CT and DT ΔΣ modulators' open-loop responses from the sampled quantizer output $V(z)$ to the sampled quantizer input $Y(z)$ are made the same, then the modulators exhibit similar closed-loop dynamic behavior. Thus, their stability and noise-shaping performances are the same. This allows a design technique for a CT ΔΣ modulator using the impulse-invariant transformation (*IIT*) [7]. The necessary condition for matched dynamic performance is

$$Z^{-1}\{H_d(z)\} = L^{-1}\{H_{dac}(s)H_c(s)\}|_{t=nT_s} \tag{5.1}$$

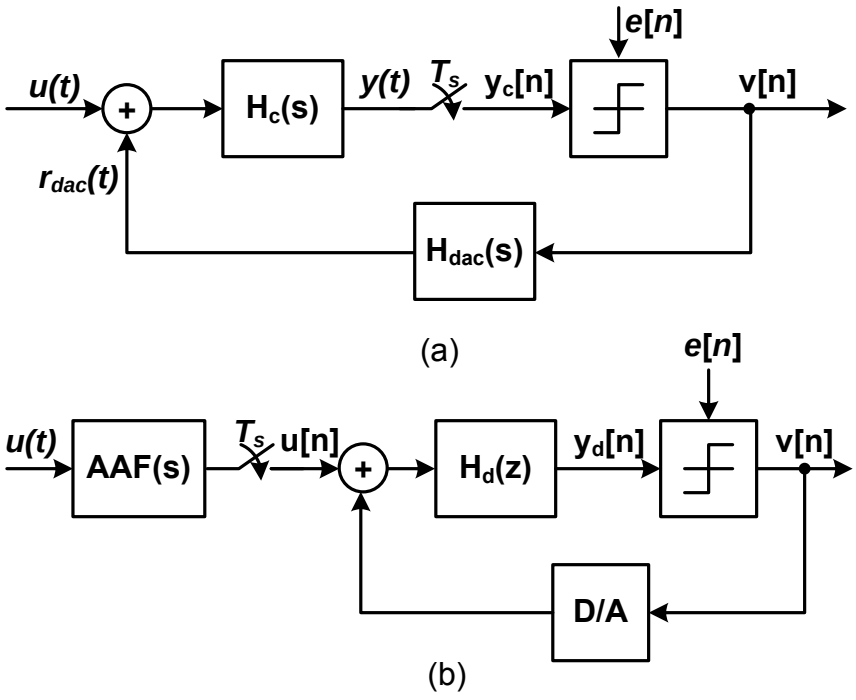

Figure 5.2: (a) The block diagram of a general CT ΔΣ modulator

(b) The equivalent block diagram of the DT ΔΣ modulator.

Here, Z^{-1} denotes the inverse Z-transform operation, and L^{-1} the inverse Laplace transform.

Noise coupling techniques can also be applied to increase the noise-shaping order of CT ΔΣ modulators. Fig. 5.3 shows the block diagrams of noise-coupled DT and CT ΔΣ modulators. To compare and analyze the loop dynamic behavior, their corresponding open-loop models are also shown in Fig. 5.4. There are two input signals to the adder preceding the quantizer: one is the loop filter output, and the other the delayed quantization noise fed back into the loop.

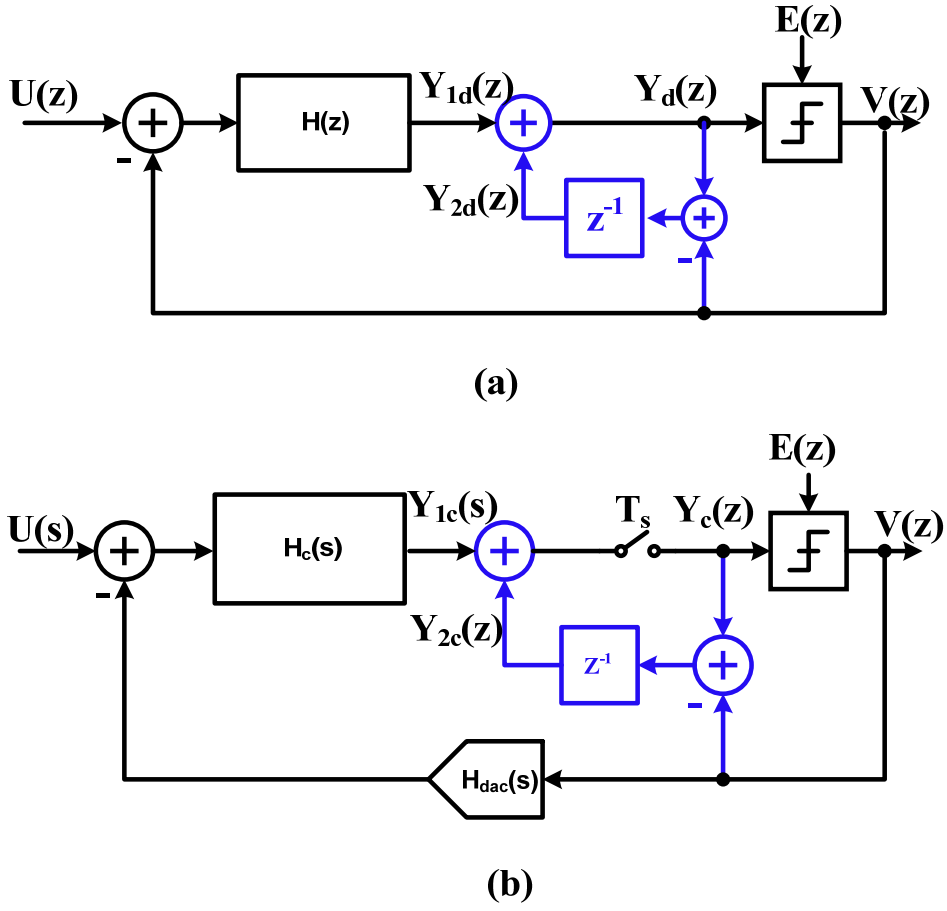

Figure 5.3: (a) Block diagram of a noise-coupled DT ΔΣ modulator.
(b) Noise-coupled CT ΔΣ modulator.

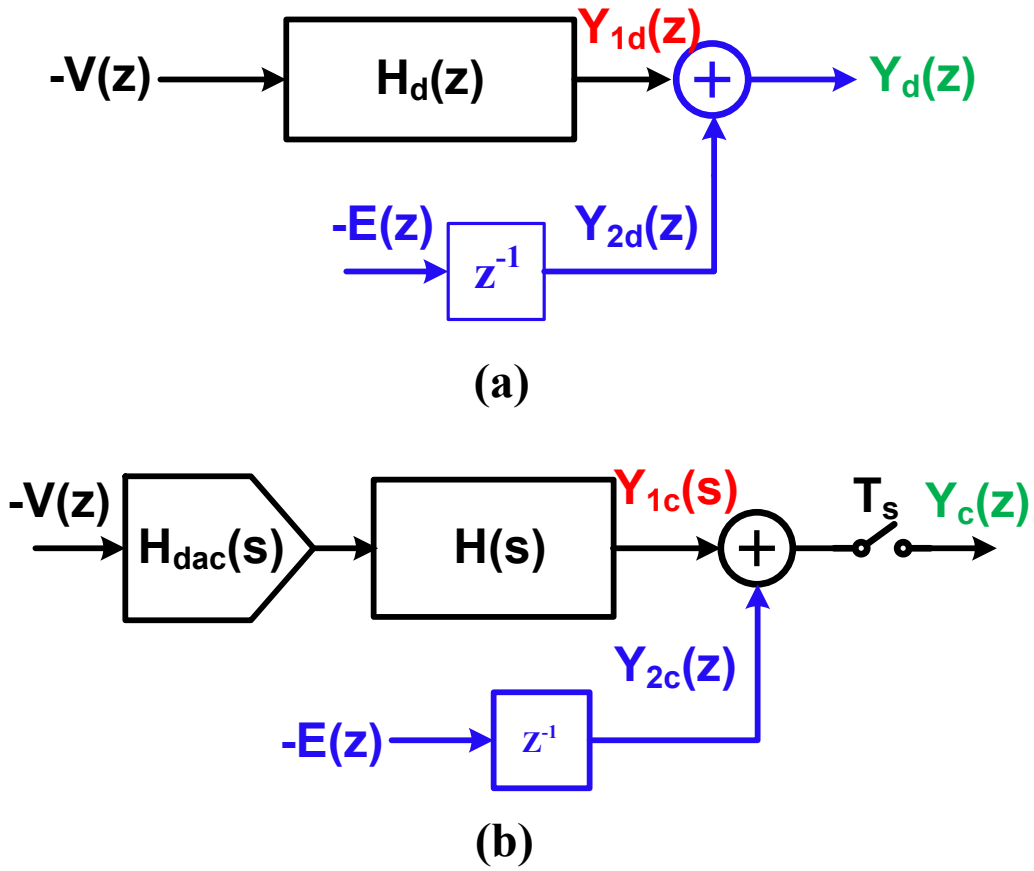

Figure 5.4: (a) Open-loop noise-coupled DT ΔΣ modulator.
(b) Open-loop noise-coupled CT ΔΣ modulator.

So, for the DT noise-coupled ΔΣ modulator, the sampled input signal of the quantizer is given by

$$y_d[nT_s] = Z^{-1}\{Y_{1d}(z)\} + y_{2d}[nT_s] \tag{5.2}$$

Here,

$$Y_{1d}(z) = H_d(z)V(z) \tag{5.3}$$

$$y_{2d}[nT_s] = -e[(n-1)T_s] \tag{5.4}$$

Similarly, for the CT ΔΣ modulator, the sampled input signal of the quantizer is

$$y_c[nT_s] = L^{-1}\{Y_{1c}(s)\}|_{t=nT_s} + y_{2c}[nT_s] \tag{5.5}$$

Here,

$$Y_{1c}(s) = H_{dac}(s)H(s)V(z) \tag{5.6}$$

$$y_{2c}[nT_s] = -e[(n-1)T_s] \tag{5.7}$$

Since $y_{2d}[nT_s]$ and $y_{2c}[nT_s]$ represent the same delayed quantization error, if Eq. 5.1 is satisfied then the two modulators have the same open-loop responses and the same $V(z)$, so also the same closed-loop stability and noise-shaping properties.

5.2.2. Stability Analysis

As what is described in Eq.5.5, the open-loop response of a noise-coupled CT ΔΣ modulator contains the delayed quantization noise. The stability performance is not clear when compared with a conventional structure. In order to simplify the discussion, the equivalent behavior model is presented in Fig. 5.5.

The noise-coupled CT ΔΣ modulator block diagram is redrawn in Fig. 5.5(a). It contains circuit blocks in CT domain, including the feedback DAC and CT loop filter, and others in DT domain such as the quantizer and coupling branches. The adder is a hybrid block, which sums the CT loop filter output and DT delayed quantization noise and then generates a sampled value at the sampling instance for the input of the quantizer. If the sampler is moved from adder output to the CT loop filter output, as is shown in Fig. 5.5(b), the adder is now a complete DT circuit block. The adder output still has the same sampled values for the quantizer and this does not change the behavior of the modulator. Also, the quantization noise coupling branch can be further separated into two delayed branches, one delay branch is from the quantizer output to the adder input and the other delay branch is from the adder output to the adder input. The latter one is effectively a delay-free integrator. The final equivalent model is shown in Fig. 5.5(c).

The feedback loop filter transfer function $LTF(z)$ is

$$LTF(z)|_{U(s)=0} = \frac{Y_c(z)}{V(z)} = \frac{-H_d(z) - z^{-1}}{1 - z^{-1}} \tag{5.8}$$

And the CT noise-coupled ΔΣ modulator output is

$$V(z) = [U(s)H_c(s)]^* NTF(z) + (1 - z^{-1})NTF(z)E(z) \tag{5.9}$$

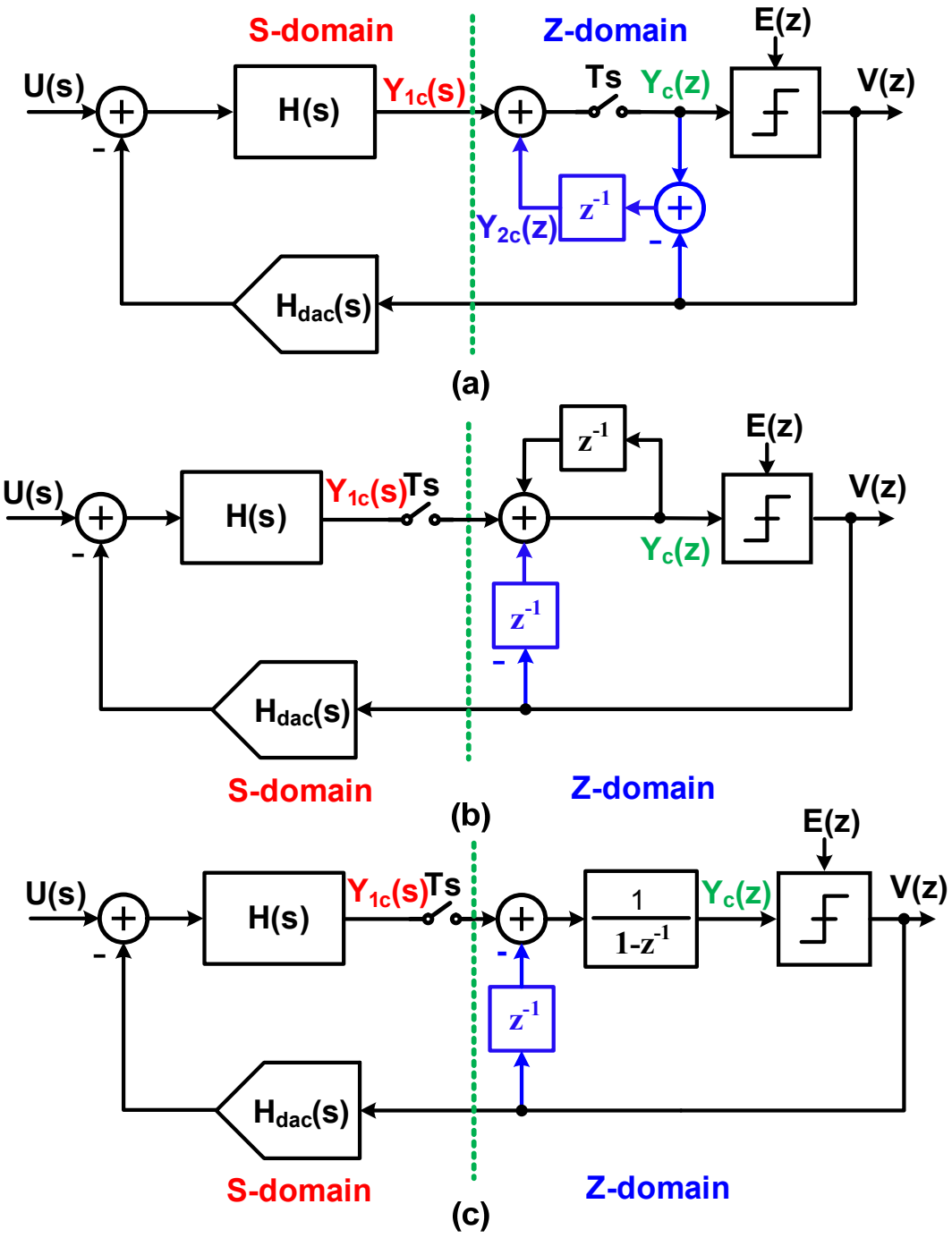

Figure 5.5: The equivalent model of noise-coupled CT ΔΣ modulator.

Here,

$$NTF(z) = \frac{1}{1 + Z[L^{-1}\{H_{dac}(s)H_c(s)\}|_{t=nT_s}]} = \frac{1}{1 + H_d(z)} \tag{5.10}$$

$E(z)$ is the quantization error of the quantizer, H_d (z) is the impulse-invariant transform of the loop filter $H_c(s)$ for the specified feedback *DAC* waveform $H_{dac}(s)$, and [ ]* represents the sampling operation.

As Eq. 5.9 shows, the order of *NTF* (z) is increased by one, and hence a first-order noise shaping enhancement is achieved. The resulting CT modulator has also increased the loop filter order by one. The stability performance is the same as the conventional DT modulators with N+1 order noise-shaping ability.

5.2.3. Noise-Coupling Realization

Since the design methodology of classical DT and CT ΔΣ ADCs is well known, the discussion here focuses on how to realize noise coupling in CT modulators. For DT ΔΣ ADCs, the quantization error can be easily extracted and coupled back into the modulator, because all integrators and adders are switched-capacitor circuits. However, in a CT ΔΣ modulator, the loop filter is usually implemented by active-RC or Gm-C integrators, while the adder before the quantizer usually uses an open-loop G_m cell or an active-R amplifier in a closed-loop configuration. This makes the quantization error extraction and coupling impractical, unless an additional S/H stage is included. To circumvent this problem, an active adder using switched-capacitor circuitry may be used. Then the quantization error extraction and coupling will be as convenient as in the DT ΔΣ prototype.

5.3 Design Example

As a demonstration of the proposed design technique, a second-order noise-coupled CT ΔΣ modulator was designed. The system level block diagram and circuit diagram are shown in Figs. 5.6 and 5.7. The feedback signal to the input integrator is generated by a non-return-to-zero (NRZ) DAC with a half-cycle delay. Both integrators used active-RC stages. The active adder was realized by a switched-capacitor circuit, as explained in the previous section. The adder output is sampled and then held for one cycle by the z^{-1} block. The full-cycle delay of the

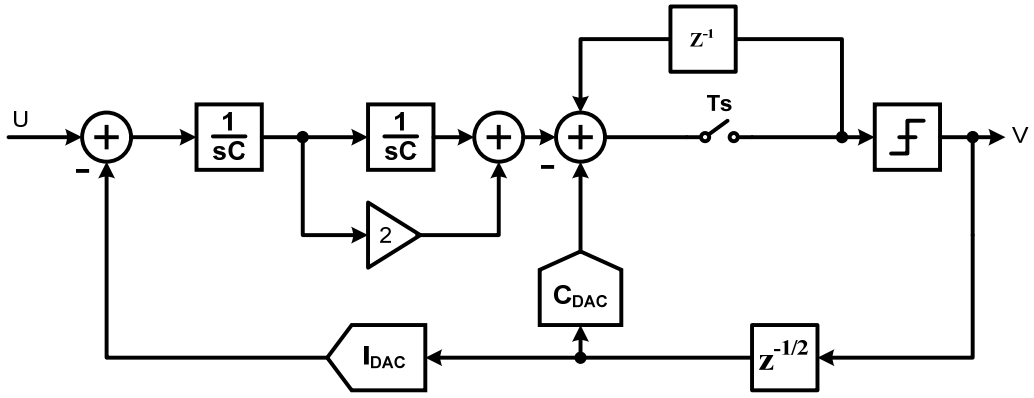

Figure 5.6: The system diagram of the 2nd order noise-coupled CT ΔΣ modulator.

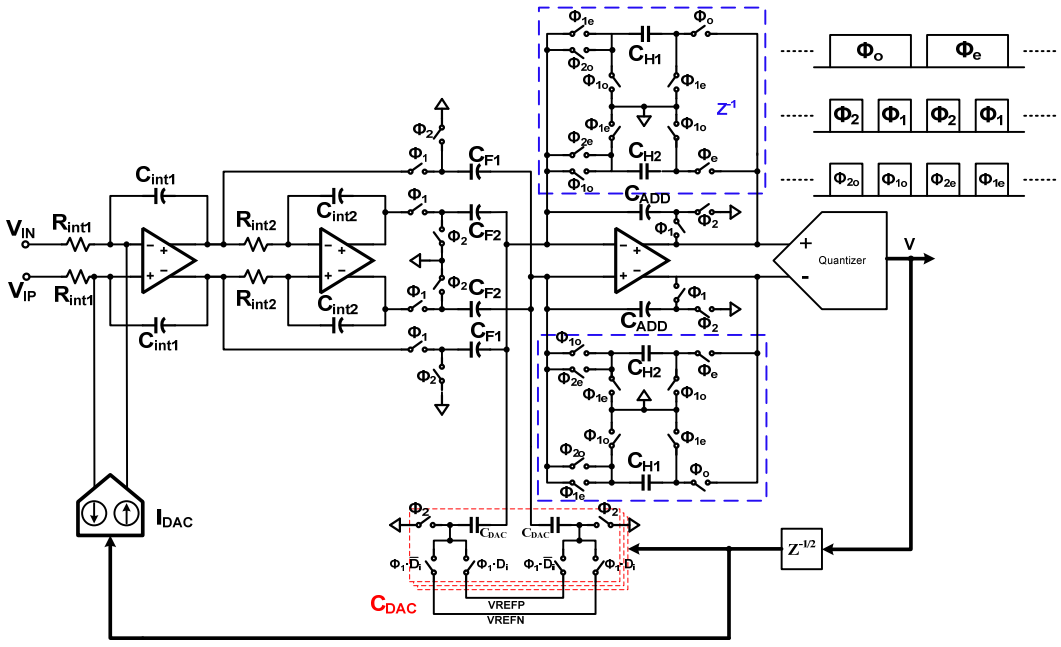

Figure 5.7: The circuit diagram of the 2nd order noise-coupled CT ΔΣ modulator.

modulator output is realized by the feedback block C_{DAC}, which is also used for the half-cycle excess-loop delay compensation. The quantization error can be extracted at the sampling instances, and the noise coupling is also realized after a one cycle delay. Fig. 5.8 shows the DT and CT loop filters impulse responses. With noise-coupling, the 2nd order CT ΔΣ modulator has the same result as a conventional 3rd order DT modulator.

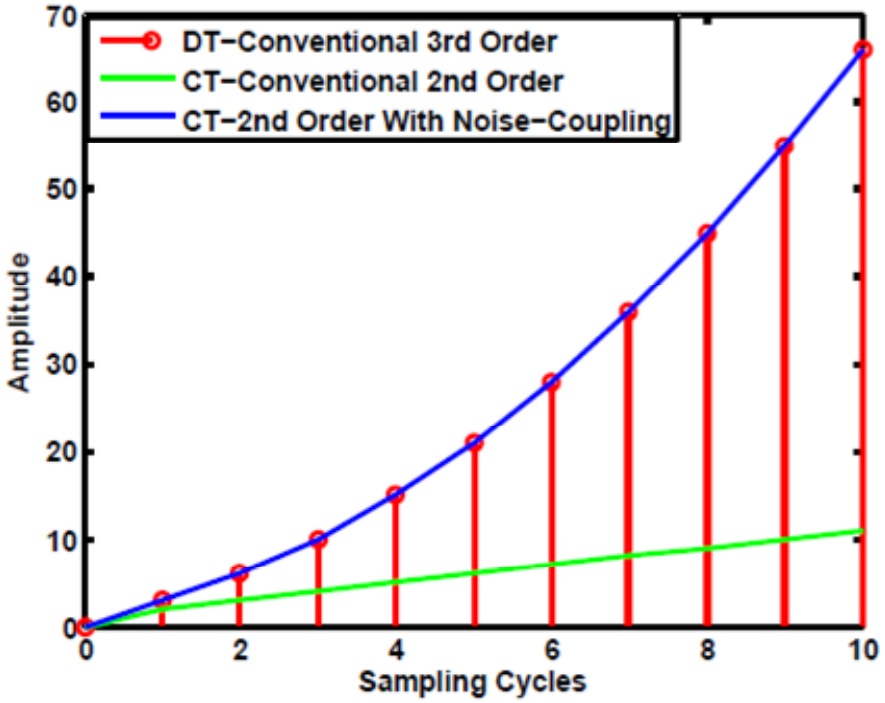

Figure 5.8: The impulse response of DT and CT loop filters.

To verify the effectiveness of the proposed design methodology, the dynamic behavior of the CT noise-coupled ΔΣ modulator circuit was simulated in Cadence Spectre simulator. The opamps were represented by macro models with finite gains (60dB). A second-order conventional CT ΔΣ modulator without noise-coupling was also designed and simulated for comparison. We assumed an NTF(z) = $(1-z^{-1})^2$ and a 20 MHz signal bandwidth, an oversampling ratio of 8, and a 4-bit quantizer. Fig. 5.9 shows the simulated output spectrum of the conventional modulator with a -2 dBFS input signal. Fig. 5.10 shows the simulated output

spectrum of the noise-coupled modulator with the same input signal. By using noise coupling, the effective noise-shaping order was raised from two to three without requiring additional integrators, and a 10-dB SQNR improvement was thus achieved. The simulated noise floor was limited by the accuracy of the simulator.

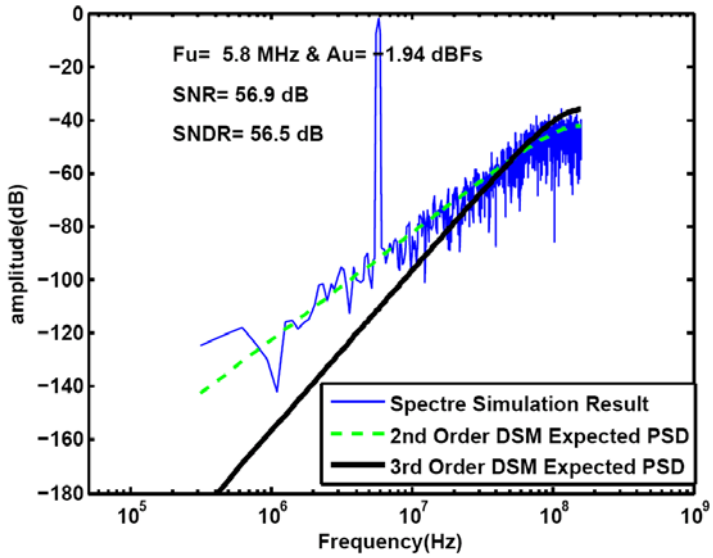

Figure 5.9: Simulated PSD of a 2nd order conventional CT ΔΣ modulator.

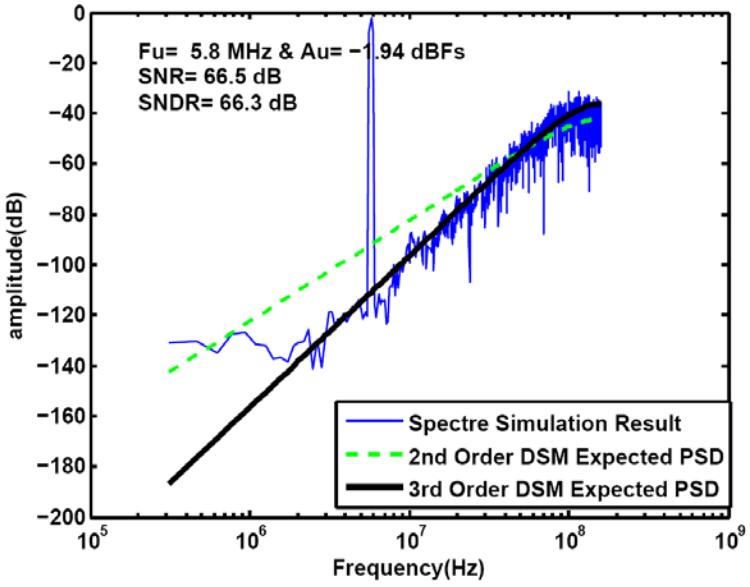

Figure 5.10: Simulated PSD of a 2nd order noise-coupled CT ΔΣ modulator.

5.4 Conclusion

A noise-coupling technique was proposed for the realization of low-power continuous-time delta-sigma ADCs. The required system and circuit design techniques were described. A second-order noise-coupled delta-sigma modulator was designed and simulated to verify the effectiveness of the scheme. While this paper discussed self-coupled CT ΔΣ ADCs, noise coupling can also be applied to other structures, such as split cross-coupled CT ΔΣ ADCs or ring-coupled CT ΔΣ ADCs.

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CHAPTER. 6 ΔΣ A/D CONVERTERS WITH SECOND-ORDER NOISE-SHAPING ENHANCEMENT [1]

The second-order noise-shaping enhancement technique is proposed and new delay cells, which can simplify the design of noise-coupling circuits, as well as of the clock generator, are discussed. To verify the proposed design methodology, a noise-coupled ADC was designed and simulated.

6.1 Introduction

Wide-band ΔΣ analog-to-digital converters with high accuracy and low power dissipation are key components of wired and wireless communication systems, consumer electronics, radar systems and medical devices. There is continuing effort focusing on novel architectures that can efficiently deal with these design requirements. Recently, the noise-coupling technique shown in Fig. 6.1 was introduced by K.Lee et al. [2] for high resolution discrete-time delta-sigma ADCs. For $C(z)=z^{-1}$,which means that the quantization noise is extracted and then coupled to the loop filter output with a one-cycle delay, first-order noise-shaping enhancement can be achieved. Compared to a conventional ΔΣ ADC with feed-forward structure, the first-order noise-coupled architecture can save one integrator and still retain the same noise-shaping ability. So the power consumption can be reduced. Combined with the low-distortion topology [3], noise coupling has been successfully applied to different ADCs [4-6], and resulted in excellent linearity and power efficiency performance.

This chapter discusses how to extend the noise-coupling technique to achieve second-order noise-shaping enhancement. A new architecture and circuit topology is proposed to reduce the complexity of the active adder and clock generator.

The chapter is organized as follows. Section 6.2 introduces the novel delay cell for noise-coupled ADCs. Section 6.3 describes the second-order noise-coupled

ADCs, its architecture and circuit implementation. Section 6.4 describes a design example and the simulation results. Section 6.5 gives the conclusions.

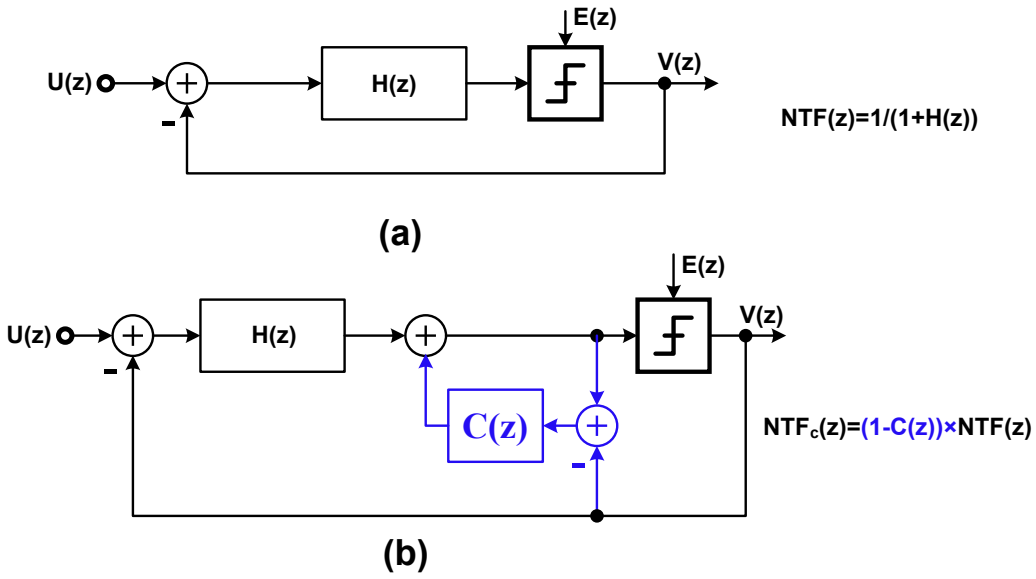

Figure 6.1: (a) Conventional ΔΣ modulator; (b) Noise-coupled ΔΣ modulator.

6.2 Delay Cell

In noise-coupled ΔΣ ADCs, the quantization noise is extracted, delayed, and added to the loop filter output. The delay cell is the fundamental block needed to achieve noise coupling. In actual circuit implementation, noise coupling can be carried out using two branches. One is the negative feedback branch from the modulator output V(z) to the adder input. The other feedback branch is from the adder output Y(z) to the adder input. Fig. 6.2 shows the block diagram of a first-order noise-coupled ADC. V(z) is the digitized modulator output, and hence the one cycle delay of the DAC feedback branch can be easily realized in the digital domain. However, the adder output signal Y(z) is analog, and the full-cycle delay from Y(z) to the adder input needs to be implemented using a switched-capacitor circuit. For a single-sampling ΔΣ modulator, let Φ_1 be the sampling/adding phase and Φ2 the holding or reset phase for the adder. Fig. 6.3. shows a switched-capacitor adder circuit with a sample-and-hold function. There are two equal-

valued capacitors $C_{H,E}$ and $C_{H,O}$ in the z^{-1} delay cell. Assuming that Φ_{1O} is high at the beginning of one clock cycle, C_{in} and $C_{H,O}$ deliver their charges to the adder input. This affects the adder output through $C_{add.}$ The adder output voltage is sampled and stored in $C_{H,E}$. Next, C_{in} and C_{add} are reset during the Φ_{2E} phase, and $C_{H,E}$ holds the output voltage. During the next clock cycle, $C_{H,E}$ will deliver the previous cycle's adder output charge to the adder, and the adder output voltage will be sampled and held by $C_{H,O}$. By alternating $C_{H,E}$ and $C_{H,O}$, the z^{-1} delay can thus be achieved.

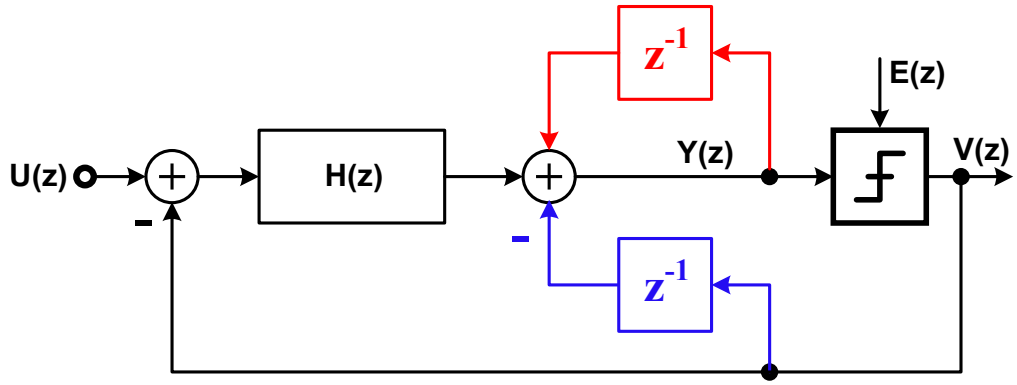

Figure 6.2: The block diagram of a first-order noise-coupled ΔΣ modulator.

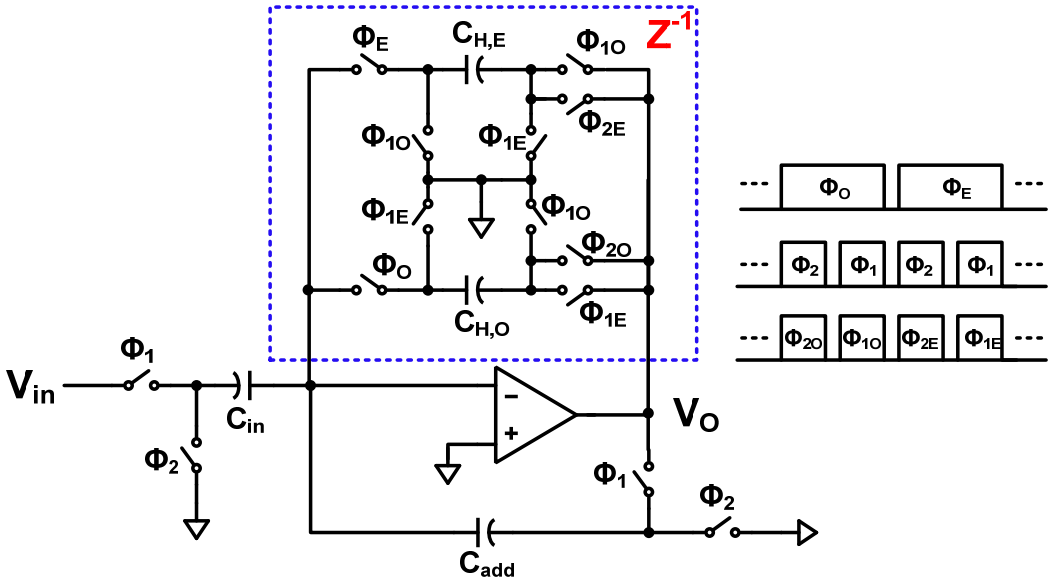

Figure 6.3: The adder circuit with the z^{-1} delay cell.

However, in order to implement the full cycle delay using the described scheme, the clock generator needs to provide six additional clock phases for the adder, and thus the complexity of clock generator is increased. To simplify the clock generator, another new scheme is proposed. The adder circuit diagram is shown in Fig. 6.4. When Φ_1 (the sampling/adding phase for the adder) rises, both C_{in} and C_H deliver charge to the adder. At the falling edge of Φ_1, the adder output voltage will be sampled and stored in C_H'. When Φ_2 is high, only C_H' is connected between the virtual ground and the adder output, and thus the adder output voltage is held. C_{in} and C_H are disconnected from the opamp, C_{in} is reset and C_H samples the output voltage at the falling edge of Φ_2. So, by repeating the charge delivering and sampling at Φ_1 and Φ_2, C_H can realize the full-cycle delay of the adder output. Since no additional clock phases are required for the z^{-1} delay cell, the clock generator circuit for the noise-coupled $\Delta\Sigma$ ADC can be as simple as for a conventional $\Delta\Sigma$ ADC. Also, C_H' can be much smaller than C_H . This can reduce the adder's output loading during the sampling phase, and thus relax the speed requirements for the opamp.

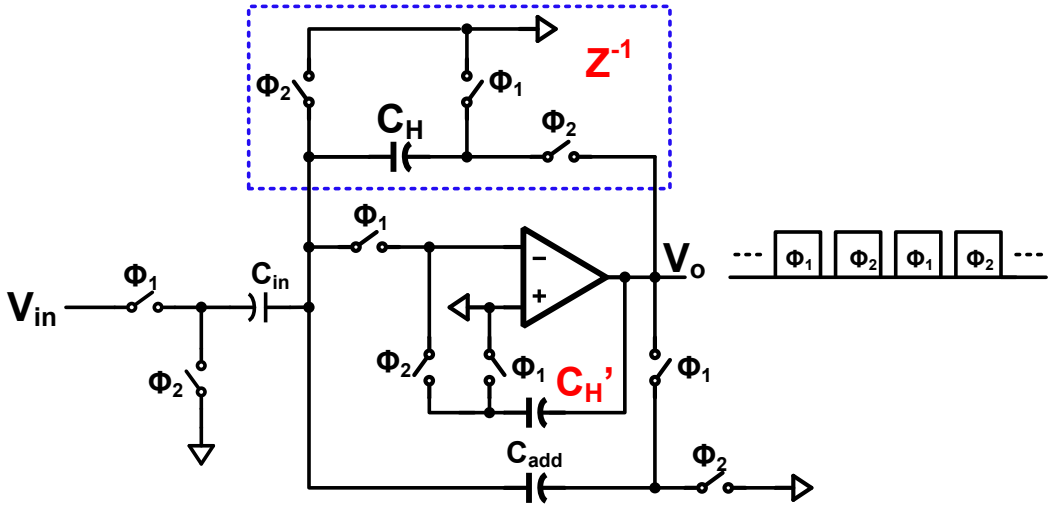

Figure 6.4: The proposed adder circuit with the novel z^{-1} delay cell.

6.3 ΔΣ ADC with Second-Order Noise-Coupling

For the first-order noise-coupled ΔΣ ADC, one integrator can be saved to obtain the same NTF(z) as conventional ΔΣ ADC. To further reduce the active components, higher-order noise-coupling technique can be used. Fig. 6.5 shows a practical structure that achieves a second-order noise-shaping enhancement. The coupling filter function is $C(z)=2z^{-1}-z^{-2}$.

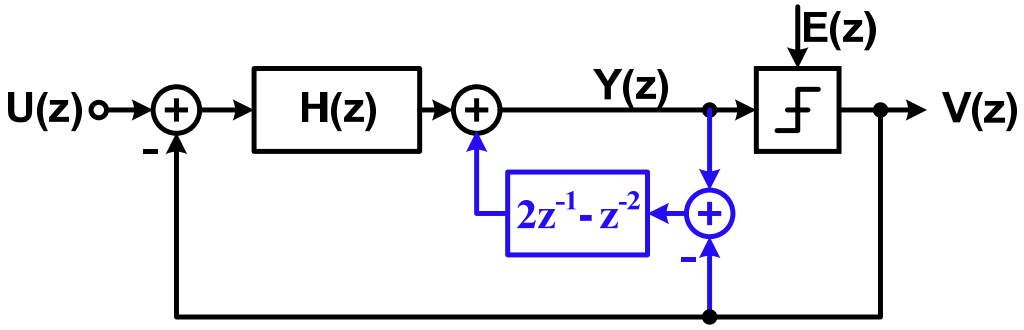

Figure 6.5: The ΔΣ modulator with 2nd order noise-shaping enhancement.

Clearly, for a second-order noise-coupled ΔΣ ADC design, both one-cycle and two-cycle delay cells are needed. The z^{-1} delay cell was described in the previous section. The design of the z^{-2} delay cell is discussed next.

One possible implementation is drawn in Fig. 6.6. Φ_1 is the sampling/adding phase for the adder and Φ_2 is the holding phase. Three identical switched-capacitor blocks are controlled by three different clock signals. The falling edge of Φ_{1i} (i=1~3) is the sampling point of the adder, so the adder output voltage is sampled in one of these three capacitors. After holding it for two cycles, the charge will be delivered to the adder input. The cyclical rotation of sampling and charge delivery implements the function z^{-2}.

Since the adder output is strobed at the adding phase when the adder is in a closed-loop feedback configuration, C_H introduces additional output loading for the adder, and hence increases the opamp's bandwidth requirements. As in the z^{-1}

delay cell, this can be remedied by sampling the adder output voltage after a half-cycle delay. The resulting adder circuit is shown as Fig. 6.7. Now only two identical switched-capacitor blocks are required. Φ_1 is still the adding phase for the adder, and Φ_2 is the holding phase during which the adder output remains unchanged. The adder output is strobed at the falling edge of Φ_2 . By properly allocating the clock phases $\Phi_{1O,E}$ and $\Phi_{2O,E}$, the z^{-2} delay is implemented.

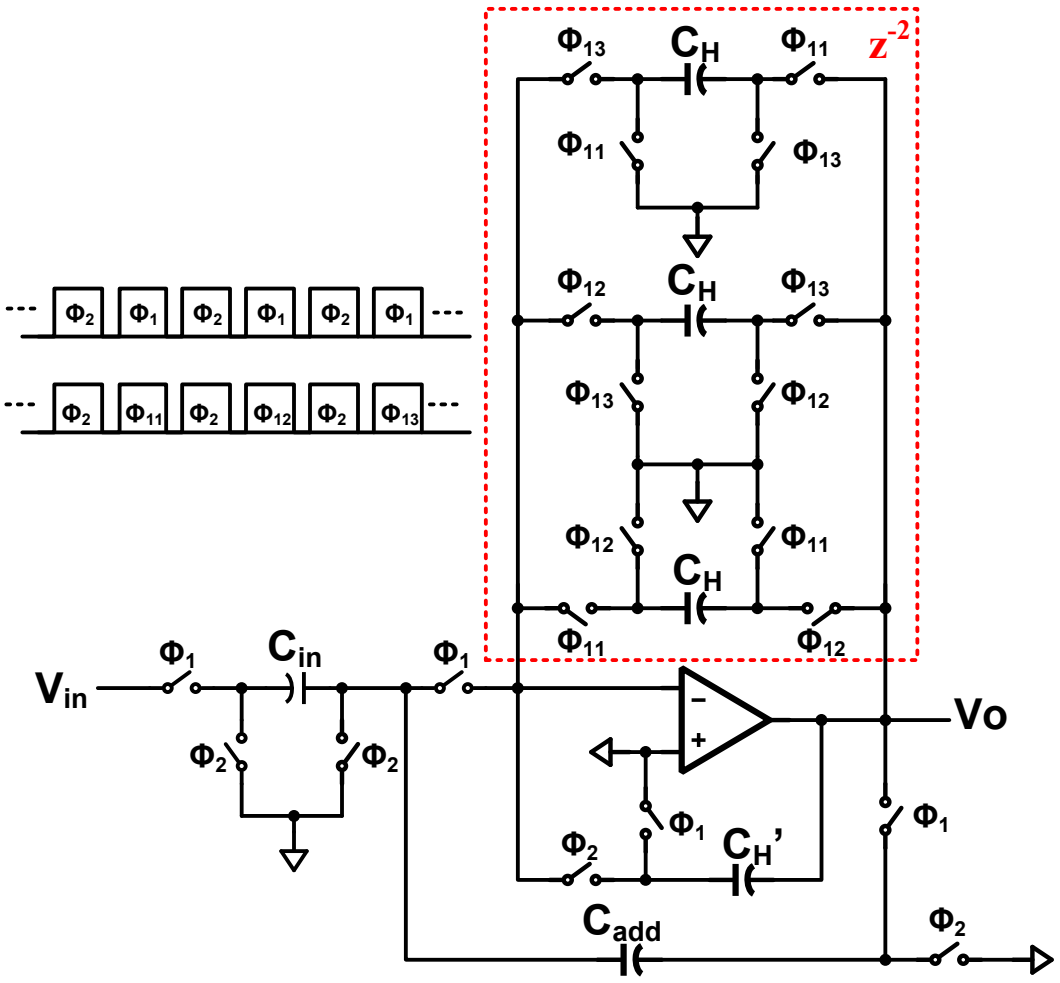

Figure 6.6: The adder circuit with a z^{-2} delay cell.

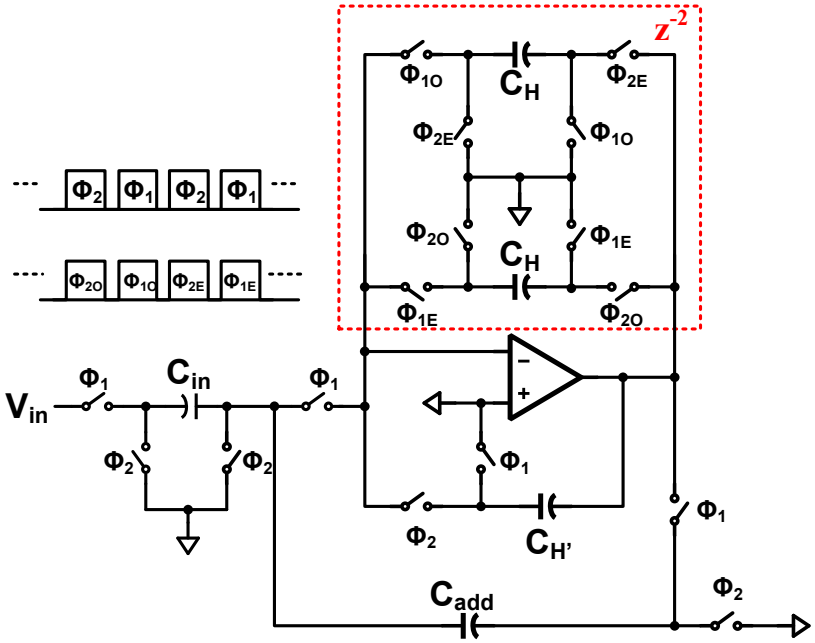

Figure 6.7: The adder circuit with the proposed z^{-2} delay cell.

6.4 Design Example

As a demonstration of proposed design technique, a second-order-coupled discrete-time delta-sigma modulator was designed. The system-level block diagram and the single-ended circuit are shown in Figs. 6.8 and 6.9. The opamps are represented by macro models with finite gains (80 dB). In the active adder, the z^{-1} and z^{-2} delay blocks are realized using the proposed schemes shown in Figs. 6.4 and 6.7.

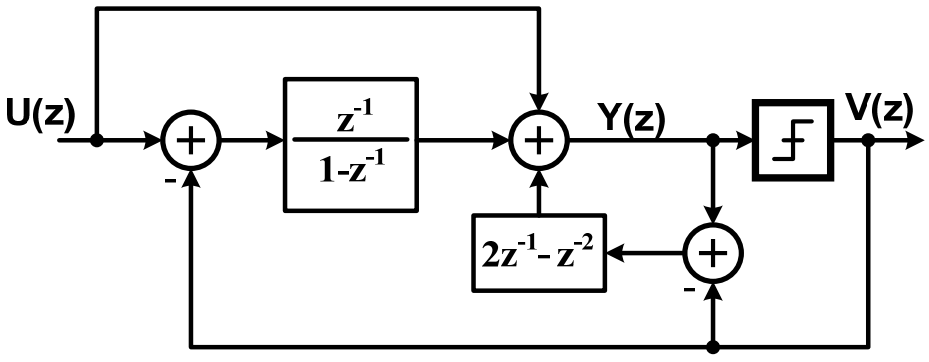

Figure 6.8: The system diagram of proposed self-coupled ΔΣ ADC.

To verify the effectiveness of noise-shaping enhancement, the dynamic behavior of the self-coupled ΔΣ modulator circuit was simulated in Cadence Spectre simulator. A first-order conventional discrete-time delta-sigma modulator was also designed and simulated for comparison. We assume NTF (z) =1-z^{-1} and a 20 MHz signal bandwidth, an oversampling ratio of 8, and 4-bit quantizers. Fig. 6.10 shows the simulated output spectrum of the conventional modulator with a -2 dBFs input signal. Fig. 6.11 shows the simulated output spectrum of the noise-coupled modulator with the same input signal. By using the second-order coupling technique, the effective order of the noise shaping was raised from one to three without additional integrators, and a 20 dB SQNR improvement was achieved. The simulated noise floor in Fig. 6.11 is limited by the accuracy of the simulator.

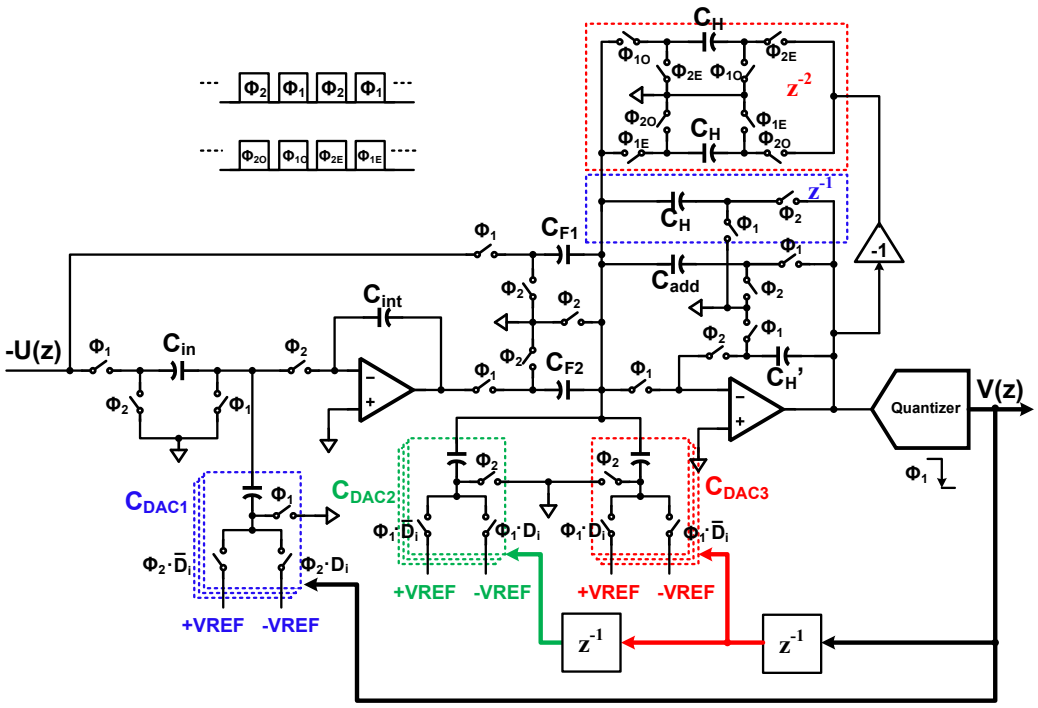

Figure 6.9: The single-ended circuit diagram of the proposed noise-coupled ΔΣ ADC.

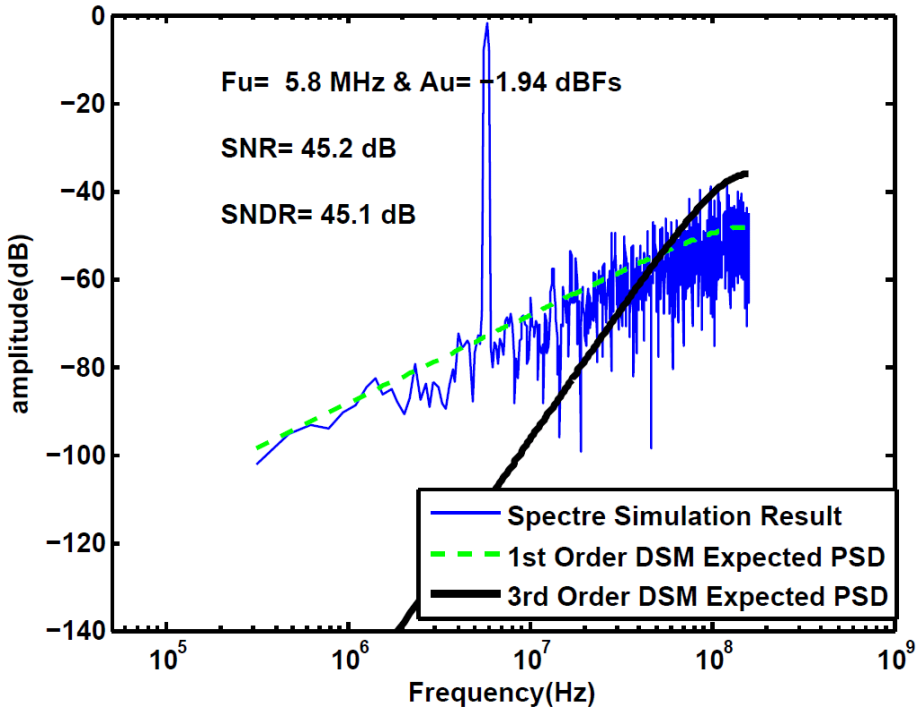

Figure 6.10: Simulated output PSD of the conventional ΔΣ ADC.

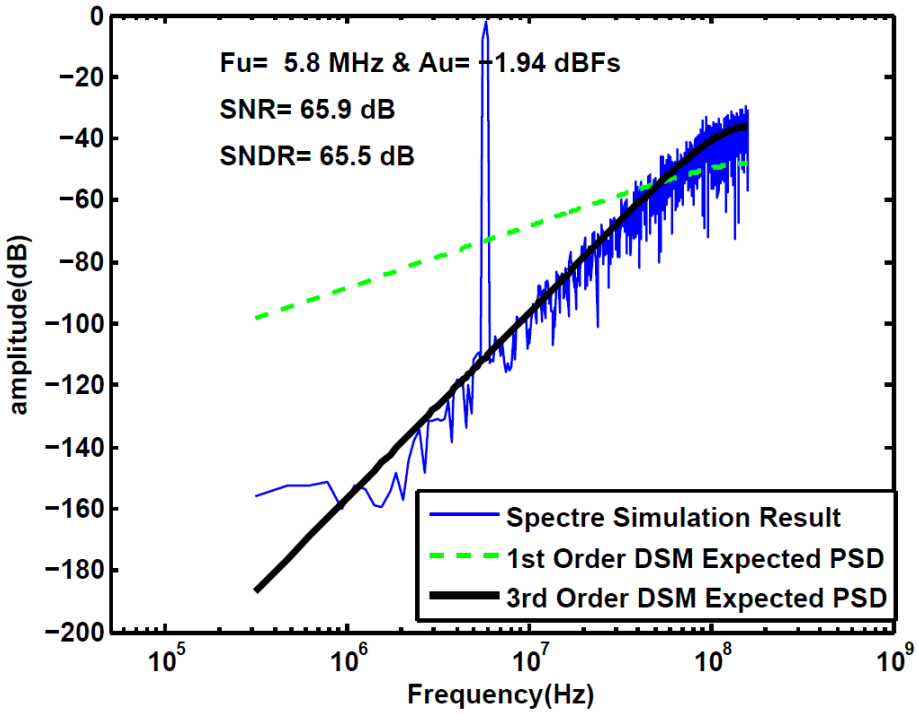

Figure 6.11: Simulated PSD of the noise-coupled ΔΣ ADC.

6.5 Conclusions

A second-order noise-coupling technique was proposed for the design of low-power delta-sigma ADCs. The required system and its key circuit blocks were described. A first-order discrete-time self-coupled delta-sigma modulator was designed and simulated to verify the effectiveness of the proposed scheme. While this paper discussed the design of discrete-time self-coupled ΔΣ ADCs, the described techniques also can be applied to other structures, such as split cross-coupled ΔΣ ADCs or ring-coupled ΔΣ ADCs.

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[6] Y. Wang, K. Lee and G. C. Temes, "A 2.5MHz BW and 78dB SNDR Delta Sigma Modulator Using Dynamically Biased Amplifiers," *Proc. IEEE Custom Integrated Circuits Conf.*(*CICC*), pp 97-100, Sep. 2008.

CAHPTER. 7 DIRECT-CHARGE-TRANSFER ADDER FOR WIDEBAND LOW-POWER ΔΣ A/D CONVERTERS [1][2]

A direct-charge-transfer (DCT) adder is proposed to reduce the active adder's speed requirements for wideband low-power ΔΣ ADCs. Its operation principle and design are discussed in detail. Its application to noise-coupled delta-sigma ADCs and double-sampling are also described. To verify the proposed design methodology, a 2^{nd} order noise-coupled ΔΣ ADC and a double-sampling ΔΣ ADC, using DCT adder technique, have been designed and simulated.

7.1 Introduction

High-accuracy wide-band ΔΣ analog-to-digital converters with low power dissipation are key components used in wired and wireless communication systems, consumer electronics, radar systems and medical applications. Feed-forward architectures with low-distortion technique [3] are extensively used for wideband high performance ΔΣ ADCs. In these circuits, the loop filters just need to process the noise, so the linearity requirements for the loop filter are greatly reduced. On the other hand, the feed-forward architecture requires a fast adder to sum all branches input signals before the quantizer (Fig.7.1). If an active adder is used for accurate summation, the input branches will reduce the opamp's feedback factor. For a high-order ΔΣ ADC design, the feedback factor becomes very small, and an ultra-wideband opamp has to be designed. The situation is even worse in noise-coupled structures [4-7] because of the additional branches. A passive adder can also be used. It may be very fast, but it suffers from the high sensitivity to the parasitic capacitances of quantizer and the adder itself, and it is also not realizable for noise-coupled ΔΣ ADCs without an additional gain stage.

This chapter proposes a new active adder using a direct-charge-transfer (DCT) technique. It can achieve accurate summation with greatly relaxed opamp bandwidth requirement. It is also insensitive to parasitic capacitance and can be

conveniently combined with noise-coupling technique, which can further increase the ADC's noise-shaping ability.

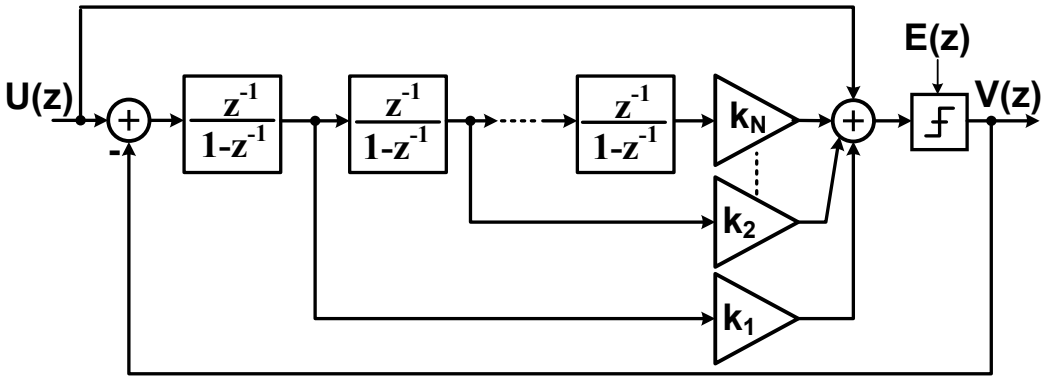

Figure 7.1: The block diagram of a general feed-forward ΔΣ ADC.

The chapter is organized as follows. In section 7.2, the proposed DCT adder for a feed-forward ΔΣ ADCs is introduced. Section 7.3 describes how to apply DCT adder in noise-coupled ADCs. Section 7.4 proposes a hybrid DCT adder scheme to optimize the design tradeoffs between the adder speed requirement and the comparator sensitivity. In section 7.5, design constraints of DCT adder for double-sampling ΔΣ ADCs are addressed, the corresponding solution is then proposed. After that, two design examples are presented in section 7.6 to verify proposed techniques. Section 7.7 summarizes the conclusions.

7.2 DCT Adder Operation Principle

The circuit diagrams of a conventional sample-and-hold adder and the proposed adder using a DCT scheme are shown in Figs. 7.2.a and b. In the conventional adder, C_1-C_N are the capacitors of the input branches, and C_{ADD} is the output capacitor which is used to set the gain of the adder. C_H holds the output during the reset phase Φ_2.When Φ_1 is high, the input capacitors and C_{ADD} are in a closed-loop

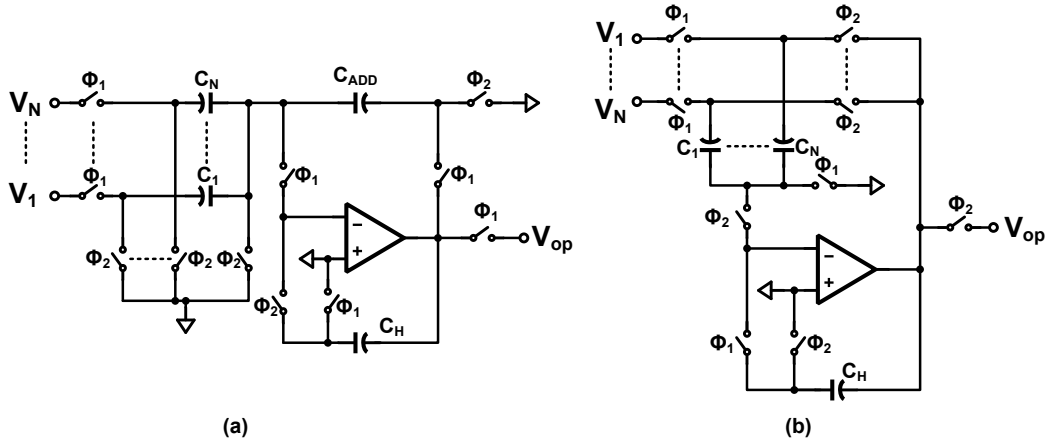

Figure 7.2: (a) Conventional S/H adder circuit. (b) S/H adder using DCT.

configuration, and the output voltage is

$$V_{OP}[n] = \sum_{i=1}^{N} k_i \times V_i[n] \tag{7.1}$$

Here

$$k_i = -\frac{C_i}{C_{ADD}} \tag{7.2}$$

To simplify the discussion, we assume that the opamp input parasitic capacitance is negligible. Then the closed-loop feedback factor during Φ_1 is

$$\beta = \frac{1}{\sum_{i=1}^{N} k_i} \tag{7.3}$$

C_H samples the adder output voltage at the falling edge of Φ_1, and then holds the adder output during Φ_2, while the other capacitances are reset.

For the adder using DCT scheme, C_{ADD} is unnecessary. C_1-C_N sample the input signals during the Φ_1 phase. During the Φ_2 phase, all charges stored in these capacitors will be shared, and the adder output will be updated to a new value. C_H samples the adder output at the falling edge of Φ_2, and then holds it for a half cycle during the next Φ_1 phase. The adder output voltage is given by

$$V_{OP}[n] = \sum_{j=1}^{N} k_j \times V_j[n - \frac{1}{2}] \tag{7.4}$$

Here,
$$k_j = \frac{C_j}{\sum_{i=1}^{N} C_i} \tag{7.5}$$

Since all capacitors (except C_H) are connected between the virtual ground and the adder output, the feedback factor in the ideal case is

$$\beta_{dct} = 1 \tag{7.6}$$

The DCT adder's output voltage, as is shown in Eq. 7.4, is very similar to that of a passive adder, except for a half-cycle delay. This half-cycle delay can be easily absorbed in the loop by choosing proper clock timing for the loop filter, and is hence not a problem for a single-sampling ΔΣ ADC. The adder output is attenuated by the stage, which can be compensated by scaling down the reference voltage of the quantizer.

Besides the opamp unit-gain bandwidth requirement, the slew-rate requirement of these two kinds of adders can also be checked. Fig. 7.3.a and b shows the adders in close-loop configuration with output loading C_L and opamp input parasitic capacitance C_p. When opamp enters the slew-rate limit situation, the slew-rate is related to output current I and output loading C_L.

$$SR = \frac{dV}{dt} = \frac{I}{C_L} \tag{7.7}$$

For a conventional active adder, the equivalent total output loading is

$$C_{L,con} = C_L + C_{ADD} // (C_p + \sum_{i=1}^{N} C_i) \tag{7.8}$$

While, for a DCT adder, the equivalent output loading is

$$C_{L,DCT} = C_L + C_p // \sum_{i=1}^{N} C_i \tag{7.9}$$

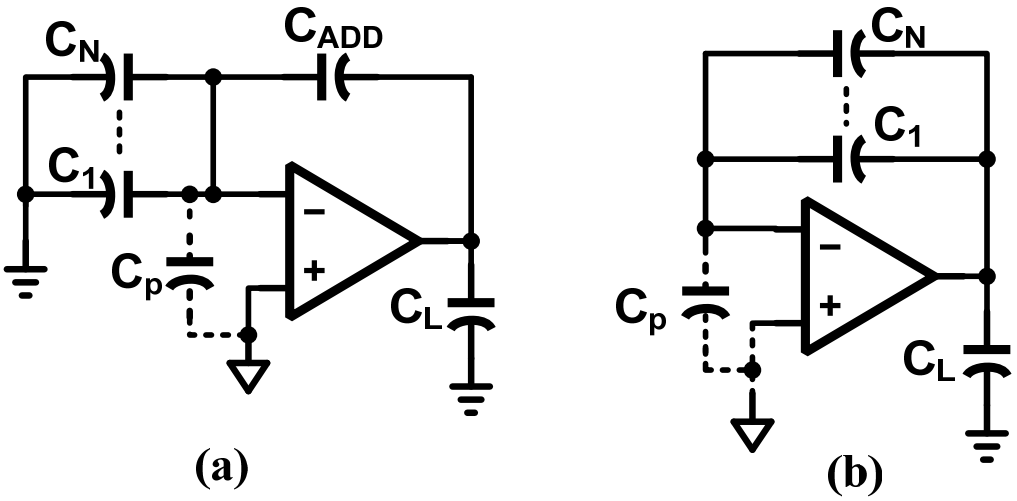

Figure 7.3: The close-loop configuration of (a) conventional adder (b) DCT adder.

From Eq. 7.8 and Eq. 7.9, it is easy to conclude that DCT adder has higher slew rate than conventional structures if the output current I , loading capacitor C_L and parasitic capacitor Cp are all the same. And the slew-rate requirement of DCT adder is even lower when the output voltage attenuation is considered.

In conclusion, the adder using the DCT scheme is insensitive to the parasitic capacitances and kickback effects, which usually cause problems in a passive adder. Furthermore, the opamp has lower slew-rate requirement and large feedback factor, which is always close to 1, and hence the stage can be much faster than a conventional active adder. So, it is suitable for wideband low-power ΔΣ ADC realization.

7.3 DCT Adder for Noise-Coupled ΔΣ ADC

For a noise-coupled ΔΣ ADC with first-order noise-shaping enhancement, the behavioral model of the proposed DCT adder is shown in Fig. 7.4. Here, k_1-k_N represent the scaled values of the input capacitors, k_Y the coupling capacitor from the adder output to its input, k_C is the pre-set gain for the adder output coupling branch during the sampling phase, and k_{dac} is the coupling capacitor from the modulator output. Also, k_s is the attenuation factor due to the DCT topology.

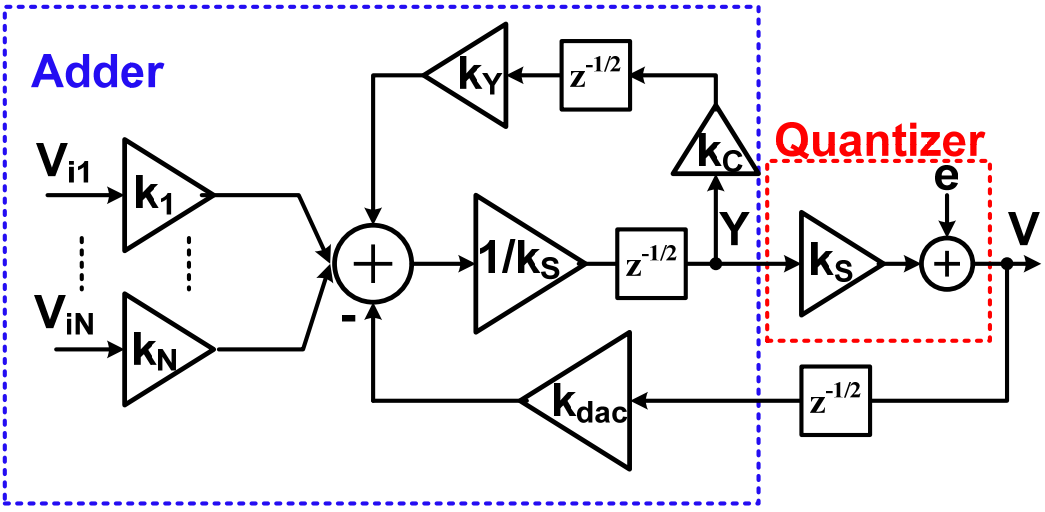

Figure 7.4: DCT adder behavioral model for a noise-coupled ΔΣ ADC.

$$k_S = k_Y + k_{dac} + \sum_{i=1}^{N} k_i \tag{7.10}$$

To achieve first-order noise-coupling, the condition

$$k_Y \times k_C = k_S \tag{7.11}$$

must hold. So, the capacitor k_Y must satisfy

$$k_Y = \frac{k_{dac} + \sum_{i=1}^{N} k_i}{k_C - 1} \tag{7.12}$$

Eq. 7.12 also indicates a limitation for realizability

$$k_C > 1 \tag{7.13}$$

In our design, k_C is set to 2, because, as is shown below, this requires no additional active components in a fully-differential structure. Hence

$$k_Y = k_{dac} + \sum_{i=1}^{N} k_i \tag{7.14}$$

Fig. 7.5 shows the single-ended circuit diagram for the proposed DCT adder. During the Φ_1 phase, C_Y is charged by the difference between V_{OP} and V_{ON}, so an

effective gain of 2 is achieved. When Φ_2 is high, C_Y is connected between virtual ground and V_{OP}, and the charge will be redistributed.

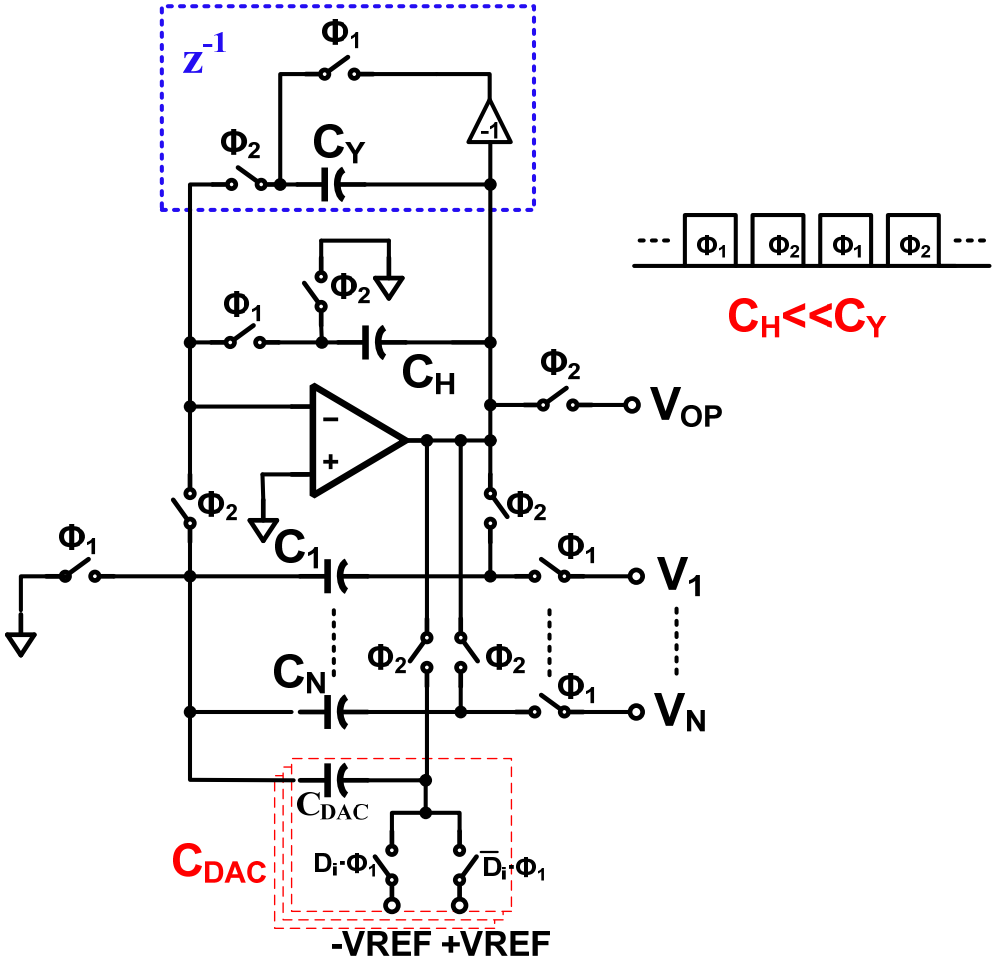

Figure 7.5: DCT adder circuit diagram for a noise-coupled ADC.

7.4 Hybrid DCT Adder

As discussed in section 7.2, the output attenuation of the DCT adder can be compensated by scaling down the reference voltage of the quantizer. This downscaling also reduces the step size of comparators' threshold voltages, and increases their required sensitivity. It is not a big issue for low order ΔΣ ADC using low-resolution quantizer. However, for a high-order ΔΣ ADC, k_S can become large with many input branches, which could make the comparator design

very challenging, and it becomes ever worse for noise-coupled structure and low-voltage system. By using a hybrid scheme for the adder, with some branches using the conventional charge transfer scheme and other branches using the DCT scheme, an optimum trade-off can be found between the opamp bandwidth and comparator sensitivity. An example is shown in Fig. 7.6. The circuit parameters are given by

$$k_S = 2\left(k_{dac} + \sum_{i=1}^{M} k_i \right) \tag{7.15}$$

$$\beta_{hybrid} = \frac{k_S}{2}\left(k_{dac} + \sum_{i=1}^{M} k_i + 0.5 \times \sum_{j=M+1}^{N} k_j \right) \tag{7.16}$$

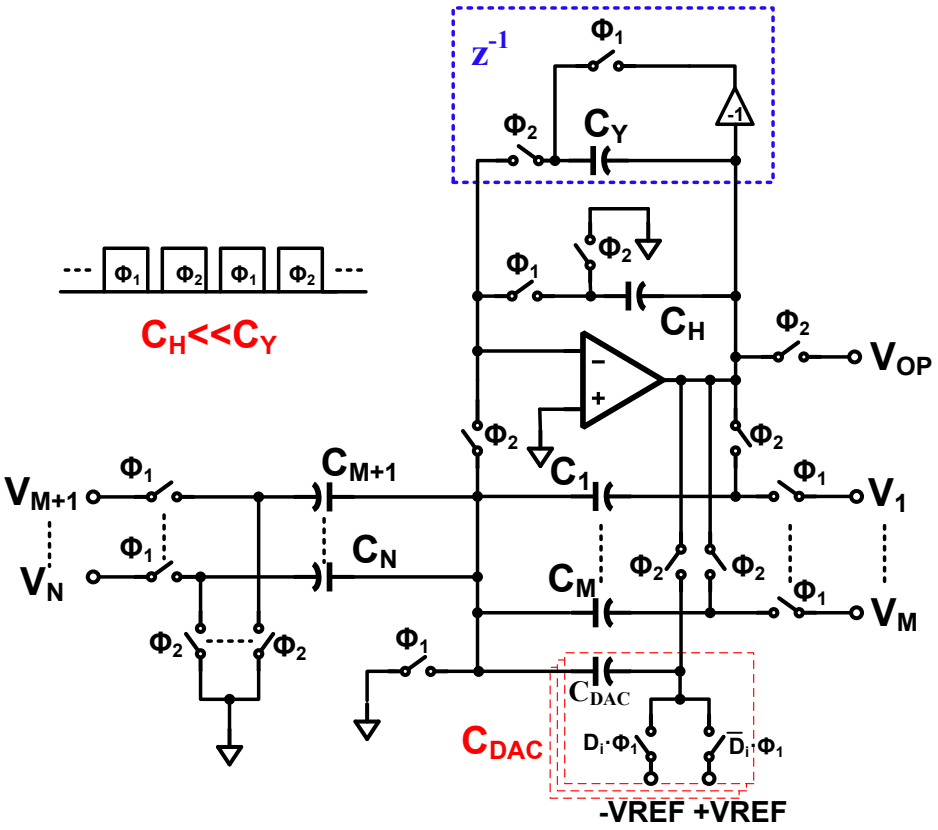

Figure 7.6: Hybrid adder circuit diagram.

7.5 DCT Adder for Double-Sampling ΔΣ ADCs

To increase the signal bandwidth of ΔΣ ADC, double sampling [8-10] may be used. By alternating between two sets of identical switched-capacitor circuits, the loop filter can do both the sampling and integration in each clock phase, and thus the effective sampling rate is doubled. Hence, the signal bandwidth can be doubled, or the clock frequency can be half as high as in a single-sampling ΔΣ ADC. Applying the DCT adder in the double-sampling ΔΣ ADC can further relax the speed requirement of the adder, which is usually the critical block for wideband applications. So, higher bandwidth and lower power requirements can be expected by applying both double sampling and DCT adder.

7.5.1 Stability Issues

In a double-sampling ΔΣ ADC, both sampling and integration are executed during each clock phase, and so is the summation in the adder. Thus a one-cycle delay will be generated by the DCT adder. This delay will increase the order of loop filter by one and then the modulator becomes unstable. Taking a conventional 2^{nd} order double-sampling ΔΣ modulator as an example, Fig. 7.7 shows the behavior model if a DCT adder is used. The loop filter transfer function is

$$H'(z) = -\frac{2 - z^{-1}}{(z-1)^2} \tag{7.17}$$

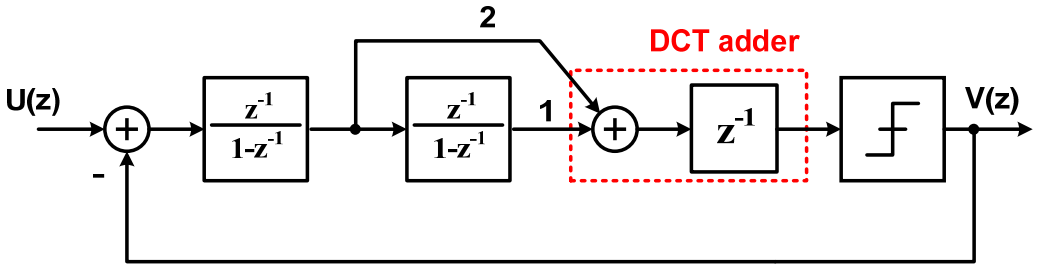

Figure 7.7: The behavior model of a double-sampling ΔΣ ADC with DCT adder.

The corresponding closed-loop noise transfer function is

$$NTF(z) = \frac{z(z-1)^2}{z^3 - 2z^2 + 3z - 1} \tag{7.18}$$

So the modulator becomes a third-order system when a DCT adder is used. Fig. 7.8 shows the NTF (z) pole/zero locations. Two of the three poles of NTF (z) are located outside the unit circle. The modulator is hence unstable.

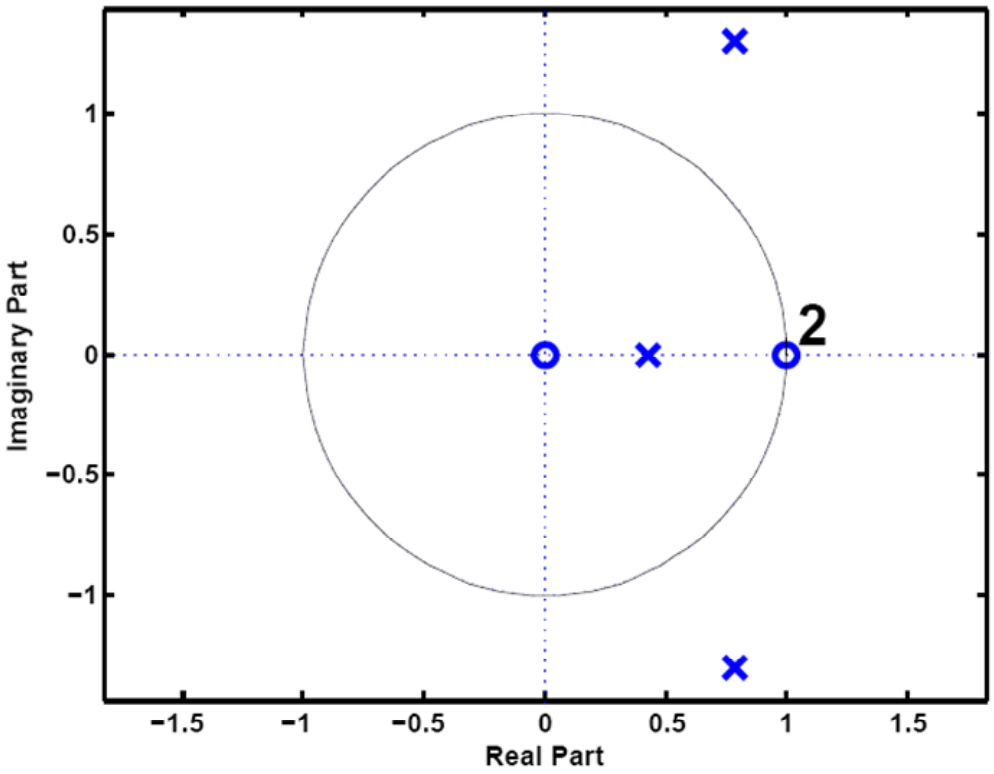

Figure 7.8: Pole/zero locations of a 2nd order double-sampled ΔΣ ADC using a DCT adder.

7.5.2 Feedback Loop Stabilization

Since the order of the loop filter increased to three due to the extra delay, tuning the coefficients of the two independent branches cannot easily stabilize the system.

Another independent branch should be added to fully control the whole modulator. By proper design of the new loop filter, its impulse response can be matched to that of the original loop filter. The concept is quite similar to the excess loop delay compensation [11] in continuous-time ΔΣ ADC design using the impulse-invariant- transformation [12]. It is easy to show that the proposed DCT scheme is also realizable for noise-coupled double-sampling ΔΣ ADCs.

Figs. 7.9.a and b shows the corresponding block diagrams of the general double-sampling ΔΣ ADC using conventional active adder or DCT adder. The $I(z)$ is the delayed integrator transfer function

$$I(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{7.19}$$

To achieve the same loop transfer function, Figs. 7.9.a and b should satisfy

$$\sum_{i=1}^{N-1} a_i I(z)^i + I(z)^N = z^{-1}\left[k_c + \sum_{j=1}^{N-1} b_j I(z)^j + b_N I(z)^N \right] \tag{7.20}$$

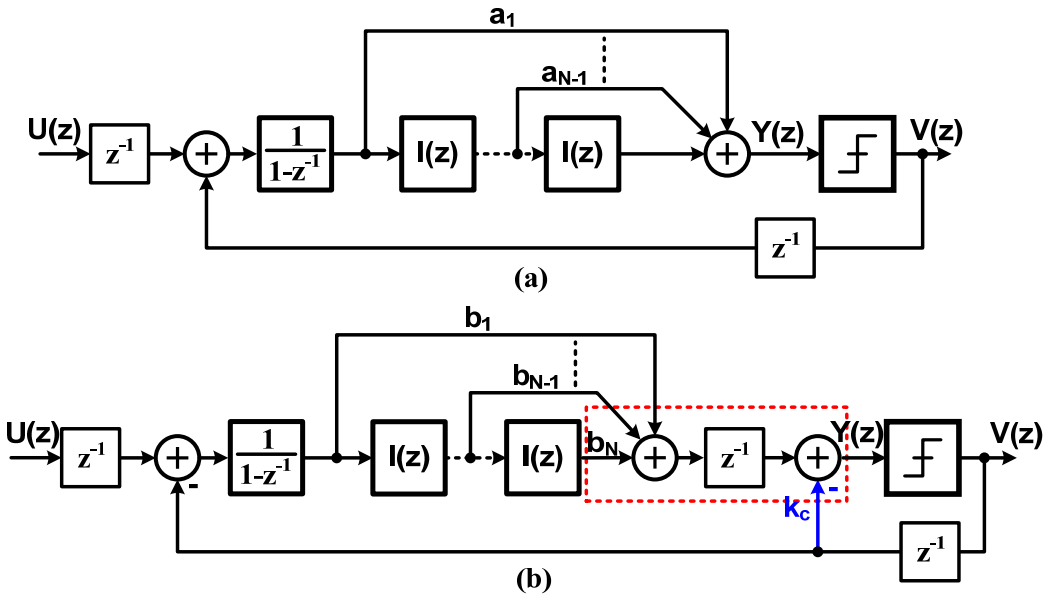

Figure 7.9: The double-sampling ΔΣ ADC with (a) conventional active adder (b)DCT adder.

From Eq. 7.19

$$z^{-1} = \frac{I(z)}{1+I(z)} \tag{7.21}$$

And Eq. 7.20 can be re-arranged as

$$\left(I(z)+1\right)\left[\sum_{i=1}^{N-1} a_i I(z)^i + I(z)^N\right] = I(z)\left[k_c + \sum_{j=1}^{N-1} b_j I(z)^j + b_N I(z)^N\right] \tag{7.22}$$

So, for double-sampling ΔΣ ADCs using conventional adder and DCT adder, same noise shaping ability can be achieved if Eq. 7.22 is satisfied. It means

$$k_c = a_1 \tag{7.23}$$

$$b_i = a_i + a_{i+1} \qquad (i < N) \tag{7.24}$$

$$b_N = 1 \tag{7.25}$$

7.5.3 Low-Distortion Technique

The low-distortion structure is widely used in high performance ΔΣ ADCs. For a conventional feed-forward structure, it achieves a unity signal transfer function STF(z)=1 by adding a direct input path to the quantizer. Then at the loop filter's input the signal component is cancelled. Thus the loop filter processes only quantization noise, and good linearity performance can be achieved. For the double-sampling ΔΣ ADC depicted in Fig. 7.9(b), the STF(z) is

$$STF(z) = \frac{z^{-1}\sum_{i=1}^{N} b_N I(z)^N}{1+z^{-1}\left[k_c + \sum_{i=1}^{N} b_N I(z)^N\right]} \tag{7.26}$$

To achieve STF(z)=1, an additional FIR filter $F(z)$ should be added at the feed-forward path.

$$F(z)=1+k_c z^{-1} \tag{7.27}$$

So, there are two coupling branches in $F(z)$, one needs to be delay-free and the other has fully-cycle delay. The generalized block diagram is shown in Fig. 7.10.

The adder shown in Fig. 7.10 contains both delay-free and full-cycle delay branches. In addition to the direct input path that needs a delay-free branch, the additional feedback path must also be delay-free due to the quantizer's inherent one-cycle delay in a double-sampling ΔΣ ADC. So, the overall adder should have a hybrid topology: for delay-free branches, conventional charge transfer must be used, while for all other branches, the DCT scheme can be applied.

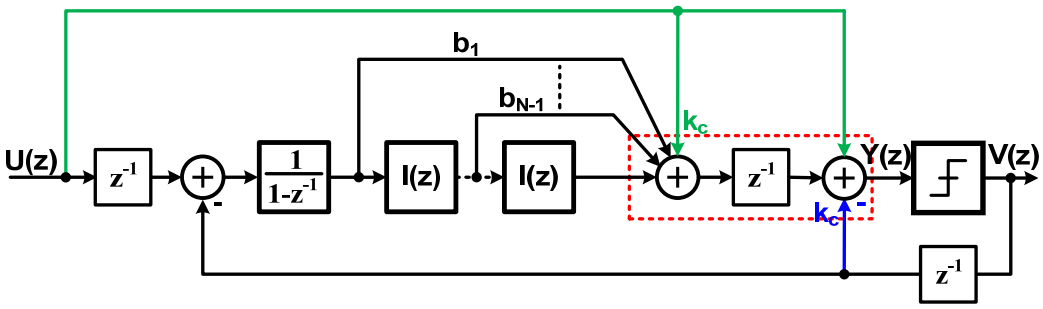

Figure 7.10: The low-distortion structure for a double-sampling ΔΣ ADC with DCT adder.

7.6 Design Examples

To verify the proposed techniques, two DT ΔΣ ADCs using DCT adder have been designed. One is a single-sampling noise-coupled ΔΣ ADC with full-DCT adder technique. The other one is a double-sampling ΔΣ ADC using hybrid-DCT adder technique.

7.6.1 Noise-Coupled ΔΣ ADC with Full-DCT Adder

The system-level block diagram of proposed noise-coupled ADC is shown in Fig. 7.11. A low-distortion structure was chosen to relax the loop filter's linearity

requirements. Since the DCT adder needs a half-cycle delay to generate the output, a half-cycle delay was also introduced in the signal input path of the first integrator. The quantization error is extracted and coupled to the loop filter output, and the effective noise-shaping order is thus raised from two to three. Using the proposed full DCT scheme, the adder output voltage is reduced by a factor of 0.1, so the reference voltages of quantizer, VREF and –VREF, were also scaled down by the same factor. The single-ended circuit block diagram is shown in Fig. 7.12.

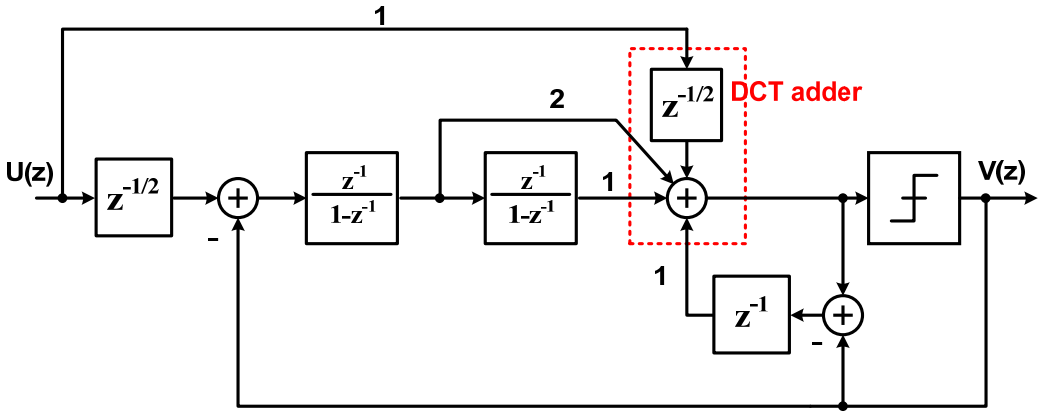

Figure 7.11: The system-level block diagram of the proposed ΔΣ ADC.

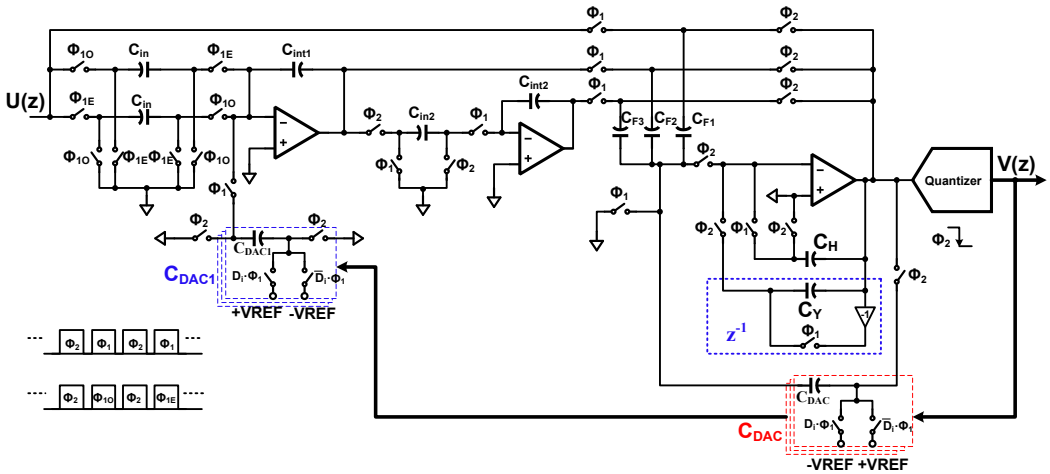

Figure 7.12: The single-ended circuit diagram of the proposed second-order noise-coupled ΔΣ modulator with a DCT adder.

To verify the effectiveness of the DCT adder, the dynamic behavior of the designed ΔΣ modulator was simulated in the Cadence Spectre simulator. The opamps were represented by macro models with finite gains (60 dB). To simplify the discussion, all capacitors in the DCT adder were normalized to the direct feed-in branch capacitor C_1. The parasitic capacitors at the opamp's virtual ground were also included and scaled to C_1 for a more realistic simulation. We assumed a noise transfer function $NTF(z)=(1-z^{-1})^2$ and a 20 MHz signal bandwidth, an oversampling ratio of 8, and a 4-bit quantizer. Fig. 7.13 shows the simulated PSD for the complete modulator verifying the third-order noise shaping expected from noise coupling.

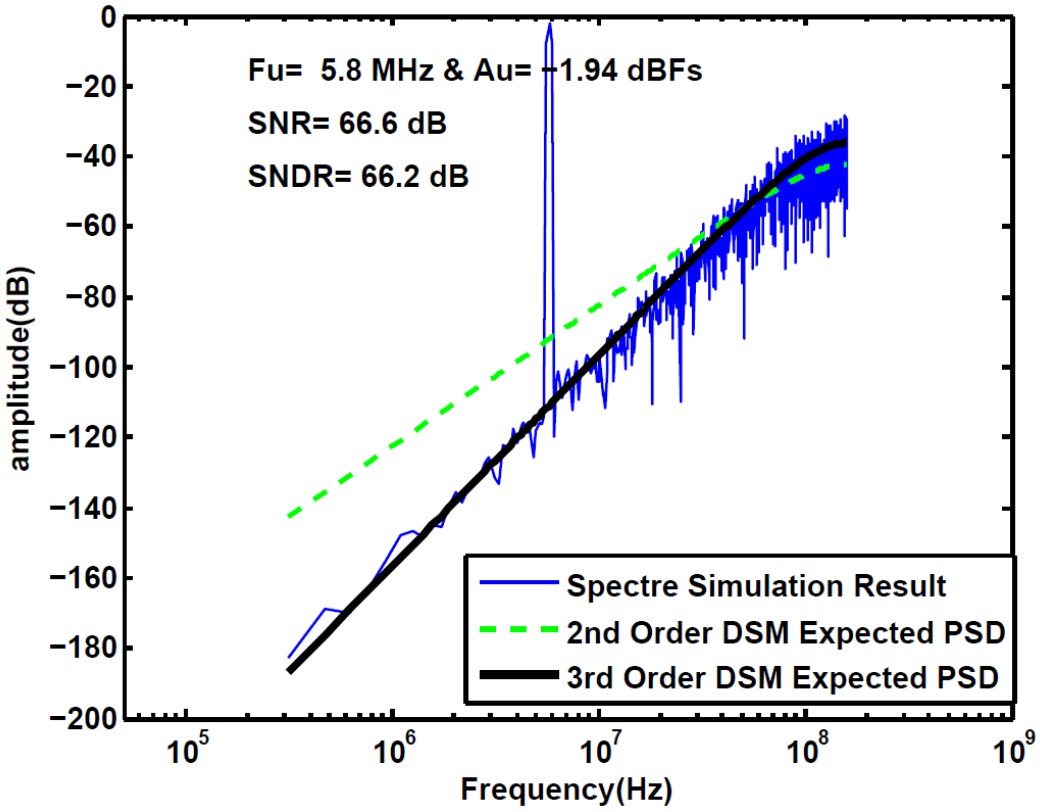

Figure 7.13: Simulated output spectrum of the proposed ΔΣ ADC with DCT adder.

To check the opamp speed requirements for the DCT adder, a left-half-plane (LHP) pole was introduced in the opamp to model its finite unity-gain bandwidth (UGBW). A second-order noise-coupled discrete-time delta-sigma modulator using a conventional adder was again designed and simulated for a comparison of the conventional and DCT adders. Fig. 7.14 shows the SNDR simulation results with these two kinds of adders, as the opamp's unity-gain bandwidth was varied from 200 MHz to 10 GHz. With a 320 MHz sampling clock, the opamp UGBW using conventional adder needed to be higher than 1 GHz for stable operation of the modulator, while the modulator using DCT remains stable even for a opamp UGBW as low as 300 MHz. Clearly, the opamp's speed requirement for the adder is greatly relaxed and its power dissipation reduced if the DCT circuit is used.

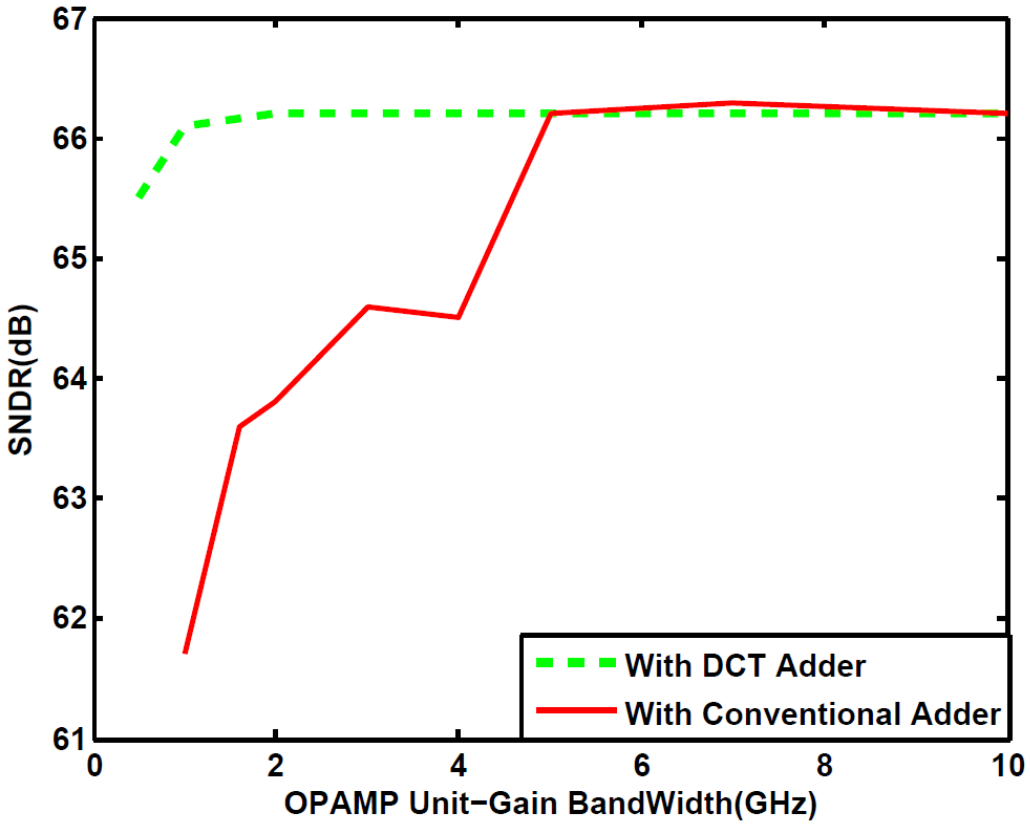

Figure 7.14: SNDR variation with opamp bandwidth.

7.6.2 Double-Sampling ΔΣ ADC Using DCT Adder

Fig. 7.15 shows the system-level block diagram of the proposed second-order double-sampling ΔΣ modulator using a DCT adder. Again, the low-distortion structure was used to relax the loop filter's linearity requirement. Using the hybrid DCT adder, the adder output is reduced by a factor 1/6, and hence the reference voltage was also scaled down by the same factor. The half-circuit diagram of the adder is shown in Fig. 7.16. Ideally, the opamp's closed-loop feedback factor is 2/3, so the adder speed requirements can be greatly reduced.

The dynamic behavior of the designed ΔΣ modulator was simulated in the Cadence Spectre simulator. The opamps were represented by macro models with finite DC gains (60dB). We assumed NTF(z) = $(1-z^{-1})^2$ and a 20 MHz signal bandwidth, an oversampling ratio of 8, and a 4-bit quantizer. The simulated PSD for the complete modulator is shown in Fig. 7.17. The absence of the input signal at the integrators' output is verified in Fig. 7.18, proving that low-distortion operation was achieved.

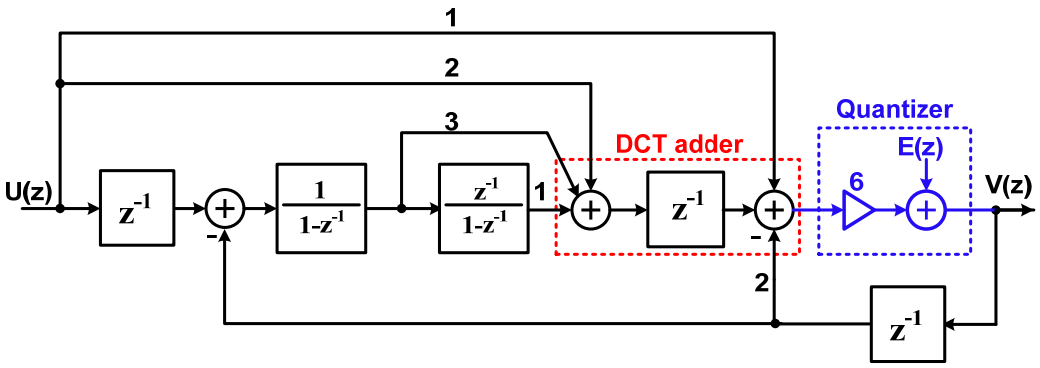

Figure 7.15: Block diagram of a 2nd order low-distortion double-sampling ΔΣ modulator using a DCT adder.

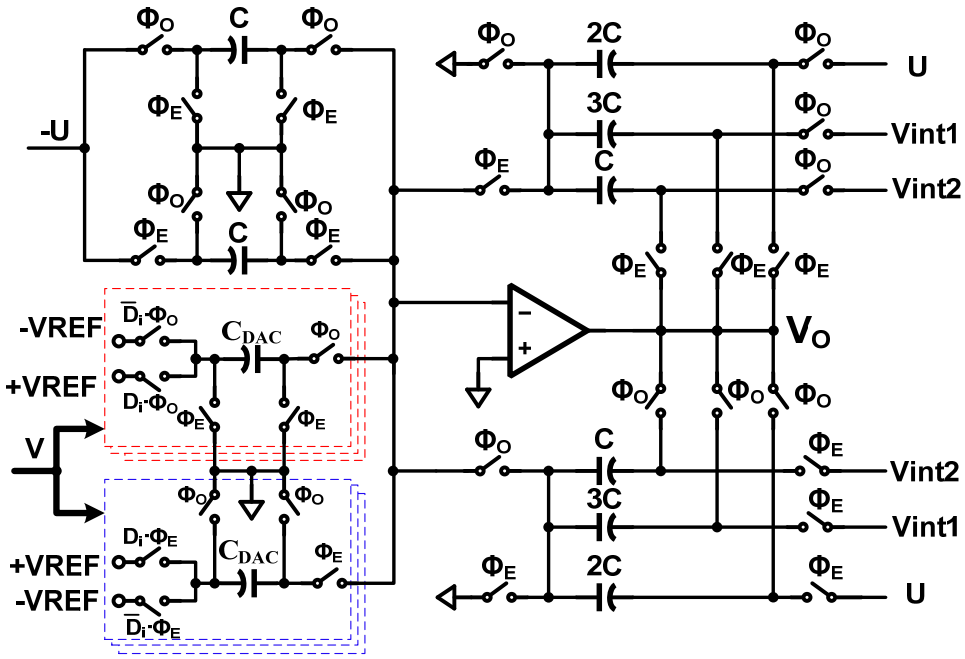

Figure 7.16: Single-ended circuit diagram of DCT adder in the 2nd order double-sampling ΔΣ modulator.

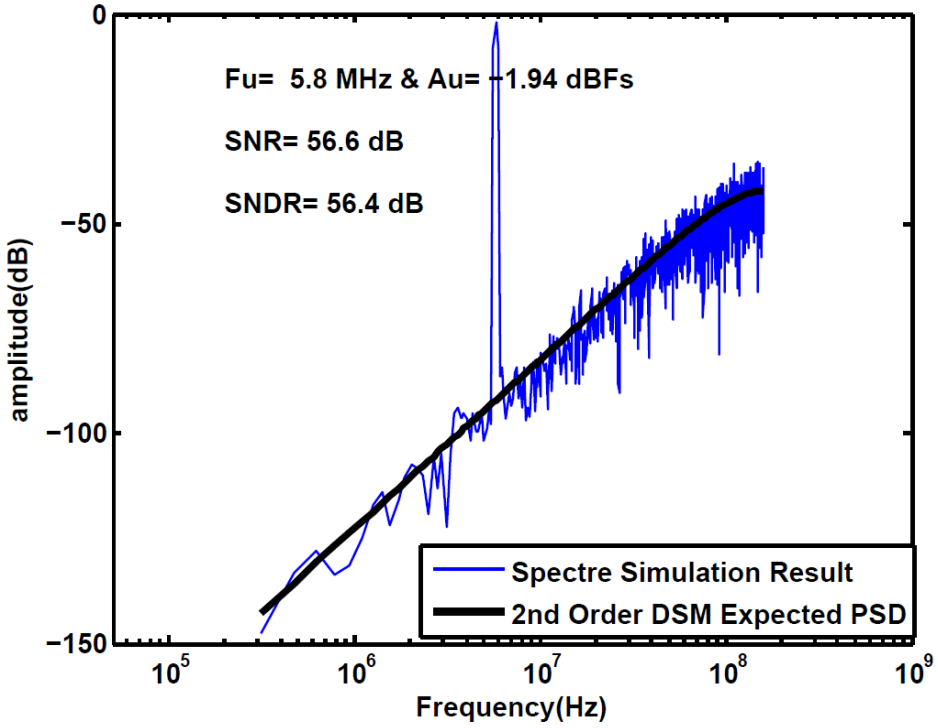

Figure 7.17: Simulated output spectrum of proposed double-sampling ΔΣ ADC.

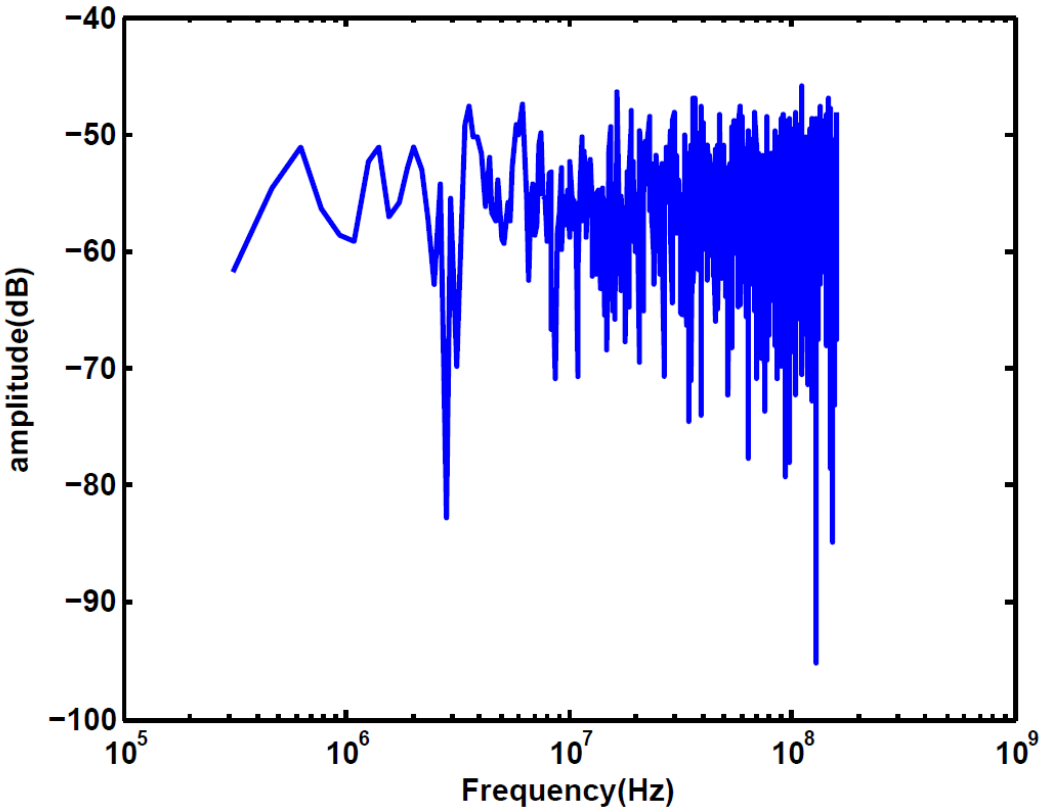

Figure 7.18: Simulated output spectrum at the second integrator output.

7.7 Conclusions

This chapter discussed new circuit design techniques for wideband low-power ΔΣ ADCs. To relax the speed requirements for the adder, a direct-charge-transfer scheme was proposed. The realization of double-sampling ΔΣ ADCs with DCT adders was also discussed. Combining the noise-coupling technique with double sampling and the DCT adder scheme, low-power and wideband performance can be achieved.

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CHAPTER. 8 NOISE-COUPLED LOW-POWER INCREMENTAL ADCS

The noise-coupling technique is introduced into the design of incremental ΔΣ ADCs using extended counting. A reduced number of integrators and hence lower power dissipation can thus be achieved. To demonstrate the proposed idea, a second-order noise-coupled incremental ΔΣ modulator with extended counting structure was designed and simulated.

8.1 Introduction

Analog-to-digital converters (ADCs) used in the instrumentation and measurement (I&M) and in biomedical applications usually deal with very low-bandwidth but very weak signals, comparable to the background noise. Therefore, they often require very high accuracy and linearity, as well as very low offset and noise. Conventional oversampling ΔΣ ADCs are not suitable for these applications, because they don't provide low offset and accurate gain without complicated digital calibration filters. However, a special type of oversampling ADCs, called incremental data converters (IDCs) [1]-[2], are well matched to such design requirements, and can provide accurate conversion within a short conversion time.

In general, IDCs perform as ΔΣ ADCs operating in a transient mode. Their operational principle can be simply illustrated as follows [3]: the input signal is first oversampled by a ΔΣ modulator for a certain number N of cycles (defined the oversampling ratio), an estimate of input signal is thus calculated based on the modulator output samples. Afterwards, all of the modulator's integrators are reset for processing the next input signal. So, IDCs can also be readily multiplexed between multiple channels.

A one-bit quantizer is often used in IDCs for high linearity consideration. As in conventional ΔΣ ADCs, the resolution of IDCs can be improved by means of increased loop filter order L and oversampling ratio N. However, a ΔΣ modulator with single-bit quantizer is susceptible to instability when the loop filter order is higher than two. The maximum oversampling ratio is also limited by the input signal bandwidth, since low power dissipation is also an important consideration. By using a technique similar to extended counting in a two-step process (Fig.8.1) [4]-[5], the resolution of IDCs with low-order single-bit modulator and lower oversampling ratio can be improved significantly. Calibration is also unnecessary for this architecture. Low power dissipation is thus achieved.

Compared to the feedback architecture, the feed-forward structure, especially the low-distortion structure [6] in Fig. 8.2, is useful in the design of ΔΣ modulators to reduce the linearity requirement of integrators and achieve better power efficiency. However, an adder is required to sum all integrators output before it is sampled by the quantizer and it requires additional opamp and extra power dissipation. A passive adder can be used to save power dissipation, but the adder output voltage is attenuated by total input capacitors and is sensitive to parasitic capacitances. The modulator performance is also prone to comparator kickback noise.

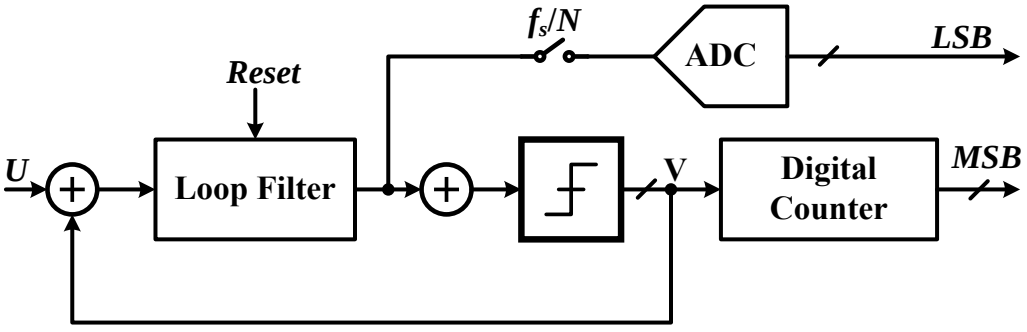

Figure 8.1: Block diagram of an extended-counting Incremental ADC.

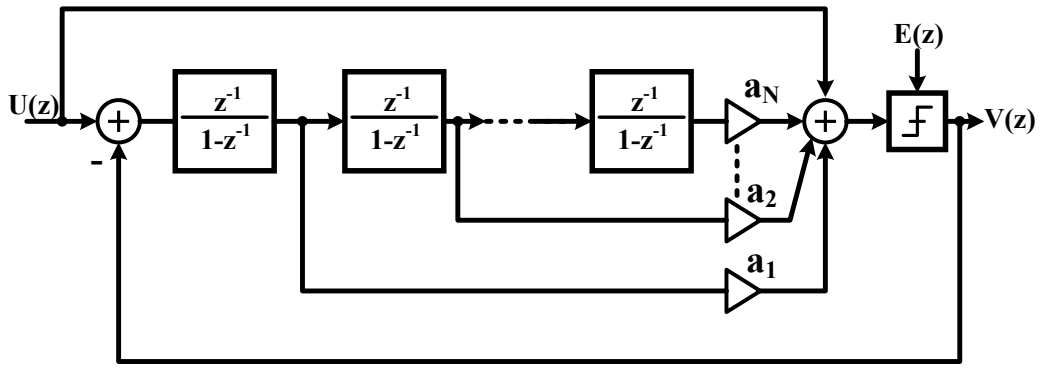

Figure 8.2: Block diagram of a low-distortion feed-forward ΔΣ modulator.

In this chapter, the noise-coupling technique [7]-[8] is proposed for the design of incremental ΔΣ modulators. By extracting the quantization noise and coupling it to the loop filter output, a first-order noise-shaping enhancement can be achieved. For a low-distortion modulator with *L*-th order noise shaping, only *L*-1 integrators are needed. The power dissipation can thus be reduced. Since the adder is realized as an active stage, the kickback noise effect and parasitic sensitivity are much relaxed.

This chapter is organized as follow. Section 8.2 describes the operating principle of noise-coupled incremental ΔΣ modulators. Section 8.3 applies the noise-coupling technique in the first stage incremental modulator of the extended counting structure, and simulation results are given to verify the proposed solution. Section 8.4 draws the conclusions.

8.2 Noise-Coupled Incremental ADCs

Fig. 8.3 shows the general block diagram of noise-coupled incremental ΔΣ modulators. The adder output is the linear combination of loop filter output and previous cycle quantization noise.

$$Y(z) = \left[U(z) - V(z)\right]H(z) - z^{-1}E(z) \tag{8.1}$$

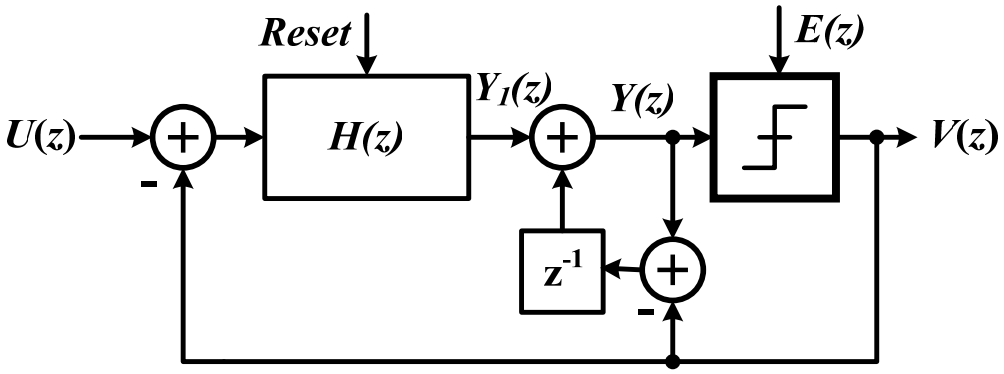

Figure 8.3: Block diagram of the noise-coupled incremental ΔΣ modulator.

To make the numerical estimation of $Y(z)$ possible, the adder output $Y(z)$ should be only determined by the deterministic signals, U(z) and V(z) of the modulator, which means that a simplified equivalent model should be derived for noise-coupled structures. As is shown in Fig. 8.4(a), the adder with noise-coupling can be decomposed into two input branches, one from $Y_1(z)$ and the other one-cycle delayed $V(z)$, followed by a local feedback loop whose transfer function is equal to a delay-free integrator. A more detailed behavioral model is thus described in Fig. 8.4(b). Actually, the adder output is the sum of $Y_{1a}(z)$ and $Y_{2a}(z)$,

$$Y_{1a}(z) = Y_1(z)\frac{1}{1-z^{-1}} \qquad \text{and} \qquad Y_{2a}(z) = V(z)\frac{z^{-1}}{1-z^{-1}} \tag{8.2}$$

Therefore, Eq. 8.1 becomes

$$Y(z) = \frac{H(z)}{1-z^{-1}}U(z) - \frac{H(z)+z^{-1}}{1-z^{-1}}V(z) \tag{8.3}$$

For a given noise-coupled incremental ΔΣ modulator, the input signal $U(z)$, modulator output $V(z)$ and the loop filter transfer function $H(z)$ are all known, so the adder output at the end of N cycles is then readily calculated knowing the initial conditions of the system, which are zero at all integrator outputs and modulator output.

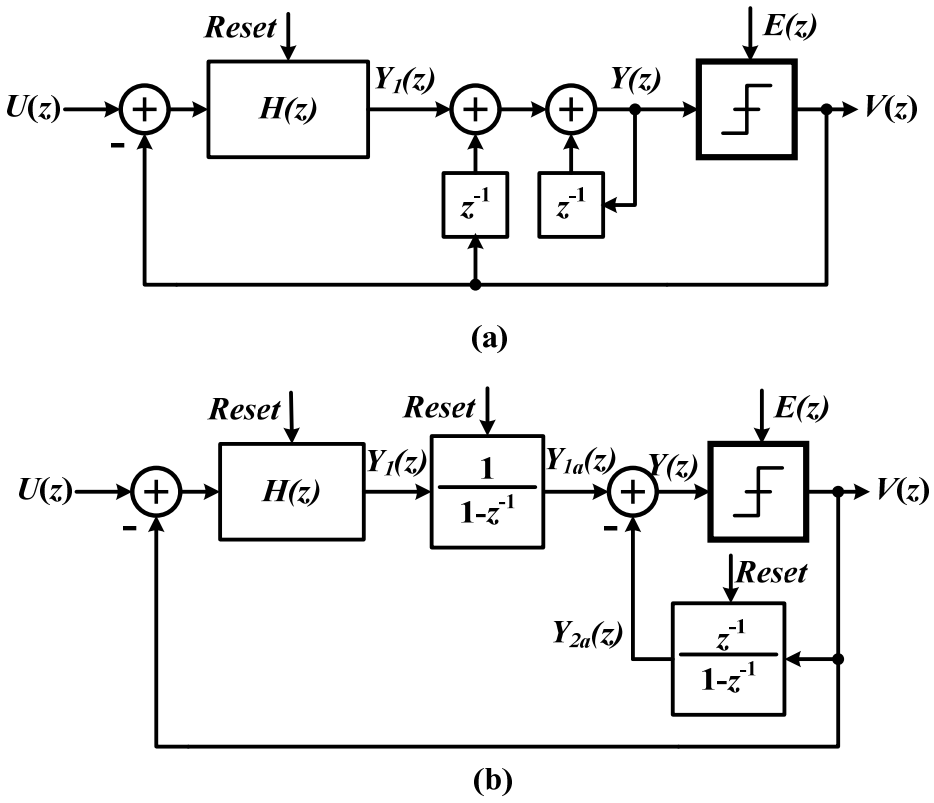

Figure 8.4: Equivalent models of the noise-coupled incremental ΔΣ modulator.

8.3 Design Example

For a verification of the effectiveness of the proposed architecture, a noise-coupled incremental ΔΣ modulator targeting a biomedical application was designed. To simplify the discussion, single-channel input signal is considered. The key design specifications are summarized at Table. 8.1.

Table 8.1: Design specification of the incremental ΔΣ ADCs.

Design Parameters	Design Specifications
Signal Bandwidth	1 kHz
Oversampling Ratio	128
Quantizer Resolution	1 bit
Conversion Resolution	16 bits

For the incremental ADC design, the conversion accuracy is usually affected by different noise sources, such as the wideband thermal noise, low-frequency flicker noise and the quantization noise. Using chopping and/or correlated-double sampling (CDS) techniques [9], the flicker noise can be effectively cancelled. For low-power design, it is desirable to make the noise floor dominated by the thermal noise, which means the conversion error due to quantization noise should be made negligible. In this application, more than 120dB signal-to-quantization noise ratio (SQNR) is targeted. Since the oversampling ratio is limited to 128 for low power dissipation, a single-loop second-order incremental ADC cannot fulfill the design requirement. To increase the conversion accuracy and at the same time maintain good stability of the loop, the extended counting structure [4], [5] is used. Fig. 8.5 shows the overall architecture. For the first-stage ΔΣ loop, a first-order modulator with noise coupling is used. So, an effective second-order noise shaping is achieved. By adding a direct input branch to the quantizer, the signal transfer function of the modulator becomes equal to 1. So, the integrator only needs to deal with the quantization noise and its linearity requirement is greatly relaxed. The modulator periodically processes the input signal for 128 clock cycles, and then reset for the next input signal conversion. Based on the discussion in Section II, the adder output voltage y(N) after N clock cycles is the accumulated input signal and modulator output bit sequence v(k). Assuming a dc input voltage, y(N) is

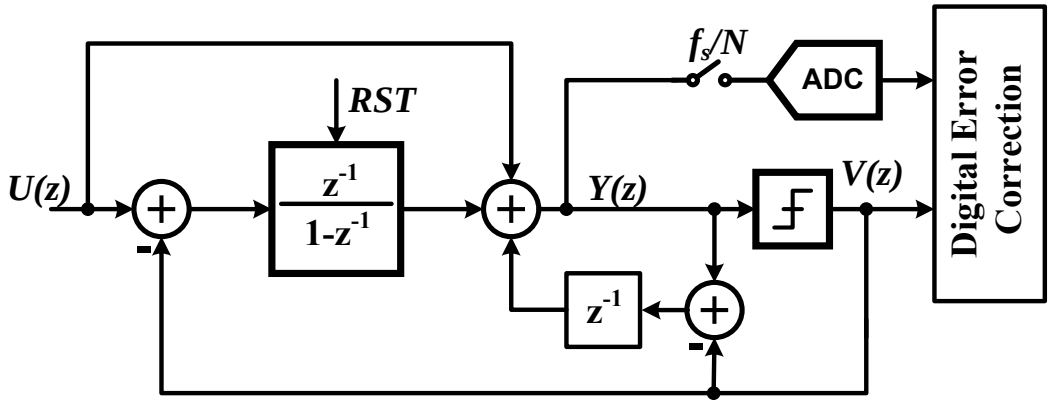

Figure 8.5: The noise-coupled IDC using extended counting.

$$y(N) = \sum_{l=1}^{N}\sum_{k=0}^{l-1} u + \sum_{k=1}^{N} u - \sum_{l=1}^{N}\sum_{k=0}^{l-1} v(k) - \sum_{k=0}^{N-1} v(k) \tag{8.4}$$

If the modulator is stable, y(N) is a bounded value. So, if N is large enough, the estimate of input signal u is

$$u \approx \frac{2}{N(N+1)} \sum_{k=0}^{N-1} (N+1-k)v(k) \tag{8.5}$$

The estimation error is

$$e_{y[N]} = \frac{2}{N(N+1)} y(N) \tag{8.6}$$

To reduce $e_{y[N]}$, the adder output is further sampled at the end of each conversion cycle, and then digitized by a power-efficient successive approximation (SAR) ADC. Using digital error correction logic, the quantization error in the overall output is then ideally only due to the quantization error of the SAR ADC:

$$e_{Q-ADC} = \frac{2}{N(N+1)} e_{Q-SAR} \tag{8.7}$$

So, with a high-resolution SAR ADC, the residue error can be greatly reduced.

From Eq. 8.5, the estimated value of input signal is given by the convolution of the modulator output sequence v(k) and the impulse response of a decimation filter H_{DEC}(z) with linear phase shift, whose transfer function is

$$H_{dec}(z) = \frac{2}{N(N+1)} \sum_{k=0}^{N-1} (k+1) z^{-k} \tag{8.8}$$

The frequency response of H_{dec}(z) is plotted as Fig. 8.6

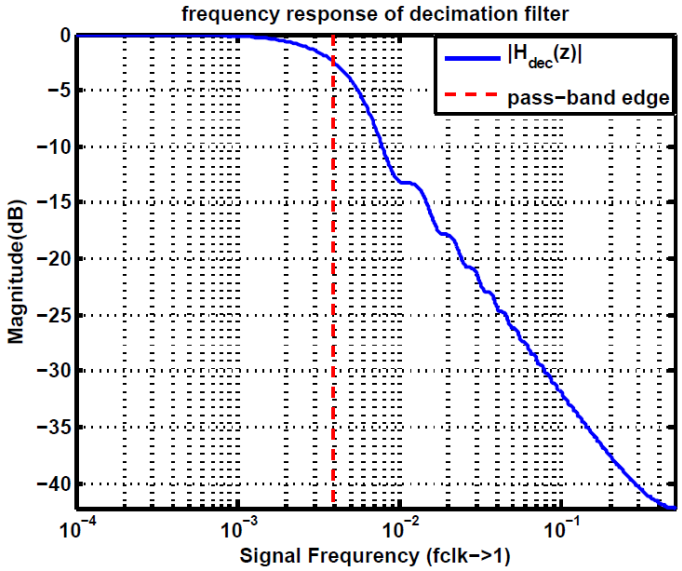

Figure 8.6: Frequency response of the decimation filter.

So, the decimation filter gain is zero dB at dc, and decreases with increased frequency. For OSR=128, the gain drop at the edge of signal band is around -2.5dB, so the input signal is attenuated at the incremental ADC output. This can be easily compensated in the following digital signal processor.

To check the incremental ADC conversion accuracy for a dc input signal, the input voltage was swept over the signal range. The resolution of the additional SAR ADC was set to 6 bits. Fig. 8.7 shows the relative quantization error, scaled to each input amplitude Au, before and after applying extended counting. Large improvements have been achieved for all input values. The conversion accuracy limited only by quantization error with extended counting is also plotted at Fig. 8.8, in which the *LSB* is for 20 bit accuracy. Therefore, with 2^{nd} order noise-shaping, an OSR=128 and single-bit quantizer, 20 bit accuracy can be achieved with an additional 6 bit SAR ADC.

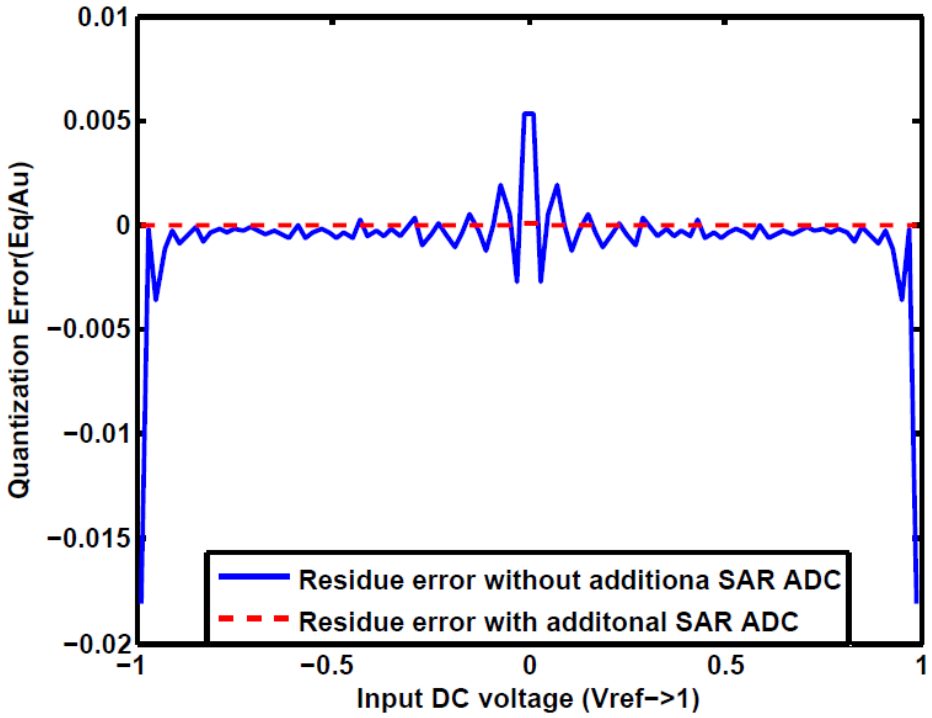

Figure 8.7: The relative quantization error before and after extended counting.

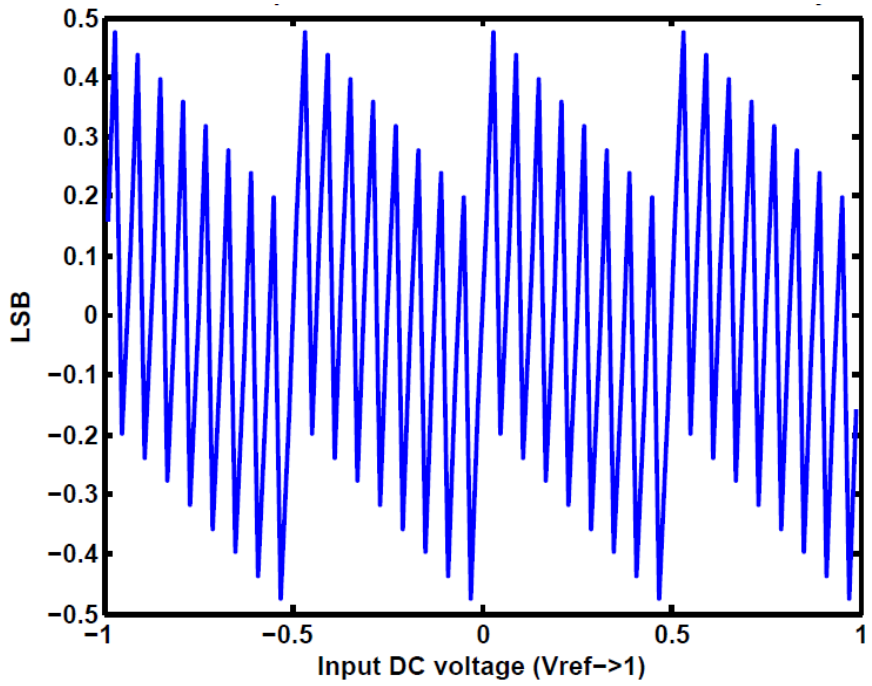

Figure 8.8: The ideal dc conversion accuracy of designed noise-coupled incremental ADC.

With a -2.5dB, 250Hz sinusoidal input signal, the simulated output spectrum is shown in Fig. 8.9. Assuming ideal analog blocks, the SQNR is 119.6 dB.

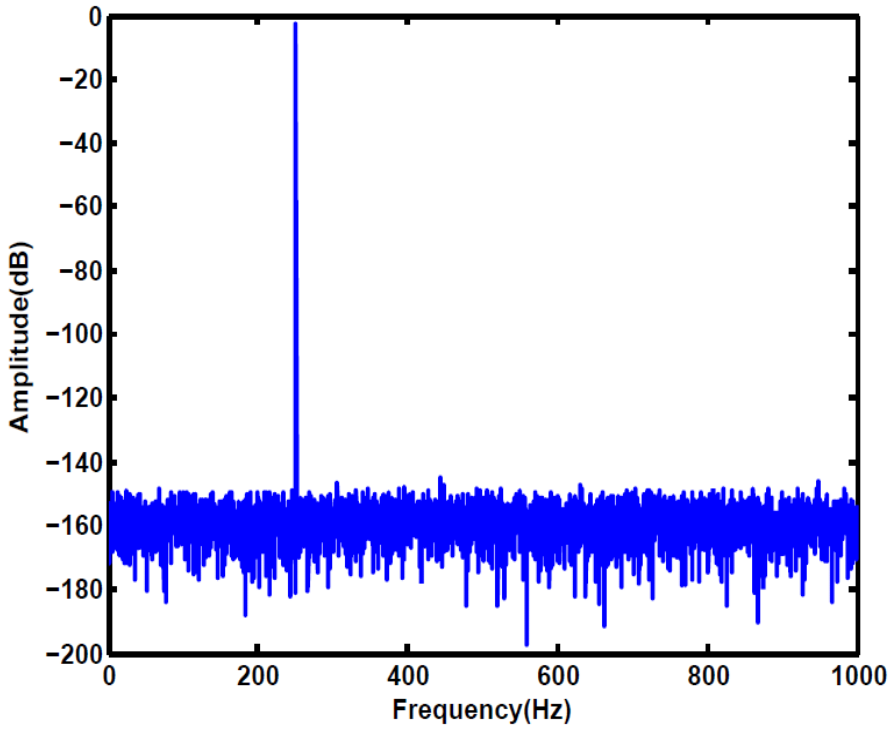

Figure 8.9: The simulated output spectrum with -2.5dB, 250Hz input signal.

8.4. Conclusions.

Noise-coupling technique is proposed for the design of incremental data converter. Combined with an extended counting structure, a low-power high-accuracy noise-coupled incremental ADC has been designed and verified with simulation.

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CHAPTER 9. CONCLUSIONS

9.1 Summary

In this dissertation, the following topics associated with wideband, low power analog-to-digital converters in different applications were studied in detail:

- A new dynamically-biasing technique was described for switched-capacitor circuits; the non-linearity issue due to the signal-dependant biasing current was solved by the proposed low-distortion DT ΔΣ ADC architecture.
- The low-distortion technique immune to excess-loop delay was introduced for CT ΔΣ modulator. The linearity requirements of the integrator are then greatly relaxed and inter-stage gain can then be applied to CT MASH. Also, a digital calibration technique was presented to compensate for the quantization noise leakage in CT MASH. The proposed new techniques were applied in a novel high-performance CT 2-2 MASH and analog circuit design requirement, and the power dissipation was greatly reduced.
- A noise-coupled CT ΔΣ ADC technique, which is promising for wideband low-power application, was proposed and theoretically proven. The effectiveness of the technique was verified by the design example.
- The second-order noise coupling technique was presented to achieve higher order noise shaping enhancement. New circuit topologies were also proposed to simplify the noise-coupling branches. With reduced number of integrators, it is promising for low-power applications.
- A new active-adder using direct-charge-transfer technique was presented for the design of wideband high performance ΔΣ modulators. The adder speed requirement is thus not limited by the order and number of input branches. The application in the noise-coupled ADCs was also described. Finally, a hybrid DCT adder was introduced to optimize the design trade-offs between adder and the quantizer.

- The noise-coupling technique was extended to the application of high resolution incremental ADCs. Lower power and wider bandwidth can be expected. The proposed idea was verified by a noise-coupled incremental data converter using extended counting architecture.

9.2 Future Works

For an extension or improvement of current research works, some existing design issues can be further explored in the future:

- The averaged biasing current of the dynamic-biased integrator is higher than constant biasing scheme due to the settling time requirement of the amplifier. Some new methods may be found to improve the biasing scheme with reduced current dissipation.
- To reduce the jitter noise of external clock source, an OSR=8 was chosen for the CT 2-2 MASH design. It would be worth checking the distortion and power dissipation performance with higher OSR values.
- The digital calibration filter was realized in software for easier verification. An improved version should realize it in hardware.
- The proposed digital calibration technique for CT MASH requires millions clock cycles to complete the noise leakage calibration, which increases the testing cost and time for mass production. It might be worth exploring a more efficient calibration algorithm to reduce the calibration time.
- The noise-coupled CT $\Delta\Sigma$ modulator, noise-coupled incremental ADC, second-order noise-coupled structure and the DCT adder were only demonstrated in behavioral systems with ideal macro-models. It might be worth verifying these ideas with real chips.