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John F. Wager

The aim of this dissertation is to develop oxide semiconductors by radio-frequency sputtering for thin-film transistor (TFT) applications. A variety of oxide semiconductors are used as the TFT channel layer, including indium gallium oxide (IGO), zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO). The variety of materials used underscores the abundance of materials options available within this nascent technology, with each material exhibiting unique chemical, mechanical, and electrical properties. The influence of several deposition parameters is explored; oxygen partial pressure of the deposition ambient is found to have a profound effect on the electrical characteristics of each material. With optimized deposition conditions, TFTs based on these materials exhibit excellent electrical properties, even when annealed at low-temperature (175 °C). Specifically, ZTO-based TFTs which are subjected to a 175 °C post-deposition anneal exhibit a channel mobility near 9 $cm^2V^{-1}s^{-1}$. However, advancement of this technology also requires research in integration-related issues. Therefore, the effect of channel

layer passivation and of TFT stability is evaluated. Passivation of the oxide semiconductor surface is required for circuits which employ multiple levels of interconnect and for mechanical/chemical protection of devices. Here, successful passivation of IGO, ZTO, and IGZO-based TFTs is demonstrated using SU-8, a negative tone epoxy-based photoresist. To appraise TFT stability, a constant voltage bias stress test of 1000 minutes is utilized, where the drain current, I_D, is monitored throughout the duration of testing and the turn-on voltage, V_{on}, is evaluated before and after stressing. TFT stability is found to be correlated to the turn-on voltage of a device and to the thickness of the semiconductor layer. IGZO-based TFTs with excellent stability are demonstrated, exhibiting almost no decrease in I_D or any shift in V_{on} throughout the duration of bias stress testing.

Development of Oxide Semiconductors: Materials, Devices, and Integration

by

Hai Q. Chiang

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Hai Q. Chiang, Author

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DEVELOPMENT OF OXIDE SEMICONDUCTORS: MATERIALS, DEVICES, AND INTEGRATION

1. INTRODUCTION

Semiconductor research began in the 1920's. However, semiconductors were initially viewed as useless materials whose properties were not reproducible. [1] Additionally, there was a lack of basic solid state physics understanding. For example, silicon was initially believed to be a metal. Despite all of this, there were many advances that helped mold the semiconductor industry as we know it today. Two key advances occurred in the 1920-30's. First, a model for point defects in ionic compounds was proposed [2, 3, 4]; this is of particular importance for oxide semiconductors, a topic of central importance to this dissertation. Second, a distinction between intrinsic and extrinsic semiconductors was provided in the context of donors and acceptors. [5, 6]

The earliest investigated oxide semiconductors include Cu_2O [7, 8] and ZnO [9]. Initially, Cu_2O was not well understood; Cu_2O samples produced by different researchers showed enormous variation in conductivities, up to six or seven orders of magnitude. [1] However, an experiment performed by Dunwald *et al*. helped identify the source of this variation. In this experiment, it was found that the conductivity of Cu_2O increased with increasing oxygen pressure, indicating that the stoichiometry of the Cu_2O sample significantly affects conductivity. A similar oxygen pressure experiment was performed using ZnO. However, the behavior of ZnO was opposite to that of Cu_2O, i.e., the conductivity

decreased with increasing oxygen pressure. To explain this discrepancy, Wagner distinguished between cation and anion vacancies, noting that cation vacancies lead to “deficit” (hole) conduction, while anion vacancies lead to “excess” (electron) conduction. [10] To this day, researchers still use oxygen pressure to control the conductivity of oxide semiconductors.

The first commercial application for oxide semiconductors came during World War II, when degenerately doped SnO_2:Sb was deposited by spray pyrolysis to serve as a window defroster in airplanes. [11] Currently, the largest application for oxide semiconductors involves coatings for low-emissivity windows. In this application, degenerately doped SnO_2:F is commonly employed, and in which free electrons in the SnO_2:F reflect infrared radiation. Other applications for oxide semiconductors include solar cells (SnO_2:F, ZnO, In_2O_3:Sn), flat-panel displays (In_2O_3:Sn), and oven window coatings (SnO_2). The commonality between these applications is that they all utilize the oxide semiconductor in a passive manner. Moreover, these applications utilize oxide semiconductors with degenerate doping as pseudo-conductors. Thus, oxide semiconductors are commonly referred to as transparent conducting oxides (TCOs).

Limited to exclusively passive applications, it is not surprising that oxide semiconductor research has primarily focused on developing materials which are highly transparent and conductive. However, with the introduction of the transparent thin-film transistor (TTFT) in 2003, there has been a paradigm shift. [12, 13] A small subset of researchers began to explore a wide variety of oxides (e.g., ZnO, zinc tin oxide (ZTO), zinc indium oxide (ZIO), and indium gallium zinc oxide (IGZO)) for active applica-

tions, rather than passive applications that have been so prevalent for over half a century. [12, 13, 14, 15, 16, 17] In essence, these oxide materials have begun to be viewed as semiconductors (once again), rather than transparent conductors.

Significant advances have been made in oxide semiconductor-based TFT research. These advances include several demonstrations. First, a transparent smart-pixel with an organic light-emitting diode and ZTO-based TFT driver was demonstrated. [18] Next, integrated ring oscillator circuits based on indium gallium oxide (IGO) and IGZO were demonstrated. [19, 20] Finally, flexible, active-matrix electronic paper with IGZO-based TFT drivers was demonstrated. [21] However, as this technology is quite nascent, there have been very few reports of fundamental research regarding these oxide materials and their stability for TFT applications. [22, 23, 24]

The primary goal of this dissertation is to identify the dominant radio-frequency sputtering process parameters which affect TFT device performance for various oxide semiconductor channel materials. These materials include ZTO, IGO, and IGZO. Low-temperature processes which are compatible with plastic substrates are also established. A secondary goal of this dissertation is to evaluate integration-related issues. These issues include TFT stability and the effect of channel layer passivation.

The structure of this dissertation is as follows. Chapter 2 reviews pertinent literature, including general information on oxide semiconductors and thin-film transistors. Chapter 3 presents TFT device development, fabrication, and characterization issues. Chapter 4 summarizes the effect several experimental variables on the performance

of oxide-based TFTs. Chapter 5 summarizes integration-related issues regarding oxide-based TFTs. Chapter 6 provides conclusions and recommendations for future work.

2. OXIDE SEMICONDUCTORS AND THIN-FILM TRANSISTORS

This chapter first provides an overview of oxide semiconductors. Then, the morphology and properties of several multicomponent oxide semiconductors (zinc tin oxide (ZTO), indium gallium oxide (IGO), and indium gallium zinc oxide (IGZO) are discussed in more detail, as they are used extensively in this work. Next, an overview of thin-film transistors (TFTs) is given; this includes a description of basic TFT operation and TFT structures typically employed. Finally, the electrical properties of several oxide semiconductor-based TFTs are reviewed.

2.1 Oxide semiconductors

This section first summarizes the properties of well-known degenerate oxide semiconductors or transparent conducting oxides (TCOs). Then, several oxide semiconductors (ZTO, IGO, and IGZO) are discussed in more detail, as they are used extensively in this work.

2.1.1 Transparent conducting oxides overview

Transparent conducting oxides (TCOs) is a class of large band gap (typically $E_g \geq$ 3.1 eV, due to the large electronegativity of oxygen in *n*-TCOs [25]) materials that exhibit a high level of optical transparency (80-90%) and conductivity. n-type TCO conduction is derived from two sources: the creation of point defects (such as oxygen vacancies and/or metal interstitials) or extrinsic substitutional doping (typically on the cation site). The

point defect concentration can be modified during the deposition process by appropriate selection of process parameters or by subjecting the sample to an oxidizing or reducing post-deposition anneal. The drawbacks of using intrinsic defects as the primary source of conduction are the possibility of film re-oxidation and (typically) inferior conductivity compared to substitutionally doped films.

The minimum theoretical resistivity limit for n-TCOs has been predicted by Bellingham *et al.* as 4×10^{-5} Ω·cm. [26] This limit is a consequence of transport that is constrained by ionized impurity scattering ($\mu < 90$ cm^{2}V^{-1}s^{-1}) and carrier concentration limitations due to increasing optical reflection with increasing carrier concentration ($n < 2 \times 10^{21}$ cm^{-3} for >90% optical transmission). Experimental results for a single crystal In_2O_3:Sn thin film have approached this theoretical resistivity limit, yielding a minimum resistivity of $\sim 7.7 \times 10^{-5}$ Ω·cm ($\mu = 42$ cm^{2}V^{-1}s^{-1}, $n = 1.9 \times 10^{21}$ cm^{-3}). [27]

TCOs are currently utilized in a number of passive applications, including thin-film solar cells and flat-panel displays. SnO_2 is commonly employed in applications where patterning is not required (as SnO_2 is difficult to chemically wet etch) and when high levels of conductivity are not required. Of the commercially available TCOs, In_2O_3:Sn is the most conductive. In_2O_3:Sn is also easier to etch than SnO_2 and can be deposited at lower temperatures. Unfortunately, the availability of indium is limited, as it is a byproduct of mining ores for other metals (such as zinc and lead). [11] Moreover, indium is not as abundant as other metals; there is $\sim$ 1000 times more zinc (132 ppm) than indium (0.1 ppm) in the earth's crust. [28, 29] Thus, efforts are being made to find a suitable replace-

ment for In_2O_3:Sn. Among the materials being explored is ZnO:Al, which is attractive for its ease of etchability, stability in hydrogen plasmas, and low process temperature requirement. [30, 31]

Table 2.1 summarizes optical and physical properties of various n-type TCOs. The tabulated electron affinity, χ, is the difference between the vacuum level and conduction band minimum and is assumed to be approximately equal to the work function (the difference between the vacuum level and the Fermi level) for these degenerate semiconductors. Also note that two TCOs, $CuInO_2$ and ZnO, exhibit bipolar conductivity. A summary of p-type TCOs can be found elsewhere. [32]

Table 2.1: Typical properties of various n-type transparent conducting oxide semiconductors. E_g^{opt} represents the optical band gap, χ represents the electron affinity, T represents the percentage transmitted in the visible portion of the electromagnetic spectrum, m^*/m_e represents the density of states effective mass, μ_H represents the Hall mobility, n represents the carrier concentration, and ρ represents the resistivity.

Material	E_g^{opt} (eV)	χ (eV)	T (%)	m^*/m_e	μ_H ($cm^2V^{-1}sec^{-1}$)	n (cm^3)	ρ ($\Omega \cdot cm$)	References
CdO	2.2-2.6		75	0.18-0.25	220	10^{19}-10^{21}	2x10^{-3}	[28, 33]
Cd_2SnO_4	2.9-3.1		90	0.29-0.42	35-60	1-7x10^{20}	1.4-12x10^{-4}	[28, 34, 35, 36]
In_2O_3	3.7	3.7	80-90	0.35	10-40	$\leq 10^{21}$	$\geq 10^{-4}$	[29, 36, 37]
$InGaO_3$	3.3	5.4	90		10	10^{20}	2.5x10^{-3}	[38, 39]
$InGaZnO_4$	3.5		80-90	0.2	24	$\sim 10^{20}$	2x10^{-3}	[40, 41, 22]
SnO_2	3.6	4.5	80-90	0.23^l, 0.30^t	5-30	$\leq 10^{20}$	$\geq 10^{-3}$	[29, 36, 42]
ZnO †	3.2-3.3	4.5-5	80-90	0.27	5-50	$\leq 10^{21}$	$\geq 10^{-4}$	[29, 36, 39]
$Zn_2In_2O_5$	2.9	4.9	80		12-20	2.4-5x10^{20}	1-4x10^{-3}	[35, 39, 43]
$ZnSnO_3$	3.5	5.3	80		7-12	10^{20}	4-5x10^{-3}	[39, 44, 45]
Zn_2SnO_4	3.3-3.9		90	0.16-0.26	12-26	6-30x10^{18}	1-5x10^{-2}	[35, 46, 47]

†Bipolar conductive material [48, 49, 50]

^{l} Longitudinal effective mass

^{t} Transverse effective mass

2.1.2 Amorphous oxide semiconductors

Amorphous oxides composed of post-transition metal cations with (n-1)$d^{10}ns^0$ (n $\geq$ 4) electronic configurations constitute an interesting subcategory of transparent conductors, since they possess relatively high electron mobilities despite their amorphous character. [51, 52, 53] Examples of such materials include indium oxide doped with tin (ITO) [54] and zinc tin oxide [55] for which amorphous-state mobilities as large as 40 and 30 $cm^2V^{-1}s^{-1}$, respectively, have been reported. Such high mobilities in an amorphous material are likely a consequence of a conduction band primarily derived from spherically symmetric, post-transition metal cation n*s* orbitals. Such orbitals have large radii, leading to a high degree of overlap between adjacent orbitals and considerable band dispersion. Moreover, the spherical symmetry of an *s* orbital makes delocalised electronic transport less sensitive to local and extended structural order as compared with band formation from anisotropic *p* or *d* orbitals. Furthermore, compared to binary oxide semiconductors, multicomponent oxide semiconductors increase the likelihood that the structure will remain amorphous over a wide range of processing conditions. Zinc tin oxide, indium gallium oxide, and indium gallium zinc oxide are discussed below, as these materials are used extensively in this work.

2.1.3 Zinc tin oxide

Zinc tin oxide (ZTO), which is sometimes referred to as zinc stannate, has recently received attention as an alternative TCO. It is most generally described as $(ZnO)_x$-$(SnO_2)_{1-x}$, where $0 < x < 1$. There are two crystalline forms of ZTO, trigonal ilmenite

($ZnSnO_3$, $x = 0.5$) [56] and spinel (Zn_2SnO_4, $x = 0.66$) [46]. As shown by Shen *et al*., powder mixtures with stoichiometry close to trigonal ilmenite ZTO ($ZnSnO_3$) decompose to spinel ZTO (dizinc tin oxide, i.e. Zn_2SnO_4) and SnO_2 at calcination temperatures above 700°C. [57] Several aspects that make ZTO attractive are its low-cost nature (does not utilize In or Ga cations), its chemical and electrical stability in highly concentrated ($> 35\%$) HCl solutions and its physical robustness, [44, 47] i.e. no damage to the thin film is visually apparent after scratching with the corner of a razor blade.

The zinc tin oxide phase space has been examined by Moriga *et al*. using dc co-sputtering from a ZnO and SnO_2:Sb (Sb_2O_5) target. [58] For temperatures up to 350 °C, films with $0.33 \leq x \leq 0.66$ were found to be amorphous. These amorphous films exhibit a constant Hall mobility of ~ 10 $cm^2V^{-1}s^{-1}$. The carrier concentration decreases linearly as the Zn concentration is increased from $x = 0.33$ ($ZnSn_2O_5$) to 0.66 (Zn_2SnO_4). The minimum resistivity is $4 \times 10^{-2}\Omega$cm and occurs at $x = 0.33$.

Other authors have shown that crystalline spinel ZTO (Zn_2SnO_4) thin films are attainable through the use of a variety of deposition techniques, including electron beam evaporation, [59] rf magnetron sputtering, [35, 46, 47, 60, 61] chemical vapor deposition, [47, 62] and spray pyrolysis. [63] In actuality, rf magnetron sputtered Zn_2SnO_4 has been found to have an inverse spinel, in which half of the Zn cations exchange sites with Sn cations. [47, 60]

Optical and electrical properties crystalline ZTO are tabulated in Table 2.1. Spinel ZTO is a direct band gap material with a fundamental band gap of 3.35 eV. Spinel ZTO exhibits a pronounced Burstein-Moss shift, a phenomenon discussed in Sec. 3.2.2. Con-

comitant with the Burstein-Moss shift is a small relative electron effective mass ($0.16m_e$). Thus, one would expect the mobility to be quite large since,

$$\mu = \frac{q\tau}{m^*}, \tag{2.1}$$

where τ is the relaxation time and m^* the effective mass. However, the maximum measured Hall mobility for a rf magnetron sputter deposited thin-film is only 26 $cm^2V^{-1}sec^{-1}$. Thin films fabricated to date have been limited by intra-grain defects due to atomic disorder, which may not be alleviated even in single crystal growth. [46, 47, 60]

Applications of ZTO have been somewhat limited due to its low conductivity, but ZTO has been employed in thin-film solar cell applications [64] and humidity and gas sensors. [63, 65, 66, 67]

2.1.4 Indium gallium oxide

Indium gallium oxide is a wide band gap, n-type semiconductor; its stoichiometry can be generally described as $In_{2x}Ga_{2-2x}O_3$, where $0 < x < 1$. Based on Raman spectroscopy [68] and X-ray diffraction (XRD) analysis [69], solid solutions of $In_{2x}Ga_{2-2x}O_3$ where $x \leq 0.43$, results in In substitution into the β-Ga_2O_3 lattice and $x \geq 0.95$ results in Ga substitution into the cubic In_2O_3 lattice. For $0.43 < x < 0.95$, phase segregation occurs and results in a β-Ga_2O_3 phase and an In_2O_3-Ga_2O_3 phase with the cubic In_2O_3 structure. [69] Thin films of $InGaO_3$ ($x = 0.5$) have been reported to be amorphous [70] and with the β-Ga_2O_3 crystal structure [38, 71].

The optical band gap without intentional doping of $InGaO_3$ is $3.3-3.4$ eV. [70, 71] The applications for indium gallium oxide have been quite limited; it has mainly

been explored as a transparent conductor. [38, 70, 71, 72] One advantage of indium gallium oxide over other transparent oxide semiconductors, e.g., indium oxide doped with tin (ITO), is its improved transmission in the blue-green region of the electromagnetic spectrum. [71]

2.1.5 Indium gallium zinc oxide

Indium gallium zinc oxide (IGZO) is a wide band gap ($\sim$3.5 eV), n-type semiconductors; its stoichiometry can be generally described as $In_{2x}Ga_{2-2x}(ZnO)_k$, where $0 < x < 1$ and k is an integer that is greater than 0. [22, 40, 41, 73, 74, 75, 76, 77] Crystalline indium gallium zinc oxide is composed of alternating layers of InO_2^- and $GaZnO_4^+$; the In^{3+} ion has octahedral coordination, the Ga^{3+} ion has pentagonal coordination, and the Zn^{2+} has tetragonal coordination. [41, 73, 74] Several groups have synthesized bulk samples with varying stoichiometry (both x and k) to appraise the solubility limits of the structure. [73, 74] The intriguing result is that, regardless of k, when $x = 0.5$ (equal proportions of In and Ga) the structure is preserved. In other words, $x = 0.5$ constitutes the base compound where all the In^{3+} ions are in the InO_2^- and all the Ga^{3+} ions are in the $GaZnO_4^+$ layer.

For $k \leq 3$, the conductivity decreases as k is increased. This trend is observed in both bulk samples [74] and thin films [75], indicating that the conductivity in indium gallium zinc oxide is primarily associated with the In 5s states. However, for $k \geq 4$, the fraction of Zn becomes increasingly large and Zn begins to contribute to conduction. [75] Considering orbital overlap interaction and comparing the ionic radii of cations in the

IGZO system is useful for understanding the shift in the conduction path. The ionic radii of Ga, In, and Zn are 1.27, 1.49, and 1.54$\sim$ *Å*, respectively. As the ionic radii of In and Zn are quite similar, it is not surprising that Zn contributes to conduction as the fraction of Zn becomes increasingly large. [75]

The structure of single crystal and amorphous $InGaZnO_4$ thin films ($\sim$250 nm) are examined using extended x-ray absorption fine structure (EXAFS), which is commonly employed to appraise short range order. [22, 78, 79] The nearest-neighbor distances for In-O, Ga-O, and Zn-O in the amorphous film are 0.211, 0.200, and 0.195 nm, respectively. [22] This short range ordering is similar to that of the single crystal structure (0.218, 0.193, and 0.193, respectively). However, it appears that medium range ordering (second nearest-neighbor distances) near the Ga and Zn ions is lost in the amorphous films. *Ab initio* calculations were performed and are in good agreement with the EXAFS results. Additional calculations show that the In-In second nearest-neighbor coordination number in the amorphous state varies with distance (i.e., ~ 1 to ~ 4 for distances of 0.32 to ~ 0.4 nm) and is significantly lower than in the crystalline structure, which has a coordination number of ~ 6. This indicates that the selective (medium range) coordination of In-In is lost in the amorphous structure. From the experimental and calculated results, the coordination numbers of In-O, Ga-O, and Zn-O are deduced to be 5, 5, and 4, respectively. Finally, pseudoband calculations show that the conduction band minimum is composed of In 5*s* (consistent with the experimental results discussed in the previous paragraph) and that that amorphous IGZO has an isotropic effective mass of $\sim 0.2m_e$.

Amorphous IGZO has been employed in a light-emitting *pn* heterojunction. [80] The IGZO layer is deposited by pulsed laser deposition (PLD) at room temperature. The carrier concentration and mobility of this layer is 1×10^{19} cm^{-3} and 5 cm^{2}V^{-1}s^{-1}. Indium gallium zinc oxide is chosen here for its reasonable conductivity at low processing temperatures and its large band gap ($\sim$3.5 eV). Blue emission ($\sim$ 430 nm peak) is observed from this *pn* heterojunction and is due to intrinsic exciton recombination in the single crystal *p*-LaCuOSe layer (which has a band gap, carrier concentration, and mobility of $\sim$2.8 eV, 1×10^{19} cm^{-3}, and 8 cm^{2}V^{-1}s^{-1}, respectively).

2.2 Oxide semiconductor devices: Thin-film transistors

As the primary goal of this work is to explore oxide semiconductor-based TFTs, a short TFT review is given. This review includes a discussion of basic TFT operation and identifies commonly employed TFT structures. Next, a summary of oxide semiconductor-based TFTs is given. As the work in this field is rapidly increasing, only the most noteworthy works are reviewed here.

2.2.1 Thin-film transistors

Invention of the first field-effect device is often credited to J. E. Lilienfeld, who patented the concept in 1934. [81] However, development of the first thin-film transistor (TFT), as it is known today, is credited to P. K. Weimer (1962). [82] TFTs based on a wide variety of channel materials, including CdS, CdSe, amorphous and polycrystalline silicon, have been developed. Currently, the most dominant TFT technology is based

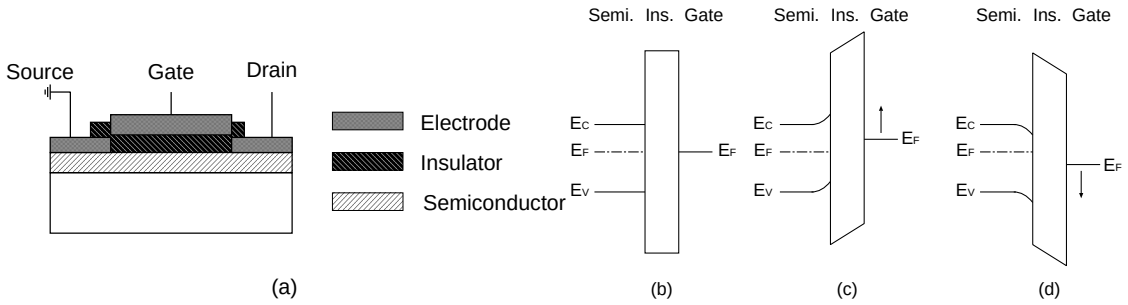


Figure 2.1: (a) The basic structure of a TFT and the corresponding energy band diagrams as viewed through the gate for several conditions, including (b) equilibrium, (c) depletion, $V_{GS} < 0$ and (d) accumulation, $V_{GS} > 0$.

on hydrogenated amorphous silicon (a-Si:H), which are commonly employed in active-matrix liquid crystal displays (AMLCDs). High performance a-Si:H TFTs typically have field-effect mobilities of approximately 1.5 to 2.0 $cm^2V^{-1}sec^{-1}$ with a maximum processing temperature of 300 °C. [83]

2.2.1.1 Basic device operation

The following discussion assumes n-channel TFT operation; a similar discussion can be applied to p-channel TFTs. Figure 2.1 shows the structure and energy band diagrams as viewed through the gate of an n-channel, accumulation-mode TFT. [84] The equilibrium band diagram shown in Fig. 2.1b assumes an ideal situation, i.e. there is no charge in the semiconductor before the application of a gate bias and indicates that the semiconductor layer is slightly n-type.

Consider two biasing schemes, depletion, $V_{GS} < 0$ and accumulation, $V_{GS} > 0$ V. Negative applied voltage ($V_{GS} < 0$) to the gate repels mobile electrons and pushes them deeper into the semiconductor, leaving a depletion layer near the interface. The posi-

tive space charge region near the semiconductor-insulator interface is consistent with the charge neutrality relationship ($-Q_M = +Q_S$, where $-Q_M$ represents the negative charge on the metal and Q_S is the depletion charge in the semiconductor). The applied voltage is dropped across the insulator and semiconductor, resulting upward band-bending in the insulator and the semiconductor (near the interface), as seen in Fig. 2.1c. As the magnitude of the negative gate bias is increased, the depletion region encroaches further into the semiconductor layer and can eventually deplete the entire layer.

On the other hand, application of a positive gate bias ($V_{GS} > 0$ V) attracts electrons towards the interface, creating an accumulation layer (or channel) near the interface. The associated energy band diagram exhibits downward band-bending in the the insulator and the semiconductor (near the interface), as shown in Fig. 2.1d. Increasing the gate bias modulates the conductivity of the surface layer and is reflected in an increased degree of band bending.

Now that channel formation has been established, application of a positive voltage on the drain attracts electrons towards the drain and accounts for the drain current, I_D. Two bias conditions (small and large V_{DS}) are depicted in Fig. 2.2 using schematic cross-sectional views and energy band diagrams (as viewed from the source to the drain). In the schematic cross-sections, red "-" symbols represent negative mobile charge in the semiconductor (localized positive counterions are not shown here for simplicity). Figure 2.2a depicts the device when biased with significantly low V_{DS}, i.e., the "linear" regime of device operation, where the channel can be modeled as a resistor since I_D increases linearly with respect to V_{DS}. Moreover, Fig. 2.2a specifically depicts *significantly* low V_{DS} ($\sim$100-

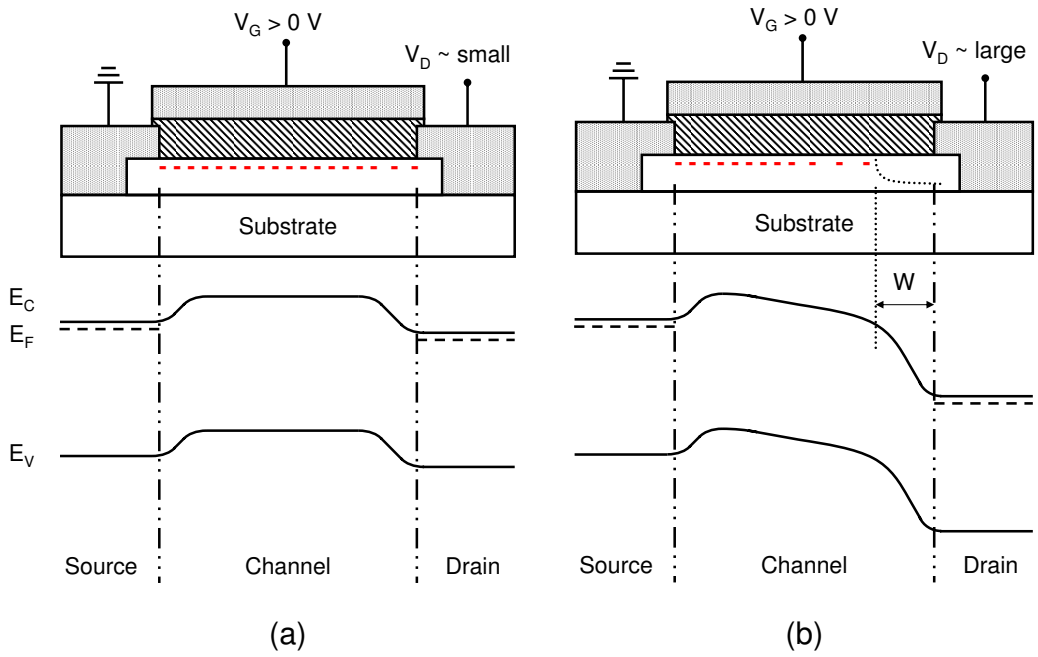


Figure 2.2: Comparison of schematic cross-sections and energy band diagrams for a device with an accumulated channel where the applied V_{DS} is (a) small and (b) large. The depletion width formed with large V_{DS} is labeled as W.

200 mV), so as to maintain a fairly uniform channel charge density across the channel from source to drain. This operation range of V_{DS} is significant since it is typically employed for estimating the channel mobility. Figure 2.2b depicts the device when biased with significantly high V_{DS} to fully deplete the region near the drain. This regime of device operation is referred to as the "saturation" regime since the drain current is constant (with respect to further increases in V_{DS}). Note that the drain voltage at which the region near the drain becomes fully depleted (negating the effect of the surface accumulation layer in this region) is called the pinch-off voltage, $V_{pinch-off}$. For the idealized case under consideration here (where the device turn-on voltage equals zero), $V_{pinch-off} = V_{GS}$;

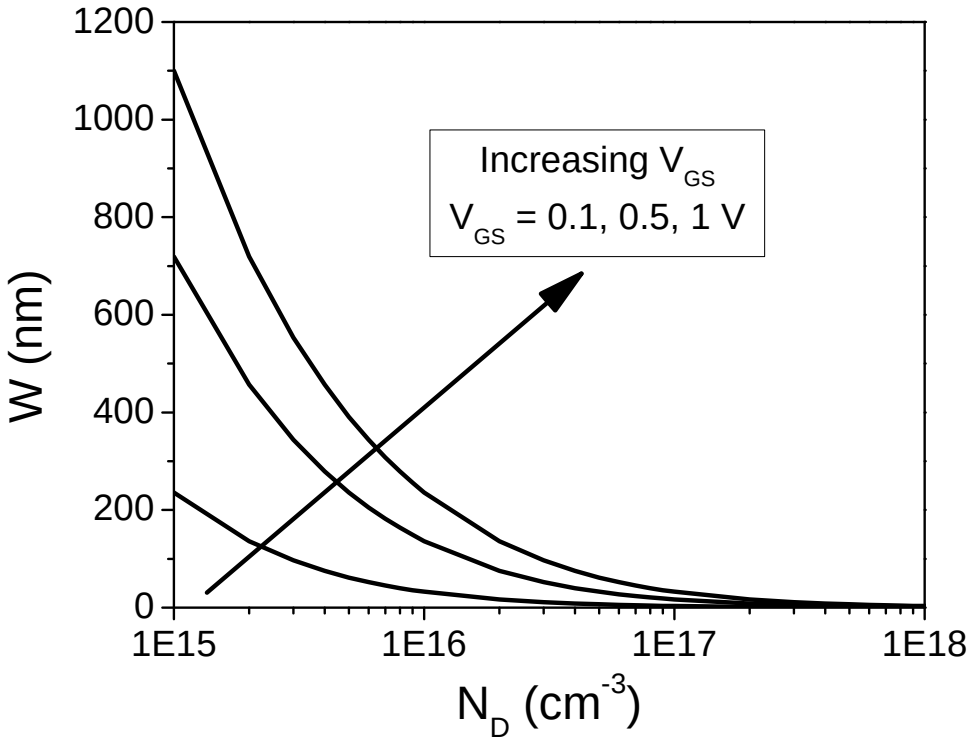


Figure 2.3: Depletion layer width in the semiconductor of a TFT as a function of carrier density for several values of V_G. This estimate of depletion width uses ε_s and C_{ins} of 8.85×10^{-13} F/cm (ε_r =10) and 3.45×10^{-8} F/cm^2 (100 nm SiO_2), respectively.

thus, for $V_{DS} > V_{GS}$, the region near the drain is depleted of carriers and results in this saturated drain current condition.

2.2.1.2 Carrier density in semiconductor layers

As previously mentioned, application of a negative bias to the gate of an n-channel TFT results in depletion of the semiconductor layer. The depletion width has been modeled as [84, 85],

$$W = \frac{\varepsilon_s}{C_{ins}} \left[\left(1 + \frac{2C_{ins}^2 V_g}{qN_D \varepsilon_s} \right)^{1/2} - 1 \right], \tag{2.2}$$

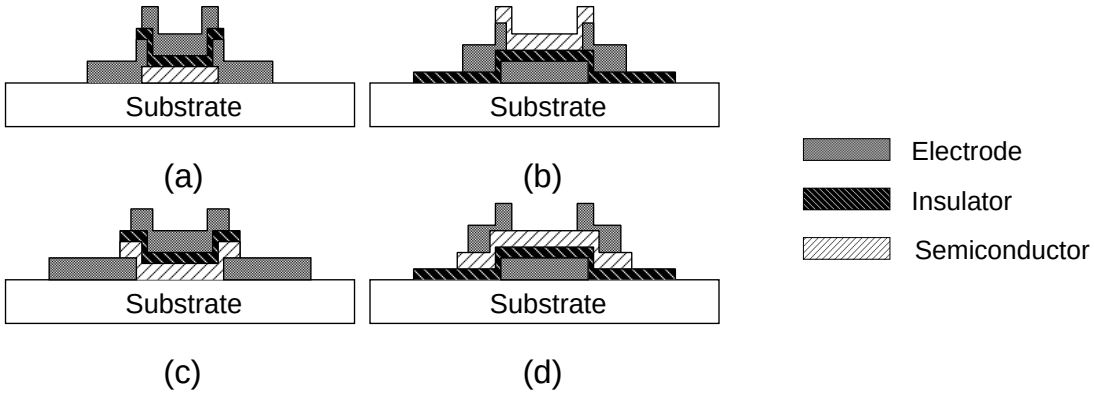


Figure 2.4: Four basic TFT structures: (a) co-planar top-gate, (b) co-planar bottom-gate, (c) staggered top-gate, and (d) staggered bottom-gate.

where C_{ins} is the insulator capacitance per unit area, ε_s is the semiconductor permittivity, and N_D is the semiconductor carrier density. Using Eq. 2.2, the effect of carrier density on depletion width can be evaluated; this effect is shown in Fig. 2.3. Here, the depletion width quickly decreases as the carrier density increases. Since the ability to fully deplete the semiconductor (which is typically $50-300$ nm thick) at reasonable gate biases is desired, Fig. 2.3 indicates that the carrier density in semiconductors should be minimized when fabricating TFTs. Additionally, it should be noted that Eq. 2.2 can be used in an alternative manner. Given an experimental device with a known semiconductor thickness, t_s, Eq. 2.2 can be used to estimate the upper limit of carrier density for proper TFT operation.

2.2.1.3 Thin-film transistor structures

Figure 2.4 shows four basic TFT structures: co-planar top-gate, co-planar bottom-gate, staggered top-gate, and staggered bottom-gate. [86] Electrode placement distinguishes the various structures, i.e. electrodes are placed on opposite sides of the semicon-

ductor-insulator interface for staggered structures, while electrodes are placed on the same side of the interface for the co-planar structures.

Process integration-related issues can motivate the use of different structures. In the co-planar top-gate structure, the semiconductor is deposited first. Therefore, the maximum semiconductor processing temperature is limited only by the semiconductor and the substrate. Notice that in both bottom-gate structures, the insulator is deposited first. If the insulator is deposited using a glow discharge process, such as rf sputtering or plasma-enhanced chemical vapor deposition, the plasma-induced damage to the channel layer can possibly be reduced using this structure (since insulator deposition typically requires the use of a higher power as compared to deposition of other layers).

The co-planar structure is difficult to realize in some technologies, such as a-Si:H. a-Si:H TFTs utilize ion implantation to form an ohmic contact to the semiconductor. Since the maximum processing temperature of a-Si:H transistors is $\sim 350^{\circ}$C, damage from implantation cannot be remedied. This implies that the channel must be protected during implantation. If the insulator is used as an implant-block, there is no source/drain-to-gate overlap. Without this overlap, the series resistance increases and retards carrier injection. [86]

2.2.2 Oxide semiconductor-based thin-film transistors

Since the introduction of oxide semiconductor-based thin-film transistors in 2003, a wide variety of n-type oxide materials have been employed for the semiconductor layer. These materials include several binary oxides (ZnO, SnO_2, and In_2O_3) and several amor-

phous multicomponent oxides (ZTO, zinc indium oxide (ZIO), IGO, and IGZO). The scope of this research includes discrete TFT performance, circuit integration (ring oscillators), and integration with other technologies (e-ink, liquid crystals, and organic light-emitting diodes). The following subsection does not detail each work. Instead, the general properties associated with each oxide semiconductor and the most noteworthy work is highlighted. References are provided for those interested in obtaining additional information.

2.2.2.1 TFTs with binary oxide layers: ZnO

ZnO was the first and most widely employed oxide semiconductor for TFTs, with over 10 institutions publishing reports on its use. [12, 13, 14, 24, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102] These reports employ a variety of deposition techniques for fabrication, including rf sputtering, ion beam sputtering, and pulsed laser deposition (PLD).

The initial reports of ZnO-based TFTs by Masuda *et al*. and Hoffman *et al*. in 2003 demonstrated the prospects for transparent TFTs. These devices were fabricated with different deposition methods (PLD and ion beam sputtering) and utilized fairly high temperature processing (450 - 700 °C). The resultant devices exhibited drain current on-to-off ratios (I_D^{on-off}) up to 10^7 and channel mobilities in the range of 0.01 to 2.5 $cm^2V^{-1}s^{-1}$. Additionally, ambient light had little effect on device performance.

More recently, several authors have explored ZnO-based TFTs with rf sputtering that do not require intentional post-deposition annealing treatments. [88, 92] It is inter-

esting to note that these authors successfully implement drastically different deposition parameters for forming their ZnO layers (high pressure/low power and low pressure/high power for Carcia *et al*. and Fortunato *et al*., respectively). The electrical properties of ZnO-based TFTs are shown to be strongly influenced by the O_2 partial pressure in the deposition ambient; TFTs with mobilities approaching 50 $cm^2V^{-1}s^{-1}$ were demonstrated. Additionally, ZnO-based TFTs on flexible polyimide substrates were also demonstrated. [88]

Two groups have alloyed ZnO with Mg ($Mg_{0.1}Zn_{0.9}O$) to increase the band gap (from $\sim$3.3 to 3.5 eV) and the activation energy of donor states (which leads to a reduction in carrier concentration). Ohtomo *et al*. observed that the increase in band gap results in electrical characteristics which are unresponsive to illumination (for wavelengths greater than 400 nm). The channel mobility and the threshold voltage (V_T) of these devices is $\sim$0.8 $cm^2V^{-1}s^{-1}$ and 10 V, respectively, with a maximum semiconductor layer processing temperature of 300 °C. [101] Kwon *et al*. have doped $Mg_{0.1}Zn_{0.9}O$ with P to further reduce the carrier concentration; the channel mobility and V_T of these devices is $\sim$5 $cm^2V^{-1}s^{-1}$ and $\sim$2.8 V, respectively, when subjected to a 600 °C post-deposition anneal. [102]

Non-vacuum techniques, including spin coating and chemical bath deposition have been employed to fabricate ZnO-based TFTs. [103, 104, 105] The reports using spin-coating employ a high temperature post-deposition anneal to attain adequate crystallization and device performance. Norris *et al*. spin a zinc nitrate precursor solution (zinc nitrate hexahydrate and glycine) and anneal at 700 °C. The channel mobility and I_D^{on-off}

of these devices is $\sim$0.2 cm^{2}V^{-1}s^{-1} and 10^7, respectively. [103] Lee *et al*. incorporate zirconium isopropoxide in their sol-gel precursor to suppress the free carrier density of their films. Spin-coated $Zn_{0.97}Zr_{0.03}O$ TFTs annealed at 500 °C exhibited channel mobilities, V_T, and I_D^{on-off} of $\sim$0.3 cm^{2}V^{-1}s^{-1}, 4.7 V, and 10^6, respectively. [104] Cheng *et al*. utilize a chemical bath containing zinc nitrate and dimethylamineborane at 60 °C to grow ZnO films. TFTs fabricated with these films exhibited channel mobilities and I_D^{on-off} of $\sim$0.25 cm^{2}V^{-1}s^{-1} and 10^5, respectively. [105]

Contributions enhancing the understanding of oxide-based TFT operation have been made by Hossain *et al*. and Hoffman. [24, 87] Hossain *et al*. appraise grain boundary effects (modeled as a two-sided Schottky barrier) for polycrystalline ZnO TFTs. These simulations show a decrease in grain boundary barrier height with increasing free carrier concentration and a decrease in channel mobility as the number of grain boundaries in the channel increases. Hoffman explains the intricacies of mobility extraction and discusses mobility characteristics of ZnO-based TFTs. Understanding mobility extraction is essential to this work and is discussed in detail in Sec. 3.3.7.

Hirao *et al*. and Park *et al*. have utilized ZnO-based TFTs in active-matrix displays. [93, 94] Hirao *et al*. have fabricated AMLCDs with staggered top-gate ZnO TFTs which utilize a SiN_x gate insulator. These TFTs exhibit a channel mobility of $\sim$50 cm^{2}V^{-1}s^{-1}. Park *et al*. have fabricated a transparent AMOLED display with coplanar bottom-gate ZnO TFTs which utilize an Al_2O_3 gate insulator. Additionally, the ZnO deposition process utilized by Park *et al*. is compatible with plastic substrates. These display prototypes

show that ZnO TFTs can be integrated into useful applications and that multiple ZnO TFTs can operate simultaneously.

2.2.2.2 TFTs with binary oxide layers: In_2O_3 and SnO_2

SnO_2 and In_2O_3 are not commonly employed as the TFT semiconductor layer due to difficulty in suppressing/controlling the carrier concentration, which leads to highly negative threshold voltages. To compensate for this, Presley *et al*. utilize extremely thin semiconductor layers (10-20 nm) to control V_T of SnO_2-based TFTs. [106] Wang *et al*. address this issue through the use of ion-assisted deposition, in which the carrier concentration of the layer is controlled (10^{17} to 10^{20} cm^{-3} in In_2O_3 films) by adjusting the O_2 partial pressure and ion beam power. Using this technique, In_2O_3-based TFTs with organic self-assembled dielectrics were fabricated. [107]

2.2.2.3 TFTs with multicomponent oxide layers: ZTO

Zinc tin oxide (ZTO)-based TFTs have been fabricated using a wide variety of methods, including rf sputtering, reactive dc sputtering, and plasma-assisted PLD. [15, 18, 23, 108, 109, 110] The initial ZTO-based TFTs ($ZnSnO_3$) exhibited a channel mobility which approached 30 $cm^2V^{-1}s^{-1}$ when subjected to a 600 °C post-deposition anneal. [15] Since this initial report, researchers have explored the effects of varying ZTO stoichiometry [23, 108], integrated ZTO-based TFTs with transparent OLEDs, and demonstrated flexible TFTs using ZTO.

The effects of stoichiometry and annealing on electrical characteristics of ZTO-based TFTs were explored by Hoffman. [108] Sputter targets of varying stoichiometry

(Zn/(Zn + Sn) = 0.0, 0.33, 0.5, 0.67, and 1.0) were used for fabrication. The intermediate stoichiometries (Zn/(Zn + Sn) = 0.33, 0.5, and 0.67) and post-deposition anneal temperatures (400-600 °C) produced devices with broad peak mobilities (approaching 30 $cm^2V^{-1}s^{-1}$). The turn-on voltage decreases with increasing anneal temperature and decreasing ratios of Zn:Sn (with the inability to deplete any of the SnO_2 devices).

Görrn *et al*. explore the effect of stoichiometry ($0.33 \leq$ Zn/(Zn + Sn) ≤ 0.65) on bias stress stability of ZTO-based TFTs. These devices were fabricated at $250-400$ °C with plasma-assisted PLD. All transistors fabricated in this study exhibited minimal hysteresis and channel mobilities in the range of $5-14$ $cm^2V^{-1}s^{-1}$. A constant voltage bias stress of 10 V is applied for 60 ks; the test is interrupted every 100 s to measure transfer ($I_D - V_{GS}$) characteristics for threshold voltage and mobility extraction. Positive and negative V_T shifts with respect to bias stress time were observed. Positive shifts in V_T were accompanied by rigid shifts in the transfer characteristic, while negative shifts were accompanied by non-rigid shifts in the transfer characteristic and degradation in the subthreshold slope. The relative change in channel mobility during testing for all devices is less than 10% and does not correlate to the behavior of V_T shifts. Zn/(Zn + Sn) = 0.36 resulted in optimal performance; a threshold voltage shift of $\sim$ 30 mV and minimal change in channel mobility is observed for this stoichiometry.

Görrn *et al*. have integrated transparent ZTO-based TFTs with transparent OLEDs as a first step towards a transparent display. [18] For this demonstration, the OLED is fabricated atop the drain (which also serves as the cathode for the OLED) of the staggered bottom-gate ZTO and SU-8 photoresist is used for pixel definition. The ZTO semiconduc-

tor layer is deposited by plasma-assisted PLD, with a maximum processing temperature of 150 °C. The channel mobility and threshold voltage range of these TFTs is 11 $cm^2V^{-1}s^{-1}$ and -1 to 1 V, respectively.

Jackson *et al*. fabricated staggered bottom-gate ZTO-based TFTs on flexible polyimide substrates. [109] These TFTs utilize a 375 nm thick SiON gate insulator. The ZTO semiconductor is subjected to a 250 °C post-deposition anneal for 10 minutes. The channel mobility and threshold voltage are 14 $cm^2V^{-1}s^{-1}$ and -8 V, respectively. The authors identify the threshold voltage and subthreshold slope as the characteristics which require greatest improvement for their devices. The threshold voltage can be shifted towards 0 V by increasing the nitrogen content in the SiON layer or reducing oxygen deficiency in the ZTO layer. The subthreshold slope is degraded by excess carriers (as indicated from capacitance-voltage characteristics) and thus, can be improved by reducing oxygen deficiency in the ZTO layer.

2.2.2.4 TFTs with multicomponent oxide layers: ZIO

Several researchers have explored various stoichiometries of zinc indium oxide (ZIO) by rf sputtering for TFTs. [16, 111, 112, 113] ZIO TFTs typically exhibit high channel mobilities (up to 40 $cm^2V^{-1}s^{-1}$), but suffer from the same issue as In_2O_3 and SnO_2, namely difficulty in suppressing the carrier concentration. As a result, many of the reported ZIO TFTs are "normally on" devices ($I_D > 0$ at $V_{GS} = 0$ V), i.e., depletion-mode devices. It is important to note that V_T is commonly reported and is thus used here for

comparison, but in many cases, significant current still flows below V_T. An alternative figure-of-merit, the turn-on voltage, is discussed in Sec. 3.3.6

The initial report of ZIO-based ($Zn_2In_2O_5$) TFTs employed a staggered bottom-gate structure with an ALD Al_2O_3-TiO_2 superlattice as the gate insulator. [16] Two types of TFTs were reported, those which were subjected to a post-deposition anneal (300 and 600 °C) and "room temperature" TFTs. TFTs subjected to a 300 °C (600 °C) exhibit a channel mobility and V_T in the ranges of $10-30$ $cm^2V^{-1}s^{-1}$ ($45-55$ $cm^2V^{-1}s^{-1}$) and $0-10$ V (-20 to -10 V), respectively. The authors contend that the positive values of V_T observed in devices annealed at 300 °C are a consequence of deep traps present in the channel and/or at the interface (which must be filled by application of a positive gate voltage). TFTs not subjected to a post-deposition anneal exhibit a channel mobility of ~ 8 $cm^2V^{-1}s^{-1}$.

Barquinha *et al*. and Yaglioglu *et al*. utilize room temperature $In_2O_3 - 10$ wt %ZnO (sometimes referred to as IZO) as the semiconductor layer in staggered bottom-gate TFTs. [112, 113] Barquinha *et al*. obtain channel mobilities approaching 40 $cm^2V^{-1}s^{-1}$ while exploring the effect of semiconductor thickness (15 to 65 nm) on device performance. V_T decreases with increasing semiconductor thickness (from 10 to 3 V); this effect is ascribed to reduced sheet resistance for thicker films and a reduced effect from the back surface (opposite to insulator-semiconductor interface), where carrier trapping may be possible. Additionally, the channel mobility decreases with increasing semiconductor thickness (38 to 25 $cm^2V^{-1}s^{-1}$); this is attributed to the longer source-drain path as the semiconductor thickness is increased (recall that a staggered structure is employed). Yaglioglu *et al*.

observe a channel mobility and V_T of $\sim$20 $cm^2V^{-1}s^{-1}$ and -3.2 V, respectively, for their TFTs which employ thermally grown SiO_2 as the gate gate insulator. The carrier density is estimated to be 2.1×10^{17} using a standard van der Pauw setup.

2.2.2.5 TFTs with multicomponent oxide layers: IGO

Indium gallium oxide (IGO)-based TFTs were employed in transparent integrated circuits (inverters and ring oscillators). [19] These TFTs used a 100 nm SiO_x gate insulator deposited by plasma-enhanced chemical vapor deposition (PECVD) and were patterned using standard photolithography techniques. Post-deposition annealing at 500 °C resulted in TFTs with a channel mobility and turn-on voltage (discussed in Sec. 3.3.6) of $\sim$7 $cm^2V^{-1}s^{-1}$ and 2 V, respectively. The maximum oscillation frequency of the ring oscillator circuit is $\sim$9.5 kHz (with 80 V supply voltage). The rather low oscillation frequency is due to loading from large parasitic capacitances associated with each TFT ($\sim$142 nF/cm, 200 μm source/gate and drain/gate overlap). Ring oscillators with a much higher oscillation frequency are discussed in the following subsection.

2.2.2.6 TFTs with multicomponent oxide layers: IGZO

Indium gallium zinc oxide (IGZO)-based TFTs have been fabricated by PLD and rf sputtering. [17, 20, 114, 115, 116] The initial IGZO-based ($InGaO_3(ZnO)_5$) TFTs employed single crystalline IGZO layers which were obtained through the use of a high temperature anneal and yttria-stabilized zirconia substrates. [17] These TFTs employ a coplanar top-gate structure with a 80 nm thick HfO_2 gate insulator. The channel mobility, V_T, and I_D^{on-off} are 80 $cm^2V^{-1}s^{-1}$, 3 V, and 10^6, respectively.

Yabuta *et al*. explore amorphous IGZO-based ($InGaZnO_4$) TFTs with a staggered top-gate structure. [115] rf sputtering is used for deposition of the semiconductor and insulator (Y_2O_3) layers. While no intentional substrate heating is used, the maximum processing temperature is 140 °C due to heating from the sputtering process during insulator deposition. The channel mobility, V_T, and I_D^{on-off} are $\sim$ 12 $cm^2V^{-1}s^{-1}$, 1 V, and 10^8, respectively.

Iwasaki *et al*. explored the IGZO phase space for TFTs (which utilize a staggered bottom-gate structure) using a combinatorial approach with rf co-sputtering from three cathodes. With this experimental setup, the range of compositional variation is $10-70\%$ for each material. [116] Iwasaki *et al*. indicate that the optimal O_2 partial pressure employed during deposition changes for different stoichiometries. A lower O_2 partial pressure is required to produce functioning TFTs (i.e., TFTs that switch from well-defined on to off regions) when the Ga content of films increases. In contrast, a higher O_2 partial pressure is required to produce functioning TFTs when the In content of films increases. In:Ga:Zn ratios of 37:13:50 resulted in the best performance, where the channel mobility, V_T, and I_D^{on-off} are $\sim$ 12 $cm^2V^{-1}s^{-1}$, 3 V, and 10^7, respectively.

Flexible IGZO-based TFTs ($InGaZnO_4$) on 200 μm thick polyethylene terephthalate using a coplanar top-gate structure have been demonstrated by Nomura *et al*. [114] All layers were deposited by PLD at room temperature, including the Y_2O_3 gate insulator. The channel mobility, V_T, and I_D^{on-off} are $\sim$ 8 $cm^2V^{-1}s^{-1}$, 1.6 V, and 10^3, respectively. TFT characteristics were not significantly altered by bending. Additionally, the TFT is stable up to 120 °C.

IGZO-based integrated circuits (inverters and ring oscillators) were demonstrated by Ofugi *et al*. [20] The gate length of these TFTs was 10 μm. Additionally, these TFTs used a 100 nm SiO_x gate insulator deposited by rf sputtering and were patterned using standard photolithography techniques. Discrete TFTs fabricated alongside the integrated circuits exhibited a channel mobility and threshold voltage of $\sim$3 $cm^2V^{-1}s^{-1}$ and 7 V, respectively. The maximum oscillation frequency of the ring oscillator circuit is $\sim$21.5 kHz (with 18 V supply voltage).

2.3 Conclusions

This chapter provides a summary of electrical and optical properties for several n-type TCO semiconductors. The properties of ZTO, IGO, and IGZO are reviewed in more detail, as these materials are of primary interest for this research. A review of qualitative TFT device operation and a summary of structures typically employed for TFT fabrication are also included. Finally, a summary of oxide semiconductor-based TFTs is given, including discrete device performance and examples of integration.

3. DEVICE DEVELOPMENT, FABRICATION, AND CHARACTERIZATION

This chapter presents an overview of TFT development. Thin-film processing techniques relevant to the fabrication of TFTs, including evaporation, sputtering, atomic layer deposition, and post-deposition annealing, are briefly discussed. Next, thin-film characterization techniques are discussed, including, Hall and optical transmission measurements. Finally, TFT characterization, including threshold voltage and channel mobility extraction from DC $I-V$ measurements is discussed.

3.1 Thin film processing

Numerous thin film deposition techniques are available for the fabrication of electronic devices based on oxide semiconductor. The commonality between these techniques is the goal of forming a high-quality thin-film (in terms of optical, electrical, and mechanical properties) onto the desired substrate. However, the details of the source material, material transport mechanisms (from source to substrate), and thin film formation differ for each technique. Within these differences, distinct advantages and disadvantages arise.

Processes which interact with the substrate to form a film (e.g., thermal oxidation) are not commonly employed for the fabrication of integrated oxide semiconductor devices, as the substrate typically acts only as a carrier and does not contribute to device functionality. The thin film deposition techniques relevant to the fabrication of oxide semiconductors are discussed below. These techniques can be separated into two cate-

gories: vacuum and non-vacuum techniques. Vacuum techniques are performed in a controlled chamber and/or pressure. Thus, films fabricated with vacuum techniques generally have a lower impurity concentration than those fabricated with non-vacuum techniques. Examples of vacuum techniques include evaporation, sputtering, and chemical vapor deposition. The benefit of non-vacuum techniques is minimal capital equipment investment. From this perspective, non-vacuum techniques are generally considered to be low cost. From a manufacturing viewpoint, the cost benefit may be reduced, as many non-vacuum processes can require extended curing cycles, which would reduce throughput. Examples of non-vacuum techniques are spin-coating and printing.

Patterning of thin films can be accomplished via shadow masks or photolithography. Basic photolithography techniques relevant to the fabrication of oxide semiconductor devices are also discussed.

3.1.1 Vacuum deposition techniques

Vacuum techniques can be further subcategorized into physical vapor deposition (PVD) and chemical vapor deposition (CVD). In PVD techniques, atoms or molecules are *physically* removed from a source material. They are then transported through vacuum and condense onto the substrate to form a thin film. CVD techniques utilize gas-phase chemicals that are transported to the substrate and react to form a thin film.

In these processes, the pressure affects the extent of impurity incorporation in growing thin films and transport of atoms from the source to substrate. [117] Atoms undergo a larger number of collisions as the pressure in the chamber is increased. The mean free

path (λ) is the average distance an atom travels between collisions and is inversely proportional to pressure,

$$\lambda = \frac{1}{\sqrt{2}\pi d_o^2 n} \rightarrow \frac{0.05}{P}, \tag{3.1}$$

where d_o is the atomic diameter and n is the gas concentration. The simplification of Eq. 3.1 is obtained assuming that the ambient is air at 300 K and P is pressure (Torr); this results in the mean free path expressed in millimeters.

3.1.1.1 Evaporation

Evaporation is a basic thin film deposition technique which involves heating of a source material such that the vapor pressure (i.e. the equilibrium pressure created by the rate difference of condensed molecules evaporating and vaporized molecules condensing) is greater than 10 mTorr. [118, 119] To increase the mean free path of vaporized molecules and reduce the amount of contamination incorporated in the thin-film during deposition, this heating process is typically performed under high vacuum ($<5 \times 10^{-6}$ Torr).

Since the vapor pressure varies for different chemical elements, stoichiometric compounds and alloys can be difficult to fabricate by evaporation. Compensation for this variation can be accomplished by modifying the source material or by using multiple evaporation sources. The complexity of a multicomponent evaporation process is further increased if the differing sticking coefficients of the deposited adatoms are considered.

3.1.1.2 Thermal evaporation

In thermal evaporation, a source material is placed in a refractory crucible, boat, or wire basket and heated using an electric current. A crucible composed of an insulating

material, such as Al_2O_3, is indirectly heated by placing it in (or on) a conductive element. In contrast, boats and wire baskets (which are often made of W or Mo) are directly heated. Extremely refractory materials cannot be evaporated thermally for multiple reasons: there is a limit to the amount of current that can be sourced, possible cross-contamination from the boat/basket, and possible physical damage to the boat/basket from overheating. For these materials, electron beam evaporation is a possible solution.

3.1.1.3 Electron beam evaporation (EBE)

Electron beam evaporation (EBE) utilizes a high energy (5-30 keV) electron beam to heat a source material, which is normally a compressed pellet that has been sintered at high temperature. [119] One requirement for EBE is that the source material be a poor conductor of heat; the beam cannot supply enough energy to offset the heat loss of a source material which is a good conductor of heat. Alternatively, the hearth/pocket which the source sits upon may be insulated when EBE is used to deposit materials that are good conductors of heat. One of the drawbacks for EBE is possible x-ray damage to the deposited thin-film from the electron beam.

3.1.1.4 Sputtering

Sputtering is the primary deposition method utilized in this work, and is thus given more attention than the previously summarized methods. Sputtering provides good thickness uniformity and controllability for deposition over a wide range of substrate types and sizes. Additionally, compositional control with sputtering is better than evaporation

since the sputter yield of materials typically varies less than the vapor pressure. For these reasons, sputtering is frequently utilized in semiconductor manufacturing. [117]

Sputtering is a process which uses high energy particles (usually inert gas ions) to remove surface atoms from a source material (sputter target). To accomplish this, sputtering is performed in a vacuum chamber with a controlled ambient. After backfilling the vacuum chamber with gas (typically an inert gas), an electric field is applied between two electrodes within the chamber. Electrons (which may have been created by a passing cosmic ray) present in the chamber are accelerated towards the anode (usually ground) and collide with gas atoms. Depending on the amount of energy transferred during the collision, excitation or ionization may occur. Excited gas atoms release their excess energy with a photon, creating what is known as a ”glow discharge”. Ionization creates the species (positive ions) required for sputtering and increases the number of available electrons. These electrons are immediately accelerated through the electric field, increasing the likelihood of further ionization and leading to gas breakdown. Additionally, ions are accelerated towards the negative cathode. The sequence of events that occur as ions impinge at the cathode (target) is depicted in Fig. 3.1. As ions impinge at the cathode, secondary electrons are emitted; these secondary electrons sustain the glow discharge and neutralize the bombarding ions. Ions within a particular energy range (10 eV $<$ E $<$ 10 keV) remove surface atoms from the sputter target for deposition. [117]

The most important region of the discharge is the Crooke’s dark space, which forms directly in front of the target. In this region, a high ion concentration (positive space charge) is present due attraction of ions (which are larger and slower than electrons) and

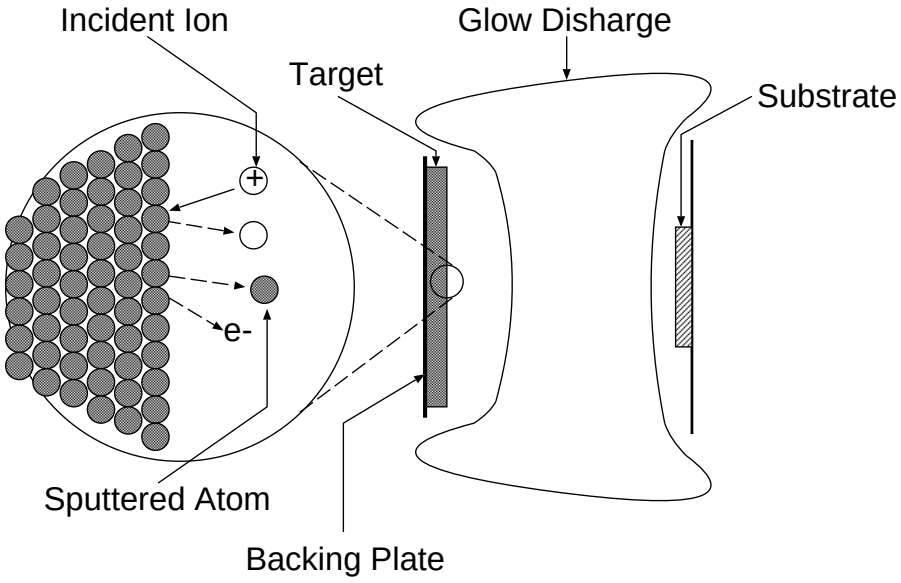


Figure 3.1: Depiction of the sputtering process.

repulsion of electrons away from the negative cathode. Consequently, a strong electric field is established in front of the target and a large portion of the voltage is dropped in this region. Moreover, the established electric field initiates sufficient ion acceleration required for sputtering.

There are multiple configurations employed in sputtering. The simplest configuration, DC-diode sputtering, utilizes a DC voltage to create the glow discharge. However, DC sputtering is limited to conductive targets that can sufficiently supply the target surface with secondary electrons. Positive charge buildup occurs when sputtering an insulating target with a DC source; this charge buildup extinguishes the glow discharge.

To circumvent charge buildup on insulating target surfaces, a high frequency ac power source can be used. A radio-frequency (rf) of 13.56 MHz is typically employed

to strike and sustain a glow discharge. During the negative portion of the applied signal, positive ions are attracted towards the target. During the positive portion of the applied signal, electrons are attracted towards the target and replenish lost secondary electrons. Additionally, since electrons are much lighter than ions, a negative dc self-bias is established on the target, establishing the electric field required for sputtering. It should be noted that the surface to be sputtered should be significantly smaller than other surfaces within the chamber. With this in mind, the chamber in most rf sputtering systems is connected to the anode.

In practice, magnetron sputtering is commonly encountered. A magnetic field is created by placing strong magnets behind the target. The established magnetic field confines electrons near the target surface (rather than allowing the electrons to be collected by the anode) and increases the possibility of ionization. The benefits of magnetron sputtering include higher deposition rates and the ability to maintain a stable glow discharge at lower pressures ($\sim$1 mTorr). However, these benefits do come at the cost of preferential target erosion (i.e., poor target utilization).

Reactive sputtering can be employed by flowing a reactive gas (solely or in combination with an inert gas) during the sputter deposition process. For example, when sputtering an oxide target, reactive sputtering in an oxygen-containing ambient is a possible approach. This is especially attractive for deposition of TFT channel layers, as the oxygen partial pressure of the sputter ambient strongly influences device performance. However, sputtering with oxygen increases the likelihood of negative ion resputtering. Due to the high electronegativity of oxygen, the probability of forming negative ions dur-

ing the sputtering process is increased. These negative ions are accelerated towards the substrate and can potentially resputter atoms from the growing thin film. [120]

The OSU solid state processing lab is outfitted with two magnetron sputtering systems: a modified Control Process Apparatus, Inc. (CPA) sputtering system [121] and a custom-designed sputtering system [122]. Both DC and rf power supplies are available for use with these systems.

3.1.1.5 Ion beam sputtering

Ion beam sputtering utilizes essentially the same deposition mechanisms as in the previously discussed sputter deposition processes, with one primary difference: the ions are created in a separate chamber and extracted. [32, 123] In the previous sputtering configurations, a potential difference between the sputter cathode/anode to ignite a glow discharge. With ion beam sputtering, a filament is heated, causing the emission of electrons, while the chamber is positively biased. The electrons are accelerated by the bias to excite/ionize gas atoms. Ions from this DC discharge plasma are extracted using an accelerating grid assembly and subsequently strike the sputter target to initiate the sputtering process. Since the source is external to the sputter target, insulators can be deposited with ion beam sputtering despite the fact DC discharge employed.

The OSU processing facility houses a modified Veeco Microetch System. The system accommodates 3” wafers and is equipped with an AC motor that is utilized for substrate rotation. Three 6” sputter targets can be simultaneously mounted. The combination

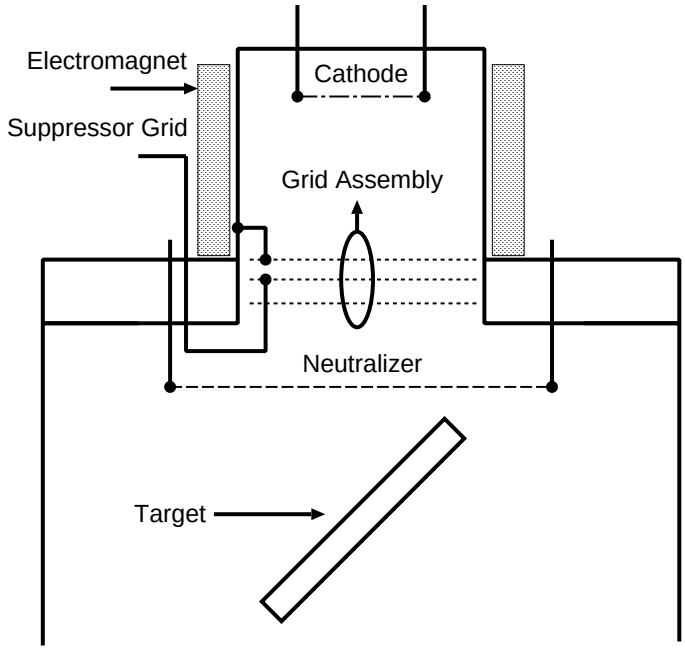


Figure 3.2: Schematic representation of the ion beam sputtering system.

of a large sputter source and rotation capability results in excellent uniformity of deposited thin-films. One drawback of this system is the lack of a substrate heater.

As shown in Fig. 3.2, ions are created using a Kaufman ion source mounted atop the deposition chamber. [123] A thoriated tungsten hot filament (cathode) is used as the electron source and the cylindrical chamber, which is made of molybdenum, acts as the anode. A feedback-controlled leak valve is used for introduction of the gas used to ignite and sustain a glow discharge. In addition, a solenoidal electromagnet surrounds the chamber and deflects electrons into cycloidal trajectories, increasing the likelihood of ionization before being collected.

Before proceeding, a few notes on the thoriated tungsten filament are required. Thorium is utilized to lower the work function of the tungsten filament, increasing electron

emission when heated. [124] However, thorium is a radioactive material which emits alpha particles; health hazards and precautions are discussed elsewhere. [125, 126]

A collimated multi-grid assembly is used for ion extraction and acceleration. The top grid is biased at the same voltage as the ion source assembly, i.e. 2 kV. The middle grid is biased at -200V to -250V, accelerating ions towards the deposition chamber and preventing a backflow of electrons from the deposition chamber. Sapphire spheres electrically isolate the grids. Over time, it is possible for a film to build up on the sapphire spheres and short the grids to each other. When this occurs, it is recommended that the entire grid assembly be removed and chemically cleaned.

Ions entering the deposition chamber have the same charge polarity, repelling each other. Thus, an electron-emitting tungsten neutralizer filament is used to "focus" the beam onto the target. In addition, the neutralizer filament eliminates any charge build-up on the target surface, allowing insulating targets to be sputtered.

3.1.1.6 Plasma-enhanced chemical vapor deposition (PECVD)

Chemical vapor deposition (CVD) techniques employ gas-phase sources (rather than solid sources as employed in PVD) to form a thin film. [117] After the gas-phase precursors are introduced into the chamber, they are transported (by diffusion) to the substrate, where a reaction that results in thin film formation occurs. This reaction can be driven in a variety of ways, including (but not limited to) thermally, by photons, or by glow discharge. Plasma-enhanced chemical vapor deposition (PECVD) utilizes both a glow discharge and heat to drive the thin film-forming reaction. Use of a glow discharge

allows for reduced processing temperatures compared to conventional CVD. In this work, PECVD is utilized to deposit SiO_2 for use as a gate insulator.

3.1.1.7 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a powerful deposition technique that produces films with excellent step coverage and few pin-hole defects. [127] The main difference between previously discussed thin film deposition techniques (i.e. evaporation and sputtering) and ALD is the growth mechanism. In the previously discussed techniques, thin film growth is dominated by nucleation, thus forming microcrystals, whereas ALD is a self-controlled process, resulting in the sequential growth of monolayers or submonolayers.

Execution of the ALD process involves anionic and cationic precursor gases which are separately introduced into the deposition chamber. [128] The cationic species is first introduced so that several monolayers are adsorbed onto the substrate surface. An inert gas then purges the surface, causing desorption of weakly bound adatoms and, ideally, retention of a single saturated monolayer of film growth. Next, an anionic species is introduced and reacts with the adsorbed cationic precursor at the substrate surface. A subsequent anion purge completes the sequence. This alternating cycle is repeated until the appropriate film thickness is achieved. Note that saturated monolayer growth does not always occur. Additionally, the alternating ALD cycle can be appropriately modified to accomplish doping or alternate atomic engineering of the deposited layer.

3.1.2 Non-vacuum deposition techniques

The advantage of employing non-vacuum techniques is reduced capital equipment costs and reduced deposition time in some cases (since no vacuum pump down time is required). Two vacuum techniques are briefly highlighted below: spin-coating and printing. These methods will likely become more prevalent in oxide semiconductors research.

Spin-coating utilizes a liquid precursor containing the desired chemical constituents for thin film deposition. The precursor is dropped atop a (preferably) hydrophillic substrate surface (stationary or already spinning) for deposition. The substrate is then spun (generally at 1-5000 rpm) to disperse the liquid over the entire substrate. This process may be repeated several times to obtain the desired thickness. The liquid is then dehydrated, typically by heating, to form the thin film. The dehydration process drives out any solvents (or other undesired constituents) which may have been used in the precursor and (ideally) improves the structural properties of the forming film. Variations of the above steps are often employed. For example, heating can be utilized between "coats" and after the entire stack is complete. Spin-coating has been used for fabrication of ZnO TTFTs by Norris *et al*. [103]

The capital equipment costs required for printing of devices and circuits are typically higher than spin-coating. However, printing is a "direct-write" process, so (expensive) photolithographic techniques would not be required for patterning. Printing techniques typically are suitable for applications that do not require a high level of resolution. Several types of printing, including ink jet printing [129], screen printing [130], and mi-

crocontact printing [131, 132] have already been employed for fabrication of organic electronics. There are sparse reports of inorganic transistors produced by printing. [133]

3.1.3 Thin film patterning techniques

Patterning of thin films is critical to device integration; the techniques relevant to the fabrication of devices for this work are shadow mask patterning, photolithography, and lift-off. Of these techniques, shadow mask patterning is the simplest. Shadow mask patterning utilizes a physical mask that is placed in the path of incoming atoms during deposition to create a pattern. While this technique is frequently used for the fabrication of devices in this work, the resolution can be limited. Resolution can be improved through the use of photolithography or lift-off, which are discussed below. [117]

3.1.3.1 Photolithography

Photolithography is a process that transfers a pattern onto another surface using ultraviolet (UV) light. The basic steps employed in photolithography are as follows. First, photoresist (a light sensitive material used to form the pattern) is deposited atop a thin film or substrate. The resist is then exposed to UV light through a mask, which contains transparent and opaque regions. The photoresist is then submerged in developer to define the pattern. Post processing (etching, ion implantation, etc.) can now be applied selectively to regions without photoresist. It should be noted that two bake steps, a soft bake and a post-exposure bake, are also required. The soft bake follows photoresist deposition and is employed to drive out solvents and dehydrate the film. The post-exposure bake is

employed to promote diffusion of photoactive components (discussed below) in the resist; this reduces ridges in the photoresist sidewalls.

Conventional photoresists contain three components: resin, a photoactive component, and solvent. Of particular interest is the photoactive component, as its operation determines the photoresist type (positive or negative). In a positive photoresist, the photoactive component decomposes when exposed to UV light; areas exposed to UV light become soluble in developer. In a negative photoresist, the photoactive component cross-links when exposed to UV light; areas exposed to UV light become insoluble in developer.

Details of the photolithography process are constantly changing, as critical dimensions for some modern Si processes are smaller than 100 nm. The usage of negative photoresists has been limited to low resolution processes due to swelling of the resist during development. Additionally, the wavelength of the UV light has shifted from 436 nm (g-line), to 365 nm (i-line), and to $\leq$ 248 nm (deep UV).

3.1.3.2 Lift-off patterning

Lift-off patterning is commonly employed in research when an etch process is not available or when selectivity between layers of a device is poor. For lift-off, the photoresist is first deposited and patterned. The thin film is then deposited atop the photoresist and substrate. The substrate is then submerged in a solvent to remove the resist, leaving a patterned film. Since photoresist is present during thin film deposition, lift-off is limited to low-temperature processes. Additionally, a bi-layer lift-off process is employed in some cases. The bi-layer process employs a lift-off resist and an imaging resist. During

development, the lift-off resist undercuts the imaging resist. This improves resolution of lift-off processing to $\sim$0.25 μm. Lift-off is employed for patterning of ITO in the fabrication of transparent circuits. [19]

3.1.4 Post-deposition annealing

Post-deposition annealing is often employed to obtain the desired properties of thin films. For example, post-deposition annealing of TCOs in an inert ambient often increases the conductivity. This is not surprising, as oxygen vacancies are a possible source of intrinsic donor defects in ZnO, In_2O_3:Sn, Zn_2SnO_4, and other TCOs. For TTFTs, post-deposition annealing of the channel layer strongly influences the turn-on voltage and mobility of a device. The effects of post-deposition annealing will be discussed in Ch. 4.

Devices fabricated for this work are annealed using either an AET Thermal, Inc. rapid thermal processing (RTP) system, Barnstead Thermolyne 62700 box furnace, or a Neytech QEX furnace. In the RTP system, the substrate is placed in a quartz chamber that is backfilled with a process gas using MFC's. Substrate heating is accomplished through the use of halogen bulbs externally mounted on the top and bottom of the chamber. Water and compressed dry air are used for cooling. Typical ramp rates are on the order of 10°C/sec, resulting in high throughput of fabricated devices. Although the RTP system is fully programmable, the box furnace is typically used when a lower ramp rate or longer soak time is required.

3.2 Thin film characterization

Two essential thin film characterization techniques are Hall and optical transmission measurements. Hall measurements can be used to determine majority carrier type and concentration, conductivity, and Hall mobility. Optical transmission measurements can be used to determine the band gap and transition type.

3.2.1 Hall measurement

The Hall effect, discovered in 1879, can be used to determine the resistivity, carrier type and concentration, and mobility of a sample. [134, 135] The Hall effect is based on the Lorentz force,

$$F = q(\overrightarrow{v} \text{ x } \overrightarrow{B}), \tag{3.2}$$

where q denotes the charge of the particle, $\overrightarrow{v}$ the velocity vector, and $\overrightarrow{B}$ the magnetic field vector. The Lorentz force deflects carriers (the direction of deflection is determined by the right-hand rule) towards the top or bottom of the sample, creating a potential known as the Hall voltage, V_H. The Hall voltage is defined as,

$$V_H = \frac{BI}{qtn}, \tag{3.3}$$

where I is the current, t is the thickness of the sample and n is the carrier concentration. In addition, one can define the Hall coefficient, R_H,

$$R_H = \frac{tV_H}{BI}. \tag{3.4}$$

Note that the sign of the Hall coefficient indicates dominant carrier type; a negative Hall coefficient indicates that electrons are the dominant carriers. [134, 135]

After determining the Hall coefficient, the carrier concentration, n, is given by,

$$n = -\frac{1}{qR_H}. \tag{3.5}$$

To determine the Hall mobility, the film resistivity is first assessed using,

$$\rho = \frac{\pi t}{\ln(2)} \frac{R_{12,34} + R_{23,41}}{2}. \tag{3.6}$$

The two resistances in Eq. 3.6 can be generalized as $R_{ab,cd}$ and are measured by forcing a current from contact a to b, then measuring the voltage between terminals d and c. Note that the contacts are defined in a clockwise fashion around the perimeter of the sample. Finally, the Hall mobility, μ_H, is obtained using,

$$\mu_H = \frac{R_H}{\rho}. \tag{3.7}$$

Note that the Hall mobility is related to the conductivity mobility for electrons (or holes) via

$$\mu_H = r\mu_{n(p)}, \tag{3.8}$$

where r, the scattering factor, and is defined as,

$$r = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2}. \tag{3.9}$$

τ is the mean time between scattering events. r is typically between 1 and 2. Specifically, r is 1.18 for lattice scattering and 1.93 for impurity scattering. [134]

For measurements conducted at OSU, a symmetric lamella-type van der Pauw structure is used. [134] When using this structure, terminals to the sample should be small and close to the sample edges. Sample and contact symmetry is not required, but

in practice is preferred. If these conditions are not met, appropriate corrections must be made.

3.2.2 Optical transmission

When an incoming photon with energy,

$$E_{ph} = h\nu, \tag{3.10}$$

is absorbed, it can interact with one of four types of carriers: inner shell electrons, valence electrons, free carriers, or electrons trapped by localized impurities and other defects. [32, 136, 137] The fundamental absorption process, which can be used to analyze band gap and transition type (allowed direct, forbidden direct, allowed indirect, and forbidden indirect), occurs when a valence electron is promoted to a higher energy state (e.g. conduction band). Due to competing absorption processes as well as quantum mechanical selection rules that need to be accounted for, there is a degree of uncertainty when fitting data to one of the four transition types.

The first step in analyzing the band gap is to measure the optical transmittance and reflectance across the appropriate wavelength spectrum. From this data, the absorption coefficient, α, can be determined.

$$\alpha = \frac{1}{t} \ln\left(\frac{1}{1-A}\right), \tag{3.11}$$

where t is the thickness and A is the optical absorptance of the film. If the optical reflectance is assumed to be constant over the portion of the spectrum in consideration,

$$A \propto 1 - T, \tag{3.12}$$

otherwise

$$A = 1 - T - R, \tag{3.13}$$

where T and R are the optical transmittance and reflectance, respectively. Although incorrect α values are obtained when using Eq. 3.12, this does not introduce additional error to extrapolation of the band gap.

Considering an energy-momentum ($E - k$) diagram, if the valence band maximum and conduction band minimum are located at the same point in k-space (e.g. $k = 0 = \Gamma$ in GaAs), the band gap is direct. If the conduction band minimum and valence band maximum are offset in k-space, the band gap is indirect (e.g. Si). Quantum selection rules determine the probability of an electron transition and determine whether the transition is allowed or forbidden. For forbidden transitions, selection rules forbid transitions at Γ, but allow transitions at $k \neq 0$ with the probability increasing as a function of k^2.

For allowed direct transitions between parabolic bands,

$$\alpha \propto (h\nu - E_g)^{1/2}, \tag{3.14}$$

where h is Planck's constant, ν is the frequency, and E_g is the band gap. For forbidden direct transitions between parabolic bands,

$$\alpha \propto (h\nu - E_g)^{3/2}. \tag{3.15}$$

To conserve momentum in indirect transitions between parabolic bands, phonon (lattice vibration) emission or absorption must accompany photon absorption. For al-

lowed indirect transitions,

$$\alpha = \alpha_a(h\nu) + \alpha_e(h\nu) \tag{3.16a}$$

$$\propto \frac{(h\nu - (E_g - E_p))^2}{exp\left(\frac{E_p}{kT}\right) - 1} + \frac{(h\nu - (E_g + E_p))^2}{1 - exp\left(-\frac{E_p}{kT}\right)}, \tag{3.16b}$$

where E_p is the phonon energy, k is the Boltzmann constant, and T is the temperature. It is apparent from Eq. 3.16b that temperature determines the dominant process. At high temperature, α is dominated by the phonon absorption process and can be approximated to,

$$\alpha \simeq \alpha_a \propto (h\nu - (E_g - E_p))^2. \tag{3.17}$$

At low temperature, α is phonon emission dominated,

$$\alpha \simeq \alpha_e \propto (h\nu - (E_g + E_p))^2. \tag{3.18}$$

For forbidden indirect transitions between parabolic bands,

$$\alpha \propto \frac{(h\nu - (E_g - E_p))^3}{exp\left(\frac{E_p}{kT}\right) - 1} + \frac{(h\nu - (E_g + E_p))^3}{1 - exp\left(-\frac{E_p}{kT}\right)}. \tag{3.19}$$

Similar to allowed indirect transitions, forbidden transitions between parabolic bands are temperature-dependent and can be simplified. At high temperature,

$$\alpha \simeq \alpha_a \propto (h\nu - (E_g - E_p))^3. \tag{3.20}$$

At low temperature,

$$\alpha \simeq \alpha_e \propto (h\nu - (E_g + E_p))^3. \tag{3.21}$$

Assuming that $E_p \ll E_g$ allows E_p to be neglected when extrapolating the band gap energy.

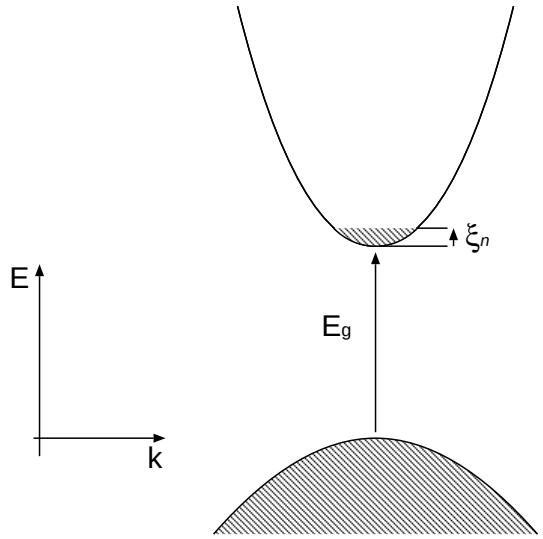


Figure 3.3: Band structure of a degenerately doped direct band gap semiconductor, illustrating the origin of the Burstein-Moss shift with the hatched area distinguishing filled states.

By plotting $(\alpha)^n$ vs $h\nu$ (where n is 2, 2/3, 1/2 or 1/3 for allowed direct, forbidden direct, allowed indirect, or forbidden indirect transitions, respectively), the transition type and band gap can be estimated. The transition type is determined by the linearity of the fit near the absorption edge. The band gap is determined by extrapolating $(\alpha)^n$ back to the x-axis ($h\nu$). However, there may be multiple competing absorption processes, making this method of band gap analysis indefinite.

3.2.2.1 Burstein-Moss shift

For degenerately doped semiconductors, it is possible for the absorption edge to shift to higher energies; this shift, which was independently discovered by Burstein and Moss in InSb, is known as the Burstein-Moss shift. [138, 139, 140] Considering a direct

band gap semiconductor,

$$\alpha \propto (h\nu - E_g - \xi_n)^{1/2}, \tag{3.22}$$

where ξ_n represents the depth the Fermi level is within the conduction band, as shown in Fig. 3.3. Note that the degree of shifting due to the Burstein-Moss phenomenon gives qualitative information on band curvature and the density of states effective mass since,

$$m^* = \frac{1}{\frac{1}{\hbar^2}\frac{d^2E}{dk^2}}, \tag{3.23}$$

where E is the electron kinetic energy, $\hbar$ is Dirac's constant, and k is the wave vector. A large Burstein-Moss shift indicates a large slope in the conduction band concomitant with a small effective mass.

3.2.2.2 Considerations for amorphous materials

The electronic states (density of states) of an amorphous semiconductor are considerably modified from that of a crystalline semiconductor. [141] Figure 3.4 compares the density of states, $N(E)$ as a function of energy, E, for crystalline and amorphous semiconductors. The most noteworthy differences between the two cases are tailing of $N(E)$ into the gap, smearing of band edges, and the presence of broad defect bands (as opposed to discrete trap levels) in the amorphous case. The mobility gap in the amorphous case plays an analogous role to the band gap in the crystalline case, where the (mobility) edges are demarkations between extended and localized states. [142]

Consequently, the optical absorption characteristic for amorphous semiconductors is less abrupt than that of crystalline semiconductors. As shown in Fig. 3.5, three regions of absorption are typically observed in amorphous semiconductors are shown: the strong

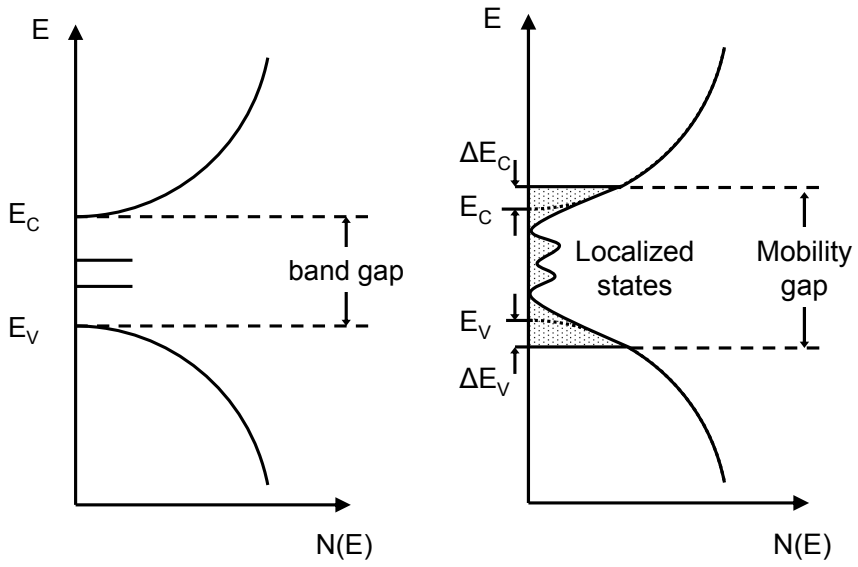


Figure 3.4: Exemplary density of states, $N(E)$ as a function of energy, E characteristics for (a) crystalline and (b) amorphous semiconductors. The lines within the band gap of the crystalline case represent discrete trap levels. The dotted area and $\Delta E_C/\Delta E_V$ in the amorphous case represent localized states and band tailing, respectively.

absorption (or interband) region (A), the exponential (or Urbach) region (B), which extends over several orders of magnitude , and the weak absorption tail (region C). [143] Note that the demarkation between regions A and B corresponds to the mobility gap. [144]

In the strong absorption region, the absorption coefficient follows the form,

$$E\alpha \propto (E - E_o)^n, \tag{3.24}$$

where E_o is the optical gap and n is a constant that is usually equal to 2 or 3. While E_o does not have a clear physical meaning, empirically determining E_o with Eq. 3.24 can be useful for comparing a series of samples with varying fabrication conditions. The constant n is equal to 2 when assuming a parabolic density of states distribution near

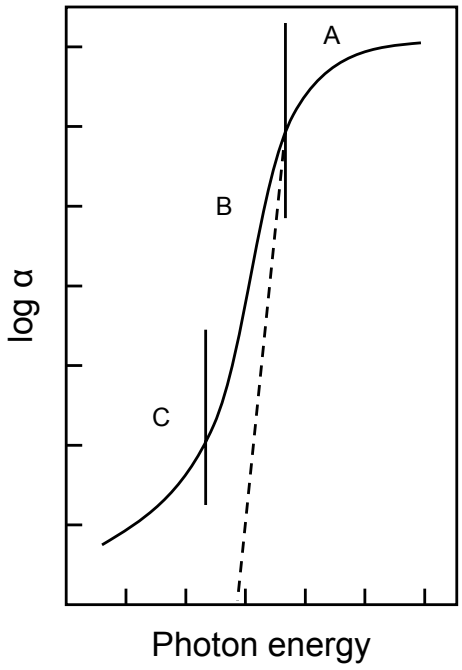


Figure 3.5: Schematic of the absorption coefficient as a function of photon energy for amorphous semiconductors. The three regions, A, B, and C, correspond to the strong absorption edge, Urbach region, and weak absorption region, respectively.

the band edge. [143] While the assumption of a parabolic distribution is appropriate for extended states, this assumption may be questionable for localized states near the band edges in some cases. In those cases, assuming a linear density of states distribution may be more appropriate and results in $n = 3$. [141]

In the exponential region, absorption primarily involves band tails. Here, the absorption coefficient follows the form,

$$\alpha \propto e^{E/E_u}, \tag{3.25}$$

where E_u is the Urbach energy, which corresponds to the width of band tails. The Urbach energy can be shifted by charged defect states and lattice vibrations.

In the weak absorption region, absorption primarily involves defect states within the mobility gap and follows an exponential form, given as,

$$\alpha \propto e^{E/E_t}, \tag{3.26}$$

where E_t is a trap energy. As the slope in this region will always be smaller than in the Urbach region, E_t is always larger than E_u. Experimentally, this region is difficult to study due to the low absorption levels. Thus, many references do not include this region in the absorption characteristic.

3.3 Thin-film transistor characterization

Methodologies for extracting several TFT figures-of-merit including the subthreshold swing, threshold voltage, drain current on-to-off ratio, turn-on voltage, and channel mobility are discussed below. While the channel mobility is most often used for device comparison, each figure-of-merit describes a specific characteristic of device performance. Moreover, each figure-of-merit, including the channel mobility, has unique shortcomings. Thus, it is imperative to consider a compilation of these figures-of-merit when assessing device performance.

3.3.1 Thin-film transistor operation

Analysis of semiconductor devices typically begins with an energy band diagram assessment. Figure 3.6 shows equilibrium energy band diagrams through the channel of a bottom-gate, n-channel, accumulation-mode TFT, composed of Al (the work function, Φ_m, is 4.1 eV [145]) - Al_2O_3 (E_g = 9.5 eV [146, 147, 148]) - ZnO (E_g = 3.2 eV [36]).

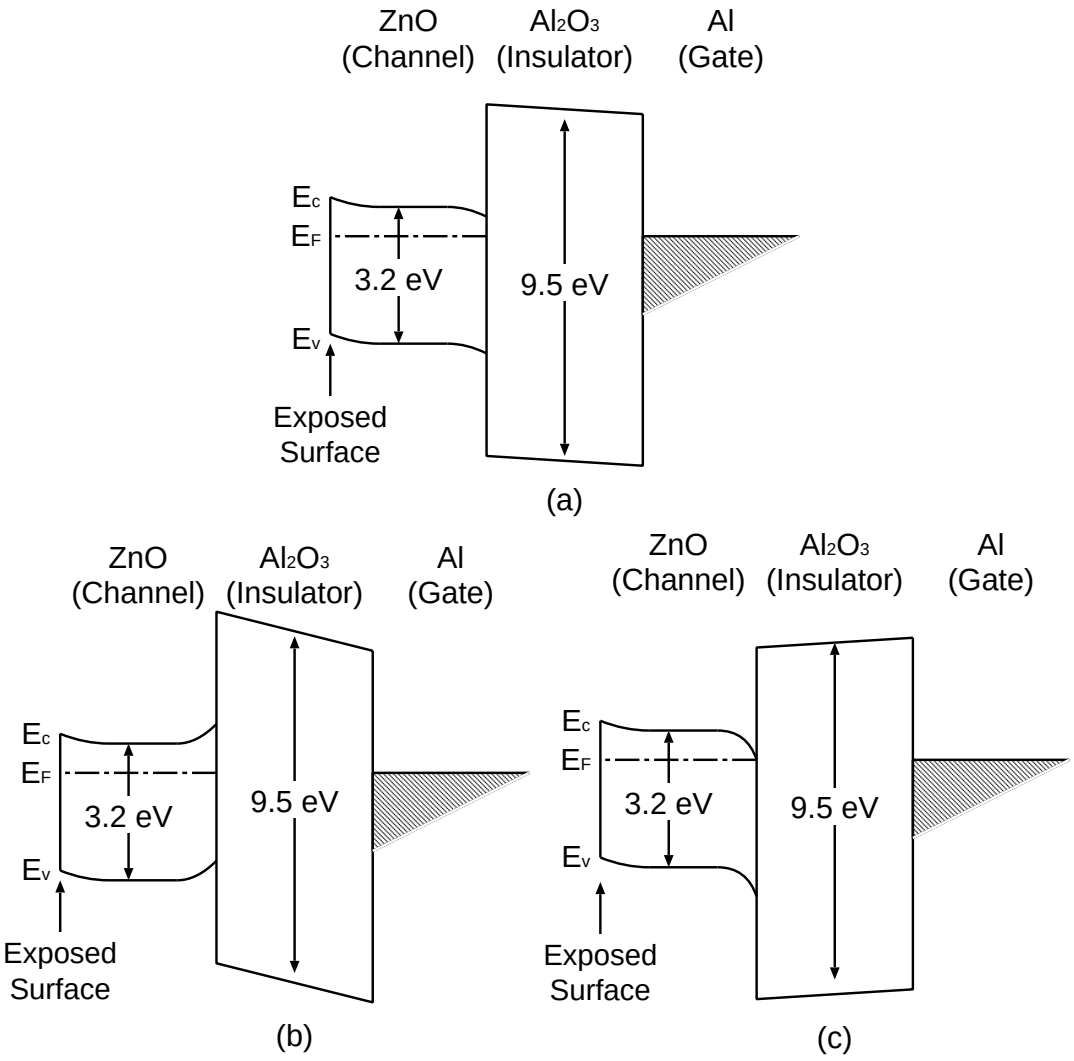


Figure 3.6: Equilibrium energy band diagram for several cases: (a) interface states are neglected, (b) acceptor-like interface states are considered, and (c) donor-like interface states are considered.

This particular structure is chosen for its similarity to the TTFTs fabricated in this thesis research. The three band diagrams shown illustrate various conditions; (a) interface states are neglected, (b) acceptor-like interface states are considered, and (c) donor-like interface states are considered. Revisiting Fig. 2.1b, the equilibrium energy band diagram shown in Fig. 3.6a differs due to consideration of the metal-semiconductor work function (the work function is the difference between the vacuum level and Fermi level) difference, which is negative for the materials shown in this case, resulting in an accumulation layer near the semiconductor-insulator interface. As seen for all three cases, there is upward band-bending of the exposed ZnO surface; this is due to acceptor-like surface states concomitant with the chemisorption of oxygen. [149, 150]

The TFTs fabricated for this thesis have many similarities with conventional MOSFETs, but there are also several differences. TFTs are fabricated on insulating substrates (which is advantageous for device isolation) rather than conductive silicon substrates as with MOSFETs. In addition, the fabricated TFTs utilize an amorphous or polycrystalline thin-film channel and are accumulation-mode rather than single-crystal, inversion-mode devices.

As TFTs and MOSFETs are both field-effect devices, classic MOSFET drain current equations are typically employed for TFT assessment. The MOSFET equations for both the triode and saturation regions of operation are shown here for convenience,

$$I_D = \mu C_{ins} \frac{W}{L} [(V_{GS} - V_T) - \frac{V_{DS}^2}{2}] \rightarrow \text{Triode: } V_{DS} \leq V_{GS} - V_T \tag{3.27a}$$

$$I_D = \frac{1}{2} \mu C_{ins} \frac{W}{L} (V_{GS} - V_T)^2 \rightarrow \text{Saturation: } V_{DS} > V_{GS} - V_T. \tag{3.27b}$$

However, the application of Eq. 3.27 for TFT assessment may be inappropriate, due to several subtleties in the device characteristics. The following equations are better suited for TFT assessment,

$$I_D = \mu(V_{GS})C_{ins}\frac{W}{L}[(V_{GS}-V_{on})-\frac{V_{DS}^2}{2}] \rightarrow \text{Triode: } V_{DS} \leq V_{GS}-V_{on} \tag{3.28a}$$

$$I_D = \frac{1}{2}\mu(V_{GS})C_{ins}\frac{W}{L}(V_{GS}-V_{on})^2 \rightarrow \text{Saturation: } V_{DS} > V_{GS}-V_{on}. \tag{3.28b}$$

Two differences are apparent between Eqs. 3.27 and 3.28. First, the channel mobility has been modified. Eq. 3.27 assumes that the mobility is constant as the gate field is varied; while this assumption is reasonable for MOSFETs, it does not apply to a variety of TFT technologies (including organic and wide band gap TFTs). Second, V_T is replaced by the turn-on voltage of the device, V_{on}. V_T is an ill-defined parameter for TFTs (and even for MOSFETs in some sense), as its assessment is quite subjective. These changes and details of the device channel mobility, V_T, and V_{on} are discussed in the following subsections.

3.3.2 DC current-voltage measurements

DC current-voltage characteristics presented in this section and throughout this work are obtained using an Hewlett Packard 4156B Precision Semiconductor Parameter Analyzer; measurements are executed in the dark unless otherwise stated. The default testing parameters are a “hold time” of 500 ms, a “delay time” of 200 ms, and “Medium” integration time. Devices are contacted using a BNC-based Micromanipulators probe station.

Bias stress testing results are obtained using the same test setup.

3.3.3 DC current-voltage measurements: Output characteristics

$I_D - V_{DS}$ or output characteristics provide qualitative information regarding the device under test. Saturation in these characteristics indicate that the channel layer can be fully depleted of carriers for the applied bias voltages used. Additionally, the low-V_{DS} region can be analyzed for significant deviations from linearity, which may be an indication of substantial contact resistance.

3.3.4 DC current-voltage measurements: Transfer characteristics

$I_D - V_{GS}$ or transfer characteristics provide quantitative information regarding the device under test. Extraction of several electrical parameters is discussed below, including the subthreshold swing, drain current on-to-off ratio, threshold voltage, turn-on voltage, and channel mobility.

3.3.5 Transfer characteristics: Subthreshold swing extraction and drain current on-to-off ratio

The subthreshold swing (S) and drain current on-to-off ratio (I_D^{on-off}) are estimated using a semi-log plot of the transfer characteristic taken at high V_{DS}. S is the inverse of maximum slope in the transfer characteristic,

$$S = \left(\frac{d\log(I_D)}{dV_{GS}}\bigg|_{max} \right)^{-1}. \tag{3.29}$$

S can be a useful quantification of how efficiently the devices turns on and is typically less than 1. For the device shown in Fig. 3.7, $S \sim$0.34 V/dec. I_D^{on-off} is a parameter for

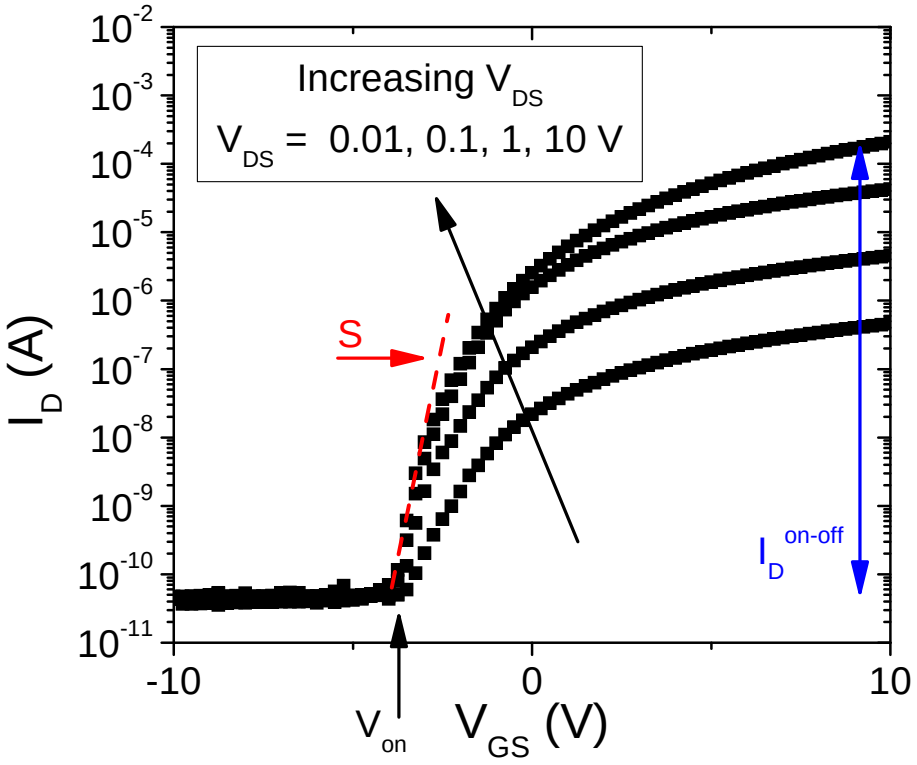


Figure 3.7: Log$(I_D) - V_{GS}$ characteristics where V_{DS} is varied as a geometric progression (0.01, 0.1, 1, 10 V) for subthreshold swing, drain current on-to-off ratio, and turn-on voltage extraction of a staggered bottom-gate ZTO-channel layer TFT.

switching applications and provides a useful measure of device performance, as I_D^{on-off} is directly affected by gate leakage. I_D^{on-off} is simply the ratio of the on-current to off-current (for the V_{DS} = 10 V measurement), as shown in Fig. 3.7. For this device, $I_D^{on-off} > 10^7$.

3.3.6 Transfer characteristics: Threshold voltage extraction and the turn-on voltage

Typically, V_T is considered to be a unique device parameter. In actuality, V_T is a rather ambiguous quantity. [134] The ambiguity arises from multiple sources. First, V_T

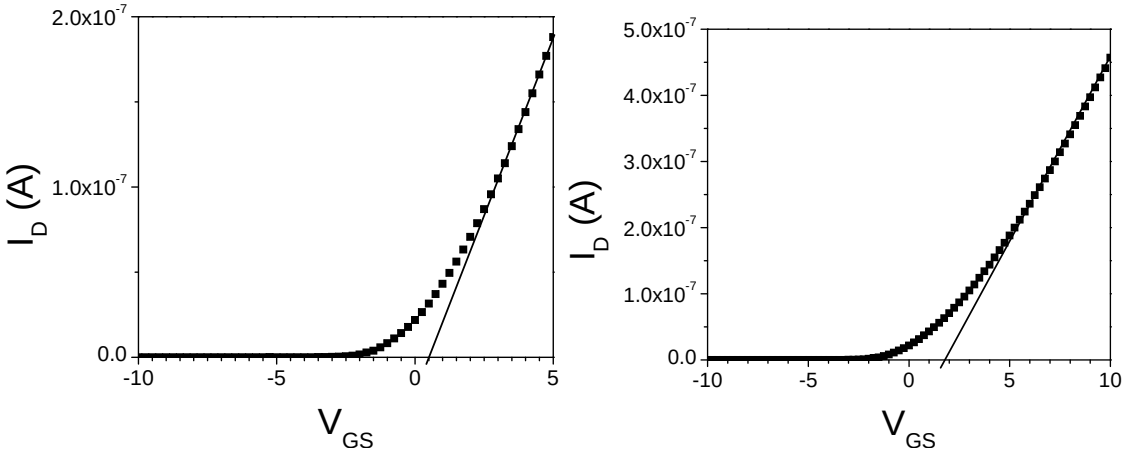


Figure 3.8: Determination of the threshold voltage using V_{DS} = 100 mV for a a staggered bottom-gate ZTO-channel layer TFT. The threshold voltage is extracted using two different V_{GS} ranges: (a) -10 $\leq V_{GS} \leq$ 5 V and (b)-10 $\leq V_{GS} \leq$ 10 V.

can be extracted using several methods, including extrapolation of the $I_D - V_{GS}$ curve (when biased in triode) or extrapolation of the $\sqrt{I_D} - V_{GS}$ curve (when biased in saturation). Additionally, extrapolation of curves can be quite subjective. Figs. 3.8(a) and (b) show $I_D - V_{GS}$ curves with V_{DS} = 100 mV for the same device at two different zoom levels (i.e., different V_{GS} ranges). The extrapolated value of V_T is $\sim$ 0.5 and 1.8 V for Figs. 3.8(a) and (b), respectively. This difference in V_T underscores the subjective nature of extrapolation for obtaining quantitative device parameters.

With this in mind, an analogous figure-of-merit, denoted the turn-on voltage, V_{on}, is used extensively in this work. Revisiting Fig. 3.7, V_{on} is determined by plotting $\log(I_D) - V_{GS}$. The gate voltage at the onset of conduction (distinguished by a sharp increase in current) establishes V_{on}. [151] V_{on} is attractive for several reasons: ambiguous model fitting (i.e., extrapolation) is not required, V_{on} identifies the lower range of device operation, and

as shown in Fig. 3.7, V_{on} is independent of drain voltage (as long as $V_{DS} >$ a few k_BT/q). In practice, anomalous subthreshold current characteristics, possibly due to a displacement or gate leakage current, are sometimes seen for low V_{DS}, so $V_{DS} > 5$ V is typically used when determining V_{on}.

3.3.6.1 Additional considerations for V_{on}

V_{on} is influenced by a number of factors, including the gate-semiconductor work function difference (ϕ_{cs}), the free volumetric carrier density before application of a gate bias (n_0, which is assumed to be uniform across the semiconductor layer), and the trap density (at the interface and/or within the semiconductor).

Of particular interest for oxide semiconductor-based TFTs is n_0, as it is highly controllable and is the dominant factor for determining V_{on} in many cases. The goal when fabricating a TFT is to minimize n_0 while maintaining the quality of the channel layer. This becomes clear as we consider N_{max}, the maximum sheet carrier density which can be injected or extracted due to the field effect prior to insulator breakdown . N_{max} is determined from analysis of the charge neutrality relationship, $Q_M = Q_S$, at the point of insulator breakdown, where Q_M is the charge density on the metal (or contact) and Q_S is the charge density in the semiconductor. Thus, N_{max} is defined as,

$$N_{max} = \frac{Q_{S-max}}{q} = \frac{V_{ins-max} \cdot C_{ins}}{q} = \frac{F_{BD} t_{ins}}{q} \cdot \frac{\varepsilon_r \varepsilon_0}{t_{ins}} = \frac{F_{BD} \varepsilon_r \varepsilon_0}{q}, \tag{3.30}$$

where F_{BD} is the insulator breakdown field, t_{ins} is the insulator thickness, ε_r is the insulator relative dielectric constant, and ε_0 is the permittivity of free space.

Now, consider the ratio of N_{max} to N_0, denoted here as the field-effect modulation ratio,

$$\beta = \frac{N_{max}}{n_0 t_s}, \tag{3.31}$$

where t_s is the thickness of the semiconductor. In cases where β is less than 1, the insulator cannot sufficiently extract the carriers already present in the semiconductor in order to fully deplete it. In other words, when β is less than 1, the insulator would break down before the device is "turned off".

It may be useful to evaluate β for several hypothetical cases. Thus, N_{max} and several other parameters for various dielectric materials are given in Table 3.1. Unless otherwise stated, E_g is obtained from Strehlow *et al*. [146] ε_r and F_{BD} are taken from Ono, [152] and χ, the electron affinity, is obtained from Peacock *et al*. [147]

With N_{max} specified, β can now be determined. In the case of oxide semiconductors, deposition parameters can vary the carrier concentration drastically; this variation can be in the range of 10^{15} to 10^{21} cm^{-3}. Assuming a semiconductor thickness of 100 nm and that the device is integrated with an Al_2O_3 gate insulator (n_{max} = 2.66 $\times$ 10^{13} cm^{-2}), β is $\sim$ 2.7 $\times$ 10^4 and 2.7 $\times$ 10^{-3} at the lower and upper carrier concentration boundaries, respectively. In the case of the upper carrier concentration boundary, the insulator cannot deplete the semiconductor before dielectric breakdown; this highlights the need to minimize n_0.

Table 3.1: Properties of various dielectric materials, including E_g, the band gap, ε_r, the relative dielectric constant, F_{BD} the breakdown field, and χ, the electron affinity. Note that * indicates values which are estimated.

Insulator	E_g (eV)	ε_r	F_{BD} (MV/cm)	χ (eV)	N_{max} (10^{13} cm^{-2})
Al_2O_3	9.5	8	3.5-6	1*	1.55 - 2.66
$BaTa_2O_6$		22	3.5		4.26
HfO_2	5.8 [147]	16	0.17-4 [118]	2.5	0.15 - 3.54
SiO_2	11	4	6	0.9	1.33
Ta_2O_5	4.6	23-25	1.5-3	3.2	1.91 - 4.15
TiO_2	3.75	60	0.2	3.9 [153]	0.66
Y_2O_3	5.6	12	3-5	2*	1.99 - 3.32
ZrO_2	5	19.8 [154]		2.5	

3.3.7 Transfer characteristics: Mobility extraction

The channel mobility of a field-effect transistor (FET) is the average mobility of carriers transported in the channel and results from consideration of all applicable scattering mechanisms (phonon, ionized impurity, and interface roughness), according to Mathiessen's rule. [155, 134] As the channel mobility quantifies the current drive capability and maximum switching frequency of a FET, accurate extraction and assessment is vital.

While the channel mobility is a useful figure-of-merit for device comparison, there are several complications. Similar to V_T estimation, there are multiple ways to extract the

channel mobility, all resulting in slightly different values. Additionally, the gate leakage current is (typically) not accounted for, and can affect the extracted value.

The classic (and most commonly encountered) methods for determining the channel mobility utilize MOSFET drain current equations. The effective mobility, μ_{eff}, and the field-effect mobility, μ_{FE}, are both determined from an assessment of the linear portion of the triode region of device operation (below pinch-off), while the saturation mobility, μ_{sat}, is established from the saturation region (above pinch-off). As these methods are commonly encountered, they are summarized in the following subsection.

Application of the classic mobility estimation techniques to the assessment of TFTs can be questioned. Hoffman has recently introduced two additional estimates of mobility, namely the average mobility, μ_{avg}, and incremental mobility, μ_{inc}.[87] For TFTs, these mobility estimates are preferred and are thus used extensively throughout this work. A short description of these mobility estimates are given in Sec. 3.3.7.2.

3.3.7.1 Mobility extraction: μ_{eff}, μ_{FE}, and μ_{sat}

The below pinch-off drain current relationship can be described and approximated as, [134, 156]

$$I_D = \mu\frac{Z}{L}Q_nV_{DS} - \mu Z\frac{kT}{q}\frac{dQ_n}{dx}, \tag{3.32a}$$

$$\simeq \mu\frac{Z}{L}Q_nV_{DS}, \tag{3.32b}$$

where Q_n is the mobile channel charge density, Z is the gate width, and L is the gate length. To directly determine Q_n, a measurement of the gate-to-channel capacitance as a function of gate voltage is required. Alternatively, it is often useful to obtain a first order

approximation of Q_n from electrostatics,

$$Q_n = C_{ins}(V_{GS} - V_T). \tag{3.33}$$

The approximation shown in Eq. 3.32b is obtained by assuming a uniform channel charge density. When biasing at low V_{DS} (50 - 100 mV), this assumption is reasonable and allows the second term of Eq. 3.32a, which is related to carrier diffusion, to be neglected. However, neglecting this diffusion-related term does introduce some error in mobility determination. Specifically, when biasing a MOSFET in the subthreshold regime (i.e. $V_{GS} < V_T$) and near the threshold voltage, a significant diffusion current flows and the approximation in Eq. 3.32b deteriorates. Thus, mobility assessment in these regions results in significant error. However, at gate voltages appreciably larger than V_T ($V_{GS} > V_T + 0.5$ V), the error is less than 10%. [134]

Differentiating Eq. 3.32b with respect to V_{DS} or V_{GS} determines the channel conductance, g_d, or transconductance, g_m, respectively. In practice, large-signal equivalents of g_d and g_m are commonly employed, as they can easily be estimated from typical DC $I_D - V_{DS}$ measurements (given that reasonable gate and drain voltage steps are used). The small- and large-signal channel conductance and transconductance are related as follows,

$$g_d = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}=Constant} \rightarrow G_D = \frac{\Delta I_D}{\Delta V_{DS}}\Big|_{V_{GS}=Constant}, \tag{3.34}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=Constant} \rightarrow G_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=Constant}, \tag{3.35}$$

where Δ in this and the following expressions refers to taking differences between discrete data points as a means of accomplishing differentiation of a discrete data set.

Using the derivative Eq. 3.32b and g_d (G_d) or g_m (G_m) determines the effective mobility or field-effect mobility, respectively.

$$\mu_{eff} = \frac{g_d}{\frac{Z}{L}Q_n} = \frac{G_d}{C_{ins}\frac{Z}{L}(V_{GS} - V_T)}, \tag{3.36}$$

$$\mu_{FE} = \frac{g_m}{\frac{Z}{L}\frac{\partial Q_n}{\partial V_{GS}}} = \frac{G_m}{C_{ins}\frac{Z}{L}V_{DS}}. \tag{3.37}$$

Note that assessment of μ_{eff} requires a value for V_T, in contrast to μ_{FE}, which is not explicitly dependent on V_T.

The channel mobility is sometimes estimated from the above pinch-off drain current relationship; mobility estimates from this region of device operation are denoted as, μ_{sat}. One method of extracting μ_{sat} is to connect the drain to the gate and measure I_{DSAT}. This biasing configuration is only applicable if the device under test is enhancement-mode (i.e. $V_T > 0$). Square law theory asserts that the above pinch-off drain current is given by,

$$I_{DSAT} = C_i \mu_{sat} \frac{Z}{2L}(V_{GS} - V_T)^2. \tag{3.38}$$

μ_{sat} is extracted using,

$$\mu_{sat} = \left(\frac{d\sqrt{I_{DSAT}}}{dV_{GS}} \sqrt{\frac{1}{C_i \frac{Z}{2L}}} \right)^2. \tag{3.39}$$

The approach taken to determine μ_{sat} is to take the square root of Eq. 3.38 and then differentiate with respect to V_{GS}. This methodology alleviates the need to evaluate V_T and reveals that μ_{sat} is determined from the slope of the $\sqrt{I_{DSAT}}$ vs. V_{GS} characteristic.

Comparing the mobility determination methods discussed above, μ_{eff} is preferred for several reasons. μ_{sat} is an inaccurate assessment of the "channel" mobility, as it is an average of the mobility in the channel and the mobility in the pinched-off region of the

channel. In practice, it is suggested that μ_{sat} only be employed when the gate leakage current significantly affects below pinch-off current characteristics. With respect to μ_{FE}, it has been shown by Kang *et al*. [157] that field-effect mobility data can be extracted from μ_{eff}. In addition, μ_{FE} is viewed as unreliable; when μ_{FE} is used in the fundamental FET equation to generate a simulated $I_D - V_{DS}$ curve, the simulated curve does not accurately fit the original experimental $I_D - V_{DS}$ characteristic. The source of this inaccuracy has been attributed to exclusion of the gate dependence in the determination of μ_{FE}. [157] Although μ_{FE} is not preferred, it is still useful since there is less ambiguity in its determination due to the fact that a value for V_T is not required.

Figure 3.9 shows exemplary $\mu - V_{GS}$ characteristics for the three mobility estimation techniques (μ_{eff}, μ_{FE}, and μ_{sat}) discussed in this section. μ_{eff} is determined using Eq. 3.36, where G_d is calculated using $V_{DS} = 0.1$ V and $V_T = 10.5$ V. μ_{FE} is determined using Eq. 3.37, where $V_{DS} = 0.1$ V. μ_{sat} is calculated using Eq. 3.39. It should be noted that the μ_{eff} characteristic shows an anomalously large value near V_T, which should be neglected, as it is not representative of device performance. Rather, it is an artifact associated with the singularity present in Eq. 3.36 when $V_{GS} = V_T$.

Considering the μ_{FE} characteristic in Fig. 3.9, the mobility initially increases with increasing gate voltage and then saturates. The initial increase may be due to an increasing ratio of free to trapped charge with increasing gate voltage, i.e. at lower gate voltages, the mobility is possibly trap-limited. [151]

In some cases, a decrease in mobility is observed at high values of V_{GS}. This decrease may be caused by several effects. At higher gate voltages, carriers are drawn

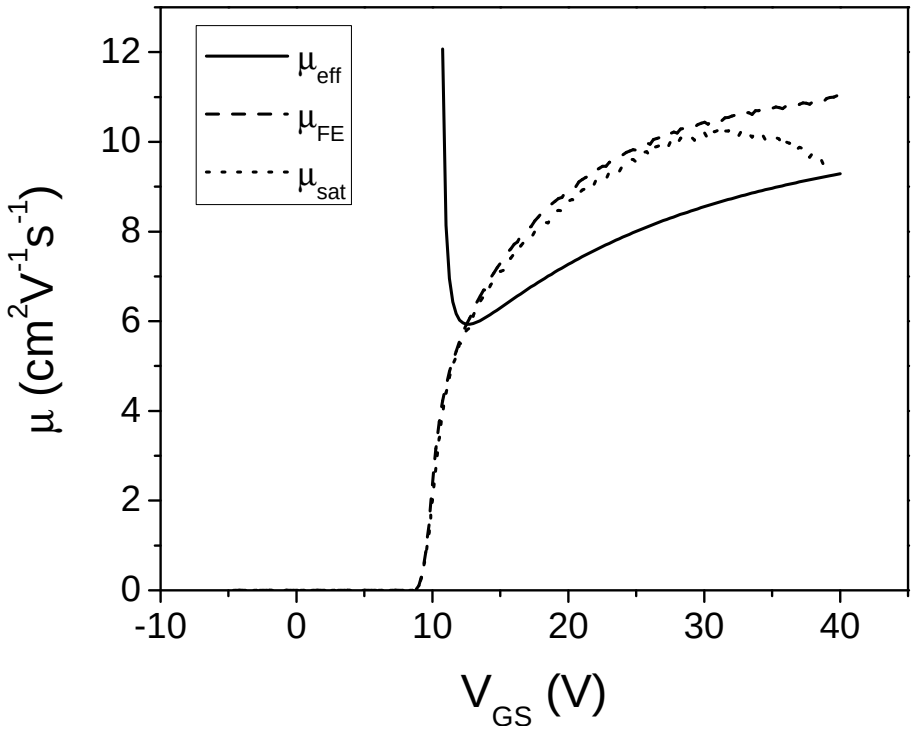


Figure 3.9: Summary of mobility determination methods for a staggered bottom-gate IGZO-channel layer TFT. For this device, V_{on} and V_T are 8.75 and 10.5 V, respectively. μ_{eff} and μ_{FE} are determined using V_{DS} = 0.1 V and Eqs. 3.36 and 3.37, respectively. μ_{SAT} is determined using V_{DS} = 30 V and Eq. 3.39. Note that the μ_{sat} characteristic is only shown for the portion of V_{GS} where the device is in the saturation regime of device operation, i.e., $V_{GS} < V_{DS} + V_{on} = 38.75$ V.

closer to the oxide-semiconductor interface and the mobility degrades due to enhanced Coulombic scattering, which arises from interface states, and interface roughness scattering. [134] The mobility decrease may also be due in part to increasing contact resistance effects with increasing gate voltage. [151]

3.3.7.2 Modified mobility extraction: μ_{avg} and μ_{inc}

The general premises of Hoffman's mobility extraction methodology are the use of basic charge transport theory (assuming drift-dominated transport) and including the

gate voltage dependence of mobility (which is significant for many TFT technologies). A short summary of Hoffman's derivation is given here. [87]

Assuming drift-dominated transport, the channel conductance can be defined as,

$$G_d(V_{GS}) = \mu_{avg}(V_{GS})\frac{Z}{L}Q_n(V_{GS}). \tag{3.40}$$

Note that G_d, μ_{avg} (the average mobility), and Q_n are all a function of V_{GS}. Additionally, note that although the large-signal channel conductance is employed here, the small-signal equivalent could be substituted.. As discussed in Sec. 3.3.7.1, Q_n can be determined by measurement of the gate-to-channel capacitance or approximated from electrostatics. Here, Q_n is approximated slightly differently than in Sec. 3.3.7.1 as,

$$Q_n(V_{GS}) = C_{ins}(V_{GS} - V_{on}). \tag{3.41}$$

Equation 3.40 can be rearranged and combined with Eq. 3.40 to determine μ_{avg},

$$\mu_{avg}(V_{GS}) = \frac{g_d}{\frac{Z}{L}Q_n} = \frac{G_d}{C_{ins}\frac{Z}{L}(V_{GS} - V_{on})}. \tag{3.42}$$

The left portion of Eq. 3.42 is identical to μ_{eff}. However, the approximation of Q_n for μ_{avg} replaces V_T with V_{on}; this eliminates the previously discussed ambiguity inherent to V_T. However, the use of V_{on} results in the inclusion of the subthreshold regime ($V_{GS} < V_T$) for analysis. In cases where the subthreshold regime is dominated by diffusion current (e.g., MOSFETs), the use of V_{on} introduces additional (undesired) uncertainty to the mobility extraction. For TFTs, the contribution from diffusion current in the subthreshold regime is likely minimal (so long as V_{DS} is approaching 0 V) and thus, significant error is not introduced in the mobility extraction.

Another mobility estimate, the incremental mobility (μ_{inc}), is derived here,

$$\Delta Q_n(V_{GS}) = C_{ins}\Delta V_{GS}, \tag{3.43a}$$

$$\Delta G_d = \mu_{inc}(V_{GS})\frac{Z}{L}\Delta Q_n(V_{GS}), \tag{3.43b}$$

$$\mu_{inc}(V_{GS}) = \frac{\frac{\Delta G_d}{\Delta V_{GS}}}{\frac{Z}{L}C_{ins}} = \frac{G'_d(V_{GS})}{C_{ins}\frac{Z}{L}}. \tag{3.43c}$$

For this derivation, the incrementally induced channel charge ($\Delta Q_n(V_{GS})$) is first assessed. Then, a corollary of Eq. 3.40 is used to determine the differential channel conductance. Finally, these equations are combined and rearranged to obtain μ_{inc}. Before proceeding, it is important to note that the validity of Eq. 3.43b is contingent upon the assumption that the mobility of carriers already present in the channel does not change as additional charge is induced.

μ_{avg} and μ_{inc} characteristics as a function of V_{GS} are shown in Fig. 3.10. Comparing these mobility estimates, μ_{avg} is of greater practical significance, as it estimates the mobility of all carriers in the channel and is more useful for quantifying device performance. On the other hand, μ_{inc} is of greater physical significance, as it estimates the mobility of incrementally induced carriers with changing gate voltage and is more useful for understanding device performance.

3.3.7.3 Additional comments for mobility extraction

All (five) of the above channel mobility estimates will be encountered when researching TFTs. While μ_{eff}, μ_{FE}, and μ_{sat} are most commonly encountered, this work will employ μ_{avg} and μ_{inc} for estimating channel mobility. These estimates are preferred, as their derivation does not utilize idealized transistor models (which are more suited to

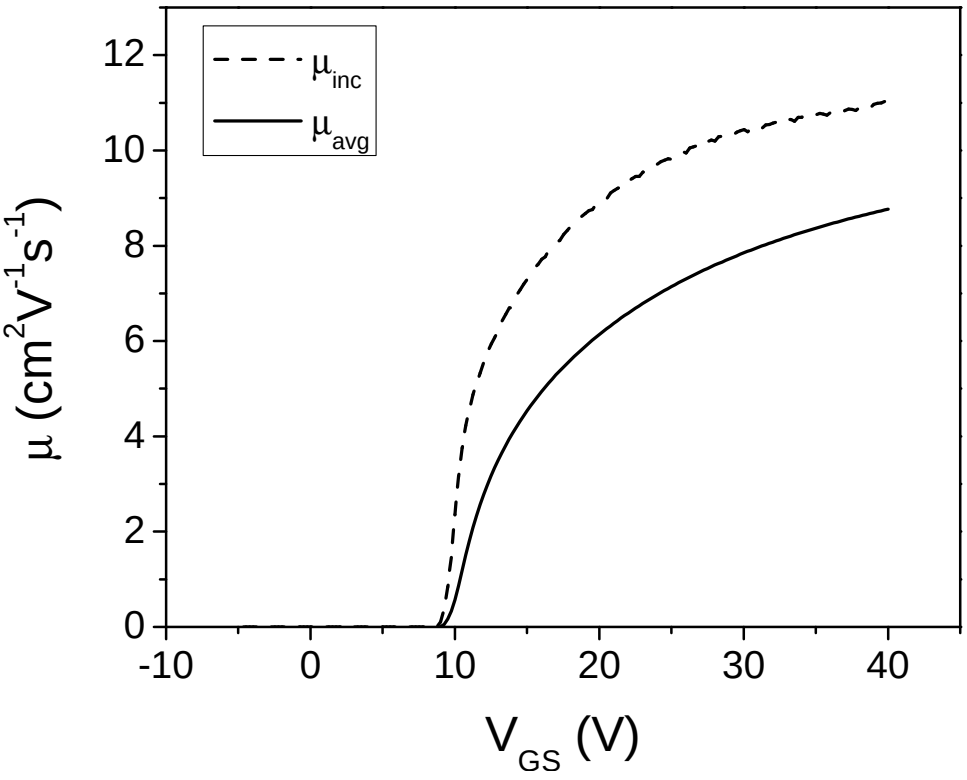


Figure 3.10: μ_{avg} and $\mu_{inc} - V_{GS}$ characteristics for the same device shown in Fig. 3.9 (a staggered bottom-gate IGZO TFT). μ_{avg} and μ_{inc} are determined using V_{DS} = 0.1 V and Eqs. 3.42 and 3.43c, respectively.

MOSFETs) and their physical interpretations are given by Hoffman. [87] Moreover, these estimates do not utilize V_T, a rather ambiguous quantity.

3.4 Conclusions

A summary of thin film processing techniques relevant to the fabrication of TFTs for this thesis is presented. Thin film processing techniques explored include evaporation, sputtering, atomic layer deposition, and post-deposition annealing. Sputtering is

discussed in some detail, as these techniques have been essential to the development of TFTs presented in Chapter 4.

Relevant thin-film characterization techniques including Hall and optical transmission measurements are presented. The Hall measurement is essential to evaluation of mobility, carrier concentration, and conductivity of thin-films. Optical characterization of films allows determination of the energy band gap and transition type. Additionally, the modified optical absorption spectrum for amorphous semiconductors is discussed.

Finally, an overview of TFT characterization is given. First, the uses of output and transfer characteristics are presented. This includes estimation of the subthreshold swing and drain current on-to-off ratio. Then, V_{on} is introduced and is identified as a device parameter that indicates the lower range of device operation. Finally, channel mobility extraction is discussed.

4. OXIDE SEMICONDUCTOR-BASED THIN-FILM TRANSISTORS

Indium gallium oxide (IGO), zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO) are explored as semiconductor layers in TFTs. Interest in these materials is garnered from a variety of sources. IGO-based TFTs have been demonstrated in transparent circuits. [19] ZTO is a low-cost material. IGZO-based TFTs have been fabricated on flexible substrates. [114] Several experimental variables are examined in this section with the intention of developing low-temperature processes compatible with a variety of flexible plastic substrates. Table 4.1 summarizes the materials experimental variables investigated for each material.

4.1 IGO-based thin-film transistors

IGO-based TFTs are fabricated by using a staggered bottom-gate test structure. [86] The structure employs a p-doped (boron, $\sim 3 \times 10^{16}$ cm^{-3}) 10×15 mm^2 Si substrate with a SiO_2 (100 nm thick) gate dielectric layer formed via thermal oxidation. The p-doped Si acts as both the gate and substrate. Ta/Au layers (10/300 nm thick, respectively) are deposited on the backside of the Si substrate to form a gate contact. The IGO semiconductor layer (typically $\sim$50 nm thick) and ITO source and drain electrodes (typically $\sim$250 nm thick) are deposited via rf magnetron sputtering and are patterned using shadow masks. IGO deposition employs a 2 in target sputtered at 75 W and 5 mTorr total Ar/O_2 processing pressure with a 10 cm target-to-substrate distance and various O_2 partial pressures

Table 4.1: Overview of materials and experimental variables employed for exploration of oxide semiconductor-based TFTs.

Material	Structure	S/D Material(s)	Experimental variables
IGO	Staggered bottom-gate	ITO	Anneal Temperature O_2 Partial Pressure Stoichiometry
ZTO	Staggered bottom-gate	Al	Anneal Temperature Anneal Ambient O_2 Partial Pressure
IGZO	Staggered bottom-gate	ZIO ITO	Anneal Temperature O_2 Partial Pressure rf Power Semiconductor thickness

(0.5, 0.25, and 0 mTorr). Two ceramic targets (Cerac, Inc.) with different In/Ga ratios ($InGaO_3$ and $In_{1.33}Ga_{0.67}O_3$) are used. Following IGO deposition, devices are furnace annealed in air for 1 hour with temperatures ranging from 200 to 800 °C. Six test structures are fabricated on each 10×15 mm^2 substrate (three with W/L = 1000 μm/200 μm and three with 2000 μm/200 μm).

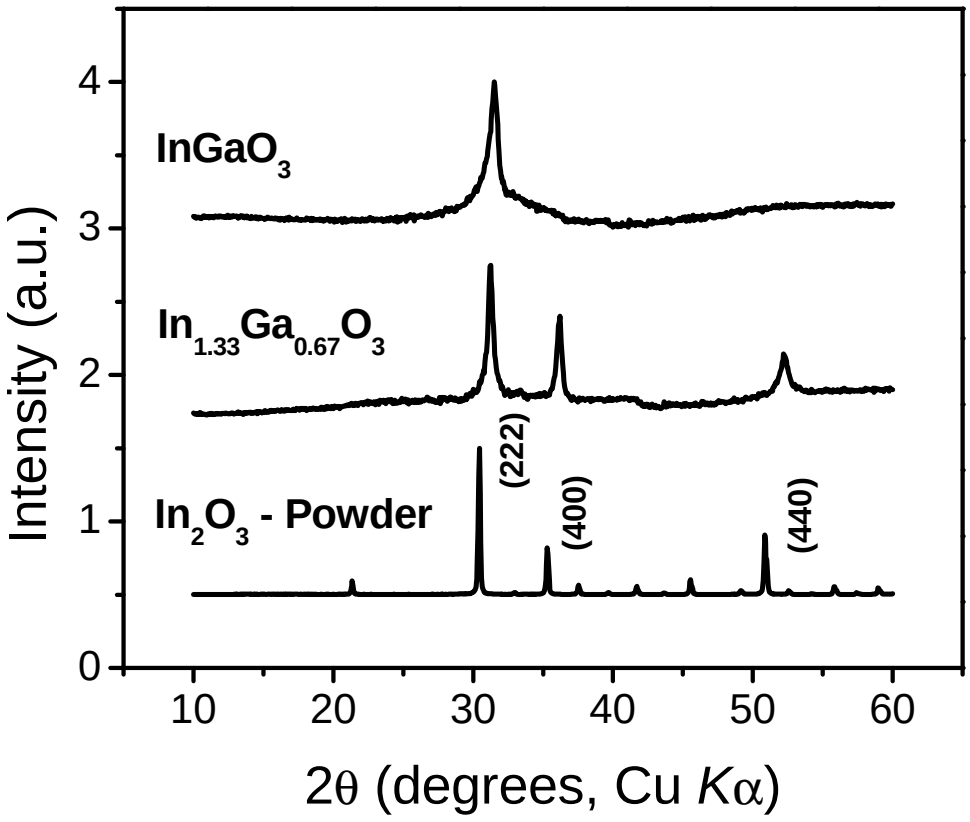


Figure 4.1: XRD patterns are obtained for $InGaO_3$ and $In_{2x}Ga_{2-2x}O_3$ (thin films) material systems from a Siemens D5000 diffractometer using Cu Kα radiation and θ-2θ scans. The thin films (∼400 nm) are subjected to a 700 °C anneal. An In_2O_3 (powder) pattern is shown for reference.

4.1.1 Thin film analysis

XRD patterns are obtained for ∼400 nm films which are deposited from $InGaO_3$ and $In_{1.33}Ga_{0.67}O_3$ sputter targets; individual films are subjected to annealings between 400 and 700 °C in 100 °C steps. The XRD data are obtained using a Siemens D5000 diffractometer with Cu Kα radiation and θ-2θ scanning. XRD patterns for $In_{1.33}Ga_{0.67}O_3$ and $InGaO_3$ films annealed at 700 °C are shown in Fig. 4.1. The $In_{1.33}Ga_{0.67}O_3$ pattern is similar to the cubic In_2O_3 powder reference pattern, but exhibits a systematic shift to

higher 2θ for the (222), (400), and (440) peaks, likely due to Ga substitution into the cubic lattice with a concomitant reduction in the unit cell size. The additional increase in Ga concentration of $InGaO_3$ results in a further shift of the (222) peak to a higher 2θ, further reduction in unit cell size, and absence of the (400) and (440) peaks.

Although not shown here, In_2O_3 thin films are examined and found to be polycrystalline as-deposited. In contrast, $In_{1.33}Ga_{0.67}O_3$ and $InGaO_3$ thin films are polycrstalline only after post-deposition anneals at temperatures in excess of 600 °C and 700 °C, respectively. Below these annealing temperatures, the XRD patterns exhibit a single, extremely broad peak at $2\theta \sim 34^\circ$, characteristic of amorphous indium gallium oxide films previously reported. [70]

4.1.2 TFT characteristics

Log(I_D)$-V_{GS}$ and log(I_G)$-V_{GS}$ characteristics (at V_{DS} = 30 V) are shown in Fig. 4.2 for an $In_{1.33}Ga_{0.67}O_3$ TFT which is subjected to a 200 °C channel layer anneal. Note that I_D, V_{GS}, I_G, and V_{DS} are the drain current, gate-to-source voltage, gate current, and drain-to-source voltage, respectively. $I_D - V_{DS}$ characteristics, where V_{GS} is decreased from 15 V (top curve) to 6 V in 3 V steps, are shown in the inset of Fig. 4.2. Qualitatively ideal TFT behavior is observed, including drain current saturation.

Electrical parameters often used to characterize a TFT are turn-on voltage, drain current on-to-off ratio, and channel mobility. The turn-on voltage, V_{on}, is the gate voltage at the onset of channel conduction, i.e., the gate voltage at the onset of the initial sharp

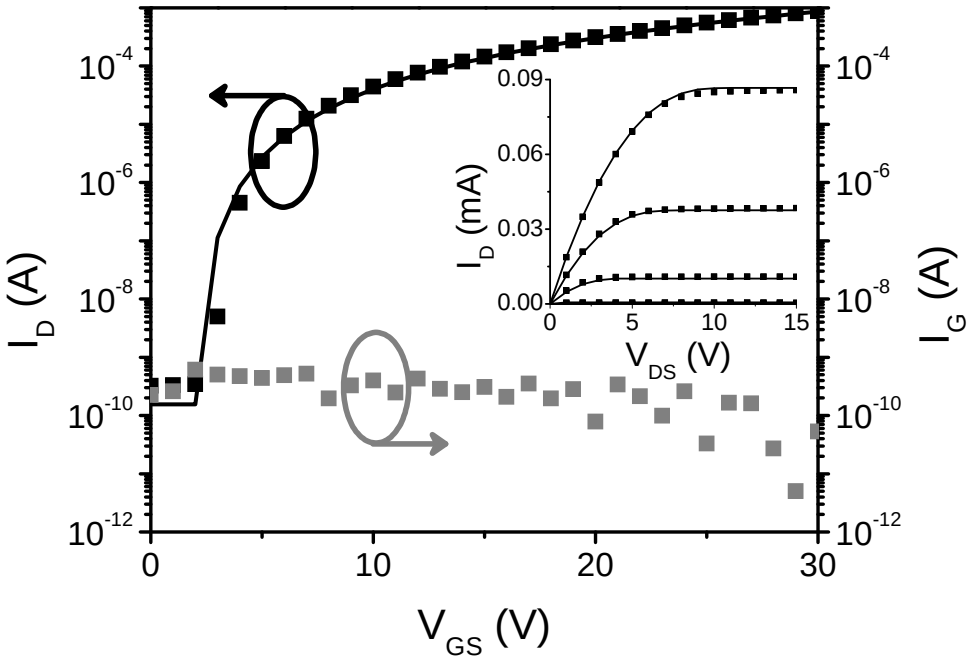


Figure 4.2: Log(I_D)$-V_{GS}$ and log(I_G)$-V_{GS}$ characteristics obtained at V_{DS} = 30 V for an $In_{1.33}Ga_{0.67}O_3$ TFT. The channel layer processing employs an Ar/O_2 processing pressure of 5 mTorr with 0.25 mTorr oxygen partial pressure and a 200 °C post-deposition anneal. (Inset) $I_D - V_{DS}$ characteristic where V_{GS} is varied from 15 (top curve) to 6 V in 3 V steps. The solid squares represent measured data points. The solid lines are generated using a closed-form DC model for long-channel TFTs with gate voltage-dependent mobility characteristics.

increase in current in a log(I_D)$-V_{GS}$ characteristic. [87] V_{on} is equal to 2 V for the device shown in Fig. 4.2. The drain current on-to-off ratio is $> 10^6$.

Two estimates for the channel mobility are the incremental (μ_{inc}) and average (μ_{avg}) mobility. [87] While both estimates are assessed in the linear region of device operation ($V_{DS} \rightarrow 0$ V), each has a unique physical interpretation. μ_{inc} represents the mobility of incrementally induced carriers with changing gate voltage, assuming that carriers already present in the channel have a constant mobility. μ_{avg} represents the average mobility of all carriers in the channel. As shown in Fig. 4.3, μ_{inc} and μ_{avg} saturate at values of $\sim$19 and

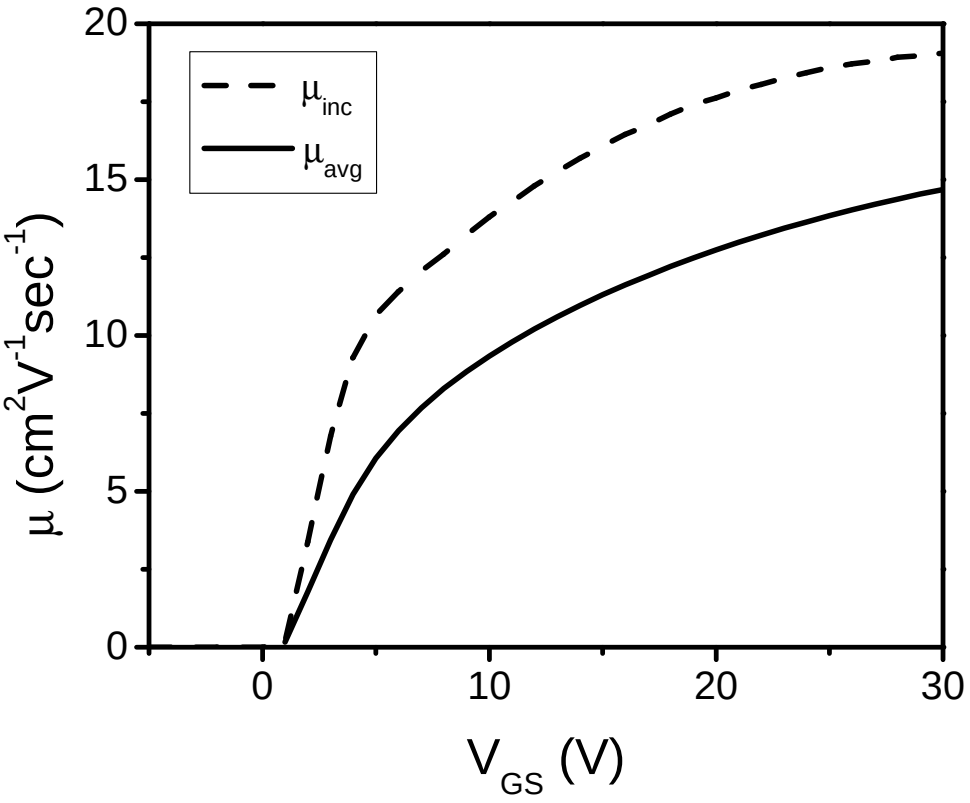


Figure 4.3: μ_{inc} and μ_{avg} as a function of V_{GS} for an $In_{1.33}Ga_{0.67}O_3$ TFT. The channel layer processing employs an Ar/O_2 processing pressure of 5 mTorr with 0.25 mTorr oxygen partial pressure and a 200 °C post-deposition anneal.

$\sim$15 $cm^2V^{-1}s^{-1}$, respectively. The validity of the channel mobility estimates is verified by calculating drain current values using the μ_{avg} curve in Fig. 4.3. The solid lines in Fig. 4.2 are generated using a DC model for long-channel TFTs with gate voltage-dependent mobility characteristics [158] and show reasonable agreement with measured data (solid squares).

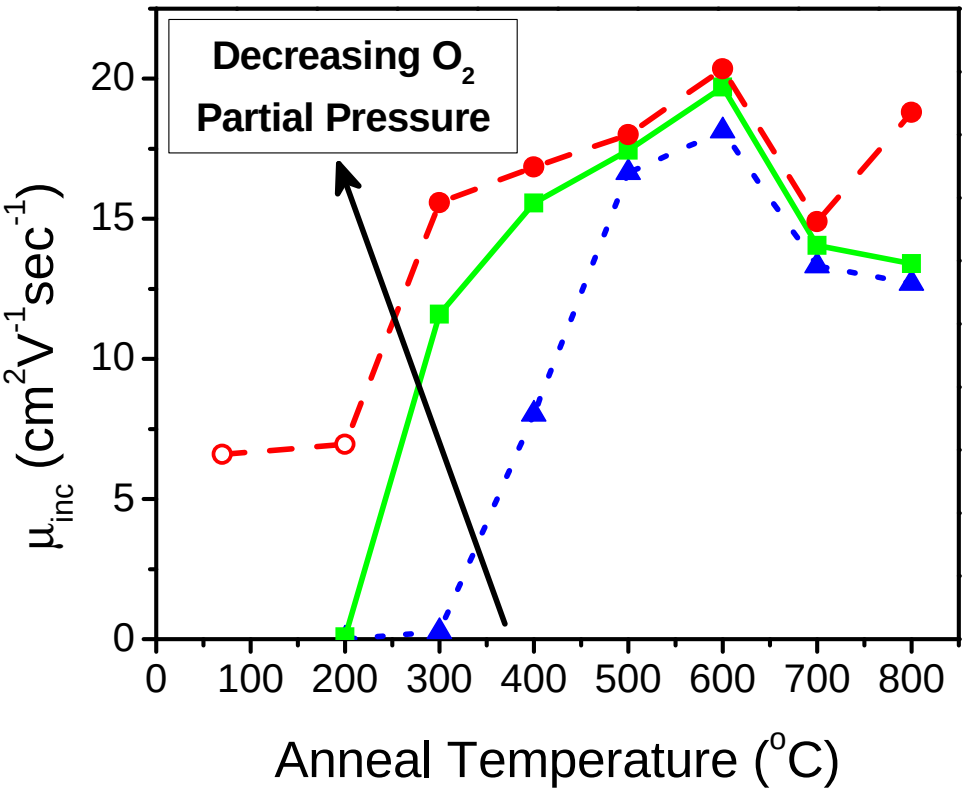


Figure 4.4: Incremental mobility−annealing temperature characteristics obtained at V_{DS} = 1 V for $InGaO_3$ TFTs sputtered in Ar/O_2 at a processing pressure of 5 mTorr with several oxygen partial pressures. These oxygen partial pressures consist of 0.5 (dotted), 0.25 (solid), and 0 (dashed) mTorr; the arrow indicates the direction of decreasing oxygen partial pressure. Note that open circles represent TFTs with $V_{on} < -20$ V.

4.1.3 Effects of O_2 partial pressure and stoichiometry

Several μ_{inc}−annealing temperature characteristics for $InGaO_3$ TFTs are shown in Fig. 4.4 and correspond to TFTs fabricated in Ar/O_2 at a processing pressure of 5 mTorr with different oxygen partial pressures (0.5, 0.25, and 0 mTorr). In these characteristics, the post-deposition annealing temperature is varied from 200 to 800 °C in 100 °C increments. Additionally, the performance of non-annealed TFTs (TFTs not subjected to an intentional post-deposition anneal) are plotted at 70 °C to account for the approx-

imate, unintentional in-situ temperature attained during deposition. Up to 600 °C, the mobility increases with increasing annealing temperature, then decreases at 700 °C. The initial increase in mobility with annealing temperature is attributed to modification of the semiconductor/insulator interface with temperature or to improved local atomic rearrangement. Recalling that $InGaO_3$ thin films are polycrystalline at 700 °C, the decrease in mobility witnessed in Fig. 4.4 is tentatively attributed to grain boundary-inhibited transport. [24]

For the characteristics shown in Fig. 4.4, first notice that two low-temperature data points are identified by open circles, indicating that V_{on} for these devices is extremely low ($<$ -20 V). Next, consider the μ_{inc} trend; in general, μ_{inc} increases with decreasing oxygen partial pressure. Devices annealed at 300 °C exhibit μ_{inc} values of $\sim$0.3, 11.6, and 15.6 $cm^2V^{-1}s^{-1}$ for oxygen partial pressures of 0.5, 0.25, and 0 mTorr, respectively. Finally, note that although the V_{on} trend is not explicitly shown here, V_{on} decreases (becomes more negative) with decreasing oxygen partial pressure. For devices annealed at 300 °C, V_{on} is $\sim$0.1, 0, and -12.8 V for oxygen partial pressures of 0.5, 0.25, and 0 mTorr, respectively. It is likely that the increase in μ_{inc} and decrease in V_{on} with decreasing oxygen partial pressure are interrelated. A decrease in V_{on} corresponds to an increase in free carrier concentration, i.e., a shift in the zero-gate bias Fermi level towards the conduction band. As the zero-gate bias Fermi level shifts towards the conduction band, a larger fraction of interface and/or traps within the semiconductor are filled, resulting in reduced trapping of injected channel electrons and a corresponding increase in channel mobility.

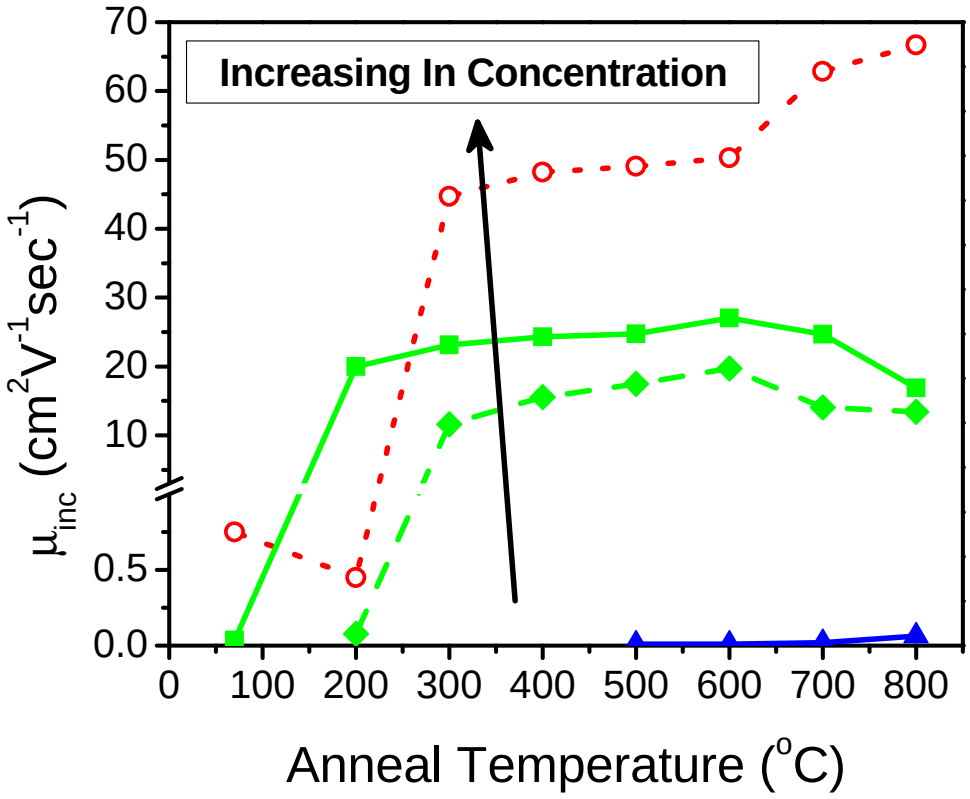


Figure 4.5: Incremental mobility−annealing temperature characteristics obtained at V_{DS} = 1 V for TFTs fabricated from several sputter target compositions, i.e., Ga_2O_3 (solid line, triangles), $InGaO_3$ (dashed line, diamonds), $In_{1.33}Ga_{0.67}O_3$ (solid line, squares), and In_2O_3 (dotted line, open circles). The arrow indicates the direction of increasing In concentration in the sputter target. These TFTs are fabricated in Ar/O_2 at a processing pressure of 5 mTorr with an oxygen partial pressure of 0.25 mTorr. Note that open circles represent TFTs with $V_{on} < -20$ V.

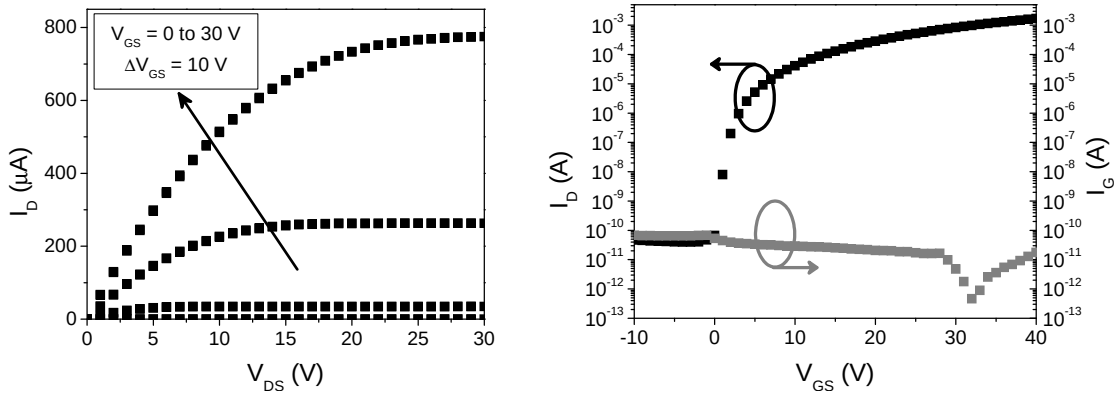
Four μ_{inc}−annealing temperature characteristics are shown in Fig. 4.5 and correspond to TFTs fabricated with similar processes (i.e., an Ar/O_2 processing pressure of 5 mTorr with an oxygen partial pressure of 0.25 mTorr), but from sputter targets of differing composition, i.e., Ga_2O_3, $InGaO_3$, $In_{1.33}Ga_{0.67}O_3$, and In_2O_3. μ_{inc} for In_2O_3 TFTs increases with annealing temperature to a maximum value of 67 $cm^2V^{-1}s^{-1}$ at 800 °C;

this increase is attributed to the monotonic increase in grain size with annealing temperature, as observed by XRD analysis.

Comparing the μ_{inc} trends exhibited by similarly processed $InGaO_3$ and In_2O_3 TFTs, a decrease in μ_{inc} is not observed in In_2O_3 TFTs subjected to high temperature anneals. This may be due to the fact that In_2O_3 is polycrystalline over the entire range of annealing temperatures, while $InGaO_3$ is amorphous at low temperature and begins to crystallize above 600 °C. Additionally, this discrepancy in the In_2O_3 and $InGaO_3$ annealing temperature trends may arise, at least partially, from the extremely negative V_{on} ($<$ -20 V) of In_2O_3 channel layer TFTs. This extremely negative V_{on} corresponds to a high electron carrier concentration in the channel, which leads to an increased fraction of filled traps and to a reduced grain boundary activation barrier, resulting in improved electron mobility. [24, 88, 159] However, it should be noted that a large negative V_{on}, as observed in In_2O_3 TFTs, will require level-shifting circuitry when integrating such discrete devices into circuits, which is undesirable.

Now, consider the Ga_2O_3 characteristic, which coincides with the x-axis in Fig. 4.5. Below an annealing temperature of 500 °C, Ga_2O_3 TFTs exhibit negligible field-effect. At 800 °C, Ga_2O_3 TFTs exhibit a maximum μ_{inc} of $\sim$0.05 $cm^2V^{-1}s^{-1}$. In contrast to In_2O_3, Ga_2O_3 TFTs exhibit large positive V_{on}'s ($>$ 10 V). This combination of low mobility and large positive V_{on} suggests that Ga_2O_3-based TFTs possess a large density of empty traps at the semiconductor/insulator interface and/or in the active channel layer.

The center curves shown in Fig. 4.5 represent TFTs fabricated from $InGaO_3$ and $In_{1.33}Ga_{0.67}O_3$ sputter targets. It is evident that μ_{inc} increases with increasing indium



(a) (b)

Figure 4.6: (a) $I_D - V_{DS}$ characteristic where V_{GS} is varied from 0 (bottom curve) to 30 V in 10 V steps. (b) Log(I_D)$-V_{GS}$ and log(I_G)$-V_{GS}$ characteristics obtained at V_{DS} = 30 V for a ZTO-based TFT. The ZTO deposition employs a rf power of 75 W, an Ar/O_2 processing pressure of 5 mTorr with 0.050 mTorr oxygen partial pressure, and a 10 cm target-to-substrate distance. Additionally, the ZTO layer is subjected to a 175 $^{\circ}$C post-deposition anneal in N_2.

concentration. The observed increase in μ_{inc} may arise from two factors or a combination thereof. First, this increase in μ_{inc} may derive from the larger radius of the In 5*s* orbital relative to the Ga 4*s* orbital, leading to better orbital overlap and a broader conduction band. [51, 52] Additionally, the increased μ_{inc} is accompanied by a decrease in V_{on} (not shown), which indicates a shift in the zero-gate bias Fermi level towards the conduction band and, potentially, improved electron mobility due to a larger fraction of filled traps, as previously discussed.

4.2 ZTO-based thin-film transistors

ZTO-based ($ZnSnO_3$) TFTs are fabricated with a staggered bottom-gate test structure. [86] The structure employs a p-doped (boron, $\sim 3 \times 10^{16}$ cm^{-3}) 10×15 mm^2 Si substrate with a SiO_2 (100 nm thick) gate dielectric layer formed via thermal oxidation.

The p-doped Si acts as both the gate and substrate. Ta/Au (10/300 nm thick, respectively) are deposited on the backside of the Si substrate to form a gate contact. The ZTO channel layer is deposited via rf magnetron sputtering and is patterned using shadow masks. ZTO deposition employs a 2 in target (purchased from Cerac, Inc.) sputtered in 5 mTorr total Ar/O_2 processing pressure with a 10 cm target-to-substrate distance. An rf power of 75 W and various O_2 partial pressures (0.075, 0.050, and 0.025 mTorr) are employed. Following ZTO deposition, devices are furnace annealed in air or N_2 for 1 hour with temperatures ranging from 175 to 325 °C. Finally, Al or ITO is deposited as the source and drain electrodes (typically ∼200 nm thick). Six test structures are fabricated on each 10×15 mm^2 substrate (three with W/L = 1000 μm/200 μm and three with 2000 μm/200 μm).

4.2.1 TFT characteristics

Exemplary $I_D - V_{DS}$ characteristics for a ZTO TFT are shown in Fig. 4.6a. This TFT is fabricated using rf sputtering with a power of 75 W, an Ar/O_2 processing pressure of 5 mTorr with 0.050 mTorr oxygen partial pressure, and a 10 cm target-to-substrate distance. The ZTO layer is subjected to a 175 °C post-deposition anneal in N_2. In Fig. 4.6a, V_{GS} is increased from 0 V (bottom curve) to 30 V in 10 V steps. For each V_{GS} step, the drain voltage is swept forward then backwards; no hysteresis is visually apparent. Moreover, qualitatively, ideal TFT behavior is observed, including drain current saturation, indicating that the entire thickness of the semiconductor layer can be fully depleted.

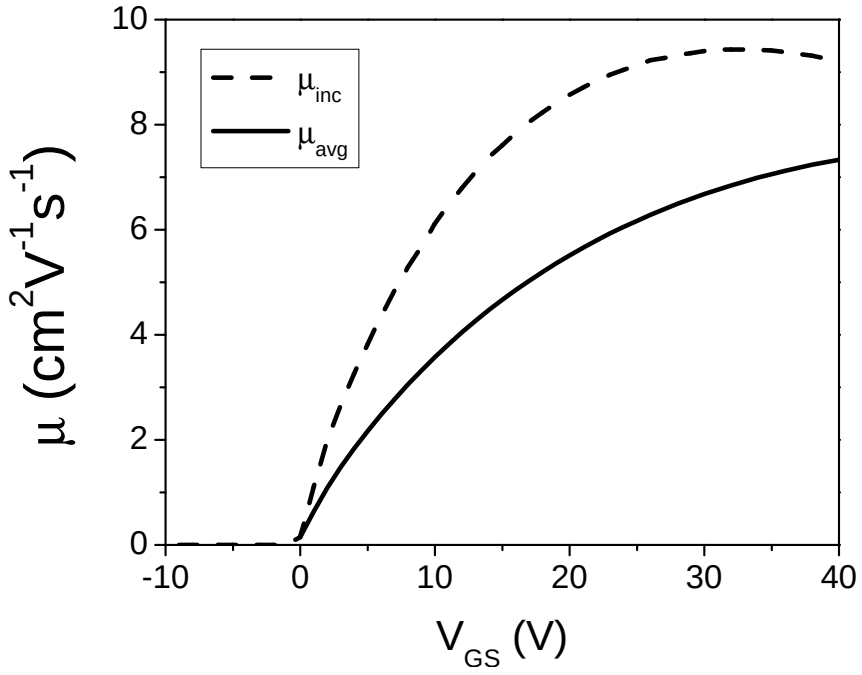


Figure 4.7: μ_{inc} and μ_{avg} as a function of V_{GS} obtained at V_{DS} = 100 mV for the ZTO-based TFT shown in Fig. 4.6.

The corresponding $\log(I_D)-V_{GS}$ transfer characteristic (at V_{DS} = 30 V) is shown in Fig. 4.6b. This transfer characteristic is utilized to estimate several figures-of-merit, including V_{on}, S, and I_D^{on-off}, which are $\sim$-1 V, 0.6 V/decade, and $> 10^7$, respectively, for this device.

Two estimates for the channel mobility obtained in the linear region of device operation ($V_{DS} \rightarrow 0$ V) are the incremental (μ_{inc}) and average (μ_{avg}) mobility. For the characteristics shown in Fig. 4.7, V_{DS} = 10 mV is used to estimate the mobility; maximum values of μ_{inc} and μ_{avg} are $\sim$9 and $\sim$7 $\mathrm{cm^2V^{-1}s^{-1}}$, respectively. For additional information on channel mobility extraction, see Sec. 3.3.7.

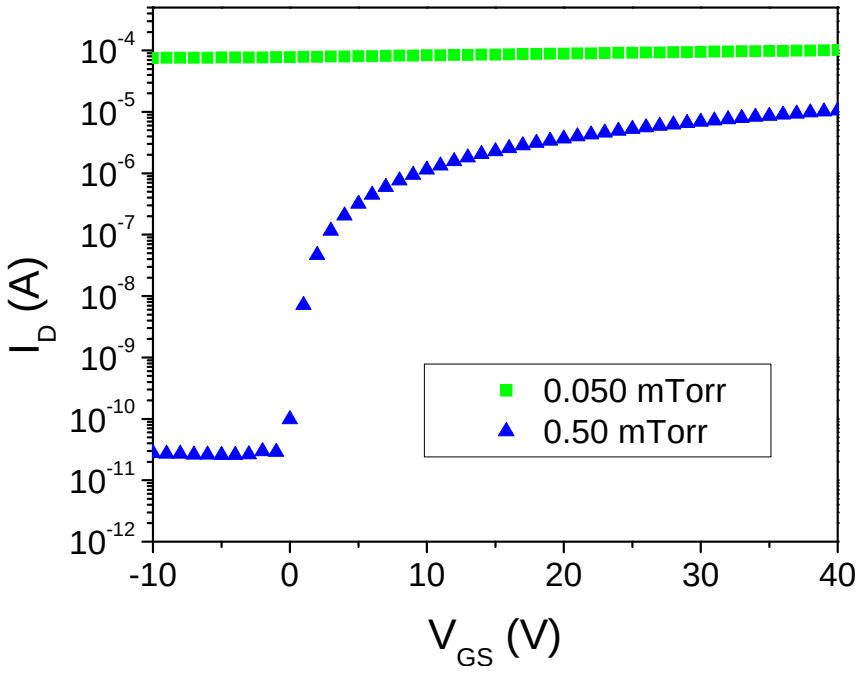


Figure 4.8: Log(I_D)−V_{GS} characteristics obtained at V_{DS} = 100 mV for ZTO-based TFTs fabricated after two different extended presputter treatments (where an Ar/O_2 processing pressure of 5 mTorr is employed with 0.050 and 0.50 mTorr O_2 partial pressures). The deposition parameters for the semiconductor layer are a rf power of 75 W, an Ar/O_2 processing pressure of 5 mTorr with 0.050 mTorr oxygen partial pressure, and a 10 cm target-to-substrate distance. The ZTO layer is subjected to a 175 °C post-deposition anneal in N_2.

4.2.1.1 Additional Remarks

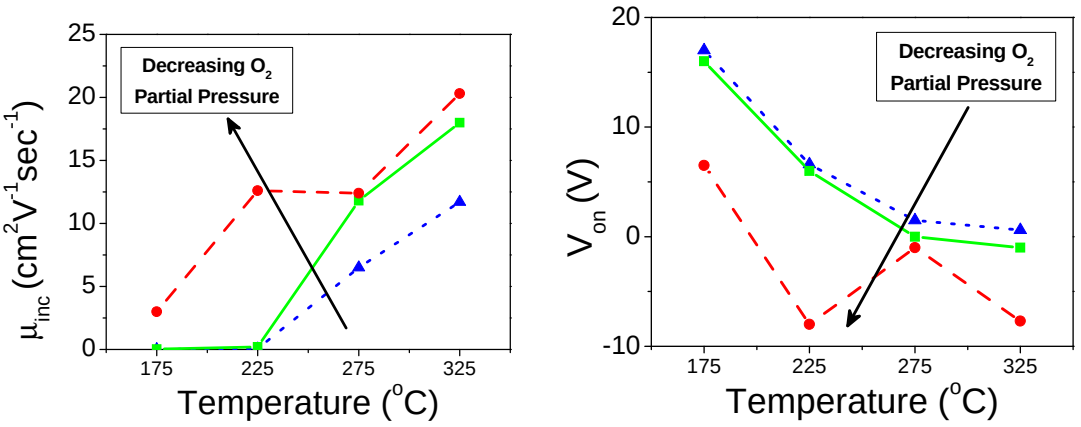
Prior to deposition of the semiconductor layer for device fabrication, two presputter procedures are employed to adequately condition the target surface to obtain reproducible results. A short presputter (10-20 minutes) is performed before each deposition; the processing conditions for this presputter are identical to those employed for the deposition. An extended presputter (1 to 4 hours) is initially performed when the target is placed in the chamber to remove any contamination that may have accumulated during target storage. This presputter is typically performed in an Ar/O_2 ambient with 10% O_2 (i.e.,

0.50 mTorr O_2 partial pressure when the total processing pressure is 5 mTorr). However, modifying the extended presputter can significantly alter device performance. Figure 4.8 shows two devices which are fabricated with identical processing conditions after the target is subjected to different extended presputter treatments. As observed in Fig. 4.8, presputtering in low O_2 percentages leads to a large negative shift in V_{on} when compared to the typical 10% O_2 extended presputter treatment. Thus, it is recommended that the extended presputter treatment not be modified after a process recipe has been established.

4.2.2 Effects of O_2 partial pressure

Several $\mu_{inc}-$annealing temperature characteristics for ZTO TFTs are shown in Fig. 4.9 and correspond to TFTs fabricated in Ar/O_2 at a processing pressure of 5 mTorr with different oxygen partial pressures (0.075, 0.050, and 0.025 mTorr). In these characteristics, the post-deposition annealing temperature is varied from 175 to 325 °C in 50 °C increments. The mobility increases with increasing annealing temperature. This increase in mobility with annealing temperature is attributed to modification of the semiconductor/insulator interface or to improved local atomic rearrangement. Comparing the three $\mu_{inc}-$annealing temperature characteristics, the mobility increases with decreasing O_2 partial pressure. Recall that a similar trend is observed with IGO-based TFTs.

The corresponding V_{on}-annealing temperature characteristics are shown in Fig. 4.9b. V_{on} generally decreases with increasing annealing temperature. Comparing the three V_{on} characteristics, V_{on} generally decreases with decreasing O_2 partial pressure. This is not surprising as intrinsic defects (i.e., oxygen vacancies) in oxide semiconductors are a



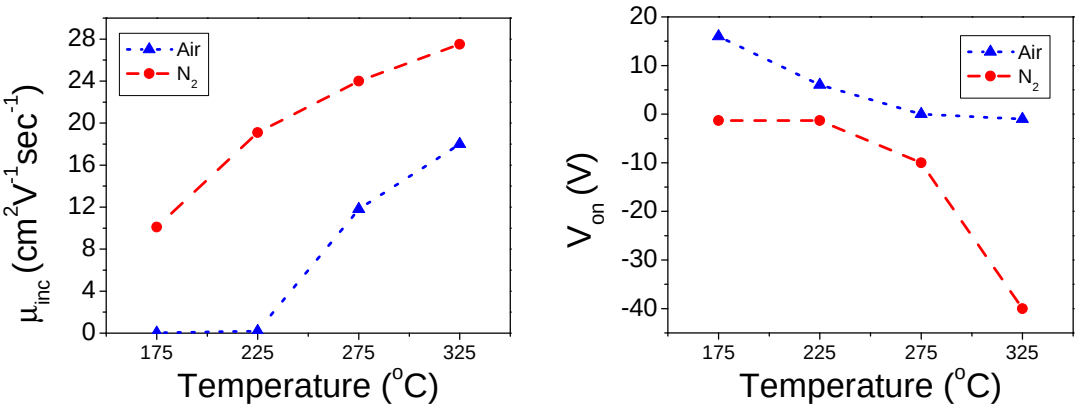
(a) (b)

Figure 4.9: (a) μ_{inc} and (b) V_{on}—annealing temperature characteristics for ZTO-based TFTs sputtered at a rf power of 75 W and in an Ar/O_2 processing ambient of 5 mTorr with several O_2 partial pressures. These O_2 partial pressures consist of 0.075 (dotted), 0.050 (solid), and 0.025 mTorr (dashed); the arrow indicates the direction of decreasing O_2 partial pressures.

source of carrier generation. It is likely that this decrease in V_{on} is associated with the observed increase in μ_{inc} as the the oxygen partial pressure is reduced. A decrease in V_{on} corresponds to an increase in carrier concentration, i.e., a shift in the zero-gate bias Fermi level towards the conduction band. As the zero-gate bias Fermi level shifts towards the conduction band, a larger fraction of interface and/or traps within the semiconductor are filled, resulting in reduced trapping of injected channel electrons and a corresponding increase in channel mobility.

4.2.3 Effects of anneal ambient

The previous sections have discussed the effect of deposition (in situ) process parameters to control device properties. Here, the effect of the post-deposition anneal am-



(a) (b)

Figure 4.10: (a) μ_{inc} and (b) V_{on}—annealing temperature characteristics for ZTO-based TFTs sputtered at a rf power of 75 W and in an Ar/O_2 processing ambient of 5 mTorr with an O_2 partial pressure of 0.050 mTorr. These devices are subjected to post-deposition annealing treatments in air (dotted) and N_2 (dashed).

bient is explored. This gives an additional experimental variable to control the turn-on voltage and is particularly useful for fabricating low temperature devices.

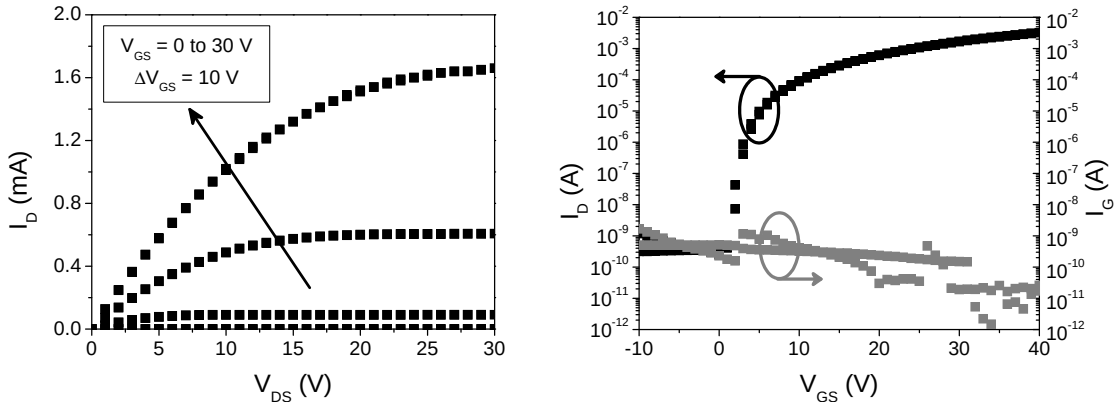
Figure 4.10 shows μ_{inc} and V_{on} as a function of annealing temperature for devices subjected to post-deposition annealing treatments in air or N_2. Compared to the air anneal, the N_2 anneal reduces V_{on} and increases μ_{inc}. The decrease in V_{on} is likely associated with an increased density of oxygen vacancies due to the inert anneal. The increase in μ_{inc} is likely associated with the decrease in V_{on}. The N_2 anneal is superior to the air anneal for devices processed in the 175-225 °C range since V_{on} is near zero and μ_{inc} is ~10-20 $cm^2V^{-1}s^{-1}$ for this temperature range. However, the N_2 anneal is inferior to the air anneal for devices processed in the 275-325 °C range; while μ_{inc} is greater when devices are annealed in N_2, V_{on} is highly negative.

4.3 IGZO-based thin-film transistors

IGZO-based ($InGaZnO_4$) TFTs are fabricated by using a staggered bottom-gate test structure. [86] The structure employs a p-doped (boron, $\sim 3 \times 10^{16}$ cm^{-3}) 10×15 mm^2 Si substrate with a SiO_2 (100 nm thick) gate dielectric layer formed via thermal oxidation. The p-doped Si acts as both the gate and substrate. Ta/Au (10/300 nm thick, respectively) are deposited on the backside of the Si substrate to form the gate contact. The IGZO channel layer is deposited via rf magnetron sputtering and is patterned using shadow masks. IGZO deposition employs a 3 in target (purchased from Cerac, Inc.) sputtered in a 5 mTorr total Ar/O_2 processing pressure with a 10 cm target-to-substrate distance. Several rf powers (75, 100, and 125 W) and various O_2 partial pressures (0.5, 0.25, and 0 mTorr) are employed. Additionally, various IGZO thicknesses (10 to 150 nm) are explored by modifying deposition time. Following IGZO deposition, devices are furnace annealed in air for 1 hour at temperatures ranging from 100 to 800 °C. Finally, ZIO ($ZnIn_4O_7$) or ITO is deposited as the source and drain electrodes (typically $\sim$200 nm thick). Six test structures are fabricated on each 10×15 mm^2 substrate (three with W/L = 1000 μm/200 μm and three with 2000 μm/200 μm).

4.3.1 TFT characteristics

Baseline IGZO-based TFTs are fabricated using rf sputtering with a power of 75 W, a processing pressure of 5 mTorr in pure Ar, and a 10 cm target-to-substrate distance. The IGZO layer is subjected to a 175 °C post-deposition anneal in air. Exemplary $I_D - V_{DS}$ characteristics for TFTs fabricated using these processing conditions are shown in



(a) (b)

Figure 4.11: (a) $I_D - V_{DS}$ characteristic where V_{GS} is varied from 0 (bottom curve) to 30 V in 10 V steps. (b) Log(I_D)$-V_{GS}$ and log(I_G)$-V_{GS}$ characteristics obtained at V_{DS} = 30 V for an IGZO-based TFT. The IGZO deposition employs a rf power of 75 W, a processing pressure of 5 mTorr in pure Ar, and a 10 cm target-to-substrate distance. Additionally, the IGZO layer is subjected to a 175 $^{\circ}$C post-deposition anneal.

Fig. 4.11a. Here, V_{GS} is increased from 0 V (bottom curve) to 30 V in 10 V steps. For each V_{GS} step, the drain voltage is swept forward, then backwards; no hysteresis is visually apparent. Moreover, qualitatively, ideal TFT behavior is observed, including drain current saturation, indicating that the entire thickness of the semiconductor layer can be fully depleted.

The corresponding log(I_D)$-V_{GS}$ transfer characteristic (at V_{DS} = 30 V) is shown in Fig. 4.11b. This transfer characteristic is utilized to estimate several figure-of-merits, including V_{on}, S, and I_D^{on-off}, which are $\sim$0 V, 0.6 V/decade, and $> 10^7$, respectively, for this device. It is interesting to note that TFTs based on other oxide semiconductors (e.g. IGO, ZTO, and ZIO) which are sputtered in pure argon typically require higher annealing temperatures ($\geq 300^{\circ}$C) to stabilize (i.e., reduce the free carrier concentration

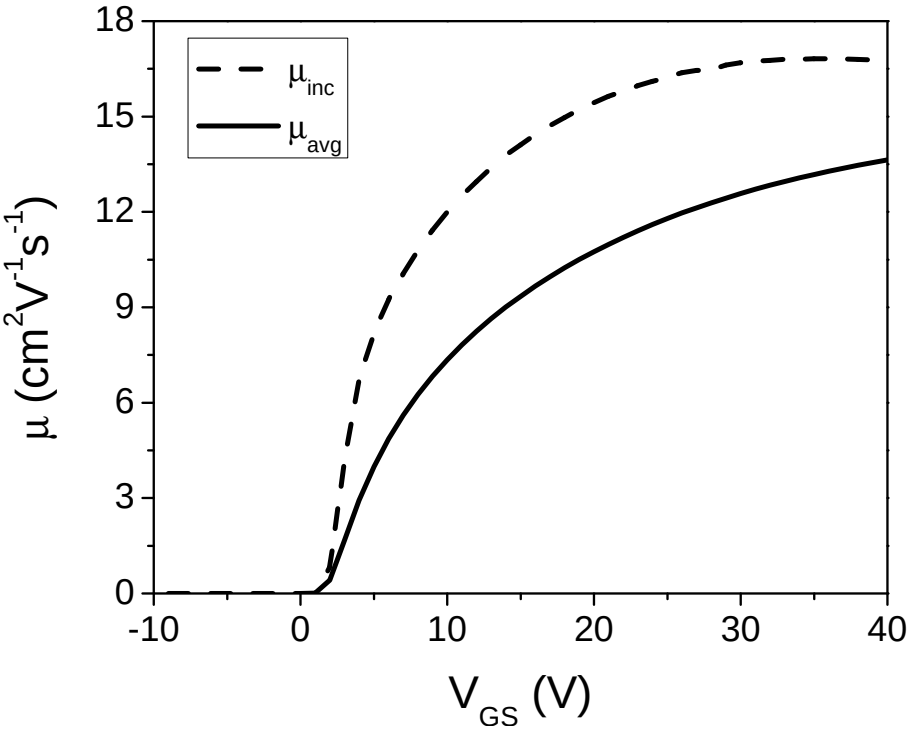


Figure 4.12: μ_{inc} (dashed) and μ_{avg} (solid) as a function of V_{GS} obtained at V_{DS} = 1 V for an IGZO-based TFT. The IGZO deposition employs a rf power of 75 W, a processing pressure of 5 mTorr in pure Ar, and a 10 cm target-to-substrate distance. Additionally, the IGZO layer is subjected to a 175 °C post-deposition anneal.

and subsequently, shift V_{on} towards zero) device characteristics. As shown here, 175 °C annealing results in stabilized device characteristics for IGZO-based TFTs.

Two estimates for the channel mobility obtained in the linear region of device operation ($V_{DS} \rightarrow 0$ V) are the incremental (μ_{inc}) and average (μ_{avg}) mobility. As shown in Fig. 4.12, μ_{inc} and μ_{avg} saturate at values of $\sim$17 and $\sim$14 $cm^2V^{-1}s^{-1}$, respectively. For additional information on channel mobility extraction, see Sec. 3.3.7.

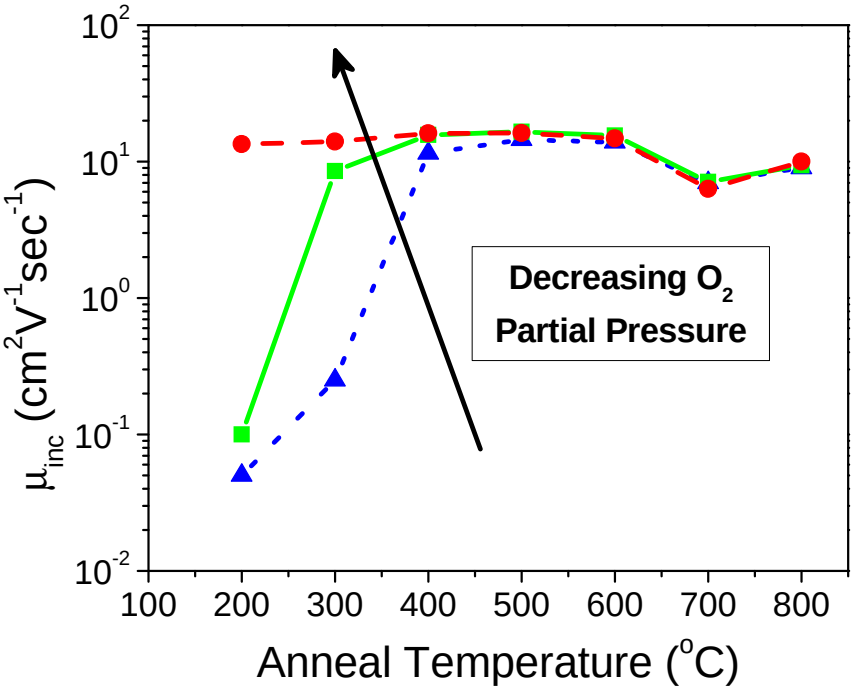


Figure 4.13: Log(μ_{inc})−annealing temperature characteristics obtained at V_{DS} = 1 V for IGZO-based TFTs sputtered at 100 W in Ar/O_2 at a processing pressure of 5 mTorr with several oxygen partial pressures. These oxygen partial pressures consist of 0.5 (dotted), 0.25 (solid), and 0 mTorr (dashed); the arrow indicates the direction of decreasing oxygen partial pressure.

4.3.2 Effects of O_2 partial pressure

Several μ_{inc}−annealing temperature characteristics for IGZO-based TFTs are shown in Fig. 4.13 and correspond to TFTs fabricated in Ar/O_2 at a processing pressure of 5 mTorr with different oxygen partial pressures (0.5, 0.25, and 0 mTorr). In these characteristics, the post-deposition annealing temperature is varied from 200 to 800 °C in 100 °C increments. It should be noted that non-annealed TFTs (TFTs not subjected to an intentional post-deposition anneal) do not exhibit an appreciable field-effect and thus, are omitted from this plot. First, consider the behavior of a single μ_{inc}−annealing tem-

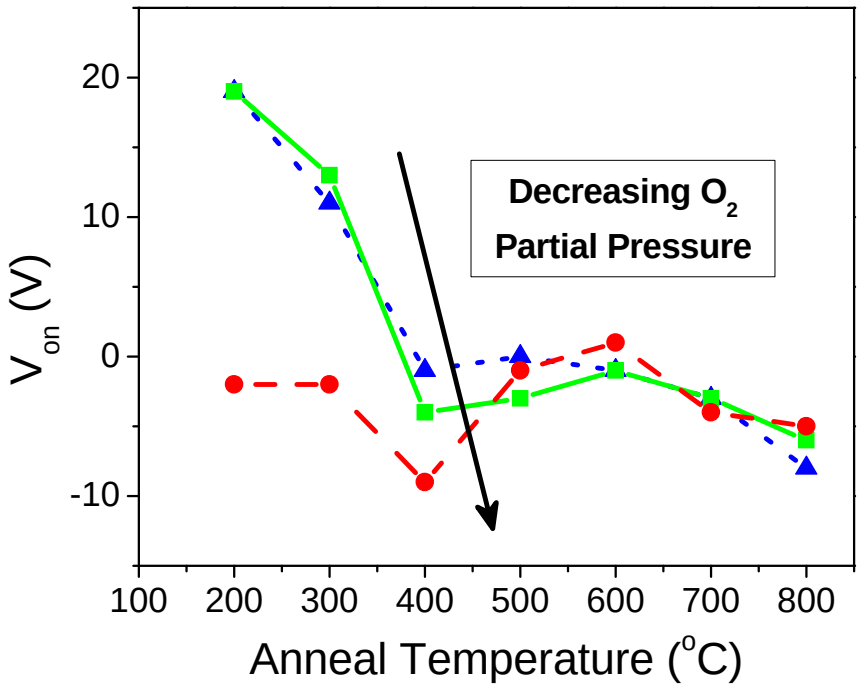


Figure 4.14: V_{on}—annealing temperature characteristics obtained at V_{DS} = 30 V for IGZO-based TFTs sputtered at 100 W in Ar/O_2 at a processing pressure of 5 mTorr with several oxygen partial pressures. These oxygen partial pressures consist of 0.5 (dotted), 0.25 (solid), and 0 mTorr (dashed); the arrow indicates the direction of decreasing oxygen partial pressure.

perature characteristic with respect to temperature. Up to 500 °C, the mobility increases with increasing annealing temperature to a maximum value of $\mu_{inc} \sim 16$ $cm^2V^{-1}s^{-1}$. This increase in mobility with annealing temperature is attributed to modification of the semiconductor/insulator interface with temperature or to improved local atomic rearrangement. For annealing temperatures above 600 °C, the mobility decreases with increasing annealing temperature. This decrease is possibly associated with crystallization (i.e., grain boundary-inhibited transport) or phase segregation in the IGZO layer. [24] As these high-temperature devices are of minimal interest for this work, the cause of this decrease is not explored.

Now, compare the $\mu_{inc}-$annealing temperature characteristics. Below 400 °C, the mobility increases with decreasing O_2 partial pressure (at 200 °C, μ_{inc} ∼0.05, 0.1, and 13.4 $cm^2V^{-1}s^{-1}$ for oxygen partial pressures of 0.5, 0.25, and 0 mTorr, respectively). As the anneal temperature is increased above 400 °C, the $\mu_{inc}-$annealing temperature characteristics for all three O_2 partial pressures begin to converge. Here, the annealing treatment dominates and minimizes the effect of other process parameters.

The corresponding V_{on}-annealing temperature characteristics are shown in Fig. 4.14. Below 400 °C, V_{on} decreases with increasing annealing temperature. Above 400 °C, V_{on} varies between 0 and -10 V. Comparing the three V_{on} characteristics, V_{on} generally decreases with decreasing O_2 partial pressure (at 400 °C, V_{on} ∼ -1, -4, and -9 V for oxygen partial pressures of 0.5, 0.25, and 0 mTorr, respectively). This is not surprising as intrinsic defects (i.e., oxygen vacancies) in oxide semiconductors are a source of carrier generation.

4.3.3 Effects of rf power

Several $\mu_{inc}-$annealing temperature characteristics for IGZO-based TFTs are shown in Fig. 4.15a and correspond to TFTs fabricated in Ar/O_2 at a processing pressure of 5 mTorr (0.5 mTorr O_2 partial pressure) with various rf powers (75, 100, and 125 W). In these characteristics, the post-deposition annealing temperature is varied from 200 to 800 °C in 100 °C increments. Below 400 °C, the mobility increases with increasing rf power (at 200 °C, μ_{inc} ∼0.004, 0.05, and 0.4 $cm^2V^{-1}s^{-1}$ for rf powers of 75, 100, and 125 W, respectively). As the anneal temperature is increased above 400 °C, the mobility

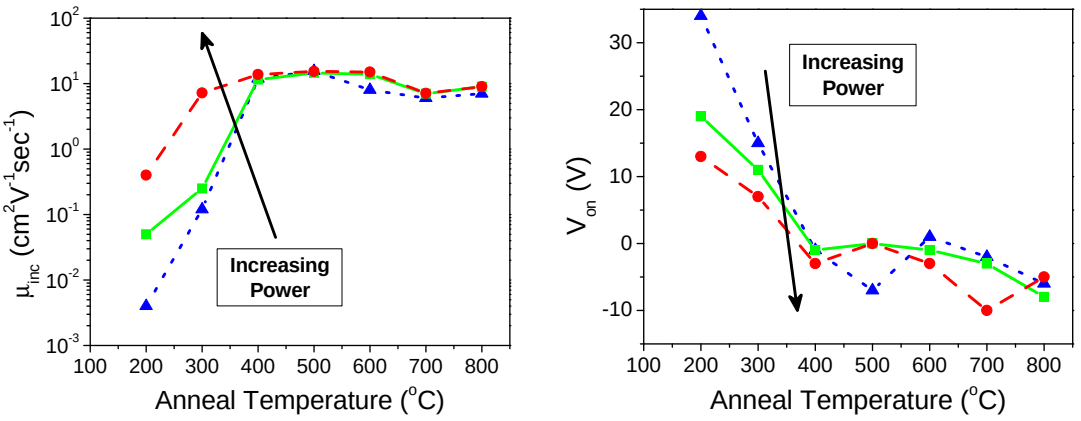


Figure 4.15: (a) Log(μ_{inc}) and (b) V_{on}−annealing temperature characteristics for IGZO-based TFTs sputtered in Ar/O_2 at a processing pressure of 5 mTorr (0.5 mTorr O_2 partial pressure) with several rf powers. These rf powers consist of 75 (dotted), 100 (solid), and 125 W (dashed); the arrow indicates the direction of increasing rf power.

characteristics for all three rf powers begin to converge. Above 400 °C, the annealing treatment dominates device characteristics and minimizes the effect of other process parameters.

Figure 4.15b shows the corresponding V_{on}-annealing temperature characteristics. First, consider one of the V_{on} characteristics; V_{on} decreases with increasing annealing temperature. Now, compare the three V_{on} characteristics; V_{on} generally decreases with increasing rf power (at 200 °C, $V_{on} \sim$ 34, 19, and 13 V for rf powers of 75, 100, and 125 W, respectively) and is associated with increasing free carrier concentration in the semiconductor layer with increasing rf power.

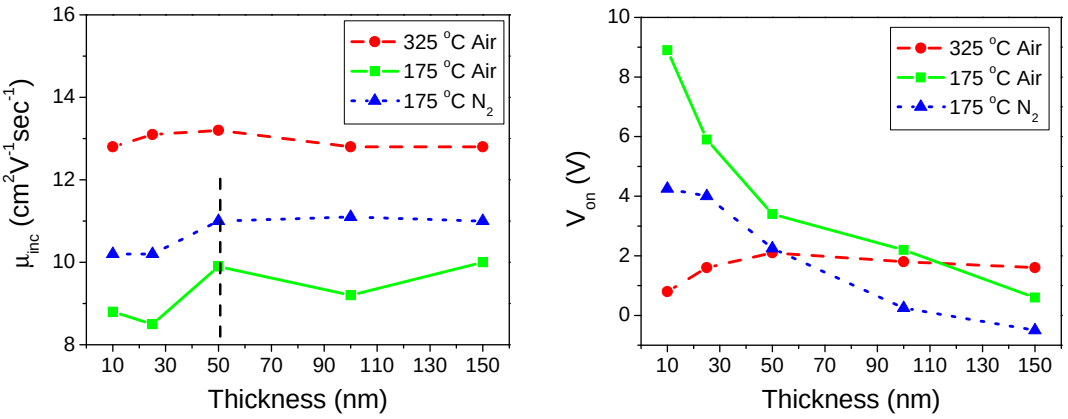
The increase in mobility and free carrier concentration (at low temperature) with increasing rf power is likely due to increased order in the semiconductor layer. As the rf power is increased, higher energy neutrals and ions can reach the substrate. This results

in increased adatom mobility and leads to increased order in the growing film. [160] Additionally, the increase in mobility and free carrier concentration are likely interrelated. An increase in free carrier concentration is concomitant with a shift in the zero-gate bias Fermi level towards the conduction band. As the zero-gate bias Fermi level shifts towards the conduction band, a larger fraction of interface traps and/or traps within the semiconductor are filled, resulting in reduced trapping of injected channel electrons and a corresponding increase in channel mobility.

4.3.4 Influence of semiconductor thickness

The effect of semiconductor thickness on TFT electrical performance has been investigated by Barquinha *et al*. for staggered bottom-gate ZIO-based devices and by Martin *et al*. for staggered top-gate a-Si:H devices. [112, 161] Trends observed in those systems are compared with the IGZO-based TFTs shown here.

Figure 4.16a shows μ_{inc} as a function of semiconductor thickness, t_s. In general, μ_{inc} does not significantly vary with respect to t_s ($< 15\%$ variation). This differs from experimental results for ZIO-based TFTs and a-Si:H TFTs, where the mobility can vary up to $3\times$ with t_s. [112, 161] For ZIO-based TFTs, the channel mobility decreases with increasing semiconductor thickness. Barquinha *et al*. attribute the reduction in mobility to the increased source-drain path length as t_s is increased. For a-Si:H TFTs, the mobility exhibits an initial increase and then a decrease as t_s is increased. The initial increase in mobility is attributed to an improvement in the quality of the a-Si:H layer, while the decrease in mobility is attributed to parasitic resistance effects.



(a) (b)

Figure 4.16: (a) μ_{inc} and (b) V_{on} as a function of semiconductor thickness for IGZO-based TFTs. The IGZO layer is rf sputtered at a power of 125 W, a processing pressure of 5 mTorr in Ar/O_2 (0.05 mTorr O_2 partial pressure), and a 10 cm target-to-substrate distance. Additionally, these TFTs are subjected to different post-deposition annealing treatments: 175 °C in N_2, 175 and 325°C in air.

Scrutinizing the mobility characteristics shown in Fig. 4.16a, there is arguably, a systematic change in mobility with respect to t_s for devices annealed at 175 °C. The vertically oriented black dashed line in Fig. 4.16a represents a demarkation between lower and higher-mobility regions for thinner and thicker TFTs, respectively. For an ultrathin semiconductor layer ($t_s \leq 25$ nm), conduction is confined near the insulator-semiconductor interface; since interface states and/or a higher concentration of defects are expected at an interface, this is likely to result in lower mobility for a thinner semiconductor layer. Additionally, an ultrathin semiconductor layer can be non-continuous and/or inhomogeneous as a consequence of the nucleation and island formation mechanism associated with the growth of a thin film. The non-continuous/inhomogeneous nature of an ultrathin semiconductor layer would be expected to inhibit conduction (and consequently, the mobility).

The associated $V_{on} - t_s$ characteristics are shown in Fig. 4.16b. For TFTs annealed at 325 °C in air, V_{on} is nearly independent of t_s, with only ∼1.3 V of variation in V_{on} across the entire range of semiconductor thicknesses. In contrast, for TFTs annealed at 175 °C (in air and N_2), V_{on} decreases with increasing thickness.

Before discussing the mechanisms which lead to this decrease in V_{on}, it is important to investigate the origin of V_{on}, which, to a large extent, is determined by charge or traps present within the semiconductor or at one of its interfaces. With this in mind, V_{on} is given as, [124, 162]

$$V_{on} \approx -\frac{Q_{IT}}{C_{ins}} - (Q_{free} + Q_{bulk})\left(\frac{1}{C_{ins}} + \frac{2}{C_{semi}}\right) - Q_{SS}\left(\frac{1}{C_{ins}} + \frac{1}{C_{semi}}\right), \quad (4.1a)$$

$$= -\frac{Q_{IT}}{C_{ins}} - qt_s(n_{free} + n_{bulk})\left(\frac{1}{C_{ins}} + \frac{2}{C_{semi}}\right) - Q_{SS}\left(\frac{1}{C_{ins}} + \frac{1}{C_{semi}}\right). \quad (4.1b)$$

Eq. 4.1a is an approximation of V_{on} and is used here for illustrative purposes. Eq. 4.1a accounts for charge present at the insulator-semiconductor interface (Q_{IT}), free electron charge in the semiconductor layer (Q_{free}), charge present in "bulk" trap states within the semiconductor band gap (Q_{bulk}), and charge present at the back surface (Q_{SS}), which is the surface opposite to the insulator-semiconductor interface. Q_{free} and Q_{bulk} are assumed to be uniform throughout the entire thickness of the semiconductor layer, which allows expansion of these terms to include the effect of t_s, as shown in Eq. 4.1b. The capacitor which is placed in series with C_{ins} in Eqs. 4.1a,b, namely , $C_{semi}/2$ is also a consequence of the assumption that Q_{free} and Q_{bulk} are uniformly distributed throughout the semiconductor layer. In the formulation of these equations, several non-idealities are neglected. The work function difference between the gate and the semiconductor is neglected since

this difference is predictable, is not a source of device instability, and its value is small in comparison to other contributions to V_{on}. Additionally, the fixed oxide charge, mobile ion charge, and oxide trapped charge within the insulator are neglected.

Finally, note that a distinction is drawn between interface and surface states in Eqs. 4.1a,b. While interface and surface states are commonly used as synonymous terms throughout device physics research, these terms are used here to account for two distinct types of states, located either at the insulator-semiconductor interface or at the back surface, respectively. This naming convention helps clarify discussions throughout this dissertation.

Now, consider two cases, one in which a TFT exhibits a positive turn-on voltage and one in which a TFT exhibits a negative turn-on voltage. In the case of a positive turn-on voltage, there is a substantial unfilled trap density and V_{on} is the gate voltage required to fill interface states, surface states, or "bulk" trap states within the semiconductor band gap. In the case of a negative turn-on voltage, free electrons are present in the semiconductor prior to application of a gate voltage, so that V_{on} is the gate voltage required to deplete these carriers.

With the origin of V_{on} established, now return to the original discussion where the $V_{on} - t_s$ characteristic was under consideration. Revisiting Fig. 4.16b, V_{on} decreases with increasing thickness for TFTs annealed at 175 °C (in air and N_2). Since V_{on} is a large, positive value for the $\sim$10 nm devices (175 °C), it is likely dominated by interface and/or surface states. As t_s increases, the relative influence of the "bulk" IGZO region increases while the effect of interface and surface states decreases, resulting in a concomitant re-

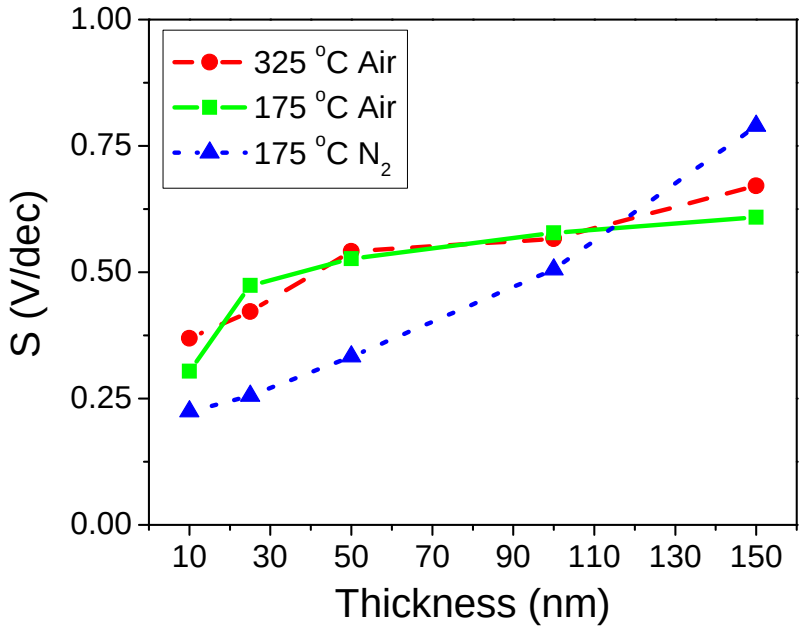


Figure 4.17: The subthreshold swing, *S*, as a function of semiconductor thickness for IGZO-based TFTs. The IGZO layer is rf sputtered at a power of 125 W, a processing pressure of 5 mTorr in Ar/O_2 (0.05 mTorr O_2 partial pressure), and a 10 cm target-to-substrate distance. Additionally, these TFTs are subjected to different post-deposition annealing treatments: 175 °C in N_2, 175 and 325 °C in air.

duction in V_{on}. This reduction in V_{on} with increasing t_s is evident from an evaluation Eq. 4.1b under the assumption that Q_{IT} and Q_{SS} are both constant for all semiconductor thicknesses. Alternatively, a reduction in V_{on} with increasing t_s could arise from a reduced surface state effect as t_s increases (since the back surface moves away from the accumulation channel as t_s increases). A similar trend, where V_{on} decreases with increasing t_s, is observed in ZIO-based and a-Si:H TFTs. [112, 161]

Figure 4.17 shows the subthreshold swing, *S*, as a function of t_s. There is significant deterioration (increase) in *S* with increasing t_s for all annealing treatments. This

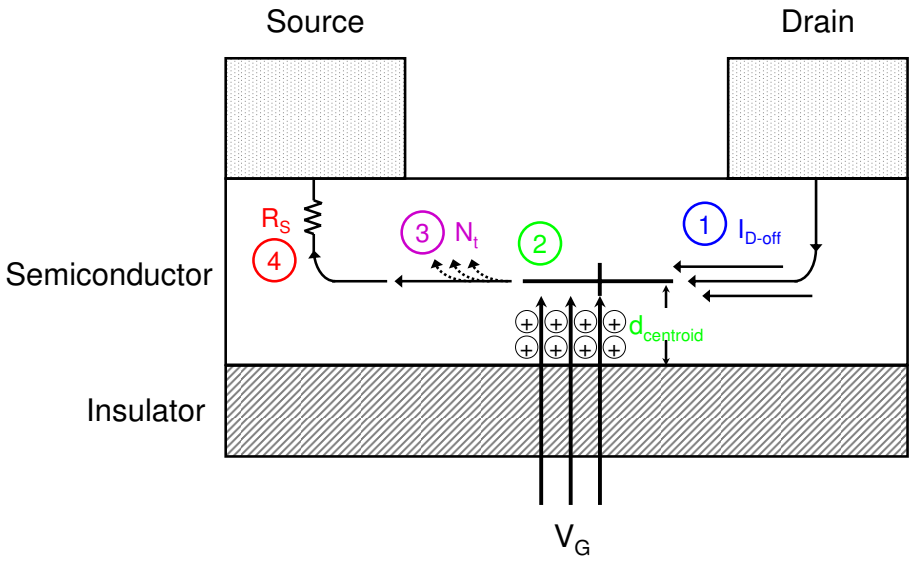


Figure 4.18: Depiction of several possible mechanisms for degradation of the subthreshold swing, S, with increasing semiconductor thickness. These mechanisms are (1) an increase in I_{D-off}, (2) movement of $d_{centroid}$ away from the insulator-semiconductor interface, (3) an increase in the sheet trap density, N_t, and (4) an increase in series resistance, R_S.

degradation in S is likely due to a combination of effects; these effects are depicted in Fig. 4.18 and are discussed below.

The first mechanism of S degradation, as identified in Fig. 4.18, is an increase in the off current (I_{D-off}) with increasing t_s. The second possible mechanism of S degradation is movement of the charge centroid of the induced accumulation layer away from the insulator-semiconductor interface as t_s increases. Other possible mechanisms of S degradation are an increase in the sheet trap density, N_t, and an increase in the series resistance, R_S.

I_{D-off} typically increases with increasing t_s. Neglecting the effect of band bending at the back surface of the semiconductor, I_{D-off} is approximated as, [163]

$$I_{D-off} \simeq \frac{\sigma_D t_s W V_{DS}}{L}, \tag{4.2}$$

where σ_D is the dark conductivity of the semiconductor layer. In practice, I_{D-off} can be difficult to measure since gate insulator leakage can obscure the measurement. For IGZO-based TFTs subjected to a 175 °C anneal in N_2, $I_{D-off} \simeq 5 \times 10^{-11}$ and 2×10^{-10} A for TFTs with t_s = 10 and 150 nm, respectively.

The manner in which the aforementioned increase in I_{D-off} leads to an increase in S is discussed here. An increase in I_{D-off} obscures the effect of gate-induced current since a larger fraction of the total drain current arises from I_{D-off} (the total drain current is the sum of the off current and gate-induced current, $I_D = I_{D-off} + I_{D-ind}(V_{GS})$). Note that a similar mechanism is observed in ZTO-based TFTs, where excess carriers in depletion-mode TFTs degrade the subthreshold swing. [109] Now, consider a numerical example, as this illustrates how S is reduced by I_{D-off}. A modified subthreshold swing equation including I_{D-off} is given as,

$$S = \frac{V_{GS2} - V_{GS1}}{\log 10(I_{D-off} + I_{D-ind}(V_{GS2})) - \log 10(I_{D-off} + I_{D-ind}(V_{GS1}))}. \tag{4.3}$$

For this example, I_{D-ind} is 1×10^{-10} and 5×10^{-10} A for V_{GS} values of 0.5 and 1.0 V, respectively. When $I_{D-off} = 5 \times 10^{-11}$ A, then $S \simeq 0.89$ V/dec. If I_{D-off} is increased to 2x10^{-10} A, S increases to ∼1.36 V/dec.

Now, consider the second possible mechanism of S degradation, movement of the charge centroid of the induced accumulation layer away from the insulator-semiconductor

interface. If $d_{centroid}$ (the distance between the charge centroid and insulator-semiconductor interface) increases, the effect of the gate field is "screened" by the semiconductor. In other words, when $d_{centroid} > 0$, a semiconductor capacitance, $C_S = \varepsilon_s / d_{centroid}$, is inserted in series with the gate insulator capacitance and reduces the effective capacitance that establishes the channel. As the thickness of the semiconductor increases, it is possible for $d_{centroid}$ to increase, reducing the effective capacitance, and consequently, leading to an increase in S.

Finally, consider the third and fourth mechanisms of S degradation (as identified in Fig. 4.18), an increase in the sheet trap density, N_t, and an increase in the series resistance, R_S. If the channel layer trap density, n_t, is uniform across the entire thickness of the semiconductor, then N_t is proportional to semiconductor thickness ($N_t = n_t * t_s$), which leads to an increase in N_t for a thicker film. An increase in R_S can be caused by the increased distance between the source and induced channel as t_s is increased. While this distance is much shorter than the channel length, manifestation of series resistance may be more likely in this region since the resistivity here is much larger than in the induced channel. However, it is important to note that this mechanism is identified here to consider all possibilities, but is thought to be an unlikely source of S degradation for the shadow mask patterned devices under consideration in which the gate-source and gate-drain overlap regions are each $\sim$300 μm.

Revisiting the subthreshold swing trend observed in Fig. 4.17, where S degrades with increasing t_s, it is important to note that a similar trend is also seen in ZIO-based TFTs. [112] However, this trend differs from that observed in a-Si:H TFTs presented

by Martin *et al*., where a decrease in S is observed with t_s. [161] The degradation in S observed by Barquinha *et al*. may be related to the behavior of I_{D-off}, which is found to increase with increasing t_s. The improvement in S observed by Martin *et al*. is attributed to an improvement in the quality of the deposited semiconductor layer with increasing t_s. It is also important to note that the semiconductor thickness does not affect I_{D-off} for the TFTs presented by Martin *et al*.

4.4 Conclusions

Electrical characteristics for IGO, ZTO, and IGZO-based TFTs are presented. Additionally, the effects of several experimental variables are investigated. Oxygen partial pressure is found to have a profound effect on the electrical performance of each material. Table 4.2 highlights the effect of O_2 partial pressure on each material; note that V_{on} increases and μ_{inc} decreases with increasing oxygen partial pressure. Another important point is that these electrical characteristics can be strongly affected by the extended pre-sputtering procedure when the sputter target is first placed in the vacuum chamber, as discussed in Sec. 4.2.1.1.

In general, experimental variables (such as rf power and O_2 partial pressure) have the greatest influence at lower post-deposition anneal temperatures ($\leq$400 °C). At higher temperatures ($>$400 °C), the annealing treatment dominates device performance and minimizes the effect of deposition process variables.

Table 4.2: Electrical characteristics for TFTs sputtered in Ar/O_2 at a processing pressure of 5 mTorr with several oxygen partial pressures (O_2 PP). The annealing temperature for each material set is identified in the column heading.

IGO - 300 °C			ZTO - 275 °C			IGZO - 400 °C		
O_2 PP (mTorr)	V_{on} (V)	μ_{inc} (cm^2/V-s)	O_2 PP (mTorr)	V_{on} (V)	μ_{inc} (cm^2/V-s)	O_2 PP (mTorr)	V_{on} (V)	μ_{inc} (cm^2/V-s)
0.0	-12.8	15.6	0.025	-1.0	12.4	0.0	-9.0	16.1
0.25	0	11.6	0.050	0.0	9.4	0.25	-4.0	15.7
0.50	0.1	0.3	0.075	1.5	6.5	0.50	-1.0	11.5

5. OXIDE SEMICONDUCTOR-BASED TFTS: INTEGRATION ISSUES

This chapter discusses integration-related issues for oxide semiconductor-based TFTs, including TFT stability and passivation. First, stability of devices processed at low temperature is presented. This provides a valuable benchmark from a materials exploration and circuit integration viewpoint. Next, IGZO-based TFTs are used as a test vehicle to identify experimental parameters which influence TFT stability. Finally, staggered bottom-gate TFTs are passivated with SU-8, an organic photoresist. Successful passivation of the oxide semiconductor surface is crucial for vertical integration in complex applications and mechanical/chemical protection of devices.

5.1 Stability of low-temperature oxide semiconductor-based TFTs

A study of the stability of ZTO and IGZO-based TFTs annealed at 175 °C are presented here. The annealing temperature is restricted with the intention of transferring these deposition processes to plastic substrates (e.g. polyethylene naphthalate) in the future.

5.1.1 ZTO-based TFTs

Figure 5.1 shows bias stress testing results for a ZTO-based TFT that is subjected to a 175 °C post-deposition anneal in N_2. For the bias stress test, I_D is monitored while applying a constant voltage bias of $V_{DS} = V_{GS} = 30$ V for 1000 minutes. This device exhibits $\sim$55% current loss throughout the duration of the testing period. The corre-

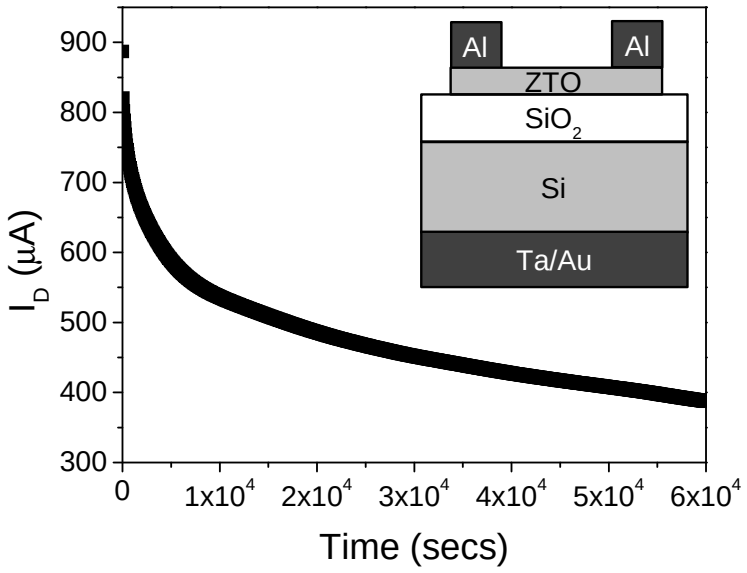


Figure 5.1: (a) I_D as a function of bias stress time for a ZTO-based TFT; this test employs a constant voltage bias of $V_{DS} = V_{GS} = 30$ V. (Inset) Staggered bottom-gate device structure. ZTO deposition employs a rf power of 75 W, an Ar/O_2 processing pressure of 5 mTorr with 0.050 mTorr oxygen partial pressure, and a 10 cm target-to-substrate distance. Additionally, the ZTO layer is subjected to a 175 °C post-deposition anneal in N_2.

sponding electrical characteristics for this device are shown in Sec. 4.2.1. Note that a cross-section (not to scale) of the device structure is shown in the inset of Fig. 5.1 and that the ZTO layer is fabricated using rf sputtering with a power of 75 W (2 in target), an Ar/O_2 processing pressure of 5 mTorr with 0.050 mTorr oxygen partial pressure, and a 10 cm target-to-substrate distance.

Pre-stress and post-stress electrical characteristics are shown in Fig. 5.2. Figure 5.2a shows the $\log(I_D)-V_{GS}$ characteristics. Due to bias stress testing, this TFT exhibits a positive V_{on} shift of $\sim$6 V. Figure 5.2b, compares the pre-stress and post-stress mobility characteristics, which show minimal change. Note that the x-axis is $V_{GS} - V_{on}$ to account for the shift in V_{on} during testing. This shift in V_{on} is attributed to electron

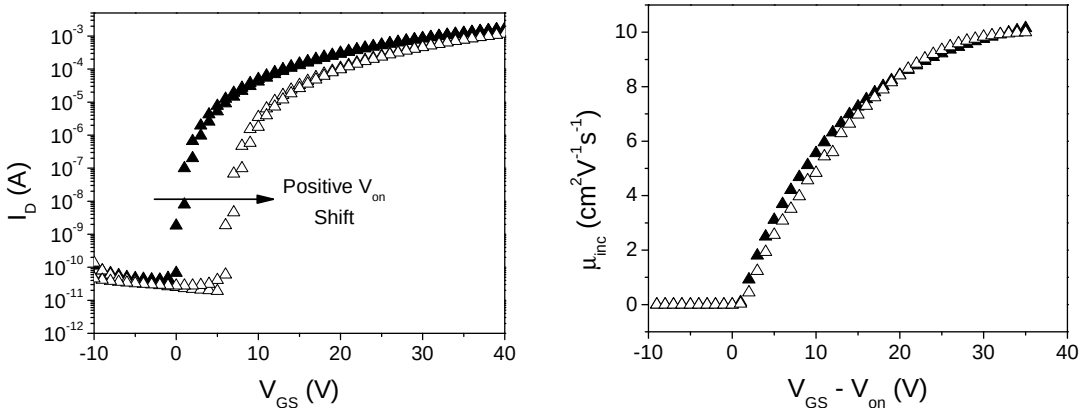
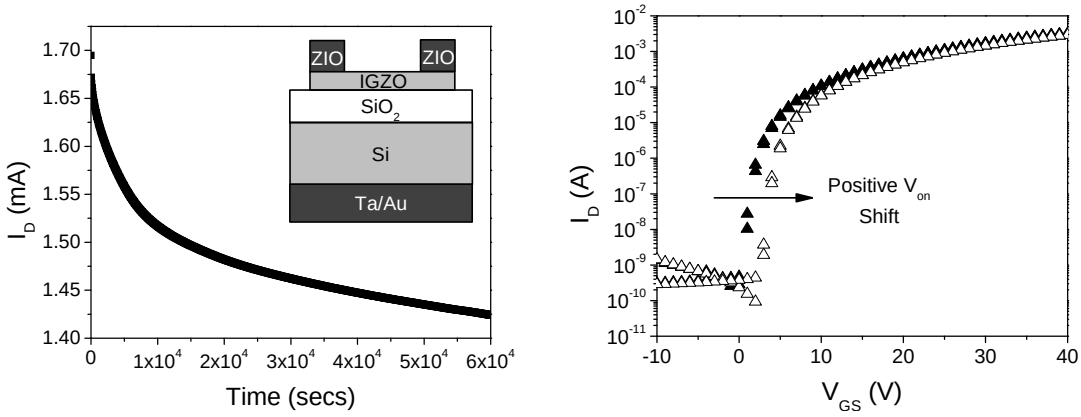


Figure 5.2: (a) Log(I_D)−V_{GS} characteristics obtained at V_{DS} = 30 V before (solid triangles) and after (open triangles) the bias stress stability test. A positive turn-on voltage shift of ∼6 V is exhibited by this device. (b) $\mu_{inc} - V_{GS}$-V_{on} characteristics obtained at V_{DS} = 1 V before (solid triangles) and after (open triangles) the bias stress test.

trapping in interface states (at the insulator-semiconductor interface), in surface states (at the back surface, which is the surface opposite to the insulator-semiconductor interface), and/or in "bulk" traps within the semiconductor band gap. Moreover, the current loss observed in Fig. 5.1 is also attributed to electron trapping and the concomitant shift in V_{on}.

Previous researchers have shown that the stability of oxide semiconductor-based TFTs improves with increasing anneal temperature. [164] Although not shown here, it is important to note that ZTO-based TFTs which are subjected to a 300 °C post-deposition anneal exhibit excellent bias stress stability, with nearly no current loss or V_{on} shift when subjected to the 1000 minute constant voltage bias stress test.



(a) (b)

Figure 5.3: (a) I_D as a function of bias stress time for an IGZO-based TFT; this test employs a constant voltage bias of $V_{DS} = V_{GS} = 30$ V. (Inset) Staggered bottom-gate device structure. (b) Log(I_D)$-V_{GS}$ characteristics obtained at V_{DS} = 30 V before (solid triangles) and after (open triangles) the bias stress stability test. A positive turn-on voltage shift of $\sim$2 V is exhibited by this device.

5.1.2 IGZO-based TFTs

Figure 5.3a shows bias stress testing results for an IGZO-based TFT that is subjected to a 175 °C post-deposition anneal. For the bias stress test, I_D is monitored while applying a constant voltage bias of $V_{DS} = V_{GS} = 30$ V for 1000 minutes. This device exhibits excellent stability, with less than 20% current loss throughout the duration of the testing period. The corresponding electrical characteristics for this device are shown in Sec. 4.3.1. Note that a cross-section (not to scale) of the device structure is shown in the inset of Fig. 5.3a and that the IGZO deposition employs a rf power of 75 W (3 in target), a processing pressure of 5 mTorr in pure Ar, and a 10 cm target-to-substrate distance.

Figure 5.3b shows the pre-stress and post-stress log(I_D)$-V_{GS}$ characteristics. Due to the bias stress testing, this TFT exhibits a positive V_{on} shift of $\sim$2 V. The shift in V_{on} is attributed to electron trapping in interface states, surface states, and/or "bulk" traps

within the semiconductor band gap. Moreover, the current loss observed in Fig. 5.3a is also attributed to electron trapping and the concomitant shift in V_{on}. Although not shown here, the mobility characteristics exhibit minimal change due to stress testing.

5.2 Oxide semiconductor-based TFT stability: IGZO-based TFTs

Here, IGZO-based TFTs are used as a test vehicle to investigate the influence of two device parameters (V_{on} and semiconductor thickness) on device stability. A similar staggered bottom-gate test structure is used to investigate both parameters. The structure employs a p-doped (boron, $\sim 3 \times 10^{16}$ cm^{-3}) 10×15 mm^2 Si substrate with a SiO_2 (100 nm thick) gate dielectric layer formed via thermal oxidation. The p-doped Si acts as both the gate and substrate. Ta/Au (10/300 nm thick, respectively) are deposited onto the backside of the Si substrate to form the gate contact. The IGZO deposition, which employs a 3 in target (purchased from Cerac, Inc.), is modified to control V_{on} and the semiconductor thickness. To control V_{on}, the oxygen partial pressure of the sputter ambient is varied (between 0.20 and 0 mTorr in increments of 0.05 mTorr). Other deposition parameters for this set of IGZO-based devices are a rf power of 125 W, an Ar/O_2 processing pressure of 5 mTorr, and a target-to-substrate distance of 10 cm. To control the semiconductor thickness, the deposition time is varied to attain the appropriate thickness. Other deposition parameters for this set of IGZO-based devices are a rf power of 125 W, an Ar/O_2 processing pressure of 5 mTorr, an oxygen partial pressure of 0.05 mTorr and a target-to-substrate distance of 10 cm. The post-deposition annealing treatment for the

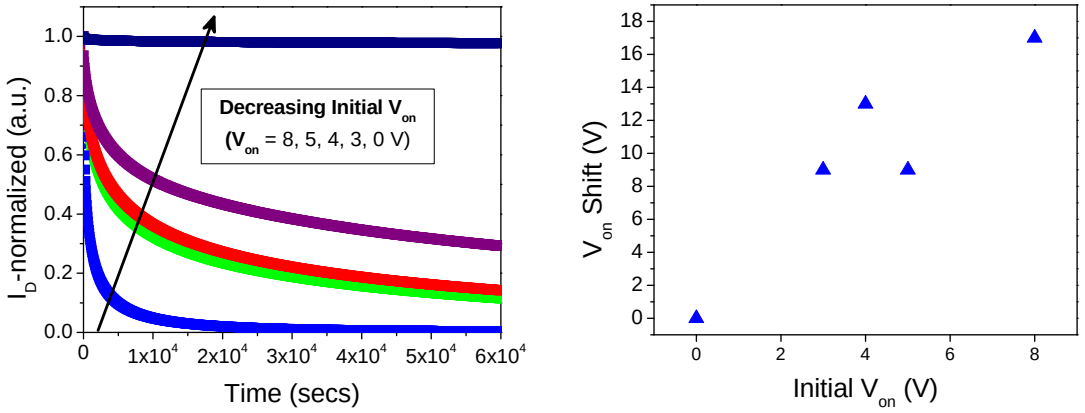
IGZO layer differs for the two experiments and is identified with presented data. For the source and drain electrodes (typically ∼200 nm thick), ITO is employed.

Before proceeding, it is important to note that when evaluating trends for an experiment, all associated device characterization should employ identical testing conditions. This aspect is crucial since testing conditions (such as the start voltage, step size of the sweep voltage, hold and/or delay times) can significantly affect V_{on} and the observed hysteresis.

5.2.1 Effects of V_{on} on bias stress stability

Before considering the effect of V_{on} on bias stress stability of IGZO-based TFTs, consider the influences which determine its value. Assuming consistent testing conditions, V_{on} is established by the work function difference between the gate and the semiconductor, oxide charges related to defects in the insulator and/or insulator-semiconductor interface, charge present in "bulk" trap states within the semiconductor band gap, the sheet concentration of free carriers present in the semiconductor prior to application of gate voltage, N_{free}. For oxide semiconductor-based TFTs, N_{free} can be controlled by varying the oxygen partial pressure in the sputter deposition ambient, as shown in Chapter 4. The work function difference between the gate and the semiconductor is neglected since this difference is predictable, is not a source of device instability, and its value is small in comparison to other contributions to V_{on}.

Now, consider two cases for oxide-semiconductor TFTs. In the first case, the turn-on voltage of an oxide-semiconductor based TFT is positive. Here, V_{on} is the voltage



(a) (b)

Figure 5.4: (a) $I_D - normalized$ as a function of bias stress time for several devices with varying values of V_{on}. A constant voltage bias of $V_{DS} = V_{GS} = 30$ V is employed. (b) V_{on} shift (the difference between V_{on} after the bias stress stability test and the initial value of V_{on}) as a function of initial V_{on}. These devices are sputtered at 125 W in Ar/O_2 at a processing pressure of 5 mTorr and subjected to a 300 °C post-deposition anneal in air. Oxygen partial pressure of the sputter ambient is varied between 0.20 and 0 mTorr in steps of 0.05 mTorr to control V_{on}. V_{on} measurement employs a delay time, hold time, and V_{GS} step size of 200 ms, 500 ms, and 1 V, respectively.

required to fill interface states, surface states, and/or "bulk" traps within the semiconductor band gap. In the second case, the turn-on voltage of a TFT is negative. Here, V_{on} is the voltage required to deplete carriers that are already present in the semiconductor prior to the application of a voltage gate voltage.

Figure 5.4a shows I_D-normalized as a function of bias stress time for several devices with varying values of V_{on}. These devices are sputtered at 125 W in Ar/O_2 at a processing pressure of 5 mTorr and subjected to a 300 °C post-deposition anneal in air. Oxygen partial pressure of the sputter ambient is varied between 0.20 and 0 mTorr in steps of 0.05 mTorr to control V_{on}. Several features of Fig. 5.4a are noteworthy. First, note that the bias stress stability improves as the initial value of V_{on} decreases. Based on previously identified parameters which affect V_{on}, this trend is not surprising, since devices with

large positive V_{on} values correspond to devices which are strongly influenced by trapping in interface states and/or "bulk" traps in the semiconductor band gap. Additionally, note that the device where $V_{on} = 0$ V (which corresponds to the device sputtered in pure Ar) is extremely stable, as negligible current loss is observed throughout the duration of the testing period.

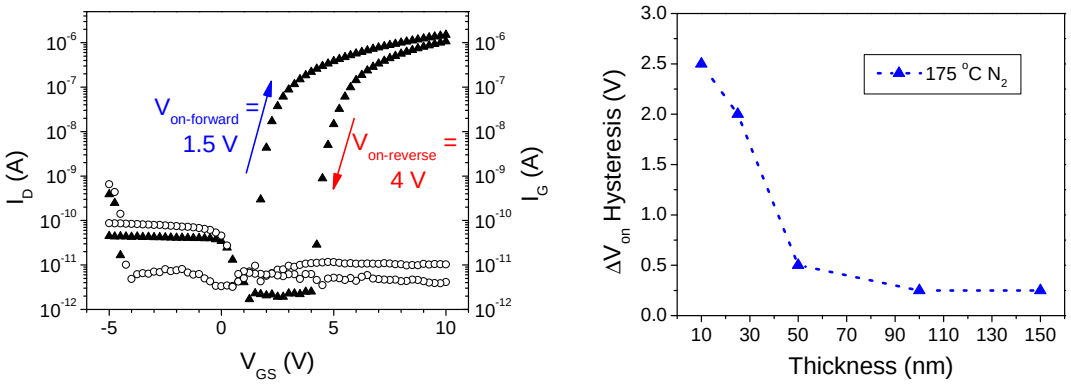
Another measure of stability is the V_{on} shift. This value is determined by the difference between V_{on} after the bias stress stability test and the initial value of V_{on}. Figure 5.4b shows V_{on} shift as a function of initial V_{on}. The general trend is in agreement with the normalized drain current measurements shown in Fig. 5.4a, where the stability improves as the initial value of V_{on} decreases.

5.2.2 Influence of semiconductor thickness

The corresponding electrical characteristics for TFTs used in this semiconductor thickness experiment are shown in Sec. 4.3.4.

5.2.2.1 Bias stress stability

Figure 5.5a shows the $\log(I_D)-V_{GS}$ and $\log(I_G)-V_{GS}$ characteristics obtained at V_{DS} = 100 mV for an IGZO-based TFT which is subjected to a 175 °C in N_2 and employs an $\sim$10 nm-thick semiconductor layer. These characteristics are obtained using a "double sweep" methodology with the arrows indicating the direction of the sweeping voltage. From the forward and reverse directions, V_{on} is measured as 1.5 and 4 V, respectively. The difference in these values is used to characterize the hysteresis and is designated, ΔV_{on}-hysteresis, which is 2.5 V for this device. The observed hysteresis is in the "clock-

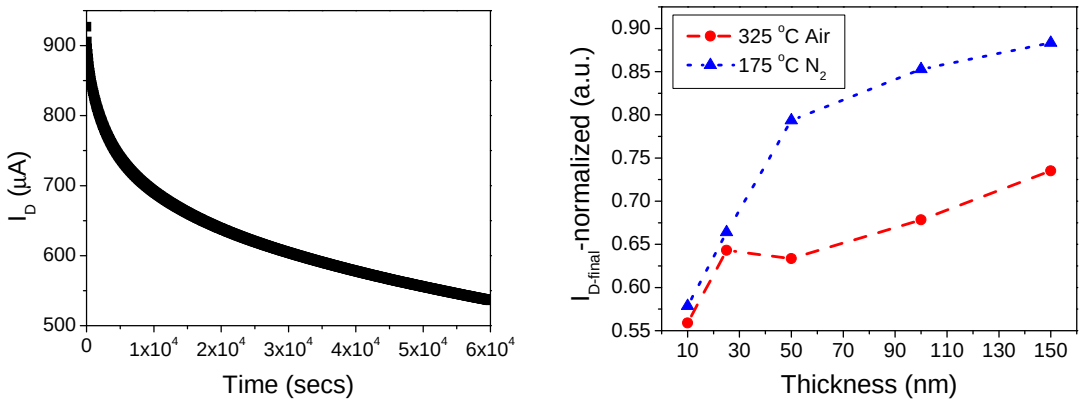


(a) (b)

Figure 5.5: (a) Log(I_D) (solid triangles) and log(I_G) (open circles) as a function of V_{GS} with V_{DS} = 100 mV for an IGZO-based TFT with a 10 nm-thick semiconductor layer. The arrows indicate the direction of the sweeping voltage. From the forward and reverse directions, V_{on} is 1.5 and 4 V, respectively. The difference in these values is used to characterize the hysteresis and is designated, ΔV_{on}-hysteresis, which is 2.5 V for this device. (b) ΔV_{on}-hysteresis as a function of semiconductor thickness. Device characterization associated with this trend employ a delay time, hold time, and V_{GS} step size of 200 ms, 500 ms, and 250 mV, respectively.

wise" direction, concomitant with electron trapping in interface states and/or "bulk" trap states within the semiconductor band gap. Note that this hysteresis analysis uses the first measurement following device fabrication or after an extended rest period (greater than 1 week). Use of the first measurement is of particular importance since subsequent measurements typically exhibit drastically reduced (by at least an order of magnitude) hysteresis, making hysteresis analysis more difficult.

Figure 5.5b shows ΔV_{on}-hysteresis as a function of semiconductor thickness. First, note that all devices shown in Fig. 5.5b exhibit clockwise hysteresis, which is evident from the positive values of ΔV_{on}-hysteresis. Additionally, note that hysteresis reduces as the semiconductor thickness is increased. For an ultrathin semiconductor layer ($t_s \leq 25$ nm), conduction is confined near the insulator-semiconductor interface, where interface states



(a) (b)

Figure 5.6: (a) I_D as a function of bias stress time for an IGZO-based TFT which is subjected to a 175 °C anneal and which employs a semiconductor layer thickness of 10 nm. A constant voltage bias of $V_{DS} = V_{GS} = 30$ V is employed. The normalized value of $I_{D-final}$ (i.e., $I_{D-final}/I_{D0}$) is 0.578 for this device. (b) Normalized value of $I_{D-final}$ as a function of semiconductor thickness.

and/or a higher concentration of defects are expected. As t_s is increased, the influence of the interface region is reduced while the influence of the "bulk" region increases, leading to a decrease in hysteresis in thicker films. Additionally, an ultrathin semiconductor layer can be non-continuous and/or inhomogeneous as a consequence of the nucleation and island formation mechanism associated with the growth of a thin film, leading to increased hysteresis for thinner films.

Figure 5.6a shows bias stress testing results for an IGZO-based TFT which is subjected to a 175 °C post-deposition anneal in N_2 and employs a semiconductor layer thickness of 10 nm. The stress testing conditions are a constant bias of $V_{DS} = V_{GS} = 30$ V for 1000 minutes. The normalized value of $I_{D-final}$ (i.e., $I_{D-final}/I_{D0}$) is useful for comparing multiple devices and is $\sim$0.58 for this device. Although not shown here, this device exhibits a V_{on} shift of $\sim$4.75 V.

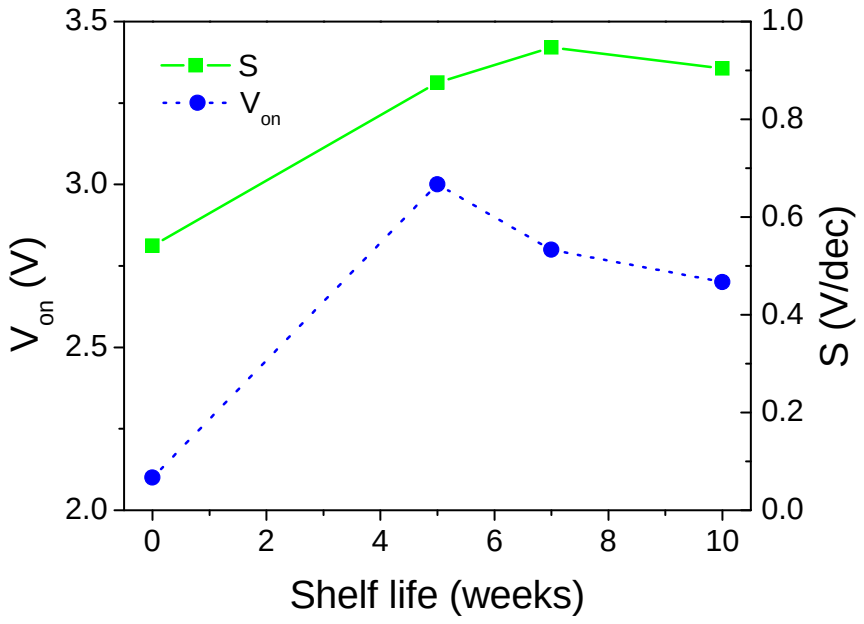


Figure 5.7: V_{on} and subthreshold swing, S, as a function of shelf life for an IGZO-based TFT that employs a ∼50 nm semiconductor thickness and a 325 °C post-deposition annealing treatment in air.

Figure 5.6b shows the normalized value of $I_{D-final}$ as a function of semiconductor thickness for devices annealed at 175 °C in N_2 and 325 °C in air. Note that the device shown in Fig. 5.6a is represented by the leftmost triangle in Fig. 5.6b. Other devices represented in Fig. 5.6b behave similarly to the device characterized in Fig. 5.6a, where I_D reduces with bias stress time and V_{on} shifts to larger values. For both annealing treatments, bias stress stability improves with increasing thickness. This is not surprising, as the same factors which affect hysteresis can also affect bias stress stability. Moreover, there is an inverse correlation between hysteresis and bias stress stability, i.e., devices which exhibit minimal hysteresis on the first measurement also exhibit excellent bias stress stability.

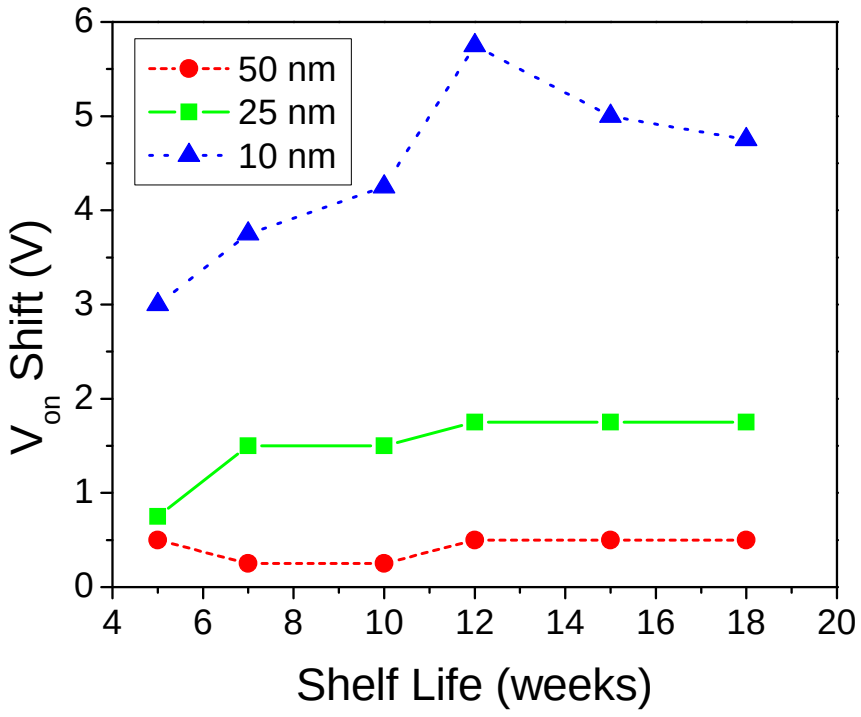


Figure 5.8: V_{on} shift as a function of shelf life for IGZO-based TFTs which employ different semiconductor thicknesses: 10 , 25, and 50 nm. These TFTs are subjected to a 175 °C post-deposition anneal in N_2. Note that V_{on} shift is calculated using the original, Week 0 value of V_{on}.

5.2.2.2 Shelf life stability

Figure 5.7 shows V_{on} and subthreshold swing, S, as a function of shelf life for an IGZO-based TFT that employs a ∼50 nm semiconductor thickness and a 325 °C post-deposition annealing treatment in air. As shown in Fig. 5.7, V_{on} and S initially increase, then decrease back towards their original values. Although not shown here, it is important to note that the channel mobility does not exhibit appreciable change with shelf life.

Figure 5.8 shows V_{on} shift as a function of shelf life for IGZO-based TFTs which employ a post-deposition anneal of 175 °C in N_2 and different semiconductor thicknesses.

For $t_s \leq 50$ nm, shelf life stability improves with increasing semiconductor thickness. Additionally, note that the device in which $t_s = 50$ nm exhibits excellent shelf life stability, with a maximum V_{on} shift of only 0.5 V. For $t_s > 50$ nm, the shelf life stability is generally excellent as well, with most devices exhibiting V_{on} shifts lower than 1 V.

Finally, note that the different shelf life characteristics observed for oxide-semiconductor-based TFTs are embodied in Fig. 5.8. The first characteristic corresponds to the device in which $t_s = 10$ nm; here, V_{on} increases, then decreases back towards its original value. The second characteristic corresponds to the device in which $t_s = 25$ nm; here V_{on} initially increases, then saturates at an elevated value. The final characteristic corresponds to the device in which $t_s = 50$ nm; here a negligible shift in V_{on} is observed.

5.3 Passivation with SU-8

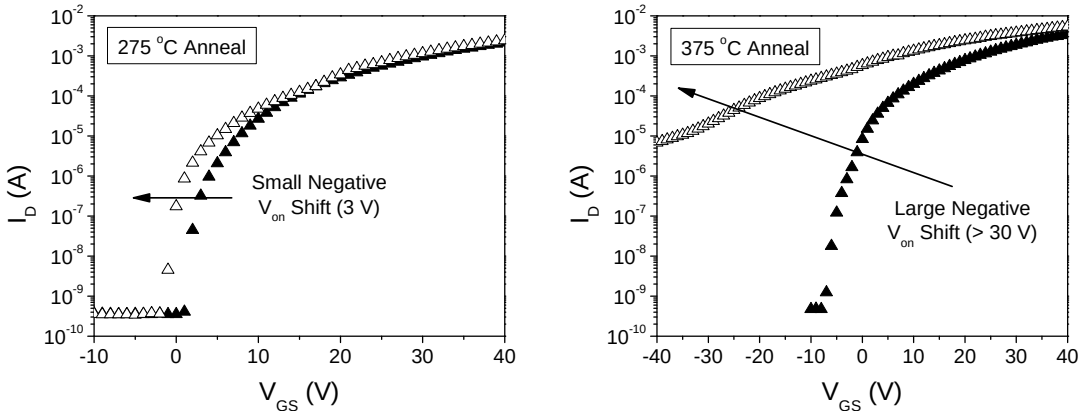
Here, SU-8 passivation is explored for IGO, ZTO, and IGZO-based TFTs using a staggered bottom-gate test structure. The structure employs a p-doped (boron, $\sim 3 \times 10^{16}$ cm^{-3}) 10×15 mm^2 Si substrate with a SiO_2 (100 nm thick) gate dielectric layer formed via thermal oxidation. The p-doped Si acts as both the gate and substrate. Ta/Au (10/300 nm thick, respectively) are deposited on the backside of the Si substrate to form the gate contact. The channel layer deposition parameters and post-deposition annealing ambient employed are given in Table 5.1. Note that the annealing temperature is varied between 175 and 375 °C in 100 °C steps. For the source and drain electrodes (typically ∼200 nm thick), ITO is employed. Finally, SU-8 is deposited atop the TFTs as a pas-

Table 5.1: Deposition parameters and post-deposition annealing ambient employed for several semiconductor materials used to investigate SU-8 passivation. Note that O_2 PP and distance are the oxygen partial pressure and target-to-substrate distance, respectively.

Material	Target Diameter	Power	Pressure	O_2 PP	Distance	Anneal Ambient
IGO	2”	75 W	5 mTorr	0.25 mTorr	10 cm	N_2
ZTO-A	2”	75 W	5 mTorr	0.5 mTorr	10 cm	Air
ZTO-B	2”	75 W	5 mTorr	0.5 mTorr	10 cm	N_2
IGZO	3”	125 W	5 mTorr	0.05 mTorr	10 cm	N_2

sivation layer; material properties of SU-8 and details of SU-8 processing are discussed below.

SU-8, a negative tone epoxy-based photoresist, is commonly used in the manufacture of micro-electro-mechanical systems (MEMS). [165, 166] Several properties of SU-8 are attractive for MEMS applications, including its chemical stability (SU-8 is extremely difficult to remove once the polymer has been cross-linked), its high photosensitivity (allowing fabrication of structures with high aspect ratios), and its ease of fabrication. One of the largest applications of SU-8 involves its use in inkjet printhead nozzles. For this dissertation, SU-8 is employed as a passivation layer, motivated by its ease of fabrication and its chemical stability. However, one drawback of SU-8 for this application is its low mechanical strength. The Young’s modulus of SU-8 is $\sim$4.4 GPa, which is considerably higher than other resists, but approximately 40 times lower than that of Si.



(a) (b)

Figure 5.9: Log(I_D)−V_{GS} characteristics obtained at V_{DS} = 30 V for an IGZO-based TFT (solid triangles) with an air-exposed surface and an IGZO-based TFT with a SU-8 passivation layer (open triangles). These TFTs are subjected to (a) 275 or (b) 375 °C post-deposition anneals prior to SU-8 passivation.

The SU-8 passivation layer is deposited atop staggered bottom-gate TFTs and is the final step in the device fabrication process. For SU-8 deposition, the substrate is first coated with SU-8 by spin-coating (3000 rpm for 30 seconds). The layer is then subjected to a two-step soft bake (65 and 95 °C for 1 minute each) to evaporate solvents in the layer and to densify the film. Next, the film is exposed to UV light and subjected to a post-exposure bake, which cross-links exposed regions of the film. The pattern is then developed. Finally, the patterned SU-8 is subjected to a hard bake (150 °C) to further cross-link the film. Additional information regarding SU-8 processing is available elsewhere. [167]

5.3.1 Effects of SU-8 passivation

Figure 5.9a compares log(I_D)−V_{GS} characteristics for an IGZO-based TFT with an air-exposed surface (i.e., an unpassivated TFT) and an IGZO-based TFT with a SU-

8 passivation layer. Both TFTs are fabricated on the same substrate and the channel layers are subjected to a 275 °C anneal prior to SU-8 passivation. Making comparisons between devices which are fabricated on the same substrate ensures that devices being compared experience identical processing conditions. For the TFTs shown in Fig. 5.9a, SU-8 passivation causes a small negative shift in V_{on} of $\sim$3 V. Figure 5.9b compares $\log(I_D)-V_{GS}$ characteristics for unpassivated and passivated IGZO-based TFTs in which the channel layers are subjected to a 375 °C anneal. In this case, SU-8 passivation causes a large negative shift in V_{on} that is $>$ 30 V and is detrimental to device performance. Although not shown here, the channel mobility is similar for unpassivated and passivated devices.

Before discussing differences in the effect of device passivation for the IGZO-based TFTs shown in Fig. 5.9, it is useful to review the effect of passivation for a larger set of devices which employ other semiconductor materials and annealing temperatures. Table 5.2 gives electrical characteristics for unpassivated and passivated IGO, ZTO, and IGZO-based TFTs. For all cases shown in Table 5.2, SU-8 passivation causes a negative shift in V_{on}. A similar effect has been observed in the passivation of ZTO-based TFTs with SiO_x by Hong *et al*. [168]

To understand the origin of this negative V_{on} shift, first consider the behavior of an air-exposed ZnO surface [149, 150] and assume that the surfaces of the multicomponent oxide semiconductors explored in this dissertation behave similarly. Oxygen chemisorbs onto an air-exposed ZnO surface, creating acceptor-like surface states. Filling of these surface states by conduction band electrons results in a depletion of the ZnO surface.

Table 5.2: Electrical characteristics of unpassivated and passivated IGO ($InGaO_3$), ZTO ($ZnSnO_3$), and IGZO-based ($InGaZnO_4$) TFTs. Recall that the ZTO-A and ZTO-B materials are subjected to post-deposition annealing treatments in air and N_2, respectively. Note that "Temp" is the post-deposition annealing temperature and that the data shown here represents the average of at least 3 devices.

Material	Temp	Unpassivated			SU-8 Passivated		
		V_{on}	μ_{inc}	μ_{avg}	V_{on}	μ_{inc}	μ_{avg}
	(°C)	(V)	(cm^2/V-s)	(cm^2/V-s)	(V)	(cm^2/V-s)	(cm^2/V-s)
IGO	175	5.5	0.35	0.21	2	0.35	0.24
	275	0	13.1	9.9	-2.7	13.9	9.9
	375	-11.3	15.7	11.5	<-40	16.3	N/A
ZTO-A (Air)	175	28	0.002	0.001	25.6	0.002	0.001
	275	5.7	0.06	0.04	2	0.05	0.04
	375	0	11.9	7.78	-1.33	9.5	5.5
ZTO-B (N_2)	175	<-40	11	N/A	<-40	11	N/A
	275	<-40	15	N/A	<-40	13.6	N/A
	375	-8.3	20.7	17.1	<-40	19.1	N/A
IGZO	175	5	3.7	2.3	3.7	8	6
	275	0.7	9.5	7.1	-2	8.8	6
	375	-8	17.2	12.6	<-40	18.5	N/A

When the surface of ZnO is covered with a passivation layer, the surface depletion layer associated with oxygen chemisorption is eliminated. Instead, the charge associated with the passivation layer and/or interface states determines the electrical state of the surface. In many cases, such as that for SU-8 and SiO_2, positive charge associated with these materials can result in the formation of a surface accumulation layer. This surface accumulation layer leads to a reduction in V_{on}.

Upon further analysis of Table 5.2, it is apparent that the value of V_{on} for the unpassivated TFTs influences the magnitude of the V_{on} shift caused by passivation. When $V_{on} \geq 0$ V for an unpassivated TFT, the corresponding passivated TFT exhibits a small, non-detrimental, negative shift in V_{on}. When V_{on} for an unpassivated TFT is highly negative (i.e., $V_{on} <$ -5 V), the corresponding passivated TFT exhibits a large, detrimental, negative shift in V_{on}. Finally, note that the channel mobility is similar for unpassivated and passivated devices in most cases.

To explore the magnitude of the V_{on} shift caused by passivation, consider equilibrium energy band diagrams near the conduction band of the semiconductor for an air-exposed TFT with a positive and negative value of V_{on}, as shown in Figs. 5.10a and 5.10b, respectively. The associated equilibrium energy band diagrams after SU-8 passivation are also shown. In the case where V_{on} is positive, several features are noteworthy: (i) minimal free electron charge is present in the semiconductor (as represented by the significant distance between E_F and E_C in the "bulk" portion of the semiconductor), (ii) a depletion region is present at the insulator-semiconductor interface (consistent with a positive V_{on}), and (iii) a large portion of bulk trap states, represented by E_T in Fig. 5.10, are unfilled

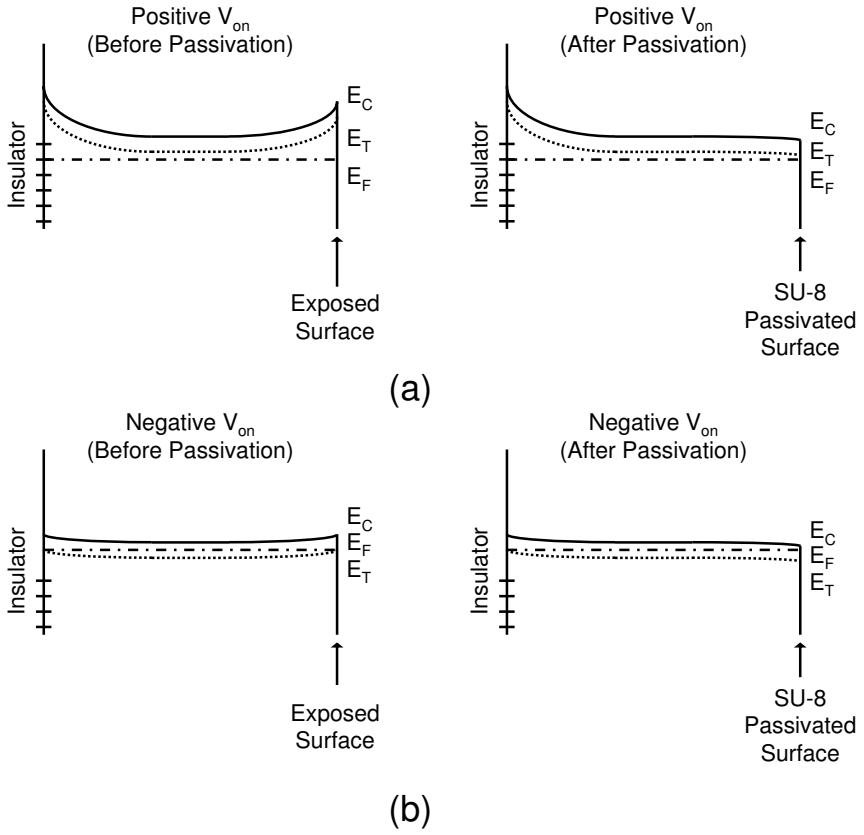


Figure 5.10: Equilibrium energy band diagrams (focusing on the conduction band of the semiconductor) before and after SU-8 passivation for a TFT where (a) V_{on} is positive and (b) V_{on} is negative. The position of the Fermi energy moves with respect to the conduction band for a TFT in which V_{on} is positive ($\sim$0.375 eV below E_C corresponding to a free electron concentration of $\sim 10^{13}$) or negative ($\sim$0.125 eV below E_C corresponding to a free electron concentration of $\sim 10^{17}$). In all cases, a hypothetical "bulk" trap energy, E_T is inserted at the same location ($\sim$0.25 eV below E_C). Additionally, the effect of interface states and oxygen chemisorption at the surface (for the unpassivated case) is included.

(since E_T is above E_F). Passivation primarily affects the semiconductor surface. Before SU-8 passivation, a surface depletion region is present (due to oxygen chemisorption, as previously discussed). After SU-8 passivation, the surface depletion layer is eliminated due to removal of chemisorbed oxygen from the semiconductor surface. Additionally, the positive charge associated with the SU-8 layer results in a weak accumulation layer at the

surface; since the E_C-E_F separation is still relatively large at the surface, this is consistent with a small negative shift in V_{on} after SU-8 passivation.

In the case where V_{on} is negative (Fig. 5.10b), E_F is close to the conduction band (and nearly degenerate) in the "bulk" portion of the semiconductor, indicating a substantial amount of free electron charge is present in the semiconductor and is available for conduction. Here, the insulator-semiconductor interface is slightly depleted, but E_C-E_F is small throughout the entire thickness of semiconductor (consistent with a negative V_{on}). Before SU-8 passivation, a depletion region is present at the surface of the semiconductor (due to oxygen chemisorption). After SU-8 passivation, an accumulation layer is formed at the surface due to positive charge associated with the SU-8 layer. The influence of this accumulation layer is significant since E_F is close to the conduction band in the "bulk" and any further perturbation that reduces E_C-E_F results in a significant increase in the free carrier concentration (since carrier concentration increases exponentially with respect to E_C-E_F/k_BT). With this in mind and the fact that the depletion width under applied gate bias becomes increasing small as carrier concentration increases (shown in Sec. 2.2.1.2, Fig. 2.3), a large negative V_{on} shift after passivation is expected. Finally, comparing the energy band diagrams for the two cases, it should be noted that the magnitude of band bending associated with depletion regions at the interface and surface are much smaller in the case of a negative V_{on} due to abundance of free carriers present here.

Alternatively, consider the charge neutrality relationship at the surface of a passivated TFT, given here as,

$$Q_{pass} + Q_{bulk} + Q_{free} = 0, \tag{5.1}$$

where Q_{pass}, Q_{bulk}, and Q_{free} is the charge associated with the passivation layer itself and the semiconductor-passivation interface, the charge associated with "bulk" trap states, and the charge associated with free carriers, respectively. Rearranging Eq. 5.1 gives,

$$Q_{pass} = -Q_{bulk} - Q_{free}. \tag{5.2}$$

In the case of a positive V_{on}, the positive charge associated with the SU-8 passivation layer is balanced by both free and trapped charge in the semiconductor. The unexpected benefit of electron trapping here, is that it restrains the formation of an accumulation layer, leading to a small negative shift in V_{on} and resulting in successful device passivation. In contrast, for the case of a negative V_{on}, since most bulk trap states are expected to already be filled (i.e., E_T is below E_F), $Q_{bulk} \approx 0$, such that $Q_{pass} \approx -Q_{free}$, giving rise to the formation of an accumulation layer and a large negative shift in V_{on}. In other words, in this case the positive charge associated with the passivation layer is balanced only by free election charge in the semiconductor accumulation layer, resulting in a large V_{on} shift. Revisiting Fig. 5.10 and summarizing in the context of an energy band diagram, the magnitude of the V_{on} shift after SU-8 passivation is related to the position of E_F with respect to both E_C and E_T.

5.4 Conclusions

Integration-related issues for oxide semiconductor-based TFTs are presented. First, the bias stress stability of low-temperature ZTO and IGZO-based TFTs is explored. Next, V_{on} and semiconductor thickness are shown to have a significant influence on bias stress

stability. Specifically, bias stress stability decreases with increasing V_{on} and decreasing semiconductor thickness. Finally, staggered bottom-gate IGO, ZTO, and IGZO-based TFTs are successfully passivated with SU-8. When $V_{on} \geq 0$ V before passivation, device characteristics exhibit minimal change after SU-8 passivation. In contrast, when $V_{on} <$ -5 V before passivation, a large negative shift in V_{on} ($>$ 30 V) occurs after SU-8 passivation.

6. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The focus of the research presented in this dissertation is development of oxide semiconductors for thin-film transistors (TFTs). A variety of oxide semiconductors are currently employed in TFTs. Thus, the research presented utilizes a variety of oxide semiconductors as the TFT channel layer, including indium gallium oxide (IGO), zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO). While the electrical properties of each material are unique, carrier generation in these materials is based on the same principles (i.e., oxygen vacancies and/or metal cation interstitials). With this in mind, the general approach to this research is to broadly identify experimental parameters that influence TFT performance. One such parameter is oxygen partial pressure of the deposition ambient, which is found to have a profound effect on the electrical performance of all of the oxide semiconductors explored.

Advancement of oxide semiconductor-based TFTs requires additional research related to integration issues. Therefore, TFT stability and the effect of channel layer passivation is evaluated. Stability of a TFT impacts circuit design and determines possible applications. Passivation of the oxide semiconductor surface is crucial for vertical integration (which allows for more complex systems) and mechanical/chemical protection of devices.

6.1 Conclusions

1. **Low-temperature TFTs:** The low-temperature device characteristics for IGO, ZTO, and IGZO-based TFTs are highlighted here. For these TFTs, the turn-on voltage (V_{on}) is near 0 V and is controlled by tuning the O_2 partial pressure of the deposition ambient and selecting the appropriate post-deposition annealing ambient (air or N_2) and temperature. IGO-based ($In_{1.33}Ga_{0.67}O_3$) TFTs which are subjected to a 200 °C post-deposition anneal in air exhibit a turn-on voltage of ∼2 V. The incremental mobility (μ_{inc}) and drain current on-to-off ratio (I_D^{on-off}) for these devices are ∼19 $cm^2V^{-1}s^{-1}$ and 3×10^6, respectively. ZTO-based TFTs which are subjected to a 175 °C post-deposition anneal in N_2 exhibit a V_{on}, μ_{inc}, and I_D^{on-off} of ∼-1 V, 9 $cm^2V^{-1}s^{-1}$, and 2×10^7, respectively. IGZO-based TFTs which are subjected to a 175 °C post-deposition anneal in air exhibit a V_{on}, μ_{inc}, and I_D^{on-off} of ∼0 V, 17 $cm^2V^{-1}s^{-1}$, and 7×10^6, respectively.

2. **Effect of O_2 partial pressure:** Oxygen partial pressure of the deposition ambient is found to have a profound effect on the electrical performance of each material. As the oxygen partial pressure decreases, the turn-on voltage decreases while the channel mobility increases. IGO-based TFTs deposited at a pressure of 5 mTorr and annealed at 300 °C exhibit μ_{inc} values of ∼0.3, 11.6, and 15.6 $cm^2V^{-1}s^{-1}$ and V_{on} values of ∼0.1, 0, and -12.8 V for oxygen partial pressures of 0.5, 0.25, and 0 mTorr, respectively. The decrease in V_{on} with decreasing O_2 partial pressure corresponds to an increased density of oxygen vacancies, leading to an increased

free carrier concentration. The increase in μ_{inc} may initially be counterintuitive; in a classic single crystalline semiconductor, such as Si, carrier mobility decreases as carrier concentration increases due to ionized impurity scattering. However, in polycrystalline and amorphous semiconductors (assuming non-degenerate conditions), mobility increases as carrier concentration increases. As carrier concentration increases, the barrier height at grain boundaries reduces in polycrystalline films and a larger fraction of "bulk" trap states within the semiconductor band gap are filled in amorphous films. Thus, for IGO-based TFTs, the increase in mobility with decreasing O_2 partial pressure is attributed to a larger fraction of filled interface traps and/or traps within the semiconductor at zero-gate bias, resulting in reduced trapping of injected channel electrons.

3. **Influence of semiconductor thickness:** The influence of semiconductor thickness, t_s (10-150 nm) is investigated using staggered bottom-gate IGZO-based TFTs. μ_{inc} varies only slightly with respect to t_s ($< 15\%$ variation), with thinner semiconductor layers exhibiting slightly lower mobility than the thicker layers. V_{on} decreases as t_s increases. TFT stability improves with increasing t_s. First, the magnitude of the hysteresis observed during device characterization reduces as t_s is increased. Next, bias stress stability improves with increasing t_s. Finally, extremely thin devices (with $t_s = 10$ nm) exhibit poor shelf life stability. Over a 10 week period, a 5.75 V shift in V_{on} is observed for the worst device. One drawback to increasing t_s is the degradation observed in subthreshold swing as t_s is increased.

4. **TFT stability:** Bias stress stability improves as V_{on} is decreased. V_{on} is controlled by tuning the O_2 partial pressure of the deposition ambient and selecting the appropriate post-deposition annealing ambient (air or N_2). For an IGZO-based TFT sputtered in pure Ar and subjected to a 175 °C post-deposition anneal in air, $V_{on} \simeq$ 0 V. This device also exhibits excellent stability. While monitoring I_D over a 1000 minute testing period and applying a constant voltage bias of $V_{DS} = V_{GS} = 30$ V, less than 20% current loss is observed. Additionally, a positive V_{on} shift of $\sim$2 V is observed. The shift in V_{on} is attributed to electron trapping in interface states (at the insulator-semiconductor interface), in surface states (at the back surface, which is the surface opposite to the insulator-semiconductor interface), and/or in "bulk" traps within the semiconductor band gap. The observed current loss is also attributed to electron trapping and the concomitant shift in V_{on}.

5. **Effect of SU-8 passivation:** Staggered bottom-gate IGO, ZTO, and IGZO-based TFTs are successfully passivated with SU-8. When $V_{on} \geq 0$ V before passivation, device characteristics exhibit minimal change after the SU-8 passivation layer is deposited. In contrast, when $V_{on} <$ -5 V before passivation, a large negative shift in V_{on} ($>$ 30 V) occurs after SU-8 passivation. This large negative shift prevents the device from being fully turned off at reasonable voltages and renders the device useless (from a circuit integration viewpoint). This underscores the importance of utilizing process parameters to achieve a turn-on voltage near zero.

6. **Device characterization:** Throughout this research, several nuances of device characterization have been discovered and are disclosed here. While it may be unrealistic to use identical testing conditions for all devices fabricated throughout research, always use identical testing conditions when making a comparison between several devices and/or establishing a trend. Additionally, device testing for an experiment should be completed within one week of fabrication, as shelf life instability can shift extracted figures-of-merit such as V_{on} and subthreshold swing. While these shifts are quite small in most cases, it is good practice to minimize any unintended experimental variables. Finally, when determining V_{on} shift for device stability testing, a V_{GS} step size of 100 mV or less should be employed.

6.2 Recommendations for Future Work

Based on the results presented in this dissertation and by others in the research community, this section provides recommendations for future work in the field of oxide semiconductor-based TFTs.

6.2.1 Recommendations for oxide semiconductor-based TFT exploration

1. **Optimization of ZTO-based TFTs:** Additional tuning of O_2 partial pressure should be investigated. However, to achieve optimal performance, a design of experiments may be useful with O_2 percentage (0.75 to 1.5 %), total pressure (5 to 30 mTorr), and power (25 to 75 W with a 2” target) as the independent variables. In addition, tuning of the sputtering pressure and power may further enhance device stability.

2. **Exploration of new channel materials:** A plethora of materials may be utilized as channel layer materials, providing a substantial research opportunity. Research should focus on previously unexplored multicomponent oxide semiconductors identified by Hosono *et al*. [51] Another option is to tune the stoichiometry of a material. For stoichiometry optimization, a combinatorial approach (where multiple sources are used to create a stoichiometry gradient across a single substrate for extensive evaluation) may be particularly useful. In distinguishing device performance, the complete spectrum of figures-of-merit (V_{on}, μ, I_D^{on-off}, subthreshold swing) should be evaluated along with device stability.

3. **Exploration of p-channel TFTs:** Exploration of p-channel TFTs is recommended as a means of realizing a complementary circuit technology with oxide-based TFTs. Potential channel materials include NiO and Cu_2O. Additionally, note that hole injection will likely pose a difficult challenge in forming these TFTs. One drawback is that most p-type oxides either have poor mobility or require a high temperature annealing treatment to achieve reasonable performance.

4. **Exploration of degenerate oxide semiconductors:** In addition to channel layer exploration, alternative degenerate oxide semiconductors should be investigated due to the limited supply of In and as a means to optimize device performance. Possible n-TCOs are listed in Table 2.1. Substitutionally doped ZnO (e.g. ZnO:Al) or SnO_2 (e.g. SnO_2:F) should be explored first due to the extensive literature available for these materials. Intrinsic TCOs should initially be avoided since their pro-

cessing typically utilizes an inert or reducing ambient, which may (depending on device structure) unintentionally reduce V_{on} of devices.

6.2.2 Recommendations for integration

1. **Developing an insulator process:** For future device integration, a reproducible, low-temperature insulator process should be developed. This will allow fabrication of flexible devices, a current topic of great interest. Additionally, an insulator process allows tuning of the gate capacitance (by controlling the insulator thickness) to minimize device operating voltages while maintaining a reasonable gate leakage current. However, exploring deposition techniques other than sputtering may be necessary to achieve this goal; one attractive alternative is atomic layer deposition.

2. **Circuit integration:** IGO and IGZO-based ring oscillators have been reported, but it may be useful to attempt other circuits, such as current mirrors or logic gates. These circuits place additional requirements on the TFT, such as congruency (for the current mirror), and may be useful in learning the limits of this nascent technology.

3. **SU-8 passivation:** The data regarding SU-8 passivation presented in Ch. 5 provides a useful initial baseline. However, several aspects require additional investigation. While SU-8 is reported to have low surface roughness, the surface roughness of SU-8 layers deposited atop TFTs should be appraised and the SU-8 deposition process optimized if necessary. Additionally, the shelf life stability of SU-8 passivated devices should be investigated to see if any improvement is observed over air-exposed

devices. Finally, other materials with a higher Young's modulus and lower permeability to air/water should be investigated; $AlPO_x$, a solution-deposited dielectric investigated by the OSU Chemistry Department, may fill the requirements needed in this application.

4. **Device stability:** The results presented in Ch. 5 approach device stability from the viewpoint of improving device stability and determining which experimental parameters affect device stability. However, it is also important to investigate the physical mechanisms (such as hydrogen diffusion in a-Si:H TFTs) that hinder device stability. Testing of devices at different temperatures may also be useful; this testing methodology can be used to extract an activation energy related to device degradation and can be helpful in fitting oxide semiconductor-based TFT stability data to a degradation model.

BIBLIOGRAPHY

1. G. Busch, “Early history of the physics and chemistry of semiconductors-from doubts to fact in a hundred years,” *Eu. J. Phys.*, vol. 10, pp. 254–64, 1989.

2. J. Frenkel, “Ueber die Wärmebewegung in festen und flüssigen Körpern,” *Z. Phys.*, vol. 35, pp. 652–69, 1926.

3. C. Wagner and W. Schottky, “Theorie der geordneten Mischphasen,” *Z. Phys. Chem.*, vol. 11, pp. 163–210, 1931.

4. W. Jost, “Diffusion and electrolytic conduction in crystals (ionic semiconductors),” *J. Chem. Phys.*, vol. 1, pp. 466–75, 1933.

5. A. H. Wilson, “The theory of electronic semiconductors I,” *Proc. R. Soc. A*, vol. 133, pp. 458–91, 1931.

6. A. H. Wilson, “The theory of electronic semiconductors II,” *Proc. R. Soc. A*, vol. 134, pp. 277–87, 1931.

7. B. Gudden, “Elektrizitätsleitung in kristallisierten stoffen unter ausschluss der metalle ergeb,” *Exakten Naturwiss.*, vol. 3, pp. 116–59, 1924.

8. H. Dunwald and C. Wagner, “Untersuchungen uber Fehlordnungserscheinungen in Kupferoxydul und deren Eintluss auf die elektrischen Eigenschaften,” *Z. Phys. Chem.*, vol. 22, pp. 212–25, 1933.

9. H. H. von Baumbach and C. Wagner, “Die elektrische Leitfähigkeit von Zinkoxyd und Cadmiumoxyd,” *Z. Phys. Chem. B*, vol. 22, pp. 199–211, 1933.

10. C. Wagner, “Theorie der geordneten Mischphasen,” *Z. Phys. Chem. B*, vol. 22, pp. 181–94, 1933.

11. R. G. Gordon, “Criteria for choosing transparent conductors,” *MRS Bull.*, vol. 25, pp. 52–7, 2000.

12. S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, “Transparent thin film transistors using ZnO as an active channel layer and their electrical properties,” *J. Appl. Phys.*, vol. 93, no. 3, pp. 1624–1630, 2003.

13. R. Hoffman, B. Norris, and J. Wager, “ZnO-based transparent thin-film transistors,” *Appl. Phys. Lett.*, vol. 82, no. 5, pp. 733–735, 2003.

14. P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, Jr., “Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering,” *Appl. Phys. Lett.*, vol. 82, no. 7, pp. 1117–1119, 2003.

15. H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer," *Appl. Phys. Lett.*, vol. 86, p. 013503, 2005.

16. N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, C.-H. Park, and D. A. Keszler, "Transparent thin-film transistors with zinc indium oxide channel layer," *J. Appl. Phys.*, vol. 97, p. 064505, 2005.

17. K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *Science*, vol. 300, pp. 1269–1272, 2003.

18. P. Görrn, M. Sander, J. Meyer, M. Kröger, E. Becker, H.-H. Johannes, and W. K. T. Riedl, "Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes," *Adv. Mater.*, vol. 18, pp. 738–41, 2006.

19. R. E. Presley, D. Hong, H. Q. Chiang, C. M. Hung, R. L. Hoffman, and J. F. Wager, "Transparent ring oscillator based on indium gallium oxide thin-film transistors," *Solid-St. Electron*, vol. 50, pp. 500–3, 2006.

20. M. Ofugi, K. Abe, N. Kaji, R. Hayashi, M. Sano, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Integrated circuits based on amorphous indium-gallium-zinc-oxide-channel thin-film transistors," *ECS Trans.*, vol. 3, no. 8, pp. 293–300, 2006.

21. M. Ito, M. Kon, M. Ishizaki, C. Miyazaki, and Y. Ugajin, "A flexible active-matrix electronic paper display driven with amorphous oxide semiconductor," (Reno, Nevada), 2006.

22. K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment and *ab initio* calculations," *Phys. Rev. B: Condens. Matter*, vol. 75, p. 035212, 2007.

23. P. Görrn, P. Hölzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, "Stability of transparent zinc tin oxide transistors under bias stress," *Appl. Phys. Lett.*, vol. 90, p. 063502, 2007.

24. F. M. Hossain, J. Nishii, S. Takagi, A. Ohtomo, T. F. H. Fujioka, H. Ohno, H. Koinuma, and M. Kawasaki, "Modeling and simulation of polycrystalline ZnO thin-film transistors," *J. Appl. Phys.*, vol. 94, no. 12, pp. 7768–7777, 2003.

25. H. Kawazoe and K. Ueda, "Transparent conducting oxides based on the spinel structure," *J. Am. Ceram. Soc.*, vol. 82, no. 12, pp. 3330–3336, 1999.

26. J. R. Bellingham, W. A. Phillips, and C. J. Adkins, “Intrinsic performance limits in transparent conducting oxides,” *J. Mater. Sci. Lett.*, vol. 11, pp. 263–5, 1992.

27. H. Ohta, M. Orita, M. Hirano, H. Tanji, H. Kawazoe, and H. Hosono, “Highly electrically conductive indiumtinoxide thin films epitaxially grown on yttria-stabilized zirconia (100) by pulsed-laser deposition,” *Appl. Phys. Lett.*, vol. 76, no. 19, pp. 2740–2, 2000.

28. T. Coutts, D. Young, and X. Li, “Search for improved transparent conducting oxides: A fundamental investigation of CdO, Cd_2SnO_4, and Zn_2SnO_4,” *J. Vac. Sci. Technol. A*, vol. 18, no. 6, pp. 2646–2660, 2000.

29. K. Ellmer, “Resitivity of polycrystalline zinc oxide films: current status and physical limit,” *J. Phys. D.: Appl. Phys.*, vol. 34, pp. 3097–3108, 2001.

30. K. Ellmer, R. Cebulla, and R. Wendt, “Transparent and conducting zno(:Al) films deposited by simultaneous RF- and DC-excitation of a magnetron,” *Thin Solid Films*, vol. 317, pp. 413–6, 1998.

31. B. Szyszka, V. Sittinger, X. Jiang, R. Hong, W. Werner, A. Pflug, M. Ruske, and A. Loppb, “Transparent and conductive ZnO:Al films deposited by large area reactive magnetron sputtering,” *Thin Solid Films*, vol. 442, pp. 179–83, 2004.

32. R. Hoffman, “Development, fabrication, and characterization of transparent electronic devices,” Master’s thesis, Oregon State University, 2002.

33. Z. Jarzębski, *Oxide Semiconductors*. Oxford: Pergamon Press, 1973.

34. F. Koffyberg and F. Benko, “Cd_2SnO_4, $CdIn_2O_4$ and Cd_2GeO_4 as anodes for the photoelectrolysis of water,” *Appl. Phys. Lett.*, vol. 37, no. 3, pp. 320–322, 1980.

35. X. Wu, T. Coutts, and W. Mulligan, “Properties of transparent conducting oxides formed from CdO and ZnO alloyed with SnO_2 and In_2O_3,” *J. Vac. Sci. Technol. A*, vol. 15, no. 3, pp. 1057–1062, 1997.

36. K. Chopra, S. Major, and D. Pandya, “Transparent conductors - a status review,” *Thin Solid Films*, vol. 102, pp. 1–46, 1983.

37. O. Lang, C. Pettenkofer, J. Sanchez-Royo, A. Segura, A. Klein, and W. Jaegermann, “Thin film growth and band lineup of In_2O_3 on the layered semiconductor InSe,” *J. Appl. Phys.*, vol. 86, no. 10, pp. 5687–5691, 1999.

38. J. M. Phillips, J. Kwo, A. Thomas, A. Carter, R. Cava, and S. Hou, “Transparent conducting thin films of $GaInO_3$,” *Appl. Phys. Lett.*, vol. 65, no. 1, pp. 115–117, 1994.

39. T. Minami, T. Miyata, and T. Yamamoto, "Work function of transparent conducting multicomponent oxide thin films prepared by magnetron sputtering," *Surf. and Coat. Tech.*, vol. 108-109, pp. 583–587, 1998.

40. M. Orita, M. Takeuchi, H. Sakai, and H. Tanji, "New transparent conducting oxides with $YbFe_2O_4$," *Jpn. J. Appl. Phys.*, vol. 34, no. 11B, pp. L1550–2, 1995.

41. M. Orita, H. Tanji, M. Mizuno, H. Adachi, and I. Tanaka, "Mechanism of electrical conductivity of transparent $InGaZnO_4$," *Phys. Rev. B: Condens. Matter*, vol. 61, no. 3, pp. 1811–6, 2000.

42. M. Islam and M. Hakim, "Electron affinity and work function of polycrystalline tin dioxide thin film," *J. Mater. Sci. Lett.*, vol. 5, no. 1, pp. 63–65, 1986.

43. T. Minami, H. Sonohara, T. Kakumu, and S. Takata, "Highly transparent and conductive $Zn_2In_2O_5$ thin films prepared by RF magnetron sputtering," *Jpn. J. Appl. Phys.*, vol. 34, no. 8A, pp. 971–974, 1995.

44. T. Minami, S. Takata, H. Sato, and H. Sonhana, "Properties of transparent zinc-stannate conducting films prepared by radio frequncy magnetron sputtering," *J. Vac. Sci. Technol. A*, vol. 13, no. 3, pp. 1095–1099, 1995.

45. T. Minami, H. Sonohara, S. Takata, and H. Sato, "Highly transparent and conductive zinc-stannate thin films prepared by RF magnetron sputtering," *Jpn. J. Appl. Phys.*, vol. 33, no. 12A, pp. 1693–1696, 1994.

46. D. L. Young, H. Moutinho, Y. Yan, and T. J. Coutts, "Growth and characterization of radio frequecy magnetron sputter-deposited zinc stannate, Zn_2SnO_4, thin films," *J. Appl. Phys.*, vol. 92, no. 1, pp. 310–319, 2002.

47. D. L. Young, *Electron Transport in Zinc Stannate (Zn_2SnO_4)*. PhD thesis, Colorado School of Mines, 2000.

48. H. Yanagi, T. Hase, S. Ibuki, K. Ueda, and H. Hosono, "Bipolarity in electrical conduction of transparent oxide semiconductor $CuInO_2$ with delafossite structure," *Appl. Phys. Lett.*, vol. 78, no. 11, pp. 1583–1585, 2001.

49. D. Look, D. Reynolds, C. Litton, R. Jones, D. Eason, and G. Cantwell, "Characterization of homoepitaxial p-type ZnO grown by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 81, no. 10, pp. 1830–1832, 2002.

50. X. Li, Y. Yan, T. Gessert, C. DeHart, C. Perkins, D. Young, and T. Coutts, "p-Type ZnO thin films formed by CVD reaction of Diethylzinc and NO gas," *Electrochemical and Sol. St. Lett.*, vol. 6, no. 4, pp. C56–C58, 2003.

51. H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, "Working hypothessis to explore novel wide band gap electrically conducting amorphous oxides and examples," *J. Non-Cryst. Sol.*, vol. 198-200, pp. 165–9, 1996.

52. H. Hosono, M. Yasukawa, and H. Kawazoe, "Novel oxide amorphous semiconductors: transparent conducting amorphous oxides," *J. Non-Cryst. Sol.*, vol. 203, pp. 334–344, 1996.

53. S. Narushima, M. Orita, M. Hirano, and H. Hosono, "Electronic structure and transport properties in transparent amorphous oxide semiconductor $2CdO \cdot GeO_2$," *Phys. Rev. B: Condens. Matter*, vol. 66, p. 0335203, 2002.

54. Y. Shigesato and D. C. Paine, "Study of the effect of Sn doping on the electronic transport properties of thin film indium oxide," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1268–70, 1993.

55. O. Kluth, C. Agashe, J. Hüpkes, J. Müller, and B. Rech, "Magentron sputtered zinc stannate films for silicon thin film solar cells," (Osaka, Japan), May 2003.

56. D. Kovacheva and K. Petrov, "Preparation of crystalline $ZnSnO_3$ and Li_2SnO_3 by low temperature ion exchange," *Sol. St. Ionics*, vol. 109, no. 3, pp. 327–32, 1998.

57. Y. Shen and Z. Zhang, "Preparation, structure and gas-sensing properties of ultramicro $ZnSnO_3$ powder," *Sensors & Actuators B, Chem.*, pp. 5–9, 1993.

58. T. Moriga, Y. Hayashi, K. Kondo, Y. Nishimura, K. Murai, I. Nakabayashi, H. Fukumoto, and K. Tominaga, "Transparent conducting amorphous Zn-Sn-O films deposited by simultaneous dc sputtering," *J. Vac. Sci. Technol. A*, vol. 22, no. 4, pp. 1705–10, 2004.

59. S. Abboudy, A. Al-Hajri, A. Al-Shahrani, M. Al-Assiri, L. Abulnasr, A. Sweyllam, and A. Brinkman, "Influence of substrate temperatue on the electrical behaviour of zinc stannate thin films deposited by electron beam evaporation technique," *Il Nuovo Cimento Della Societa di Fisica*, vol. 20, no. 12, pp. 1881–1889, 1998.

60. D. L. Young, D. Williamson, and T. Coutts, "Structural characterization of zinc stannate thin films," *J. Appl. Phys.*, vol. 91, no. 3, pp. 1464–1471, 2002.

61. H. Enoki, T. Nakayama, and J. Echigoya, "The electrical and optical properties of the ZnO-SnO_2 thin films prepared by rf magnetron sputtering," *J. Phys. D.: Appl. Phys.*, vol. 34, pp. 3097–3108, 2001.

62. R. Gordon, D. Pang, R. Broomhall-Dilard, X. Liu, and J. Barton, "Transparent conductors and barrier layers for thin-film solar cells," technical report, Harvard Univerity/NREL, 2001.

63. I. Stambolova, K. Konstantinov, D. Kovacheva, P. Peshev, and T. Donchev, "Spray pyrolysis preparation and humidity sensing characteristics of spinel zinc stannate thin films," *J. Solid State Chem.*, vol. 128, no. 2, pp. 305–309, 1997.

64. X. Wu, R. Ribelin, R. Dhere, D. Albin, T. Gessert, S. Asher, D. Levi, A. Mason, H. Moutinho, and P. Sheldon, "High-efficiency $Cd_2SnO_4/Zn_2SnO4/Zn_xCd_{1-x}S$/CdS/CdTe polycrystalline thin-film solar cells," in *Conference Record of the Twenty-Eighth IEEE Photovoltaic Specialists Conference - 2000*, (Anchorage, AK, USA), pp. 397–402, IEEE, 2000.

65. S. Matsushima, S. Kunitsugu, K. Kobayashi, and G. Okada, "NO_2 sensing properties of thick Zn_2SnO_4 film," *J. Vac. Sci. Technol. A*, vol. 15, no. 3, pp. 1057–1062, 1997.

66. N. Hiratsuka, A.Hosoi, H. Kobayashi, and K. Kakizaki, "Isobutane gas sensing characteristics of zinc-tin complex oxide system," *J. Ceram. Soc. Jpn.*, vol. 104, no. 12, pp. 1158–1159, 1996.

67. Y. Yamada, Y. Seno, Y. Masuoka, and K. Yamashita, "Nitrogen oxides sensing characteristics of Zn_2SnO_4 thin film," no. 3, pp. 248–252, 1998.

68. C. Vigreux, L. Binet, D. Gourier, and B. Piriou, "Formation by laser impact of conducting $\beta - Ga_2O_3 - In_2O_3$ solid solutions with composition gradients," *J. Sol. State Chem.*, vol. 157, p. 94, 2001.

69. D. D. Edwards, P. Folkins, and T. Mason, "Phase equilibria in the $Ga_2O_3 - In_2O_3$ system," *J. Amer. Cer. Soc.*, vol. 80, p. 253, 1997.

70. T. Minami, Y. Takeda, T. Kakumu, S. Takata, and I. Fukuda, "New multicomponent transparent conducting oxide films for transparent electrodes of flat panel displays," *J. Vac. Sci. Technol. A*, vol. 15, p. 958, 1997.

71. R. Cava, J. Philips, J. Kwo, G. A. Thomas, R. B. van Dover, and S. A. Carter, "$GaInO_3$: A new transparent conducting oxide," *Appl. Phys. Lett.*, vol. 64, p. 2071, 1994.

72. T. Minami, "Preparation of highly transparent and conducting $Ga_2O_3 - In_2O_3$ films by direct current magnetron sputtering," *J. Vac. Sci. Technol. A*, vol. 17, p. 1765, 1999.

73. M. Nakamura, N. Kimizuka, and T. Mohri, "The phase relations in the $In_2O_3 - GaZnO_4 - ZnO$ system at 1350°c," *J. Sol. St. Chem.*, vol. 93, no. 2, pp. 298–315, 1991.

74. T. Moriga, D. R. Kammler, and T. O. Mason, "Electrical and optical properties of transparent conducting homologous compounds in the Indium-Gallium-Zinc Oxide system," *J. Am. Ceram. Soc.*, vol. 82, no. 10, pp. 2705–10, 1999.

75. M. Orita, H. Ohta, H. Hosono, K. Morita, H. Tanji, and H. Kawazoe, "Properties of a novel amorphous transparent conductive oxide, $InGaO_3(ZnO)_m$," *Mat. Res. Soc. Symp.*, vol. 623, pp. 291–6, 2000.

76. M. Orita, H. Ohta, M. Hirano, S. Narushima, and H. Hosono, "Amorphous transparent conductive oxide $InGaO_3(ZnO)_m$ $(m \leq 4)$: a zn 4s conductor," *Philos. Mag. B*, vol. 81, no. 5, pp. 501–15, 2001.

77. H. Ohta, K. Nomura, M. Orita, M. Hirano, K. Ueda, T. Suzuki, Y. Ikuhara, and H. Hosono, "Single-crystalline films of homologous series $InGaO_3(ZnO)_m$ grown by reactive solid-phase epitaxy," *Ad. Funct. Mater.*, vol. 13, no. 2, pp. 139–44, 2003.

78. B. K. Teo, *EXAFS: basic principles and data analysis*. Springer, 1986.

79. D. C. Koeningsberg and R. Prins, *X-ray absorption principles, applications, and techniques of EXAFS, SEXAFS, and XANES*. Wiley, 1988.

80. H. Hiramatsu, K. Ueda, H. Ohta, M. Hirano, and H. Hosono, "Excitonic blue luminescence from *p*-LaCuOSe / *n*-$InGaZn_5O_8$ light emitting diode at room temperature," *Appl. Phys. Lett.*, vol. 87, p. 21107, 2005.

81. J. E. Lilienfeld, "Device for controlling electric current." US Pat. 1,900,018, 1933.

82. P. K. Weimer, "The TFT - a new thin-film transistor," *Proceedings of the IRE*, vol. 50, pp. 1462–1469, 1962.

83. C. Chen, C. Chiang, C. Malone, and J. Kanicki, "Electronic performance and instability of high-field-effect-mobility a-Si:H TFT made from high-deposition-rate pecvd materials," *AM-LCD 96*, pp. 37–40, 1996.

84. A. R. Brown, C. P. Jarrett, D. M. de Leeuw, and M. Matters, "Field-effect transistors made from solution-processed organic semiconductors," *Syn. Metals*, vol. 88, pp. 37–55, 1997.

85. A. Goetzberger and E. H. Nicollian, "Transient voltage breakdown due to avalanche in MIS capacitors," *Appl. Phys. Lett.*, vol. 9, no. 12, pp. 444–6, 1966.

86. C. R. Kagan and P. Andry, *Thin-film transistors*. New York: Marcel Dekker, Inc., 2003.

87. R. L. Hoffman, "ZnO-channel thin-film transistors: Channel mobility," *J. Appl. Phys.*, vol. 95, no. 10, pp. 5813–19, 2004.

88. P. F. Carcia, R. S. McLean, and M. H. Reilly, "Oxide engineering of zno thin-film transistors for flexible electronics," *J. SID*, vol. 13, no. 7, pp. 547–54, 2005.

89. P. F. Carcia, R. S. McLean, and M. H. Reilly, "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 88, p. 123509, 2006.

90. J. Nishii, F. M. Hossain, S. Takagi, T. Aita, K. Saikusa, Y. Ohmaki, I. O. S. Kishimoto, A. Ohtomo, T. Fukumura, F. Matsukura, Y. Ohno, H. Koinuma, H. Ohno, and M. Kawasaki, "High mobility thin film transistors with transparent ZnO channels," *Jpn. J. Appl. Phys.*, vol. 42, no. 4A, pp. 347–349, 2003.

91. E. Fortunato, A. Pimentel, L. Pereira, A. Gonçalves, G. Lavareda, H. Águas, I. Ferreira, C. Carvalho, and R. Martins, "High field-effect mobility zinc oxide thin film transistors produced at room temperature," *J. Non-Cryst. Sol.*, vol. 338-400, pp. 806–9, 2004.

92. E. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, L. M. N. Pereira, and R. F. P. Martins, "Fully transparent ZnO thin-film transistor processed at room temperature," *Adv. Mater.*, vol. 17, no. 5, pp. 590–4, 2005.

93. T. Hirao, M. Furuta, H. Furuta, T. Matsuda, T. Hiramatsu, H. Hokari, and M. Yoshida, "High mobility top-gate zinc oxide thin-film transistors (ZnO-TFTs) for active-matrix liquid crystal displays," *SID Digest*, vol. 2006, pp. 18–20, 2006.

94. S.-H. K. Park, C.-S. Hwang, J. Lee, S. M. Chung, Y. S. Yang, L.-M. Do, and H. Y. Chu, "Transparent ZnO thin film transistor array for the application of transparent AM-OLED display," *SID Digest*, vol. 2006, pp. 25–8, 2006.

95. H.-H. Hseih and C.-C. Wu, "Scaling behavior of ZnO transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 89, p. 041109, 2006.

96. H. S. Bae, M. H. Yoon, J. H. Kim, and S. Im, "Photodetecting properties of ZnO-based thin-film transistors," *Appl. Phys. Lett.*, vol. 83, no. 25, pp. 5313–5, 2003.

97. H. S. Bae and S. Im, "ZnO-based thin-film transistors of optimal device performance," *J. Vac. Sci. Technol. B*, vol. 22, no. 3, pp. 1191–5, 2004.

98. H. S. Bae, C. M. Choi, J. H. Kim, and S. Im, "Dynamic and static photoresponse of ultraviolet-detecting thin-film transistors based on transparent NiO_x electrodes and an *n*-ZnO channel," *J. Appl. Phys.*, vol. 97, p. 076104, 2005.

99. K. Lee, J. H. Kim, S. Im, C. S. Kim, and H. K. Baik, "Low-voltage-driven top-gate ZnO thin-film transistors with polymer/high-k oxide double-layer dielectric," *Appl. Phys. Lett.*, vol. 89, p. 133507, 2006.

100. K. Lee, J. H. Kim, and S. Im, "Probing the work function of a gate metal with a top-gate ZnO-thin-film transistor with a polymer dielectric," *Appl. Phys. Lett.*, vol. 88, p. 023504, 2006.

101. A. Ohtomo, S. Takagi, K. Tamura, T. Makino, Y. Segawa, H. Koinuma, and M. Kawasaki, "Photo-irresponsive thin-film transistor with $Mg_xZn_{1-x}O$ channel," vol. 45, no. 27, pp. L694–6, 2006.

102. Y. Kwon, Y. Li, Y. W. Heo, M. Jones, P. H. Holloway, D. P. Norton, Z. V. Park, and S. Li, "Enhancement-mode thin-film field-effect transistor using phosphorus-doped (Zn,Mg)O channel," *Appl. Phys. Lett.*, vol. 84, no. 14, pp. 2685–7, 2004.

103. B. Norris, J. Anderson, J. Wager, and D. Keszler, "Spin-coated zinc oxide transparent transistors," *J. Phys. D: Appl. Phys.*, vol. 36, pp. L105–7, 2003.

104. J. H. Lee, P. Lin, J. C. Ho, and C. C. Lee, "Chemical solution deposition of $zn_{1-x}zr_xo$ thin films as active channel layers of thin-film transistors," *Electrochem. Sol. St. Lett.*, vol. 9, no. 4, pp. G117–20, 2006.

105. H.-C. Cheng, C.-F. Chen, and C.-C. Lee, "Thin-film transistors with active layers of zinc oxide (ZnO) fabricated by low-temperature chemical bath method," *Thin Solid Films*, vol. 498, pp. 142–5, 2005.

106. R. E. Presley, C. L. Munsee, C. H. Park, D. Hong, J. F. Wager, and D. A. Keszler, "Tin oxide transparent thin-film transistors," *J. Phys. D: Appl. Phys.*, vol. 37, pp. 2810–2813, 2004.

107. L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, and T. J. Marks, "High-performance transparent inorganicorganic hybrid thin-filmn-type transistors," *Nat. Mater.*, vol. 5, pp. 893–900, 2006.

108. R. L. Hoffman, "Effects of channel stoichiometry and processing temperature on the electrical characteristics of zinc tin oxide thin-film transistors," *Solid-St. Electron*, vol. 50, pp. 784–7, 2006.

109. W. B. Jackson, R. L. Hoffman, and G. S. Herman, "High-performance flexible zinc tin oxide field-effect transistors," *Appl. Phys. Lett.*, vol. 87, p. 193503, 2005.

110. D. Hong, H. Q. Chiang, and J. F. Wager, "Zinc tin oxide thin-film transistors via reactive sputtering using a metal target," *J. Vac. Sci. Technol. B*, vol. 24, no. 5, pp. L23–5, 2006.

111. P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins, and E. Fortunato, "Effect of UV and visible light radiation on the electrical performances of transparent tfts based on amorphous indium zinc oxide," *J. Non-Cryst. Sol.*, vol. 352, pp. 1756–60, 2006.

112. P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins, and E. Fortunato, "Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide," *J. Non-Cryst. Sol.*, vol. 352, pp. 1749–52, 2006.

113. B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine, "High-mobility amorphous $In_2O_3$10 wt % ZnO thin film transistors," *Appl. Phys. Lett.*, vol. 89, p. 062103, 2006.

114. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, p. 288, 2004.

115. H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering," *Appl. Phys. Lett.*, vol. 89, p. 112123, 2006.

116. T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Combinatorial study on In-Ga-Zn-O semiconductor films as active-channel layers for thin-film transistor," *Mater. Res. Soc. Symp. Proc.*, vol. 928, pp. 0928–GG10–04, 2006.

117. S. Wolf and R. Tauber, *Silicon Processing for the VLSI Era: Volume 1 - Process Technology*. California: Lattice Press, 2000.

118. P. D. Keir, *Fabrication and Characterization of ACTFEL Devices*. PhD thesis, Oregon State University, 1999.

119. L. Maissel and R. Glang, *Handbook of Thin Film Technology*. New York: McGraw-Hill, 1970.

120. J. J. Hanak and J. P. Pellicane, "Effect of secondary electrons and negative ions on sputtering of films," *J. Vac. Sci. Technol.*, vol. 13, no. 1, pp. 406–409, 1976.

121. W. M. Ang, "ACTFEL phosphor deposition by rf sputtering," Master's thesis, Oregon State University, 1993.

122. H. Q. Chiang, "Development of zinc tin oxide-based transparent thin-film transistors," Master's thesis, Oregon State University, 2003.

123. Veeco Instruments, Inc., *Veeco Microecth System: Operation & Maintenance*, first ed., 1981.

124. J. F. Wager. Private Communication, 2003.

125. TWI, "The use of thoriated electrodes." World Wide Web page, http://www.twi.co.uk/., 2003.

126. Pro-fusion, "Thoriated tungsten radioactivity." World Wide Web page, http://www.pro-fusiononline.com/., 2003.

127. T. Suntola and J. Hyvärinen, "Atomic layer epitaxy," *Ann. Rev. Mater. Sci.*, vol. 15, pp. 177–195, 1985.

128. B. A. Baukol, *Alternating-Current Thin-Film Electroluminescent Device Fabrication and Characterization*. PhD thesis, Oregon State University, 2002.

129. T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu, and J. C. Sturm, "Ink-jet printing of doped polymers for organic light emitting diodes," *Appl. Phys. Lett.*, vol. 72, no. 5, pp. 519–21, 1998.

130. F. Garnier, R. Hajlaoui, A. Yassar, and P. Srivastava, "All-polymer field-effect transistor realized by printing techniques," *Science*, vol. 265, no. 5179, pp. 1684–6, 1994.

131. J. A. Rogers, Z. Bao, A. Makhija, and P. Braun, "Printing process suitable for reel-to-reel production of high-performance organic transistors and circuits," *Adv. Mater.*, vol. 11, no. 9, pp. 741–5, 1999.

132. J. A. Rogers, J. Tate, W. Li, Z. Bao, and A. Dodabalapur, "Printed organic transistors and molded plastic lasers," *Israel J. of Chem.*, vol. 40, no. 2, pp. 139–45, 2000.

133. B. A. Ridley, B. Nivi, and J. M. Jacobson, "All-inorganic field effect transistor fabricated by printing," *Science*, vol. 286, pp. 746–9, 1999.

134. D. K. Schroeder, *Semiconductor Material and Device Characterization*. New York: John Wiley & Sons, Inc., 1998.

135. E. Putley, *The Hall Effect and Related Phenomena*. London: Butterworth, 1960.

136. J. I. Pankove, *Optical Processes in Semiconductors*. New York: Dover Publications, Inc., 1971.

137. R. A. Smith, *Wave Mechanics of Crystalline Solids*. London: Chapman and Hall Ltd., 1969.

138. E. Burstein, "Anamolous optical absorption limit in InSb," *J. Vac. Sci. Technol. B*, vol. 93, p. 632, 1954.

139. T. Moss, "The interpretation of the properties of indium antimonide," *Proc. Phys. Soc. B*, vol. 67, pp. 775–782, 1954.

140. T. Moss, *Optical Properties of Semi-Conductors*. London: Butterworths Scientific Publications, 1959.

141. S. Adachi, *Optical Properties of Crystalline and Amorphous Semiconductors: Materials and Fundamental Principles*. Massachusetts: Kluwer Academic Publishers, 1999.

142. R. Zallen, *The Physics of Amorphous Solids*. New York: Wiley-Interscience, 1983.

143. J. Tauc, *Amorphous and liquid semiconductors*. New York: Plenum Press, 1974.

144. S. R. Elliot, *Physics of Amorphous Materials*. New York: Longman, 1983.

145. S. Sze, *Physics of Semiconductor Devices*. New York: John Wiley & Sons, 1981.

146. W. Strehlow and E. Cook, "Compilation of energy band gaps in elemental and binary compound semiconductors and insulators," *J. Phys. Chem. Ref. Data*, vol. 2, no. 1, pp. 163–199, 1973.

147. P. Peacock and J. Robertson, "Band offsets and Schottky barrier heights of high dielectric constant oxides," *J. Appl. Phys.*, vol. 92, no. 8, pp. 4712–4721, 2002.

148. J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Technol. B*, vol. 18, no. 3, pp. 1785–1791, 2000.

149. A. Many, "Relation between physical and chemical processes on semconductor surfaces," *CRC Critical Reviews in Sol. St. Sci.*, vol. 4, no. 3, pp. 515–539, 1974.

150. P. Mark, "Chemisorption and trapping on insulator surfaces," *Trans. of the New York Academy of Sci.*, vol. 27, no. 8, pp. 946–958, 1965.

151. R. Hoffman. Private Communication, 2003.

152. Y. A. Ono, *Electroluminescent Displays*. Singapore: World Scientific, 1995.

153. R. Konenkamp and I. Rieck, "Electrical properties of Schottky diodes on nano-porous TiO_2 films," *Mat. Sci. & Eng., B: Sol. St. Mat. for Ad. Tech.*, pp. 519–521, 2000.

154. S. Chatterjee, S. Nandi, S. Maikap, S. Samanta, and C. Maiti, "Electrical properties of deposited ZrO_2 films on ZnO/n-Si substrate," *Semi. Sci. and Tech.*, vol. 18, pp. 92–96, 2003.

155. D. W. Greve, *Field Effect Devices and Applications: Devices for Portable, Low-Power, and Imaging Systems*. New Jersey: Prentice Hall, 1998.

156. L. Risch, "Electron mobility in short-channel MOSFET's with series resistance," *IEEE Trans. Electron Devices*, vol. ED-30, no. 8, pp. 959–961, 1983.

157. J. Kang, D. Shroder, and A. Alvarez, "Effective and field-effect mobilities in Si MOSFETs," *Solid State Electronics*, vol. 32, no. 8, pp. 679–681, 1989.

158. R. L. Hoffman, "A closed-form DC model for long-channel thin-film transistors with gate voltage-dependent mobility characteristics," *Solid-St. Electron*, vol. 49, pp. 648–53, 2005.

159. P.-S. Lin, J.-Y. Guo, and C.-Y. Wu, “A quasi-two-dimensional analytical model for the turn-on characteristics of polysilicon thin-film transistors,” *IEEE Trans. Elec. Dev.*, vol. 37, p. 666, 1990.

160. E. Terzini, G. Nobile, S. Loreti, C. Minarini, T. Polichetti, and P. Thilakan, “Influences of sputtering power and substrate temperature on the properties of rf magnetrion sputtered Indium Tin Oxide thin films,” *Jpn. J. Appl. Phys.*, vol. 38, pp. 3448–52, 1999.

161. S. Martin, C.-S. Chiang, J.-Y. Nahm, T. Li, J. Kanicki, and Y. Ugai, “Influence of the amorphous silicon thickness on top-gate thin-film transistor electrical performance,” *Jpn. J. Appl. Phys.*, vol. 40, pp. 530–537, 2001.

162. J. F. Wager, D. A. Keszler, and R. E. Presley, *Transparent Electronics*. New York: Springer, 2008.

163. M. Shur and M. Hack, “Physics of amorphous silicon based alloy field-effect transistors,” *J. Appl. Phys.*, vol. 55, no. 10, pp. 3831–42, 1984.

164. C. Hung, “Contact resistance and stability analysis of oxide-based thin film transistors,” Master’s thesis, Oregon State University, 2006.

165. M. Joshi, R. Pinto, V. R. Rao, and S. Mukherji, “Silinization and antibody immobilization on SU-8,” *App. Surf. Sci.*, vol. 253, pp. 3127–32, 2007.

166. Semi.Org, “SU-8: A versatile material for MEMS manufacturing.” World Wide Web page, http//www.semi.org/mems, 2006.

167. Microchem, “SU-8: Negative tone photoresist.” World Wide Web page, http//www.microchem.com/, 2007.

168. D. Hong and J. F. Wager, “Passivation of zinc tin oxide thin-film transistors,” *J. Vac. Sci. Technol. B*, vol. 23, no. 6, pp. L25–7, 2005.