# *Analysis and design optimization of enhanced swing CMOS LC oscillators based on a phasor based approach*





| | |
|---|---|
| **Citation** | Roy, A. G., Mayaram, K., & Fiez, T. S. (2015). Analysis and design optimization of enhanced swing CMOS LC oscillators based on a phasor based approach. Analog Integrated Circuits and Signal Processing, 82(3), 691-703. doi:10.1007/s10470-015-0490-6 |
| **DOI** | 10.1007/s10470-015-0490-6 |
| **Publisher** | Springer |
| **Version** | Accepted Manuscript |
| **Terms of Use** | http://cdss.library.oregonstate.edu/sa-termsofuse |

**Noname manuscript No.**
(will be inserted by the editor)

# Analysis and Design Optimization of Enhanced Swing CMOS LC Oscillators based on a Phasor Based Approach

**Ankur Guha Roy · Kartikeya Mayaram · Terri S. Fiez**

Received: Aug 19, 2014 / Accepted: Jan 08, 2015

**Abstract** Analysis and design optimization of enhanced swing, low power CMOS LC oscillators is presented. A phasor analysis based approach for determining the amplitude and phase noise of these oscillators is used. MOSFET operation in cut-off, linear and saturation regions is included. The calculated steady state output amplitude and phase noise from this analysis are in good agreement with Cadence Spectre simulations for different bias conditions. Application of this analysis to the design optimization of LC oscillators is demonstrated.

**Keywords** LC oscillator, enhanced swing oscillator, Colpitts oscillator, X-coupled, voltage biased, phase noise, phasor model, ISF, PPV, spectrum conversion, amplitude analysis, design optimization, design oriented analysis, oscillator design.

## 1 Introduction

Wireless Sensor Networks (WSN) have been an important area of research in recent years. A WSN usually consists of numerous independent sensor nodes. The sensor nodes are usually implemented battery free and are powered by energy harvesters, e.g., radio frequency (RF), thermoelectric or piezoelectric power generators. These energy harvesters usually produce sub 0.5 V outputs. A reduction in supply voltage produces many design challenges for analog and RF circuits. Most RF transceivers use an oscillator with low phase noise for frequency generation. In WSN applications, an open loop oscillator is often used as a frequency reference [1]. The phase noise performance of on-chip oscillators suffers drastically from a reduction in the supply voltage. In order to achieve good phase noise performance at a sub 0.5 V supply voltage, output swing enhancement techniques have been developed [1–3]. These enhanced swing oscillators show performance comparable to the state-of-the-art current source biased LC oscillator implementations [4]. Current source biased LC oscillators are extensively used for on-chip applications and their amplitude and phase noise expressions have been analyzed extensively [5–8]. However, no detailed amplitude and phase noise analysis is available for enhanced swing oscillators which are inherently voltage biased oscillators.

In a current biased CMOS oscillator, the transistors are forced to operate in a current limited regime [5]. This ensures that the transistors mostly operate in either the saturation or cut-off region which simplifies the analysis. However, for voltage biased oscillators, MOSFET operation in the triode region adds significant complexity in characterizing their performance. Furthermore, the analysis procedure for finding the amplitude and phase noise of current biased oscillators in [4] cannot be directly applied to the voltage biased, enhanced swing oscillators due to the absence of a tail current source. Even for a current biased Colpitts oscillator, if the transistor is allowed to operate in the triode region for a considerable time, the analysis leads to expressions that are complicated [9] and necessitates the use of a non-linear equation solver.

In [10] it was shown that a phasor based approach can be used to evaluate the oscillation amplitude and phase noise of LC oscillators. In this approach, all voltages and currents are represented as a combination of

School of EECS
Oregon State University
Corvallis, OR 97331
Tel: (541) 737-3617
Fax: (541)-737-1300
E-mail: guharoya@eecs.oregonstate.edu

phasors. The interaction between these phasors in the steady state can be used to evaluate the amplitude. The phase noise can be computed as a result of the interaction of these phasors with the noise sources [11, 12].

Our work, for the first time applies the phasor based approach for amplitude and phase noise analysis to enhanced swing differential and quadrature oscillators. Three enhanced swing oscillator topologies are compared and it is shown that this analysis is effective for these architectures. Our analysis accounts for transistor operation in the triode region and the contribution of $1/f$ noise for phase noise analysis. Prior work in [9], [10] and [13] has addressed these issues partially. In [9] a phasor based amplitude analysis of a current biased Colpitts oscillator with emphasis on triode region operation was proposed but it is not applicable for enhanced swing voltage biased oscillators. We have generalized and extended the method of [9] for the enhanced swing, voltage biased oscillators. In [10], the amplitude of a cross-coupled voltage biased oscillator was analyzed using a level-I MOSFET model and a polynomial approximation. Furthermore, a phasor based noise analysis was developed only for the $1/f^2$ region. In [13] a phasor based phase noise analysis valid for both the $1/f^3$ and $1/f^2$ regions was reported. However, the analysis was only applicable for current biased Colpitts oscillators. Our work extends the noise analysis of [13] to voltage biased enhanced swing oscillators.

Simplified models of amplitude and phase noise of a oscillator, based on device dimensions and component parameters are useful for a circuit designer to find the performance trade-offs. A design tool based on such a model allows for a quick exploration of the design space and to obtain the optimal parameters. However, no such tool exists for the design and optimization of oscillators. A few techniques for oscillator optimization have been reported in [14, 15], where a circuit simulator was used internally to calculate the phase noise and power consumption of an oscillator and can take hours to converge to an optimum solution. By replacing the use of a circuit simulator with a simple MATLAB based algorithm, the optimum design choices can be quickly obtained. We demonstrate the applications of our analysis in a tool for oscillator design optimization. The tool is used for a first pass design estimate without running extensive circuit level simulations enabling fast design of oscillators.

The paper is organized as follows: Section II presents the amplitude analysis of various enhanced swing LC oscillator implementations. Section III outlines the analysis approach for evaluating the phase noise of an enhanced swing LC oscillator. Section IV provides the simulation results and Section V shows the application of the analysis for oscillator design along with an example. Finally, conclusions are drawn in Section VI.

## 2 Amplitude Analysis of CMOS LC Oscillators

An amplitude analysis approach for MOSFET based voltage biased cross-coupled oscillators was discussed in [10], where the non-linear, MOSFET cross-coupled pair characteristics are approximated by a $5^{th}$ order polynomial. In [9] and [16], the amplitudes for current biased Colpitts oscillators and voltage biased cross-coupled oscillators were obtained respectively with the square law MOSFET characteristics requiring no polynomial fitting. In our work, the amplitude is evaluated with the square law MOSFET level-I model. It will be shown later that a level-I MOSFET model can give a good estimate of amplitude and phase noise even for deep sub-micron CMOS processes. The generalized amplitude analysis method valid for both differential and quadrature oscillators is described next.

### 2.1 Amplitude Evaluation for Differential Oscillators

The two oscillators analyzed in this section are the Enhanced Swing Differential Colpitts (ESDC) oscillator [2] and the cross-coupled Colpitts (XCC) oscillator [1] with a DC bias shift. They are shown in Fig. 1(a) and (b). The single-ended equivalent circuit is shown in Fig. 1(c).

The MOSFET based oscillators can be mapped from the original circuit in terms of a drain-to-gate feedback factor ($k$), drain-to-source feedback factor ($n$) and an equivalent capacitance $C_e$ at the drain. By selecting a $C_{bias} \gg c_{gs}$, in Fig. 1(b), $n$ and $C_e$ can be expressed as,

$$n = \frac{C_1}{C_1 + C_2};\ C_e = \frac{C_1 C_2}{C_1 + C_2} \tag{1}$$

where $C_2$ is the equivalent capacitance at the source of the MOSFET and is given by, $C_2 = \quad C_{2S} - \frac{1}{\omega_o^2 L_2}$. $k$ is 0 for an ESDC oscillator and 1 for an XCC oscillator.

The oscillation frequency ($\omega_o$) of the oscillators can be shown to be [2],

$$\omega_o \approx \frac{1}{\sqrt{L_1 C_e}} \tag{2}$$

Assuming a nearly sinusoidal oscillation, the output signal for an oscillator can be approximated by $A\cos(\omega t)$ where $A$ is the amplitude of oscillation. If the tank circuit has a sufficiently high quality factor ($Q > 3$) this assumption is valid [9]. The drain, source and gate voltages can be approximated by,

$$V_d = V_D - A\cos\theta;\quad V_s = -nA\cos\theta;\quad V_g = V_G + kA\cos\theta$$

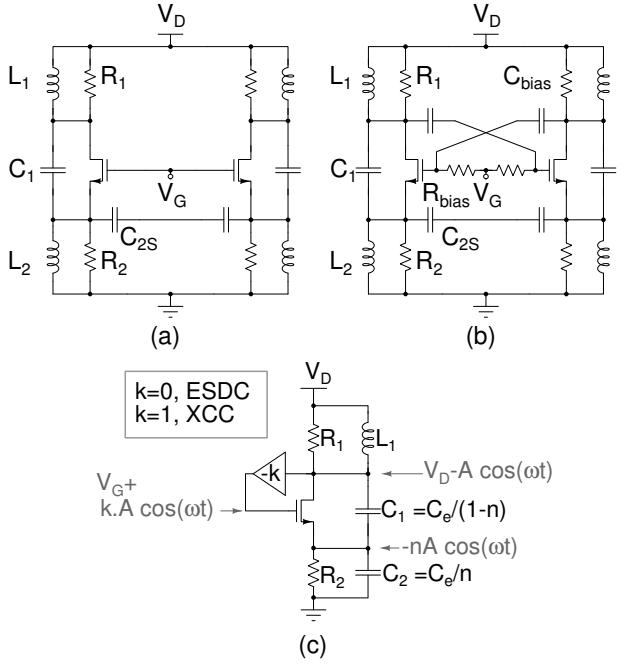


**Fig. 1** Differential oscillator architectures. (a) ESDC oscillator. (b) XCC oscillator with a DC bias shift. (c) Single ended equivalent circuit.

(3)

where $\theta = \omega t$ and it is assumed that the impedance of $C_2$ at the oscillation frequency is much lower than the impedance looking into the source of $M_1$. A careful design choice can ensure this.

In a voltage biased oscillator, the transistors in the circuit can operate in all three regions: saturation, triode and cut-off respectively. Assuming a Level-1 MOSFET model the transistor current can be expressed as,

$$I_d(\theta) = \begin{cases} \frac{k'}{2}\frac{W}{L}[2(V_{gs}(\theta)-V_T)-V_{ds}(\theta)] & , \text{ linear} \\ \qquad V_{ds}(\theta)(1+\lambda V_{ds}(\theta)) & \\ \frac{k'}{2}\frac{W}{L}(V_{gs}(\theta)-V_T)^2(1+\lambda V_{ds}(\theta)) & , \text{ saturation} \\ 0 & , \text{ cut}-\text{off} \end{cases} \tag{4}$$

where, $k' = \mu_n C_{ox}$ is a constant, $V_T$ and $\lambda$ are the threshold voltage and the channel length modulation parameter of the transistor, respectively.

In order to simplify the expressions, two angles $\theta_c$ and $\theta_n$ are defined. They signify the saturation–cut-off boundary and the triode–saturation boundary, respectively. The transistor turns on if $V_{gs} \geq V_T$. This translates to $\theta_c = \cos^{-1}\left[\frac{V_T - V_G}{(n+k)A}\right]$. Similarly, the transistor operates in the triode region if $V_{gd} \geq V_T$. This implies $\theta_n = \cos^{-1}\left[\frac{V_D-(V_G-V_T)}{(1+k)A}\right]$. Therefore, the MOSFET operates in the cut-off region for $\theta_c \leq \theta \leq 2\pi - \theta_c$. Similarly, it operates in the triode region for $0 \leq \theta \leq \theta_n$ and $(2\pi - \theta_n) \leq \theta \leq 2\pi$. A time varying small-signal transconductance, $g_m(\theta)$ and a small-signal output conductance, $g_{ds}(\theta)$ for the transistor can be expressed as,

$$g_m(\theta) = \frac{\partial I_d(\theta)}{\partial V_{gs}(\theta)} = \begin{cases} k'\frac{W}{L}V_{ds}(\theta) & , \text{ linear} \\ k'\frac{W}{L}\left[V_{gs}(\theta)-V_T\right] & , \text{ saturation} \\ 0 & , \text{ cut}-\text{off} \end{cases} \tag{5}$$

$$g_{ds}(\theta) = \frac{\partial I_d(\theta)}{\partial V_{ds}(\theta)} = \begin{cases} k'\frac{W}{L}\left[V_{gs}(\theta)-V_T\right] & , \text{ linear} \\ \lambda I_d(\theta) & , \text{ saturation} \\ 0 & , \text{ cut}-\text{off} \end{cases} \tag{6}$$

$I_d(\theta)$, $g_m(\theta)$ and $g_{ds}(\theta)$ are periodic and can be expressed in terms of their Fourier series components $I_D[n\omega_o]$, $G_M[n\omega_o]$ and $G_{DS}[n\omega_o]$, respectively. For example,

$$I_d(\theta) = \sum_{n=-\infty}^{\infty} I_D[n\omega_o]e^{jn\theta} \tag{7}$$

If $A$ is a known quantity, the time-domain waveforms of $I_d(\theta)$, $g_m(\theta)$ and $g_{ds}(\theta)$ can be evaluated in terms of $A$ using Eqs. (3), (4), (5) and (6). $I_D[n\omega_o]$, $G_M[n\omega_o]$ and $G_{DS}[n\omega_o]$ can be evaluated analytically, as in [9]. Since the objective of our work is to implement a MATLAB based toolbox, the computational effort can be reduced by evaluating the harmonics numerically using the MATLAB FFT function [17] from the time-domain waveforms of $I_d(\theta)$, $g_m(\theta)$ and $g_{ds}(\theta)$.

Evaluation of the oscillation amplitude for an LC oscillator requires simultaneously solving two sets of boundary conditions [9]. The first boundary condition is the following: if the oscillator is operating at resonance, the load seen at the transistor's drain is purely resistive at the oscillation frequency. The fundamental component of the drain current passes through this resistor and causes the output voltage swing. Therefore, by following a methodology similar to [9], the steady state amplitude $A$ of an ESDC or XCC oscillator can be expressed as,

$$A = \quad (1-n)I_D[\omega_o]R_p \tag{8}$$

where $R_p$ is the parallel tank resistance given by,

$$R_p = R_1||(R_2/n^2) \tag{9}$$

This equation is valid under the assumption that $R_2$ does not considerably load the capacitive divider created by $C_1$ and $C_2$, which can be ensured by a careful design.

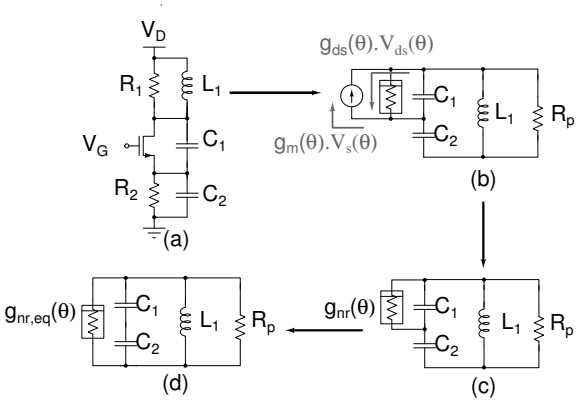


**Fig. 2** Evaluation of the equivalent negative resistance. (a) ESDC oscillator. (b) $g_m(\theta)$ and $g_{ds}(\theta)$. (c) $g_{nr}(\theta)$: equivalent conductance of the combination of $g_m(\theta)$ and $g_{ds}(\theta)$. (d) $g_{nr,eq}(\theta)$: scaled version of $g_{nr}(\theta)$ in parallel with the RLC tank.

Next consider the second boundary condition. In a current biased oscillator, the average current through the transistor is determined by the tail current source [9]. If the tail current source value is known, the second boundary condition can be established by setting this value equal to the average current flowing through the transistor. Enhanced swing oscillators are voltage biased and do not have a fixed bias current. If a voltage biased oscillator is designed such that the transistor is initially biased in saturation, the amplitude would increase progressively. Eventually, the MOSFET is pushed into the triode region. As the device spends more time in the triode region, it introduces an average loss component across the tank. The oscillation amplitude builds up until the point where the power driven by the transistor, $\overline{P_{nr}}$ (modeled by a negative resistance) is fully compensated by the power dissipated through the resistive load $R_p$, $\overline{P_{diss}}$ .

Therefore, the second boundary condition is given by,

$$\overline{P_{diss}} = \overline{P_{nr}} \tag{10}$$

As shown in [10], simplifying (10) yields the following result,

$$\frac{1}{R_p} = -G_{NR,eff} \tag{11}$$

where $G_{NR,eff}$ is a quantity called the "effective conductance" of the non-linearity.

In the ESDC oscillator in Fig. 2(a) there are two time varying resistances $g_m(\theta)$ and $g_{ds}(\theta)$ both of which can be evaluated using the Level-1 model as shown in Eqs. (5) and (6). The effect of these two conductances can be combined into a single time varying conductance $g_{nr}(\theta)$ as shown in Figs. 2(b) and (c). The value of $g_{nr}(\theta)$ can be expressed in terms of $g_m(\theta)$ and $g_{ds}(\theta)$ as [10],

$$g_{nr}(\theta) = -\frac{n}{(1-n)} g_m(\theta) + g_{ds}(\theta) \tag{12}$$

If the transistor non-linearity can be expressed as a time varying conductance $g_{nr,eq}(\theta)$ across the the RLC tank shown in Fig. 2(d) then $g_{nr,eq}(\theta)$ can be found from Fig. 2(c) by observing that this conductance appears across a capacitive divider formed by $C_1$ and $C_2$. By an impedance transformation,

$$g_{nr,eq}(\theta) = (1-n)^2 g_{nr}(\theta) \tag{13}$$

It can be shown that the effective conductance defined in Eq. (11) is given by [10],

$$G_{NR,eff} = \quad G_{NR,eq}[0] - G_{NR,eq}[2\omega_o] \tag{14}$$

where $G_{NR,eq}[n\omega_o]$ is the $n^{th}$ Fourier coefficient of the time varying conductance $g_{nr,eq}(\theta)$. $G_{NR,eff}$ includes the loss component introduced by the MOSFET in the triode region of operation.

According to Eqs. (5) and (6), $g_m(\theta)$ and $g_{ds}(\theta)$ are functions of $A$. As $G_{NR,eff}$ is dependent on $g_m(\theta)$ and $g_{ds}(\theta)$ it is also a function of $A$. If $A$ is a known quantity, $G_{NR,eff}$ can be evaluated using the Level-1 MOSFET equations described above.

If the two boundary conditions in Eq. (8) and Eq. (11) are solved simultaneously the exact value of the amplitude can be determined. However, both $I_D[\omega_o]$ and $G_{NR,eff}$ are implicitly functions of $A$ and cannot be solved analytically. Alternatively these equations can be solved numerically with the optimization toolbox in MATLAB. Eqs. (8) and Eq. (11) can be merged into a single equation, $C(A)$ as follows,

$$C(A) = \left(A - (1-n)\, I_D[\omega_o] R_p\right)^2 + \left(G_{NR,eff} + \frac{1}{R_p}\right)^2 \tag{15}$$

Ideally $C(A)$ is zero if Eqs. (8) and (11) are satisfied simultaneously, i.e., the correct value of $A$. The optimization toolbox of MATLAB computes $C(A)$ for different values of $A$ and finds the value of $A$ for which $C(A)$ is zero.

### 2.2 Amplitude Evaluation for Quadrature Oscillators

The enhanced swing quadrature (ESQ) oscillator shown in Fig. 3(a) was reported in [3] as an extension of the ESDC oscillator for quadrature generation. In [3] the quadrature component ($Q$) leads the in-phase component ($I$) and this is ensured by a capacitive coupling circuit.

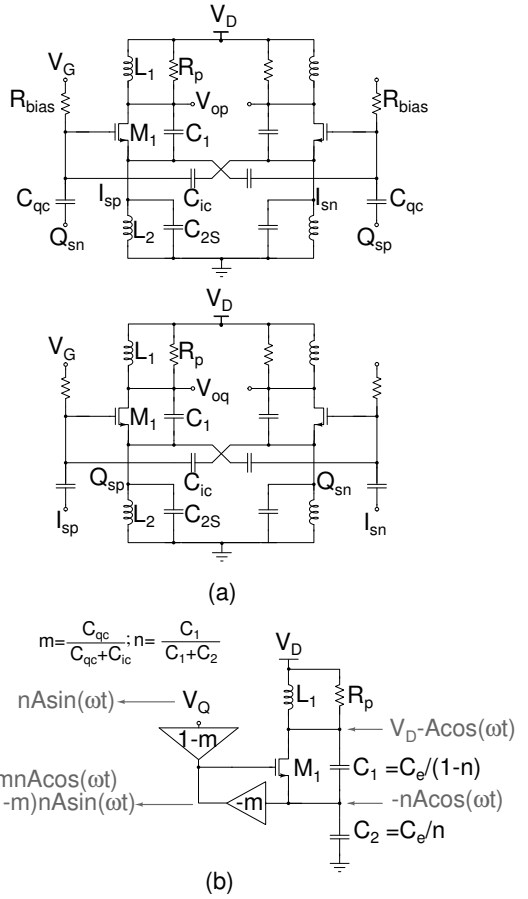


**Fig. 3** ESQ oscillator. (a) Architecture. (b) Single-ended equivalent circuit representation.

The amplitude of an ESQ oscillator can be evaluated by using a single-ended equivalent circuit as shown in Fig. 3(b).

To facilitate the calculations, two quantities: coupling factor ($m$) and feedback factor ($n$) are defined as follows:

$$m = \frac{C_{qc}}{C_{qc}+C_{ic}}, \quad n = \frac{C_1}{C_1+C_2} \tag{16}$$

From Fig. 3 it can be seen that if the oscillation amplitude is $A$, then

$$\begin{aligned} V_{gs}(\theta) &= \begin{array}{l} V_G + (mn+n)A\cos(\theta) \\ \quad +(1-m)nA\sin(\theta) \end{array} \\ &= V_G + R_1\cos(\theta-\alpha_1) \\ V_{gd}(\theta) &= \begin{array}{l} V_G - V_D + (m.n+1)A\cos(\theta) \\ \quad +(1-m)nA\sin(\theta) \end{array} \\ &= V_G - V_D + R_2\cos(\theta-\alpha_2) \\ V_{ds}(\theta) &= V_D - (1-n)A\cos(\theta) \end{aligned} \tag{17}$$

The constants $R_1$, $R_2$, $\alpha_1$ and $\alpha_2$ are given by,

$$\begin{aligned} R_1 &= An\sqrt{(1+m)^2+(1-m)^2} \\ R_2 &= A\sqrt{(1+mn)^2+n^2(1-m)^2} \end{aligned} \tag{18}$$

$$\alpha_1 = \tan^{-1}\left(\frac{1-m}{1+m}\right); \qquad \alpha_2 = \tan^{-1}\left(\frac{n-mn}{1+mn}\right)$$

It can be concluded that $V_{gs}$ and $V_{ds}$ are slightly phase skewed (say by an angle $\phi_e$). The fundamental component of $I_d$ (denoted as $I_D[\omega_o]$) is in phase with $V_{gs}$ and can be expressed as,

$$I_D[\omega_o] = |I_D[\omega_o]|\angle\phi_e \tag{19}$$

$I_D[\omega_o]$ can be evaluated if $V_{gs}(\theta)$ and $V_{ds}(\theta)$ are known.

At the oscillation frequency, the resonant tank circuit compensates for $\phi_e$ by providing an extra phase shift, $-\phi_e$. The tank impedance can be expressed as,

$$\begin{aligned} Z = \frac{1}{\frac{1}{R_p}+j\omega C_e+\frac{1}{j\omega L_1}} &= \frac{1}{\sqrt{\frac{1}{R_p^2}+\left(\omega C_e-\frac{1}{\omega L_1}\right)^2}}\angle-\phi_e \\ &= R_p\cos(\phi_e)\angle-\phi_e \end{aligned} \tag{20}$$

where $\phi_e = \tan^{-1}\left[R_p\left(\omega C_e - \frac{1}{\omega L_1}\right)\right]$ .

From Eqs. (20) and (19) the oscillation amplitude can be approximated by,

$$\begin{aligned} A = \quad (1-n)\,|I_D[\omega_o]Z| &= (1-n)\,|I_D[\omega_o]|\,R_p\cos(\phi_e) \\ &= (1-n)\,Re\{I_D[\omega_o]\}R_p \end{aligned} \tag{21}$$

The in-phase component of $I_D[\omega_o]$ with $V_{ds}$, i.e., $Re\{I_D[\omega_o]\}$ directly gives $|I_D[\omega_o]|\cos(\phi_e)$.

Following a methodology similar to the differential oscillators, two angles $\theta_c$ and $\theta_n$ can be defined. The MOSFET is ON if $V_{gs} \geq V_T$ and it operates in the triode region if $V_{gd} \geq V_T$. These two conditions translate to $\theta_c = \cos^{-1}\left[\frac{V_T-V_G}{R_1}\right]$ and $\theta_n = \cos^{-1}\left[\frac{V_D-(V_G-V_T)}{R_2}\right]$, respectively. Therefore, the MOSFET operates in the cut-off region for $\theta_c \leq (\theta-\alpha_1) \leq 2\pi-\theta_c$. Similarly, the MOSFET operates in the triode region for $0 \leq \theta-\alpha_2 \leq \theta_n$ and $(2\pi-\theta_n) \leq (\theta-\alpha_2) \leq 2\pi$.

The second boundary condition can be formed by following a similar approach as in Eq. (10). Since the output waveform is $A\cos(\omega_o t)$, only the real part of $G_{NR,eff}$ contributes to power loss.

$$\frac{1}{R_p} = -Re\{G_{NR,eff}\} \tag{22}$$

Therefore, the cost function, $C(A)$ for optimization in this context is obtained from Eqs. (21) and (22) following a similar approach as in Eq. (15) and it is given by,

$$C(A) = \begin{aligned}&\left(A-(1-n)\,.Re\{I_D[\omega_o]\}.R_p\right)^2 \\ &+\left(Re\{G_{NR,eff}\}+\frac{1}{R_p}\right)^2\end{aligned} \tag{23}$$

As in the differential oscillators $C(A)$ can be optimized in terms of $A$ to get an accurate estimate of $A$.

## 3 Phase Noise Analysis of A Low Voltage, Enhanced Swing LC Oscillator

The most popular approach to derive an analytical phase noise model of an oscillator is the linear time varying (LTV) analysis. There have been several LTV analysis based models reported in literature [5,10]. Among these the impulse sensitivity function (ISF) based model [5] is a popular one. An ISF based approach using simulations can be applied for enhanced swing oscillators. However, to reduce the computational effort, the phasor results calculated in the last section ($G_M[n\omega_o]$, $G_{DS}[n\omega_o]$ and $I_D[n\omega_o]$) can be exploited for evaluating the phase noise.

In our approach the analysis of [13] was used and has been generalized to voltage biased oscillators. Furthermore, the thermal and flicker noise contributions from the transistor operating in saturation, triode and cut-off regimes is included.

If the oscillator is used as a voltage controlled oscillator (VCO), the additional varactor may introduce additional phase noise at the oscillator output by AM-PM conversion. The exact AM-PM conversion mechanism and its calculation was reported in [18]. In order to simplify the procedure, this effect is neglected in the subsequent analyses. However, the analysis can be extended to include AM-PM conversion. The assumption that the AM-PM conversion is not the dominant noise contributor for a voltage biased oscillator was shown in [19].

There are three noise generators in the single ended equivalent circuit of the ESDC, XCC and ESQ oscillators: $R_1$, $R_2$ and $M_1$. The noise sources are shown in Fig. 4. The effect of $R_1$ and $R_2$ can be combined into a single equivalent resistance $R_p$ as defined in Eq. (9). The contributions of noise sources $i_{n,R_p}$ and $i_{n,M_1}$ to the output current noise through the tank can be evaluated by using a Norton equivalent circuit.

$$\frac{i_{on,M_1}}{i_{n,R_p}}=1;\quad \frac{i_{on,R_p}}{i_{n,M_1}}=(1-n) \tag{24}$$

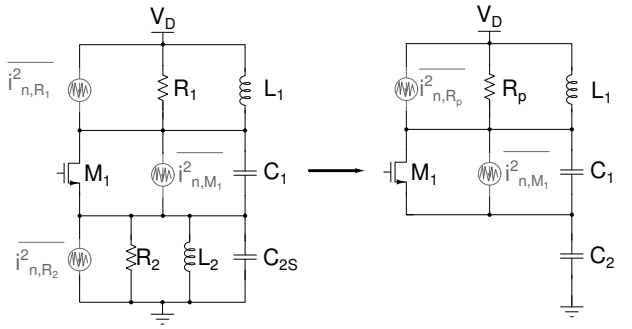


**Fig. 4** Output noise sources in the single-ended equivalent circuit of the enhanced swing oscillators (ESDC, XCC, ESQ).

where $n$ is the feedback factor defined in Eq. (1), $i_{on,M_1}$ and $i_{on,R_p}$ are the contributions of $i_{n,M_1}$ and $i_{n,R_p}$ to the output node, respectively.

The noise contribution of $M_1$ can be modeled as a current-noise source between the source and the drain. This noise source has thermal and flicker noise components.

$$\overline{i^2_{n,M_1}}=\overline{i^2_{n,thermal}}+\overline{i^2_{n,flicker}} \tag{25}$$

The time varying thermal noise power spectral density (PSD) can be expressed as a current noise between the drain and the source of a transistor,

$$\overline{i^2_{n,thermal}}(\theta)=4kT\gamma g_m(\theta)+4kTg_{ds}(\theta)\quad=4kT\gamma g(\theta) \tag{26}$$

where $\gamma$ is the excess noise factor of the transistor, $k$ is the Boltzmann's constant, $T$ is the absolute temperature and $g(\theta)$ is defined as,

$$g(\theta)=g_m(\theta)+\frac{g_{ds}(\theta)}{\gamma} \tag{27}$$

Assuming $\gamma\approx 1$,

$$g(\theta)\approx g_m(\theta)+g_{ds}(\theta) \tag{28}$$

For a Level-1 MOSFET model,

$$\begin{aligned} g_m(\theta)|_{triode} &\ll g_{ds}(\theta)|_{triode}\\ g_{ds}(\theta)|_{saturation} &\ll g_m(\theta)|_{saturation}\\ g_m(\theta)|_{saturation} &\approx g_{ds}(\theta)|_{triode}\end{aligned} \tag{29}$$

whereby,

$$g(\theta)=\begin{cases}k'\frac{W}{L}\left[V_{gs}(\theta)-V_T\right] & \text{on}\\ 0 & \text{cut}-\text{off}\end{cases} \tag{30}$$

The approximate expression of $g(\theta)$ in Eq. (28) deviates from the actual value in Eq. (27) depending on the value of $\gamma$. When the transistor operates in the saturation region, the two expressions yield the same result.

In the triode region the two expressions differ by the factor $\gamma$. $\gamma$ usually varies between $\frac{2}{3}$ to 1.1, depending on the channel length. The thermal noise expression of Eq. (26) with $g(\theta)$ approximated by Eq. (30) can thus overestimate the noise by $10\log(\gamma) \approx 1.6\,\text{dB}$ in the triode region. However in an oscillator, the MOSFET periodically operates from saturation, triode, to cut-off and vice versa. The transistor spends only a fraction of the overall time period in the triode region [20]. Therefore, the thermal noise estimation error would be much smaller than 1.6 dB.

A periodically time varying noise source can be modeled as a stationary noise source which is modulated by a periodic time varying waveform. If $g(\theta)$ and $I_d(\theta)$ have maximum values $g_{max}$ and $I_{d,max}$ respectively, then the modulating waveforms for the thermal noise and flicker noise sources are $g_{norm}(\theta) = \frac{g(\theta)}{g_{max}}$ and $I_{d,norm}(\theta) = \frac{I_d(\theta)}{I_{d.max}}$, respectively. The stationary current noise sources were modeled as $4kT\gamma g_{max}$ and $\frac{k_{flicker} I_{d,max}}{f^\alpha}$ respectively. $I_{d,max}$ is the maximum current flowing through the MOSFET.

The modeling of a time varying noise source by an equivalent stationary noise source modulated by a periodic time varying waveform is shown in Fig. 5(a). The noise modulation procedure in the time domain can be viewed as a convolution in the frequency domain. Any periodic signal can be expressed as a combination of its Fourier series components. Let the $n^{th}$ harmonic components of $g_{norm}(\theta)$ and $I_{d,norm}(\theta)$ be $G_{norm}[n\omega_o]$ and $I_{D,norm}[n\omega_o]$. A stationary white noise source has noise components at all possible frequencies including $(n\omega_o \pm \Delta\omega)$. These components are convolved by $G_{norm}[(n-1)\omega_o]$ and $G_{norm}[(n+1)\omega_o]$ and are shifted to $(\omega_o \pm \Delta\omega)$ [13]. Fig. 5(b) illustrates this concept. Since the thermal noise source is white, all harmonic components of $g_{norm}(\theta)$ contribute to phase noise through this mechanism.

The SSB current noise spectral density at $(\omega_o + \Delta\omega)$ due to all of the harmonic components can be expressed as [13],

$$\begin{aligned}\overline{i^2_{n,thermal}} &= 4kT\gamma g_{max} \sum_{n=1}^{\infty} |G_{norm}[(n-1)\omega_o] \\ &\qquad + G_{norm}[(n+1)\omega_o]|^2 \\ &= \frac{4kT\gamma}{g_{max}} \sum_{n=1}^{\infty} |G[(n-1)\omega_o] + G[(n+1)\omega_o]|^2\end{aligned} \tag{31}$$

Similarly, the effective translated flicker noise current to the output at $(\omega_o + \Delta\omega)$ between the drain and the source of the MOSFET can be expressed as,

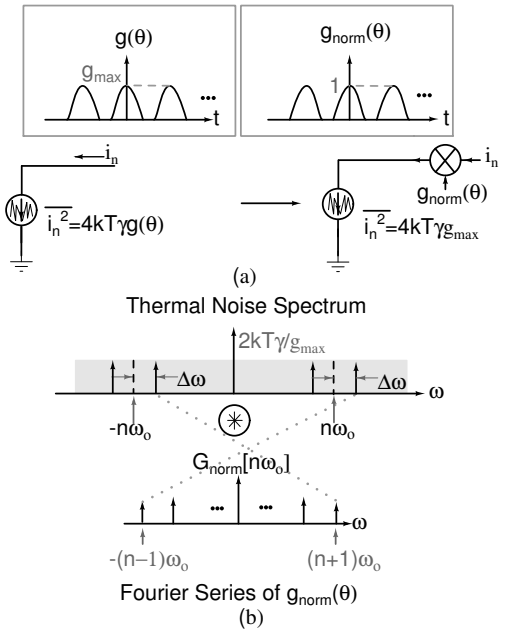


**Fig. 5** (a) Modeling a time varying noise source as a stationary noise source modulated by a periodic waveform. (b) Mixing of noise by the modulating waveform.

$$\begin{aligned}\overline{i^2_{n,flicker}} &= \frac{k_{flicker} I_{d,max}}{f^\alpha} \frac{1}{4} |I_{D,norm}[-\omega_o] + I_{D,norm}[\omega_o]|^2 \\ &= \frac{k_{flicker}}{I_{d,max} f^\alpha} \frac{1}{4} |I_D[-\omega_o] + I_D[\omega_o]|^2\end{aligned} \tag{32}$$

This extra 1/4 factor in Eq. (32) takes into account the correlation of different sidebands [13].

The noise source values in Fig. 4 are,

$$\overline{i^2_{n,M_1}} = I_{eff} \frac{k_{flicker}}{f^\alpha} + 4kT\gamma G_{eff} \quad ; \quad \overline{i^2_{n,R_p}} = \frac{4kT}{R_p} \tag{33}$$

where

$$\begin{aligned} G_{eff} &= \frac{1}{g_{max}} \sum_{n=1}^{\infty} |G[(n-1)\omega_o] + G[(n+1)\omega_o]|^2 \\ I_{eff} &= \frac{1}{I_{d,max}} \frac{1}{4} |I_D[-\omega_o] + I_D[\omega_o]|^2 \end{aligned} \tag{34}$$

Using Eq. (24) the total output current noise is given by,

$$\overline{i^2_{o,noise}} = \overline{i^2_{n,M_1}} (1-n)^2 + \overline{i^2_{n,R_p}} \tag{35}$$

This output noise current flows through the tank circuit and gets converted to voltage noise. If the tank has a quality factor $Q$, the output impedance of the

tank circuit at an offset frequency $\Delta\omega$ from the carrier $\omega_o$ can be approximated by,

$$Z(\omega_o + \Delta\omega) \approx \frac{jR_p\omega_o}{2Q\Delta\omega} \tag{36}$$

where the tank quality factor at the oscillation frequency is,

$$Q = \frac{R_p}{\omega_o L_1} \tag{37}$$

The output voltage noise power spectral density is,

$$\overline{v_{o,noise}^2} = \overline{i_{o,noise}^2}\left(\frac{R_p^2\omega_o^2}{4Q^2\Delta\omega^2}\right) \tag{38}$$

The voltage noise gets converted to phase noise by a non-linear mechanism [21,22]. It is assumed that only half of the total voltage noise power contributes to the output phase noise. This is commonly known as the equi-partition theorem [5]. The equi-partition theorem usually holds for white thermal noise. For slow frequency noise sources such as $1/f$ noise, the contribution of the time varying flicker noise to the output phase noise depends on the oscillator architecture. An exact procedure to find the flicker noise contribution to the output phase noise for a voltage biased cross-coupled oscillator using an ISF based analysis was presented in [19]. Although this method can be extended for enhanced swing oscillators, the purpose of our analysis is to get a fast estimation of the output phase noise within an error margin. For the oscillator architectures discussed in this paper, the equi-partition assumption overestimates the output phase noise within a 3 dB accuracy in the flicker noise dominated region. A similar approach was used in [13].

The voltage noise contribution to the output signal phase is thus expressed as,

$$\overline{v_{o,noise,PM}^2} = \left(\frac{1}{2}I_{eff}\frac{k_{flicker}}{f^\alpha} + 2kT\gamma G_{eff}(1-n)^2 + \frac{2kT}{R_p}\right)\cdot\left(\frac{R_p^2\omega_o^2}{4Q^2\Delta\omega^2}\right) \tag{39}$$

The phase noise expression of the single-ended equivalent circuit can be obtained by normalizing $\overline{v_{o,noise,PM}^2}$ with respect to the oscillation amplitude,

$$L\{\Delta\omega\}|_{\text{single-ended}} = 10\log\left(\frac{\overline{v_{o,noise,PM}^2}}{A^2/2}\right) \tag{40}$$

The differential oscillator circuit has 3 dB less noise compared to this single-ended phase noise equivalent circuit since the individual noise sources are uncorrelated. Therefore, the final phase noise expression for the differential oscillator circuit can be expressed as,

$$L\{\Delta\omega\}|_{\text{differential}} = 10\log\left(\frac{\overline{v_{o,noise,PM}^2}}{A^2/2}\right) - 3 \tag{41}$$

The analysis of the phase noise described above has been derived in terms of the time varying function $g(\theta)$ given by, Eq. (30) in the thermal noise dominated region. $g(\theta)$ depends only on the gate-source voltage ($V_{gs}(\theta)$). Therefore, the phase noise expression in Eq. (41) can be used for ESDC, XCC and ESQ oscillators with the required modifications in $V_{gs}(\theta)$ to account for the noise effects of the MOSFET. The noise contributions of $R_1$ and $R_2$ remain unchanged for all the architectures. However, unlike the ESDC oscillator, the XCC and ESQ oscillators have an extra noise generator: the bias shifting resistance ($R_{bias}$) as shown in Fig. 1. A careful design choice of $R_{bias}$ can reduce its contribution to the output phase noise eventually making it considerably less than the other noise generators. To understand the design trade-offs, we need to examine how the $R_{bias}$ noise affects the circuit's noise response. $R_{bias}$ can affect the output phase noise in two ways. At high frequencies this resistance effectively appears in parallel with $R_p$. If, $R_{bias}$ is chosen one order of magnitude higher than $R_p$, its contribution to the output noise can be neglected. At low offset frequencies, $C_{bias}$ ($C_{ic}$ and $C_{qc}$ for the ESQ oscillator in Fig. (3)) acts like an open circuit. So, $R_{bias}$ is not connected to $R_p$. Thermal noise generated by $R_{bias}$ near dc can be translated to the output phase noise by modulation of the time varying $g_m(\theta)$ of the transistor. If $C_{bias}$ ($C_{ic}$ and $C_{qc}$) is chosen sufficiently high, the noise generated by $R_{bias}$ at close-in offset frequencies is filtered out and its effect to the output is negligible. Therefore, sufficiently large values of $R_{bias}$ and $C_{bias}$ ensure that the phase noise expression in Eq. (41) holds for XCC and ESQ oscillators without any modification.

## 4 Analysis Verification With Simulation Results

All of the oscillators discussed in Sections II and III were designed with a 5.5 GHz center frequency. In this section their amplitude and phase noise characteristics are discussed.

The selected component values of the ESDC oscillator are shown in Table 1. These values were chosen in order to compare it with the oscillator reported in [2] which was fabricated in an IBM130 RF-DM process.

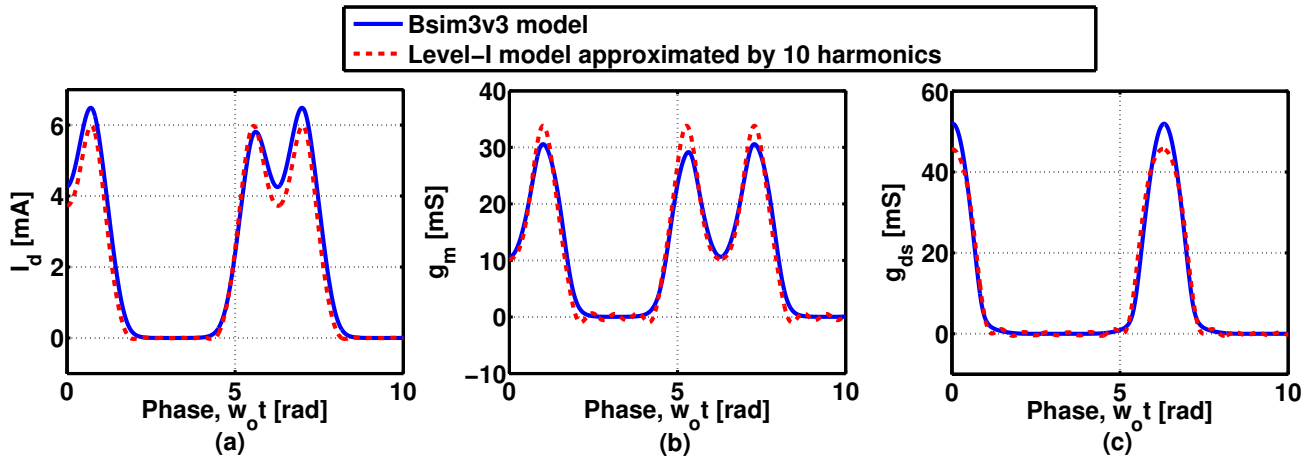


**Fig. 6** Waveforms of the small-signal time varying components and their approximation with the first 10 harmonics. (a) $I_d(t)$. (b) $g_m(t)$. (c) $g_{ds}(t)$.

**Table 1** Component Values and Extracted Parameter Values

| Component Name | Value | Model Parameter | Value |
|---|---|---|---|
| $L_1$ | 0.69 nH | $V_{Tn}$ | 0.21 V |
| $L_2$ | 1.25 nH | $k' = (\mu_n C_{ox})$ | 410 $\mu$A/V$^2$ |
| $C_1$ | 1.858 pF | $\lambda$ | 0.46 V$^{-1}$ |
| $C_{2S}$ | 2.704 pF | $\gamma$ | 1.14 |
| $R_1$ | 450 $\Omega$ | $k_{flicker}$ | $1.55 \times 10^{-13}$ A |
| $R_2$ | 550 $\Omega$ | $\alpha$ | 0.86 |
| $\left(\frac{W}{L}\right)_{MOS}$ | $\frac{80\,\mu m}{0.24\,\mu m}$ | - | - |

The extracted transistor parameters from the BSIM3v3 MOSFET model are also shown in the table.

For a direct comparison, the XCC oscillator was designed with the same component values as the ESDC oscillator. The extra resistor ($R_{bias}$) and capacitor ($C_{bias}$) in the level-shifter path were chosen to be 100 k$\Omega$ and 5 pF, respectively. The ESQ oscillator was designed with the same component values as the ESDC oscillator. The coupling capacitors $C_{ic}$ and $C_{qc}$ in Fig. 3 were chosen as 500 fF and $R_{bias} = 1$ k$\Omega$. The differential and quadrature oscillators were simulated for $V_G = 300$ mV and $V_D = 500$ mV. The $I_d$, $g_m$ and $g_{ds}$ waveforms for the ESDC oscillator are shown in Fig. 6.

It is seen from Fig. 6 that harmonics above the $10^{th}$ harmonic can be neglected. Therefore, the series in Eq. (34) can be truncated after the first 10 terms for all practical purposes.

### 4.1 Amplitude Results

Spectre simulated amplitude results with the BSIM3V3 transistor model were compared to the analytical results. The comparisons are shown in Figs. 7(a), (b) and (c).

For both the ESDC and XCC oscillators, the predicted amplitude is within 12 % of the simulated value. From the plots, it is seen that the XCC oscillator has a higher amplitude compared to the ESDC oscillator for the same bias conditions.

The predicted amplitude of ESQ oscillator is within 16 % of the simulation results. This behavior can be attributed to the $c_{gs}$ and $c_{gd}$ of the transistors. The coupling capacitors $C_{qc}$ and $C_{ic}$ in Fig. 3 form a potential divider with $c_{gs}$ and $c_{gd}$. This reduces the signal swing at the gate of the transistors. This swing reduction at the gate also reduces the effective transconductance $g_m(\theta)$ of the transistor and consequently reduces the amplitude of oscillation.

### 4.2 Phase Noise Results

The phase noise of the three oscillators was calculated using Eq. (41). The analysis and simulated values of phase noise for the three oscillators are shown in Fig. 8. In all cases the phase noise in both the thermal and flicker noise dominated regions is predicted with an accuracy of 3 dB.

The XCC oscillator shows approximately 2.5 dB better phase noise performance than the ESDC oscillator in the thermal noise dominated region.

The phase noise of the ESDC oscillator at a 3 MHz offset frequency for a fixed gate bias and varying $n$ is shown in Fig. 9. The gate bias is kept sufficiently high (at 400 mV for all simulations) to ensure start-up for all possible values of $n$. The observed trend of phase noise in this figure is monotonically decreasing. A similar trend can be seen from the phasor based analysis in Section III. *Fig. 9 shows that the phase noise minimum for a current biased Colpitts oscillator at a feedback fac-*

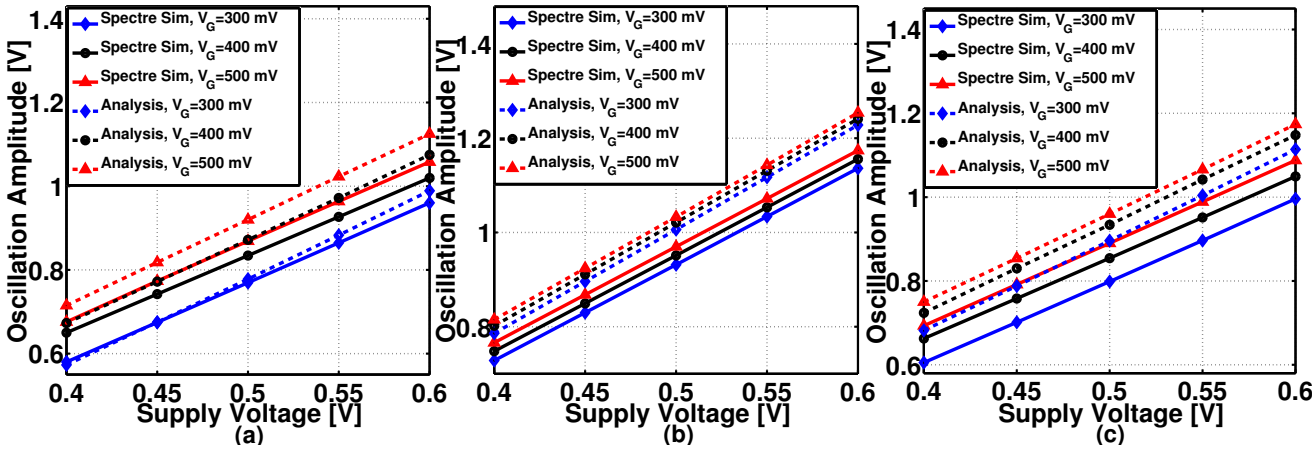


**Fig. 7** oscillator output amplitude variation with supply voltage for different gate biases. (a) ESDC. (b) XCC. (c) ESQ.

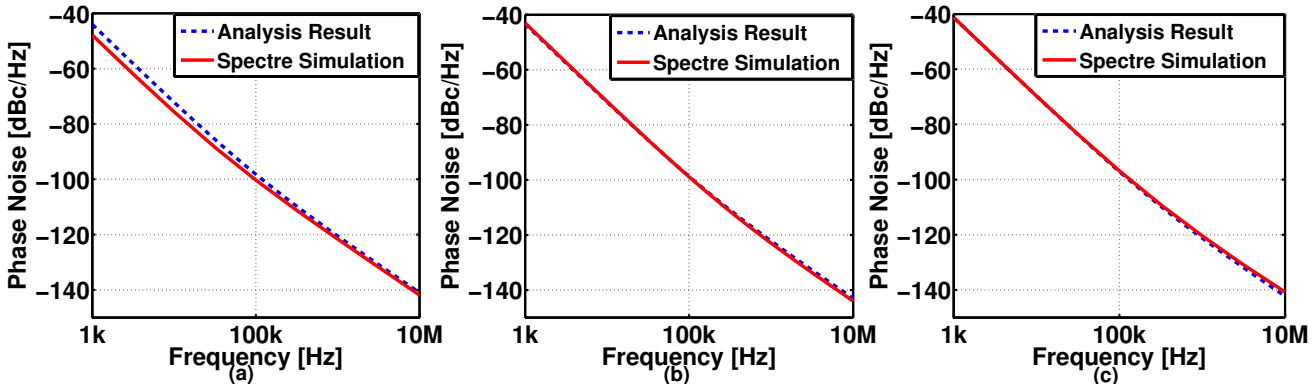


**Fig. 8** Phase noise for different oscillator architectures. (a) ESDC. (b) XCC. (c) ESQ.

*tor, $n \approx 0.3$ reported in [4] does not hold for a voltage biased Colpitts oscillator.*

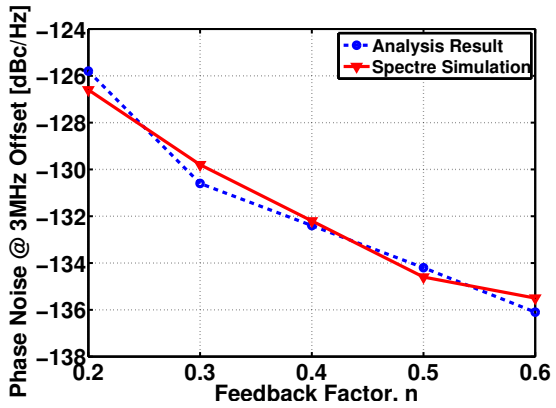


**Fig. 9** Phase noise at 3 MHz offset frequency with different feedback factors for the ESDC oscillator.

The phase noise results of the ESDC oscillator with this analysis matches well with the fabricated chip results in [2] shown in Fig. 10.

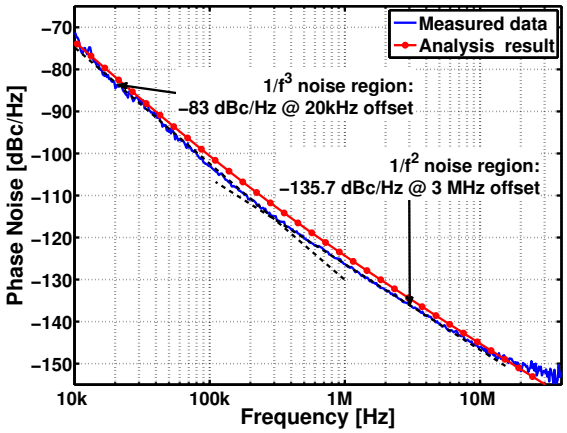


**Fig. 10** Measured test-chip results of the ESDC oscillator with $V_D = 500\,\text{mV}$, $V_G = 300\,\text{mV}$ and comparison with the analysis.

## 5 Design Example

To demonstrate the application of the proposed analysis as a useful design tool, an ESDC oscillator with the following specifications has been designed:

- Center frequency ($f_o$) = 5.5 GHz;
- Power consumption ($P_{dc}$) $\leq$ 4 mW;
- Phase Noise @1 MHz offset $\leq -122$ dBc/Hz;
- Figure-of-Merit (FoM): Highest possible.

The amplitude and phase noise expressions evaluated in the previous sections can be used to determine the average power consumed in an ESDC oscillator and it is given by,

$$P_{dc} = 2V_D\overline{I(t)} \tag{42}$$

where $\overline{I(t)}$ is the average current through each transistor in the ESDC oscillator.

The FoM of an oscillator is a measure of its efficiency to convert the dc power to the carrier power. It is defined as [4],

$$FoM = 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{dc}}{1\,\text{mW}}\right) - L\{\Delta f\} \tag{43}$$

A higher FoM oscillator has a higher efficiency.

For start-up of any oscillator, the loop gain (LG) of the oscillator should be higher than unity. To account for the PVT variations, in practice a $LG > 2$ is selected. The detailed start-up analysis for an ESDC oscillator was derived in [2]. For clarity the final result is shown below:

$$LG(j\omega) = \frac{g_m\omega^3 L_1 L_2 C_1}{B(\omega)} \tag{44}$$

where

$$\begin{aligned} B(\omega) = \quad & -\omega^3 L_1 L_2[G_1C_1 + G_1C_2 + (g_m + G_2)C_1] \\ & +\omega[L_1G_1 + L_2(g_m + G_2)] \end{aligned} \tag{45}$$

$G_1$ and $G_2$ are the equivalent parallel conductances of $L_1$ and $L_2$, respectively at the oscillation frequency, $g_m$ is the transconductance of the transistor at the dc operating point. The design procedure is summarized in Fig. 11 as a flow-chart. $L_1$ can be designed with an electromagnetic solver/optimizer such as ASITIC [23]. As discussed in [2], $L_2$ should be chosen sufficiently higher than $L_1$. In order to verify the design choices of [2], the same values of $L_1$ and $L_2$ are used, i.e., $L_1 = 690$ pH, $L_2 = 1.25$ nH. At the oscillation frequency, $G_1 = \frac{1}{450}$ S and $G_2 = \frac{1}{550}$ S. The total equivalent tank capacitance is 1.21 pF.

Following the method described in Fig. 11, the transistor dimensions were varied from $\frac{40\,\mu\text{m}}{0.24\,\mu\text{m}}$ to $\frac{200\,\mu\text{m}}{0.24\,\mu\text{m}}$ and the feedback factor, $n$, was varied from 0.2 to 0.6. The predicted power, phase noise and FoM plots for different values of $n$ with varying $\frac{W}{L}$ values are shown in the Figs. 12(a), (b) and (c), respectively. It is evident from Fig. 12(a) that for a maximum power consumption of 4 mW, the value of $n$ should be between $0.2 - 0.5$. A suitable point from this graph has to be selected that ensures proper start-up of the oscillator. Any point inside the shaded region has a loop gain $< 1$ and has to be avoided. The phase noise performance for different values of $n$ and $\frac{W}{L}$ are shown in Fig. 12(b). $n = 0.2$ is excluded since it does not give an adequate phase noise performance. Therefore, $n$ should be chosen within the range $0.3 - 0.5$. There are multiple combinations of $\frac{W}{L}$ and $n$ values that satisfy the design requirement. The best design choice would be to use the most efficient oscillator among all possible options. Fig. 12(c) shows that the oscillator has the highest FoM for $n \approx 0.4$ with $\frac{W}{L} \approx 1.6\left(\frac{40\,\mu\text{m}}{0.24\,\mu\text{m}}\right)$. In order to ensure sufficient start-up gain $\frac{W}{L} = 2\left(\frac{40\,\mu\text{m}}{0.24\,\mu\text{m}}\right)$ was chosen. The LG for this transistor size is $\approx 2.5$. The degradation of the FoM with a larger transistor size is nominal as seen from Fig. 12(c). The optimal design values for $C_1$ and $C_2$ are 2.02 pF and 3.03 pF, respectively. These are fairly close to (within 10 %) the design choices of [2]. Therefore, this analytical model can be used to search through the design space much faster than using circuit simulations. For comparison, the MATLAB code of the proposed algorithm was run on a PC with 2.8 GB RAM and an Intel Quad Core 2.5 GHz Processor. The SpectreRF PSS and PNOISE analysis for all 66 data points in Fig. 12 took 66 minutes whereas the MATLAB code produced comparable results in 4.3 minutes. Therefore, the analysis model and its MATLAB based implementation can work as a valuable design assistant for a oscillator designer and it can be used to rapidly find out the optimal design parameters. This design procedure can be further automated by augmenting the existing tool with a numerical optimization loop as in [14, 15].

The proposed design method can be a very effective design tool if it is used along with a space mapping based algorithm [24]. The space mapping algorithm simplifies an optimization procedure by mapping a computationally intensive problem to a simplified problem and running the optimization over the simplified problem. A level-I MOSFET model based analysis can be used for refining the optimization procedure of a more sophisticated and computationally intensive BSIM3V3 model based approach, used in a circuit simulator.

## 6 Conclusion

A generalized analysis technique has been developed for determining the amplitude and phase noise of CMOS low voltage oscillator topologies. An oscillator design approach for optimal oscillator design based on this analysis has been described.

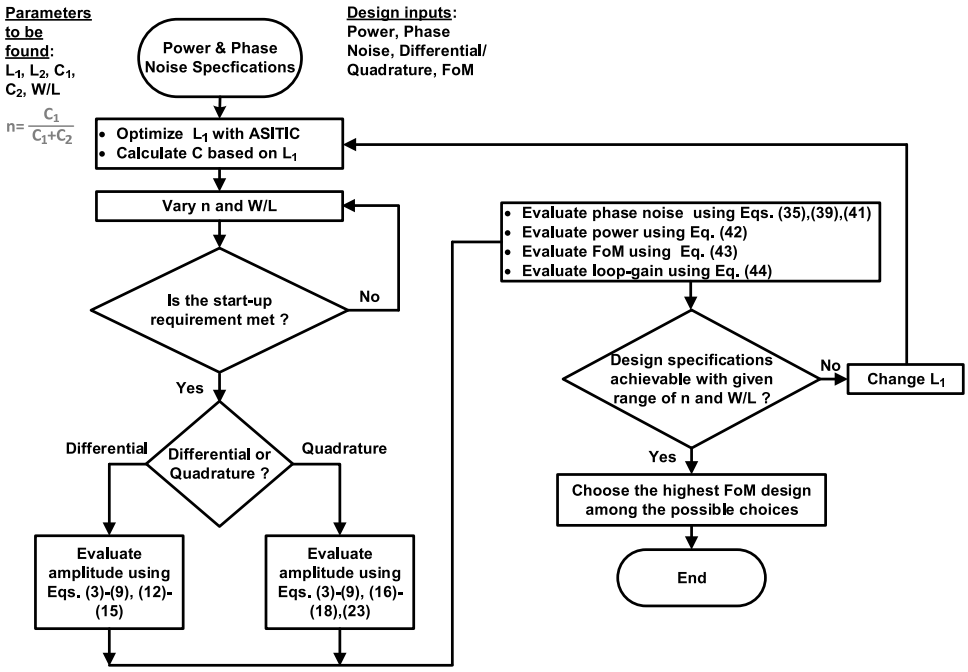


**Fig. 11** Design flow-chart. [1]

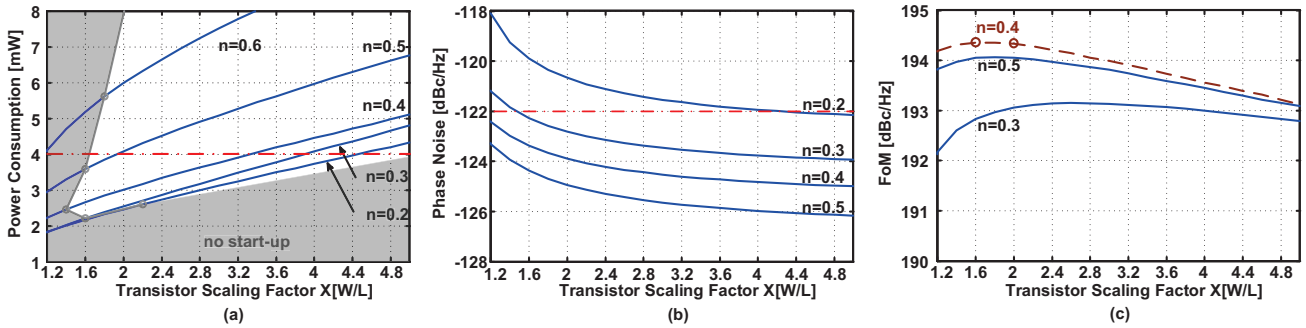


**Fig. 12** Variation of (a) Power, (b) Phase Noise, and (c) FoM with $\frac{W}{L}$ (in multiples of $\frac{40\,\mu\text{m}}{0.24\,\mu\text{m}}$) and $n$.

The analysis forms the basis for a MATLAB based oscillator design tool. This tool allows a designer to properly size the transistors without the need for time consuming simulations.

## References


1. A. Heiberg, T. Brown, T. Fiez, and K. Mayaram, "A 250 mV, 352 w GPS receiver RF front-end in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 938–949, Apr. 2011.
2. T. Brown, F. Farhabakhshian, A. Guha Roy, T. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1782–1795, Aug. 2011.
3. F. Zhao and F. Dai, "A 0.6V quadrature VCO with enhanced swing and optimized capacitive coupling for phase noise reduction," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 8, pp. 1694–1705, Aug. 2012.
4. P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
5. A. Hajimiri and T. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
6. A. Mazzanti and P. Andreani, "Time-variant analysis of fundamental phase noise in CMOS parallel LC tank quadrature oscillators," in *IEEE Trans. Circuits Syst. I*, vol. 56, no. 10, Feb. 2009, pp. 1173–2180.
7. J. Roychowdhury and P. Feldmann, "A new linear-time harmonic balance algorithm for cyclostationary noise analysis in rf circuits," *Proc. ASP-DAC*, pp. 483–492, 1997.
8. A. Suarez, S. Sancho, S. Hoeye, and J. Portilla, "Analytical comparison between time- and frequency-domain techniques for phase-noise analysis," *IEEE Trans. Mi-*


[1] This flowchart has been implemented in MATLAB. Code is available upon request.

*crow. Theory Tech.*, vol. 50, no. 10, pp. 2353–2361, Oct 2002.
9. K. Mayaram, "Output voltage analysis for the MOS colpitts oscillator," *IEEE Trans. Circuits Syst. I*, vol. 47, no. 2, pp. 260–263, Feb. 2000.
10. D. Murphy, J. Rael, and A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.
11. C. Samori, A. Lacaita, F. Villa, and F. Zappa, "Spectrum folding and phase noise in LC tuned oscillators," *IEEE Trans. Circuits Syst. II*, vol. 45, no. 7, pp. 781 –790, Jul. 1998.
12. S. Levantino, C. Samori, A. Bonfanti, S. L. J. Gierkink, A. Lacaita, and V. Boccuzzi, "Frequency dependence on bias current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise upconversion," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1003–1011, Aug 2002.
13. Z. Li, J. Bao, P. Tang, and F. Wang, "Analysis of phase noise spectrum in LC oscillator based on nonlinear method," in *Proc. Int. Conf. Microw. Millimeter Wave Technol. (ICMMT)*, May 2010, pp. 649–652.
14. C. De Ranter, G. Van der Plas, M. Steyaert, G. G. E. Gielen, and W. Sansen, "CYCLONE: automated design and layout of RF LC-oscillators," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 10, pp. 1161–1170, 2002.
15. M. Chu, D. Allstot, J. Huard, and K. Wong, "NSGA-based parasitic-aware optimization of a 5GHz low-noise VCO," in *Asia South Pacific Design Automation Conference*, 2004, pp. 169–174.
16. M. Daliri and M. Maymandi-Nejad, "Analytical model for CMOS cross-coupled LC-tank oscillator," *Circuits, Devices Systems, IET*, vol. 8, no. 1, pp. 1–9, Jan 2014.
17. MATLAB, *version 7.13.0.564 (R2011b)*. Natick, Massachusetts: The MathWorks Inc., 2011.
18. E. Hegazi and A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.
19. F. Pepe, A. Bonfanti, S. Levantino, C. Samori, and A. Lacaita, "Analysis and minimization of flicker noise upconversion in voltage-biased oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 6, pp. 2382–2394, June 2013.
20. F. Pepe, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, and A. Lacaita, "Simulating phase noise induced from cyclostationary noise sources," in *Proc. ISCAS*, May 2013, pp. 2686–2689.
21. A. Demir, "Phase noise and timing jitter in oscillators with colored-noise sources," *IEEE Trans. Circuits Syst. I*, vol. 49, no. 12, pp. 1782–1791, 2002.
22. F. Kaertner, "Determination of the correlation spectrum of oscillators with low noise," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 1, pp. 90–101, Jan 1989.
23. A. Niknejad and R. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, 1998.
24. J. Bandler, Q. Cheng, S. Dakroury, A. Mohamed, M. Bakr, K. Madsen, and J. Sondergaard, "Space mapping: the state of the art," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, pp. 337–361, Jan 2004.