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An efficient technique for excess loop delay compensation in continuous-time ΔΣ modulators

Y. Zhang, C.-H. Chen and G.C. Temes

A highly-digital technique is proposed for excess loop delay (ELD) compensation in multi-bit continuous-time ΔΣ modulators. A digitally controlled reference switching matrix is used to replace the power-hungry signal adder and extra DAC driving the quantizer, which are commonly used in ELD compensation. With the proposed technique, the feedback DAC is embedded in the quantizer and implemented by a few switches. Thus it allows low voltage and low-power operation.

Introduction: Continuous-time (CT) ΔΣ modulators suffer from excess loop delay (ELD) due to the nonzero delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback node in the modulator [1]. Delay compensation methods described in the literature implement an extra fast direct local feedback path around the quantizer or change the filter coefficients with different feedback DAC pulse shapes [1]-[3]. Figure 1 shows the block diagrams and impulse responses of a first-order loop filter with and without ELD compensation. By introducing an extra direct feedback path around the quantizer, the impulse responses of both loop filters can be matched at the sampling instants as shown in Figs.1(a) and (b).Then,

$$X_2(t)\big|_{t=nTs} = W(t)\big|_{t=nTs} - U_2(t)\big|_{t=nTs} = X_1(t)\big|_{t=nTs} \tag{1}$$

This compensation technique makes the allowable quantizer time delay relaxed to half a clock period. Moreover, any signal-dependent quantizer delay is absorbed by the re-timing block in front of DAC_2. However, this ELD compensation technique requires both an added feedback DAC_2 and a power-hungry signal adder at the input of the quantizer.

Proposed Reference Switching Technique: In Fig. 1(b), the output bit-stream D_{OUT} is given by:

$$\begin{aligned} D_{OUT} &= sgn\big[X_2(t) - V_{ref}\big] \\ &= sgn\big\{W(t) - \big[V_{ref} + U_2(t)\big]\big\} \end{aligned} \tag{2}$$

where sgn(·) = 1 when (·) > 0, otherwise sgn(·) = 0. Note that in the term $V_{ref} + U_2(t)$ in (2), V_{ref} denotes the fixed reference levels whereas $U_2(t)$, the output of DAC_2, denotes the reference levels controlled by D_{OUT}. The combination of the two terms is equivalent to generating a group of discrete reference levels modulated by D_{OUT}. In other words, for each sampling clock cycle, the fixed reference levels in the reference string are shifted by an amount which is determined by the output data D_{OUT}. This translates into the proposed technique shown in Fig.2(a). A switching matrix, which is digitally controlled by the binary coded output D_{OUT}, replaces the direct feedback DAC_2 and the signal adder before the quantizer shown in Fig. 1(b). Figure 2(b) shows more details.

In Fig. 2(b), let $V_{FS} \triangleq V_{refp} - V_{refn}$, where V_{FS} is defined as the full-scale range of DAC_2. Thus the differential full-scale range of DAC_2 is$(-V_{FS}, V_{FS})$. The resulting 2-bit feedback DAC_2 levels are thus given by $\left[-V_{FS}, -\frac{V_{FS}}{3}, \frac{V_{FS}}{3}, V_{FS}\right]$. Therefore the possible values of U_2 in (2), which are the amounts of differential reference shift, are given by:

$$\begin{aligned} U_2(D_{OUT}) &= k \cdot \left[-V_{FS}, -\frac{V_{FS}}{3}, \frac{V_{FS}}{3}, V_{FS}\right] \\ &= \left[-\frac{V_{FS}}{2}, -\frac{V_{FS}}{6}, \frac{V_{FS}}{6}, \frac{V_{FS}}{2}\right] \end{aligned} \tag{3}$$

where $k = 0.5$ is the feedback coefficient of the DAC_2 in Fig. 1(b). According to (3), the interval between adjacent levels in the reference string is $\frac{V_{FS}}{12}$ for differential implementation. The fixed V_{ref} values for the 2-bit quantizer are denoted in Fig. 2(b). The control logic of the reference switching matrix is shown in the left side of the Fig. 2(b), in which two thermometer-to-binary blocks and four AND gates are

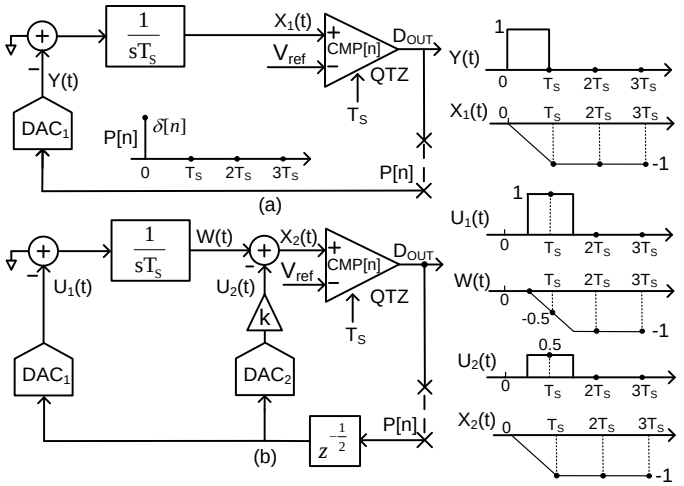
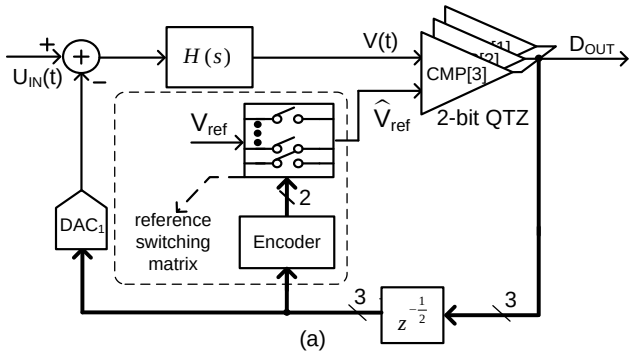


Fig.1 *Impulse response of the first-order loop filter (a) without ELD compensation; (b) with ELD compensation (direct feedback path k=0.5).*



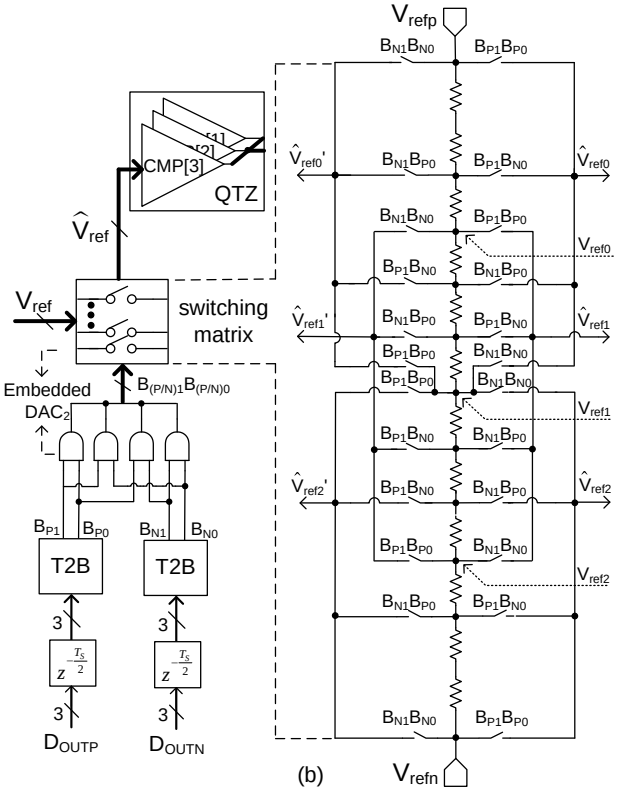


Fig.2 *(a) Proposed ELD compensation technique with reference switching matrix (b) Implementation of reference switching matrix with control logic*

employed. This whole process is equivalent to introducing an implicit feedback DAC_2 in the reference switching matrix.

Simulation results: A 3rd order CT ΔΣ modulator in Fig. 3 was fully designed and simulated on the transistor level to verify the proposed ELD compensation technique. It is a combined feed-forward and feedback topology with a non-return-to-zero (NRZ) FIR feedback DAC. The modulator is clocked at 1.2 GHz and the signal bandwidth is 15 MHz. With the proposed ELD compensation, half a clock period is allocated to the delay of quantizer and dynamic element matching (DEM). Figure 4 shows the SQNR as a function of the sum of the quantizer and DEM delays. It indicates that the maxim tolerable delay is around $\frac{T_S}{2}$. The simulated PSD is shown in Fig. 5 with a -1.9 dBFS input signal of 2.6 MHz. The achieved SQNR is about 88.3 dB.

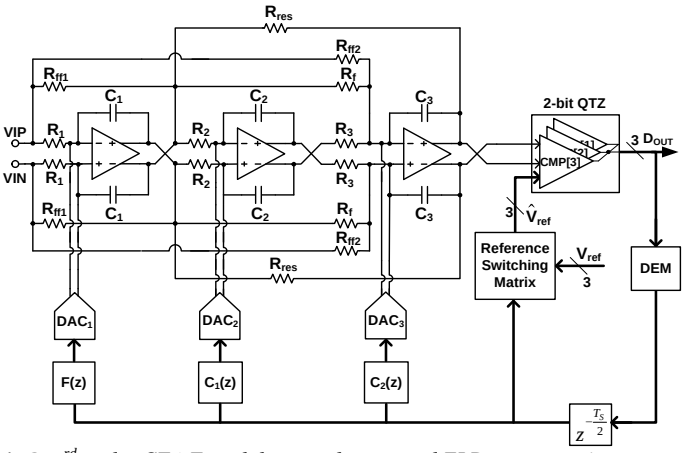


Fig.3. *3rd-order CT ΔΣ modulator with proposed ELD compensation*

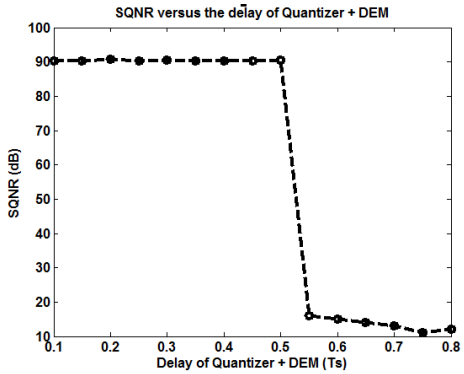


Fig.4. *SQNR versus sum of the quantizer delay and DEM of the CT ΔΣ modulator with the proposed ELD compensation*

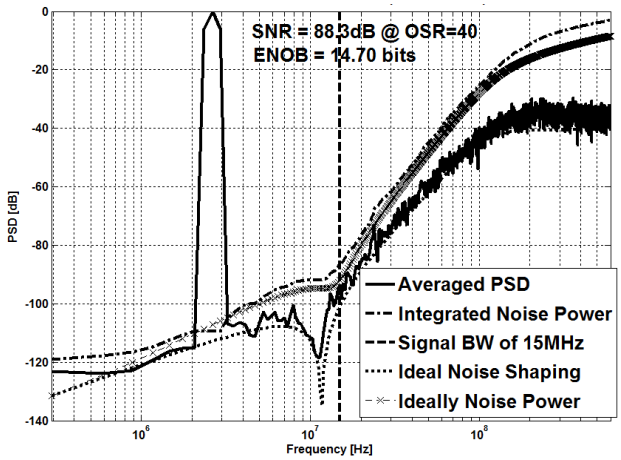


Fig.5. *Simulated PSD of the CT ΔΣ modulator with proposed ELD compensation technique*

Conclusion: An excess loop delay compensation technique is proposed for multi-bit CT ΔΣ modulator. A reference switching matrix, together with simple control logic, is used for the ELD compensation. This technique avoids the use of a power-hungry signal adder and an added feedback DAC as commonly used in the conventional ELD compensation scheme. The proposed technique was verified by the simulated example of a 3rd-order CT ΔΣ modulator.

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Y. Zhang, C. H. Chen and G. C. Temes (*Department of Electrical and Computer Science, Kelley Engineering Centre, Oregon State University, Corvallis, OR 97331-5501, USA*))

E-mail: zhangy7@eecs.oregonstate.edu

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