Noise-Shaping SAR ADC Using Three Capacitors

C.-H. Chen, Y. Zhang, J.L. Ceballos, and G. C. Temes

In this letter, a simple and highly efficient successive-approximation Registers (SAR) ADC realization is proposed. It requires an op-amp, a comparator and only three equal-valued capacitors. The proposed scheme is insensitive to the capacitor parasitics, and has a small capacitance spread. With an oversampled scheme, it also allows noise-shaping the remaining quantization error. It is well-suited for low-frequency instrumentation and measurement applications, and for use in extended-counting ADCs.

Introduction: SAR ADC is a highly power-efficient data converter, because it uses a binary search scheme, and most components are passive. In this letter, a simple and efficient SAR ADC with two equal capacitors DAC, a comparator, and an op-amp is described. As a stand-alone data converter, it has a small capacitance spread, and therefore its input capacitance is small and easy to drive. Furthermore, it is insensitive to parasitic capacitance. For low-frequency applications, the sampling frequency can be much higher than the Nyquist frequency of the signal. Then the proposed SAR ADC can perform noise-shaping, and achieve significantly higher SQNR than a Nyquist-rate SAR ADC.

The Proposed SAR ADC: Fig. 1 illustrates the proposed data converter. Nominally, $C_1 = C_2 = C_F$. Capacitors C_{P1} and C_{P2} are the top-plate parasitic capacitances of C_1 and C_2. The step-by-step operation of the ADC is as follows:

1. *Sampling:* assuming all capacitors are initially discharged, phases φ1, φ4 and φ5 rise to 1, so V_{in} is sampled on C_2, and C_1 is charged to $V_1 = V_{ref}$ (Fig. 2a). Next, φ3 and φ6 rise, and a charge $q_f = -C_2 \cdot V_{in}$ enters C_F. Hence, the output voltage is $V_{op} = V_{in}$ (Fig. 2b).
2. *MSB test:* φ6 stays high, φ3 goes low, and φ2 goes high. Now V_1 becomes $V_{ref}/2$, and a charge $C_2 \cdot V_{ref}/2$ enters C_F. The sign of the new output $V_{op} = V_{in} - V_{ref}/2$ determines the MSB (Fig. 3a). *If MSB = 1,* go directly to Step 4 (Fig. 4a).
3. *If MSB = 0,* the charge $C_2 \cdot V_{ref}/2$ must be removed from C_F . This is achieved by keeping φ6 high, opening φ2 and setting φ3 high (Fig. 3b). V_{op} then returns to V_{in}, and Step 4 follows.
4. *Next MSB test:* φ6 goes low, while φ3 and φ5 go high to discharge C_2. Then, φ2 and φ6 go high, so $V_1 = V_{ref}/4$, and a charge $C_2 \cdot V_{ref}/4$ enters C_F (Fig. 4b). The sign of V_{op} gives the next MSB.
5. The rest of the bits are determined the same way as the two MSBs in Steps 2 - 4.

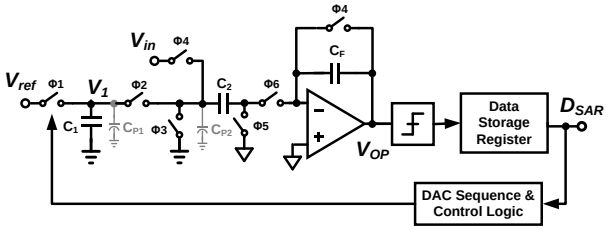

Fig. 1 The analog core circuits of the proposed SAR ADC

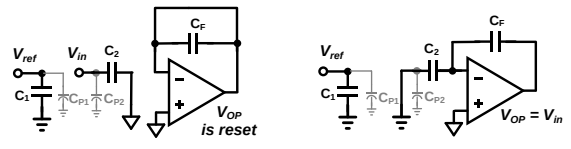

Fig. 2 Step 1: The proposed SAR ADC during sampling phase.

The clock phases must be appropriately delayed to prevent signal-dependent charge injection. Thus, φ4 should cut off after φ5 in Step 1, and φ4 is cut off after φ2 and φ3 in Step 2.

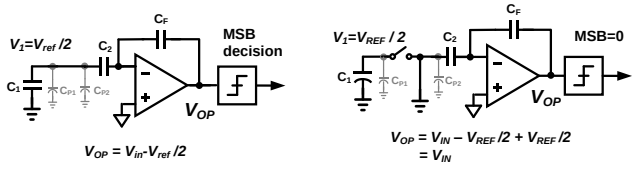

Fig. 3 DAC Operation for MSB decision.

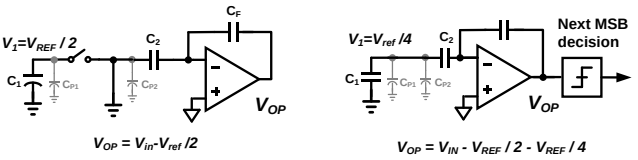

Fig. 4 DAC Operation for MSB=0 and next MSB decision

Comparison with Earlier SAR ADCs: The described SAR ADC is somewhat similar to the proposed one in the pioneering paper by Suarez et al. [1], which was also the first one to propose the two-capacitor DAC. Their ADC contained a serial two-capacitor DAC and a comparator performing the SAR conversion. Thus, they did not need a holding amplifier. However, since their structure did not allow stepping back the DAC output for a zero-valued bit, the serial DAC had to be completely reset for every new bit. Hence, for an *N*-bit conversion, *N(N+1)* steps were required by their ADC. The SAR ADC described here needs only *N* steps, with a large saving in conversion time. Also, the Suarez scheme did not allow noise-shaping the error, and was less suitable for fully-differential implementation than the one proposed here.

Used as a stand-alone ADC, the proposed circuit needs an extra op-amp, but it has several advantages over earlier SAR ADCs. If the parasitic capacitances C_{P1} and C_{P2} are equal, then they do not affect V_1, and hence do not influence the conversion. Also, the charge left in C_F after all bits have been obtained may be saved, and thereby a noise-shaping factor $(1 - z^{-1})$ is introduced into the *z*-transform of the quantization error sequence. As shown on Fig. 5a, in this case V_{op} is not reset when sampling a new data ($V_{in}[n]$). Hence, the last quantization error ($V_{in}[n-1]-V_{DAC}[n-1]$) is stored at the output. This implements the error feedback scheme [2], which performs a first-order noise shaping, as shown on Fig. 5b. The easy implementation of error shaping is an added advantage over most alternative architectures.

The proposed SAR ADC has fewer capacitors than the conventional one, and these have equal values, allowing better matching for C_1 and C_2 (the exact value of C_F is not important.) Specifically, C_1 and C_2 should be large enough for reducing the *kT/C* noise, and are typically around 0.1 pF for 12-bit conversion. For such capacitors, a 0.1 % matching accuracy is easily achieved. Since the two-capacitor DAC accuracy can be estimated from $\Delta V/V_{ref} \sim 0.14.\Delta C/C$ [1], the capacitor mismatch will not limit the ADC resolution. For embedded application in an extended-counting ADC[3] the holding opamp and the comparator are already available, and only the capacitors need to be added.

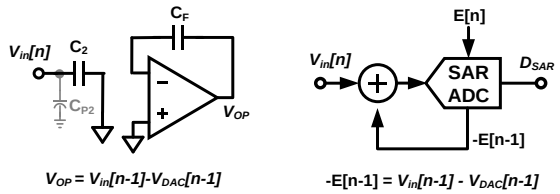

Fig. 5 SAR ADC using noise-shaping.

Simulation Results: The proposed SAR ADC was designed for a 10-bit resolution, and 40 Hz signal bandwidth. It was simulated by Simulink, assuming a 1% RMS capacitance mismatch. The resulting power spectral density (PSD) is shown on Fig. 6. With a -3 dBFS input signal, the simulated SNDR was 57.3 dB. For each data conversion, two clock periods were assigned for the sampling, and 10 clock periods for the bit cycling. Fig. 7 shows the SNDR versus the capacitor mismatch up to 1% with a -3dBFS input signal. The results show that the proposed

ADC is insensitive to capacitance error, as well as the parasitic capacitances.

When the10-bit 2-C SAR ADC was oversampled by a factor OSR = 32, the simulated PSD shown in Fig. 8 resulted. The SNDR within the 40Hz bandwidth was now 97dB with a -3dBFS input signal. About 15 dB of the increment was contributed by the oversampling, and about 20 dB by the noise-shaping. The sampling frequency was 2.56 kHz (32 times the Nyquist rate of 80 Hz), and the internal frequency 12 times the sampling frequency, 30.72 kHz.

In ultra-deep-submicron CMOS technologies, the operation of SAR ADCs at sampling rates of a few kS/s may be degraded by leakage current during comparison [4] if no additional circuitry is present to prevent the leakage. With the oversampled scheme, the sampling rate can be chosen higher, so that the leakage current degradation is reduced. As illustrated, noise-shaping will also raise the accuracy of the conversion significantly.

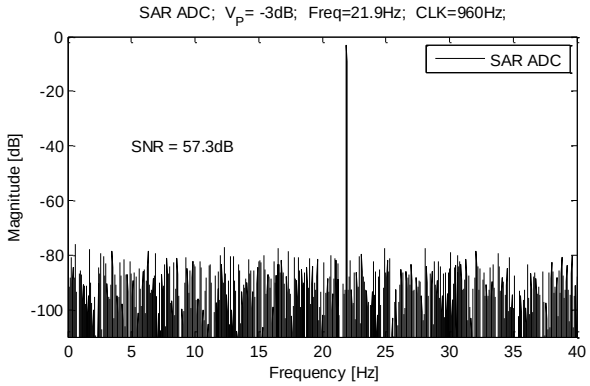

Fig. 6 Simulation of the proposed SAR ADC with 1% mismatch.

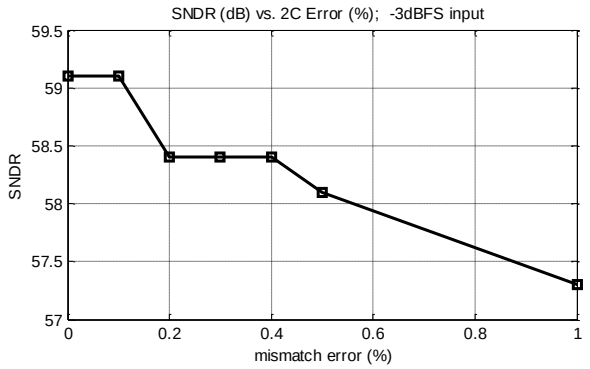

Fig. 7 SNDR (dB) vs. 2-C capacitor mismatch (%)

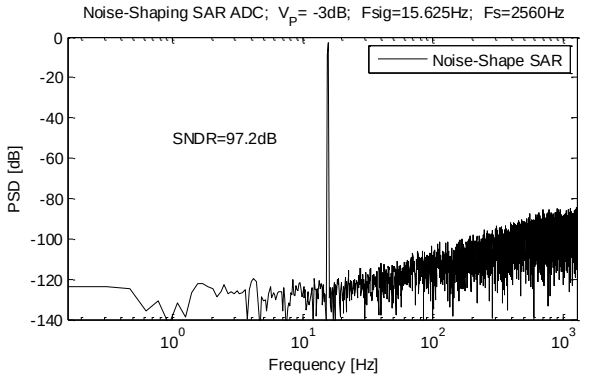

FIg. 8 The simulated PSD of the proposed noise-shaping SAR

Conclusion: An efficient SAR ADC was proposed. It needs only three equal-valued capacitors. The capacitance spread is small, and hence the input capacitance is low, and easy to drive. An oversampled scheme can be applied to the proposed ADC to achieve a higher SQNR. The performance of the proposed noise-shaped ADC will be less degraded by leakage current for low-frequency operation in ultra-deep-submicron CMOS technologies than for existing converters.

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References

1 R.E. Suarez, and et al.,"All-MOS charge re-distribution analog-to-digital conversion techniques-Part II," IEEE JSSC, Dec.1985.

2 R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters: IEEE Press, 2005, p. 81.

3 A. Agah, and et al., "A high-resolution low-power incremental ADC with extended range for bio-sensor arrays," IEEE JSSC, Jun. 2010.

4 D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13-um CMOS for medical implant devices," in *Proc. ESSCIRC*, Sep. 2011, pp. 467–470.