ZnO-based transparent thin-film transistors

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Highly transparent ZnO-based thin-film transistors (TFTs) are fabricated with optical transmission (including substrate) of ~75% in the visible portion of the electromagnetic spectrum. Current–voltage measurements indicate *n*-channel, enhancement-mode TFT operation with excellent drain current saturation and a drain current on-to-off ratio of $\sim 10^7$. Threshold voltages and channel mobilities of devices fabricated to date range from ~10 to 20 V and ~0.3 to 2.5 $cm^2/V\,s$, respectively. Exposure to ambient light has little to no observable effect on the drain current. In contrast, exposure to intense ultraviolet radiation results in persistent photoconductivity, associated with the creation of electron-hole pairs by ultraviolet photons with energies greater than the ZnO band gap. Light sensitivity is reduced by decreasing the ZnO channel layer thickness. One attractive application for transparent TFTs involves their use as select-transistors in each pixel of an active-matrix liquid-crystal display. © *2003 American Institute of Physics.*
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Transparent electronics is a nascent technology involving the realization of invisible electronic circuits.[1] The ''birth'' of transparent electronics appears to coincide with the announcement of a *p*-type transparent electrical conductor, $CuAlO_2$.[1,2] The availability of such a *p*-type material, in conjunction with conventional *n*-type transparent conductors such as ZnO, SnO_2, and In_2O_3:Sn, makes feasible the construction of a *pn* junction, the most fundamental electronic device. Recently, transparent *pn* heterojunction diodes,[3] *pn* homojunction diodes,[4] and *pn* heterojunction-based UV-light-emitting diodes[5] have been realized. The latter achievement heralds the beginning of transparent optoelectronics. Furthermore, reports of transparent ferromagnetic materials with Curie temperatures above room temperature[6,7] open the door to the possibility of transparent spintronics. Clearly, there are manifest marriage possibilities between these and perhaps other transparent as well as nontransparent technologies.

What applications will emerge for transparent electronics, optoelectronics, or spintronics? The honest answer to this question is: it is too early to tell. More precisely, the viability of most transparent applications will be dictated by the quality of the materials employed and the performance of associated devices. Thus, many material, device, circuit, system, and manufacturing issues need to be identified, explored, and elucidated before a realistic assessment of these transparent technologies is possible.

Given this as a backdrop, the purpose of the work reported herein is to describe an *n*-channel, enhancement-mode thin-film transistor (TFT) that is highly transparent in the visible portion of the electromagnetic spectrum, has very little light sensitivity, and exhibits electrical characteristics that appear suitable for implementation as a transparent select-transistor in each pixel of an active-matrix liquid-crystal display (AMLCD). Moreover, the processing technology used to fabricate this device is relatively simple and appears to be compatible with inexpensive glass substrate technology.

The realization of a transistor is a significant development in the context of transparent electronics since the control electrode of such a device facilitates the achievement of logic, amplification, memory, and other types of signal conditioning and processing functions which, within the context of microelectronics, play an important role in our modern information society.

Several TFTs of relevance to the work reported herein have been reported recently.[8–10] Prins *et al.* fabricated an *n*-channel, depletion-mode ''transparent'' ferroelectric TFT in which SnO_2:Sb serves as the channel layer, as well as the source and drain, nontransparent $SrRuO_3$ acts as the gate, and $PbZr_{0.2}Ti_{0.8}O_3$ is employed as the gate insulator. A $SrTiO_3$ substrate is used, presumably to allow for enhanced channel layer crystallinity and/or high-temperature annealing; processing temperatures are not specified. Qualitatively, the transparency of the nongate portion of this device is clearly evident from a picture included in Ref. 8; however, no quantitative information about the transparency of this device is provided. An important aspect of this work is the use of a ferroelectric gate insulator, which demonstrates the possibility of realizing transparent TFTs with inherent memory. Kobayashi *et al.* describe a nanocrystalline GaN TFT fabricated on an opaque silicon substrate using opaque aluminum source and drain contacts and processed at a maximum temperature of 900 °C. Similarly, on an opaque silicon substrate with opaque gold source and drain contacts and using a maximum processing temperature of 900 °C, Ohya *et al.* provide evidence of *n*-channel, enhancement-mode TFT behavior using a ZnO channel layer and an oxidized

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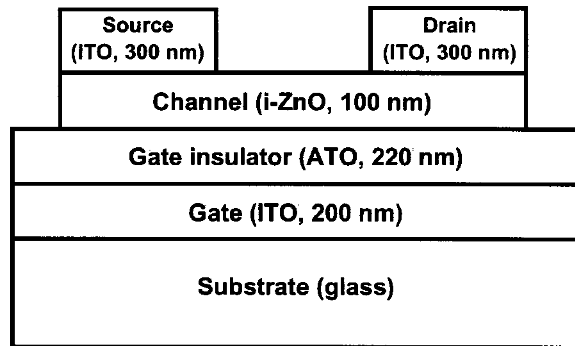

FIG. 1. The typical TTFT structure.

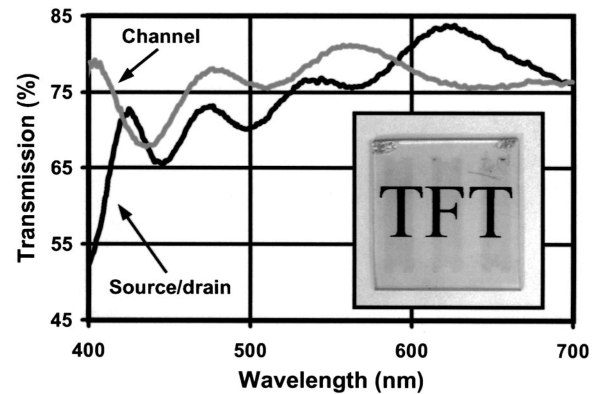

FIG. 2. Optical transmission spectra for the entire TTFT structure (including substrate) through the source/drain region and the channel region of a TTFT. The ITO (source/drain), ZnO (channel), ATO (gate insulator), and ITO (gate) thicknesses are 300, 100, 220, and 200 nm, respectively. The inset shows a one inch substrate with three vertically oriented TTFTs.

SiO_2 gate insulator. An interesting aspect of this TFT is that the ZnO is prepared via chemical solution deposition with subsequent annealing. The electrical performance of this device is not known since drain current–drain voltage and other conventional device characteristics are not specified in Ref. 10.

Figure 1 shows a typical transparent thin-film transistor (TTFT) device structure. A glass substrate is blanket coated with a 200-nm-thick layer of sputtered indium tin oxide (ITO) and a 220 nm thick layer of aluminum–titanium oxide (ATO) deposited by atomic layer deposition. ITO is a highly transparent, n-type conductor which serves as the TTFT gate. ATO is an engineered insulator consisting of a superlattice of alternating layers of Al_2O_3 and TiO_2 which is capped on either end by an Al_2O_3 layer.[11] The ATO layer acts as the gate insulator. The ZnO channel and ITO source/drain electrode films are deposited via ion beam sputtering in 10^{-4} Torr of Ar/O_2 (80%/20%); the substrate is unheated during deposition. Shadow masks are used to pattern the ZnO channel and ITO source/drain electrodes. The channel width and length are 15 000 and 1500 μm, respectively, yielding a width-to-length ratio of 10:1; the source/drain contact dimensions are 15 000 μm$\times$1500 μm. After deposition of the ZnO layer, a rapid thermal anneal (RTA) (typically at 600–800 °C in O_2) is employed to increase the ZnO channel resistivity, to improve the electrical quality of the ATO/ZnO interface, and to enhance the crystallinity of the ZnO layer. Following deposition of the ITO source/drain electrodes, a 300 °C RTA in O_2 is performed to improve the transparency of the ITO layer.

Figure 2 shows the optical transmission spectra through the source/drain region and the channel region of the TTFT, these spectra portray the raw transmission through the entire structure (including the glass substrate), and are uncorrected for thin film interference. The figure inset shows a one inch substrate with three vertically oriented TTFTs, through which the underlying text is clearly visible. The ZnO and ITO thicknesses for this device are 100 and 300 nm, respectively. The average optical transmission in the visible portion of the electromagnetic spectrum is ~ 75%. Note that simple glass reflection losses result in ~92% transmission of the light incident upon an uncoated glass substrate. Thus, the reduction in transmitted light intensity due to the TTFT thin film layers (as compared to that expected for an uncoated glass substrate) is ~17%.

Figure 3 displays dc drain current–drain voltage (I_D-V_{DS}) curves for a TTFT. Several aspects of these characteristics merit mention. First, this TTFT operates as an n-channel enhancement mode device, as evident from the fact that a positive gate voltage is required to induce a conducting channel, and that the channel conductivity increases with increasing positive gate bias. Enhancement mode is preferable to depletion mode behavior, in which application of a gate voltage is required to turn the transistor off, since circuit design is easier and power dissipation is minimized when normally-off, enhancement-mode transistors are employed. Second, this device exhibits "hard" saturation, as witnessed by the fact that the slope of each I_D curve is flat for large V_{DS}. Hard saturation indicates that the entire thickness of the ZnO channel can be depleted of free electrons. Hard saturation is highly desirable for most circuit applications, since transistors exhibiting this property possess a large output impedance. An annealing temperature of at least ~700 °C is required to insure that TTFTs exhibit hard saturation. Third, I_D is in the microamp range, whereas currents in the milliamp range are desirable for many circuit applications. One way to increase I_D is to simply increase the TTFT width-to-length ratio, since I_D scales directly with this ratio. We have found that changing the width-to-length ratio from 2:1 to 10:1 increases I_D by a factor of ~5, as expected from simple scaling. Fourth, the range of V_{GS} and V_{DS} used to bias the TTFT shown in Fig. 3 is large compared to that typical of silicon transistors. The magnitudes of these operating volt-

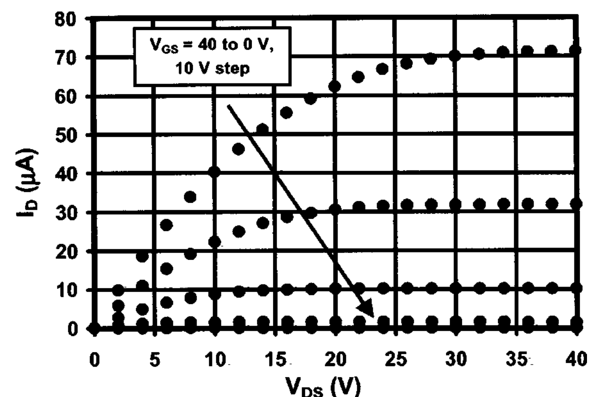

FIG. 3. Drain current–drain voltage (I_D-V_{DS}) characteristics for a TTFT with a width-to-length ratio of 10:1.

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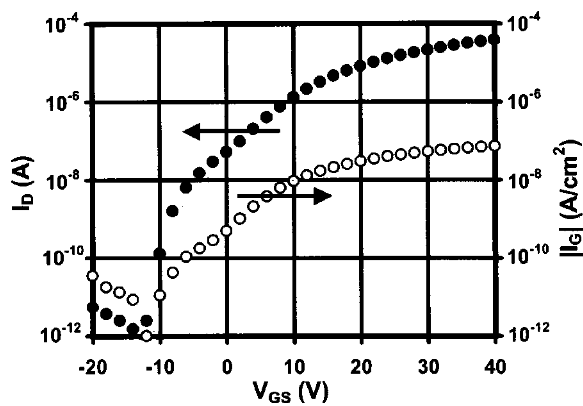

FIG. 4. Transfer characteristics and gate leakage current for a TTFT with a width-to-length ratio of 10:1 for $V_{DS}=10$ V.

ages, as well as that of the threshold voltage, are directly proportional to the gate insulator thickness; thus, it is clear that these operating voltages can easily be reduced by a factor of ~5–10 with a corresponding reduction in the gate insulator thickness.

Further assessment of TTFT dc current–voltage characteristics allows estimation of the effective channel mobility and threshold voltage. For the TTFT with drain current characteristics portrayed in Figs. 3 and 4 the effective channel mobility and threshold voltage are found to be 0.35–0.45 cm^2/V s and 10–15 V, respectively. For all of the ZnO-based TTFTs manufactured to date, the effective channel mobilities and threshold voltages are found to range from ~0.3 to 2.5 cm^2/V s and ~10 to 20 V, respectively. The effective channel mobility increases with annealing temperature. Although TTFT mobilities are low with respect to those obtained using conventional semiconductor materials, e.g., single crystal Si, they are comparable to or better than those obtained in amorphous Si and organic transistors.

Typical TTFT dc transfer characteristics $[\log(I_D)-V_{GS}]$ and gate leakage current $[\log(|I_G|)-V_{GS}]$, involving the drain current, I_D, gate current, I_G, and the gate voltage, V_{GS}, are portrayed in Fig. 4. These curves indicate a maximum drain current on-to-off ratio of $\sim 10^7$. This is an important figure-of-merit for AMLCD applications; a ratio of greater than $\sim 10^6$ is typically required. The gate leakage current magnitude is quite respectable and can be significantly reduced by decreasing the gate area; note that the gate leakage current scales directly with gate area, while the drain current is established by the transistor width-to-length ratio, not by absolute device dimensions.

All of the electrical characterization results presented herein are obtained at dc since the large parasitic capacitance of our TTFT test structure precludes meaningful ac assessment. Work has been initiated to fabricate TTFTs with reduced dimensions. Preliminary characterization of these TTFTs confirms their operation under low-frequency ac voltage excitation, as expected.

Although the light sensitivity of these TTFTs has not yet been studied in detail, several general trends are apparent. Exposure to typical ambient light intensity has little to no effect on current–voltage characteristics. Additionally, TTFT light sensitivity decreases with decreasing ZnO channel layer thickness. For example, a TTFT fabricated with a channel thickness of ~15–20 nm exhibits an increase in drain current due to ambient light exposure of ~1% for $V_{DS}=V_{GS}=40$ V, compared to ~5% for a TTFT with a 100 nm ZnO channel layer. Remarkably, the current–voltage characteristics of the device with reduced channel thickness are virtually identical to those shown in Fig. 3, underscoring the fact that these TTFTs are surface channel devices whose operation depends upon the formation of an electron channel at the channel/gate insulator (ZnO/ATO) interface. The electrical characteristics of such a device are not expected to depend strongly upon the thickness of the ZnO layer, as long as the ZnO layer thickness is significantly greater than the thickness of the induced electron channel, which is likely to be ~1–2 nm.[12]

When subjected to intense UV irradiation, TTFTs exhibit persistent photoconductivity (PPC) to varying degrees, depending upon the fabrication process employed. This effect is likely related to anomalous PPC found in ZnO thin films and ascribed to surface oxygen adsorption.[13,14] Further investigation is required to clarify the mechanism responsible for this behavior and to evaluate whether TTFT PPC or related phenomena have potential for use in commercial applications.

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