AN ABSTRACT OF THE DISSERTATION OF

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Title: Ultra-energy-efficient Silicon Photonic Modulators Driven by Transparent Conductive Oxides

Abstract approved:

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Silicon photonics has become the most promising platform for future large-scale optical interconnect and optical computing systems due to its inherent CMOS compatibility, which brings exclusive advantages in bandwidth density, energy efficiency, and cost effectiveness. Parallel optical interconnects based on photonic integrated circuits (PICs) have the capacity to meet the high bandwidth density requirement of parallel computing systems, however, are facing the same challenge in energy efficiency and bandwidth limit as their electrical counterparts because the margin shrinks unfavorably for shorter distance optical interconnects. Unprecedented requirement in energy efficiency has been outlined, which poses tremendous challenges to existing PIC devices, even to the state-of-the-arts silicon photonics.

In recent years, transparent conductive oxides (TCOs) have emerged as increasingly favorable tunable materials for active photonic devices. TCOs exhibit a large refractive index tunability on the order of unity, which enables unique epsilon-near-zero (ENZ) light confinement and significant enhancement in light-matter interaction. These intriguing optical properties offer us the potential to expand the functionality and improve the device performance of the silicon photonics platform. This dissertation

presents design and demonstration of novel active photonic devices driven by TCOs on silicon photonics platform, with a focus on achieving ultra-energy-efficient silicon photonic modulator.

Three types of photonic devices are investigated. Firstly, an electrically tunable plasmonic subwavelength grating based on a metallic subwavelength slit array coupled with a Si/SiO_2/ITO MOS capacitor is designed and demonstrated. We show that large modulation depth can be achieved for both transmission and reflection modes through modifying the electron concentration within 0.5 nm thick TCO accumulation layer. In the second part, we develop a novel device platform of TCO-gated silicon micro-resonators. A Si-TCO photonic crystal (PC) nanocavity modulator is designed and demonstrated. We achieve extreme large wavelength tuning of 250 pm/V, single digit femto-joule per bit energy efficiency, and 2.2 GHz operation bandwidth with a deep sub-λ ultra-small modulation volume. We also propose a strategy to improve bandwidth to over 23GHz and reduce energy consumption to atto-joule per bit level. Besides, TCO-gated microring resonators are investigated for two applications. We design and demonstrate a tunable microring filter with an unprecedented wavelength tuning of 271 pm/V, a large electrical tuning range of 2 nm, and a negligible static energy consumption, which can be used for wavelength division multiplex (WDM) application. A TCO-gated microring modulator is also designed, which can potentially achieve a large operation bandwidth over 50GHz. Lastly, a sub-micron, sub-pico-second, femto-joule level all-optical switch (AOS) using hybrid plasmonic-silicon waveguides driven by high mobility TCOs is proposed. By defining a comprehensive metric using the product of device size, switching energy and switching time, the proposed device shows superior performance than any existing on-chip AOS device.

In addition to the device research, we systematically analyze the energy efficiency and bandwidth limit of resonator-based silicon photonic modulators from three fundamental perspectives: free carrier dispersion strength of the active materials, Purcell factors of the resonators, and electrical configuration of the capacitors. The analysis lays the theoretical foundation and identifies possible routes for achieving atto-

joule per bit energy efficiency and approaching the bandwidth limit of silicon photonic modulators.

In summary, TCOs could play an important role in the development of future photonics technology, which provide a CMOS compatible solution to overcome the intrinsic weak E-O effect of the silicon photonics platform, lead to unprecedented reduction in energy consumption, increasing bandwidth, as well as enable novel functionalities. Future researches should include, but not limited to, optimizing the design and fabrication of TCO-driven modulators to reduce series resistance and increasing overlapping factor, integrating TCO-driven devices with photonics foundry fabricated PICs, and developing of high mobility TCOs.

Ultra-energy-efficient Silicon Photonic Modulators Driven by Transparent Conductive Oxides

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Erwen Li, Author

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TABLE OF CONTENTS

Page

TABLE OF CONTENTS (Continued)

Page

TABLE OF CONTENTS (Continued)

Page

LIST OF FIGURES

LIST OF FIGURES (Continued)

Figure Page

LIST OF FIGURES (Continued)

Figure Page

LIST OF TABLES

Table Page

Chapter 1. Introduction

1.1 Motivation for ultra-energy-efficient optical interconnects

As clock frequency scaling ended in the mid-2000s, the microelectronics industry has progressively embraced parallel computing architecture to sustain performance improvement. Parallel architectures are now pervasive across most high-performance electronic devices. For example, a NVIDIA Tesla V100 includes up to 100 central process units (CPUs) with 5120 cores in a single graphic process unit (GPU), which can achieve 125 teraflops computation but requires GPU-to-memory bandwidth close to 10 terabits per second (Tbps) [1]. The benefits of parallel computing systems, however, are currently constrained not by the limits of computation at individual nodes, but by the interconnect bottleneck, namely, how to move data between nodes with high energy efficiency. Although photonics technologies have been widely agreed as the most essential solution to resolve the interconnect bottleneck, existing optical input/output (I/O) that has taken the form of pluggable modules on circuit boards cannot completely resolve the challenge due to their high power dissipation and low areal bandwidth density limit. Photonic integrated circuits (PICs) with high density parallel data links have the capacity to meet the high bandwidth density requirement of parallel computing systems. Nevertheless, PIC-based optical interconnects are also facing the same challenge in energy efficiency and bandwidth limit as electrical interconnects because the margin shrinks unfavorably for shorter distance optical interconnects. D. Miller pointed out that the key question is whether optics can reduce energy to atto-joule per bit level in interconnects inside cabinets, racks, and circuit boards, down at least to the edges of the chips themselves, and possibly even on the chip [2]. This unprecedented requirement in energy efficiency poses tremendous challenges to existing PIC devices, even to the state-of-the-arts silicon photonics.

1.2 Overview of silicon photonics

The development of silicon photonics in the past two decades offers the most feasible platform to fulfill parallel optical interconnects due to its inherent CMOS compatibility.

As III-V compound semiconductor light sources can be off-chip coupled or heterogeneously integrated [3]–[6], and Si/Ge photodetectors can potentially be directly powered by the signal light [7], electro-optic (E-O) modulators becomes one of the most critical active devices that will consume the biggest portion of the on-chip power in the optics module, especially for high-speed high-density parallel optical links.

Conventional silicon E-O modulators are based on Mach-Zehnder interferometer (MZI). The basic structure consists of an input waveguide that splits into two waveguide arms and combine again after certain distance. Through modulating the refractive index of one waveguide arm, a modulated phase difference is introduced between the light propagating along two waveguide arms. Then, when the light combines, it forms constructive/destructive interference depending on the phase different, modulating the output amplitude. Because of the simple operation principle, MZI-based E-O modulators can support a broad operation bandwidth. The prime design metric of a is $V_{\pi}L$, which means the length required to achieve π phase shift for 1V applied voltage.

From the refractive index modulation method perspective, two mechanisms are most widely used for silicon photonics: thermal-optic effect and plasma dispersion. Silicon has a thermal-optical coefficient of $\sim 1.8\times10^{-4}$ K^{-1} at 1.55 μm wavelength. Through integrating heater along the silicon waveguide, we can modulate the refractive index of silicon waveguide by changing the local temperature. However, thermal tuning method has drawbacks of high energy consumption and slow response speed, which are not suitable for high speed modulator. While due to its large refractive index tuning range and pure real part of refractive index modulation, thermal tuning is widely used for low-speed and less-power-hungry applications, such as beam steering [8] and optical switches [9]. On the other hand, plasma dispersion is a carrier density dependent optical effect, which can be described by the Drude model. Through modifying the free carrier density inside a silicon waveguide, we can modulate its refractive index. Since silicon does not have the Pockel effect due to its intrinsic symmetric crystalline structure, plasma dispersion is the only E-O effect in silicon that can be used for an E-O modulator.

There are three electrical structures for silicon E-O modulators: forward biased p-i-n diode using carrier injection, reverse biased p-n junction based on carrier depletion, and metal-oxide-semiconductor (MOS) capacitor based on carrier accumulation. Among these electrical structures, p-i-n diode can induce large index changing through heavy carrier injection. However, it is not suitable for future optical interconnects due to two major drawbacks: long minority-carrier-lifetime-limited operation speed (only a few GHz) and large static energy consumption under forward bias. For the latter two structures, a detailed comparison can be found in section 7.3.4. To date, the mainstream electrical structure is the p-n junction. MZI silicon E-O modulators driven by p-n junctions have been extensively researched. A bandwidth of 30 GHz and a date rate over 50 Gbps can be achieved [10]–[14]. Such device has been commercialized for today's 100G optical transceiver [15]. However, in silicon, plasma dispersion is a relative weak effect, which only induces moderate refractive index perturbation. The change of refractive index at 1.55 μm is usually given by [16]

$$\Delta n = -8.8 \times 10^{-22} N_n - 8.5 \times 10^{-18} \left(N_p\right)^{0.8}. \qquad (1.1)$$

Here, N_n and N_p are the electron and hole density, respectively. For example, for a typical depletion-based silicon photonic modulator with a moderate doping level of 2.5×10^{18} cm^{-3} in its active region, when it is completely depleted, the refractive index only changes by 0.06%. For this reason, silicon MZI E-O modulators have the drawbacks of large footprint usually in hundreds of microns in length and the relatively large energy consumption above pico-joule per bit, which are not suitable for future on-chip optical interconnects.

In the past few years, silicon E-O modulators based on micro-resonators have attracted escalating attention. In a resonator-based E-O modulators, the phase shift from perturbation of refractive index is transferred to the shift of resonance peak wavelength, achieving amplitude modulation. Due to the enhancement of the light-matter interaction inside a high-quality factor (Q-factor) micro-resonator, such as micro-ring [6], [7], [25]–[28], [17]–[24], micro-disk [29]–[32] or photonic crystal (PC) nanocavity

[33]–[37], a resonator-based E-O modulator has the advantages of compact device footprint in tens of microns and low switching energy consumption in a few tens of femto-joule per bit. A high operation speed over 25Gbps can be achieved [7], [17], [25], [30]. Recently, over 100Gbps PAM-4 modulation has been demonstrated with microring modulator [38], [39]. In addition, micro-resonators can work as multiplexers/de-multiplexers as well allowing high density optical network-on-chip system [25], [26], [40]. In 2015, C. Sun et al. demonstrated the first micro-processor that communicates with on-chip photonic interconnect link using micro-ring modulators for the E-O modulation [41]. Recently, a 400G optical I/O chiplet based on microring modulator is reported [42]. Overall, resonator-based silicon E-O modulators have been widely accepted as one of the most promising candidates for future on-chip optical interconnects. However, they also suffer from the speed limit due to the long photon lifetime of high Q-factor resonator. Besides, excessive Q-factor also requires heaters with precise feedback circuits to lock the operational wavelength, which consumes additional energy.

Basically, the performances of silicon E-O modulators are limited by the weak plasma dispersion of silicon. To overcome this intrinsic limitation, people are seeking to take advantage of the E-O effects from heterogeneously integrated materials such as germanium [43]–[47], III-V compound semiconductors [41], [48]–[51], plasmonics [52]–[59], $LiNbO_3$ [60]–[63], E-O polymers [64]–[68], ferroelectric materials [69]–[72], transparent conductive oxides (TCOs) [33], [34], [73]–[75], graphene and 2-D materials [76]–[82], and most recently phase change materials [83]–[88]. These emerging materials offer very unique, and often very large E-O effects. The energy efficiency and scaling laws of broad type modulators have been reviewed by a few excellent papers recently [2], [89]–[93].

1.3 Organization of the dissertation

In this dissertation, we present design and demonstration novel active photonic devices driven by TCOs on silicon photonics platform, with a focus on achieving ultra-energy-

efficient silicon photonic modulator. The dissertation is organized as the following sequence.

In Chapter 2, we introduce TCO material and review the development of E-O devices driven by TCOs. In Chapter 3, we present the design and demonstration of an electrically tunable plasmonic subwavelength grating driven by ITO for light modulation in both transmission and reflection modes. In Chapter 4, we report the development of an ultra-compact Si-TCO photonic crystal nanocavity modulator, which can potentially achieve an ultra-low-energy-consumption of atto-joule per bit and a high-speed operation over 23 GHz. In Chapter 5, we investigate TCO-gated microring resonators for two applications: tunable filter with a negligible static energy consumption for wavelength division multiplex (WDM) application and high-speed modulator. In Chapter 6, we propose and model the performance of a sub-micron, sub-pico-second, femto-joule level all-optical switch (AOS) using hybrid plasmonic-silicon waveguides driven by high mobility TCOs. In Chapter 7, we present systematically analysis on the energy efficiency and bandwidth limit of resonator-based silicon photonic modulators from three fundamental perspectives: free carrier dispersion strength of the active materials, Purcell factors of the resonators, and electrical configuration of the capacitors. Finally, in Chapter 8, we summarize this dissertation and outline future research directions.

Chapter 2. Transparent Conductive Oxides (TCOs) for Electro-optical (E-O) Modulators

2.1 Introduction of TCOs

Transparent conductive oxides (TCOs), such as indium-tin oxide (ITO) and aluminum-zinc oxide (AZO), are a family of wide bandgap semiconductor oxide materials that can be degenerately doped to a high level. Because TCOs combine the optical transparency with good electrical conductivity, they have been widely used for varieties of applications in both research and industry, such as flat panel displays [94] and photovoltaics [95]. The manufacturing technology of TCO thin film is mature, CMOS

compatible and has been extensively investigated [96]. TCO thin films can deposited with varieties of physical vapor deposition methods, such as electron beam evaporation, direct current (DC) sputtering, radio frequency (RF) magnetron sputtering, pulsed laser deposition (PLD), etc. The optical response of TCOs is governed by the free carriers. The free carrier concentrations can be adjusted across a wide range through controlling the doping, fabrication process [97] and electrical gating [75], [98]. Correspondingly, the optical properties can be changed dramatically from dielectric-like to metallic-like, offering unique advantages to engineering TCO for different photonic applications at different wavelength range.

In this work, we focus on the photonics application of TCOs in the near-infrared (NIR) wavelength range. The optical properties of TCOs, similar to many other semiconductor materials, can be described by the well-established Drude model. The relative permittivity, $\varepsilon_r = \varepsilon_1 + i\varepsilon_2$, is given by

$$\varepsilon_r = \varepsilon_\infty - \frac{\omega_p^2}{\omega(\omega+i\Gamma)}, \tag{2.1}$$

where ε_∞ is the high frequency dielectric constant, ω_p is the plasma frequency, and Γ is the plasma collision frequency. Generally, the plasma frequency term ω_p^2 is proportional to the free carrier density N_c by

$$\omega_p^2 = \frac{N_c q^2}{\varepsilon_0 m^*}, \tag{2.2}$$

Here N_c is the free carrier concentration, q is the electron charge, ε_0 is the vacuum permittivity, and m^* is the effective mass of the carrier. The plasma collision frequency Γ and mean free time between ion collisions τ are related with the carrier mobility μ by

$$\Gamma = \frac{1}{\tau} = \frac{q}{\mu m^*}. \tag{2.3}$$

The complex refractive index can be calculated from the permittivity, $(n + i\kappa)^2 = \varepsilon_r$. Fig 2.1 plots the comparison of refractive index and permittivity between p-type silicon and ITO as a function of carrier density. With free carrier concentrations ranging from 1×10^{19} cm^{-3} to 1×10^{21} cm^{-3}, the real part n of the ITO refractive index could experience more than 1 refractive index unit (RIU) change, as shown in Fig 2.1a. In the meanwhile, the imaginary part κ increases to the same order of magnitude as the real part, which causes dramatic increase of the absorption 30-140x larger than that of silicon, as shown in Fig 2.1b. In recent years, a unique property called epsilon-near-zero (ENZ) is verified with TCO materials [99]. At very high free carrier concentration, the real permittivity of TCOs reaches zero while the absolute permittivity is a minimum value due to the small value of the imaginary part as indicated by the vertical dotted lines in Fig 2.1c and 2.1d. For silicon, although the absolute tuning range of permittivity is comparable to that of ITO, however, it is still far from ENZ even at 10^{21} cm^{-3} free carrier concentration due to the large value of its high frequency permittivity. In our calculation, undoped silicon dielectric constant $\varepsilon_{\infty,Si} = 12.27$, hole effective mass $m_h^* = 0.36m_0$, where m_0 is the free electron mass, and hole mobility $\mu_h = 450$ $cm^2V^{-1}s^{-1}$ are used for the p-type silicon. $\varepsilon_{\infty,ITO} = 3.9$, $m_e^* = 0.35m_0$, and $\Gamma=1.8\times10^{14}$ rad s^{-1} [2] are used for the ITO calculation.

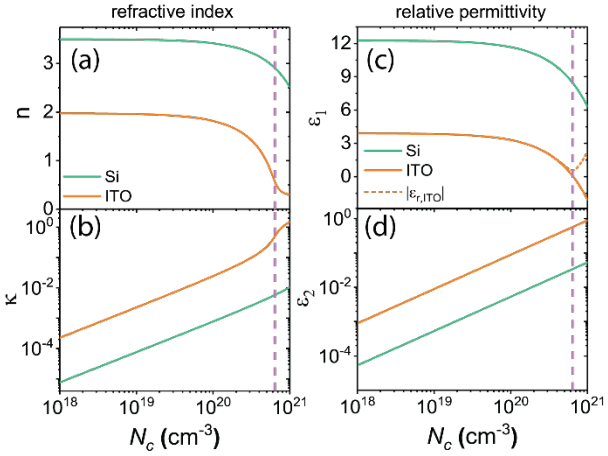

Figure 2.1 (a) The real part (n) and (b) imaginary part (κ) of the refractive indices of p-type Si (green solid) and ITO (orange solid) as a function of free carrier concentration N_c (hole in Si, $N_{h,Si}$, and electron in ITO, $N_{e,ITO}$) at wavelength λ=1.55 μm. (See Supporting Information for calculation details.) (c) The

real part (ε_1) and (d) imaginary part (ε_2) of the relative permittivity of p-type Si (green solid line) and ITO (orange solid line) as a function of N_c at wavelength λ=1.55 μm. The orange dashed line in (c) shows the absolute permittivity of ITO ($|\varepsilon_{r,ITO}|$), and the pink dashed line indicates the N_c where the ITO reaches ENZ.

2.2 Epsilon-near-zero (ENZ) induced light confinement

ENZ materials with vanishingly small permittivity exhibits intriguing optical properties, such as subwavelength light confinement, enhanced light-matter interactions, slow light effect, and extreme nonlinear dispersion. These effects have been summarized in a few review papers [100]–[102]. One of the most important ENZ effects for the E-O applications of TCO is that, at ENZ condition, the electric field will be strongly confined in TCOs due to the continuity of electric field displacement at the material interface.

$$\frac{D_{\perp,TCO}}{D_{\perp,adjacent}} = \frac{|\varepsilon_{TCO}E_{TCO}|}{|\varepsilon_{adjacent}E_{adjacent}|} = 1$$
$$\frac{|E_{TCO}|}{|E_{adjacent}|} = \frac{|\varepsilon_{adjacent}|}{|\varepsilon_{TCO}|} \tag{2.4}$$

When the electric field is perpendicular to the interface between the TCO and adjacent material, the ratio between the electric field, $E_{TCO}/E_{adjacent}$, is inversely proportional to the ratio between the absolute permittivity, $|\varepsilon_{TCO}/\varepsilon_{adjacent}|$. As the permittivity of TCO approaches zero, the electrical field will be enhanced by a factor of $|\varepsilon_{adjacent}/\varepsilon_{ENZ}|$. Considering the conservation of energy, such electric field enhancement means that the electric energy of the propagating light wave will be confined in the ENZ TCO layer. Obviously, the nearer to zero is the absolute permittivity, the stronger is the light confinement.

The ENZ induced light confinement strongly enhances the light-matter interaction, and is also the origin of other ENZ effects, such as ENZ enhanced absorption. Based on the

dissipation power density in the TCO, $P_d = \omega\varepsilon''\varepsilon_0 E_{TCO}^2/2$, we can define the TCO absorption factor A as $A = \varepsilon''_{TCO}/|\varepsilon_{TCO}|^2 \propto P_d$. The intrinsic absorption of TCO, ε''_{TCO}, will be enhanced by a factor of $1/|\varepsilon_{ENZ}|^2$, at the ENZ condition. Furthermore, when the real part of the permittivity equals zero, the imaginary part dominates the permittivity, $|\varepsilon_{ENZ}| = \varepsilon''_{ENZ}$. Then we have the absorption factor inversely proportional to the imaginary part of the permittivity, $A_{ENZ} = 1/\varepsilon''_{ENZ}$. Interestingly, at the ENZ condition, low loss material actually absorbs more photon energy than the more lossy material.

2.3 Review of E-O devices based on TCOs

In past decade, various E-O devices based on TCOs have demonstrated, such as electro-absorption (EA) modulators [73]–[75], [103], [104], MZI modulators [105]–[107], and tunable meta-surfaces [99], [108], [109]. Among them, electro-absorption (EA) modulators based on ENZ induced absorption are the most widely investigated. The basic active structure consists of a TCO/oxide/metal (or semiconductor like silicon) MOS capacitor. The electron accumulation layer at the TCO/oxide interface can be switched to ENZ condition through negative bias applied on the TCO layer, enhancing the light absorption. Through integrating the TCO MOS capacitor with an optical waveguide, we can modulate the propagating light between "ON"/ "OFF" states through switching the bias voltage. Besides, in order to increase the modulation strength, TCO based EA modulators always accompany a metal structure near the TCO layer, to further concentrate the light to the TCO active layer due to plasmonic effect [110]. Therefore, generally, there are two types of TCO EA modulators based on the waveguide structure: hybrid plasmonic silicon waveguide [74], [75], [103], [104] and metal-insulator-metal (MIM) waveguide (plasmonic slot waveguide) [73], [104], as is shown in fig 2.2a and 2.2b, respectively. In terms of experimental demonstration, H. Atwater group first reported the demonstration unit-order of refractive index modulation of TCO accumulation layer in a MOS capacitor structure in 2010 [98]. After that, several theoretical designs of EA modulators based on ENZ TCOs have been reported [103], [111]–[113]. In 2012, V. Sorger et al. experimentally demonstrated the

first EA modulator based on ENZ ITO using hybrid plasmonic silicon waveguide, achieving a 1dB/μm ER with 3λ-long device [74]. In 2018, M. Wood et al. reported the first high speed operation of this kind modulator, achieving a 2.5Gb/s modulation speed and 1.65 dB/μm ER [75]. Later, our group's demonstration improves the modulation speed to 4.5 Gb/s and shows operation speed can be potentially increased to over 15 GHz[114]. On the other hand, the first TCO EA modulator based on plasmonic slot waveguide is reported by H. Lee et al. in 2014, which achieves an ER of 2.71 dB/μm [73]. Later, our group demonstrated an plasmonic slot waveguide based ITO EA modulator [104]. Analysis shows the modulation speed can potentially exceeds to 250 GHz.

Despite EA modulators, TCO can also be used for real part refractive index modulation by biasing away from the ENZ region to avoid the large absorption. In 2018, R. Amin et al. reported an ITO-based phase shifter driven by an ITO/Al_2O_3/Si MOS capacitor, achieving a small $V_\pi L$ of 0.52 V·mm [105]. Very recently, the same group demonstrated a sub-λ MZI modulator driven by an Au/Al_2O_3/ITO MOS capacitor (fig 2.2c). Due to the plasmonic effect of the Au layer, an ultra-small $V_\pi L$ of 95 V·μm is achieved [106]. These ITO-based compact phase shifters achieving miniature $V_\pi L$ by taking advantage of the large capacitance density of the MOS capacitor, however, is at the expense of large accompanied free carrier loss, which limits the ER. It is reported that such drawback can be overcome by using high mobility TCO, such as Cadmium oxide (CdO) [107].

Moreover, the large tunability of optical properties of TCO near ENZ condition has been used to develop tunable meta-surfaces. In 2015, M. Brongersma group reported a tunable meta-surface for reflection mode which consists a subwavelength MIM plasmonic grating integrated with an metal/oxide/ITO MOS capacitor [99]. The ENZ enhanced absorption is further enhanced by the plasmonic resonance, inducing a 15% change in reflectance by modulation a thin accumulation layer. In 2016, H. Atwater group reported a gate tunable meta-surface for reflection beam steering application based on similar MIM structure [108] (fig 2.2d). At ENZ condition, small change in permittivity not only induces large variation in absorption enhancement, but also

exhibits huge relative change of real part of permittivity. The device utilizes such effect, achieving a large phase tuning of 180°. Recently, the same group reported a dual-gated meta-surface extending the phase tuning range to 303°[109].

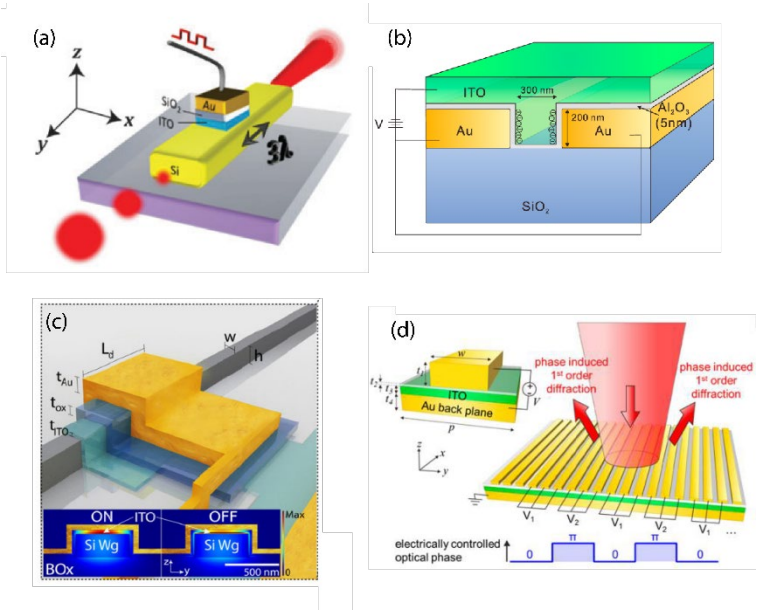

Figure 2.2 Schematic of reported TCO-based EO devices: (a) EA modulator based hybrid plasmonic Si waveguide [74]*; (b) EA modulator based on plasmonic slot waveguide* [73]*; (c) Sub-wavelength phase shifter* [106]*; (d) Gate-tunable meta-surface* [108].

Chapter 3. Electrically Tunable Subwavelength Grating Using TCO

In this chapter, we introduce our first E-O device driven by TCO, an electrically tunable subwavelength grating based on a metallic subwavelength slit array driven by a $Si/SiO_2/ITO$ MOS capacitor. In section 3.2, we introduce the design and simulation modeling of the subwavelength grating. In section 3.3, we present experimental demonstration of tunable subwavelength grating. Transmission modulation of the device is measured. In section 3.3, we conclude this chapter.

3.1 Introduction

The optical properties of TCOs can be dramatically tuned from dielectric-like to metallic-like through electrical gating [98]. During the transition, TCOs exhibit the

unique ENZ effect, which induces light confinement and enhancing the light-matter interaction. In the past few years, tunable meta-surfaces based on subwavelength MIM plasmonic gratings driven by metal/oxide/ITO MOS capacitors have reported [99], [108], which can efficiently modulate the reflected light by a thin active ITO layer. In this chapter, we design and demonstrate an electrically tunable plasmonic subwavelength grating based on a metallic subwavelength slit array coupled with a Si/oxide/ITO MOS capacitor, which can be used for both transmission and reflection modes modulation.

3.2 Design and simulation

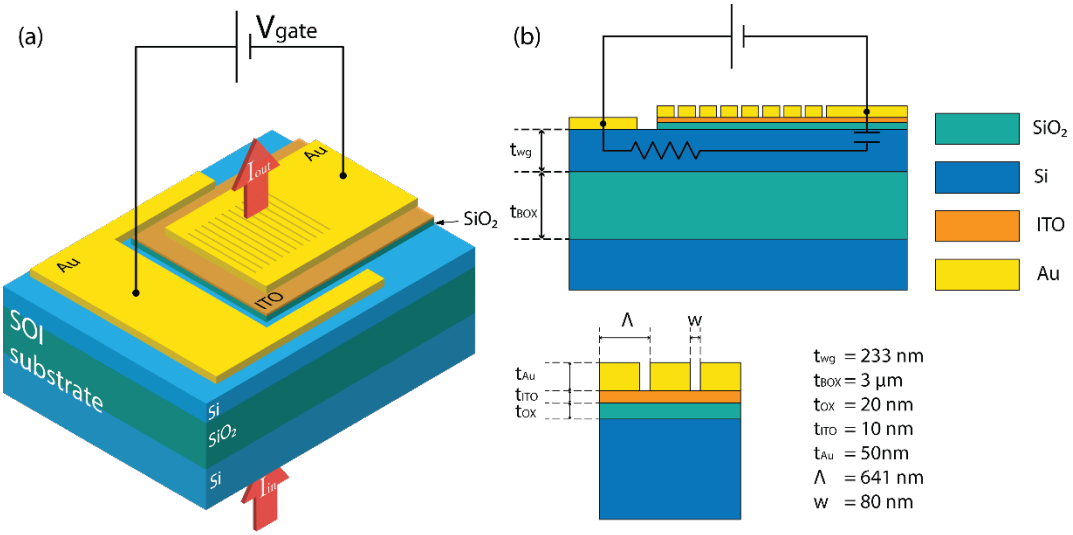

Figure 3.1 (a) 3D schematic of the tunable plasmonic subwavelength grating. (b) Cross-sectional schematic of the tunable plasmonic grating. The design parameters are labeled and listed on the figure.

Fig 3.1a and 3.1b show the 3D and cross-sectional schematic of our tunable plasmonic subwavelength grating. A Si/oxide/ITO/Au film stack is made on top of a silicon-on-insulator (SOI) substrate, which forms a MOS capacitor. Nanoslit array is fabricated on the top Au layer. The Si layer here performs as the waveguide layer, as well as the bottom electrode of the MOS capacitor. Here, we use SiO_2 as the oxide layer of the MOS capacitor. When a transverse-magnetic (TM) polarized wave is incident on the structure, surface plasmon polaritons (SPPs) excited at the Au/ITO interface are

coupled with the guided-mode resonances (GMRs) supported by the Si waveguide layer [115]. The GMR, which is also called the leaky mode, induces a peak in transmittance spectrum and a valley in the reflectance spectrum at the phase matching condition $k_{\parallel} = \beta \pm 2\pi m/\Lambda$, where $k_{\parallel}$ is the in-plane wavevector of the incident light and $k_{\parallel} = 0$ for normal incidence, β is the propagation constant of the guided mode, and m is the diffraction-order index. The main parameters that can be modified based on design are the waveguide layer thickness t_{wg}, the MOS capacitor insulator thickness t_{OX}, ITO thickness t_{ITO}, the gold layer thickness t_{Au}, the gold slit width w, and the grating period Λ. The peak transmission wavelengths of each filter are tuned by Λ. Design and optimization of subwavelength grating is performed by the DiffractMOD of RSoft photonic component design suite, which is based on rigorous coupled-wave analysis (RCWA).

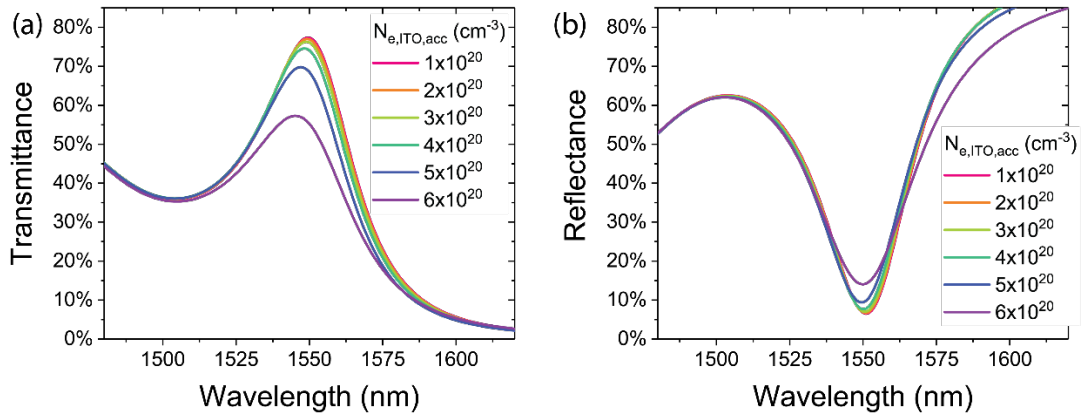

Figure 3.2 Simulated transmittance (a) and reflectance (b) spectra of the tunable grating at different electron concentration in the ITO accumulation layer.

By applying a negative bias on the ITO gate layer, electrons accumulate at the ITO/SiO_2 interface, resulting in increase of the imaginary part of the permittivity, so as the light absorption. To simplify the analysis, we consider the carrier accumulation process by adding an effective accumulation layer at the ITO/SiO_2 interface in the simulation. The thickness of the accumulation layer is usually estimated by the Thomas-Fermi screening length, l_{tf}, which is estimated to be ~1nm [111]. However, considering the triangular shape of the electron concentration distribution at the interface, we choose the thickness of the accumulation layer to be half of l_{tf}, ~0.5nm. Fig 3.2a and 3.2b show

the simulated transmittance and reflectance spectrum at different electron concentrations in the ITO accumulation layer ($N_{e,ITO,acc}$). Parameters used for simulation can be found in fig 3.1a. At zero bias, the plasmonic coupled GMR exhibits a low Q factor of ~50, due to the large index contrast between Si waveguide layer and the buried oxide cladding layer [116]. As we increase the bias voltage, ITO enters the ENZ region, and the light absorption becomes more prominent due to the ENZ induced light concentration effect in the ITO accumulation layer (Fig 3.2d). As a result, the resonance behavior is suppressed, and the transmittance/reflectance decreases/increases. Fig. 3.3a to Fig 3.3d plot the simulated electric field distribution at two different $N_{e,ITO,acc}$: the as-sputtered ITO carrier concentration with $n_0 = 1 \times 10^{20}$ cm^{-3} and the ENZ carrier concentration with $n_{ENZ} = 6.5 \times 10^{20}$ cm^{-3}. Fig 3.3e shows the modulation depth, which is defined as (high state-low state)/high state, of transmittance (ΔT/T) and reflectance (ΔR/R) as a function of $N_{e,ITO,acc}$ at 1550nm. The modulation depth achieves 32% for transmission mode and 56% for reflection mode.

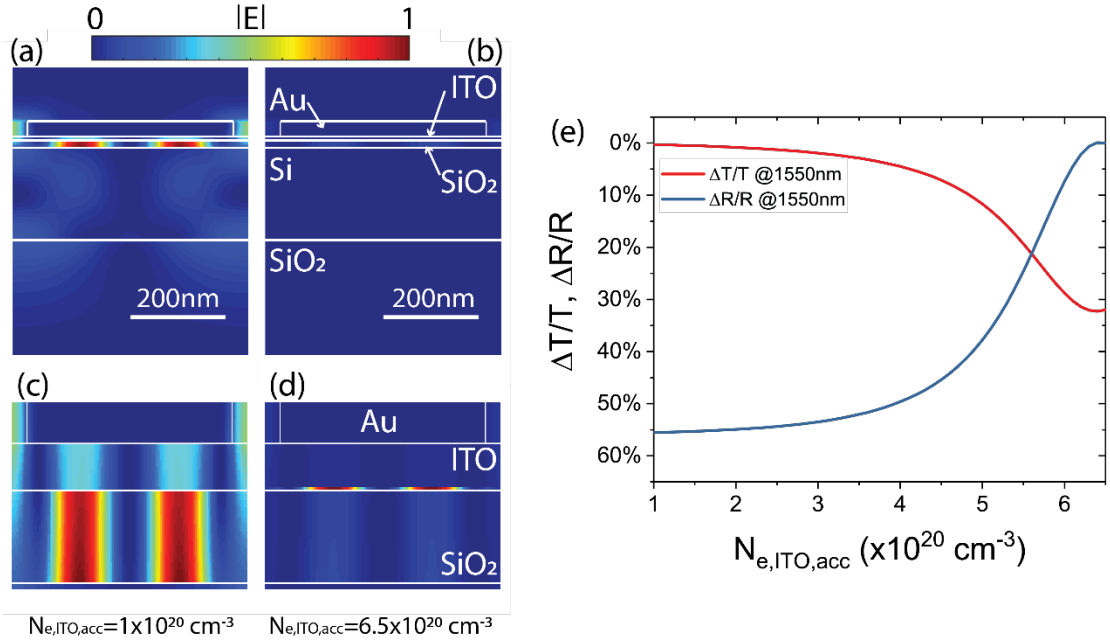

Figure 3.3 (a)-(b) Simulated electric field distribution when $N_{e,ITO,acc}$ equals to 1×10^{20} cm^{-3} and 6.5×10^{20} cm^{-3} (ENZ). (c)-(d) Zoomed in view of (a) and (b) at the ITO/SiO$_2$ interface. (e) Modulation depth of transmittance and reflectance as a function of the electron concentration in the ITO accumulation layer.

3.3 Fabrication and measurements

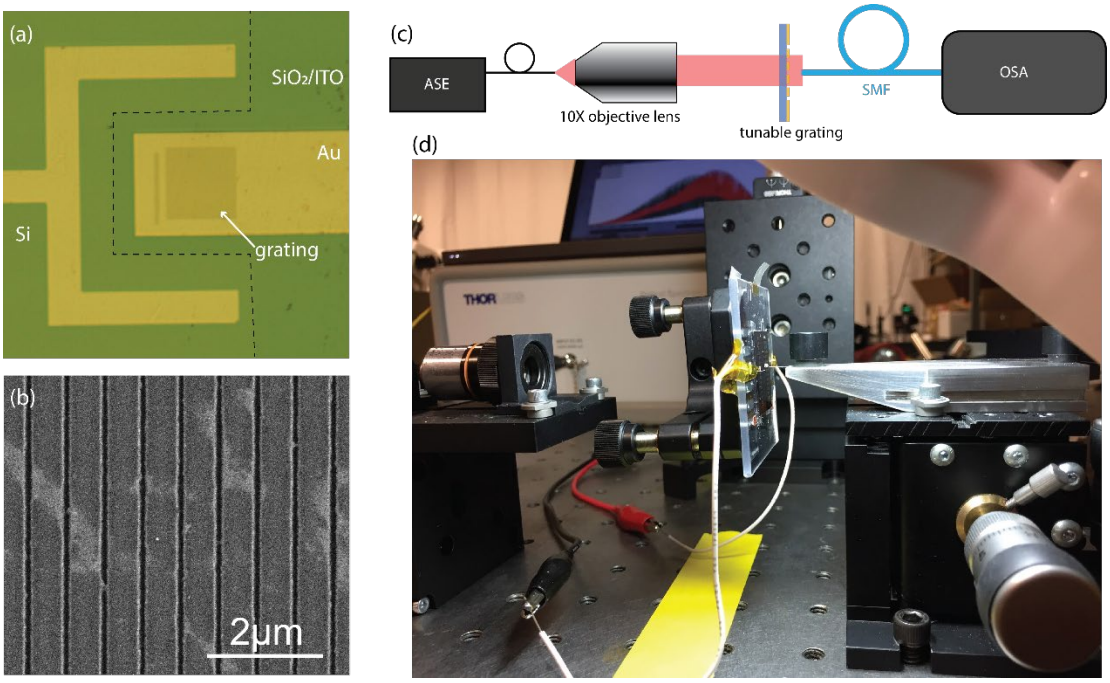

Figure 3.4 (a) Optical image and (b) Scanning electron micrograph (SEM) of the fabricated grating. (c) Schematic of the testing setup. (d) Photo of the measurement setup.

A prototype grating was fabricated. First, we started with a back side polished SOI wafer. 20nm of SiO_2 gate oxide layer is formed by thermal oxidation. Then, 10nm of ITO thin film is sputtered, followed by thermally evaporating 40 nm of Au film. 3nm of Cr film is evaporated before Au to improve the adhesion of gold. Finally, nanoslit array pattern is written on the Au film by focused-ion beam (FIB) lithography. The dimension of nanoslit array is 100 μm×100 μm. The fabricated device is shown in fig 3.4a and 3.4b.

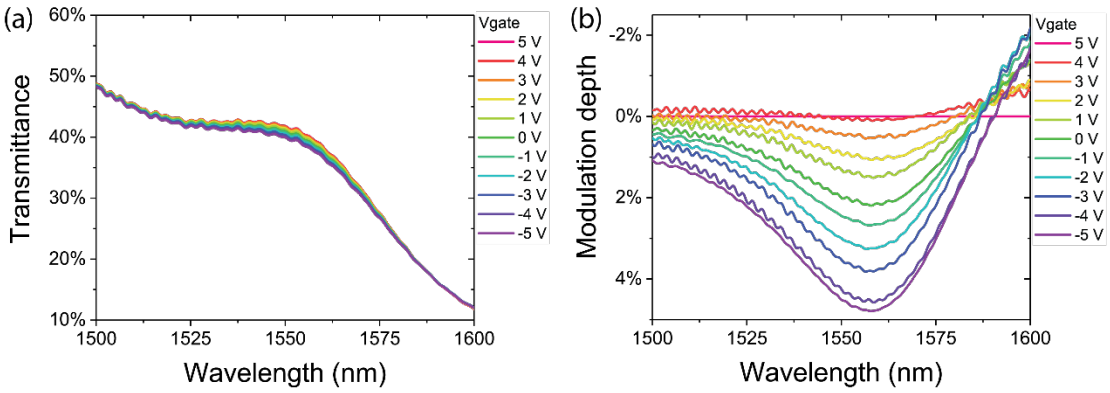

Figure 3.5 (a) Experiment transmittance and (b) modulation depth at different gate voltage.

We measure the transmittance modulation of the tunable grating. Fig 3.4c illustrates measurement setup. An amplified spontaneous emission (ASE) source with center wavelength at 1550nm is used as a input. The light from the light source is collimated by a 10× objective lens and normally incident onto the sample from the substrate side (polished silicon side). On the other side, the transmitted light is directly coupled into a single-mode fiber (SMF-28) with core diameter of 10 μm. Then, the SMF is connected to a Fourier transform IR spectrometer (OSA203, Thorlabs) to measure the transmission spectrum. The fabricated grating is mounted on a customized sample holder. The contact pads on the grating sample and holder are connected through wire bonding. Finally, the device is connected to a voltage source for applying bias. The image of the measurement setup is shown in fig 3.4d. Fig. 3.5a and 3.5b plot the transmittance spectrum and modulation depth at different gate voltage, V_{gate}. A maximum modulation depth of ~5% is observed with - 5V applied voltage (normalized to V_{gate}=5V), which is much smaller than simulation. Despite the fabrication imperfection, this is also because the dielectric strength of SiO_2 gate oxide also limits the electron concentration that can accumulate at the interface. The value $N_{e,ITO,acc}$ can reach is determined by the electrical displacement field in the gate oxide layer. Based on our calculation, SiO_2 gate oxide can accumulate $N_{e,ITO,acc}$ up to ~4×10^{20} cm^{-3} before breakdown (See section 4.1.3 for calculation details), which doesn't reach the ENZ condition. In this sense, our experiment result shows good agreement with Fig 3.3e.

We anticipate that larger modulation depth can be achieved by changing the gate oxide with high-k materials, such as HfO_2.

3.4 Summary

In summary, we design and demonstrate an electrically tunable plasmonic subwavelength grating based on a metallic subwavelength slit array coupled with a Si/oxide/ITO MOS capacitor. The electrical tunability is achieved through modifying the electron concentration in the TCO accumulation layer. Simulation shows that large modulation depth of 32% (56%) can be achieved for both transmission (reflection) mode due to ENZ induced light concentration and absorption enhancement. Experimentally we measured a transmission modulation efficiency of 5%, verifying the concept of our design. However, the device doesn't fully reach the ENZ condition limited by the dielectric strength of the SiO_2 layer, which can be improved by replacing the SiO_2 gate oxide with high-k dielectric materials.

Chapter 4. Ultra-compact High-speed Ultra-energy-efficient Silicon-TCO Photonic Crystal (PC) Nanocavity Modulator

In this chapter, we report our work on the development of the ultra-compact high-speed ultra-energy-efficient silicon-TCO PC nanocavity modulator, which consists of a one-dimensional silicon PC nanocavity integrated with a voltage switched TCO gate in the center of the PC nanocavity. Our development of the silicon-TCO PC nanocavity modulator consists of three steps, which are covered from section 4.1 to 4.3, respectively. In section 4.1, we introduce the basic device structure and the working principle of the PC nanocavity modulator, followed by the first proof-of-concept experimental demonstration. In section 4.2, we report our experimental demonstration of low-voltage operation of the nanocavity modulator, which is enabled by the extreme large resonance tunability through using the high-k material, HfO_2, as the gate insulator. In section 4.3, we describe how we optimize the nanocavity modulator for high speed

operation and present the experimental demonstration of gigahertz speed operation. In addition to that, we propose strategy to optimize the silicon-TCO PC nanocavity modulator to achieve higher bandwidth and atto-joule per bit ultra-low energy consumption. Finally, we summarize this chapter in section 4.4.

4.1 Proof-of-concept demonstration of ultra-compact silicon-conductive oxide nanocavity modulator

4.1.1 Introduction

Existing TCO-based E-O modulators are exclusively based on straight hybrid plasmonic silicon waveguide [74], [75], [103], [114], [117], [118] or plasmonic slot waveguide [73], [104] using electrically induced optical absorption from the integrated MOS capacitor. The phase change induced by the real part of the permittivity of the TCO materials, although automatically accompanying the imaginary part of the index change, does not contribution to any E-O modulation. Therefore, a relatively long modulation length (a few microns) is required to induce sufficient optical absorption. Moreover, these TCO modulators require the presence of metal gates for strong plasmonic light confinement and electronic signal conductance, which introduce relatively high optical loss even at the transparent state. In this section, we present an ultra-compact hybrid silicon-TCO PC nanocavity modulator to overcome the intrinsic drawbacks of those straight waveguide modulators. There are two exclusive advantages compared with existing TCO-based modulators. First, the active region of our plasmonic E-O modulator is free of metal. The metal gate of the MOS capacitor is replaced by an ITO gate, which induces much smaller optical absorption compared with other metal-gated modulators. This ITO-Oxide-Si capacitor offers the possibility to build a relatively high Q-factor resonator while traditional metal-oxide-ITO cannot. Second, in our nanocavity modulator, both the phase change and the absorption, from both the Si and ITO materials, will contribute coherently to E-O modulation.

4.1.2 Device design

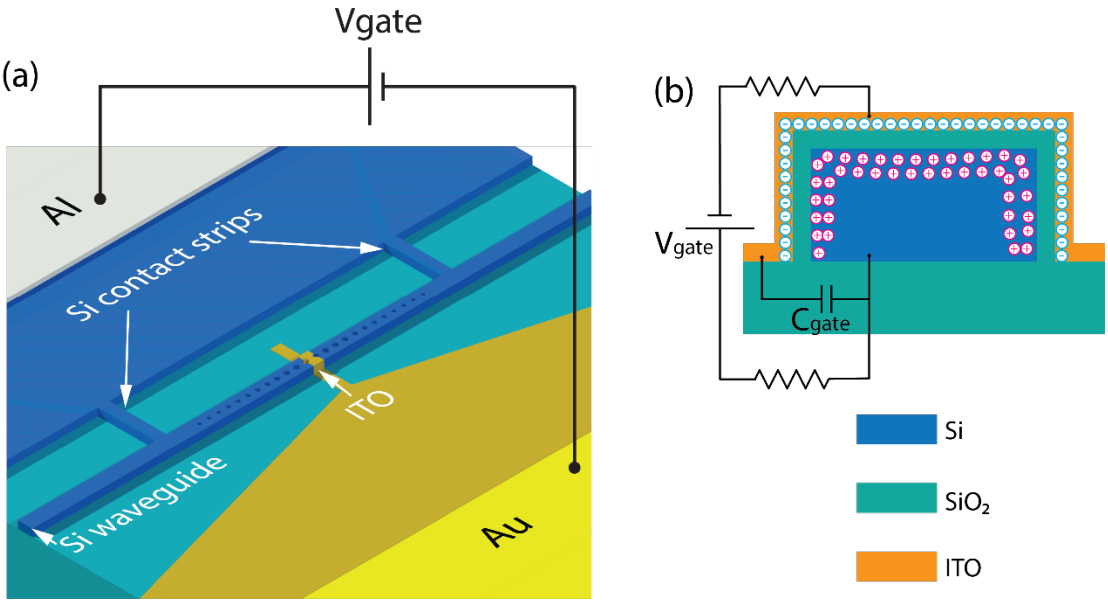

Figure 4.1(a) The 3D schematic of the Si-ITO PC nanocavity modulator. (b) The cross-section of the Si/oxide/ITO MOS capacitor at the center of the hybrid Si-ITO modulator. When a negative bias is applied on the ITO gate, electron and hole accumulates at the ITO/oxide and Si/oxide interfaces respectively.

The schematic of the Si-ITO PC nanocavity is shown in Fig 4.1a. The device consists of a MOS capacitor built at the center of the nanocavity on a silicon strip waveguide. The strip waveguide is fabricated on a p-type silicon-on-insulator (SOI) substrate with 500 nm in width and 250 nm in height. A pair of grating couplers are integrated to couple light in and out of an optical fiber. The PC cavity operates in the TE mode. Two PC mirror segments are placed back to back adjacent to the nanocavity. The air hole size is quadratically tapered down from the center of cavity region to the edge of the two mirror segments [119]. In our design, each mirror segment has 12 air holes. The filling factor, which is defined as $f=A/pw$, is tapered down from 0.23 in the center to 0.1 at the edge, where A is the air hole area, p is the air hole period, and w is the waveguide width. The period p is chosen to be 340 nm to allow the modulator to operate in the telecom wavelength range. In the center of the cavity, an ITO/SiO_2/Si film stack creates a MOS capacitor with cross-sectional view shown in Fig 4.1b. Here,

the silicon waveguide also serves as the bottom electrode despite of its relatively high resistivity. Two 400 nm wide silicon strips are used to form the conduction path between the silicon waveguide and the silicon slab with the contact electrodes. On top of that, a 20 nm thick SiO_2 layer covers the entire silicon PC nano-cavity serving as the gate insulator. Finally, a 20 nm thick ITO layer is patterned in the center of PC nanocavity, performing as the metallic gate electrode. We need to emphasize that the center nanocavity length is only 120 nm, which is at least 50× shorter than ring resonators or micro-disk resonators. A 375 nm long ITO gate is made to compensate the misalignment of the electron beam lithography (EBL) process during the fabrication. The total device footprint of our TCO modulator is only 0.6 × 8 μm^2. The E-O modulation volume is less than 0.06 μm^3 (width × height × length= 0.56 μm × 0.28 μm × 0.375 μm), namely only 2% of lambda-cubic ($0.02\lambda^3$) volume, which is the smallest active modulation region that has ever been reported to the best of our knowledge.

4.1.3 TCO/oxide/Si Metal-oxide-semiconductor (MOS) capacitor

The device operates in the accumulation mode of the MOS capacitor with the negative gate bias on the ITO gate. The applied gate voltage induces free electron and hole accumulation at the ITO/SiO_2 and Si/SiO_2 interfaces, respectively. The free carrier accumulation at both sides of the oxide interfaces contribute to the E-O modulation. We perform a numerical simulation systematically to analyze the carrier distribution in the accumulation layers versus the applied gate bias.

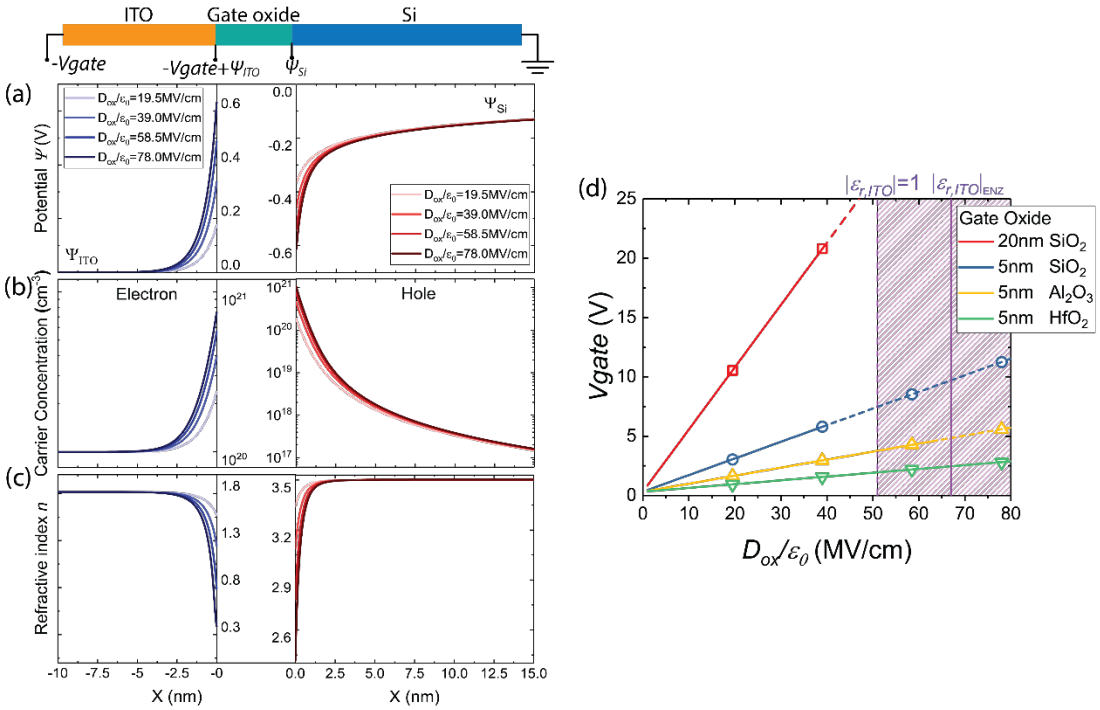

Figure 4.2 (a) Electrical potential distribution in ITO (blue lines) and Si (red lines) as a function of electrical displacement field in the gate oxide layer, D_{ox}. (b) Carrier density distribution in ITO (electron) and Si (hole) as a function of D_{ox} field. (c) The real part refractive index (n) distribution in ITO and Si as a function of D_{ox} field. (d) Gate voltage as a function of the D_{ox} field for different gate oxide layers: 20 nm SiO_2 (red line), 5 nm SiO_2 (blue line), 5 nm Al_2O_3 (yellow line), and 5 nm HfO_2 (green line). The dashed lines show the D_{ox} field range when the gate oxide layer will breakdown. The shaded area enclosed by the purple dashed line shows the D_{ox} field range when the permittivity of ITO accumulation layer, $|\varepsilon_{r,ITO}|$, is smaller than 1, representing the ENZ region; the purple solid line indicates the D_{ox} field when $|\varepsilon_{r,ITO}|$ reaches minimum ENZ value.

The carrier concentration distribution is calculated based on classic MOS theory, by numerically solving the Poisson equation [120]. Because of the huge difference of the doping level between ITO and Si, different expressions are needed to model the relationship between the carrier density distribution and the electric potential distribution. The main difference is that the degenerated doping of ITO results in an initial Fermi level higher than the bottom of the conduction band. Therefore the electron density and electric potential in ITO behave more like a metal, which can be approximated by the Thomas-Fermi screening model [103], [111]. The local electron

density distribution near the conduction band *n* and electrical potential Ψ is expressed as

$$n = \frac{1}{3\pi^2}\left(\frac{8\pi^2 m_e^*}{h^2}\right)^{\frac{3}{2}}(E_F + \Psi)^{\frac{3}{2}}, \tag{4.1}$$

where h is the plank constant and $m_e^* = 0.35m_0$ is the electron effective mass near the conduction band. The Fermi energy is defined as

$$E_F = \frac{h^2}{8\pi^2 m_e^*}(3\pi^2 N_0)^{\frac{2}{3}}, \tag{4.2}$$

where N_0 is the initial carrier concentration of the ITO bulk. On the Si side, since a large band bending is expected in our device, traditional Boltzmann distribution approximation is not accurate. Therefore, a rigorous analysis using Fermi-Dirac distribution is considered to model the Si. The local hole density distribution p is calculated as

$$p = 4\pi(\frac{2m_{h,DOS}^*}{h^2})^{\frac{3}{2}}\int_{-\infty}^{E_V}(E_V - E)^{\frac{1}{2}}f(E)\,dE, \tag{4.3}$$

where $m_{h,DOS}^* = 1.15m_0$ is the density of states effective mass of hole in silicon and E_V is valence band top. The Fermi-Dirac distribution is defined as $f(E) = \frac{1}{1+\exp\left[(E_F-\Psi-E)/kT\right]}$. Because $m^*_{h,DOS}$ of Si is more than 3× of m^*_e of ITO, the effective density of state for holes in the Si valence band, $N_V = 2[\frac{2m_{h,DOS}^* kT}{h^2}]^{\frac{3}{2}}$, is much larger than that for electrons in the ITO conduction band, $N_C = 2[\frac{2m_e^* kT}{h^2}]^{\frac{3}{2}}$. After we get the carrier concentration distribution, we can calculate the electric field and electric displacement field at the gate insulator interface.

In order to obtain representative results, we conduct our modeling using the electric displacement field D_{ox} instead of the electric field *E*. The boundary condition only requires the value of D_{ox} in the gate oxide layer, making the modeling independent of the gate oxide material and thickness. We plot the electric potential and carrier distribution as a function of D_{ox} as shown in Fig 4.2a and 4.2b. We can see that the

electron concentration in ITO ($N_{e,ITO}$) accumulates from 1x10^{20} cm^3 to 7.46x10^{20} cm^{3}and the hole concentration in Si ($N_{h,Si}$) accumulates from 1x10^{17} cm^3 to 1.08x10^{21} cm^3 with a D_{ox}/ε_0 value of 78 MV/cm. Surprisingly, the peak $N_{h,Si}$ is even higher than that of $N_{e,ITO}$, which is because of the larger effective density of state of Si compared with ITO. As a result, $N_{h,Si}$ in Si is more sensitive to electrical potential modulation than $N_{e,ITO}$ in ITO. The ITO reaches the ENZ region when the $N_{e,ITO}$ is 6.4x10^{20} cm^3 with D_{ox}/ε_0 of 67 MV/cm. Figure 4.2c plots the corresponding distribution of the refractive indices of ITO and Si. Both ITO and Si exhibit dramatic refractive index modulation within a thin layer of ~1 nm thick close to the interface even at a relatively small D_{ox} field. For the ITO side, the effect of this thin accumulation layer is already well recognized [74], [103], [111]. This layer is often treated as an effective accumulation layer and the thickness can be estimated by the Thomas-Fermi screening length, L_{tf}. On the Si side, this thin accumulation layer could also play a critical role for the E-O modulation but was not utilized by simple straight waveguides in published papers. Detailed analysis will be provided in the following section. Next, knowing the D_{ox} field, we can calculate the gate voltage by

$$V_{gate} = |\Psi_{ITO}| + \frac{D_{ox}t_{ox}}{\varepsilon_0\varepsilon_{oxide,st}} + |\Psi_{Si}|, \tag{4.4}$$

where Ψ_{ITO} and Ψ_{Si} are the surface potential at the ITO/SiO_2 and the Si/SiO_2 interface, ε_0 is the vacuum permittivity, and $\varepsilon_{oxide,st}$ and t_{ox} is the static relative permittivity and thickness of the gate oxide layer. Static relative permittivities used for the calculation are: $\varepsilon_{ITO,st}$=9.3, $\varepsilon_{Si,st}$=11.2, $\varepsilon_{SiO2,st}$=3.9, $\varepsilon_{Al2O3,st}$=9, and $\varepsilon_{HfO2,st}$=25. The dielectric strength of the gate insulators we use to estimate the breakdown voltage are E_{SiO2}=10 MV/cm, E_{Al2O3}=7 MV/cm and E_{HfO2}=5 MV/cm [121]. Figure 4.2d plots the applied gate voltage as a function of D_{ox} field with different oxide materials and thickness. Here the dashed lines indicate a large D_{ox} field exceeding the breakdown of the gate oxide. From this analysis, it is obvious to draw a conclusion that thinner oxide layer thickness and high-k materials will help to reduce the applied bias voltage. Besides, to truly reach the ENZ operation of the ITO layer, a high-k gate material such as HfO_2 is necessary. In our

experimental demonstration, we chose SiO_2 as the gate oxide material primarily due to ease of access with our fabrication facilities.

4.1.4 Operation principle

The Si-ITO nanocavity modulator operates in the dual mode of cavity resonance and optical absorption. At a relatively small applied bias, the device operates in the "normal mode", when the $N_{e,ITO}$ is not high enough to push ITO into the ENZ confinement. Modulation of the nano-cavity resonance dominates, which mainly comes from the real parts of the permittivity change ($\Delta\varepsilon_1$) induced by the plasma dispersion effect of the ITO and Si. Based on the cavity perturbation theory (See section 7.3.1 for details), we can have that the permittivity change caused by the plasma dispersion is proportional to the change of free carrier concentration, namely $\Delta\varepsilon \propto \Delta N_c$. This means that the resonance shift induced by a 1 nm thick accumulation layer with a N_c of 1×10^{20} cm^{-3} is equivalent to the shift induced by a 100 nm thick layer from fully depletion to a N_c of 1×10^{18} cm^{-3} under the uniform optical field distribution approximation.

We simulate the optical properties of the Si-ITO PC nanocavity by the commercial software package (Lumerical MODE) based on modified 2-D finite-difference time-domain (FDTD) method which treats the vertical direction with the effective index approximation. Because of the thickness of the ITO accumulation layer is very thin, it requires very fine mesh at the accumulation layer to numerically simulate the device, which would make the simulation of this kind of device very time-consuming if 3-D FDTD was used. Through the current method we can visualize the operation principle of the PC nano-cavity modulator at the cost of spectral accuracy which can be improved by 3-D FDTD. In the simulation, we consider the ITO accumulation layer thickness to be 1 nm L_{tf}. On the Si side, uniform optical field distribution approximation is used to simplify the analysis. Basically, we assume the same amounts of holes are induced in the Si side and they are uniformly distributed over the active region.

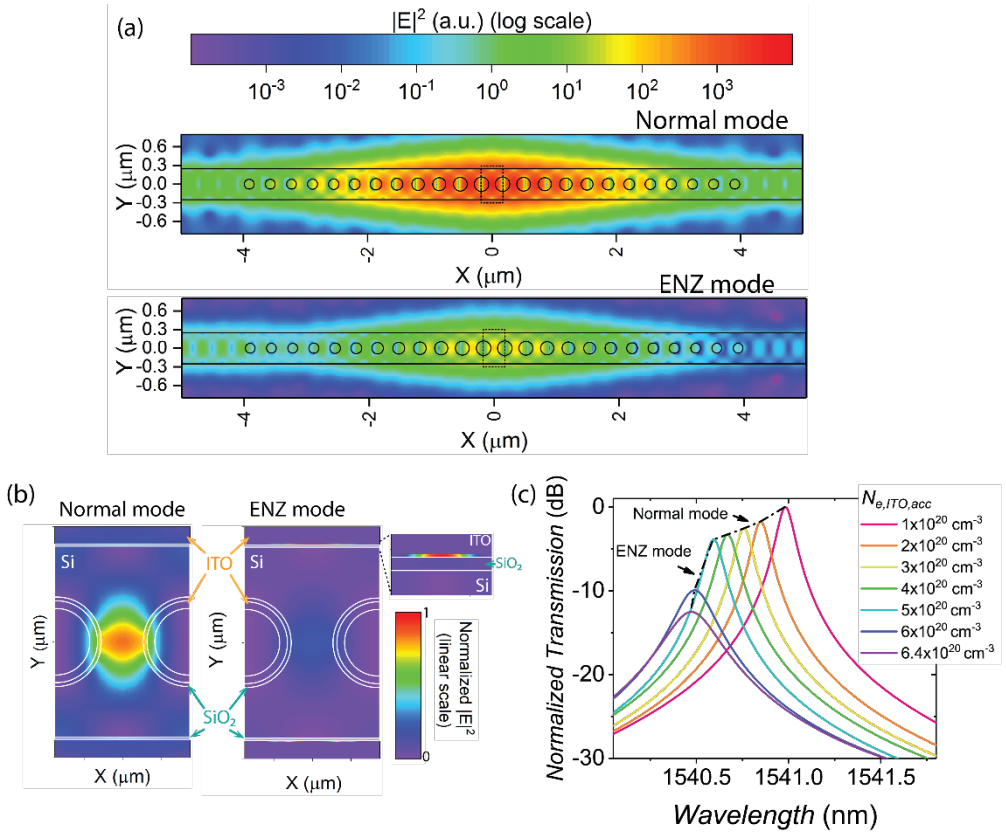

Figure 4.3 (a) The PC cavity mode profiles of "normal mode" (accumulation layer $N_{e,ITO}=1\times10^{20}$ cm^{-3}) and "ENZ mode" (accumulation layer $N_{e,ITO}=6.4\times10^{20}$ cm^{-3}). The optical field intensity is plotted in log scale. Clearly, at "ENZ mode" the transmission drops due to the ITO absorption. (b) The zoomed-in mode profile of "normal mode" and "ENZ mode". The optical intensity is plotted in normalized linear scale. Insert: further zoomed-in mode profile of "ENZ mode" at the ITO/SiO_2 interface. It is clearly shown that in "ENZ mode" the optical field is strongly confined in the accumulation layer at the side wall. (c) Simulated normalized transmission spectrum at different free carrier concentration $N_{e,ITO,acc}$ in the ITO accumulation region. The black dashed line outlines the change of the transmission peak as $N_{e,ITO}$ increases.

Fig 4.3a and 4.3b show the PC crystal cavity mode profile. The cavity mode has a good overlap with the accumulation layer of the MOS structure near the center air holes and is relatively uniform. Thus, it is reasonable to assume an approximately uniform optical distribution here. The resonance shift has the relationship:

$$\Delta\omega \propto \frac{\omega \int \Delta N_c \cdot dv}{\varepsilon_{eff} \cdot v_c} = \frac{\omega \Delta Q}{\varepsilon_{eff} \cdot v_c} = \frac{\omega CV}{\varepsilon_{eff} \cdot v_c} = \frac{\omega CV}{\varepsilon_{eff} \cdot \gamma v_a} \propto \frac{C}{v_a}, \tag{4.5}$$

where ε_{eff} and v_c are the effective permittivity and mode volume of the cavity mode; ΔQ is the accumulated free carriers induced by the applied voltage V; C and v_a are the capacitance and volume of the active modulation region of the modulator respectively; and γ is the coefficient describing the overlapping between v_a and v_c. Additionally, due to the small mode volume of the PC cavity mode and its large overlap with the active modulation region of the modulator (Fig 4.3b), we can conclude that the resonance shift is proportional to the capacitance per unit active volume. Large capacitance C and small active volume v_a are preferred for high modulation efficiency. Since we effectively construct a 3-D MOS capacitor in the center of the PC cavity, free carriers accumulate at all three interfaces. As large C/v_a ratio is realized, we can achieve significant resonance modulation within 0.02 λ^3 active modulation volume. In spite of the resonance shift induced by the real part permittivity change, the optical absorption from the imaginary part change of the permittivity, which is usually a minor effect in pure silicon modulators, also plays an important role in the Si-ITO hybrid modulator because of the 30-140× larger imaginary part of ITO compared with Si. As a result, larger extinction ratio can be achieved at the same resonance tuning. As the applied bias increases, the accumulation layer of ITO approaches the ENZ region as shown by the shaded area in Figure 4.2d. Once the modulator reaches the "ENZ mode", the optical mode starts to be confined in the ITO accumulation layer. This ENZ confinement effect is highly polarization sensitive. For our PC nano-cavity design operating in the TE mode, it mainly happens at the sidewall interface as shown in Figure 4.3b. The ENZ confinement effect will dramatically enhance the absorption which is proportional to $\frac{\varepsilon_{2,ITO}}{2|\varepsilon_{ITO}|^2}$ [122]. In this case, the optical absorption mode dominates. Figure 4.3c plots the simulated transmission spectra of the hybrid Si-ITO modulator at different carrier concentration in the accumulation region, $N_{e,ITO,acc}$. The black dashed line outlines the evolution of the transmission peak. The trend from the normal resonance modulation to ENZ electro-absorption is clearly shown as $N_{e,ITO}$ increases.

4.1.5 Fabrication and experiment measurements

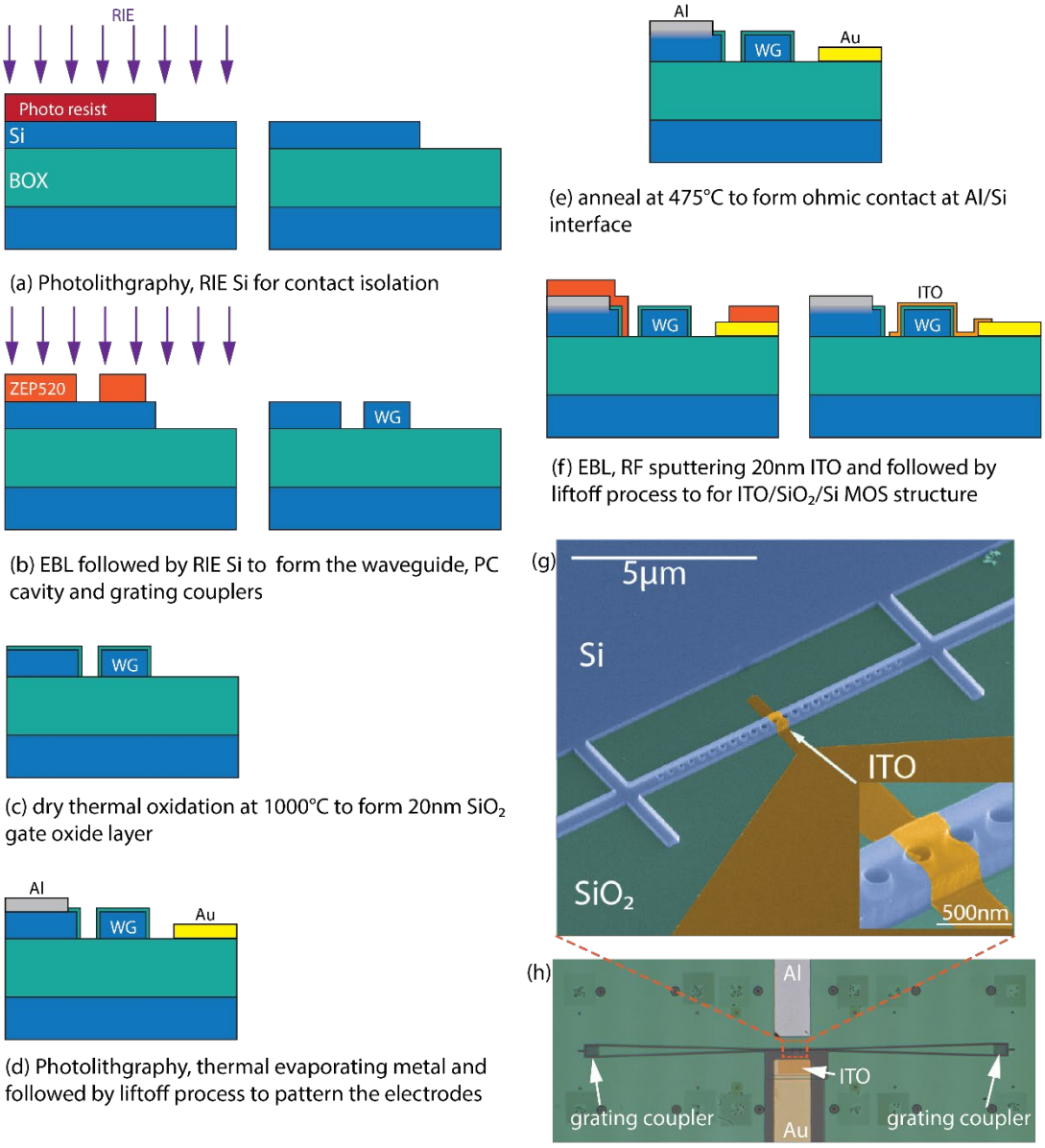

Figure 4.4 (a)-(f) Fabrication process flow charts of the Si-ITO PC nanocavity modulator. (g) The colored scanning electron micrograph (SEM) of the fabricated Si-ITO modulator. The insertion figure shows the zoomed-in view of the center of the MOS capacitor region. (h) Optical image of the fabricated modulator.

Fig 4.4a to 4.4f illustrate the fabrication process of the Si-ITO PC nanocavity modulator. The fabrication starts on a p-type silicon-on-insulator (SOI) substrate with doping level

of 1×10^{15} cm^{-3}. A first step contact photolithography and reactive ion etching (RIE) process is performed to pattern the Si layer in order to provide electrical isolation for the electrodes. Then, the silicon waveguide, cavity and grating coupler patterns are defined by electron beam lithography (EBL). RIE is used to etch into the 250 nm thick silicon layer to the bottom oxide. Next, 20 nm thick SiO_2 is formed through thermal oxidation. After that, metal contact is patterned using contact photolithography, thermal evaporation and lift off process. Al is deposited on Si and annealed at 475°C in H_2:N_2 forming gas environment for 10min to form ohmic contacts. Au is chosen to form the contact with the ITO. Finally, the ITO pattern is also defined by a second step EBL, followed by RF sputtering 20 nm thick ITO and lift off process.

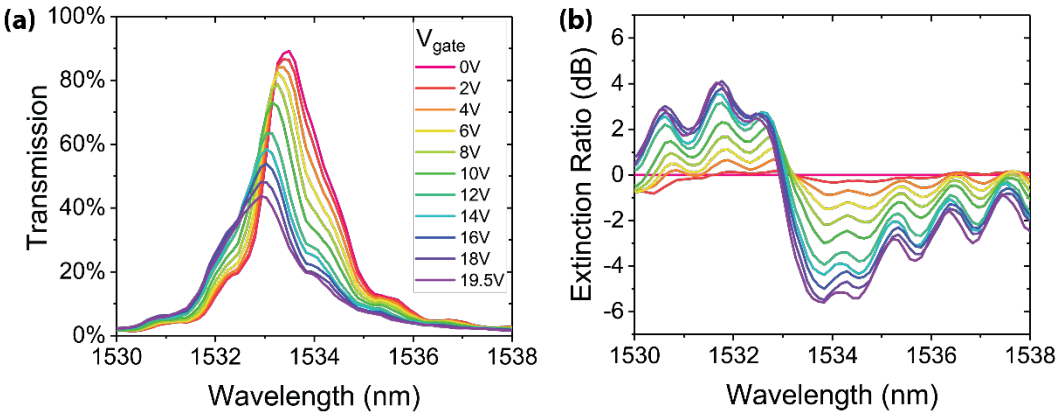

Figure 4.5 (d) Measured static transmission spectrum of the Si-ITO PC nanocavity modulator as a function of the applied bias voltage. The DC applied bias ranges from 0 to 19.5 V. (e) Measured extinction ratio (ER) spectrum as a function of the applied bias voltage.

The E-O modulation response of fabricated hybrid Si-ITO modulator was characterized. To test the device, light from a tunable laser or an amplified spontaneous emission (ASE) diode is coupled into and out of the silicon waveguide by grating couplers using single-mode optical fibers with 10° tilted angle. Polarization-maintaining fiber is used as the input fiber in order to maintain the TE polarization. For the DC modulation testing, a DC bias voltage is applied on the top ITO gate electrode, while the bottom silicon waveguide is grounded. The output spectrum is measured by the spectrum analyzer (Thorlabs, OSA203). For the dynamic testing, an AC signal from a function generator (Tektronix, FG 503) is applied. The output signal is detected by a

photodetector (Thorlabs, PDA10CF) and measured by an oscilloscope. Fig 4.5a shows the measured transmission spectra as a function of the applied bias. The spectra are normalized to a straight Si waveguide as the reference. The insertion loss (IL) of the PC nano-cavity modulator is only 0.5 dB at the peak resonance wavelength. The free carrier concentration of as-sputtered ITO is 1×10^{20} cm^{-3}, which is still a dielectric material at telecom wavelengths. The measured Q-factor after ITO deposition is around 1,000, which is slightly smaller than the Q-factor measured before sputtering the ITO (~1,200), proving that the degradation of the Q-factor due to the thin ITO layer is minor. The resonance wavelength blue-shifts by 0.57 nm with a change in DC bias from 0 to -19.5 V, indicating a 30 pm/V modulation efficiency. In the meanwhile, we observe a significant drop of the peak transmission by 45.34%, which is caused by the resonance shift as well as the optical absorption. The MOS capacitor operation is verified by the low leakage current, which is measured to be less than 100 fA at -20V. Fig 4.5b plots the extinction ratio (ER) spectrum as a function of the applied bias. A usable optical bandwidth of greater than 1nm is observed if we allow 1 dB variation of the ER. The maximum modulation is observed at 1533.78 nm, which introduces an additional loss of 0.75 dB than the peak wavelength. The transmission varies by 5.6 dB with a bias changing from 0 V to -19.5 V. The dynamic modulation speed is demonstrated up to 3.2 MHz with an AC voltage swing of 0 to -12 V (as shown in Fig 4.6), which is limited by our testing instruments.

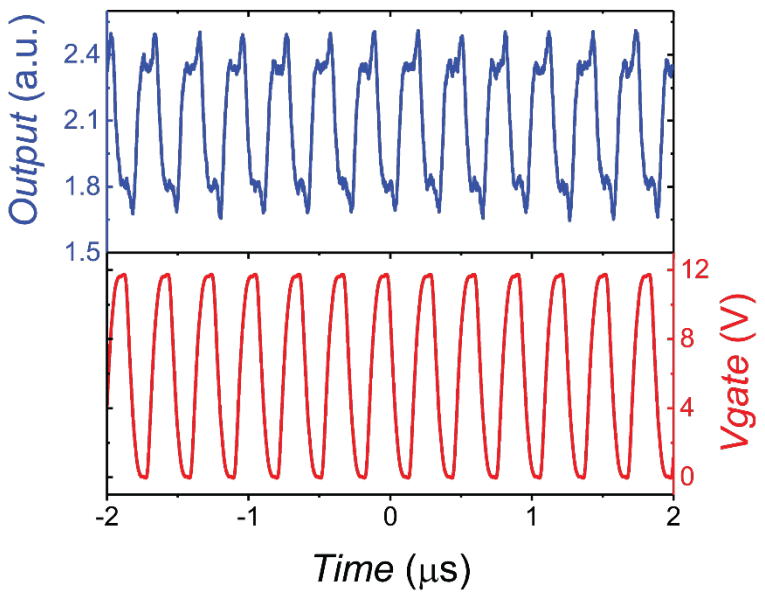

Figure 4.6 AC optical modulation testing results at 1534.78 nm with 0 to -12 V sweep input bias voltage at 3.2 MHz.

4.1.6 Modulation bandwidth and energy efficiency

Here we estimated the modulation speed and energy efficiency of the hybrid Si-ITO nano-cavity modulator. The speed of the modulator is limited by the RC delay since its operation is based on the fast accumulation mode of a MOS capacitor. Fig 4.7 shows the equivalent circuit model of the modulator. We simulate the capacitance of the modulator (including the whole PC nano-cavity and ITO gate in the active region) through commercially available software (ANSYS HFSS) based on finite element method (FEM). The simulation gives the capacitance of the modulator to be 1.28 fF. The total series resistance consists of three parts: the electrode resistance $R_{electrode}$, the resistance of ITO gate R_{ITO}, and the resistance of Si conduction path R_{Si}. R_{Si} again consists of three parts: the resistance of the conduction strips (2 μm long) R_{strip}, the resistance of PC waveguide (~5 μm long on each side) $R_{waveguide}$, and the resistance of the PC cavity (~200 nm long) R_{cavity}. For our current fabricated device, the series resistance is dominated by R_{Si} due to the lightly doped SOI slab. The doping level is around 1×10^{15} cm^{-3}, and the corresponding Si resistivity is 13.5 Ωcm [120]. Then, R_{strip}, $R_{waveguide}$ and R_{cavity} can be estimated to be 1.4 MΩ, 3.4 MΩ and 70 kΩ, respectively.

The total R_{Si} is around 4.9 MΩ. Consequently, our current device has a relative slow RC limited speed of around 26 MHz. However, because the optical mode of PC cavity is concentrated in the center cavity region, so that we can greatly reduce the series resistant while keep the optical loss at a moderate level by separately doping the Si conduction strip and PC waveguide region to a high doping level of 5×10^{18} cm^{-3} and keeping the cavity region at a moderate high doping level of 1×10^{17} cm^{-3}. The Si resistivity is reduced to 0.0145 Ωcm and 0.197 Ωcm, respectively. Then, R_{strip}, $R_{waveguide}$ and R_{cavity} can be reduced to 1.5 kΩ, 3.5 kΩ and 1 kΩ, respectively. Thus, the total R_{Si} becomes 6 kΩ, which is at the same order of magnitude of R_{ITO} under current configuration, ~3 kΩ. The total series resistance becomes 9 kΩ. The optical loss of a passive silicon waveguide with high level doping is around 0.017 dB/μm according to our optical FEM simulation. A 10 μm long silicon waveguide with high doping level will only introduce an additional loss of 0.17 dB. Besides, the corresponding silicon waveguide loss of moderate high doping level is 3.4×10^{-4} dB/μm. For a cavity with moderate high Q factor of a few thousand, the increasing in optical loss is also minor. As a result, the RC limited bandwidth can be increased to 14 GHz.

The energy efficiency of the modulator is estimated using $E_{per\ bit} = CV^2/4$. Assuming a 12 V voltage swing (3dB ER at the resonance peak), the energy consumption of the device is only 46 fJ/bit. Since the free carrier accumulation in the MOS only depends on the *D* field in the gate insulator, the performance of the hybrid silicon-ITO modulator can be further improved with high-k materials such as HfO_2. For example, if we replace the 20 nm SiO_2 with 5 nm thick HfO_2, the applied voltage will be reduced to 1 V to achieve the same *D* field using current 12 V bias. In this case, the RC limited speed will decrease due to the increased capacitance. However, the resonance tuning efficiency will increase to 360 pm/V and the energy consumption will drop to 6.2 fJ/bit. In addition, our current hybrid silicon-ITO nano-cavity modulator only possesses a moderate Q-factor of 1,000 due to our fabrication quality such as the surface roughness and the deviation of the air hole diameters. Through advanced designs [123] and optimized fabrication, PC nano-cavity with higher Q factor is achievable. We anticipate that both the ER and the operation voltage will be improved in further development,

offering the possibility to achieve hundreds of atto-joule/bit energy efficiency in the future.

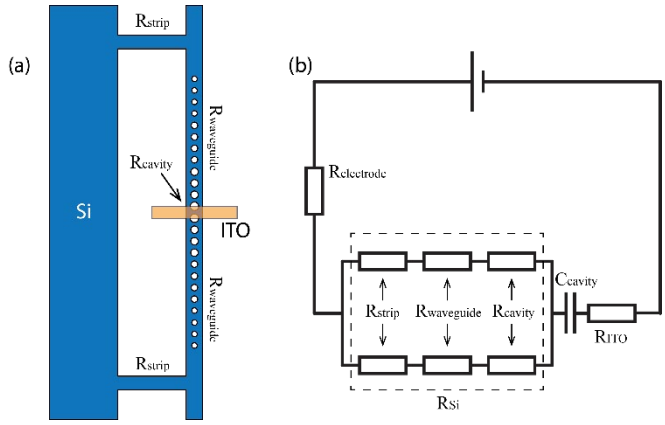

Figure 4.7 (a) Schematic of the hybrid Si-ITO modulator. (b) Equivalent circuit model of the modulator.

4.1.7 Summary

In summary, we demonstrate an ultra-compact electro-optic modulator with total device footprint of 0.6 × 8 μm^2 based on a one-dimensional silicon PC nanocavity integrated with an ITO/SiO_2/Si MOS capacitor. The active modulation volume is only 0.06 um^3, which is less than 2% of the lambda-cubic volume. The device operates in the dual mode of cavity resonance and optical absorption by exploiting the refractive index modulation from both the conductive oxide and the silicon waveguide induced by the applied gate voltage. We experimentally achieved a wavelength tuning of 30 pm/V with a moderate Q-factor of 1000, which corresponds to 3dB driving voltage of 12V and high energy efficiency of 46 fJ/bit. Compared with reported TCO-based plasmonic modulators, the active region of our device is completely free of metallic materials, which offers a low device loss of only 0.5 dB and better compatibility with CMOS processes. Compared with conventional silicon ring resonator or micro-disk modulator, our device shows exclusive advantages as it can provide a larger resonant wavelength tuning due to the small modulation volume. Finally, we show that with reasonable optimization, the Si-TCO PC nanocavity modulator can potential achieve both low driving voltage, high operation bandwidth, and ultra-low energy consumption with reasonable optimization, such as using high-k material as MOS insulator, reducing

series resistance by optimizing doping of the semiconductor conduction path, and improving Q factor.

4.2 Low driving voltage silicon-conductive oxide nanocavity modulator

4.2.1 Introduction

Silicon photonics offers the great potential to increase the integration level of photonics systems with CMOS circuits, and ultimately monolithic integration that can significantly enhance the bandwidth of the optical interconnects and reduce the cost and energy consumption by orders of magnitude. To achieve this goal, it requires future silicon E-O modulators, the basic building block for optical communication systems, to be ultra-compact, high bandwidth and energy efficient. More importantly, the driving voltage of the modulator must be compatible with CMOS driving circuits, ideally directly driven by a CMOS logic gate. For example, 32 nm CMOS technology node requires a peak-to-peak voltage swing around 0.9V [124] and this value will further scale down with more advanced CMOS technology.

In section 4.1, we report that by building a TCO/oxide/Si MOS capacitor on a PC nanocavity, we may take full advantage of the real part and imaginary part modulation of the optical permittivity from both TCO and Si, which enables us to achieve an efficient modulation in a sub-wavelength scale active region. However, the tuning efficiency is limited by the small capacitance density due to the SiO_2 gate insulator layer. In this section, we report a low-voltage TCO-gated silicon PC nanocavity modulator using optimized MOS capacitor consisting of indium oxide (In_2O_3)/HfO_2/p-Si stacked nanostructure. Using the 10nm thick high-k dielectric material, HfO_2, as the gate insulator layer greatly increases the capacitance density in the active region, bringing unprecedented energy efficiency.

4.2.2 Device design

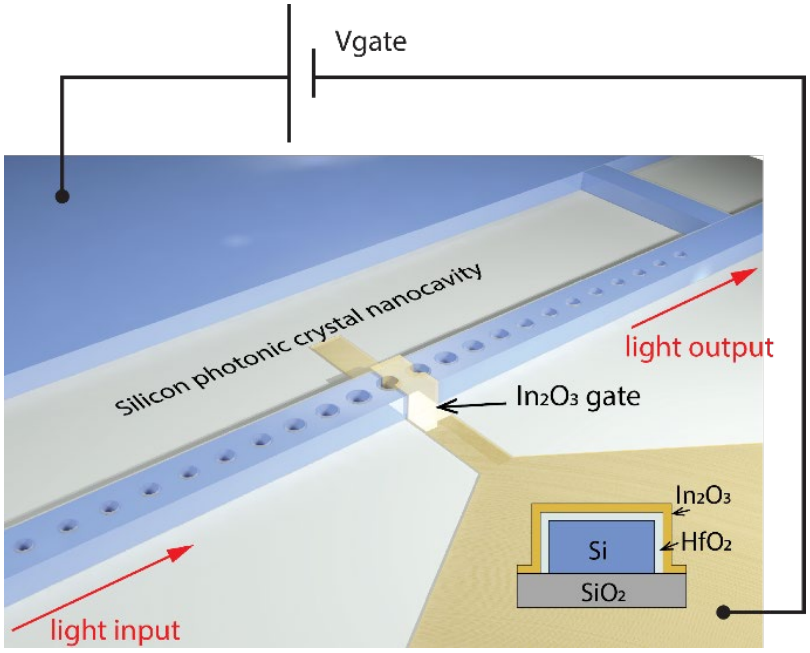

Figure 4.8 3D Schematic of the Si-In_2O_3 PC nanocavity modulator. Inset: cross section schematic of the In_2O_3/HfO_2/p-Si film stack in the active region.

Fig 4.8 shows the schematic of the PC nanocavity E-O modulator. The PC nanocavity is similar to the previous section, which is created on a strip silicon waveguide with 500 nm in width and 245 nm in height. Two tapered PC mirror segments are placed back to back, resulting in a zero-length cavity. Each mirror segment consists of 12 air holes with a period of 340 nm. The size of air holes is quadratically tapered from the edge to the center. An In_2O_3/HfO_2/p-Si film stack is formed in the center of nanocavity, forming a MOS capacitor which is the active region of the modulator with cross sectional view shown in the fig 1 inset. Here, the p-Si performs as the semiconductor layer. Two silicon strips are placed 5μm away from the center on each side of the cavity, providing electrical connection between the silicon cavity and the silicon slab contacted with the metallic electrode. A 10nm thick high-k dielectric, HfO_2, film serves as the gate oxide. On the top, a 20nm thick In_2O_3 film acts as the TCO gate electrode. Here, we choose In_2O_3 as the TCO material instead of previously used ITO, because In_2O_3 offers slightly higher mobility than ITO in our fabrication facility, which can

potentially improve the plasma dispersion effect. The total length of the overlapping area is 350 nm.

4.2.3 Optical mode volume

Compared with other high-Q resonators such as micro-ring and micro-disks, PC nanocavity has more confined mode volume [119], [125]. (See section 7.3.2 for a detailed comparison between different types of silicon micro-resonators.) We simulate the PC nanocavity modulator based on 3D finite-difference time-domain (FDTD) method. The nanocavity operates in the transverse-electric (TE) mode. The simulation shows an ultra-compact mode volume of 0.049 μm^3 ($0.25(\lambda/n)^3$), which is more than one order of magnitude smaller than the most compact micro-disk resonator [126]. Fig 4.9a and 4.9b shows cross sectional and top view of the optical mode profile of the TE cavity mode. Best tuning efficiency of plasma dispersion effect happens when the carrier modulation happens near the region where the optical field has the maximum power density (See section 7.3.1). In the PC nanocavity modulator, this corresponds to the center silicon region (~130 nm wide) between two PC segments. Again, we chose the In_2O_3 gating length to be slightly bigger than one period between air holes, majorly due to the consideration of fabrication tolerance. But it still gives us an ultra-small active volume of V_a =0.06 μm^3.

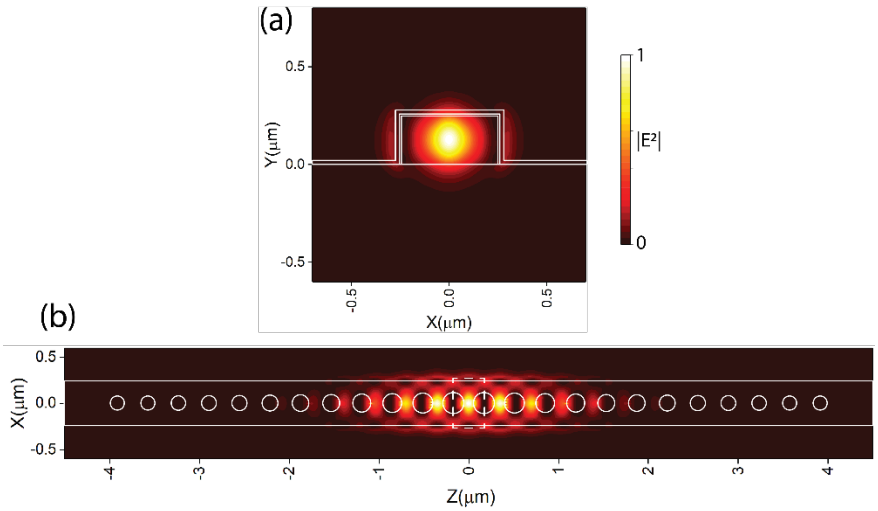

Figure 4.9 (a) Cross sectional $|E^2|$ distribution in the center of the Si-In_2O_3 PC nanocavity (Z=0μm). (b) $|E^2|$ distribution in the center plane of the PC nanocavity.

4.2.4 Capacitance density

The active region of the PC nanocavity modulator is driven by a MOS capacitor. A negative bias applied on the In_2O_3 gate produces free carrier accumulation at both the In_2O_3/HfO_2 (electron) and the HfO_2/p-Si (holes) interfaces. We know that the permittivity change caused by the plasma dispersion is proportional to the change of free carrier concentration. A MOS capacitor can easily provide a huge capacitance density using thin high-k gate insulator layer. For example, a MOS capacitor with 10 nm HfO_2 gate oxide layer has a large capacitance density of 22.1 fF/μm^2. As comparison, the capacitance density for PN junction with doping level of 10^{18} cm^{-3} is only ~1.5 fF/ μm^2. Especially for our PC nanocavity modulator, it is actually a 3D-MOS capacitor. Free carriers can accumulate at all the surrounding interfaces (side wall interfaces in four in-plane directions and the top interface). A large capacitance (C) can be achieved in a very small active volume (V_a). We simulate the capacitance of the modulator through commercially available software (ANSYS HFSS). The simulation gives a gate capacitance of 13 fF, which corresponds to a capacitance over active volume ratio of C/v_a =216 fF/ μm^3.

4.2.5 Fabrication and experiment measurements

The modulator fabrication process starts with a p-type silicon-on-insulator (SOI) wafer with a silicon layer thickness of 250 nm and the buried oxide layer thickness of 3 μm. First, the SOI wafer is uniformly implanted with 34 keV B+ ions at a flux of 2×10^{13} ions cm^{-2} to lightly dope the silicon layer and reduce the resistivity. Then, the silicon waveguide, PC cavity and grating couplers are patterned by diluted ZEP520A resist using electron beam lithography (EBL), followed by a reactive ion etching (RIE) process to etch through the silicon layer. We found that the resonance peak of our fabricated device shifts to shorter wavelength compared with the design value. The dimension of the actual fabricated device is 5% larger than the designed value as listed above. A 10nm thick SiO_2 layer is then formed by thermal oxidation at 1000°C in order to smooth the etching surface (to improve the Q factor) and also activate the dopants. After etching the SiO_2 layer by buffered oxide etchant (BOE), a 10nm thick HfO_2 is deposited using atomic layer deposition (ALD). Next, Al and Au electrode pads are patterned by contact photo lithography, thermal evaporation and lift-off process, contacting with the Si and In_2O_3 layer respectively. Before metal evaporation, the overlapped HfO_2 layer is removed by BOE. The sample is then annealed at 475 °C to form Ohmic contact between Al and Si. Finally, the 20 nm In_2O_3 gate layer is patterned by a second time EBL with ZEP resist followed by room-temperature RF sputtering and lift-off process. Fig 4.10a-4.10c show the scanning electron microscopy (SEM) images of one fabricated device.

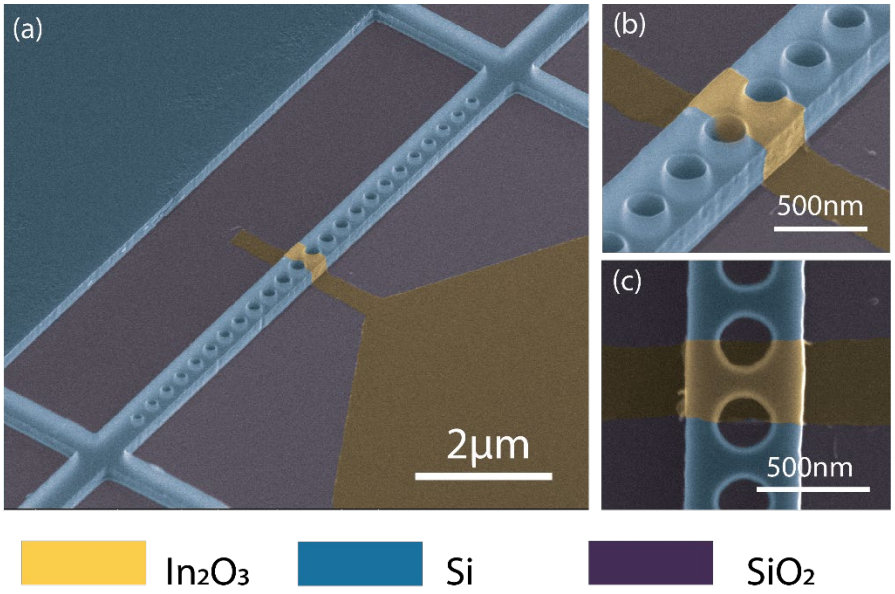

Figure 4.10 (a) Colored SEM of one fabricated Si-In_2O_3 PC nanocavity modulator. (b) Zoomed-in SEM of the MOS structure in the active region of the nanocavity modulator. (a) and (b) are taken with the sample tilted at 45°. (c) Top view SEM of the active region of the nanocavity modulator.

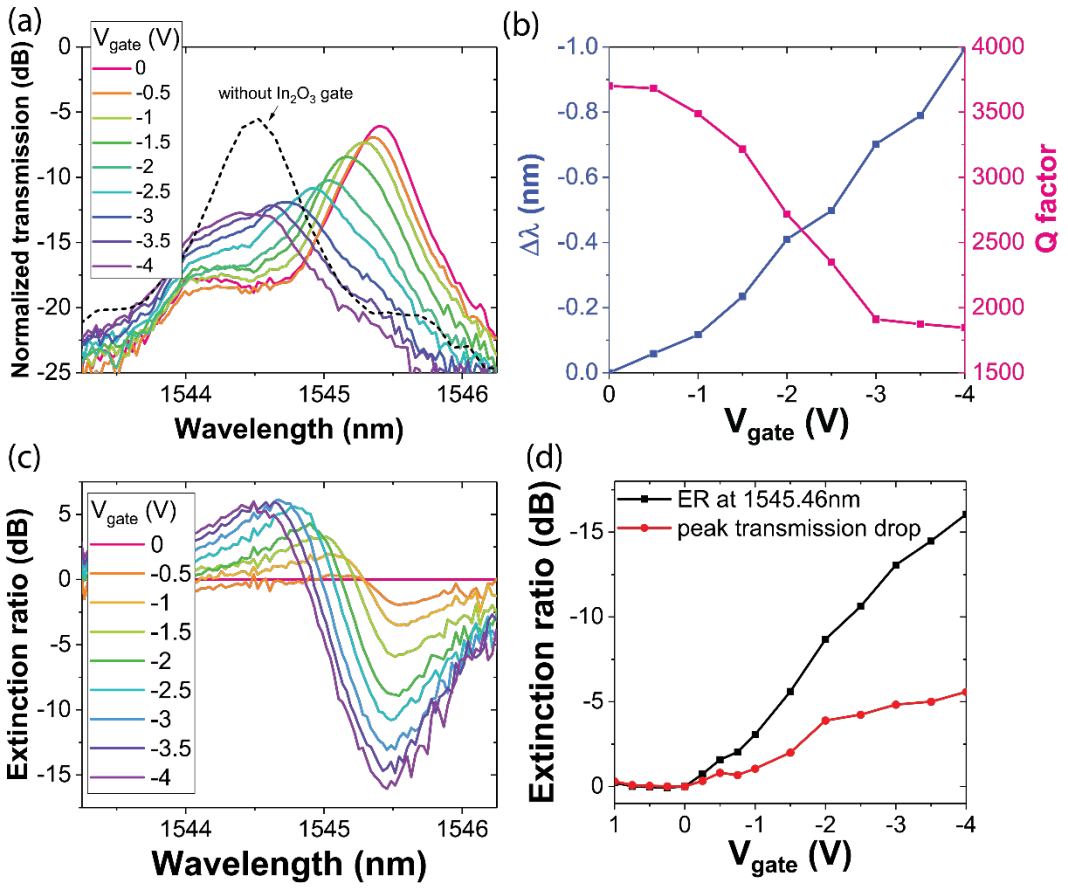

Figure 4.11 (a) Transmission spectra of the nanocavity modulator at different bias voltages (solid lines) and before sputtering the In_2O_3 gate (black dashed line). (b) Peak wavelength shift and Q factor as a function of applied bias. (c) Extinction ratio spectra at different bias voltages. (d) Extinction ratio at maximum efficiency wavelength (1545.46nm) and the peak transmission reduction as a function of the applied voltage.

We perform optical and E-O modulation characterization of the device. Fig 4.11a shows the plots of the transmission spectra at different applied bias voltages. The spectra are normalized to a straight Si waveguide with same crossing strips as the reference. When no bias applied, a transmission peak with a relative high Q factor of 3,700 is observed at 1545.39 nm. The insertion loss at peak wavelength is ~6dB, which is majorly caused by fabrication errors and waveguide surface roughness. Compared with the transmission spectrum before sputtering the In_2O_3 gate (black dashed curve in fig 4.11a), the effect of the In_2O_3 gate on the Q factor is negligible. We should point out that the current moderate Q factor of our device is majorly limited by our fabrication

errors. With optimized process, higher Q factor and lower insertion loss should be achievable [36]. As we apply the bias voltage on the In_2O_3 gate, electrons and holes start to accumulate at the In_2O_3/HfO_2 and Si/HfO_2 interfaces, respectively. The accumulated carriers induce modulation to both the real part and the imaginary part of the optical permittivity, and both contributes to the E-O modulation. The real part variation of the permittivity causes the resonance peak blue shift to shorter wavelength. By increasing the applied voltage from 0 to -4V, the resonant peak blue shifts by 1 nm, which corresponds to resonance tuning of 250 pm/V. It is among one of the largest tuning efficiencies induced by fast carrier effect (depletion and accumulation) ever reported so far. To have an easy comparison with conventional silicon MZI modulator, such tuning efficiency corresponds to an equivalent $V_\pi L$ of 0.18 V·cm. Although higher tuning efficiency can be achieved through heavy carrier injection in PIN diode structures [35], [127], those devices suffer from the high energy consumption and low E-O modulation speed due to the life time of free carriers, which are not suitable for high speed modulators. The Q factor drops to 1,850 due to increased imaginary part of the permittivity as the voltage increases. The shift of the peak wavelength and the degradation of the Q factor are plotted in fig 4.11b. The imaginary part modulation of the optical permittivity, majorly from the In_2O_3 layer, also increases the optical loss and reduces the peak transmission.

Fig 4.11c plots the extinction ratio (ER) spectra as a function of the applied bias. The maximum modulation is observed at 1545.46nm. The ER at this wavelength as a function of the applied voltage is shown in fig 4.11d. The flat band voltage of roughly 0V is observed, which is due to the similar Fermi levels of In_2O_3 and p-type silicon. An ER of 16dB is achieved with a bias changing from 0V to -4V. We also plot the peak transmission versus the applied voltage as shown in Fig 4.11d. With -4V applied voltage, the peak transmission drops by 5.6 dB. Compared with the peak transmission drop, the imaginary part modulation of the optical permittivity roughly contributes to around 1/3 to the total ER. The leakage current of the device at -4V is around 10^{-14} A, which is at the noise level of our measurement equipment. This also means the static power consumption of the MOS capacitor is negligible. The driving voltage for 3dB

ER is reduced to less than 1V, 12 times less than our previous work in section 4.1, which is compatible with CMOS driving circuits. We can estimate the energy consumption of the modulator by ($CV^2/4$) to be 3 fJ/bit. The driving voltage can be further reduced by decreasing the gate oxide layer thickness. For example, by decreasing the HfO_2 thickness to 5 nm, we can double the tuning efficiency to 500 pm/V, while decrease the driving voltage to 0.5V. If we can increase the Q factor to 5000, we can further decrease the driving voltage to 0.37V, achieving an energy efficiency of 0.8 fJ/bit.

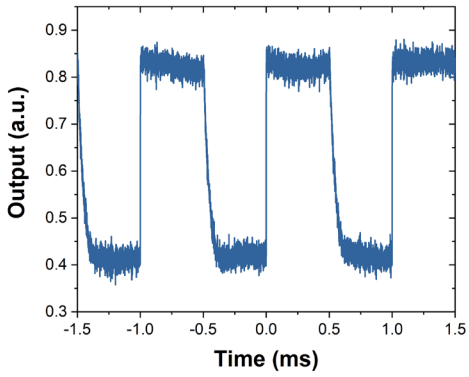

Figure 4.12 AC modulation of the Si-In_2O_3 PC nanocavity modulator

The speed of the photonic crystal nanocavity modulator is only limited by the RC time constant given the moderate Q factor below 5,000. However, the series resistance of the PC nanocavity device is still large, estimated to be a few MΩ, possibly due to the fabrication issue related to the silicon dopant activation and electrical contact. The RC-delay limited bandwidth is estimated to be a few MHz. Fig 4.13 shows the AC measurement of the nanocavity modulator. The rising time of the transmitted optical signal shows a good match with our estimation of ~10^{-7} s. Unfortunately, a large falling time of ~10^{-5}s is observed possibly due to the Schottky contact at the In_2O_3/Au interface. This issue is addressed during our follow-up work. The RF bandwidth can be increased to 2GHz by simply increasing the silicon doping concentration to 5×10^{18} cm^{-3} (based on the resistance calculation in section 4.1.6). According to our 3-D FDTD simulation, such doping concentration won't limit the Q factor up to at least 5,000. The additional insertion loss from increased doping level can be estimated by the passive waveguide

loss (0.017dB/μm for 5×10^{18} cm^{-3} doping concentration) and the photon lifetime of the nanocavity (~4ps for Q factor of 5,000), which equals to only ~1dB.

4.2.6 Summary

In summary, we demonstrate a low-voltage silicon PC nanocavity modulator with an ultra-short In_2O_3 electrical gate of only 350 nm in length, showing a large resonance tuning efficiency of 250 pm/V and an average modulation strength of 4dB/V for a medium Q factor of 3,700. One-volt CMOS compatible driving voltage is required to drive the 13 fF gate to achieve 3dB modulation, which corresponds to an energy efficiency of 3 fJ/bit. The performance of the device can be further improved to less than 0.5V operating voltage and sub-1fJ/bit energy consumption by reducing the gate oxide thickness and improving Q factor, offering the possibility to be directly driven by CMOS logic gates. These combined merits prove the great potential of the TCO-gated silicon nanocavity modulator for future CMOS driven integrated photonic interconnect systems.

4.3 High-speed femto-joule per bit silicon-conductive oxide nanocavity modulator

4.3.1 Introduction

In section 4.2, we show that Si-TCO PC nanocavity modulator, which combines the small mode volume of PC nanocavity and large capacitance density of the MOS capacitor, can achieve extremely large wavelength tunability of 250 pm/V, showing great potential for low-voltage and ultra-energy-efficient E-O modulator application. However, the modulation speed of previous device was limited to a few Mega-Hertz range due to the large series resistance and the lack of high-speed electrode design. In this section, we conducted holistic design of ultra-compact, high-speed PC nanocavity modulator driven by an ITO gate based on silicon rib waveguide and high-speed coplanar electrodes. Experimentally, we achieved a 3-dB bandwidth of 2.2 GHz. In-depth analysis of the energy efficiency and high frequency simulation of the nanocavity

modulator reveals the critical role played by the semiconductor conduction path and the overlapping factor between the accumulated free carriers and the cavity resonant mode. To the best of our knowledge, this is the first systematic analysis of any high-speed TCO photonic devices.

4.3.2 Device design

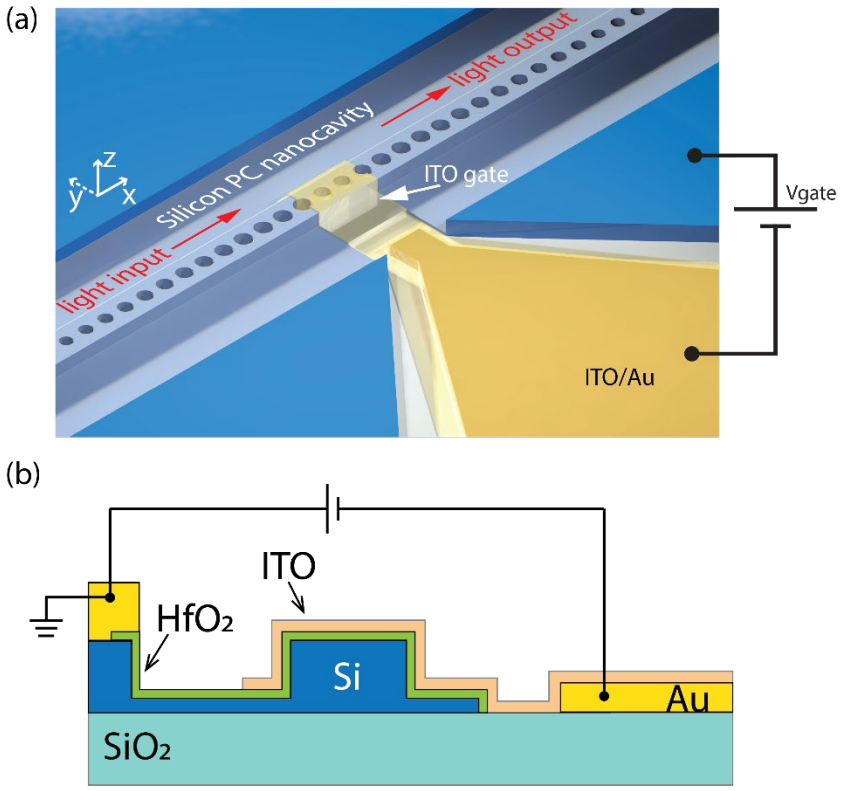

Figure 4.13 (a) 3D schematic of the high speed ITO-gated silicon PC nanocavity modulator. (b) Cross-sectional schematic of the ITO/HfO_2/Si MOS capacitor in the active region. The Si bottom and ITO gate contact pads are drawn on two sides of the waveguide for the ease of illustration.

Fig 4.13a shows the 3D schematic of the high-speed device design using silicon rib waveguide to achieve reduced series resistance in this work. The PC nanocavity consists of two back-to-back PC mirror segments on a silicon rib waveguide with 500 nm width and 250 nm height. The active region of the nanocavity modulator consists of an ITO/HfO_2/Si MOS capacitor. The cross-sectional schematic is shown in fig 4.13b. Here the 50nm thick silicon slab waveguide serves as both the bottom of the MOS

capacitor and electrical conduction path. The PC nanocavity is covered by 16 nm thick HfO_2 gate oxide layer. On top of that is the 20 nm thick ITO gate layer covering the center active region.

4.3.3 Free carrier-optical mode overlapping factor analysis

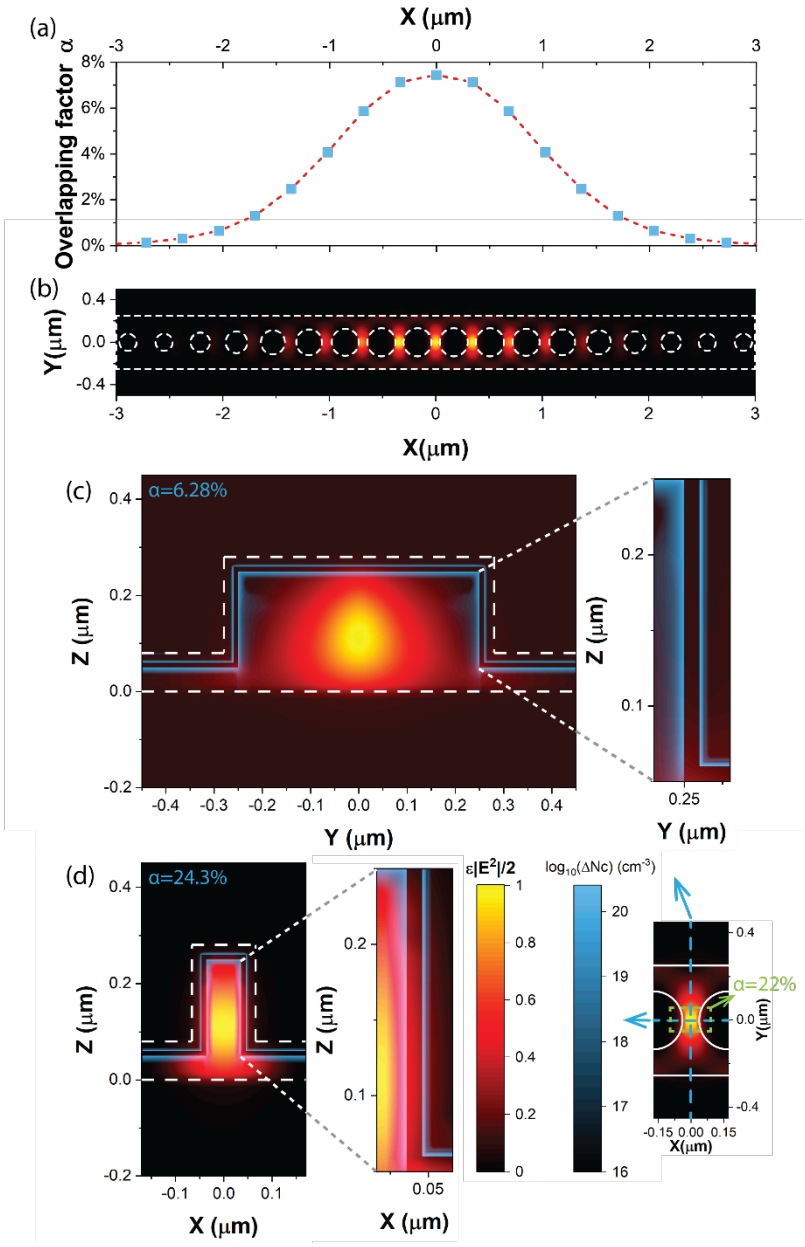

Figure 4.14 (a) Overlapping factor vs. position of the ITO/HfO_2/Si MOS capacitor by assuming the MOS capacitor covering 1 period of the PC nanocavity. (b) Top view of the electrical energy density

distribution of the PC nanocavity. (c) and (d) Cross-sectional view of energy density distribution at (c) X=0 μm and (d) Y=0 μm with overlay of simulated free carrier density accumulation distribution at -2V (blue shadow). Inset: Zoomed-in top view of nanocavity mode profile in the center period. Blue dashed lines label the cross-section positions of (c) and (d). Green dashed box labels the region where the overlapping factor reaches 22%.

When a negative bias is applied to the ITO gate, electrons and holes accumulate at both the ITO/ HfO_2 and Si/ HfO_2 interfaces, respectively. The accumulated free carriers induce blue-shift of the resonance peak, modulating the light transmission. We have developed a general model to describe carrier-driven resonator-based modulator, which will be covered in Chapter 6. The relationship between resonance frequency detuning and accumulated free carriers can be described as (See section 7.3.1 for model details):

$$\frac{\Delta\omega}{\omega} = -\frac{\int \Delta\varepsilon|E|^2\, dv}{2\int \varepsilon|E|^2 dv} = \frac{\alpha K Q_{tot}}{2V_m}. \tag{4.6}$$

Here, E is the electric field distribution of the cavity mode, ε and Δε are the initial and perturbed permittivity distribution. Because the plasma dispersion induced permittivity change is linear to the change of free carrier density, the second term of (4.6) can be rewritten into the third term, where there are four major factors: $K = -\partial(\Delta\varepsilon/\varepsilon)/\partial(\Delta N_c q)$ is the free carrier dispersion coefficient, which equals to the relative permittivity perturbation per unit change of free carrier charge; Q_{tot} is the total change of the accumulated carrier charge; V_m is the optical mode volume of the cavity mode; and α is the overlapping factor that describes the overlapping between the free carrier perturbation and the electrical energy of the cavity mode, which can be expressed as:

$$\alpha = \frac{\int \Delta N_c q\varepsilon|E|^2 dv}{Q_{tot}\, max(\,\varepsilon|E|^2)}. \tag{4.7}$$

In order to maximize the energy efficiency of the modulator, optimizing the overlapping factor α is also equally important. The overlapping factor determines the percentage of the electrically accumulated free carriers that can be used to interact with the light. Fig 4.14b plots the top view of the normalized electrical energy density

($\varepsilon|E|^2/2$) distribution of the PC nanocavity simulated by 3D finite-difference time-domain (FDTD) using Lumerical FDTD, which corresponds to an ultra-compact optical mode volume of 0.058 μm^3 ($0.66(\lambda/n_{Si})^3$). We can estimate the overlapping factor from the electrical energy distribution under the assumption of 1nm thick uniform accumulation layer. Fig 4.14a plots the calculated overlapping factor versus the position of the active TCO-Si MOS capacitor by assuming the MOS capacitor covering one period of the PC nanocavity. Clearly, covering 3 periods of the PC nanocavity can provide a balance between energy efficiency and modulation speed. Fig 4.14c and 4.14d show the cross sectional electrical energy density distributions of the center period of the nanocavity modulator at positions X=0 μm and Y=0 μm, respectively with overlays of accumulated free carrier distribution after applying -2V bias on the ITO gate, which was simulated by Silvaco. We can directly visualize how the accumulated carriers are overlapped with the electrical energy. The overlapping factors of two cross sections are calculated to be 6.28% and 24.3%, respectively. It is very clear that the subwavelength silicon bridge (72 nm wide) between air holes of the PC nanocavity helps to improve the overlapping factor.

4.3.4 *Electrical Design for high speed E-O modulation*

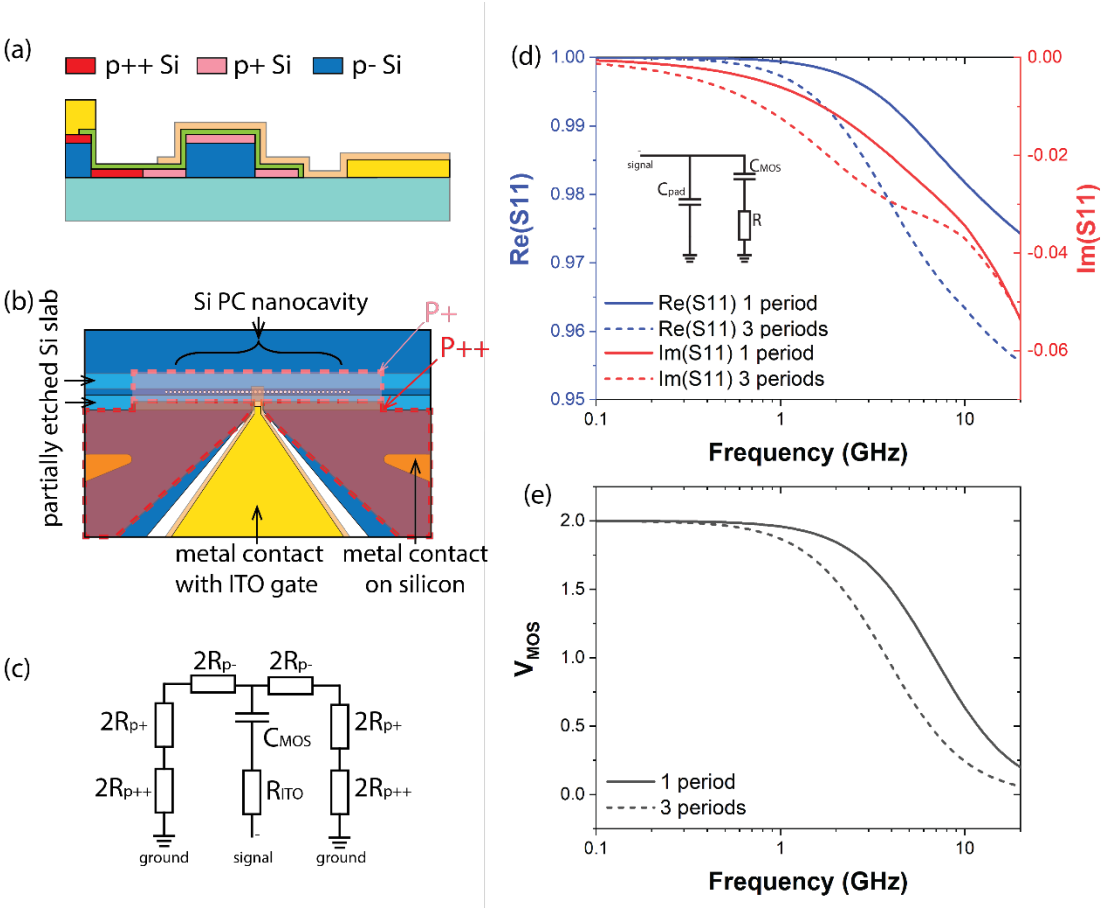

Figure 4.15 (a) Cross-sectional schematic of the silicon doping profile considered in the HFSS simulation. (b) Partial layout of the patterns used for the fabrication of the nanocavity modulator. (c) Equivalent circuit model of the PC nanocavity modulator in the active region. (d) S11 parameters from the HFSS simulation. Inset: circuit model used to fit the S11 parameters. C_{pad} is the parasitic capacitance between the contact pads. (e) Normalized voltage across the MOS capacitor as a function of frequency.

For resonator-based E-O modulators, the modulation speed depends on two factors: the photon lifetime and the resistance-capacitance (RC) time delay constant. The overall 3dB bandwidth can be calculated as $f_{3dB} = 1/\left(1/{f_{opt}}^2 + 1/{f_{RC}}^2\right)^{1/2}$. The photon-lifetime-limited bandwidth can be calculated as $f_{opt} = f/Q$, where f is the resonance frequency and Q is the Q factor of the resonator. For PC nanocavity, the Q factor can be controlled by the air holes in the PC mirror segments [119] and the doping level. In this design, we target a Q factor of 5,000, which won't limit the bandwidth up to 38

GHz at 1.55 μm wavelength. Therefore, the speed of the PC nanocavity modulator is majorly limited by the RC delay. However, a high capacitance density of the MOS capacitor is crucial to reduce the driving voltage and improve the energy efficiency. Thus, it is especially important to reduce the series resistance in order to achieve both high-speed and high energy efficiency. The nanocavity modulator contains semiconductor conduction path through the silicon waveguide and thin ITO gate layer, which contribute to the majority of the series resistance. Thus, we optimized the electrical configuration, and reduced the resistance from both silicon and ITO. First, on the silicon side, the high-resistance silicon strip conduction path is replaced by partially etched silicon slabs. Then, the doping of the silicon conduction path is carefully engineered. Fig 4.15b shows the partial layout used for the fabrication of the nanocavity modulator. The 50nm thick silicon slabs and the top 50nm-thick layer of the silicon waveguide (p+ region) are moderately doped, leaving the bottom 200nm-thick layer of the silicon waveguide lightly doped (p-). The top 50nm-thick layer of the silicon contact area (p++ region) is highly doped and extends to only 500nm away from the silicon waveguide edge. Fig 4.15a illustrates the cross-sectional doping profile in this design. Next, on the ITO side, the length of the TCO conduction path is reduced by patterning the metal contact pad 1 μm away to the nanocavity. In order to quantitatively evaluate the high-speed performance of the PC nanocavity modulator, we performed simulation of the modulator using ANSYS HFSS. The resistance and capacitance parameters are extracted according to the equivalent circuit model shown in Fig 4.15c. In the simulation, the dielectric constant of HfO_2 has been adjusted to match the 8 fF/μm^2 capacitance density of the ITO/16nm HfO_2/Si MOS capacitor simulated by quantum moment model [128]. We simulate both cases for the MOS capacitor covering the centric one and three periods of the PC nanocavity, which correspond to capacitances of 6.1 fF and 18.3 fF, respectively. The silicon series resistance can be divided into contributions from the three different doping regions (p-, p+, p++). Then, the total series resistance R can be expressed as:

$$\begin{aligned} R &= R_{Si} + R_{ITO} = (R_{Si,p-} + R_{Si,p+} + R_{Si,p++}) + R_{ITO} + R_r \\ &= R_{s,p-}A_{p-} + R_{s,p+}A_{p+} + R_{s,p++}A_{p++} + R_{s,ITO}A_{ITO} + R_r \end{aligned} \quad (4.8)$$

Here R_s and A are the sheet resistance and the effective aspect ratio of different regions, and R_r is the remaining resistance that can't fit into the simplified linear resistance model. The effective aspect ratio is fitted by changing the sheet resistance of different regions. Detailed extracted parameters are listed in Table 4.1. In our design, we choose doping concentrations of 1×10^{17} cm^{-3}, 5×10^{18} cm^{-3}, 1×10^{20} cm^{-3} for p-, p+ and p++ regions of silicon, and 2×10^{20} cm^{-3} carrier density for ITO. The corresponding S11 parameters from the HFSS simulation is plotted in Fig 4.15d. It gives us a total series resistance of ~3720 Ω and ~2250 Ω for 1 period and 3 periods coverage of the MOS capacitor, yielding RC-limited bandwidth of 7GHz and 3.9GHz, respectively. Fig 4.15e shows the normalized voltage across the MOS capacitor V_{MOS} as a function of frequency by assuming 1V at the signal input. It equals to 2V at low frequency due to the signal reflection. We have verified the electrical configuration with FDTD simulation that with such doping we can still achieve a Q factor of ~5,000.

Table 4.1 Circuits parameters extracted from HFSS simulation

4.3.5 Fabrication and experiment measurements

The nanocavity modulator is fabricated on a 250 nm thick lightly doped p-type silicon-on-insulator (SOI) substrate. First, the waveguide and PC nanocavity are patterned by electron-beam lithography (EBL), followed by reactive ion etching (RIE) of 200 nm thickness into the silicon, leaving a 50 nm thick Si slab for conduction and PC nanocavity with partially etched air holes. The grating couplers are pattern by a second round of EBL and RIE. Then, the p+ region and p++ region is selectively implanted with 5 keV B+ ions at flux of 2.5×10^{13} cm^{-2} and 6×10^{14} cm^{-2} with tilted angles of 7° and 30°, respectively. After the ion implantation, the dopants are activated by rapid thermal annealing at 1000 °C for 10 seconds. Next, 16nm thick HfO_2 layer is deposited using atomic layer deposition (ALD). After the ALD, the oxide at the silicon contact region is removed by buffered hydrofluoric acid. Ni/Au coplanar ground-signal-ground (GSG) electrode pads are patterned by photolithography, thermal evaporation and lift-

off. Finally, the Au contact pads under the ITO and the ITO gate layer are patterned by EBL and lift-off. 20 nm of ITO gate layer is sputtered at 1% O_2/Ar gas flow, which yields an ITO resistivity of ~1.4×10^{-3} Ω·cm. The fabricated device is shown in Fig 4.16a and 4.16b. The length of the ITO gate is 1 μm, which covers the centric three periods of the PC nanocavity as shown in Fig 4.16c.

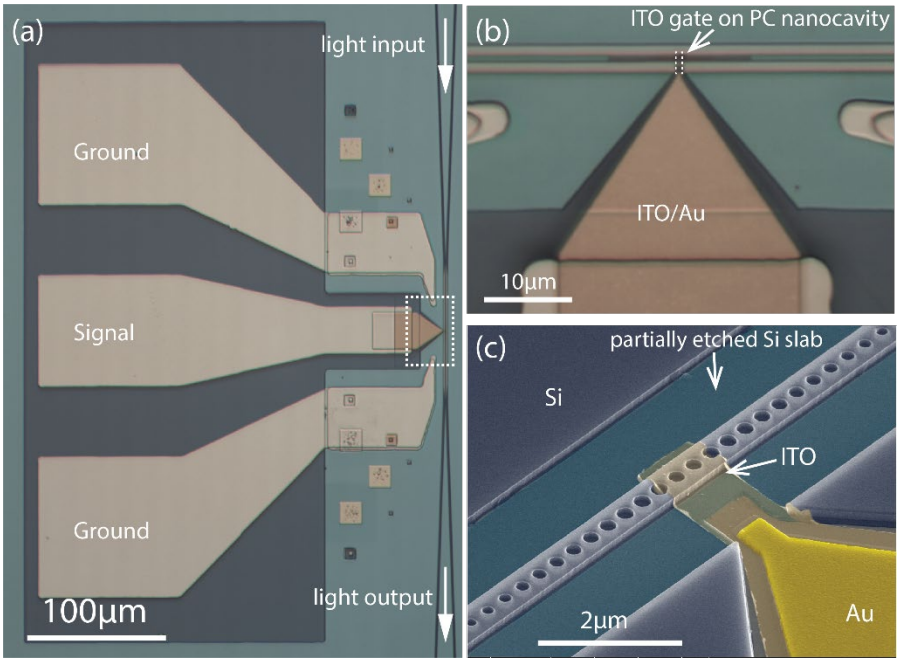

Figure 4.16 (a) Optical image of the fabricated PC nanocavity modulator. (b) Zoomed-in optical image of the nanocavity modulator at the active region (dashed box in (a)). (c) Colored scanning electron micrograph (SEM) of the active region of the modulator.

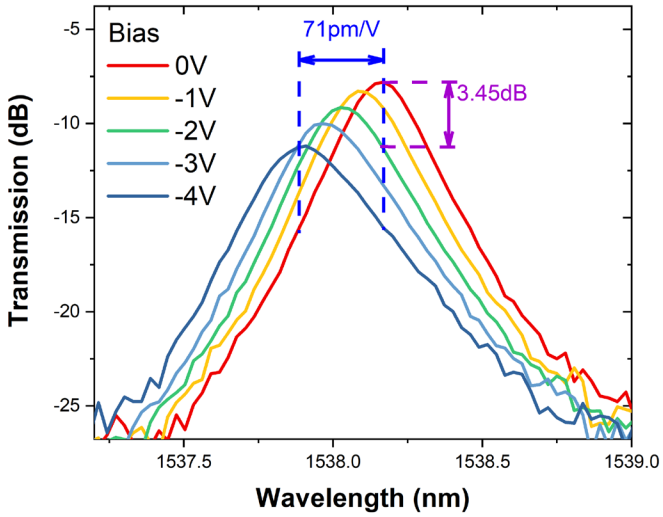

Figure 4.17 Transmission spectra of one fabricated PC nanocavity modulator at different bias voltage.

The fabricated devices are characterized with light input and output via surface grating couplers. A polarization controller is used to excite the transverse electric (TE) mode light. The PC nanocavities are designed to operate at C-band. Fig 4.17 shows the transmission spectra at different bias voltages of a fabricated nanocavity modulator with resonance wavelength at 1538 nm. The plotted transmission is normalized to that of a straight waveguide with the same grating couplers. The device has 22 air holes in each PC mirror segments, which corresponds to a total device length of 14.8 μm. Considering the partially etched silicon slab width of 1.2 μm, the device occupies a compact footprint of only 43 μm^2. The PC nanocavity exhibits a Q factor of 9,460 before doping and ITO gate deposition. After the device fabrication, the Q factor is reduced to ~5,600, which is majorly due to the silicon doping. Insertion loss (IL) of the nanocavity is 7.8 dB, which is primarily limited by the fabrication imperfection of EBL and RIE process. With better control of fabrication processes, the IL can potentially be reduced to less than 0.5 dB [36]. With -4 V applied bias, the peak resonance wavelength shifts 284 pm, corresponding to a wavelength tunability of 71 pm/V. At -2 V bias, a peak extinction ratio (ER) of 3.45 dB can be reached. The wavelength tunability is less than the previous section due to two reasons. First, the HfO_2 gate oxide layer is thicker than the previous case, which results in smaller capacitance density of the MOS capacitor. Second, limited by the alignment accuracy

of our EBL instrument, we have to pattern and etch the air holes and silicon slabs in the same step of fabrication process. This leads to under etching of air holes due to the local loading effect of the RIE [129]. As a result, the real overlapping factor is smaller than the previous ideal estimation, since more optical field is contained inside the silicon waveguide slab. The overlapping factor can be estimated as

$$\alpha = \frac{\Delta\lambda}{V}\frac{V_m}{\lambda \cdot K \cdot C}, \tag{4.9}$$

where $\Delta\lambda/V$ is the wavelength tunability, λ is the resonance wavelength, and C is the capacitance. The average free carrier dispersion coefficient can be estimated, as $(K_{p\text{-}Si}+K_{ITO})/2$, to be ~$8.1\times10^{-3}$ C·cm^3 (See section 7.2 for calculation details). Then, we can calculate the actual overlapping factor to be 1.79%. As a comparison, our previous demonstration achieved a wavelength tunability of 250 pm/V with 1 period coverage of the MOS capacitor and an overlapping factor of 7.43%, which is very close to the overlapping estimation in the previous section. Therefore, optimizing the fabrication processes to achieve a similar overlapping factor for high speed E-O modulators is still necessary for future research.

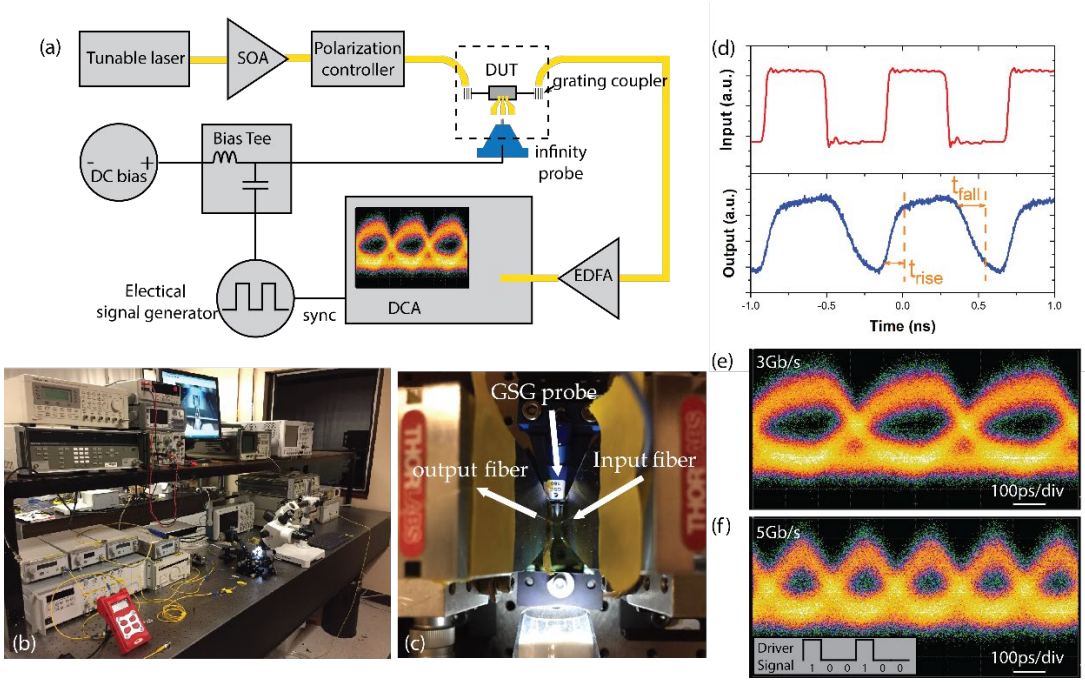

Figure 4.18 (a) Schematic of the AC testing setup. (b) Photo of the testing lab. (c) Photo of the PC nanocavity modulator chip under testing. Light is coupled in and out through optical fibers. The AC signal is applied on the device through the GSG probe. (b) Electrical input and optical output AC modulation signal at 1.25 GHz with 2 V_{pp} voltage swing. (c) and (d) Digital modulation signals at 3 Gb/s and 5 Gb/s, respectively.

The high-speed response of the nanocavity modulator is measured using the setup shown in Fig 4.18a-4.18c. The AC signal is generated by Anritsu MP1763B and combined with a DC bias through a bias tee before applying to the device through a high-speed probe (Infinity Probe). The output optical signal is measured by a digital communications analyzer (Agilent 86100A). Fig 4.18d plots the AC E-O modulation at 1.25 GHz with 2 V_{pp} rectangular voltage swing. The rising and falling time of the optical response are measured to be ~0.135 ns and ~0.18 ns, respectively, which corresponds to a 3-dB bandwidth of 2.2 GHz. The asymmetric waveform is due to the dynamics of resonator based modulator [7]. Assuming the capacitance of 18.3 fF from the previous simulation, we can calculate the series resistance of the nanocavity modulator by $R = f/(2\pi C)$, to be ~3.9 kΩ. The ITO conduction path contributes ~0.6 kΩ to the series resistance, which can be calculated from the ITO sheet resistance. Then, ~3.3 kΩ comes from the silicon conduction path, which also matches the estimation

from the resistance between the two ground electrode pads. Overall, the experiment result matches well with the HFSS simulation. Besides, the sheet resistance of the p++ region on the device chip is measured to be ~1100 Ω/□, which indicates that the larger resistance from the silicon conduction path may be due to inaccurate implantation conditions or partial activation of the dopants, and the induced large contact resistance. Finally, we measured the high-speed digital modulation of the nanocavity modulator up to 5 Gbps. Fig 4.18e and 4.18f show the measured signals at 3 Gbps and 5 Gbps data rate. The asymmetric shape of the signal is due to the input driven signal we used for the measurement, as is shown in the inset of Fig 4.18f.

4.3.6 Towards higher modulation bandwidth and atto-joule per bit energy efficiency

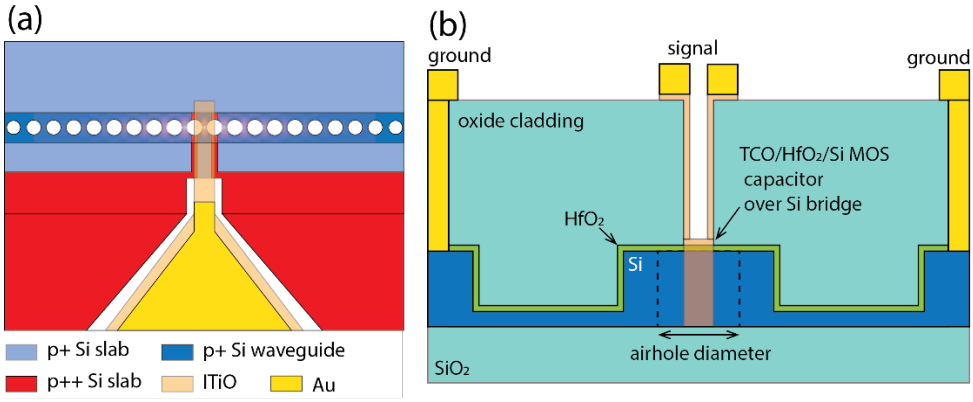

Figure 4.19 (a) Layout schematic of node-matched doping profile with overlay of the electrical energy density distribution. (b) Cross-sectional schematic for building Si-TCO MOS capacitor over the subwavelength Si bridge through making window on the top cladding layer.

We have proved the capability of the gigahertz operation of the Si-TCO PC nanocavity modulator, which matches the prediction of our design and simulation. Here, we discuss how we can further improve the modulation speed of the Si-TCO PC nanocavity modulator. Basically, the series resistance from both the silicon and ITO need to be reduced. On the silicon side, the series resistance can be further reduced using node-matched doping technique [35]. Such method allows us to put the p++

doping region closer to the active cavity region without significantly affecting the optical mode as is illustrated in Fig 4.19 a. FDTD simulation also gives us a Q factor larger than 5,000. On the gate side, by replacing ITO (μ=20 $cm^2/(Vs)$) with high mobility TCO materials such as Ti-doped In_2O_3 (μ>80 $cm^2/(Vs)$) [130], the TCO series resistance can be reduced by more than 4×. In the meantime, larger mobility also induces less plasma absorption. We simulated the resistance of the proposed structure. It yields a total series resistance of less than 852 Ω, which leads to a RC bandwidth of 30 GHz for 1 period coverage of MOS capacitor. The overall 3dB bandwidth reaches over 23.5 GHz. Such optimized nanocavity modulator can be modulated at 25 Gbps using simple OOK for on-chip optical interconnects.

The energy consumption of this PC nanocavity modulator can be calculated as $CV^2/4$, to be 18.3 fJ/bit by assuming 2 V_{pp}. However, we anticipate that larger wavelength tunability, smaller driving voltage, and higher energy efficiency can be achieved. For example, 285 pm/V wavelength tunability should be achievable by increasing the overlapping factor from 1.79% to 7.2%. Based on the Q factor and capacitance of current device, the driving voltage can be reduced to 0.5 V, leading to energy consumption of 1.14 fJ/bit. Furthermore, as discussed in section 4.3.3, the subwavelength silicon bridge between air holes exhibits much larger overlapping factor than the overall PC nanocavity. By principle, we can build the active TCO-Si MOS capacitor only at the subwavelength bridge region, for example, through making window on top of the cladding layer as shown in Fig 4.19b. Assuming we can increase the overlapping factor from 7.2% to ~22%, which corresponds to 100 nm long region of the silicon subwavelength bridges (green dashed box in inset of Fig 4.14d), we can further reduce the required capacitance by nearly 3× to 6 fF, while not sacrificing the wavelength tunability. In that case, the energy consumption can potentially be reduced to 375 aJ/bit.

4.3.7 Summary

In summary, we presented comprehensive design and in-depth analysis of an ultra-compact, high-speed Si-TCO PC nanocavity modulator based on ITO/HfO_2/Si MOS

capacitor. We quantitatively analyzed the overlapping factor between the accumulated free carriers and the cavity resonant mode. Its contribution to the energy efficiency of the modulator is sufficiently discussed. The relationship between the doping of semiconductor conduction path and modulation speed was systematically investigated via high frequency simulation. In our experimental demonstration, the fabricated Si-TCO nanocavity modulator shows a wavelength tunability of 71 pm/V with a Q factor of ~5,600, achieving 3.45 dB ER with 2 V_{pp} applied bias. We demonstrated a 3dB modulation bandwidth of 2.2 GHz. E-O modulation was measured up to 5 Gb/s with 2 V_{pp} voltage swing, which corresponds to an energy efficiency of ~18.3 fJ/bit. Besides, we proposed that the series resistance can be further reduced by node-matched doping of Si and high-mobility TCO material, which can improve the 3dB bandwidth to over 23.5 GHz. Furthermore, based on the quantitative analysis of the overlapping factor, we predict that single-digit femto-joule per bit energy efficiency of 1.14 fJ/bit can be reached through optimizing the gate oxide thickness and fabrication processes. Further increasing the overlapping factor is possible through precisely covering the TCO-Si MOS capacitor at the subwavelength silicon bridge of PC nanocavity. With that, an extremely low energy consumption of 375 aJ/bit can be achieved. As the first systematic analysis and experimental demonstration of high-speed Si-TCO resonator-based modulator, this work directly proves the potential of TCO-gated silicon photonic devices for high density, high-speed, ultra-low energy optical interconnect systems.

4.4 Summary

Table 4.2 Summary of Si-TCO PC nanocavity modulators' performance reported in Chapter 4.

	Device reported in section 4.1 [33]	Device reported in section 4.2 [34]	Device reported in section 4.3 [131]	Design proposed in section 4.3.7
Bottom electrical connection	Si contact strip	Si contact strip	Partially etched Si slab	Partially etched Si slab with node-matched doping
Gate oxide	20nm SiO_2	10nm HfO_2	16nm HfO_2	16nm HfO_2
TCO gate	ITO	In_2O_3	ITO	Ti-doped In_2O_3

Q factor	1,000	3,700	5,600	5,600
Insertion loss	0.5 dB	6 dB	7.8 dB	1 dB
Tuning efficiency	30 pm/V	250 pm/V	71 pm/V	285 pm/V
Driving voltage	12 V	1 V	2 V	0.5 V
MOS capacitance	1.28 fF	13 fF	18.3 fF	6 fF
Energy efficiency	46 fJ/bit	3 fJ/bit	18.3 fJ/bit	375 aJ/bit
Bandwidth	3.2 MHz	\	2.2 GHz	23.5 GHz

In summary, we present our development of the Si-TCO PC nanocavity modulators in this chapter. The performance of devices reported in this chapter is summarized in table 4.2.

In section 4.1, we design and demonstrate a Si-ITO PC nanocavity modulator driven by an ITO/SiO_2/Si MOS capacitor. By taking advantage of small mode volume of the PC nanocavity and large capacitance density of MOS, we can achieve large E-O modulation with an ultra-small modulation volume of ~0.02 λ^3. Experimentally, we demonstrated a wavelength tuning of 30 pm/V with a moderate Q-factor of 1000, which corresponds to 3dB driving voltage of 12V and energy efficiency of 46 fJ/bit.

In section 4.2, we show that the capacitance density of the MOS capacitor can be significantly enhanced by using high-k dielectric material, HfO_2, as gate insulator. Therefore, we can enhance the E-O tuning efficiency of the Si-TCO PC nanocavity modulator, achieving a low-voltage operation. Experimentally, we demonstrated an unprecedented large wavelength tuning of 250 pm/V. Together with an improved Q factor of 3,700, we achieved an average modulation strength of 4dB/V, and CMOS compatible 1V 3dB driving voltage and 3 fJ/bit corresponding energy efficiency.

In section 4.3, we performed systematical investigation on the relationship between the semiconductor conduction path and the modulation speed of the Si-TCO PC nanocavity modulator. The series resistance of the device is greatly reduced by using silicon rib

waveguide and carefully designed silicon doping profile and high-speed coplanar electrodes. Experimentally, we achieved a high-speed Si-TCO PC nanocavity modulator with 3dB bandwidth of 2.2 GHz. Digital modulation using on-off-key (OOK) was measured up to 5 Gb/s with only 2 V voltage swing, which corresponds to an energy efficiency of 18.3 fJ/bit. Besides, we proposed a new method using node-matched doping and high-mobility TCO gate material, which can extend the modulation bandwidth to 23.5 GHz. Based on the quantitative analysis of the overlapping factor, we proposed a strategy to further improve the energy efficiency to hundreds of atto-joule per bit level.

Chapter 5. TCO-gated Silicon Microring Resonator

In Chapter 4, we introduce our work on the TCO gated silicon PC nanocavity modulators. We have proved that TCO material, combining optical transparency and high electrical conductivity, can be perfect gate material for heterogeneous integration with silicon micro-resonators. In this chapter, we report our work on integrating the TCO/oxide/Si MOS capacitor with silicon microring resonators. In section 5.1, we present our experimental demonstration of TCO-gated silicon microring with extreme resonance wavelength tunability using HfO_2 as gate insulator. In section 5.2, we introduce the design principle of utilizing the large wavelength tunability of TCO-gated microring to overcome the speed limit of the conventional silicon microring, followed by the proof-of-concept experimental demonstration. In section 5.3, we summarize this chapter.

5.1 TCO-gated silicon microring filter with extreme resonance wavelength tunability

5.1.1 Introduction

Microring resonators play a pivotal role in the success of silicon photonics as silicon enables microring resonators of an unprecedented small size. Various silicon photonic devices such as add-drop filters, tunable filters, electro-optic (E-O) modulators, optical

delay lines, biosensors [132], compact WDM/DWDM systems [133] and on-chip optical I/O [41] have been developed. Silicon microring resonators as active devices have to rely on the relatively weak plasma dispersion effect to induce resonance wavelength tuning or E-O modulation, which are majorly achieved using reversed PN junctions[7], [17], [22]–[25], [28], [134]. Such silicon photonic microring resonators usually possess E-O tuning efficiencies of 10-40 pm/V, which is suitable for high-speed E-O modulation. However, the resonance wavelength λ of silicon microring depends on process variations and temperature fluctuations that requires in-situ tuning and closed-loop compensations, which cannot be sufficiently compensated by the reversed PN junction structure and is usually achieved by free carrier injection using PIN diode structure [135] or by thermal heaters [25], [136], [137]. Free carrier injection and thermal tuning can induce much larger resonance wavelength tuning exceeding 100pm/V or >120 pm/mW; nevertheless, the high-power dissipation at the steady state limits the application, especially for large scale parallel optical links where hundreds and even thousands of microrings are needed.

In this section, we designed and experimentally demonstrated a MOS-structured silicon microring filter with ITO gate as the electric-tuning electrode. It achieved an ultra-large resonance wavelength tunability of 271pm/V, which is obtained through the reduced width (300 nm) of the ring waveguide and the 16 nm thick high dielectric constant HfO_2 insulator. We demonstrated a broad resonance wavelength tuning range over 2nm with ultra-fast response time less than 12 ns and near-zero static power consumption, which can potentially replace traditional thermal tuning for many on-chip optical interconnect applications.

5.1.2 Design and principle

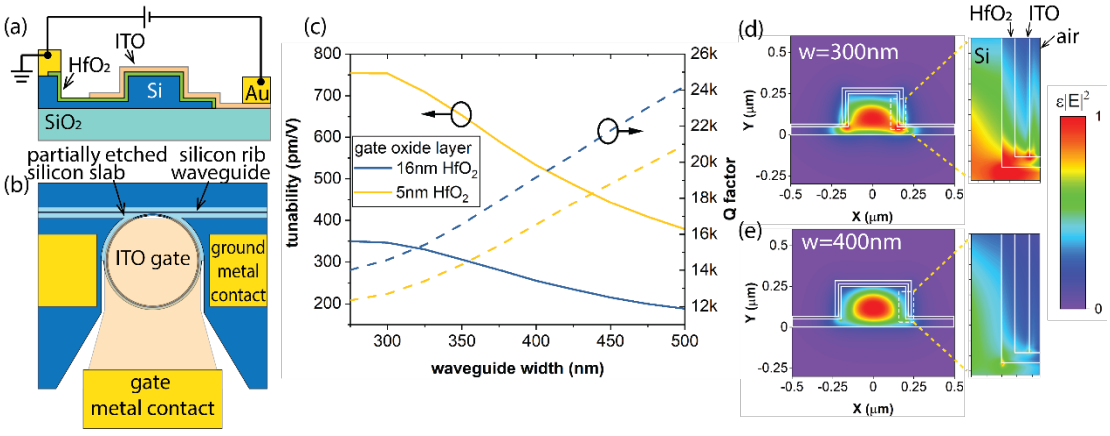

Figure 5.1 (a) Cross sectional and (b) top view schematic of the hybrid TCO-silicon microring tunable filter. (c) Simulated tunability (solid lines) and Q-factor (dashed lines) of the microring tunable filters as a function of the waveguide. Two different thickness of gate oxide layers are simulated (16 nm HfO_2 and 5 nm HfO_2). (d) and (e) Simulated cross sectional electrical energy ($\varepsilon|E|^2$) distribution of the microring filter with different waveguide width, 300 nm and 400 nm, respectively. Zoomed-in view of the distributions at the interface region (white dashed box) are plotted on the right.

The tunable filter is driven by a hybrid TCO-silicon MOS capacitor operating in carrier accumulation mode. As illustrated in Fig 5.1a and 5.1b, a 250 nm thick p-type silicon rib waveguide serves as the bottom electrode of the MOS capacitor, and a 50-nm-thick slab is used for electrical connections. The silicon microring is covered by HfO_2 as the gate oxide layer. On top of the gate oxide layer, 20 nm thick ITO layer performs as the top gate electrode. Because the entire microring is metal-free, we can build a high Q-factor microring resonator. By applying a negative bias on the ITO gate, electrons and holes accumulate at the ITO/HfO_2 and silicon/HfO_2 interfaces, respectively. The plasma dispersion of the accumulated carriers in both ITO and silicon decreases the refractive indices, causing blue shift of the resonance peaks. The plasma dispersion of semiconductor follows the Drude model. The change of permittivity $\Delta\varepsilon_r$ is proportional to the change of carrier density ΔN_c (See section 7.2 for details). Then, according to the perturbation theory, we can have the resonance shift proportional to the total carriers accumulated per unit volume of the microring (See section 7.3.1 for details). Two main factors determine the tunability of a microring tunable filter: the capacitance density of

the capacitor and the overlapping of the modulated carriers with the optical mode. First, electrically, the larger the capacitance density, the more carrier density perturbation can be induced with certain voltage, and thus larger tunability. A MOS capacitor offers additional freedom to control the capacitance density by controlling the thickness and dielectric constant of the gate oxide layer. Using thin high-k material such as HfO_2 as the gate insulator layer, much larger capacitance density can be achieved compared with conventional reversed biased Si PN junction. In section 4.2, we have shown that the large capacitance density of TCO/HfO_2/Si MOS capacitor can enable extreme large wavelength tuning of the Si-TCO PC nanocavity. Besides, unlike carrier-injection-based PIN diode, in which large carrier perturbation can also be achieved through heavy carrier injection, requiring large holding power consumption due to the forward bias, the power consumption of a MOS capacitor is almost negligible. Second, optically, an efficient tuning of the microring requires good overlapping of the accumulated carriers with the optical mode. For the hybrid TCO-silicon MOS capacitor configuration, the carrier accumulation only happens at the ITO/oxide and silicon/oxide interfaces, which are away from the center of the optical mode. In order to improve the overlapping, a narrower waveguide is preferred. We simulated the tunability of the microring with radius of 12 μm as a function of the waveguide width using the Lumerical MODE software, which is based on finite-element method (FEM). The carrier density distribution in the accumulation layer is simulated by Silvaco and imported into Lumerical MODE. The result is plotted in fig 5.1c. The tunability is calculated as $\Delta\lambda = \left(\Delta n_{eff}/n_{eff}\right)\lambda_{res}$, here n_{eff} is the effective index of the guided mode of the bent waveguide and λ_{res} is the resonance wavelength. Clearly, the tunability increases as we decrease the waveguide width. Fig 5.1d and 5.1e plot the simulated cross sectional electrical energy distribution ($\varepsilon|E|^2$) of microrings with waveguide width of 300 nm and 400 nm, respectively. The zoomed-in distributions of the interface region (white dashed box) are plotted on the right. We can see that for narrower waveguide, the electrical energy at the interfaces is much larger. For the case of 16 nm HfO_2 as the gate oxide layer, the tunability of micro-ring increases from 255 pm/V for 400 nm wide waveguide to 346 pm/V for 300 nm wide waveguide due to better overlapping. Moreover, the tunability can be further improved by reducing the gate

oxide thickness, which is inversely proportional to the capacitance density. For example, the tunability of 300 nm wide waveguide increases to 753 pm/V for 5nm HfO_2 layer thickness. Fig 5.1c also plots the Q-factor of the simulated micro-ring, which is calculated as $Q = \pi n_g L\sqrt{ra}/[\lambda_{res}(1-ra)]$ [132]. Here n_g is the group index, L is micro-ring circumference, a is the single-pass amplitude transmission which can be calculated from the waveguide loss (bending loss and free carrier dispersion loss), and r is the self-coupling coefficient (assuming critical coupling condition r=a). For 300nm width waveguide with 5nm HfO_2 gate oxide layer, a high Q-factor of ~12k is achievable. In simulation, the Q-factor of the micro-ring is majorly limited by the free carrier dispersion loss. The doping level of p-Si and ITO used in the simulation is 1×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, respectively.

5.1.3 Fabrication and experiment measurements

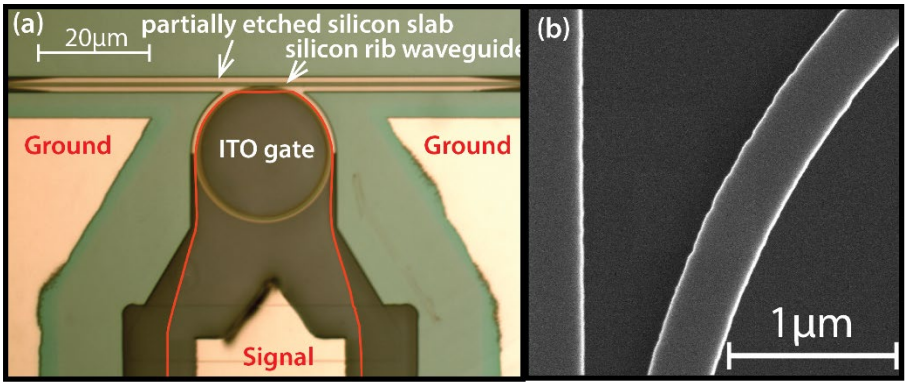

Figure 5.2 (a) Optical image of a fabricated microring tunable filter with radius of 12 μm. The ITO gate (high-lighted by the red line) covers the majority of the microring except the coupling region. The ground electrodes are connected to the silicon ring through partially etched silicon slab. (b) Scanning electron micrograph (SEM) of part of the fabricated silicon microring, showing side wall roughness after RIE process.

The device is fabricated on a 250nm thick silicon-on-insulator (SOI) substrate with p-type background doping of 1×10^{17} cm^{-3}. First, the waveguide, microring, and grating couplers are patterned by two steps of electron-beam lithography (EBL) and reactive

ion etching (RIE). The microrings have a radius of 12 µm. Then, the contact region is highly doped by implantation with 5keV B^+ ions at flux of 6×10^{14} cm^{-2}, which corresponds to equivalent dopant concentrations of 1×10^{20} cm^{-3} at the top 50nm thick silicon layer. After the ion implantation, the dopant is activated by rapid thermal annealing (RTA) at 1000 °C for 10 seconds. Next, 16 nm thick HfO_2 layer is deposited using atomic layer deposition (ALD). After that, the ITO gate layer is pattern by EBL. 20nm of ITO is RF sputtered under O_2/Ar mix gas flow with 2% O_2, followed by the liftoff process. Then, the gate oxide at the silicon contact region is removed by Buffered Hydrofluoric acid. After that, Ni/Au electrode is evaporated and patterned by photolithography to form Ohmic contact with both p-type silicon and ITO. Finally, the sample is annealed at 275 °C for 10 minutes. The fabricated device is shown in fig 5.2.

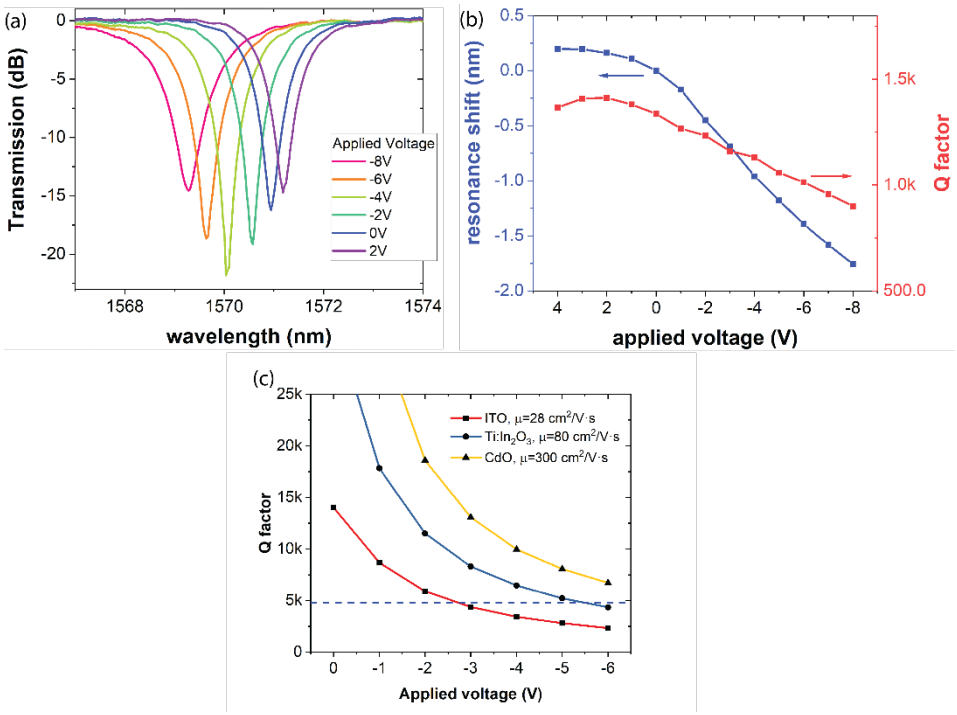

Figure 5.3 (a) Measured transmission spectra of a microring tunable filter under different applied gate bias. The microring has a waveguide width of 300 nm and HfO_2 gate oxide layer thickness of 16 nm. (b) Resonance shift (blue line, left axis) and Q factor (red line, right axis) of the microring filter as a function of applied gate bias. (c) Simulated Q factor of 300 nm waveguide width microring with 16 nm HfO_2 gate oxide as a function of applied bias for different TCO gate material.

Light is coupled into and out of the silicon waveguide through the grating couplers from optical fibers. The fibers are mounted with 10° tilted angle. A polarization controller is used at the input side to excite the TE mode. The output light is measured by an optical spectrum analyzer. A DC bias voltage is applied across the silicon waveguide and ITO gate. Fig 5.3a shows the transmission spectra of the 12μm radius microring tunable filter with 300 nm waveguide at different bias voltages. The resonance shift as a function of the applied bias is shown in fig 5.3b (left axis). The microring filter exhibits almost linear resonance tuning for negative applied bias due to the carrier accumulation. At positive bias, the tunability is smaller due to the depletion operation. At negative bias, an average tuning efficiency of 216 pm/V is achieved. The largest tunability is measured from -2V to -4V, reaching 271.6 pm/V, which is the largest experimental tuning efficiency to the best of our knowledge. The value is less than the simulation results, which may be caused by the deviation of the dielectric constant of the ALD HfO_2 layer from the ideal value used in simulation. At large negative bias beyond -4V, the tunability slightly decreases. We speculate that the large electrical field may force the accumulated electrons at the ITO interface into the HfO_2 layer, forming trapped charges which effectively reduce the free carrier dispersion effect. However, the mechanism is still subject to further investigation. The tuning range of the tunable filter is determined by the dielectric strength of the gate oxide layer. In our testing, the 16nm thick HfO_2 layer breaks down slightly over -8V bias (fig 5.5). This corresponds to a total tuning rang of more than 2nm of the resonance wavelength. The thermal-optical coefficient of silicon is around 1.8×10^{-4} K^{-1} at 1.55 μm, which corresponds to a thermal tuning efficiency of ~0.1nm/K. The tuning range of our microring filter can compensate thermally induced wavelength shifting of around 20K.

Fig 5.3b also plots the Q factor of the microring as a function of the applied bias. A relatively low Q factor of ~1,300 is measured at 0V bias due to two reasons. First, the rough side wall induces significant the optical scattering loss as shown in Fig 5.2b, which is limited by our EBL and dry etching processes. The narrower waveguide design also makes our microring resonator more vulnerable to the surface roughness.

This issue can be resolved in the future using commercial silicon photonics foundry to obtain high quality, loss optical passive devices. Second, the gap width between the bus waveguide and microring is not optimized. The current gap width of 150 nm is too small, which increases the coupling loss of the microring resonator, also limiting the Q-factor, as is indicated by the critical coupling condition near -4V bias (fig 5.3a). This coupling issue can be resolved straightforwardly by increasing the gap width. Besides, we also observed that as the negative bias increases, the Q-factor gradually decreases since refractive modulation by plasma dispersion effect is always accompanied by the free carrier absorption. To evaluate how the free carrier absorption will affect the Q-factor in the biased condition, we simulated the Q-factor of microring with 300 nm waveguide width and 16nm HfO_2 gate oxide as a function of applied bias in fig 5.3c. It shows that the Q-factor is significantly reduced. However, it is still possible to maintain a reasonable Q factor above 5,000 for at least 1nm wavelength tuning range. To further increasing the wavelength tuning range, we can replace the ITO gate layer with high mobility TCO materials such as Ti-dopoed In_2O_3 [130] and CdO [107]. High mobility TCOs induce much smaller free carrier loss and can help to main a high Q-factor across the whole wavelength tuning range, as is shown in fig 5.3c.

We measure the AC modulation response of the microring filter. Because carrier accumulation is a fast process. The speed of the microring is only limited by the resistance-capacitance (RC) delay. Fig 5.4a and 5.4b show the AC response of our tunable filter at 20 kHz. Over 20dB modulation depth is measured. Fig 5.4c and 5.4d plot the rising and falling edge of fig 5.4b, respectively. The rising and falling time is ~12ns, which is much faster than traditional thermal tuning.

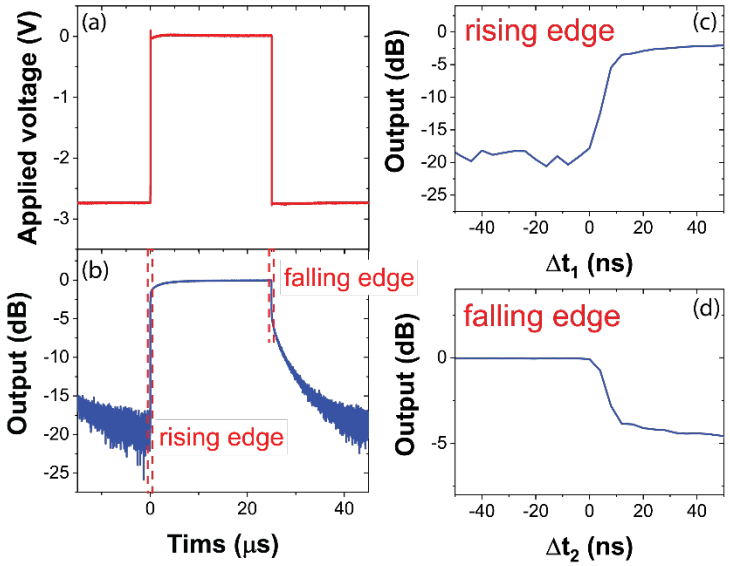

Figure 5.4 (a) 0V~-3V voltage swing applied on the microring tunable filter. (b) Output response of the microring filter. (c) and (d) Rising and falling edge of output in (b).

5.1.4 Negligible energy consumption and potential applications

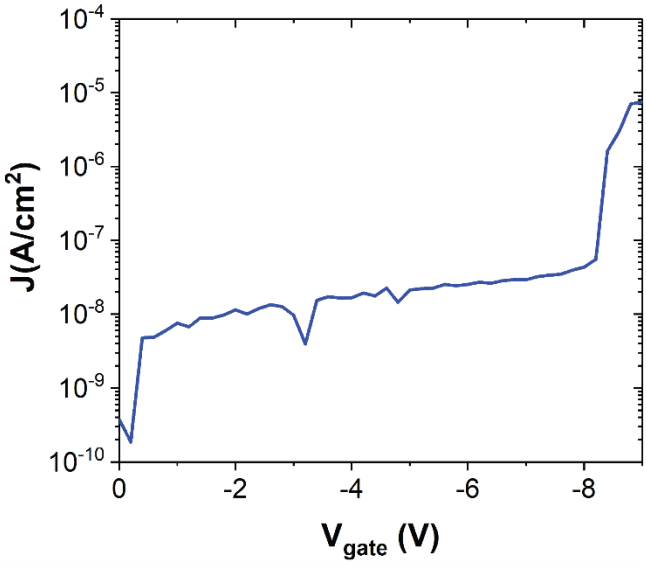

Figure 5.5 Leakage current density as a function of the applied voltage of a testing Si/HfO_2/Au MOS capacitor with 16nm thick HfO_2 gate oxide layer.

The static power consumption of the TCO-gated Si microring tunable filter is only determined by the leakage current, which is below the noise level of our measurement tool (10^{-14}A). Fig 4 shows the leakage current density as a function of the gate voltage in a testing Si/HfO_2/Au MOS capacitor with large area and the same 16 nm HfO_2 gate oxide layer. The capacitor exhibits a leakage current density of 3×10^{-8} A/cm^2 at -8V bias. Then, we can calculate the leakage current of the tunable microring filter to be ~20 fA at -8V bias, which indicate near-zero (0.16pW) static power consumption.

For microring resonators fabricated by CMOS process, the resonance wavelength is strongly affected by the manufacturing variations, such variations in waveguide width, silicon thickness, and etching depth [138]. It is reported that the wavelength variation can be up to over 10nm for resonators with same design parameters and spaced 20 mm apart on a single wafer [139]. Admittedly, the 2 nm wavelength tuning range of the TCO-gated Si microring is still less the conventional thermal tuning, which can tune the resonance wavelength across the entire free spectral range (FSR). For example, a 10-μm-radius silicon microring modulator has a FSR of 6.6 nm [38]. Therefore, the TCO-gated Si microring may not be suitable for those scenarios requiring FSR tunability. However, there are applications where microring resonators are used as microring arrays with equal wavelength spacing, such as microring-based wavelength-division multiplexing/demultiplexing (WDM/DWDM) systems. In those cases, full FSR tunability is not necessary. The wavelength tuning requirement is typically the channel spacing $\delta\lambda$=FSR/N, where N is the number of wavelength channels. In addition, the chip-scale manufacturing nonuniformities are generally smaller. In ref [140], the authors reported that the average tuning requirement is only 1.2nm for an 8-channel microring mux/demux with channel spacing of 1.6nm, which can be completely covered by the electrical tuning of the TCO-gated Si microring. Therefore, we can potentially replace the conventional thermal tuning in those applications with our TCO-gated Si microring, which achieving negligible energy consumption.

5.1.5 Summary

In summary, we designed and fabricated a silicon microring resonator gated by an ITO electrode. Benefited from the large capacitance density and the narrow microring waveguide, it achieved ultra-large resonance wavelength tunability of 216~271pm/V. We demonstrated a broad resonance wavelength tuning range over 2 nm with ultra-fast response time less than 12 ns and near-zero static power consumption. The TCO-gated tunable microring filters can replace conventional thermal tuning for on-chip microring WDM/DWDM optical interconnects.

5.2 TCO-gated silicon microring modulator (MRM)

5.2.1 Introduction

The performance of pure silicon-based MRM is limited by the weak plasma dispersion of silicon. For example, a typical silicon MRM based on lateral reversely biased PN junction usually has a small tuning efficiency of ~20pm/V [22]. For this reason, it requires a large Q factor (~10^4) to reach enough extinction ratio (ER), which limits the modulation bandwidth less than 20 GHz due to the long photon lifetime. However, the RC-delay-limited bandwidth of conventional silicon MRM is typically much larger, ~150GHz. Therefore, in order to overcome the fundamental speed limit of the silicon MRMs, the key is to increase the wavelength tuning efficiency so that we can modulate the light with a relatively low-Q resonator and increase the photo lifetime-limited bandwidth. In section 5.1, we have demonstrated extreme large wavelength tunability of 271pm/V with TCO-gated Si microring resonator. In this section, we optimize the TCO-gated Si microring for high-speed operation, and demonstrated a high-speed MRM driven by an ITO/SiO_2/Si MOS capacitor.

5.2.2 Design and principle

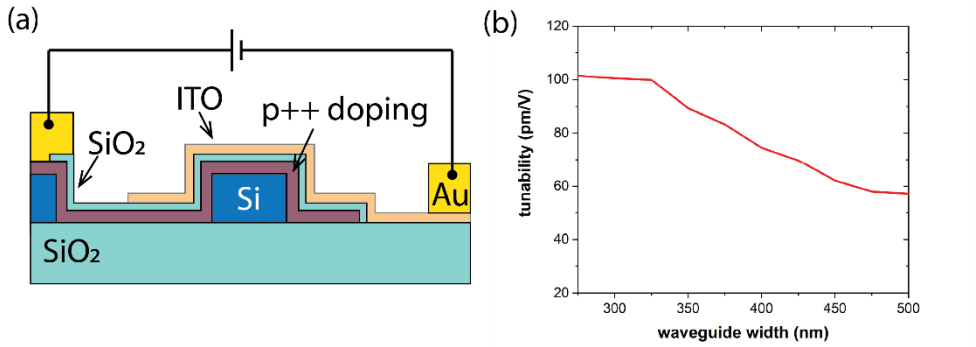

Figure 5.6 (a) Cross sectional schematic of the hybrid silicon-TCO microring modulator in the active region. (b) Simulated tunability as a function of the waveguide width for 15nm thick SiO_2 MOS insulator layer.

Fig 5.6a shows the cross-sectional schematic of the hybrid silicon-TCO microring modulator. The active region consists of an ITO/SiO_2/Si MOS capacitor. The bottom electrode consists of a 250nm thick p-type silicon rib waveguide and 50nm thick silicon slab for electrical connection. The insulator oxide and gate layer consist of 15nm thick SiO_2 and 20nm thick ITO. When a negative bias is applied on the ITO gate, the accumulated carriers at the interfaces blue shift the resonance of the microring. In previous sections, we have shown that the large capacitance density of the MOS capacitor can help achieve ultra-large wavelength tuning. So that we can efficiently drive a relative low Q-factor resonator, increasing the photon lifetime-limited bandwidth. However, large capacitance increases the RC delay, which may also limit the overall bandwidth. For this reason, here, we choose 15nm SiO_2 as the gate insulator layer, for the consideration of balance between tuning efficiency and RC delay. Similar to section 5.1, we optimize the E-O tuning efficiency by narrowing the waveguide width, due to increase of the overlapping between the accumulated carrier with the optical mode. Fig 5.6b shows the simulated E-O tuning efficiency as a function of the waveguide width. We can achieve a large tunability of 100 pm/V for 300nm wide waveguide with 15nm thick SiO_2 MOS insulator layer. With this large wavelength tunability, by principle we can reduce the Q-factor of the MRM to 1000~2000. Then,

we can increase the photon lifetime-limited bandwidth of over 100GHz, which will no longer be the limiting factor for overall bandwidth. Instead, the overall bandwidth will be limited by the RC delay bandwidth. Therefore, in order to reduce the series resistance, we doped the top 50nm thick of the rib waveguide and partially etched silicon slab to 1×10^{20} cm^{-3}. Fig 5.7b plots the mask layout we used for our device fabrication.

5.2.3 Fabrication and measurements

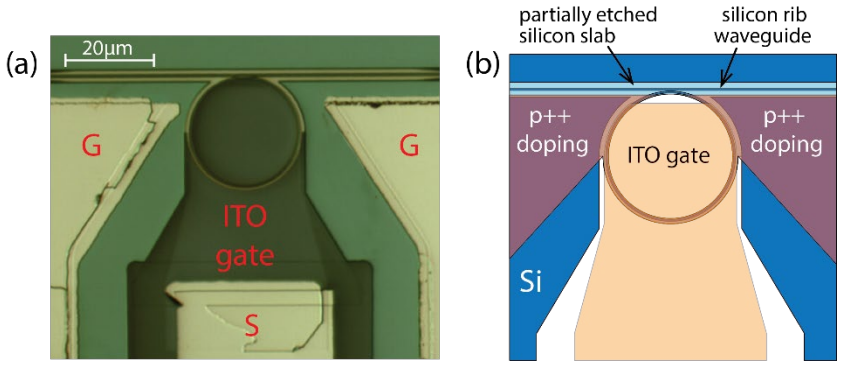

Figure 5.7 (a) Optical image of a fabricated hybrid silicon-TCO microring modulator. (b) Partial layout of the mask used for the fabrication of the device.

The MRM is fabricated on a 250nm thick silicon-on-insulator (SOI) wafer. First, the waveguide, microring are patterned by two steps of electron-beam lithography (EBL) and reactive ion etching (RIE). The microring has a radius of 12μm and a waveguide width of 300nm. Next, the active region and contact region are patterned and doped by by implantation with 5keV B^+ ions at flux of 6×10^{14} cm^{-2}. The implanted region is shown in fig 5.7b. Then, 15nm SiO_2 is formed by dry oxidation at 1000°C. After that, 20nm of ITO is RF sputtered, followed by the liftoff process. The oxide on silicon contact region is etched by Buffered HF. Then, Ni/Au electrode is thermally evaporated and patterned by photolithography to form Ohmic contact on both p-type silicon and ITO. Finally, the sample is annealed to reduce the resistivity. The fabricated device is shown in Fig 5.7a.

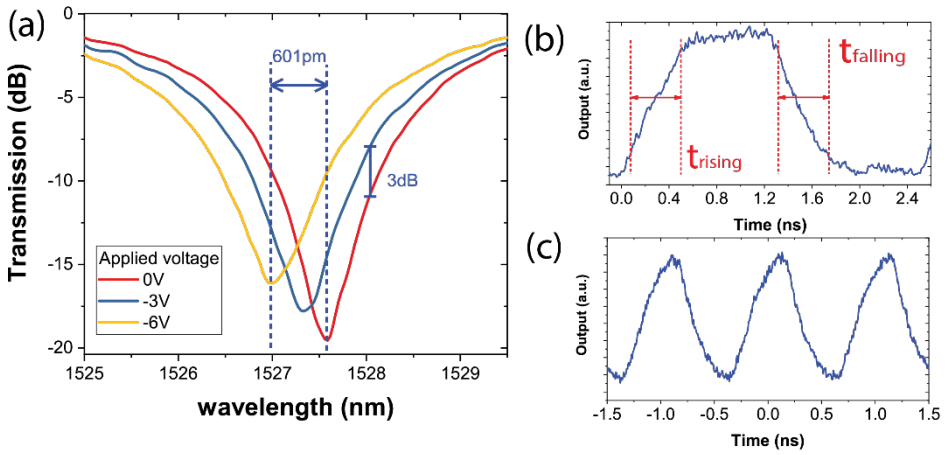

Figure 5.8 (a) Spectra of microring modulator under different negative bias voltage. (b) AC modulation output at 400MHz. (c) AC modulation signal at 1GHz.

Fig. 5.8a shows the resonance detuning at different bias voltage around 1527nm. The resonance wavelength blue shifts by ~601pm with -6V bias. It corresponds to an average tuning efficiency of ~100pm/V which matches with the simulation expectation. At zero bias, a low Q-factor of ~1000 is measured, which corresponds to a photon lifetime-limited bandwidth of 196 GHz. More than 3dB modulation can be achieved with $3V_{pp}$ voltage swing. Fig 5.8b shows the AC modulation output signal at 400MHz. We can clearly distinguish the "On" and "Off" states. Fig 5.8c shows the AC modulation signal at 1GHz. The modulation bandwidth can be estimated by the rise and fall time of 0.42ns to be 0.83GHz.

5.2.4 Modulation speed analysis and future optimization

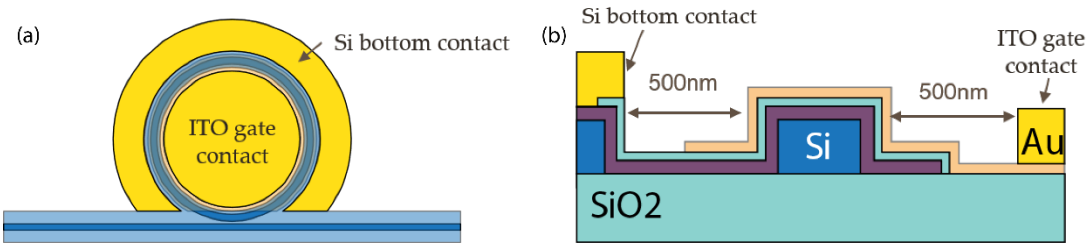

Figure 5.9 (a) Top view and (b) cross-sectional schematic of TCO-gated Si MRM with concentric metal contact.

The speed of our modulator is limited by the RC delay. The total capacitance of modulator is ~120fF. Then, the total series resistance can be estimated based on the bandwidth and capacitance, to be ~1500Ω. This large series resistance is due to the non-optimized electrode configuration, especially the long ITO conduction path between the metal electrode and the active microring, as we can see from fig 5.7a. However, the series resistance can be greatly reduced through optimizing the electrode design, such as using the concentric metal contact shown in fig 5.9a, which is used by most MRMs [22], [25], [38], [134], [141]. In this case, the RC-limited bandwidth can be calculated from resistance-length product R·L and the capacitance per length C/L according to the cross section of the active microring (fig 5.9b). The sheet resistance of the doped silicon and ITO are measured to be ~1100Ω/□ and ~700Ω/□, respectively. Assuming the metal contact is 500nm away from the waveguide edge, the resistance-length product is calculated to be 1500Ωμm. The capacitance density of MOS capacitor with 15nm thick SiO_2 insulator layer is around 2fF/μm^2, which give us a capacitance per length of 2.4 fF/μm. Then, we can have RC-limited bandwidth increased to 45 GHz, which corresponds to an overall 3dB bandwidth of 44GHz. Moreover, the resistance can be further reduced by using high mobility TCO as the gate layer, such as Ti-doped In_2O_3 or CdO. For example, if we replace ITO with Ti-doped In_2O_3 with mobility of (μ>80 m^2/(Vs)), we can increase the overall bandwidth to over 52 GHz, at the meantime also improving the Q factor to ~2,000.

5.2.5 Summary

In summary, we designed a silicon MRM driven by an ITO/SiO_2/Si MOS capacitor. The large capacitance density of the MOS capacitor results in large wavelength tunability, which enables us to overcome the speed limit of conventional Si MRM. Experimentally, we achieved a large tuning efficiency of 95pm/V with a low Q-factor of 1000. AC modulation is demonstrated up to 1GHz. Analysis shows that with the concentric metal contact design and high mobility TCO gate material, the modulation speed can be increased to over 52 GHz.

5.3 Summary

In summary, we introduce our work of the TCO-gated Si microring resonators in this chapter. The freedom of controlling the capacitance density via gate insulator of MOS capacitor enables us to tail the microring resonator for different applications.

In section 5.1, we designed and demonstrated a TCO-gated tunable microring filter driven by an ITO/HfO_2/Si capacitor. We took advantage of the large capacitance density of MOS capacitor with high-k material as gate insulator and improved the carrier-optical mode overlapping factor by narrowing waveguide. We achieve an unprecedented wavelength tuning efficiency of 271pm/V and over 2 nm electrical wavelength tuning range. Such TCO-gated microring filters can be used to replace conventional thermal tuning in on-chip microring WDM/DWDM optical interconnect systems while achieving faster response and negligible static energy consumption

In section 5.2, we optimized the TCO-gated microring for high-speed operation. Experimentally, we demonstrated a Si MRM driven by an ITO/SiO_2/Si MOS capacitor, achieving a large tuning efficiency of 95pm/V with a low Q-factor of 1000 and 1GHz AC modulation. Such wavelength tuning efficiency and the balanced the capacitance density of MOS capacitor with SiO_2 as insulator may help us overcome the speed limit of the conventional Si MRM. We show that with optimized metal contact design and high mobility TCO gate material, the bandwidth of the MRM can be increased to over 52 GHz.

Chapter 6. Ultra-fast Femto-joule All-optical Switching Using Epsilon-near-zero TCO

In previous chapters, we focus on the E-O applications of TCO materials. Besides the E-O applications, recently discovered extraordinary optical nonlinearities in ENZ TCO also open a new realm of ultra-energy-efficient, all-optical switching devices for future optical communication and computation. In this chapter, we propose a sub-micron, sub-pico-second, femto-joule level all-optical switch (AOS) using hybrid plasmonic-silicon

waveguides driven by high mobility transparent conductive oxides (HMTCOs) such as cadmium oxide. In section 6.2, we briefly introduce the origin of optical nonlinearity in TCO material. Our analysis indicates that the ENZ-induced nonlinear optical effect is greatly enhanced by the high free carrier mobility in the telecom wavelength region. In section 6.3, we propose an electrically tunable AOS device which is precisely biased at the ENZ condition, or the high-loss "OFF" state. Our simulation shows that the AOS device can be switched to the "ON" state with an unprecedented modulation strength of 15.9dB/μm and a rapid switching time of 230fs at the cost of an ultralow switching energy of 13.5fJ. In section 6.4, we compare our proposed AOS device with reported on-chip AOS devices by defining a comprehensive metric using the product of device size, switching energy and switching time. We show that the proposed ENZ-enabled device exhibits superior performance than any existing on-chip AOS device.

6.1 Introduction

Optical computing has resurged in recent years due to the tremendous throughput and low latency superior to the electronic counterpart [142]. While most state-of-the-art optical computing systems adopt hybrid photonic-electronic approaches due to the lack of optical logic gates and optical signal processing units, ultra-fast and energy-efficient all-optical switching (AOS) devices may hold the key to enable true photonic computing systems in the incoming decade [143]. Especially, on-chip AOS devices based on integrated photonics offers the potential for compact size, high density integration, ultra-high bandwidth and energy efficiency. Traditional AOS integrated photonic devices rely on the refractive index change of the waveguide induced by various optical nonlinearities, such as inter-sub-band transition (ISBT) in quantum wells [144]–[147], Kerr effect [148]–[150], band-filling dispersion (BFD) [151], [152], and two-photon-absorption (TPA)[153] . However, such devices require hundreds of microns to millimeters length of waveguide and high-energy input optical signals, which are not suitable for on-chip optical computation and signal processing. The energy consumption and device footprint can be dramatically reduced by microcavities, for example, microring resonators[154]–[157] and photonic crystal (PC) cavities

[158]–[161]. Nevertheless, it sacrifices the operational bandwidth due to the elongated photon lifetime, which undermines the most significant advantage of AOS devices. A thorough comparison of most representative on-chip AOS devices can be found at section 6.4, which shows a general trade-off between the switching time and energy efficiency. To break such intrinsic limit, it is essential to discover new nonlinear optical effects for AOS devices.

Recently, unprecedented nonlinear optical effects have been observed in ENZ TCO materials, such as indium-tin oxide (ITO) [162]–[165], aluminum-zinc oxide (AZO) [166]–[168], and cadmium oxide (CdO) [169], [170]. For example, unit order light-induced refractive index change has been demonstrated in bulk ITO [162], which is beyond the common perturbative description of nonlinear optical response [171]. The nonlinear optical effect in TCOs occurs in the sub-picosecond range, which offers the promise to break the intrinsic limit of switching speed and energy efficiency of AOS devices.

In this chapter, we propose the first design of integrated AOS device with femto-joule per bit switching energy based on a hybrid plasmonic-ENZ TCO-silicon waveguide. The innovation of this work comes from the following aspects. First, the low optical loss of the high mobility transparent conductive oxide (HMTCO) enables extremely small absolute permittivity at the ENZ condition, resulting in unprecedented ENZ-induced light confinement and optical nonlinearity. Second, the AOS device is electrically tunable by precisely biasing the HMTCO gate to reach the ENZ condition, which ensures high energy efficiency. We envision that such HMTCO-driven AOS device can be integrated with silicon photonic integrated circuits to realize on-chip optical signal processing and computation with ultra-low energy and ultra-high bandwidth.

6.2 Unprecedented optical nonlinearities in ENZ TCOs

We know that the optical properties of TCO in the telecom wavelength range can be described by the Drude model:

$$\varepsilon = \varepsilon_{\infty} - \frac{{\omega_p}^2}{\omega^2 + i\omega\Gamma}. \tag{6.1}$$

Here, the plasma frequency ω_p, which is usually given by

$$\omega_p = \sqrt{\frac{N_c q^2}{m_e^* \varepsilon_0}}, \tag{6.2}$$

depends is determined by the carrier density and material band structure. The information of the material's conduction band structure is embodied in the electron effective mass term m_e^*. In previous discussion, we always assume m_e^* is a constant for each material. However, it is only true under the assumption that the conduction band has a parabolic shape. In reality, it is not always the case. For example, TCO's optical nonlinearity is actually induced by the non-parabolicity of the conductive band [164], which means that the electron effective mass m_e^* in (6.2) is no longer a constant. A more accurate form of plasma frequency can be written as [163]:

$$\begin{aligned} {\omega_p}^2(E_F, T) = \frac{e^2}{3m_{e0}^* \varepsilon_0 \pi^2} \int_0^{\infty} dE(1 + 2CE)^{-1} \left[\frac{2m_{e0}^*}{\hbar^2}(E + \right. \\ \left. CE^2)\right]^{\frac{3}{2}} \left[-\frac{\partial f_{FD}}{\partial E}(E_F)\right], \end{aligned} \tag{6.3}$$

where m_{e0}^* is the effective mass of electron at the conduction band bottom, C is the non-parabolic parameter of the conduction band, and $(-\partial f_{FD}/\partial E)$ is a measure of the thermal broadening of the Fermi-Dirac distribution which is determined by the electron temperature. As a result, the average electron effective mass is a function of both the electron density and electron temperature. When a light pulse propagates through the TCO material, the absorbed photon energy heats up the electron temperature. The dynamics of this thermal process can be quantitatively interpreted by the two-temperature model (TTM), which we will discuss in section 6.3.2. The electron density of TCOs is orders of magnitude smaller than that of noble metals, which leads to

smaller electron heat capacitance [162]. Therefore, the electron temperature can experience significant change with moderate photon energy, which induces larger optical nonlinearity. Fig 6.1a plots the calculated plasmas frequency of CdO as a function of electron density and electron temperature. The material parameters used for calculation are as follows: ε_∞=5.6 [107], m_{e0}*=0.16m_0[172], C=0.5eV^{-1} [164], and μ=300 cm^2/V·s [169]. We can see that increase in electron temperature decreases the plasma frequency, similar to the decrease in the electron density. Fig 6.1b plots the permittivity spectra of CdO at different plasma frequencies, which correspond to electron density of 1×10^{20} cm^{-3}, 8.5×10^{20} cm^{-3}, 9×10^{20} cm^{-3}, and 9.5×10^{20} cm^{-3} at room temperature (outlined by white lines in fig 6.1a), respectively. As the plasma frequency increases, the permittivity decreases and the ENZ wavelength, where the real part of permittivity crosses zero, shifts to shorter wavelength and reaches 1.55 μm with electron density of 9.5×10^{20} cm^{-3} at the room temperature.

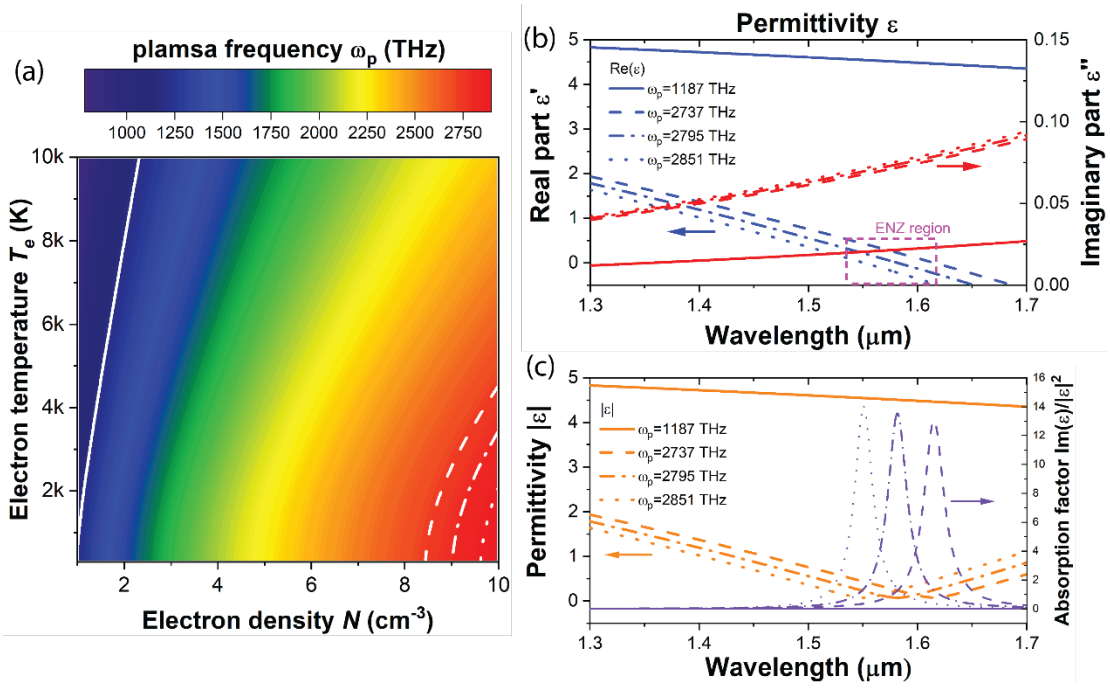

Figure 6.1 (a) Plasma frequency of CdO as a function of the electron density and electron temperature. (b) The real and imaginary part of CdO permittivity spectra at different plasma frequencies. (c) Absolute CdO permittivity and absorption factor spectra at different plasma frequencies.

The optical nonlinear process in TCOs involves two steps: absorbing the photon energy and transferring it into electron thermal kinetic energy. Since the conduction band non-parabolic parameters are similar for different TCOs [172], [173], how efficiently the photon energy can be absorbed determines the strength of nonlinear effect of the TCOs. In a typical TCO-based ENZ photonic device, there are two major factors contributing to the absorption of TCO: the intrinsic absorption due to the intra-band absorption and the extrinsic absorption enhancement by the ENZ effect. The intrinsic absorption is described by the Drude model. The imaginary part of the permittivity ε'' is proportional to the damping frequency Γ, $\varepsilon'' \propto \Gamma = q/\mu m_e^*$, which is determined by the electron mobility μ. For different TCOs, the electron mobility can vary over one order of magnitude from 20-30 $cm^2/V{\cdot}s$ of the lossy TCOs like ITO [118] to over 300 $cm^2/V{\cdot}s$ of HMTCOs such as CdO [169]. On the other hand, the extrinsic ENZ-induced absorption enhancement comes from the continuity of electric displacement field, as is discussed in section 2.2. When the real part of the permittivity equals zero, the TCO absorption factor, $A = \varepsilon''_{TCO}/|\varepsilon_{TCO}|^2$, is inversely proportional to the imaginary part of the permittivity, $A_{ENZ} = 1/\varepsilon''_{ENZ}$. It means that, at the ENZ condition, low loss HMTCO material actually absorbs more photon energy than the lossy TCO material, thus, having larger nonlinear optical effect. Fig 6.1c plots the absolute permittivity and absorption factor spectra of CdO at different plasma frequencies. We can see that the ENZ-enhanced absorption of CdO is like a low-Q resonant absorber with full width at half maximum of ~20nm. The peak absorption wavelength red shifts by ~30nm with a 2% decrease in the plasma frequency, which corresponds to reducing the electron density from 9.5×10^{20} cm^{-3} to 9.0×10^{20} cm^{-3} at the room temperature, or an increase of the electron temperature from room temperature to 2400K for electron density of 9.5×10^{20} cm^{-3}.

6.3 Electrically tunable ultrafast femto-joule per bit AOS based on plasmonic TCO-silicon waveguide

6.3.1 Device design and operation principle

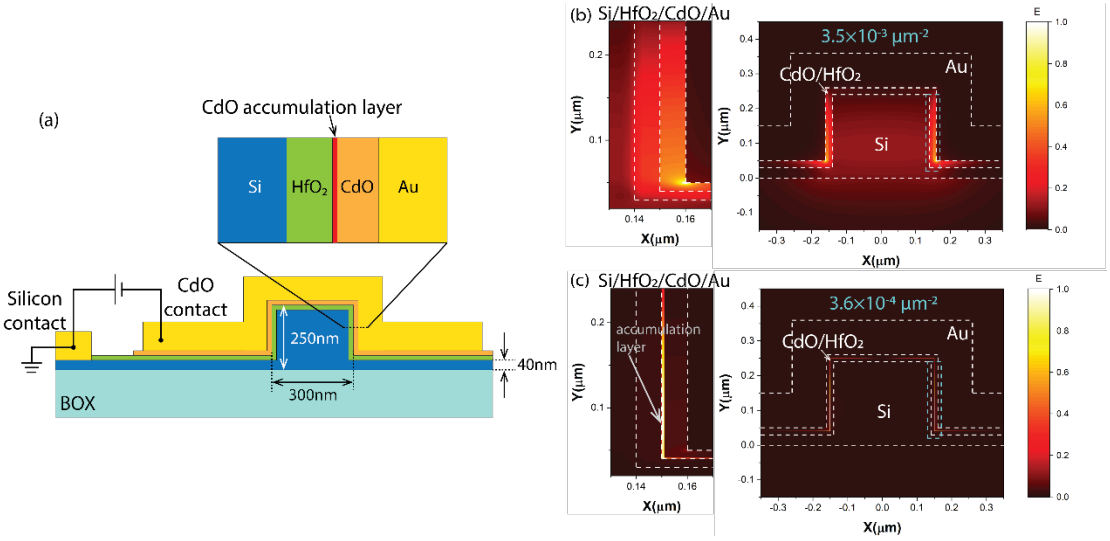

Figure 6.2 (a) Cross sectional schematic of the proposed plasmonic-CdO-Si AOS device. (b) and (c) Electric field distribution of the AOS at the (b) zero bias ("ON" state) and (c) ENZ condition ("OFF" state). Inset: zoomed-in electric field distribution at the side wall of the AOS device (cyan dashed box in 2b and 2c).

The working principle of the proposed on-chip AOS device depends on the unique design to electrically bias the CdO at the ENZ condition, which brings two exclusive advantages. First, it can guarantee that maximum nonlinear optical effects can be achieved and by tuning the bias voltage, the ENZ wavelength can be dynamically adjusted. Second, the bias voltage will only cause a very thin layer (~1nm) of accumulation layer while the majority of the CdO layer is still at moderate doping concentration, which will reduce excessive optical waveguide loss. The AOS device initially operates at a high-loss "OFF" state by biasing the CdO at the ENZ condition. Then the device is optically pumped to a low-loss "ON" state due to the increase of free electron temperature by the input optical pulse. Because of the high free electron mobility and the ultra-thin accumulation layer of CdO, the device can be switched with

an ultra-high energy efficiency and with an extremely large modulation strength between the “ON” and “OFF” state.

Fig 6.2a shows the cross-sectional schematic of the proposed AOS device based on a plasmonic CdO-Si waveguide. The active region consists of an Au/CdO/HfO_2/Si capacitor. The silicon rib waveguide in the center has a height of 250 nm and a width of 300 nm. 40 nm silicon slab provides the conduction path between the waveguide and the metal contact pad. On top of that are 10 nm HfO_2 as the insulator, 10 nm CdO and 100 nm Au as the gate electrode. Similar structures have already been used as high speed electro-absorption (EA) modulators in previous articles [74], [75], [114], but first time for on-chip AOS devices in this work. A negative gate bias induces electron accumulation at the CdO/HfO_2 interface. To simplify the analysis, we adopted an uniform electron density approximation for the optical simulation, where the continuous distribution of electron density in the accumulation layer is treated as an equivalent accumulation layer with a uniform electron density distribution over the thickness of the Thomas-Fermi screening length around 1nm [111]. Fig 6.3a plots the loss of the AOS device as a function of the accumulated electron density and wavelength. At zero bias, the accumulated electron density equals to the initial bulk electron density of CdO, which is ~3×10^{20} cm^{-3}, away from the ENZ region in the telecom wavelength range. The waveguide exhibits an “ON” state with low loss of 1dB/μm. The device loss remains low as the bias increases due to the high electron mobility of CdO until it reaches the “OFF” state at the ENZ condition. When the accumulated electron density increases from 8.78×10^{20} cm^{-3} to 9.75×10^{20} cm^{-3}, the ENZ wavelength is tuned from 1610nm to 1550nm. Therefore, we can precisely match the ENZ wavelength with the pump wavelength by controlling the bias to maximize the absorption efficiency and optical nonlinearity. For example, the loss spectrum with electron density of 9.18×10^{20} cm^{-3} (dashed cutline in fig 6.3a) is plotted in fig 6.3b, which exhibits an ENZ wavelength of 1585nm. The peak loss reaches over 35dB/μm due to the ENZ enhanced absorption. At this condition, if a pump pulse at the ENZ wavelength is coupled into the AOS device, the optical energy will be absorbed efficiently to heat up the electron temperature in the accumulation layer. Fig 6.3b shows

the loss spectra of 9.18×10^{20} cm^{-3} electron density at different electron temperature T_e by assuming the accumulation layer has a uniform electron temperature. As discussed above, increase of the electron temperature has a similar effect as reducing the electron density, which will red-shift the ENZ wavelength. In this case, we can send a probe signal at 1570nm, achieving both large extinction ratio (ER) and relatively low insertion loss (IL). Fig 6.2b and 6.2c plot the simulated electric field distribution of the AOS device at zero bias ("ON" state) and at the ENZ condition ("OFF" state), respectively. At zero bias, due to the plasmonic effect, the electric field is pulled towards the metal surface from the silicon core and concentrates in the CdO/HfO_2 oxide layer on both side walls of the waveguide. At the ENZ condition, the electric field is dramatically concentrated into the thin CdO accumulation layer due to the ENZ induced field confinement. Strong electric field confinement is especially important for reducing the optical energy consumption of the AOS device. Because the TCO nonlinear effect is quasi-proportional to the optical power intensity [162], [163], more confined optical modes induce larger optical intensity to enhance the nonlinear optical effect. In our design, the AOS device generates an ultra-small mode area of 3.6×10^{-4} μm^2 at the ENZ condition. It produces a power intensity of ~0.15GW/cm^2 in the accumulation layer with a moderate optical power of 1mW in the waveguide, which is one order of magnitude larger than the plasmonic effect only, and more than two orders of magnitudes larger than a regular silicon waveguide. In addition, we want to point out that the electrically accumulated 1nm thick TCO ENZ layer in our AOS device can achieve higher energy efficiency than the conventional bulk stoichiometric doped ENZ TCO [163], which has the entire TCO layer (10nm thick) at ENZ condition. Because in terms of ENZ induced field confinement, the level of light confinement is also affected by thickness of the ENZ layer, despite the free carrier mobility as discussed above. The light power intensity in the accumulated ENZ layer is ~10× higher than the case of bulk doped ENZ TCO for the same energy input due to thinner ENZ layer thickness, even though the total absorption for latter case is larger.

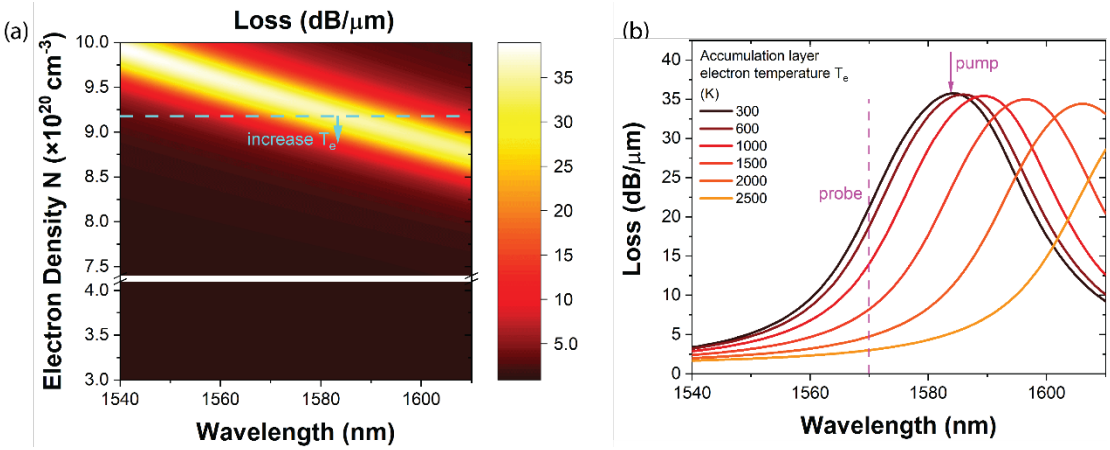

Figure 6.3 (a) Optical loss of the AOS device as a function of the wavelength and electron density in the accumulation layer. (b) Optical loss spectra of the AOS with accumulated electron density of 9.18×10^20 cm^-3 (dashed line in 3a) at different electron temperatures.

6.3.2 Transient response of AOS based on two-temperature model simulation

To evaluate the energy efficiency of the AOS device, we performed transient simulation of the AOS process by integrating the TTM with Lumerical MODE software, which is based on finite difference eigenmode (FDE) method. According to TTM, the evolution of the electrons and lattice temperature can be described by the following equations [162], [163]:

$$\begin{aligned} C_e \frac{\partial T_e(t)}{\partial t} &= -g_{ep}(T_e(t) - T_l(t)) + \frac{N(t)}{2\tau_{ee}(t)}, \\ C_l \frac{\partial T_l(t)}{\partial t} &= g_{ep}(T_e(t) - T_l(t)) + \frac{N(t)}{\tau_{ep}(t)}, \\ \frac{\partial N(t)}{\partial t} &= -\frac{N(t)}{2\tau_{ee}(t)} - \frac{N(t)}{\tau_{ep}(t)} + P. \end{aligned} \tag{6.4}$$

Here, N is the energy density stored in the non-thermalized part of the electron distribution, T_e and T_l are the electron and lattice temperature, C_e and C_l are the heat capacity of the electron and lattice, g_{ep} is the electron-phonon coupling coefficient, τ_{ee} and τ_{ep} are the electron-electron and electron-lattice relaxation time, and P is the

absorbed power density. The calculation of each parameter can be found in ref [162], [163]. We first extracted the absorbed power density distribution from the eigenmode simulation and plugged into (6.4). Then, the updated temperature-dependent CdO refractive index distribution was fed back into the eigenmode solver. Repeating this process, we can simulate the change of guided mode properties when a short laser pulse is passing through the AOS device. Because the absorption is majorly confined in the ENZ accumulation layer, we only considered the change of the refractive index in the accumulation layer. Also, for the ease of simulation, we ignored the thermal diffusion of electrons. When the electron temperature in the accumulation layer increases, the hot electrons tend to diffuse away from the accumulation layer, which shifts the ENZ wavelength in the same direction as heating up the electron temperature. Therefore, it is safe to ignore the thermal diffusion.

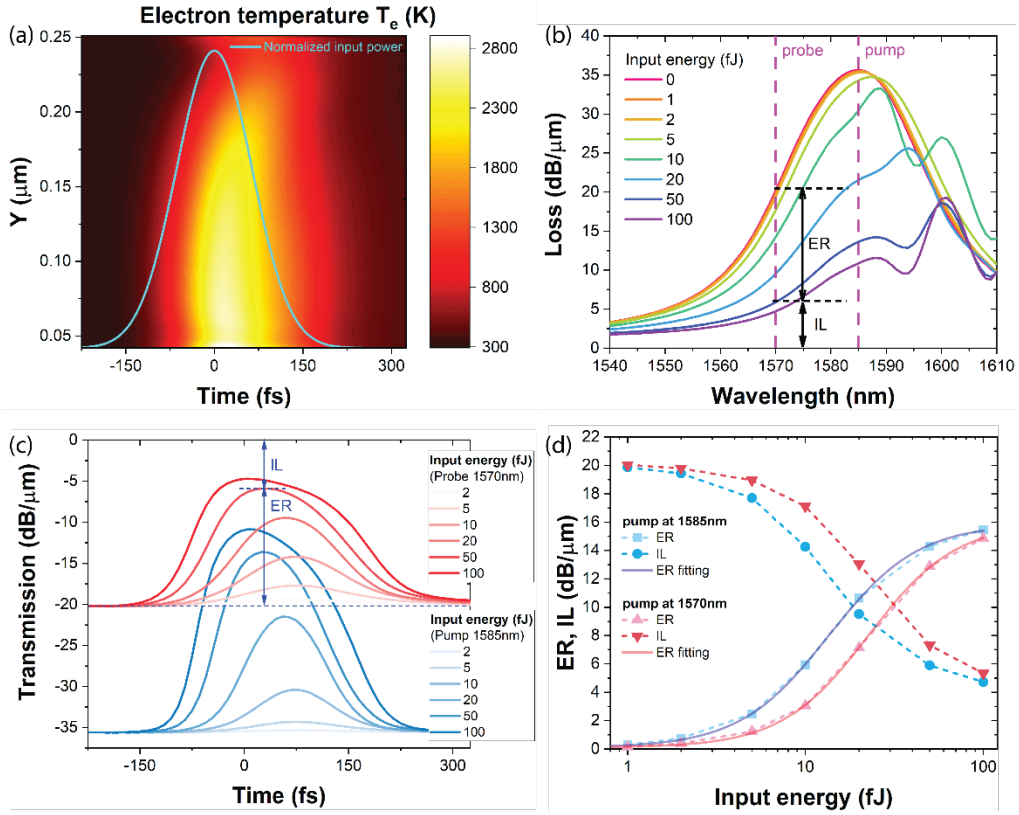

Figure 6.4 (a) Simulated evolution of the electron temperature distribution in the CdO accumulation layer at the side wall of AOS device with input pump pulse energy of 50fJ, assuming the accumulated electron density of 9.18×10^{20} cm^{-3}. The solid curve indicates the input laser pulse profile (arbitrary unit).

(b) Loss spectra of the AOS device with different input pump pulse energy. (c) Transient transmission of the AOS device at 1570nm and 1585nm with different input pump pulse energy. (d) Extinction ratio and optical loss of the AOS device at 1570 nm as a function of input pulse energy for different pump wavelengths.

We chose an accumulation layer with electron density of 9.18×10^{20} cm^{-3} for the transient simulation. A femtosecond pump pulse with a duration of 150fs at 1585nm is coupled into the AOS device. Fig 6.4a shows the evolution of the electron temperature distribution in the CdO accumulation layer at the side wall with the input laser pulse energy of 50fJ. The cyan curve denotes the incident pump laser pulse. The non-thermal energy stored in the excited electrons acts like a delayed source, heating the electrons and exhibits a quasi-intensity-dependent optical nonlinear effect. Fig 6.4b plots the loss spectra of the AOS device at the maximum modulation point for different energy of the pump pulse. The AOS provides a broadband nonlinear response near the ENZ wavelength. The pump wavelength reaches the largest ER over 20dB/μm. The probe wavelength is chosen at 1570nm since it produces the largest ratio between the ER and IL, which is critical for real applications. We should point out that the irregular shape of the loss spectra at the large input pump energy is because of the different electron temperatures in the accumulation layer as shown in fig 6.4a. Fig 6.4c plots the transient response of the AOS device loss at the pump and probe wavelength with different input pulse energy. Generally, the simulation predicts rising time ~100fs and slightly longer relaxation time, matching the previous reported experimental results [169]. The total switching window is ~230fs at 100fJ input energy. It means that the device can potentially operate at a repetition rate over 1Tera bit/s. Fig 6.4d shows the ER and IL at 1570nm as a function of input pump energy at different pump wavelength. Clearly, as the input energy increases, the ER increases while the IL decreases. With sufficiently large input pump energy, the AOS device exhibits saturable absorption. To quantitatively analyze the saturable absorption, we fit the AOS device to the following absorption coefficient α:

$$\alpha = \frac{\alpha_S}{1+\left(U/U_S\right)^p} + \alpha_{NS}, \tag{6.5}$$

where α_S and α_{NS} are the saturable and non-saturable absorption coefficients, which correspond to the maximum ER and minimum IL, respectively, U and U_S are the input pump energy and saturation energy, and p describes the sharpness of the transition. The fitted curve is plotted in fig 6.4d as solid lines. We derive α_S, α_{NS} and U_S to be 15.9dB/μm, 4.3 dB/μm, and 13.5fJ, respectively, which will provide a guidance for the AOS device design. For example, assuming a length of 330nm, the AOS device can achieve an ER of ~3dB and an IL of ~2.2dB with 25fJ input energy, but with requirement of pumping the AOS device at the ENZ wavelength. As comparison, if we pump the AOS device away from the ENZ wavelength, for example at the probe wavelength of 1570nm (red curves in fig 6.4d), the saturation energy U_S increases from 13.5fJ to 22.7fJ due to the reduced absorption efficiency.

6.3.3 Effect of TCO mobility on device performance

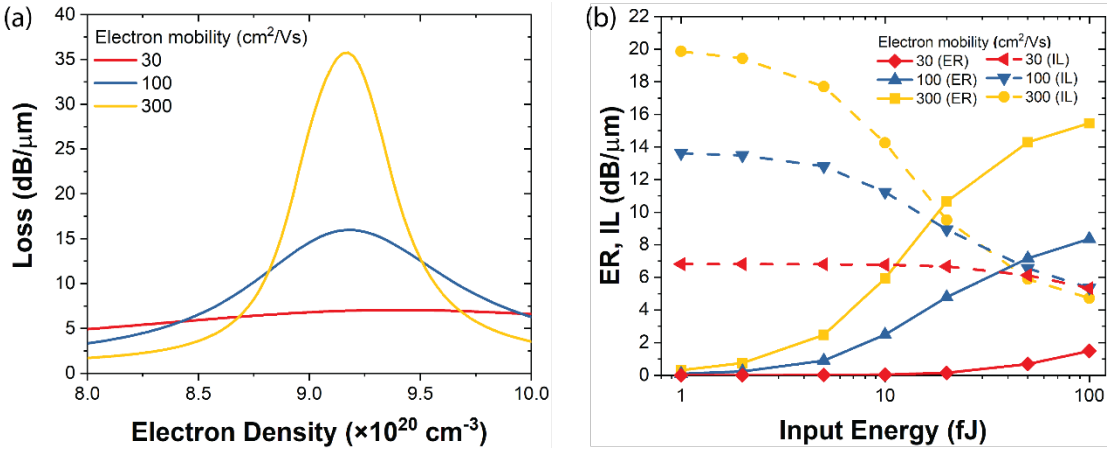

Figure 6.5 (a) Optical loss of the AOS device as a function of the accumulation layer electron density for different electron mobilities. (b) Extinction ratio and optical loss of the AOS device at 1570 nm as a function of input pump pulse energy at 1585nm for different TCO electron mobilities.

We have discussed the AOS design based on CdO with a high electron mobility of 300 cm^2/Vs. Similar AOS structure may also apply to other TCO materials. There are other

HMTCO materials, such as Ti-doped In_2O_3, which has a mobility ~100 cm^2/Vs [130]. In fact, the electron mobility of CdO itself may also vary from ~30 cm^2/Vs to 600 cm^2/Vs depending on the material process conditions, such as the deposition method, substrate materials, and dopant types [174]–[177]. Here, we compare how the electron mobility of TCOs will affect the performance of the AOS device. Fig 6.5a plots the optical loss of the AOS device as a function of the accumulation layer electron density for different electron mobilities of 30 cm^2/Vs, 100 cm^2/Vs, and 300 cm^2/Vs by assuming other parameters remaining the same as CdO. We can see that HMTCOs bring two major advantages. First, the peak absorption is proportional to the electron mobility. TCOs with higher mobility can be heated up to higher temperatures due to the larger absorption efficiency at the ENZ wavelength. Second, when the plasma frequency is shifting away from the ENZ condition, the slope of optical loss versus the shift of the plasma frequency is steeper for higher electron mobility. We simulated the AOS nonlinear response with the three electron mobilities. The pump and probe wavelength are kept the same during the simulation. The results are plotted in fig 6.5b. Generally, reducing the electron mobility from 300cm^2/Vs to 100 cm^2/Vs, the ER of the AOS reduces by half, and the saturation energy increases around 3× but still in the femtojoule range. However, for the mobility of 30 cm^2/Vs, the peak absorption is significantly smaller at the ENZ wavelength and it is not sensitive to the change of the accumulation layer electron density. The maximum ER is 3× smaller than the IL within the simulation range of the input energy. Thus, the energy consumption is significantly higher. Obviously, HMTCO plays a critical role in the operation of the AOS device.

6.4 Comparison with other on-chip AOS devices

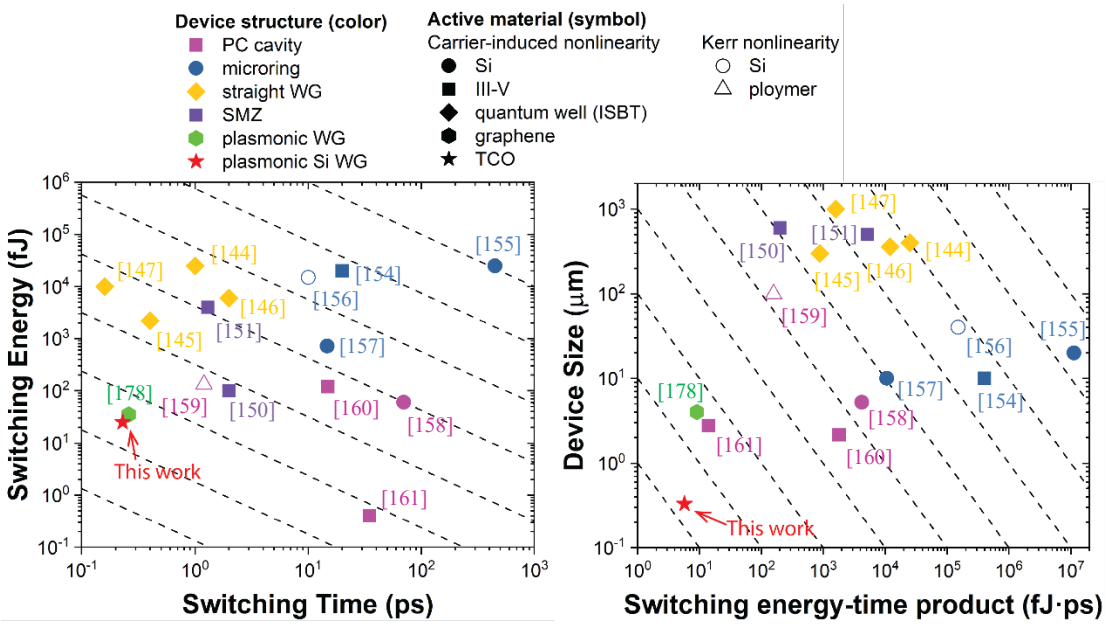

Figure 6.6 (a) AOS device performance comparison in terms of switching time and switching energy. (b) AOS device performance comparison in terms switching energy-time product and device size. The color of symbols represents the structure of the AOS devices. The shape of the symbols represents the active material of the AOS devices. The solid symbol indicates carrier-induced nonlinearity, and the hollow symbol indicates Kerr nonlinearity. (Ref [144] [145] [146] [147] [150] [151] [154] [155] [156] [157] [158] [159] [160] [161][178]*)*

The development of future on-chip optical computing systems has raised stringent requirement for AOS devices in terms of device footprint, energy efficiency and switching speed [143]. Here, we define a comprehensive metric of device size-switching energy-switching time product to compare our proposed AOS with other on-chip AOS devices. The results are summarized in fig 6.6. Fig 6.6a summarizes the device performances in terms of switching time and switching energy, and fig 6.6b compares the AOS devices versus switching energy-switching time product and device size. The color and shape of the symbols represent the structure and active material of the AOS devices, respectively. The solid symbol indicates that the AOS is based on a carrier-induced optical nonlinearity, which involves real transitions, such as TPA, single-photon absorption (SPA), BFD, carrier heating and ISBT. While the hollow

symbol indicates that the device is based on virtual transition optical nonlinearity, such Kerr effect. Generally, there are two types. The first type is based on light-induced real part change of the refractive index, which requires either a symmetric Mach Zehnder (SMZ) structure [151], [152] or a micro-resonator to convert the phase modulation to intensity modulation. SMZ based AOS can achieve an ultrafast switch on/off time of 2ps, by sending two control pulses to the two symmetric branches of the SMZ, despite the relative long carrier recombination time. However, such devices require a long device length of hundreds of microns. For a micro-resonator based AOS device, the Q factor is proportional to the required index shift which determines the switching energy, and is inversely proportional to the photon lifetime which limits the switching speed. In this sense, there is a trade-off between energy consumption and the switching speed. For a given material system, the wavelength detune of a resonator is proportional to the ratio between Q factor and mode volume, Q/V_m [179]. Since PC nanocavities offer much better light confinement than microring resonators, the switching energy-switching time product is also significantly smaller. In addition, the carrier-induced nonlinearity in III-V materials is larger than that in Si, therefore, III-V AOS is generally more efficient. To date, the most energy-efficient AOS device was achieved based on InGaAsP 2D PC nanocavity [161] with a switching time of tens of pico-seconds, but impossible to scale to sub-picosecond switching because of the limit of the long carrier lifetime and photon lifetime. The second type of AOS is based on saturable absorption, such as ISBT in semiconductor quantum wells, Pauli blocking of graphene, and the TCO nonlinear effect discussed in this paper. Generally, these nonlinear effects exhibit ultrafast switching time of less than 1ps. The energy efficiency is usually determined by how efficiently the light can be absorbed, which is often related to the light confinement in the active material. Recently, an ultrafast, energy-efficient AOS was demonstrated based on graphene-loaded deep-subwavelength plasmonic waveguide [178]. It reduces the length of device (~4μm) by 2 orders of magnitude compared with those ISBT AOS, achieving a switching energy of 35 fJ and a switching time of 260fs. However, the deep-subwavelength plasmonic waveguides induces significant insertion loss and may limit its potential for mass production. For our proposed AOS based on a HMTCO, it exhibits the largest absorption efficiency at the ENZ condition. We can

reduce the device length by another order of magnitude to less than 1μm with similar energy consumption as the graphene-loaded plasmonic waveguide. As a result, the proposed AOS device exhibits the smallest device size-switching energy-switching time product, unprecedented for any known design.

6.5 Summary

In summary, in this chapter, we propose a sub-micron, sub-picosecond, femtojoule level AOS device based on an electrically tunable plasmonic-CdO-Si waveguide. Our analysis shows that the high free carrier mobility of CdO plays a critical role in the ENZ-enhanced optical nonlinearity. It ensures the vanishingly small absolute permittivity at the ENZ condition due to the low optical loss, leading to unprecedented optical confinement and enhanced nonlinear optical interaction. Benefited from the electrically tunable design to induce only 1nm of ENZ layer, the energy efficiency of the device can be maximized by a gigantic saturable absorption coefficient of 15.9dB/μm with 13.5fJ energy and a switching time of 230fs. In addition, this unique design enables a sub-micron compact device size of less than 1 μm, which is essential for advanced optical processing and computing systems such as optical neural network [180]. Our simulation results indicate that HMTCOs play a pivotal role in achieving such superior performance and deserve future experimental investigation. Compared with existing on-chip AOS devices, our proposed HMTCO-driven device shows decisive advantages in terms of the device size-switching energy-switching time product. Furthermore, the AOS device is compatible with silicon photonic integrated circuits. Thus, we anticipate that our proposed HMTCO-driven AOS device will pave a new avenue for future development of ultra-fast, low-power, high-density on-chip optical signal processing and computing systems.

Chapter 7. Theoretical Analysis of Energy Efficiency and Bandwidth Limit of Resonator-based Silicon Photonic Modulators

In this chapter, we provide in-depth analysis and objective comments of resonator-based E-O modulators on silicon photonic platform driven by free carriers, the scope

of which is defined by comprehensive consideration of device footprint, energy efficiency, bandwidth, fabrication processes, and compatibility with silicon photonics and CMOS circuits. The chapter is organized as the following sequence. After a brief introduction in section 7.1, we review the free carrier dispersion effect of different active materials in section 7.2, which proves that many heterogeneously integrated E-O modulators should have higher E-O modulation efficiency than pure silicon photonic modulators. In section 7.3, we comprehensively analyze the energy efficiency of E-O modulation, showing that the carrier dispersion strength, the Purcell factor of the resonator and the total capacitance are the three prime parameters to improve the energy efficiency. Based on that, we compare the TCO-gated silicon resonator devices presented in this dissertation with other representative E-O modulator devices from the literatures. We show that Si-TCO PC nanocavity modulator is indeed one of the most promising strategies to push the energy efficiency boundary into the atto-joule per bit range. In section 7.4, we evaluate the bandwidth of the resonator E-O modulators from the perspective of Q-factor and RC delay due to the electrical structure of the device. In addition, the trade-off between the energy efficiency and bandwidth is outlined. In section 7.5, we discuss two other main sources of power dissipation which play dominate roles in practical PICs: wavelength control and driving electronic circuits. At last in section 7.6, we conclude this chapter.

7.1 Introduction

For every E-O modulator, the performance is ultimately determined by three main factors: active materials, photonic device design, and electrical structure. Because the majority of the reported E-O modulators are based on the refractive index perturbation induced by free carrier plasma dispersion effect. The scope of this chapter is limited to free-carrier-driven silicon E-O modulators, including silicon modulators with heterogeneously integrated materials. From the photonic device perspective, we focus on resonator-based E-O modulators, which have been widely accepted as the most energy-efficient devices for future on-chip optical interconnects. Besides, we will constrain our comparison between reverse biased p-n junction and MOS capacitor

silicon E-O modulators, which can potentially reach atto-joule/bit energy efficiency and greater than 10GHz bandwidth.

7.2 Free carrier dispersion of different semiconductor materials

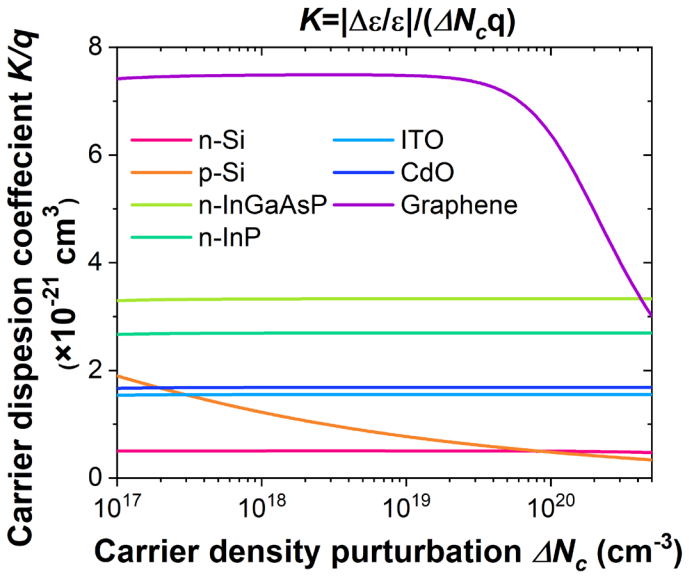

Figure 7.1 Carrier dispersion coefficient K of typical active materials as a function of carrier density perturbation ΔN_c.

The relationship between free carriers and semiconductor permittivity can be described by the well-known Drude model:

$$\varepsilon_r = \varepsilon_\infty - \frac{\omega_p^2}{\omega(\omega+i\Gamma)}. \tag{7.1}$$

The critical term here is the plasma frequency term ω_p^2, which is proportional to the free carrier density N_c. Then we can have the relationship between the relative permittivity perturbation $\Delta\varepsilon/\varepsilon$ and the change of free carrier density ΔN_c:

$$\frac{\Delta\varepsilon}{\varepsilon} = -\frac{\Delta N_c q^2}{\varepsilon_0 \varepsilon_r m^*}\frac{1}{\omega(\omega+i\Gamma)} \approx -\frac{\Delta N_c q^2}{\varepsilon_0 \varepsilon_r m^*}\frac{1}{\omega^2}, \tag{7.2}$$

To simplify the discussion, we ignore the imaginary part here for two reasons. First, the major modulation of a resonator-based E-O modulator comes from the resonance peak shift, which is due to real part of permittivity change. Second, in most cases the collision frequency (10^{12}~10^{13} Hz) in the imaginary part, which is determined by the carrier mobility μ, is much smaller than the optical frequency (1.93×10^{14} Hz for 1.55 μm wavelength). To be mentioned here, the E-O efficiency of MZI modulators is determined by the absolute change of the refractive index, which corresponds to the phase shift per unit length waveguide. However, for an optical resonator working at the resonance wavelength, the material permittivity and device physical dimension are correlated. The E-O efficiency is actually determined by the relative permittivity perturbation $\Delta\varepsilon/\varepsilon$. Here we define the carrier dispersion coefficient K to describe the strength of the free carrier dispersion effect of a semiconductor material:

$$K = -\frac{\partial \Delta\varepsilon/\varepsilon}{\partial \Delta N_c q} = \frac{q}{\varepsilon_0 \varepsilon_r m^* \omega^2} = \frac{1}{q N_{ENZ}}. \tag{7.3}$$

The physics meaning of K can be revealed by rewriting it into the fourth term of (7.2), where $N_{ENZ} = \varepsilon_0 \varepsilon_r m^* \omega^2 / q^2$ indicates the carrier concentration that is required to reduce the real part of permittivity to zero, or in other word, to reach ENZ. Table 6.1 lists the parameters of some typical carrier-driven active materials that are compatible with silicon photonics platform and the corresponding N_{ENZ} at 1.55μm according to (7.3). Fig 7.1 shows the carrier dispersion coefficient K of different materials as a function of free carrier density perturbation ΔN_c. From (7.3) we know that the plasma dispersion is only determined by the free carrier effective mass m^* and the semiconductor permittivity ε_r. N-type III-V semiconductors exhibit 5~6× stronger plasma dispersion effect than n-type silicon due to their small electron effective mass at the Γ point of the conduction band. On the other hand, TCOs exhibit ~3× stronger plasma dispersion which mainly comes from the smaller permittivity due to their wide bandgap. While for p-type semiconductors, due to the similar valence band structures, the difference in hole effective mass is much smaller compared with electron. Therefore, only p-type silicon is listed as the difference is minor. We have to point out that the

plasma dispersion model in (7.1) is simplified. In reality, the permittivity is determined by the complex band structure especially for large band bending. We also did not consider other carrier density-based mechanisms such as band-filling effect [2]. However, the principle of analysis still holds valid when the index perturbation is moderate or the driving voltage is not excessive, which applies to most on-chip E-O modulators. For silicon that serves as the baseline for comparison of various semiconductor materials, we use the more widely accepted model for plasma dispersion given in [16]:

$$\Delta n = -8.8 \times 10^{-22} N_n - 8.5 \times 10^{-18} \left(N_p\right)^{0.8}. \tag{7.4}$$

Similarly, we can also define the carrier dispersion coefficient K for graphene. Unlike most bulk semiconductors in which plasma dispersion is dominated by the Drude-like intra-band transitions, 2D material like graphene also exhibits large carrier induced dispersion due to the combined effect of both inter-band and intra-band transitions. The permittivity of graphene can be calculated from its in-plane conductivity given by the Kubo formula [181]:

$$\sigma_{\parallel} = \frac{iq^2(\omega - i2\Gamma)}{\pi(2\pi h)^2}\left[\frac{1}{(\omega - i2\Gamma)^2}\int_0^{\infty} \varepsilon \left(\frac{\partial f_d(-\varepsilon)}{\partial \varepsilon} - \frac{\partial f_d(\varepsilon)}{\partial \varepsilon}\right) d\varepsilon - \int_0^{\infty} \frac{f_d(-\varepsilon) - f_d(\varepsilon)}{(\omega - i2\Gamma)^2 - 4\left(\frac{\varepsilon}{2\pi h}\right)^2} d\varepsilon\right], \tag{7.5}$$

$$\varepsilon_{\parallel} = 1 - \frac{\sigma_{\parallel}}{i\omega\varepsilon_0 \Delta}. \tag{7.6}$$

Here $f_d(\varepsilon) = 1/\left\{e^{(\varepsilon - \mu_c)/k_B T} + 1\right\}$ is the Fermi-Dirac distribution, μ_c is the Fermi level, h is the plank constant, and Δ = 0.35 nm is the graphene thickness. The first and second term of (7.5) correspond to the intra-band and inter-band transitions, respectively. When the fermi level μ_c reaches half of the photon energy, the permittivity of graphene

reaches maximum as is listed in table 7.1. Further increasing the Fermi level (increasing carrier density of course), the inter-band absorption in graphene will be prohibited due to Pauli blocking [182], which dramatically decrease the imaginary part of the permittivity. In the meantime, there is a dramatic decrease of the real part of the permittivity due to the Kramers-Kronig relation. The combined effect of both inter-band and intra-band transitions offers the largest carrier dispersion effect enhancement of ~15× compared with n-Si and the smallest N_{ENZ}. However, an initial bias of graphene is required in order to achieve such huge enhancement. Moreover, the enhancement factor reduces to ~4× when the inter-band transitions are completely blocked as $\Delta N_c > 10^{20}$ cm^{-3} and the intra-band transition becomes the dominating effect.

Table 7.1 Parameters for typical active materials

material	Type	ε_r	Mobility (cm^2/Vs)[a]	Effective mass (m_0)	N_{ENZ} ($\times 10^{20}$ cm^{-3})
n-Si	IV group	12.1	720	0.26	19.75[b]
p-Si	IV group	12.1	290	0.37	9.78[b]
n-InGaAsP [49], [183]	III-V group	10.65	1800	0.06	2.98
n-InP [49], [183]	III-V group	9.95	2000	0.08	3.71
ITO [184]	TCO	3.9	28	0.35	6.37
CdO [174], [185]	TCO	5.3	205	0.24	5.93
Graphene [181]	2D material	9.03	1000 [186]	~	1.33

[a] Mobilities of IV and III-V group semiconductors listed here are considered with carrier density of 1×10^{18} cm^{-3}; mobilities of TCOs are considered with carrier density of ~1×10^{20} cm^{-3}; mobility of graphene is under condition when in-plane permittivity reach maximum (Fermi level $\mu_c = 0.4$eV).

[b] N_{ENZ} for silicon is calculated using the carrier dispersion coefficient K from (7.4) at doping level of 2.5×10^{18} cm^{-3}.

7.3 Resonator-based modulators

7.3.1 General model for the energy efficiency of resonator-based modulators

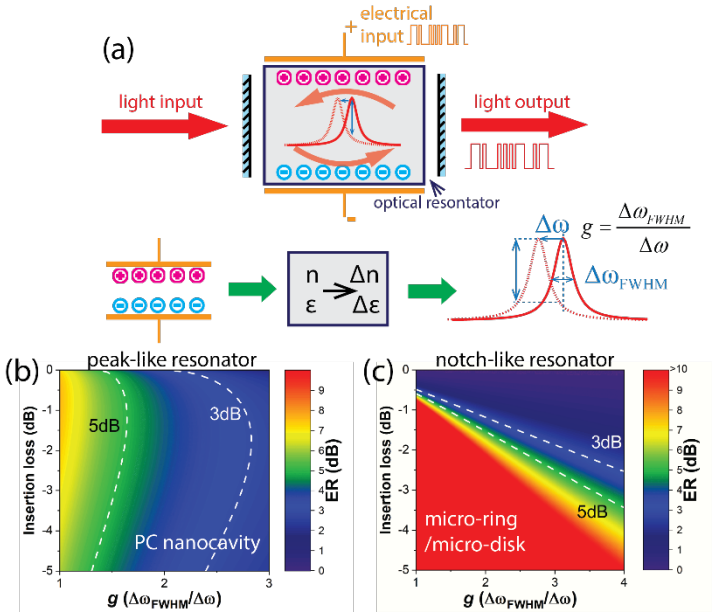

Figure 7.2 (a) Principle schematic of a carrier-driven resonator-based E-O modulator. (b) and (c) Extinction ratio as a function of insertion loss and wavelength detuning factor g for peak-like (PC nanocavity) and notch-like (micro-ring/micro-disk) resonator, respectively.

For a carrier-driven resonator-based modulator, the process to convert electronic signals into coded optical signals can be divided into three steps as illustrated in Fig 7.2a. First, the electrical energy is consumed by charging the active capacitor, changing the distribution of free carriers inside the device; next, the modified free carrier distribution changes the local material optical permittivity or refractive index; finally, the change of local optical properties detune the resonator, modulating the transmitted optical waves. Considering an optical resonator with a Q-factor of Q operating at the resonant frequency of ω, the resonance detuning $\Delta\omega$ of the resonator can be described by cavity perturbation theory [187]:

$$\Delta\omega = \frac{-\frac{\omega}{2}\int \Delta\varepsilon|E|^2 dv}{\int \varepsilon|E|^2 dv}, \tag{7.7}$$

where ε and $\Delta\varepsilon$ are the distribution of the initial and perturbed permittivity, and E is the electric field distribution of the optical resonance mode. The required resonance detuning to achieve certain ER can be expressed as $\Delta\omega = \Delta\omega_{FWHM}/g = \omega/(\mathrm{gQ})$, where wavelength detuning factor g is defined as the ratio of the full width at half maximum (FWHM) of the resonance, $\Delta\omega_{FWHM}$, to the required resonance detuning. This factor depends on the resonator type, whether it has a peak (PC nanocavity) or a notch (micro-ring and micro-disk) in the transmission spectrum, and the target ER. Fig 7.2b and 7.2c plot the ER as a function of the insertion loss (IL) and g factor for peak-type and notch-type resonator, respectively. In the calculation, we assume both resonators having Lorentzian-shape resonance. To simplify the analysis, the effect of carrier absorption is ignored since most resonator modulators only require moderate free carrier concentrations. Generally, a g factor of 1~2 is required for a reasonable IL. However, for the notch-like resonator, much smaller wavelength detuning is possible by sacrificing the IL.

Then, by plugging (7.2) and (7.3) into (7.7) and considering both n-type (ΔN_e) and p-type (ΔN_h) free carriers, we can rewrite (7.7) as:

$$\begin{aligned}\frac{1}{\mathrm{gQ}} = \frac{\Delta\omega}{\omega} &= \frac{\int \varepsilon(K_n \Delta N_e + K_p \Delta N_h) q |E|^2 \, dv}{2V_m \max(\varepsilon|E|^2)} \\ &= \frac{\alpha K Q_{tot}}{2V_m} = \frac{\alpha(K_n Q_n + K_p Q_p)}{2V_m}\end{aligned}, \tag{7.8}$$

where $K_n = q/(\varepsilon_0 \varepsilon_r {m_e}^* \omega^2)$and $K_p = q/(\varepsilon_0 \varepsilon_r {m_h}^* \omega^2)$.

Here V_m is the optical mode volume of the resonant mode which is defined as $V_m = \int \varepsilon|E|^2 dv/max(\varepsilon|E|^2)$ [188]. The overlapping factor $\alpha = [\int \varepsilon(\Delta N_e + \Delta N_h) q|E|^2 dv]/[Q_{tot}\, max(\varepsilon|E|^2)]$, describes the overlapping between

the carrier distribution perturbation and the optical mode. Based on this definition, the maximum efficiency (α = 1) happens when all the free carrier distribution perturbation is induced at the region where the optical field has the maximum electrical energy density. From (7.8) we can get that the total charge Q_{tot} required to drive the modulator is inversely proportional to the ratio between the Q-factor and the mode volume (Q/V_m), which is more often referred to as the Purcell factor, F_p, which is an intrinsic factor of an optical resonator defined by (7.10) [189].

$$Q_{tot} = \frac{2V_m}{\alpha K g Q} \propto \frac{V_m}{Q} \propto \frac{1}{F_p}, \tag{7.9}$$

$$F_p = \frac{3}{4\pi^2}\left(\frac{\lambda}{n}\right)^3 \frac{Q}{V_m}. \tag{7.10}$$

Here λ is the resonance wavelength, and n is the refractive index of the semiconductor. Now, bridging the relationship between the free carrier and optical resonator, we analyze the electrical energy consumption. Since every silicon E-O modulator is essentially a capacitor. The energy consumption per bit can be estimated by:

$$E_{bit} = \frac{1}{4}CV^2 = \frac{1}{4}\frac{(Q_{tot}/2)^2}{C}, \tag{7.11}$$

where C is the capacitance of the E-O modulator and V is the operation voltage. Since we have shown that the total charge perturbation Q_{tot} is directly related to the optical modulation, it is more straightforward to consider the energy consumption based on the rightmost side of (7.8). In a short summary, by plugging (7.9) and (7.10) into (7.11), we can quantitatively calculate the energy efficiency of the E-O modulator:

$$E_{bit} = \frac{9}{64\pi^4}\left(\left(\frac{\lambda}{n}\right)^3 \frac{1}{gF_p}\right)^2 \frac{(qN_{ENZ})^2}{\alpha^2 C} \propto \frac{1}{K^2}\cdot\frac{1}{g^2F_p^2}\cdot\frac{1}{\alpha^2 C}. \tag{7.12}$$

From (7.12) it is very clear to see how the three factors can determined the energy consumption of an E-O modulator: the active material determines the carrier dispersion coefficient K; the resonator design determines the Purcell factor F_p and wavelength detuning factor g; and the electrical configuration determines the total capacitance C and the overlapping factor α.

Similarly, we can express the electrical wavelength tunability and the required driving voltage as:

$$\frac{\Delta\lambda}{V} = \lambda\left(\alpha \cdot K \cdot \frac{C}{V_m}\right), \tag{7.13}$$

$$V = \frac{3}{4\pi^2}\left(\left(\frac{\lambda}{n}\right)^3 \frac{1}{gF_p}\right)\frac{(qN_{ENZ})}{\alpha C} \propto \frac{1}{K}\cdot\frac{1}{gF_p}\cdot\frac{1}{\alpha C}. \tag{7.14}$$

7.3.2 Comparison of micro-resonator designs

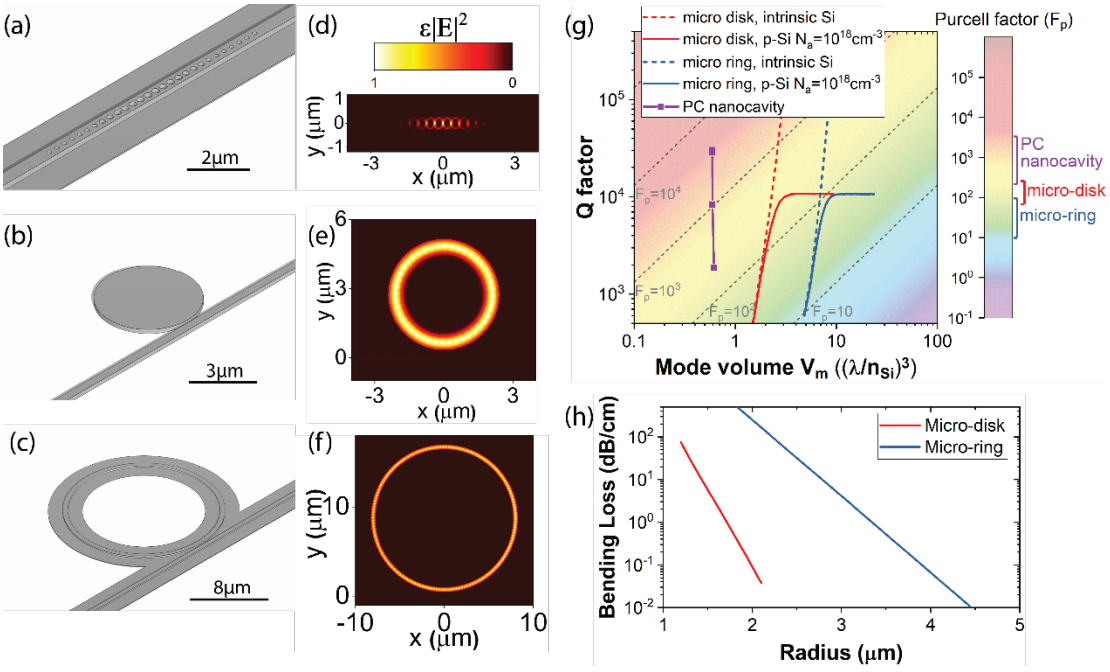

Figure 7.3 (a)-(c) 3D schematics of the PC nanocavity (a), micro-disk (b) and micro-ring (c) resonator used in the simulation; (d)-(f) Simulated corresponding electrical energy density distribution of resonators shown in (a)-(c). (g) Simulated Q-factor of the three resonator designs as a function of mode

volume V_m. The dashed lines refer to the case of intrinsic silicon when the Q factor is only limited by the bending loss of the micro-disk/micro-ring; and solid lines refer to the case of moderately doped Si with doping level of 10^{18} cm^{-3} when carrier absorption limits the Q factor at large mode volume. (h) Simulated bending loss of micro-disks and micro-rings as a function of radius.

Three main optical resonator designs have been used for E-O modulators: PC nanocavity, micro-disk and micro-ring. Fig 7.3g plots the simulated Q-factor versus the cavity mode volume of these three kinds of resonators. The exact structures in our simulation are illustrated in Fig 7.3a-7.3c. Fig 7.3d-7.3f plot the electrical energy density (εE^2) distribution of the corresponding resonators shown in Fig. 7.3a-7.3c. We can directly see the difference in mode volume of these three resonators. For the PC nanocavity, we consider the 1D ridge PC nanobeam cavity design from [36], which is also the PC nanocavity design used in section 4.3. We need to point out that there are other more complex PC nanocavity designs that can offer even smaller mode volume [190], [191]. But we limit our analysis to this design due to its design simplicity. Here, two PC mirror segments are placed back to back with air hole size quadratically tapered from the center to the edge of the cavity. The waveguide is 500nm in width and 250nm in height, and the slab thickness is 50nm. The thickness of the micro-disk resonator is 220nm used in [30]. The micro-ring resonator has the ridge waveguide cross section in [23] with 500nm waveguide width, 220nm waveguide thickness, and 60nm slab thickness. Because of the rotation symmetry, the micro-disk and micro-ring resonators can be simulated by solving the cross section eigenmode using 2D finite element method (FEM). Then the Q factor can be calculated as [192]: $Q = \pi n_g L\sqrt{ra}/[\lambda(1-ra)]$, where n_g is the group index, L is the round trip length, a is the single-pass amplitude transmission and r is the self-coupling coefficient which equals to a under critical coupling condition. On the other hand, PC nanocavities have to be simulated by 3D finite-difference time-domain (FDTD) method. The Q factor is calculated from the slope of the envelope of the decaying signal. Here, the simulations are conducted by Lumerical MODE and FDTD software, respectively.

The micro-disk and micro-ring resonators are similar to some extent. The Q-factor scales up with the resonator radius due to smaller bending loss (Fig 7.3h). However,

the whisper-gallery-mode in micro-disk provides better mode confinement compared with the waveguide confinement in micro-ring, micro-disk offers 2.5× smaller mode volume compared with micro-ring to reach the same Q-factor. In principle, ultra-high Q-factor can be achieved in both micro-disk and micro-ring as shown by the dashed lines in Fig 7.3f. However, in reality the Q-factor is limited due to many engineering reasons such as surface roughness, carrier absorption, and concerns of photon lifetime. For example, the solids lines in Fig 7.3f plot the cases when micro-disk or micro-ring is uniformly p-type doped to carrier density of 10^{18} cm^{-3}, in which the carrier absorption limit the Q-factor to ~10^4. So typically, a micro-ring resonator gives a Purcell factor less than 100 and a micro-disk resonator exhibits a Purcell factor between 70 and 250.

The Q-factor of the PC nanocavity is majorly limited by the mirror strength of the PC segment which is determined by the number and tapering manner of air holes [119]. In Fig 7.3f, three purple dots correspond to the cases with 11, 14 and 17 air holes in each PC mirror segment. We can see that as the Q-factor increases to ~10^4, the mode volume is almost a constant since the mode volume is only determined by how the air holes are tapered in the center region of the nanocavity. Compared with micro-disk, a PC nanocavity provides 5~7× reduction in mode volume, thus yielding a Purcell factor from 200 to 4000. Clearly, PC nanocavity surpasses micro-disk and micro-ring resonators in terms of the Purcell factor, which is very crucial for atto-joule/bit E-O modulators.

7.3.3 Case study

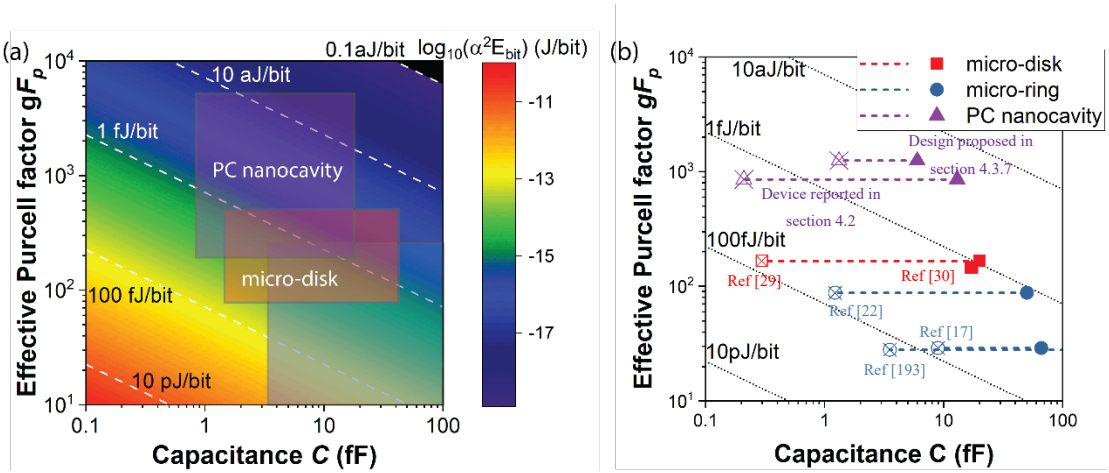

Figure 7.4 (a) Energy consumption per bit of a pure silicon resonator-based E-O modulator operating at 1.55μm as a function of the effective Purcell factor and the capacitance under maximum efficiency condition (α=1). The result is calculated assuming a silicon doping level of 2.5×10^{18} cm^{-3} for both n-type and p-type. The wavelength detuning factor g used to estimated the upper boundary of PC nanocavity, micro-disk and microring are 1.6, 2 and 2.7, respectively. (b) Visualization of the relationship among Purcell factor, total capacitance, overlapping factor and energy efficiency for reported E-O modulators.

Fig. 7.4a plots the calculated energy consumption per bit of a silicon resonator-based E-O modulator as a function of the effective Purcell factor (gF_p), which includes the effect of wavelength detuning factor g, and total capacitance under maximum overlapping factor condition (α=1) operating at 1.55 μm according to (7.12). The corresponding regions of different types of resonators are outlined. For better illustration, we also analyze some reported resonator-based silicon E-O modulators from literatures by comparing the effective Purcell factor, capacitance, and energy efficiency. The results are summarized in Fig 6.4b, which is overlaid on top of Fig 7.4a. The solid symbols indicate the theoretical limit of the energy efficiency, which is calculated from the reported capacitance and calculated effective Purcell factor in each reference based on the assumption of perfect overlapping factors. In most cases, however, the capacitor-induced free carrier charge is not perfectly overlapped with the optical mode. Therefore, the reported energy consumption is always higher than the

theoretical limit, the results of which are represented by the cross-centered symbols. The overlapping factor can be extracted by $C_{solid}/C_{cross} = 1/\alpha^2$. From this, we can also obtain the effective capacitance that contributes to the E-O modulation as C_{solid}/α.

Table 7.2 Parameters for reported resonator-based modulators

Ref	Capacitor /resonator type	Q-factor	Vm $((\lambda/n_{Si})^3)$	gFp	C (fF)	α	Ebit (fJ/bit)
[29]	vertical PN junction /micro-disk	9700	4.46	166	20	12.2%	61
[30]	vertical PN junction /micro-disk	6480	6.82	146.5	17	100%	1
[22]	lateral PN junction /micro-ring	14500	36.29	87.5	50	15.6%	50
[193]	Si/oxide/Si MOS /micro-ring	3500	21.20	28	320	10.5%	180
[17]	interleaver PN junction /micro-ring	14500	105.74	29	66	36.9%	66
Device reported in section 4.2 [34]	hybrid Si-ITO MOS /PC nanocavity	3700	0.55	855	13	7.4%	3.25
Design proposed in section 4.3.7	hybrid Si-ITO MOS /PC nanocavity	5600	0.66	1247	6	22%	0.375

Parameters for the case study are listed in table 6.2. We briefly comment on these three different resonator E-O modulators. Micro-ring resonator E-O modulators have been extensively developed [6], [7], [25]–[28], [17]–[24] and can be fabricated using standard silicon photonics foundry. Here we just list some representative examples with different doping configurations. Due to the relative small Purcell factors, the energy efficiency of micro-ring E-O modulators using on-off key (OOK) signal is typically

limited to a few tens of femto-joule per bit. Using more advanced coding techniques such as pulse-amplitude modulation (PAM) can further improve the energy efficiency of micro-ring modulator [23], but may require higher energy for decoding on the receiver side. For the micro-disk E-O modulators, the state-of-the-art experimental demonstration achieved ~1fJ/bit energy efficiency at 25Gb/s data rate using a vertical p-n junction electrical configuration. [30] We can see that this result is already the theoretical limit of the modulator design due to the perfect overlapping factor. To further reduce the energy consumption, it requires one or more of following approaches: reducing the micro-disk size to increase the Purcell factor, integrating more efficient active materials, or implementing new electrical configuration with larger capacitance density while still maintaining the overlapping factor. In comparison, a PC nanocavity based modulator driven by hybrid Si-ITO MOS capacitor presented in section 4.2 has the smallest theoretical energy consumption due to the high Purcell factor enabled by the ultra-compact mode volume and the large capacitance of the MOS capacitor in the active region. The main drawback of the Si-TCO hybrid PC nanocavity modulator is the relatively small overlapping factor. The carrier accumulation of MOS capacitors occurs at the interfaces of the waveguide, while the perturbation of free carriers of reversed biased PN junction is inside the waveguide, which intrinsically has better overlapping with the optical mode. For example, the overlapping factor of the PC nanocavity modulator from section 4.2 is more than one order of magnitude smaller than that of a vertical PN junction micro-disk modulator [30], which reaches a perfect overlapping. Luckily, the overlapping factor of the TCO-Si hybrid PC nanocavity modulator can be further optimized by taking advantage of the subwavelength structure of PC nanocavities as discussed in section 4.3.6. Besides, further reducing the energy consumption can also possibly be achieved by adapting PC nanocavities with more miniaturized cavity mode volume, such as slot PC cavities [190] or bowtie PC cavities [191]. In summary, Si-TCO PC nanocavity modulator offers us the best possibility to achieve both high-speed operation and extremely low energy consumption at hundreds of atto-joule per bit level simultaneously. However, significant engineering optimization is still needed to achieve such ultimate goals.

7.3.4 Comparison of p-n junction and MOS capacitor

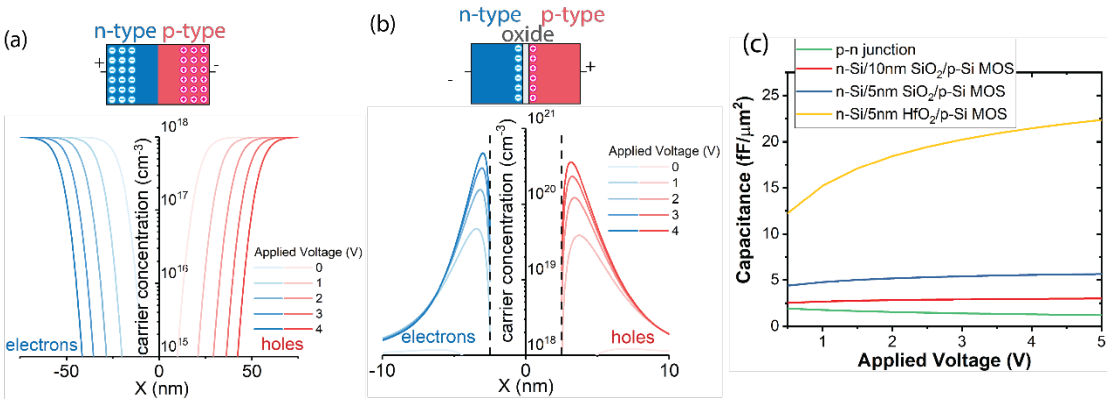

Figure 7.5 (a)-(b) Free carrier distribution of p-n junction (a) and Si/5nm SiO_2/Si MOS (b) at different applied voltage. Inset: schematics of two capacitor configurations; (c) Capacitance density as a function of the applied voltage for different configurations.

Two electrical configurations of free carrier-driven modulators have been demonstrated: reversed p-n junction and MOS capacitor as schematically represented in the inset of Fig 7.5a and 7.5b. According to (7.12), the energy efficiency of a resonator-based E-O modulator is proportional to its total capacitance. Given the size of an optical resonator, especially for ultra-compact resonator like PC nanocavity, the key metric to determine the energy efficiency is the capacitance density. The capacitance density of an abrupt p-n junction under reverse bias approximately follows:

$$\frac{C_j}{A} \approx \frac{1}{2}\sqrt{\varepsilon_0 \varepsilon_s q \frac{N}{V+\phi_B}} \propto N^{\frac{1}{2}}, \tag{7.15}$$

assuming equal donor and acceptor concentration N_D=N_A=N, ε_s is the static relative permittivity of the semiconductor and ϕ_B is the built-in potential. For given semiconductors, the only parameter we can tune is actually the doping concentration N. However, higher doping concentration also leads to higher optical loss, which can limit the Q-factor. As a result, almost all experimentally reported silicon E-O modulators choose the doping concentration to around 10^{18} cm^{-3}, which balance the energy

efficiency with other performance metrics. The room to improve the capacitance density of reversed p-n junction is very limited.

While for MOS capacitors, the capacitance density can be estimated as:

$$\frac{C_{MOS}}{A} \approx \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}, \tag{7.16}$$

Where ε_{ox} is the static relative permittivity of the gate oxide, and t_{ox} is the gate oxide thickness. MOS capacitors offer us the freedom to scale up the capacitance density over a wide range by varying the gate oxide thickness or using high-k gate oxide materials such as HfO_2. As comparison, Fig 7.5c plots the capacitance densities of p-n junction and Si/oxide/Si MOS capacitor as a function of the applied voltage simulated by SILVACO Atlas assuming a silicon doping concentration of 10^{18} cm^{-3}. Three different gate oxide layers (10nm SiO_2, 5nm SiO_2, 5nm HfO_2) are simulated for the MOS capacitor. At 1V applied voltage, the capacitance density of MOS capacitor with 10nm SiO_2 gate oxide is comparable to that of a reversed p-n junction. While for MOS capacitors with 5nm SiO_2 and 5nm HfO_2 gate oxide layers, the capacitance densities are 2.8× and 9.6× times larger than that of the p-n junction, respectively. In the current 32 nm CMOS technology node, the equivalent oxide thickness (EOT) is now less than 1nm [194]. Therefore, there is still room for further increase of the capacitance density using the MOS structure. Besides, we can see that the capacitance density of both configurations is a function of the applied voltage. Figure 7.5a and 7.5b plot the carrier density distribution of the p-n junction and MOS capacitor at different applied voltage. For p-n junction, the voltage dependence is implied in (7.15), as applied voltage increases electrons and holes are more separate from each other; while for the MOS capacitor, this is because as voltage increases, the average center of the accumulation layer moves towards oxide interface as is shown. Obviously, the two different configurations have completely different distributions of the free carrier perturbation. While such difference won't affect the modulation efficiency. According to (7.8), the resonance detuning is only proportional to the total charge perturbation, as long as the

charge is overlapped with optical field. The even extreme case would be that all the charge perturbation is induced at the maximum electrical energy density point. The ability to enhance the E-O efficiency by a MOS capacitor configuration has been verified in MZI based E-O modulators. The most efficient Si MZI modulator was demonstrated using Si/oxide/Si MOS configuration in the accumulation mode fabricated by 130nm CMOS technology node (gate oxide thickness ~2nm), exhibiting a $V_\pi L$ of 2V·mm [195], which is nearly one order of magnitude improvement compared with the common lateral p-n junction MZI modulators [10], [196]. Moreover, because n-type and p-type semiconductors are separated by a thin oxide layer in a MOS capacitor, it is easier to heterogeneously integrate other active semiconductor materials with silicon in a hybrid MOS configuration to further improve the energy efficiency. Still using MZI modulators as examples, a $V_\pi L$ of 0.9 V·mm was demonstrated using InGaAsP/Si hybrid MOS capacitor [48], and a $V_\pi L$ of 2.8 V·mm using graphene/Si hybrid MOS capacitor [80], both of which use 10nm SiO_2 as the gate oxide.

Only until recently, there have been resonator-based silicon modulators using MOS or hybrid MOS configurations [19], [26], [33], [34], [197]. The over-all performance still cannot compete with the best reversed p-n junction modulators because of the relative large capacitance and poor overlapping between carrier and optical mode due to increased fabrication complexity. However, by improving the overlapping factor using advanced slot waveguide structures [190], [191], the MOS capacitor can potentially achieve better energy efficiency than p-n junction.

7.4 Trade-off between bandwidth and energy efficiency

Although the energy efficiency has been the primary driving force for future on-chip optical interconnects, the bandwidth is still the most basic requirement for an E-O modulator. A minimum data rate of 25Gb/s is expected, which means the E-O modulator should operate at the frequency above 10GHz. The bandwidth of a resonator-based modulator is determined by both the optical bandwidth and the electrical modulation bandwidth. The optical bandwidth is limited by the photon life time of the resonator cavity, which can be extracted by the Q-factor of the resonator by

$f_{opt} = f/Q$, where f is the resonance frequency of the resonator. The electrical bandwidth is determined by the RC time delay constant $\tau_{RC} = RC$, by $f_{el} = 1/(2\pi\,\tau_{RC})$. Then the total 3dB bandwidth can be calculated as $(1/f_{3dB})^2 = \left(1/f_{opt}\right)^2 + (1/f_{el})^2$. Contrary to the energy efficiency, the bandwidth of an E-O modulator decreases as increasing the Q-factor and the RC time constant, which is proportional to the Purcell factor ($1/f_{opt} \propto Q \propto F_p$) and capacitance ($1/f_{el} \propto \tau_{RC} \propto C$), respectively. Then, we can get the general relationship between the energy efficiency and bandwidth from (7.12) as

$$E_{bit} \propto f_{opt}^2 f_{el}. \tag{7.17}$$

Clearly, there is an intrinsic trade-off between the bandwidth and the energy efficiency. For certain 3dB bandwidth, we can also obtain the optimized relationship between the optical bandwidth and electrical bandwidth to minimize the energy consumption as $f_{el} = \sqrt{2} f_{opt}$. At this minimum energy consumption condition, the total power consumption P scales with the fourth power of modulation bandwidth as $P \propto f_{3dB}^4$. Therefore, in order to keep the total power consumption at acceptable levels while scaling up the modulation bandwidth, it becomes especially critical to reduce the energy consumption per bit.

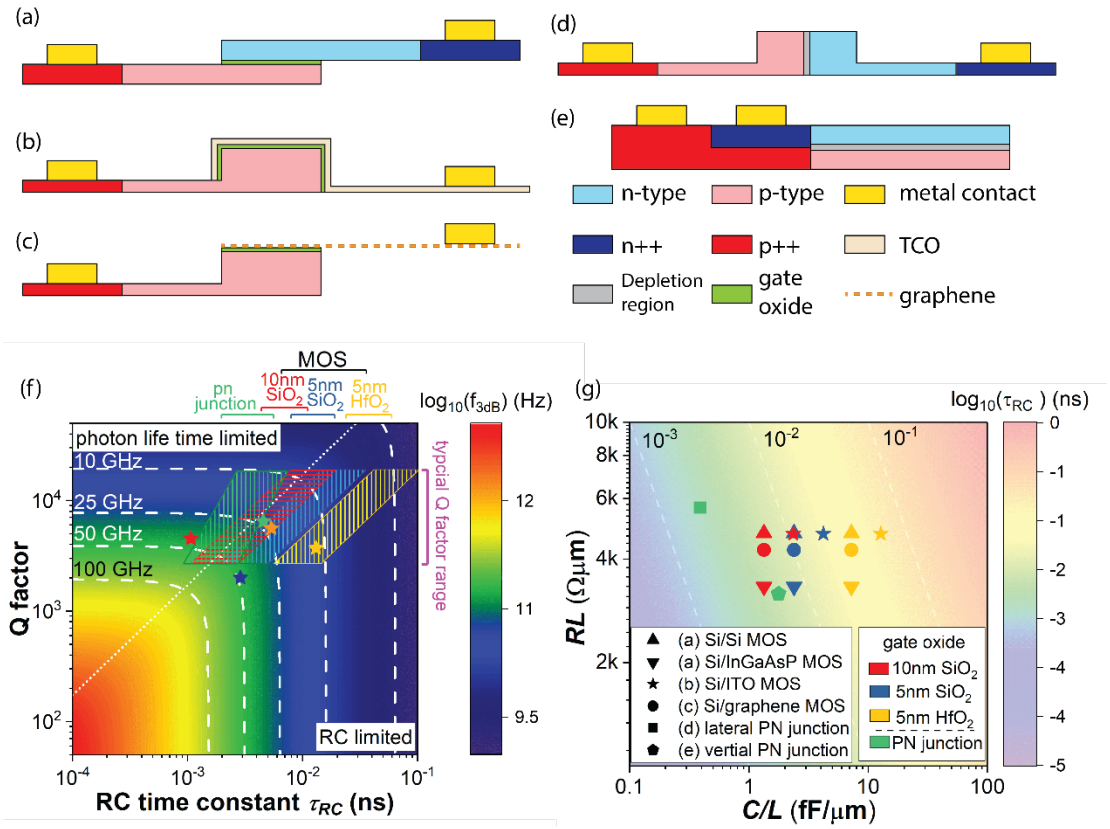

Figure 7.6 (a)-(e) Waveguide cross sections of typical silicon or silicon hybrid modulators: (a) Si MOS or III-V/Si MOS, (b) Si/TCO MOS, (c) Si/graphene MOS, (d) lateral PN junction, and (e) vertical PN junction (micro-disk). (f) 3dB bandwidth as a function of RC time constant and Q factor at 1.55μm. Solid symbols: Q factor and RC time constant reported in ref [38] *(red), ref* [30] *(green), PC nanocavity modulator presented in section 4.2 assuming node-matched doping was used (yellow), PC nanocavity proposed in section 4.3.6 (orange), TCO-gated MRM proposed in section 5.2.4. (g) Capacitance per length and resistance-length product of waveguide cross sections shown in (a)-(e).*

The total capacitance of a waveguide-based modulator is proportional to the device length, while the total resistance is inversely proportional to the device length. Therefore, the RC time constant of a resonator modulator is almost independent of the resonator size or even type, which can simplify our comparison. The electrical bandwidth is indeed only determined by the electrical configuration of the waveguide cross section. Here we compare some typical electrical configurations of silicon or silicon hybrid E-O modulators by calculating the two metrics: capacitance per length (*C/L*) and resistance length product (*RL*). The cross sections of different configurations are illustrated in Fig 7.6a-7.6e. Three types of MOS configurations are considered

according to the gate materials: high-index semiconductors (Fig 7.6a) such as Si [195] and InAsGaP [48], [49], TCOs such as ITO (Fig 7.6b) [33], [34], and 2D material such as graphene (Fig 7c) [80]. 10nm SiO_2, 5nm SiO_2 and 5nm HfO_2 as gate oxide layer are calculated. Besides, Fig 7.6d shows the lateral p-n junction which is the most widely used in micro-ring modulators. Fig 7.6e plots the vertical p-n junction used in micro-disk modulators. For comparison, a waveguide core with height of 220nm and width of 500nm are chosen for all cases. Highly doped semiconductor regions and metal contact are placed 500 nm away from the core except for the vertical p-n junction in the micro-disk, in which the active region has a width of 1μm [30]. The slab cladding thickness in Fig 7.6b-7.6d is 60nm; and in Fig 7.6a and 7.6e, the moderately doped region has a thickness of 100 nm. All the moderately doped semiconductor regions (light blue and light red), which contributes to the majority of the resistance, have a doping level of 1×10^{18} cm^{-3}. The results are summarized in Fig 7.6g, where different symbols represent the cross-section configurations and different colors symbolize the capacitor configurations. We can see that the resistance-length product of different configurations doesn't vary too much, ranging from 3000~5500 Ω·μm. Since the resistance is the sum of both the n-side resistance R_n and p-side resistance R_p. Although n-type III-V semiconductor and graphene produce a lower R_n due to its larger carrier mobility, the total resistance is limited by the relatively large silicon resistance on the p-side. 20nm thick ITO gate with doping of 1×10^{20} cm^{-3} produces a similar resistance as the n-Si gate in Fig. 7.6a. While for the capacitance per length, different configurations produce values across over two orders of magnitude, so as the RC time constant.

Fig 7.6f plots the 3dB bandwidth of an E-O modulator as a function of the Q-factor and RC time constant at 1.55μm. The minimun energy consumption condition ($\sqrt{2}f_{opt} = f_{el}$) is indicated by the dotted line. The shadowed areas in Fig 7.6f mark the corresponding region of different electrical configurations versus typical Q-factor range. As discussed in section 7.3, the Q-factor is related to the size of the resonator and the doping induced loss. This offers us the freedom to control the Q-factor, typically ranging from a few thousand to ~10^4. For example, an E-O modulator

operating at 10GHz requires a Q-factor below 2×10^4. Because different parameters scale differently versus the doping concentration, such as free-carrier-limited Q factor $Q \propto N^{-1}$, resistance $R \propto N^{-1}$, p-n junction capacitance $C_j \propto N^{1/2}$ and MOS capacitance $C_{MOS} \propto N^0$, we can have the relationship between the free-carrier-limited Q factor and the RC time constant as $Q \propto \tau_{RC,junction}^2$ and $Q \propto \tau_{RC,MOS}$, which is represented by the slope of the shadowed area boundary. Generally, pn junction configurations have the smallest τ_{RC} due to the small capacitance density, which are suitable for high bandwidth application. However, the majority of the p-n junction region (green shadow area) is above the matching condition. This means the bandwidth of p-n junction driven modulator is always limited by the optical bandwidth, while some of the electrical bandwidth is actually wasted. The red star in Fig 7.6f labels the recently demonstrated 128Gb/s micro-ring modulator [38]. The capacitance per length still has the potential to increase for better energy efficiency. The green star labels the micro-disk modulator with vertical p-n junction in [30], which shows a balance between optical bandwidth and electrical bandwidth due to the large capacitance density of the micro-disk resonator design and vertical junction. It is similar for MOS configurations with 10nm SiO_2 gate oxide layer. The corresponding region (red shadow area) shows good overlapping with the mininmun energy consumption condition for a wide bandwidth up to 50GHz. For example, a Q-factor of 10^4 and a RC time constant of 10 ps would be desired for an E-O modulator operating around 15GHz. Increasing the capacitance density by reducing the gate oxide thickness can improve the energy efficiency based on previous discussion, however, we have to sacrifice the bandwidth due to the increased τ_{RC}. For the example of 5nm HfO_2 gate oxide MOS, based on the assumption of 1×10^{18} cm^{-3} doping concentration, it will limit the electrical bandwidth to a few GHz. Further increasing the bandwidth requires the reduction of the series resistance, usually at the cost of reduced Q factor. PC nanocavity offers a unique advantage over micro-ring and micro-disk in this aspect. Because of the standing wave pattern in a PC nanocavity, we can use the mode-matched doping method by highly doping the anti-node (low energy region) [35] to reduce the distance between the highly doped region and the active capacitor. This method may potentially reduce the

resistance by one order of magnitude without increasing the loss or reducing the Q factor. While this strategy cannot be applied to travel-wave resonators such as micro-ring and micro-disk. The yellow star in Fig 7.6f labels the estimated τ_{RC} of a PC nanocavity modulator presented in section 4.2 [34] assuming using the node-matched doping method. Which can achieve an operation speed larger than 12 GHz with 10nm HfO_2 gate oxide layer, however, the speed is still limited by the RC deley. Increasing the HfO_2 can further increase the bandwidth. The orange star labels the PC nanocavity modulator proposed in section 4.3.6. The operation bandwidth increases to ~23.5 GHz with 16nm HfO_2 gate insulator layer, which is more close to the balance condition between the bandwidth and energy efficiency, maintaining the potential to ahieve an attojoule/bit energy efficiency.The blue start labels the TCO-gated Si MRM design proposed in section 5.24, which has a 15nm thick SiO_2 gate insulator layer. Comparing with ref [38], such device design offers us the potential to achieve large operation bandwidth through a different route by using a low Q-factor resonator with large tuning efficiency. However, for that specific design, the advantage of low Q resonator is not yet fully utilized. Because, there is a large portion of the MOS capacitor on top of the silicon slab, as we can see from the difference between fig 5.9b and fig 7.6b, which doesn't provide efficient modulation to light while increases the RC delay. Therefore, the operation bandwidth of TCO-gated Si MRM still has room to be improved, however, significant engineering optimization is still needed. We want to mention again that the achievement of larger operation bandwidth will be at the cost of sacrificing the energy efficiency even at minimun energy consumption condition ($\sqrt{2}f_{opt} = f_{el}$).

7.5 Energy consumption of wavelength control and driving electronic integrated circuits

7.5.1 Wavelength control

In practice, in order to compensate the fabrication error and temperature fluctuation, active control of the resonance wavelength is always necessary. Thermal tuning is the

most widely used method. State-of-the-art integrated heaters based on embedded silicided c-Si can achieve a high tuning efficiency of ~1.6nm/mW (3.5μW/GHz) on 45nm CMOS platform [198]. For a micro-ring resonator based DWDM system with channel distance of ~1nm, it requires an average wavelength tuning range of ~2nm [140]. Then, it consumes ~1.25mW power for each micro-ring, which corresponds to energy efficiency of 50fJ/bit for 25Gb/s OOK channel and 10fJ/bit for 128Gb/s PAM4 channel. The thermal tuning efficiency can be further increased to 4.8nm/mW (1.67μW/GHz) by improving the thermal isolation between the resonator and the silicon substrate through topside silicon undercut-etching [199], which means ~3.3fJ/bit for 128Gb/s channel. However, better thermal isolation also increases the response time to sub-millisecond range. It would be chalenging to further reduce the energy consumption using thermal tuning. Alternatively, electrial wavelength tuning is much faster and more energy efficient. According to the analysis in section 7.3, we can optimize the electrical wavelength tunability based on (7.13). Large wavelength tunability (>250pm/V) that is comparable with thermal tuning can be achieved. For example, the micro-disk modulator in [30] can compensate 10°C temperature change using electrical tuning with power consumption less than 50μW. In section 5.1 of this dissertation, we presented a hybrid TCO-silicon MOS-structured micro-ring achieved extremely large wavelength tunability of 271pm/V and tuning range of 2nm with a negligible static power consumption of 0.16pW. This near-zero-energy wavelength tuning method can potentially replace the power-hungry thermal tuning in future on-chip optical interconnect systems.

7.5.2 Driving electric integrated circuits

According to the power break down analyis of a micro-ring based DWDM transmitter in [198], it is the driving electrical ICs that limit the total energy efficiency to 0.83 pJ/bit. There are two groups of ICs that consume most power: modulator driver (33% of total power) and timing-issue related ICs (55% of total power), such as phase-locked loop (PLL), clock distribution, serializer, etc. To reduce the energy consumpton of the modulator driver, it is essential to reduce the required driving voltage of the modulator

to eliminate the use of electrial amplifer. Such optimizaiton can similarly be done based on (7.14). The ideal case would be that the switching of an opitcal modulator can be comparable to fliping an electrical transistor [2]. For example, in section 4.2, we demonstrate a Si-TCO PC nanocavity modulator with 1V CMOS compatiable driving voltage. Further optimization can potentially reduce the driving voltage to ~0.5V. For the timing-issue related ICs, it can only be solved by optimizing the IC architecture, which is beyond the scope of this dissertation. Ref [2] provided a thorough review and insightful perspectives on this issue by pointing out that such timing-issue related energy disspation may potentially be eliminated by optical approaches, such as optical clock distribution and pulsed opitcal readout.

7.6 Summary and outlook

In this chapter, we developed a general model to quantitatively describe the energy efficiency of carrier-driven resonator-based silicon photonic modulators. Three most fundamental factors, namely the free carrier dispersion strength of the active materials, the Purcell factor of the resonators, and the electrical configuration of the capacitors, are identified as the most critical factors to achieve atto-joule/bit energy efficiency. The development of future atto-joule/bit modulators should consider one or all of these three aspects. We analyzed the approach of heterogeneous integration of silicon photonics with different active materials benefited from the enhanced free carrier plasma dispersion effect, which shows the possibility to improve the energy efficiency by 3~100×. We also proved that PC nanocavities surpasses micro-ring and micro-disk resonators in terms of Purcell factor, and MOS capacitor is more efficient than PN junction due to its larger, more scalable capacitance density and compatibility with other active semiconductor materials. Through the aforementioned investigation, we conclude the possibility theoretically to reach atto-joule/bit energy efficiency using existing carrier-driven resonator-based silicon photonic modulators.

In addition, we investigated the intrinsic tradeoff between the energy efficiency and bandwidth, which is caused by both the photon lifetime of the resonators and the RC delay product. To maximize the energy efficiency while still achieving high bandwidth,

both optical bandwidth and electrical bandwidth need to be carefully engineered. The use of MOS capacitor configuration offers additional design freedom to tune the capacitance density. It is shown that MOS capacitors with 10nm SiO_2 gate oxide layer offer a good balance between the energy efficiency and bandwidth up to 50GHz. Moreover, our model also guides the optimization of large electrical wavelength tunability and low driving voltage, which provides the possibility to eliminate the energy dissipation from thermal wavelength control.

To conclude, the modeling and simulation in this chapter laid a solid theoretical foundation for silicon photonic modulators to continue to play key roles in extreme scale parallel optical interconnects between on-chip cores and within multi-chip modules. However, to truly realize atto-joule/bit energy efficiency for the entire optical interconnect system, efforts are required to minimize or eliminate the energy consumption from wavelength tuning and electronic driving Ics in parallel to the photonic device advancement.

Chapter 8. Conclusion and Perspectives

In the dissertation, we investigate three types of E-O photonic devices by integrating TCOs on the silicon photonics platform: tunable meta-surfaces, TCO-gated silicon resonators, and all-optical switches.

In Chapter 3, an electrically tunable plasmonic subwavelength grating is presented. The grating consists of a metallic subwavelength slit array coupled with a Si/oxide/ITO MOS capacitor. Simulation shows large modulation depths of 32% and 56% can be achieved for transmission and reflection modes, respectively, through tuning the electron density in the 0.5nm thick ITO accumulation layer. The large tuning efficiency is enabled by the ENZ induced light confinement and absorption enhancement inside the ITO accumulation layer. We experimentally demonstrate a transmission modulation depth of 5% with SiO_2 as the MOS gate insulator, which matches with the simulation prediction. The small modulation efficiency is limited by dielectric strength

of SiO_2. Our calculation indicate that a high-k dielectric material gate insulator layer is necessary to complete tune the ITO accumulation layer into ENZ condition.

In Chapter 4 and Chapter 5, we develop a novel device platform of TCO-gated silicon resonators. In Chapter 4, an ultra-compact high-speed ultra-energy-efficient Si-TCO PC nanocavity modulator is presented. First, we show that TCOs can be perfect gate materials for silicon resonators due to the optical transparency and good electrical conductivity. Thus, we can take advantage of the small mode volume of a PC nanocavity by integrating it with an ITO/oxide/Si MOS capacitor, achieving an E-O modulator with an ultra-small modulation volume of ~0.02 λ^3. Then, we show that using high-k dielectric material, HfO_2, as gate insulator can significantly improve the capacitance density of the MOS capacitor, which reduces the driving voltage and energy consumption of the Si-TCO PC nanocavity modulator. We experimentally demonstrate an extreme large wavelength tuning of 250 pm/V, a CMOS compactible 1V driving voltage and 3 fJ/bit energy efficiency. Next, we conduct comprehensive investigation the operation speed of the Si-TCO PC nanocavity. By using silicon rib waveguide with carefully designed doping profile and high-speed coplanar electrodes, we achieve a 2.2 GHz operation bandwidth and 5Gb/s data rate. Finally, based on our analysis, we propose a strategy to extend the further extended modulation bandwidth of the Si-TCO PC nanocavity modulator to 23.5GHz by using node-matched doping and high mobility TCOs at gate material. We also show that we can reduce the capacitance of the modulator and improve the energy efficiency to hundreds of atto-joule per bit level by optimizing the MOS capacitor design with improved the overlapping factor. In Chapter 5, we apply TCO gate to silicon microring resonators for two applications. First, we demonstrate an electrical tunable microring filter driven by an ITO/HfO_2/Si capacitor, achieving an unprecedented wavelength tuning efficiency of 271pm/V and over 2 nm electrical wavelength tuning range. The filter can potential replace the conventional energy-consuming thermal tuning in microring WDM/DWDM systems. Next, we show that TCO-gated silicon microring can be optimized for high-speed operation. We demonstrate a silicon MRM driven by an ITO/SiO_2/Si MOS capacitor, achieving a large tuning efficiency of 95pm/V with a low

Q-factor of 1000 and 1GHz AC modulation. Our analysis indicates that with optimized metal contact design and high mobility TCO gate material, the bandwidth of the MRM can be increased to over 52 GHz, overcoming the speed limit of the conventional Si MRM.

In Chapter 6, a sub-micron, sub-picosecond, femtojoule level AOS driven by high mobility TCO, CdO, is proposed. The AOS device consists of an electrically tunable plasmonic-CdO-Si waveguide, which can be precisely biased at the ENZ "OFF" state. Our transient simulation shows that the AOS device can be switched to the "ON" state with an unprecedented modulation strength of 15.9dB/μm and a rapid switching time of 230fs at the cost of an ultralow switching energy of 13.5fJ. Our simulation results also indicate that the high free carrier mobility of CdO plays a pivotal role in achieving such superior performance and deserve future experimental investigation. Finally, by defining a comprehensive metric using the product of device size, switching energy and switching time, the proposed AOS device shows superior performance than any existing on-chip AOS device, which can be integrated with silicon PIC to realize on-chip optical signal process and computation.

In addition to the device research, in Chapter 7, we systematically analyze the energy efficiency and bandwidth limit of resonator-based silicon photonic modulators. First, we develop a general model to quantitatively describe the energy efficiency of carrier-driven resonator-based silicon photonic modulators from three fundamental perspectives: free carrier dispersion strength of the active materials, Purcell factors of the resonators, and electrical configuration of the capacitors. Our analysis indicates that the Si-TCO PC nanocavity modulator presented in this dissertation, which combines the advantages of large refractive index tunability of TCO, large Purcell factor of PC nanocavity, and large capacitance of MOS capacitor, is the most promising approach to real atto-joule/bit energy efficiency. Next, we investigated the intrinsic tradeoff between the energy efficiency and bandwidth. We conclude that to maximize the energy efficiency while still achieving high bandwidth, both optical bandwidth and electrical bandwidth need to be carefully engineered. The modeling and analysis lay a theoretical foundation for future silicon photonic modulator design.

To conclude, TCOs could play an important role in the development of future photonics technology, which provide a CMOS compatible solution to overcome the intrinsic weak E-O effect of the silicon photonics platform, lead to unprecedented reduction in energy consumption, increasing bandwidth, as well as enable novel functionalities. Based on the aforementioned results, here we list some potential directions for the future researches, which may include, but not limited to, the following perspectives. First, from the device perspective, the experimental demonstrated TCO-driven devices in this dissertation still have large room to be improved. For the tunable plasmonic subwavelength grating, replacing the gate insulator with high-k dielectric material is necessary to reach ENZ condition for the TCO accumulation layer. For the Si-TCO PC nanocavity modulator, in order to truly achieve atto-joule per bit energy efficiency and desired high bandwidth, significant engineering effort is still required in optimization of the electrical design to reduce the series resistance and improve the overlapping factor, as well as for the TCO-gated silicon MRM. Next, from the application perspective, efforts should not be only focused on single devices. Integrating the TCO-driven active devices with photonic foundry fabricated silicon PIC and potentially CMOS driving circuits to achieve practical photonic systems is waiting to be demonstrated. Finally, from the TCO perspective, developing TCO with higher mobility is desired. As is discussed through this dissertation. Free carrier mobility plays a critic role for TCO-driven devices. On one hand, higher mobility means better electrical conductivity and lower optical loss, which can be used to increase the Q factor and reduce resistance of TCO-gated silicon resonator devices. On the other hand, high free carrier mobility enhances the ENZ related effects, such as light confinement and absorption enhancement, and is essential for the high energy efficiency AOS application.

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