AN ABSTRACT OF THE DISSERTATION OF

Jinyong Kim for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on August 30, 2021.

Title: New Techniques for Multi-Channel Biosignal Acquisition and Low-Power, Low-Resistance-Measurement Systems

Abstract approved: _____

Matthew L. Johnston

Dense electrical recordings of biosignals has been developed to provide spatial resolution and precise temporal information for health monitoring, diagnostics, and clinical research. However, more electrodes require more wires, and wiring density quickly becomes a limiting factor. To break this bottleneck, we proposed a frequency-division multiplexing (FDM) based architecture for multi-channel acquisition systems. In this dissertation, I present two applications that make use of this FDM technique. The first is an FDM-based multi-channel electromyography (EMG) acquisition system, which demonstrates that the FDM system not only reduces wire count, but also mitigates the effect of low frequency motion artifacts and 50/60 Hz mains interference introduced in the wire. An FDM-based four-channel EMG recording is demonstrated, while carrying all channels over a 3-wire interface, and the system achieves an attenuation of low-frequency cable motion artifacts by 15X and 60Hz mains noise coupled in the cable by 62X. A second application that forms the basis of my current research

effort is an FDM-based neural recording system with multiple graphene active electrodes. We demonstrated a two-channel system including graphene FET electrodes, a custom integrated circuit (IC) analog front-end (AFE), and digital demodulation.

In related multi-channel sensor work, a growing need for ultra-low-power sensors has driven continuous advancement in read-out circuits for temperature, humidity and pressure. IC-integrated Wheatstone bridges, commonly used, are efficient for large sensor resistance (5 $k\Omega$ - 500 $k\Omega$), but measuring small resistance ($<$ 1 $k\Omega$) with low power remains a fundamental challenge. In this dissertation, I present an approach that uses a duty-cycled resistor and auto-balancing frequency-locked-loop to decrease power consumption. Measured IC results demonstrate 2X - 10X lower area and similar power consumption despite >30,000x smaller nominal sensor resistance.

New Techniques for Multi-Channel Biosignal Acquisition and Low-Power, Low-Resistance-Measurement Systems

by

Jinyong Kim

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Head of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Jinyong Kim, Author

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Chapter 1: Introduction

In the past couple of decades, biosensors have been rapidly developed by exponentially decreasing the scale of complementary metal-oxide-semiconductor (CMOS) processes, which enables integration of a large number of sensing array and readout circuits to analyze signals of multi-channel in biochips. And these dense electrical recording systems of biosignals have been developed to provide spatial resolution and precise temporal information for health monitoring, diagnostics, clinical research, and brain-computer-interface (BCI) applications [2, 3, 4]. However, more electrodes require more wires, and wiring density quickly becomes a limiting factor. To break this bottleneck, multiplexing techniques, which have been used in communication field for some time, have started to apply more directly to sensing systems.

In this dissertation, I present three different applications based on a frequency-division multiplexing (FDM) for multi-channel signal acquisition systems. The first is an FDM-based multi-channel electromyography (EMG) acquisition system, which demonstrates that the FDM system not only reduces wire count, but also mitigates the effect of low frequency motion artifacts and 50/60 Hz mains interference introduced in the wire. An FDM-based four-channel EMG recording is demonstrated, while carrying all channels over a 3-wire interface, and the system achieves an attenuation of low-frequency cable motion artifacts by 15X and 60Hz mains noise coupled in the cable by 62X. The second is an FDM-based biopotential signal acquisition

system for extended scalability, which is an enhanced version of the first architecture. This approach not only extends the modulation frequency bandwidth by more than 3X using a harmonic cancellation, but also enables one-wire operation with a single ADC. Lastly, A third application is an FDM-based neural recording system with multiple graphene active electrodes. We demonstrated a two-channel system including graphene FET electrodes, a custom integrated circuit (IC) analog front-end (AFE), and digital demodulation.

In related multi-channel sensor work, a growing need for ultra-low-power sensors has driven continuous advancement in read-out circuits for temperature, humidity, and pressure [5, 6, 7]. IC-integrated Wheatstone bridges, commonly used, are efficient for large sensor resistance (5 $k\Omega$ - 500 $k\Omega$), but measuring small resistance (< 1 $k\Omega$) with low power remains a fundamental challenge. In this dissertation, I present an approach that uses a duty-cycled resistor and auto-balancing frequency-locked-loop to decrease power consumption. Measured IC results demonstrate 2X-10X lower area and similar power consumption despite >30,000x smaller nominal sensor resistance.

This remainder of this dissertation is organized as follows: Chapter 2 introduces a background of the multiplexing techniques; Chapter 3 describes the FDM-based, 4-channel EMG acquisition system; Chapter 4 describes an FDM-based biopotential signal acquisition system with a wider modulation frequency bandwidth; Chapter 5 presents FDM-based neural recording system with graphene-FET-based sensor array; Chapter 6 presents ultra-low-powered low resistance measurement system; and, Chapter 7 provides a brief summary and conclusion.

Chapter 2: Multi-Channel Background

2.1 Multi-channel biosignal acquisition systems

Multi-channel biosensors can be used to improve the overall sensitivity and resolution of the systems. For IC-based sensors, since the limited chip area restricts the number of available input and output pins, multiplexing techniques, which have long been used in communications, can be applied to the biochip sensing systems to increase channel count without increasing wire count.

2.1.1 Overview of multiplexing techniques

Depending on the operating environment and application, different kinds of multiplexing techniques have been applied to arrays of biosensors. Broadly, time-division multiplexing (TDM), frequency-division multiplexing (FDM), and code-division multiplexing (CDM) are three of the most commonly used approaches for biosensing and bioelectrical measurement applications. In addition, $\Sigma\triangle$-modulation-based multiplexing has more recently been adapted for use with biosensing arrays. This section briefly introduces the four multiplexing approaches.

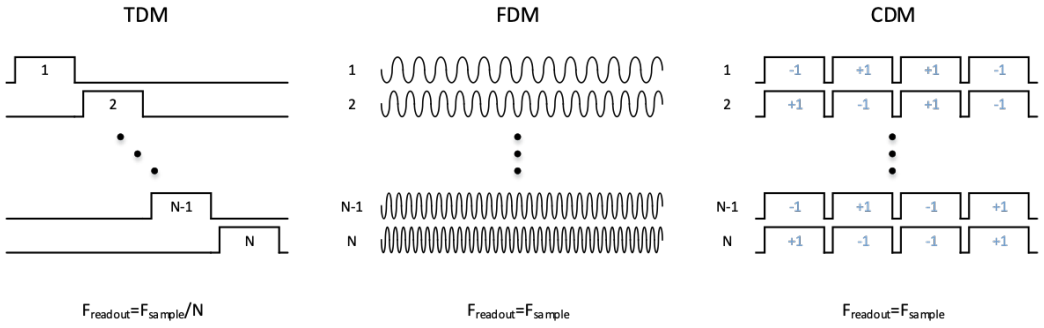


Figure 2.1: Multiplexing techniques: time-division multiplexing (TDM), frequency-division multiplexing (FDM), and code-division multiplexing (CDM).

2.1.1.1 Time-division multiplexing (TDM)

Time-division multiplexing (TDM) technique has been commonly used for large sensing arrays [8, 9, 10]. This multiplexing approach comprises periodic sets of time slots, and the sensed signal of each sensor is sequentially allocated to the multiple small time slots. For example, four signals generated from four sensors can be temporally shared to one wire through a simple binary counter and MUX. In this example, the required clock frequency is four times of the sampling frequency. On the de-multiplexing side, the original signals of each sensor are reconstructured using a recovery clock, which is operating in the same frequency as the sampling clock. The biggest advantage is that the design implementation of TDM is straightforward. Also, since there is only one signal per time slot, ideally there is no interference or crosstalk from other signals. However, when the number of sensing channels increases, wide dynamic range of time is required, which reduces the data processing speed because the recovery frequency is proportional to the number of channels.

2.1.1.2 Frequency-division multiplexing (FDM)

Frequency-division multiplexing (FDM) is a technique in which multiple, non-overlapping frequnecy bands placed using respective different high frequency carriers are allocated across the available bandwidth of the system. These multi-bands, with the original sensing signals, are demodulated trough several processing methods including programmable bandpass filters, mixing and downconversion using a target carrier, and so on. This technique is straightforward to implement in circuitry when the number of sensors is not too large. And, unlike TDM, this approach can simultaneously recover the data from across all channels continuously, which means no missing signal sampling as in TDM. However, the available dynamic range is finite due to the input limitation in the circuit. Furthermore, in digital processing, the limited sampling rate causes the digital error to be proportional to the sampling speed [11]. Increasing the number of sensors using FDM also causes the interference from other sensors to increase. To deal with the unwanted signals and cross-talk, careful design of high precision circuits is required.

2.1.1.3 Code-division multiplexing (CDM)

Code-division multiplexing (CDM) technique is based on the use of spread spectrum encoding, which is made by a pseudo-random sequenced signal. At the demodulation side, the original sensing signals are demodulated by the same code used in the modulation side. This technique has been mainly used for wireless communication

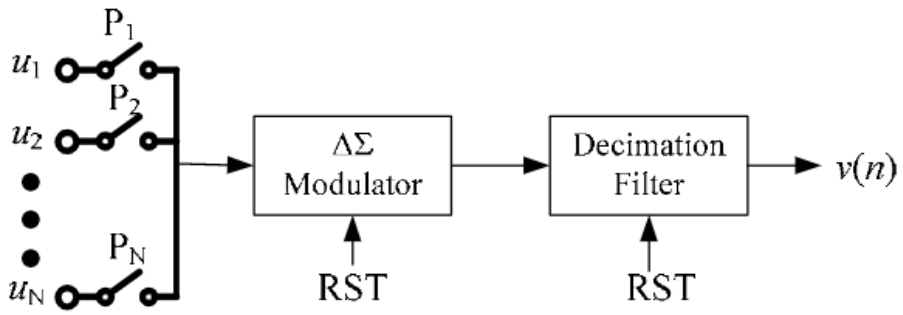


Figure 2.2: Block diagram of a multiplexed incremental ADC [1].

systems, but has also recently been used for the large sensing arrays as the number of sensors exponentially increases [12, 13, 14]. Because the desired signal tones are spread like white noise, the original signals can be recovered from CDM spread spectrum signals without mutual interference from other sensors; this is the main advantage of CDM. On the other hand, the disadvantage of CDM is that the CDM signal has much larger bandwidth than the sensing signal and more complex circuitry is required.

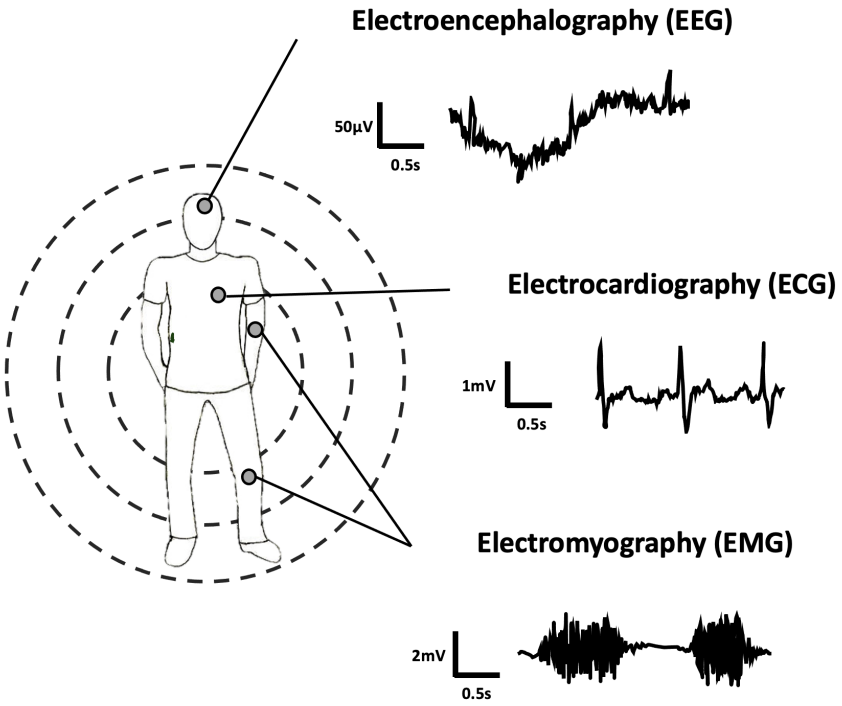
2.1.1.4 $\Sigma\triangle$-modulation-based multiplexing

The incremental ADC (IADC), which is a $\Sigma\triangle$ ADC, has been successfully used to detect biological signals, such as EEG and ECG. IADC provides very precise conversion with high linearity, accurate gain, and low offset [15]. As shown in Fig. 2.2, there are two resets applying to $\Sigma\triangle$ modulator and decimation filter. Using these periodic resets, the time-division multiplexing (TDM) technique can apply a single IADC to multiple sensor or signal channels [1]. However, the performance of IADC can be degraded when multiplexing between multiple input channels.

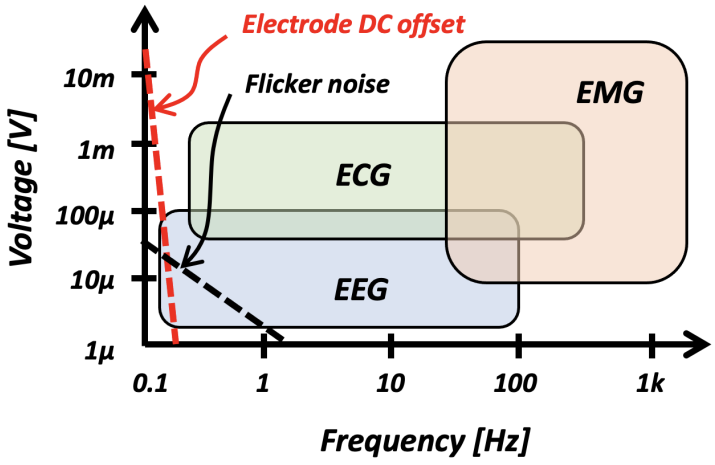
Chapter 3: Fully-Integrated, FDM-based Multi-Channel Biopotential Acquisition System with Cable Motion Artifact Suppression

3.1 Introduction

Biopotential readout systems using non-invasive and comfortable electrodes can indirectly record the biosignals, such as multi-electrode electromyography (EMG), electrocardiography (ECG) or electroencephalography (EEG), shown in Fig. 3.1, for a variety health monitoring, diagnostic, clinical research, and brain-computer-interfaces (BCI) applications [2, 3, 4]. Multi-channel acquisition enhances spatial accuracy and physiological information. For instance, a 12- or 24-lead ECG system is generally used for diagnosis of cardiovascular disease [16, 17], and in recent years, multi-channel ECG measuring systems with more than 24 leads have been developed to obtain increasingly in-depth information of cardiac activity [18]. Similarly, in both intramuscular and surface EMG technologies, multi-channel EMG recording provides a rich information stream for EMG decomposition [19, 20]. However, adding more channels increases the number of cables that connect from surface electrodes to readout instrumentation, which may not only impede ambulatory use, but may also be physically limited. In addition, electrode cables introduce motion artifacts and are subject to mains interference due to low-frequency biopotential signal bandwidth ($\sim$1 Hz$-$150 Hz) and micro-volt signal amplitude (Fig. 3.1(b)). For example, motion artifacts introduced



(a)



(b)

Figure 3.1: Biopotential signals; electromyography (EMG), electrocardiography (ECG), and electroencephalography (EEG).

in long-term recording (1-24 hours or longer) ExG recording in children and infants [21, 22] are a critical bottleneck that limits the performance.

To mitigate noise introduced in the cables connecting electrode and readout instrumentation, first-stage amplification can be performed at the electrode site. In such an active electrode (AE) arrangement, as shown in Fig. 3.2a, a front-end instrumentation amplifier (IA) [23, 24] is located close to the electrodes. A high gain amplifier (>40 dB) is typically required in each AE to reduce the cable motion artifacts and other cable noise sources. This one-to-one AE approach, however, still requires a large number of cables, and several additional approaches have been developed to decrease the size of the required cable bundle.

Digital active electrodes (DAE) provide near-electrode analog-to-digital conversion and all-digital communicating with back-end (BE) readout instrumentation, minimizing cable count and providing high noise immunity [25]. However, this introduces a significant increase in power and area, where each DAE includes an IA, a low-pass filter (LPF), an analog-to-digital converter (ADC), and a digital communication interface. As an alternative approach, frequency modulated frequency-division multiplexing (FM-FDM) is presented in [26], which reduces the number of ADCs and required cables, but alternatively requires off-chip inductors to minimize VCO phase noise and to meet required bandpass amplifier response, and increasing power consumption due to high-frequency modulation. Such approaches may limit scaling for multi-channel ExG applications requiring dozens or more electrodes, such as high-density EMG and high-resolution EEG.

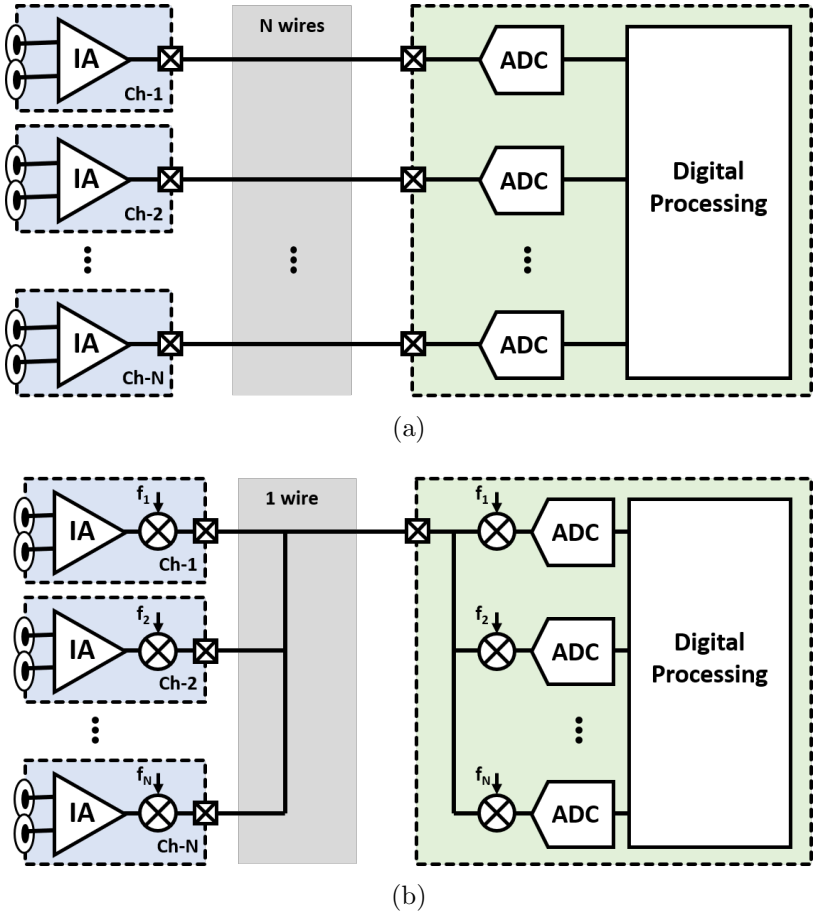


Figure 3.2: Block diagram of differential N-channel biopotential acquisition system: (a) Typical active electrodes (AEs) and (b) Proposed FDM-based active electrodes (AEs).

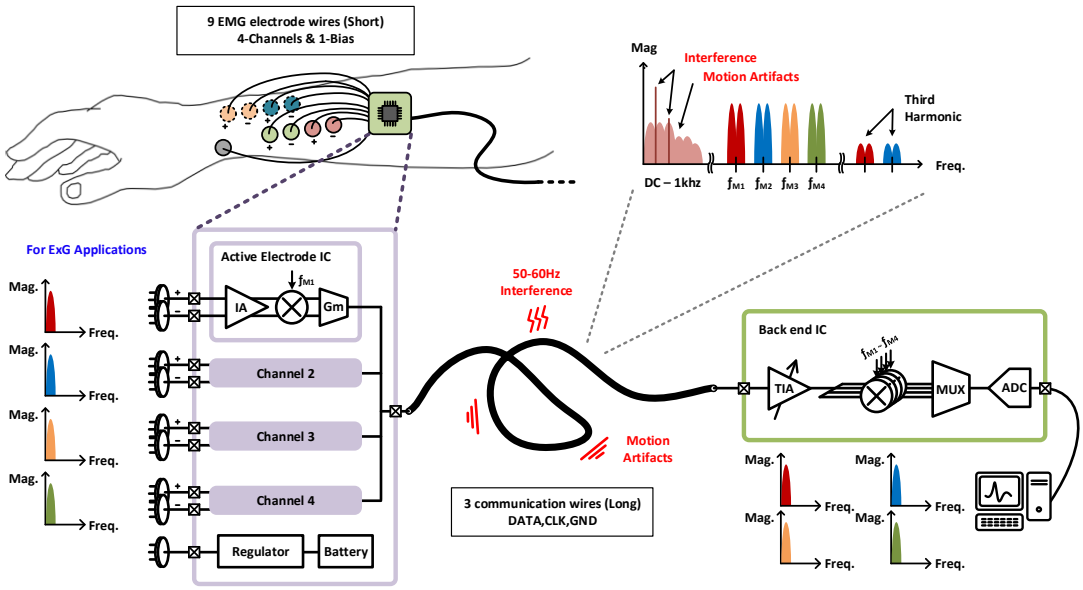


Figure 3.3: High-level architecture of the FDM-based four-channel EMG signals readout system with short nine-electrode wires and long three-communication wires, minimizing low frequency noise and motion artifacts and reducing wire counts.

3.1.1 Frequency-Division-Multiplexing-based Multi-Channel Readout

In this work, I present an alternative approach leveraging amplitude-modulated FDM to build a fully-integrated, highly scalable biopotential acquisition architecture towards the development high-density ExG readout platforms. As illustrated in Fig. 3.2b, this approach combines multiple input signals on a single wire by modulating them at different frequencies, where upconversion also separates the signals from low-frequency cable noise artifacts, which include both motion artifacts and noise injection from mains interference (50/60 Hz). In addition, back-end signal demodulation prior to digitization enables the use of a lower-speed ADC and simplified filtering, and unlike TDM, all signals are sent simultaneously over a three-wire cable bundle without

requiring an AE-side switch matrix.

3.2 FDM-based Four-Channel EMG Acquisition System Overview

The high-level architecture of the FDM-based ExG readout system is illustrated in Fig. 3.3, where multi-channel electromyography (EMG) is used as an example application. Four AE channels are integrated in a single front-end die and powered by a battery. Each differential surface electrode pair connects to an AE through short (centimeter-scale) wires. The modulated and summed current output of the four-channel AE-IC is connected to input of the BE-IC through a single, long wire (meter scale), with two additional wires carrying ground and a shared reference clock. Up-conversion mitigates both motion artifacts and mains interference in the connecting cable. The BE-IC performs current-to-voltage conversion, frequency demodulation, and on-chip digitization. A final, off-chip digital processing step includes finite impulse response (FIR) low-pass filtering for final signal reconstruction.

This FDM-based approach needs only three communication wires: a single data line for frequency-modulated, summed, current-mode electrode signals; a reference clock for the modulation up-mixer in the AE-IC and the demodulation down-mixer in the BE-IC, generated from an internal relaxation RC oscillator in BE-IC; and, a shared common ground between AE and BE. As the number of electrode channels increases, the required number of wires remains the same.

While scalable, two practical factors of this system will limit the maximum number of adjacent signal channels. First is the required dynamic range (DR) of the com-

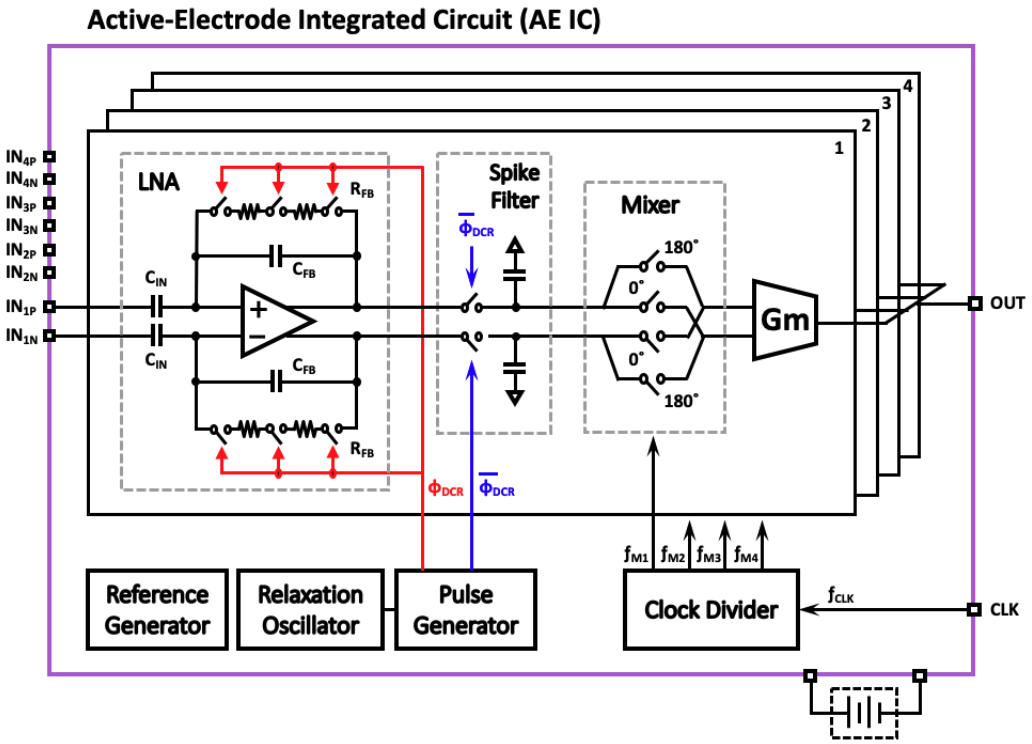


Figure 3.4: Block diagram of four-channel active electrode integrated circuit (AE-IC) used for electrode readout, up-conversion, and summing of modulated signal currents into a single, shared wired using FDM.

bined FDM signal voltage, where an amplitude-modulated signal can be saturated to the maximum voltage range, limited by the power supply rail. Second are overtones, specifically the third harmonic, generated from the lowest frequency modulation signal; the highest modulation frequency should be lower than this third harmonic to avoid overlapping a signal channel.

3.3 Active Electrode Integrated Circuit (AE-IC)

3.3.1 Overview

The architecture of the active electrode IC is shown in Fig. 3.4. A battery-powered AE-IC supports four active electrode channels, where each AE channel contains a low-noise amplifier (LNA) with duty-cycled resistive feedback used as an instrumentation amplifier (IA), a spike filter, a mixer to provide frequency modulation, and a transconductor to enable channel combining in the current domain. An RC relaxation oscillator generates a reference clock for the duty-cycle resistor (DCR) in the IA, and the clock frequency can be controlled by an external resistor, R_{EXT}. Using the reference clock, a pulse generator generates a pulse with a programmable duty cycle.

3.3.2 Capacitively-coupled Instrumentation Amplifier

As illustrated in Fig. 3.4, a capacitively-coupled instrumentation amplifier (CCIA) form the input to each active electrode channel. Capacitive coupling enables rail-to-rail offset rejection. The gain of CCIA is determined by the ratio the input capacitor (C_{IN}) and the feedback capacitor (C_{FB}). In addition, to attain a very low corner frequency ($\sim$1 Hz) in this architecture to support ExG signal acquisition, a large feedback capacitor (C_{FB}) and a large resistor (R_{FB}) are typically required. However, it is not practical to increase C_{FB} and C_{IN} in a limited circuit area while maintaining the required gain. To address this challenge, several architectures have been developed

to achieve a very large R_{FB} with limited circuit area. An active pseudo-resistor, using diode connected MOSFET transistors, is often employed to implement very large ($\gg$100 MΩ) on-chip resistance [27]. However, pseudo-resistors provide linear behavior only for very small signals. Alternatively, a duty-cycled resistor (DCR), as depicted in Fig. 3.5a, can be used to improve linearity and reliability across a larger signal range [28]. However, the DCR switch parasitic capacitance, C_p, may limit saturated maximum resistance to $R = 1/(f_1 C_p)$ [29].

In this work, I propose a multi-switching duty-cycle resistor (MS-DCR) [30], as illustrated in Fig. 3.5b, where switches are placed on either side of a center resistor, which extends the effective resistance range typically limited by DCR parasitic capacitance. When the switches are turned off, they induce charge sharing with symmetric parasitic capacitors, C_p, and when the switches are turned on, only the divided charge goes into the load capacitor, C. Cascading multiple stages, as illustrated in Fig. 3.5c, including in each a switch and a resistor with $R/2N$ resistance, can theoretically approach the ideal DCR resistance and eliminate the effect of C_p:

$$\frac{1}{R_{eq}} = \lim_{N\to\infty}\left(\frac{f_R \cdot C_p}{2^{N+1}} + \frac{D}{R}\right) \cong \frac{D}{R} \tag{3.1}$$

where R_{eq} is the equivalent resistance of the MS-DCR, f_R is a clock frequency for the switched resistor, C_p is a parasitic capacitance, N is the number of channels, D is the duty cycle of Φ_R defined by f_R, and R is a practical on-chip feedback resistance. As implemented in this work, the effective resistance using a 2-stage MS-DCR is 6X larger than achievable by a conventional DCR.

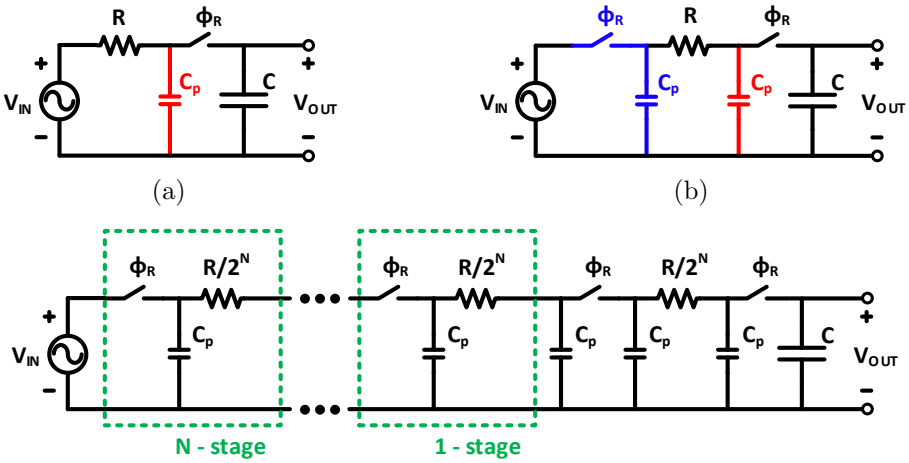


Figure 3.5: Instrumentation amplifier employing the improved duty-cycled resistor: (a) conventional; (b) double-switching duty-cycled resistor (DS-DCR); and, (c) multi-switching duty-cycled resistor (MS-DCR).

For the active electrode, the CCIA is the primary noise contributor for the signal chain, as the input-referred noise of each following block is divided by the CCIA gain (>40dB) and becomes negligible. To minimize total noise of the CCIA, we implemented a two-stage amplifier with inverter-type differential pairs as a core amplifier of the CCIA [23]. As illustrated in Fig. 3.7, in the first stage of the core amplifier, the series-connected NMOS and PMOS inputs double the input transconductance of the amplifier without additional power consumption, where increased input transconductance can mitigate the input-referred noise of the amplifier. The second stage boosts the gain of core amplifier, and a common-mode feedback circuit is implemented to operate the fully differential amplifier.

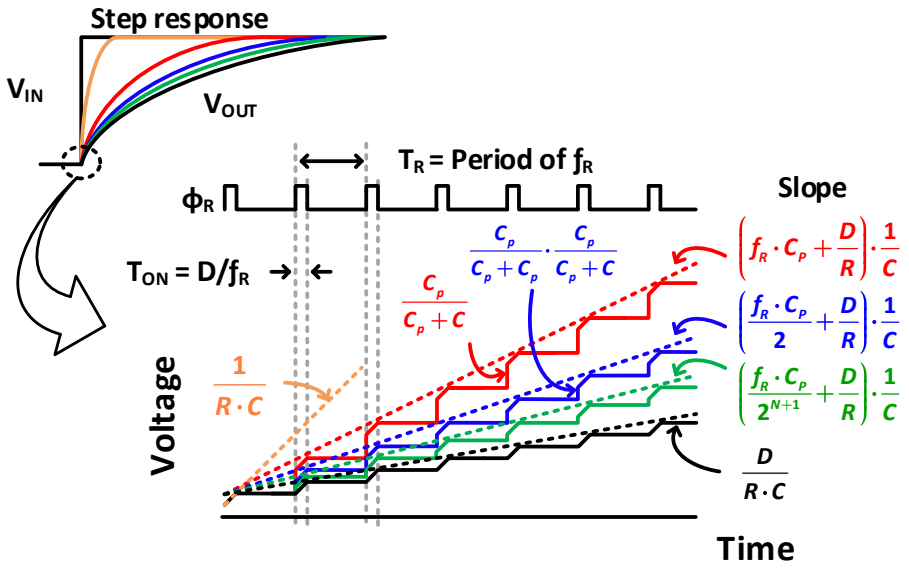


Figure 3.6: Step response characteristic of MS-DCR with increasing stages.

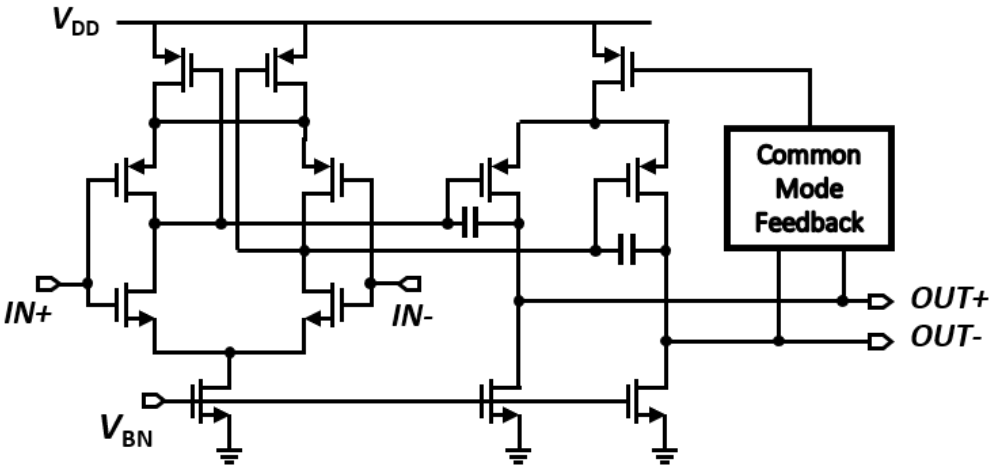
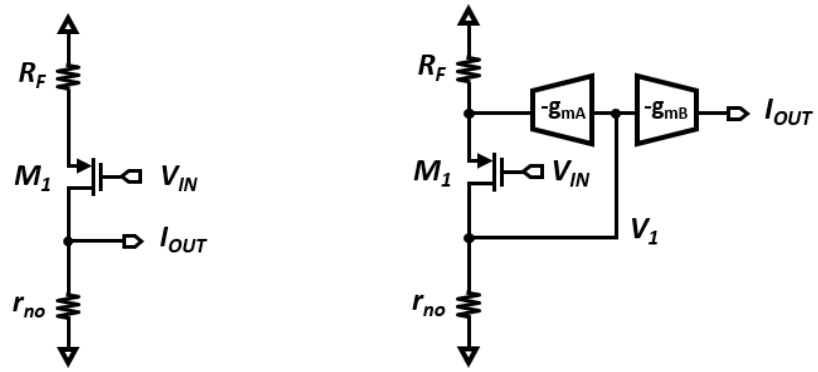


Figure 3.7: Circuit diagram of a two-stage inverter-type fully differential amplifier for LNA.



(a) (b)

Figure 3.8: Gm amplifier small signal model: (a) Conventional type; and (b) Negative feedback current-balancing type.

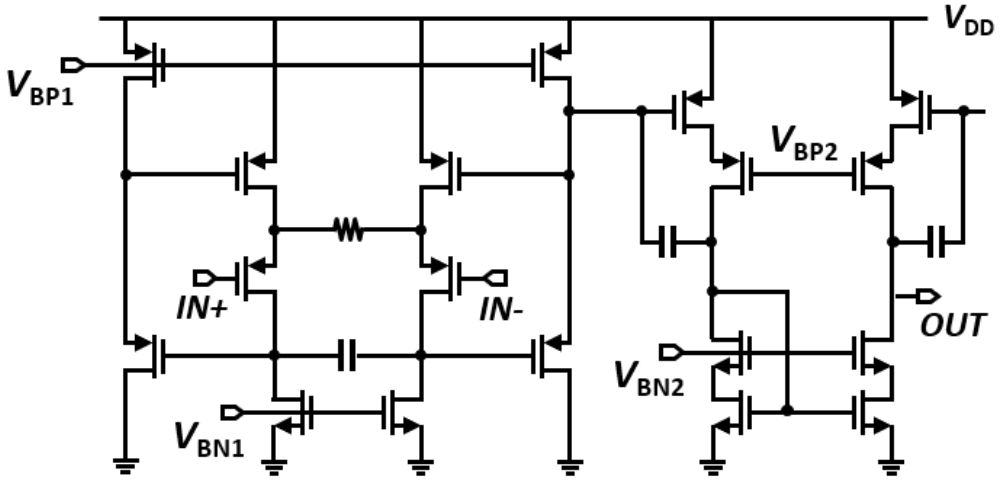


Figure 3.9: Circuit diagram of a Gm amplifier.

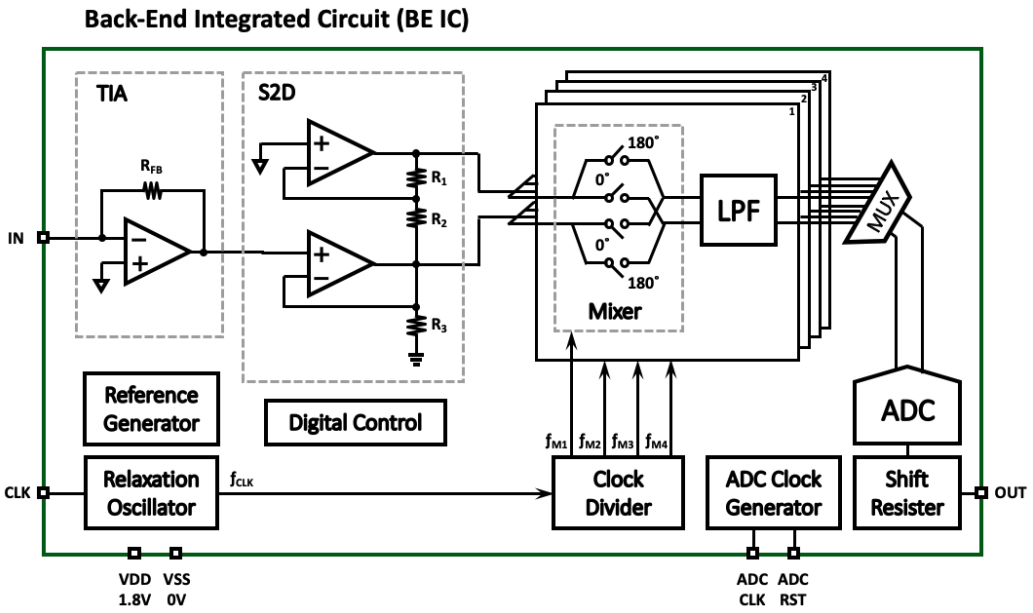


Figure 3.10: Block diagram of back-end integrated circuit (BE-IC) for demodulation and digitization of the summed FDM signal from the active electrodes.

3.3.3 Frequency Modulator

Each frequency modulator (one per AE channel) comprises a passive up-converting mixer and a current-balancing G_m amplifier. The up-converting mixer operates as a modulator with different per-channel modulation frequencies ($f_{M1} - f_{M4}$), where the modulation clocks are generated by an oscillator and a clock divider shared across all channels. The switches of the mixer use transmission gates with bidirectional resistive connections.

The transconductance, g_{mA}, of a conventional G_m amplifier using source degener-

ation (Fig. 3.8a), can be written as

$$G_{mA} = \frac{-g_{m1}}{1 + g_{m1} \cdot (R_F || r_{no})} \approx \frac{-g_{m1}}{1 + g_{m1} \cdot R_F} \tag{3.2}$$

where g_{m1} is the transconductance of input MOS (M_1), R_F is the feedback resistance used for source degeneration, and r_{no} is a drain-source resistance of a current source. For low power-systems, the transconductance of a conventional G_m amplifier is highly susceptible to PVT variation of the input g_{m1}, where $g_{m1}R_F$ does not greatly exceed unity.

An alternative G_m amplifier, implemented in our system, employs negative feedback in the first stage and adds an output g_m stage, as illustrated in Fig. 3.8b. The overall transconductance can be written as

$$G_{mB} = \frac{g_{mB}}{\frac{1+g_{m1} \cdot R_F}{g_{m1} \cdot r_{no}} + g_{mA} \cdot R_F} \approx \frac{g_{mB}}{g_{mA} \cdot R_F} \tag{3.3}$$

where g_{m1}, R_F, and r_{no} are as defined in (3.2), g_{mA} is the transconductance of a negative feedback g_m stage, and g_{mB} is the transconductance of an output g_m stage. Since $g_{m1}r_{no}$ is much larger than $1 + g_{m1}R_F$, we can ignore the $(1 + g_{m1}R_F)/(g_{m1}r_{no})$ term even for low-power systems. Therefore, the transconductance variation is determined by g_{mA} and g_{mB} matching, which is easier to control than absolute g_m across PVT variation. Fig. **??** shows the implemented circuit diagram, where an additional g_m stage is placed in negative feedback as a current-balancing amplifier [31].

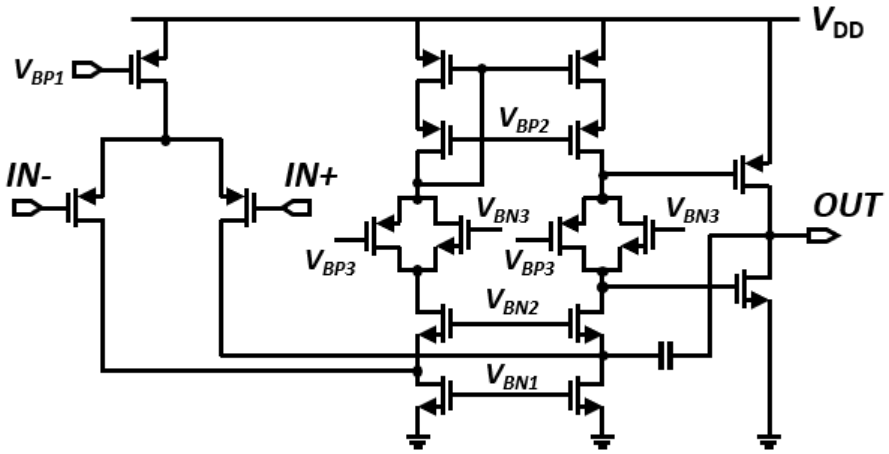


Figure 3.11: A circuit diagram of folded cascode amplifier with class-AB uffer

3.4 Back End Integrated Circuit (BE-IC)

3.4.1 Overview

The combined, multi-channel FDM current-mode signal from the active electrodes is sent over a single wire to the back-end IC (Fig. 3.3). As illustrated in Fig. 3.10, the FDM input is first converted to a voltage-mode signal by a transimpedance amplifier (TIA). A single-to-differential amplifier (S2D) converts the single-ended voltage to differential voltage for fully differential demodulation circuitry and analog-to-digital conversion (ADC). The demodulation clocks are internally generated by a RC relaxation oscillator and a clock divider, where the oscillator output is also sent via cable to the AE-IC for phase-aligned modulation and demodulation. Individual circuit blocks of the BE-IC are described here in more detail.

3.4.2 Transimpedance Amplifier and Single-to-Differential Converter

A transimpedance amplifier (TIA), which converts the summed input current to a voltage signal, has a gain determined by a value of $R_F B$. The TIA bandwidth is designed as 300 kHz to provide multi-channel modulation frequency range for kiloHertz-bandwidth ExG signals of interest. In this system, we implemented single-to-differential (S2D) converter with two single-ended amplifiers and three resistors [32] . The transfer function of the S2D circuit can be written as

$$\frac{V_{outp} - V_{outn}}{V_{in}} = \frac{R_1 + R_2}{R_3} \tag{3.4}$$

where V_{in} is the single-ended input, V_{outp} and V_{outn} are the differential outputs, and R_{1-3} are resistors that define the gain of S2D amplifier. Since R_{1-3} are designed to be same value, the gain is two in this system. Fig. 3.11 shows a schematic of a two-stage folded cascode amplifier implemented and used in both the TIA and S2D circuits. In order to increase drive strength, a class-AB buffer is applied to the amplifier [33].

3.4.3 Frequency Demodulator

The frequency demodulator for each channel consists of a down-converting mixer and a low-pass filter (LPF). For the down-conversion mixer, the combined, modulated signal from AEs is demodulated by four different demodulation frequencies ($f_{M1} - f_{M4}$) generated by a relaxation oscillator and a clock divider. Since the reference clock from the BE-IC oscillator supports both AE and BE, modulation and demodulation

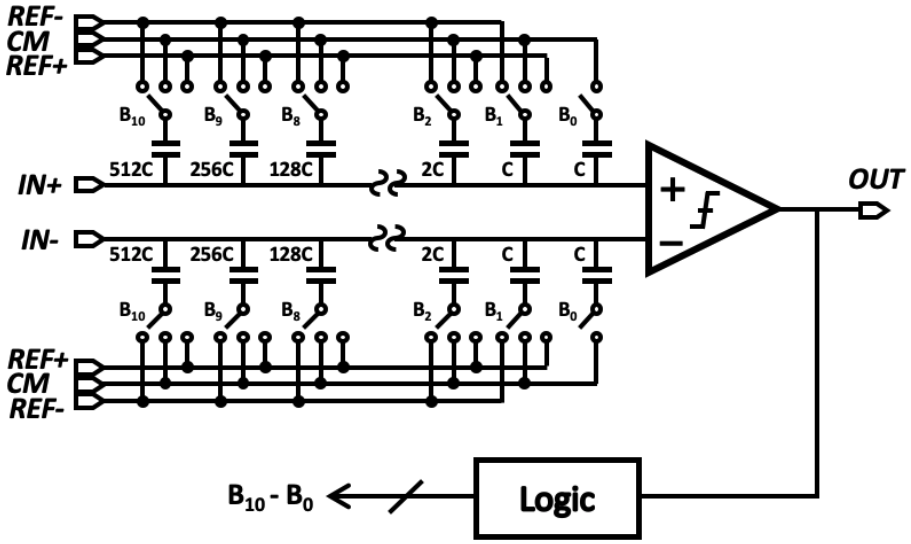


Figure 3.12: Implemented successive-approximation register (SAR) analog-to-digital converter(ADC).

frequencies are effectively synchronous, as the phase delay across the cable is negligible compared to the kiloHertz-scale clock frequency. There are four dividers with different division factors (2, 3, 5, 7) in the clock divider, so that the four different demodulation clocks are reproduced using the reference clock. As the demodulated signal still contains unwanted high-frequency harmonics of the demodulation frequency, a low-pass filter (LPF) follows the down-conversion mixer for filtering this high frequency noise. This filter also acts as an anti-aliasing filter for the ADC input.

3.4.4 Successive Approximation Analog-to-Digital Converter

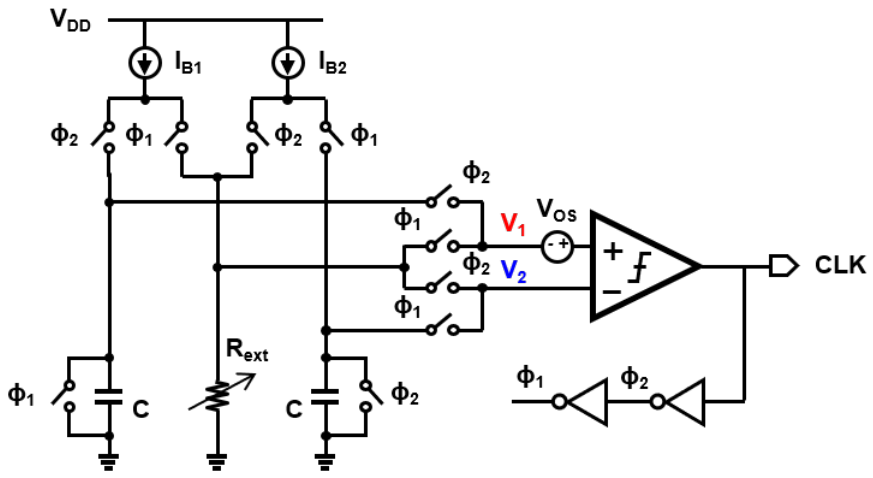
To digitize the demodulated signal selected by a 4:1 multiplexer (MUX), an 11-bit successive-approximation register (SAR) analog-to-digital converter (ADC) was im-

plemented in this system, as shown in Fig. 3.12. A SAR ADC has been used to provide low-power, moderate resolution data converter in many applications. As a smaller unit capacitance for the SAR capacitor array reduces power consumption, a 7 fF standard finger metal-oxide-metal (FMOM) capacitor was used as the unit capacitor in this work, instead of a metal-insulator-metal (MIM) capacitor structure with a larger minimum unit capacitance. Additionally, as switching within the capacitive digital-to-analog converter (CDAC) is a primary source of power consumption, a merged capacitor switching (MCS) topology was implemented to reduce switching energy in this work [34].

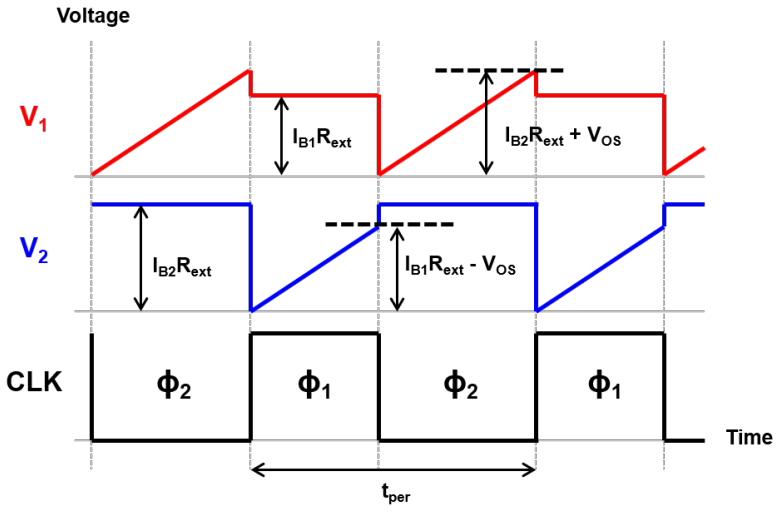
3.4.5 RC relaxation oscillator

An offset-compensated RC oscillator, shown in Fig. 3.13, was implemented for generating the system-wide modulation reference clock in the back-end integrated circuit. The oscillator architecture uses a switch matrix with two-phase operation to attenuate the offset of the comparator and to improve long-term stability of the oscillator for low-power systems [35]. Fig. 3.13a describes the architecture with the input-referred offset due to mismatch and process variation of the comparator, and Fig. 3.13b shows the timing diagram for this operation. The clock period, t_{per}, can be written as

$$t_{per} = (\frac{R_{ext} \cdot C_1 \cdot I_{B2}}{I_{B1}} + \frac{R_{ext} \cdot C_2 \cdot I_{B1}}{I_{B2}}) + V_{OS} \cdot (\frac{C_1}{I_{B1}} - \frac{C_2}{I_{B2}}) \tag{3.5}$$



(a)



(b)

Figure 3.13: Implemented RC oscillator; (a) circuit diagram, (b) timing diagram.

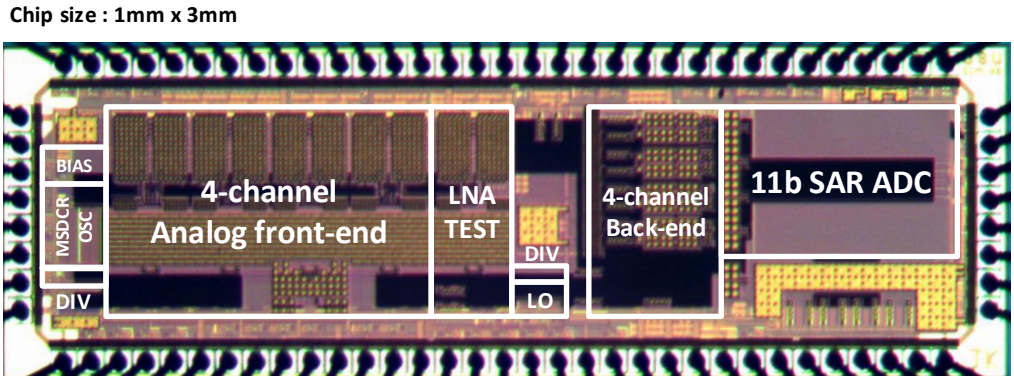
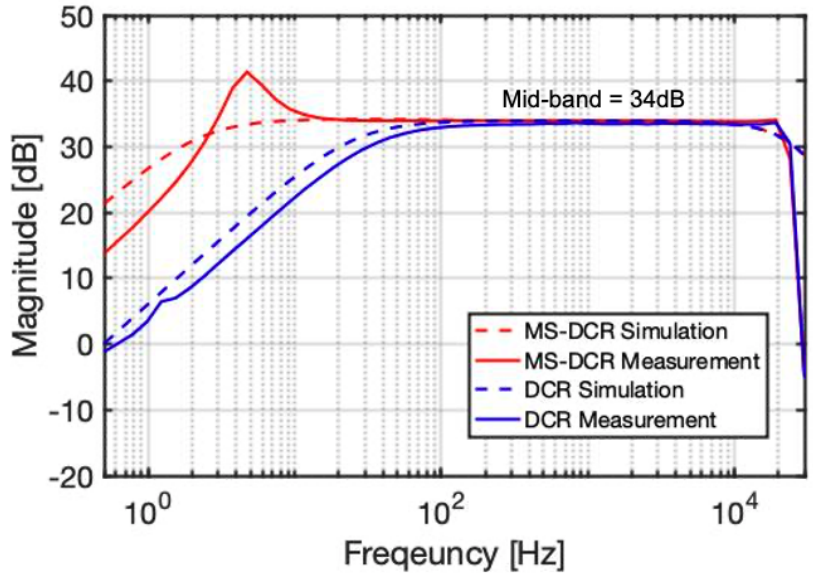


Figure 3.14: Micrograph of the AE-BE IC fabricated in 0.18 μm CMOS.

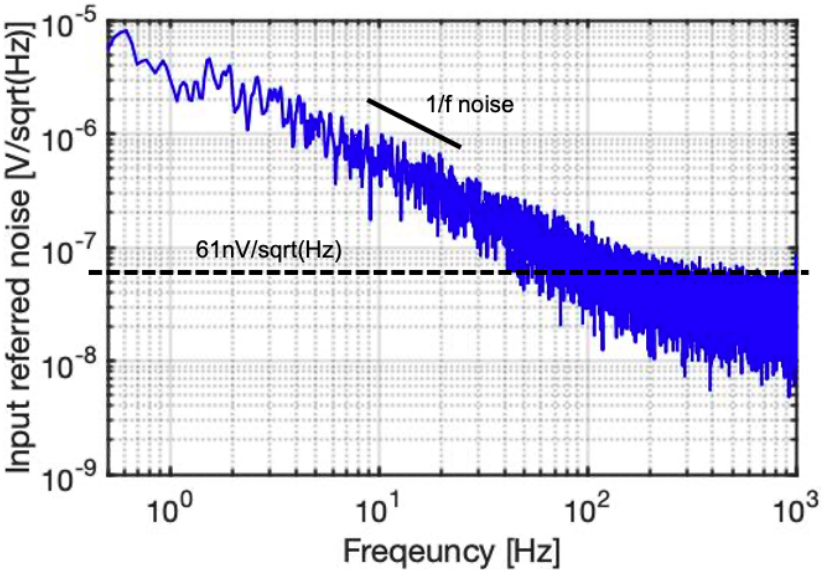
where R_{ext} is a variable external resistor, I_{B1} and I_{B2} are current sources, C_1 and C_2 are the capacitors, and V_{OS} is the comparator offset. The effect of this offset, V_{OS}, on t_{period} significantly decreases when the components (I_{B1} and I_{B2}, C_1 and C_2, respectively) are well matched.

3.5 Measurement Results and Discussions

A prototype of the four-channel FDM-based biopotential measurement system was implemented in a 0.18 μm silicon CMOS process, including active electrode (AE-IC) circuitry and back-end (BE-IC) readout architecture, with a total die area of 1mm x 3 mm; an annotated die micrograph is shown in Fig. 3.14. Both AE and BE were implemented in the same IC for fabrication, but separate dice were used to physically separate AE and BE over a cable during experimental testing.



(a)



(b)

Figure 3.15: (a) Measured and simulated AE LNA ac response with conventional duty-cycled resitor (DCR) and with proposed multi-switching duty-cycled resistor (MS-DCR); and, (b) measured input-referred noise of AE LNA.

3.5.1 Active Electrode LNA Characterization

The measured ac gain response for the active electrode LNA is shown in Fig. 3.15a. The mid-band amplitude of the LNA is 34 dB, and it demonstrates that the effective resistance of the proposed MS-DCR is 10X larger than is achievable by conventional duty-cycled resistance. The cutoff frequency can be adjusted by controlling the duty cycle of the switching clock. However, series-connected resistance boosting techniques such as MS-DCR can introduce a parasitic capacitor at the shared node, which creates an additional pole in the frequency response. For the MS-DCR measurement shown in Fig. 3.15a, this causes a resulting peak in the ac gain response near the cutoff frequency [36, 37]. This effect can be mitigated using various approaches [38]; one simple modification is to apply a bypass capacitor without added power consumption, and another approach is to employ an additional G_m amplifier in the negative feedback.

As measured, the total input-referred noise of the LNA from 1 Hz to 150 Hz is 3.52 μV_{rms}, where the input-referred thermal noise is 61 nV/$\sqrt{Hz}$ as depicted in Fig. 3.15b.

3.5.2 Active Electrode FDM Cross-talk

As with all FDM systems, cross-talk between channels is present due to modulation artifacts and harmonics located within the signal band of another channel. To measure cross-talk between channels, 1.4 mV_{rms} 50 Hz and 100 Hz sinusoidal waves were applied to Channels 1 and 3, respectively, while Channels 2 and 4 were driven with

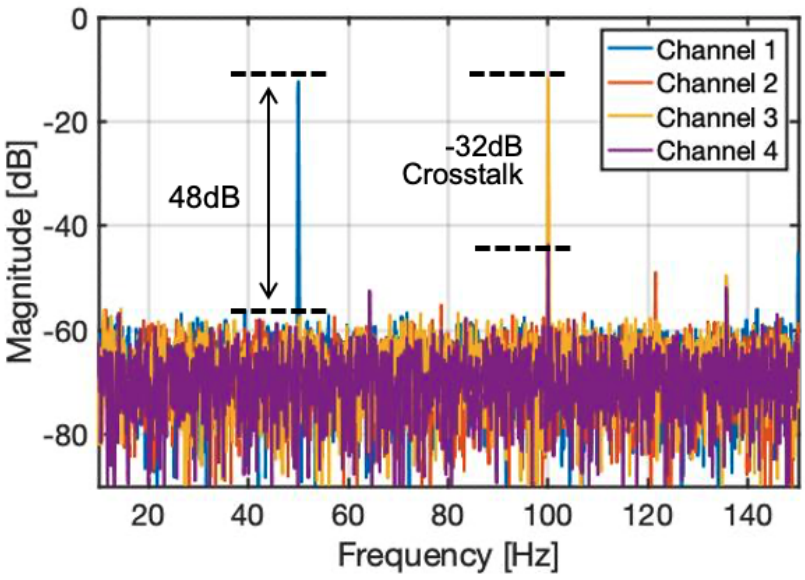


Figure 3.16: Measured result of four-channel system performance with two sine inputs and two V_{CM} inputs

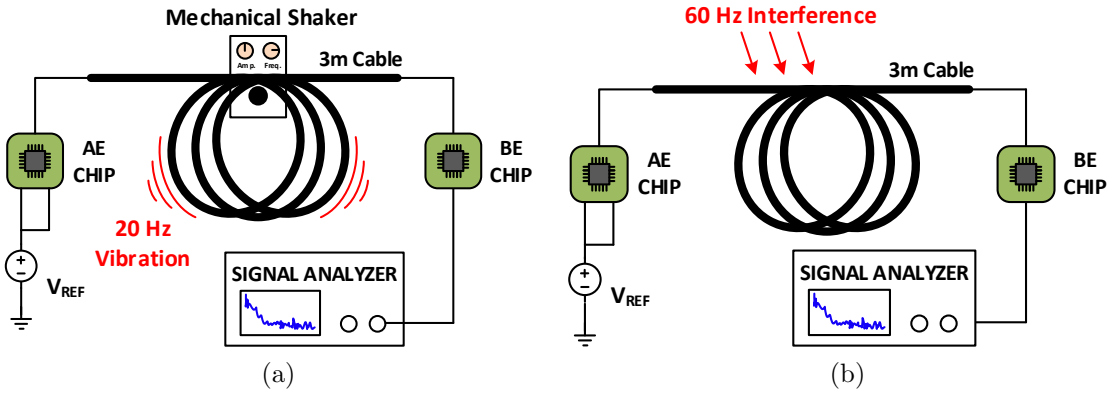
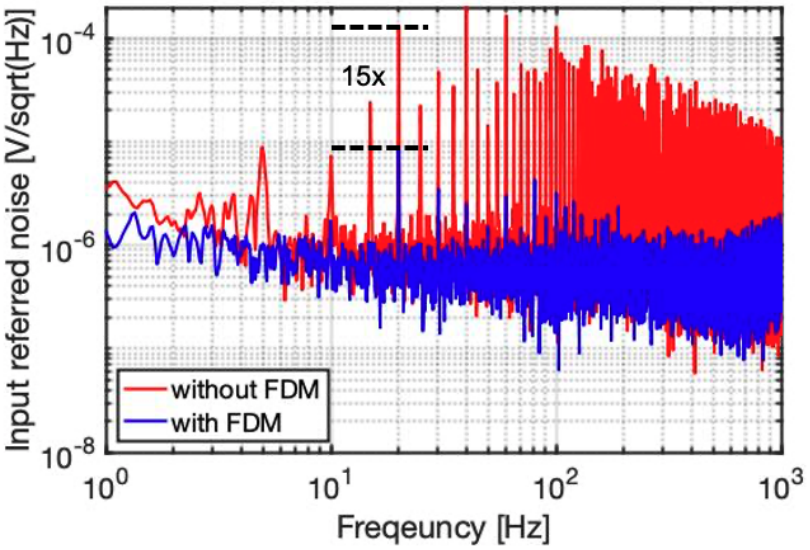
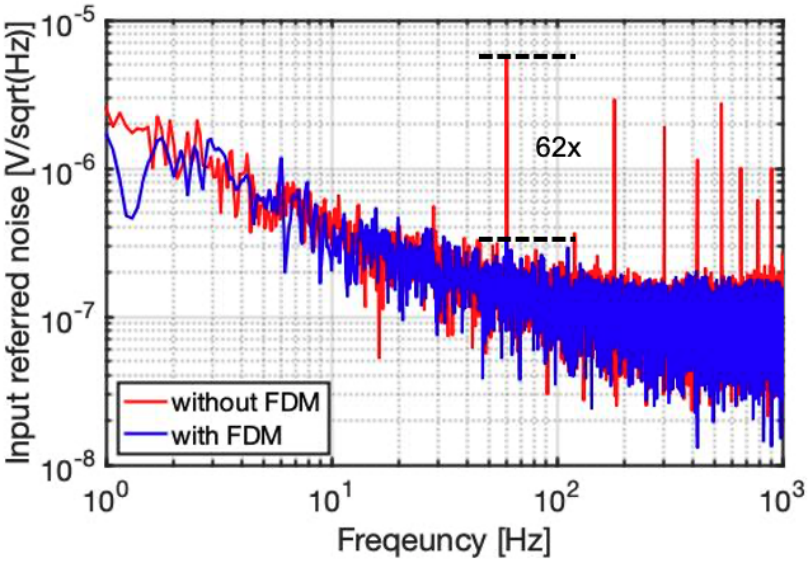


Figure 3.17: Experimental setup for FDM-based rejection of induced cable noises in the primary AE-BE cable: (a) 20 Hz cable motion artifacts and (b) 60 Hz mains interference.



(a)



(b)

Figure 3.18: Measured results for FDM-based rejection of induced cable noises in the primary AE-BE cable: (a) 20 Hz cable motion artifacts and (b) 60 Hz mains interference.

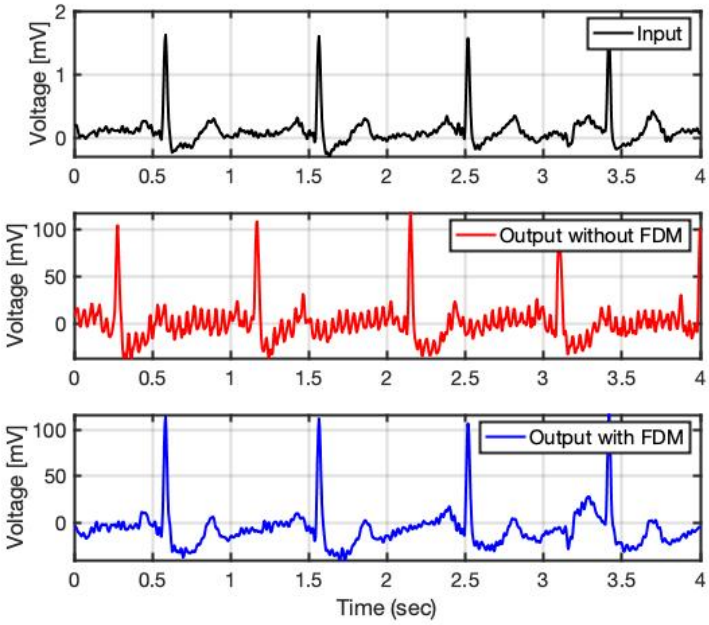
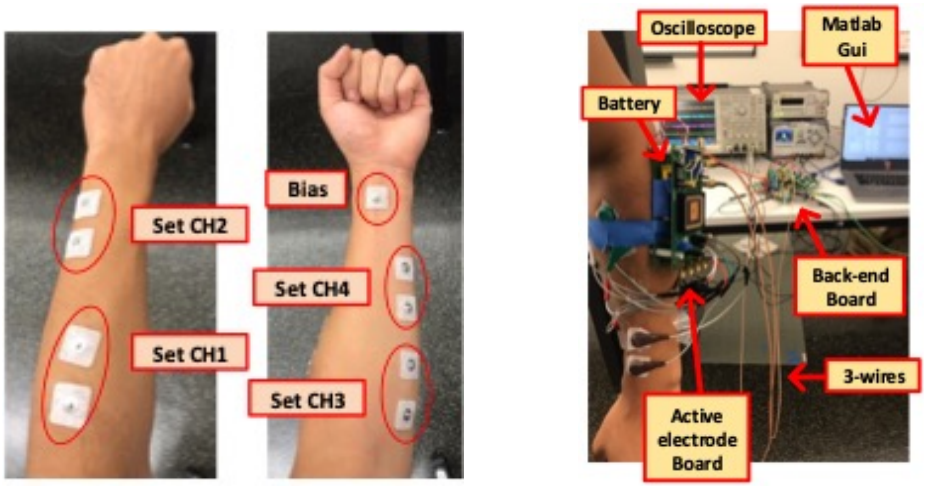


Figure 3.19: Measured reduction of induced cable motion artifacts using AM-FDM system for ECG application.



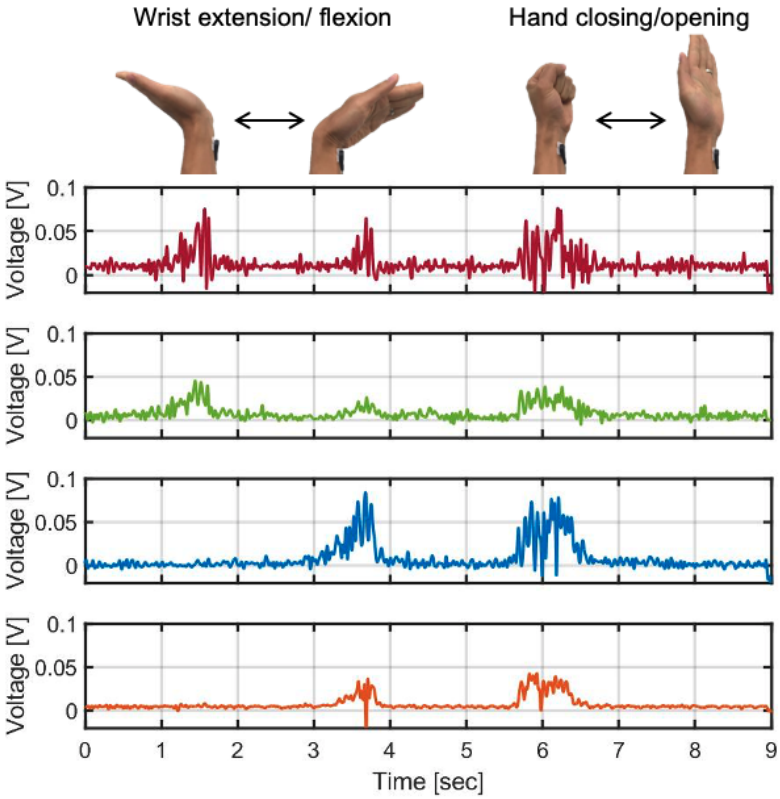
(a) (b)

Figure 3.20: Demonstration of the implemented AM-FDM system for wearable EMG measurement: (a) Electrode position; (b) Experimental setup.

common mode dc voltage. All four input signals were modulated by separate modulation frequencies (1.28 kHz, 1.8 kHz, 2.25 kHz, and 3 kHz) in the AE. Fig. 3.16 shows measured performance of the implemented FDM-based architecture using these test input signals. Final demodulated output signals demonstrate 48 dB half-differential (54 dB fully-differential) in-channel gain. As measured, the cross-talk signal magnitude is 32 dB lower than the primary signal, which can be further reduced by increasing the modulation frequency spacing.

3.5.3 Mains and Motion Artifact Rejection

Experimental setups for demonstrating the cable noise rejection of the implemented FDM-based architecture are illustrated in Fig. 3.17. In order to mimic motion artifacts, a programmable mechanical shaker was connected to a 3 m cable connected



(a)

Figure 3.21: Measured results.

Table 3.1: Performance comparison with state-of-the-art

	JSSC'14[23]	TBCAS'20[39]	JSSC'19[40]	TBCAS'19[41]	JSSC'15[25]	ISSCC'19[26]	This work
Application	EEG/ETI	EEG	ECG	ETI	EXG	EEG	**EMG/ECG**
Electrode type	Passive	Passive	Passive	Passive	Active	Active	**Active**
Multiplexing type	TDM	TDM	AM-FDM	AM-FDM	Digital bus	FM-FDM	**AM-FDM**
N-channel signal wires	2N	2N	2N	2N	2	1	**2**
Off-chip component	None	None	8 · LO	None	Capacitor	2 · Inductor	**None**
Electrode offset rejection [mV]	±250	±200	±125	-	±350	Rail-to-rail	**Rail-to-rail**
Process [nm]	180	180	130	130	180	65	**180**
Supply [V]	1.8	1.0	1.0	1.0	1.8	1.2	**1.8**
Bandwidth [Hz]	0.5-100	0.5-100	0.5-150	15k-125k	0.5-100	0-250	**1-150**
Input ref. noise [µV_{rms}]	1.75(100Hz)	0.63(100Hz)	1.44(150Hz)	-	0.65(100Hz)	0.99(250Hz)	**3.52(150Hz)**
AE Gain [dB]	20-40	54/60	29.3	-	40	-	**35**
ADC	12b SAR	-	16b SDM	16b SDM	12b SAR	12b SAR	**11b SAR**
Area per ch. [mm^2]	21.6	0.077(only IA)	0.525(only IA)	0.87	15.75	1	**0.75**
Power per ch. [μW]	82	1.5(only IA)	7.5(only IA)	118	104.4	228	**43.8**

LO - Local Oscillator IA - Instrumentation Amplifier

between AE and BE. While applying a dc input into the AE IC, we analyze the noise performance of FDM-based architecture through a signal analyzer connecting the output of the BE-IC (Fig. 3.17a). In a simlar way, Fig. 3.17b shows the measurement setup for 60 Hz interference induced by nearby electrical devices injected into the AE-BE cable. In this test environment, the AE-BE cable was looped and placed on the surface of a powered electrical machine to mimic ambient mains noise.

Measured results demonstrating motion artifact and mains interference reduction in the communication cable are depicted in Fig. 3.18. For measuring a 20 Hz motion artifact, the system employing FDM (blue line) reduces the induced noise by greater than 15X at 20 Hz compared to the system operated without FDM (red line). Also, most of the harmonics induced from main vibration frequency are removed by FDM, as shown in Fig. 3.18(a). For measuring 60 Hz mains interference, the re-

sult (Fig. 3.18(b)) demonstrates that the system with FDM in operation (blue line) improves noise performance more than 62X compared the system operated without FDM (red line).

As a further demonstration of cable noise reduction specific to bioelectronic signal acquisition, a pre-recorded ECG data taken from MIT-BIH database [42] is used as an input signal of AM-FDM system. Measured results present that mechanically-induced 20 Hz cable motion artifacts are reduced by the FDM technique as shown in Fig. 3.19.

3.5.4 Four-channel EMG using AM-FDM System

A wearable, FDM-based four-channel EMG readout system has been demonstrated using the implemented AE-IC and BE-IC, as shown in Fig. 3.20. Since skin surface electrodes convert biopotential signals to electrical signals as the first component of signal acquisition block chain, a type of electrode interface can limit a system performance [43]. In this measurement, we chose commercially available, disposable wet electrodes with Ag/AgCl [44]. Fig. 3.20a shows the placement of four surface electrodes pairs and one reference electrode for measuring surface biopotential signal changes in conjunction with different muscle activations [45]. As shown in Fig. 3.20b, a battery-powered AE-IC module worn on the arm is connected to a bench-top BE-IC module over a long (3 m) three-wire interface. The measured transient outputs demonstrate that the AM-FDM system enables distinguishing wrist extension/flexion and hand closing/opening gestures from the surface EMG measurements (Fig. 3.21a).

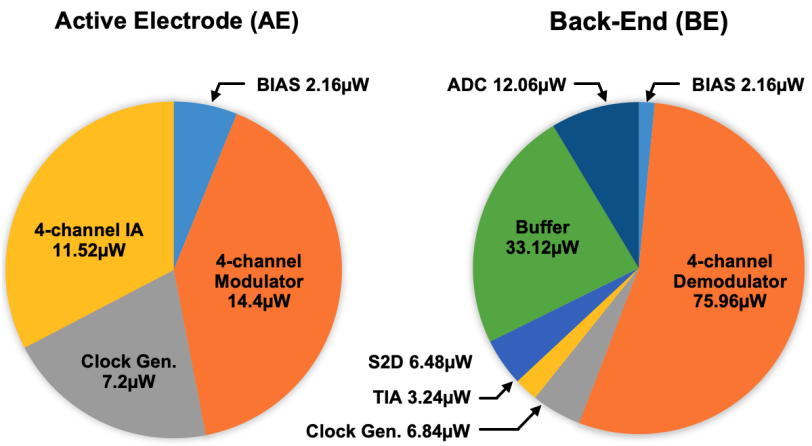


Figure 3.22: Power breakdown.

3.5.5 AM-FDM Power Consumption

A key feature of the implemented readout system is its low power consumption, which makes it suitable for battery-powered active electrode applications. As shown in Fig. 3.22, the four-channel AE-IC consumes a total average power of 20.8 μW, and the BE-IC supporting four channels consumes approximately 76.5 μW, most of which is consumed by the four demodulation circuits, as well as analog buffers for monitoring analog signals. Overall, each combined AE-BE channel consumes 43.8 μW in operation, including apportioned ADC power.

The performance of the implemented readout system is compared with state-of-the-art biopotential measurement systems presented in recent literature in Table 3.1, where the low-power and low-noise operation combined with the low wire count enabled by the AM-FDM approach will enable long-term ExG recording and future scaling for ExG applications requiring high-density electrodes.

3.6 Conclusion

A fully-integrated, FDM-based multi-channel biopotential signal acquisition system is presented, which reduces both cable motion artifacts and low frequency cable noise and minimizes the number of wires required for multi-channel recording systems. Both a front-end active electrode IC and a back-end demodulation IC were implemented and used in conjunction for system-level verification.

The use of passive up-conversion and down-conversion mixers mitigates additional power consumption required for FDM. In addition, a multi-switching duty-cycled resistor (MS-DCR) architecture applied the feedback network of the capacitively-coupled instrumentation amplifier (CCIA) in the active electrode (AE), extends the limited effective resistance of the conventional DCR for high-gain operation.

Overall, the proposed four-channel acquisition system fabricated in 0.18 μm CMOS process achieves 15X reduction in cable motion artifacts and 62X reduction in mains interference, and both one-channel ECG and four-channel real-time EMG systems are demonstrated as proof-of-principles. This scalable approach can be applied to many-electrode measurements of EEG, ECoG, and other ExG applications.

Chapter 4: One-Wire Frequency-Division Multiplexing Multi-Channel Biopotential Active Electrode for Extended Scalability

4.1 Introduction

Biopotential signal acquisition systems, such as for ECG, EEG, and other ExG monitoring and diagnosis applications, are tending toward higher electrode count to provide increased resolution and accuracy. However, the increasingly large wire bundles limit both scalability and ambulatory use. As shown in Fig. 4.1(a), a conventional N-channel passive electrode system [46] requires 2N wires. These long wires are highly susceptible to low frequency interference, where in-band frequency range of biopotential signals are placed at very low (1 Hz – 150 Hz); mains interference and motion artifacts also fall in this range. In order to reduce wire count and mitigate wire noise effects, frequency-division multiplexing (FDM) architectures [30, 26, 41] have been employed; an example is depicted in Fig. 4.1(b). The maximum channel count is determined by the bandwidth of the modulation frequency, which is further limited by the third harmonic of the first modulation frequency (f_1). Also, ADC count is proportional to the number of electrodes.

In this work, I present an alternative FDM-based acquisition system that addresses these limitations using a harmonic rejection technique [47], as shown in Fig. 4.2. This approach extends the modulation frequency bandwidth by more than 3X by cancelling

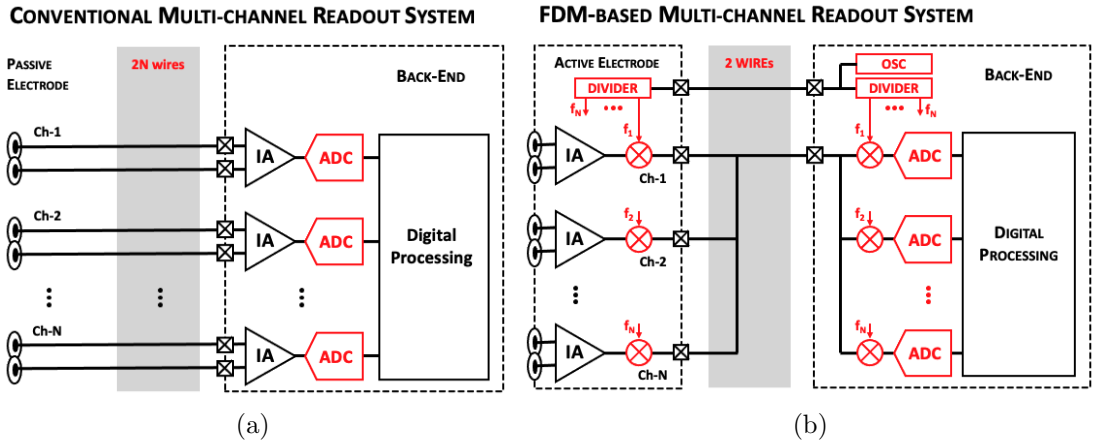


Figure 4.1: High-level architecture of the FDM-based multi-channel biopotential readout system: (a) Conventional, (b) Previous works.

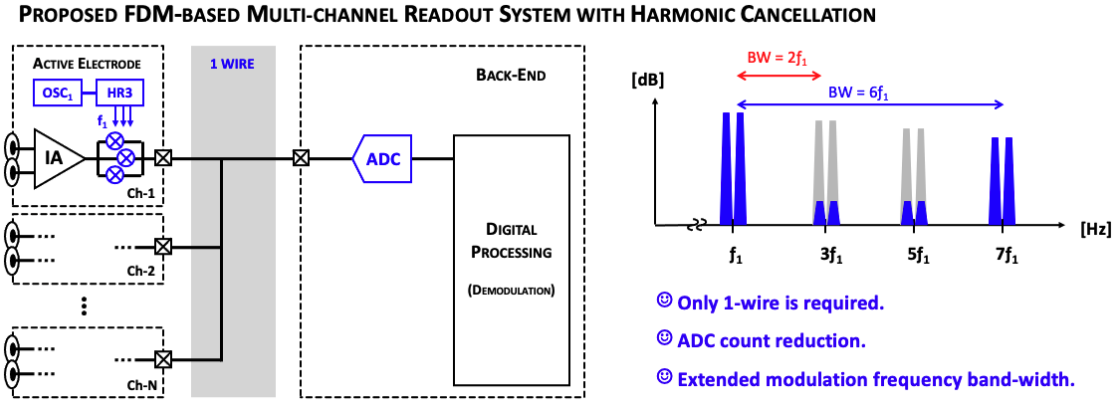


Figure 4.2: High-level architecture of the proposed FDM-based multi-channel biopotential readout system.

third and fifth harmonics of f_1. Further, fully-digital demodulation enables one-wire operation using a single, higher speed ADC.

4.2 FDM-based multi-channel biopotential readout system with extended bandwidth

4.2.1 Overview of the approach

The implemented circuit diagram is described in Fig. 4.3. Each biopotential channel uses an active electrode integrated circuit (AE-IC) placed close to differential electrodes, each of which consists of an instrumental amplifier (IA), a spike filter, and a modulation block. A capacitively coupled amplifier acts as the IA, providing high-pass filtering to reject electrode DC offset and amplifying the input signal by C1/C2 = 50. The feedback resistor (R_2) uses a duty-cycled resistor (DCR) to generate a very high resistance ($10\,G\Omega$) with greater tunability and higher linearity than a MOS-based pseudo resistor. The core amplifier for the IA employs an inverter-type differential input two-stage design to achieve high gm without further increasing total current. The spike filter compensates transient spikes induced by DCR and is switched by an inverse DCR clock signal. For the next stage, the modulation signal path comprises three passive, up-converting mixers and three gm amplifiers that operate as a harmonic rejection modulation circuit. Three phase-shifted ($-45\,^\circ, 0\,^\circ, 45\,^\circ$) clock sources are applied to the mixers, and three gain weights (1, 2, 1) are provided to source resistance (R_S) of the source-degeneration-based gm amplifiers. Additionally,

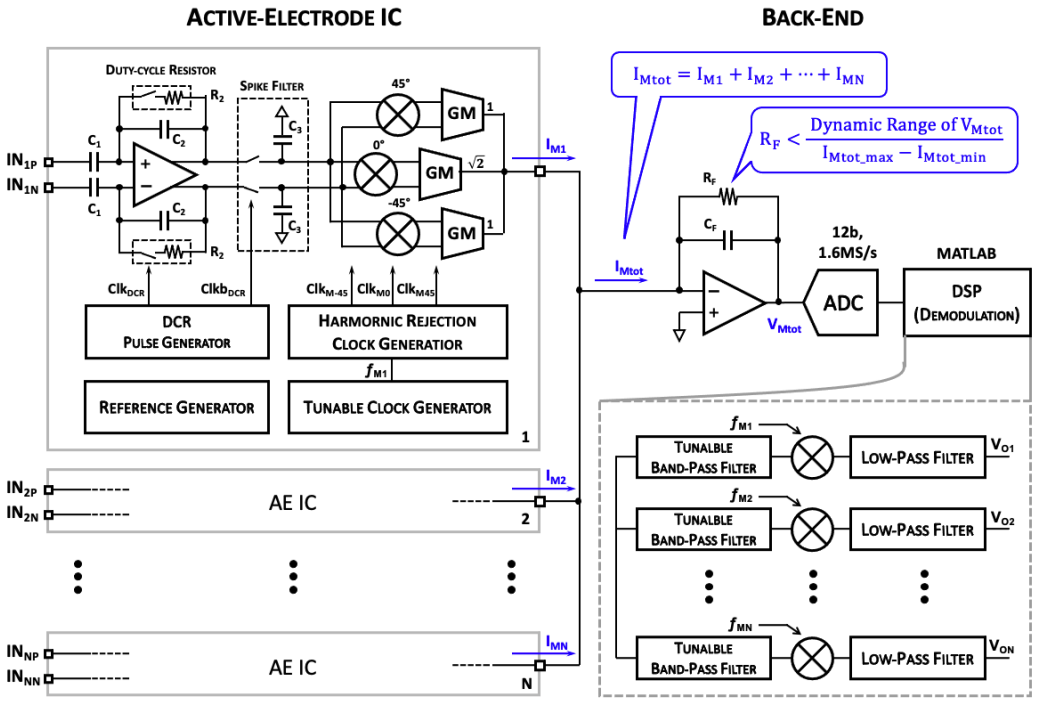


Figure 4.3: Block diagram of N-channel biopotential readout system using frequency division multiplexing (FDM) with harmonic rejection to increase the available multi-channel bandwidth.

internal RC relaxation clock generators provide reference clock sources for the DCR pulse signal and for the modulation clock signals.

The frequency-modulated output currents (I_{M1} - M_N) of all channels are combined at a single wire connected to a back-end (BE) circuit, as shown in Fig. 4.3(right). The merged current (I_{Mtot}) is converted to a modulated voltage (V_{Mtot}) by a transimpedance amplifier (TIA). The programmable feedback resistor (R_F) determines a gain of TIA; the value of R_F must be properly selected to determine input dynamic range, where VMtot may otherwise saturate to the maximum system voltage. The feedback capacitor (C_F) is used for system stability. A 12-bit, 1.6 MS/s external ADC

digitizes the analog output voltage, V_{Mtot}. Demodulation is performed using digital signal processing (DSP), using the architecture depicted in Fig. 4.3. A tunable band-pass filter is aligned to each modulated signal channel, and each filtered signal is then down-converted using the product operation and low-pass filtering. This approach obviates the need for AE and BE phase alignment, enabling one-wire operation in place of two-wire.

4.2.2 Harmonic cancellation technique

Fig. 4.4 illustrates the operation of the harmonic rejection clock generator. The input reference clock (Ref) frequency is determined by a selected channel's modulation frequency (f_M). A ring counter circuit using four D flip-flops generates four clock phases, where three of them are used for the harmonic cancellation. Four 2:1 Multiplexers are used to optionally enable or disable the harmonic cancellation. The three clocks connect to each switch of the up-conversion modulation blocks, and each gm is set considering weight coefficients required for third harmonic rejection for the GM amplifiers (Fig. 2). The summed output current of each AE-IC is shown in Fig. 4.4(b), where harmonic cancellation better approximates a sinusoidal wave than does pure square-wave modulation, while still using only simple digital on-chip clock generation circuits.

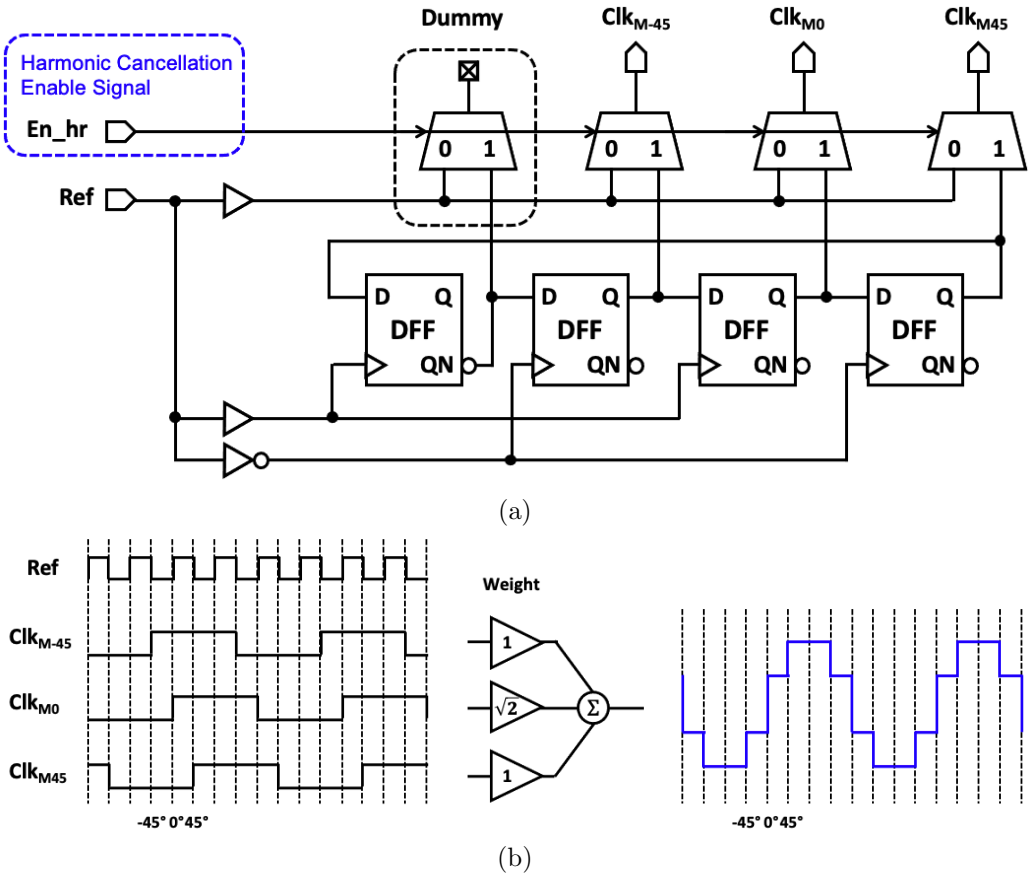


Figure 4.4: Implemented harmonic rejection clock generator included in each AE channel: (a) Circuit diagram, (b) transient waveforms.

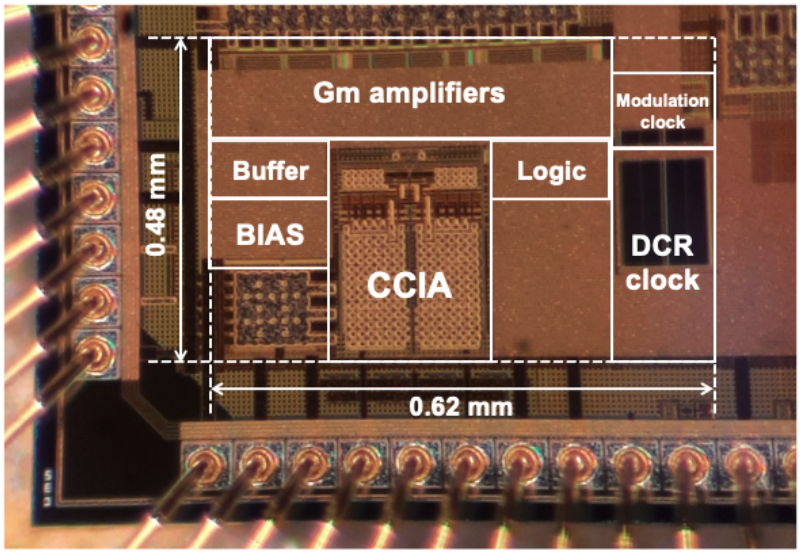


Figure 4.5: Die photo of the AE-IC fabricated in 0.18 μm CMOS.

4.3 Measurement Results and Discussions

A prototype AE-IC implementing harmonic cancellation for FDM was fabricated in a 0.18 μm CMOS process and packaged in a 64-pin CQFJ carrier. Each 1-channel AE-IC occupies 0.3 mm^2 circuit area, as shown in Fig. 4.5, and consumes 12.3 μW per channel in operation.

4.3.1 Experimental Setup

For the experimental setup (Fig. 4.6), two AE-ICs were attached on a printed circuit board (PCB) to facilitate multi-channel demonstration. Differential input signals were applied using arbitrary signal generators (AWGs). A discrete TIA ($R_F = 1\,M\Omega$, $C_F = 0.3\,pF$) was included on the PCB for demonstration of back-end readout, and

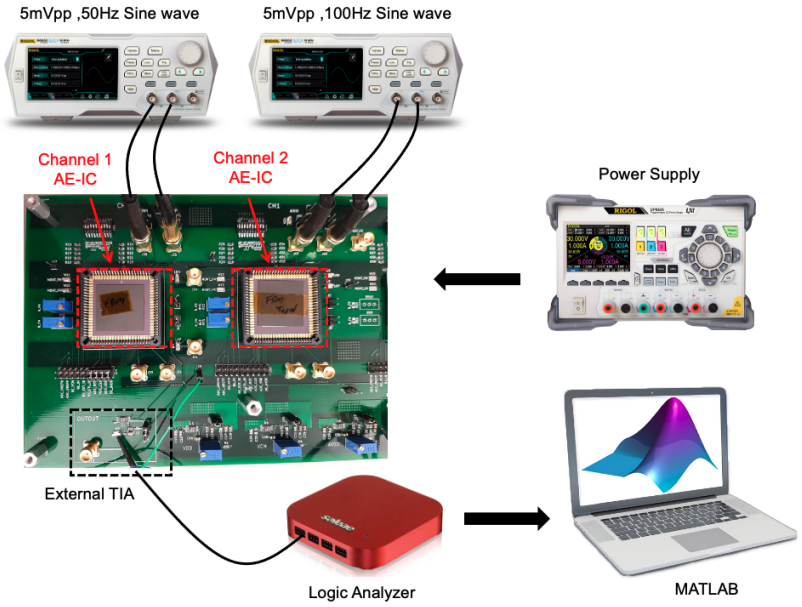
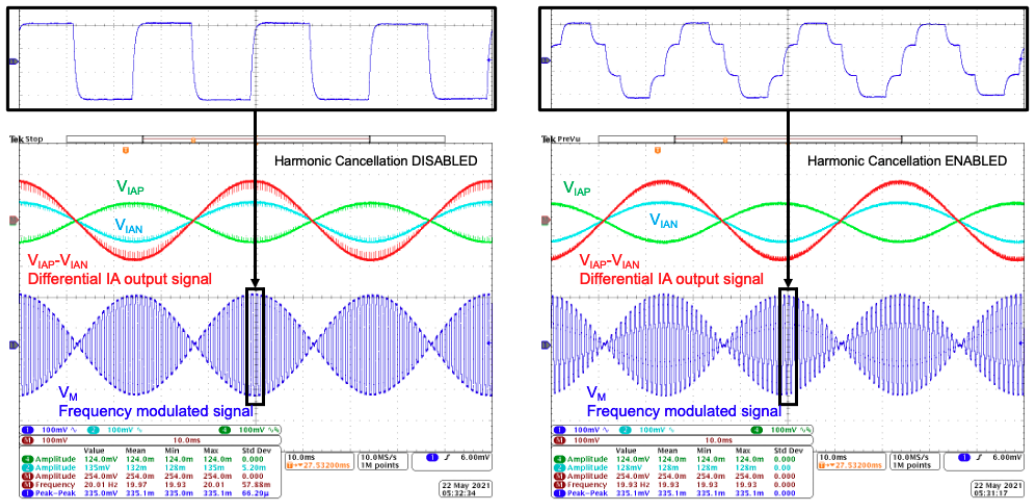


Figure 4.6: Experimental setup for two-channel readout system demonstration.

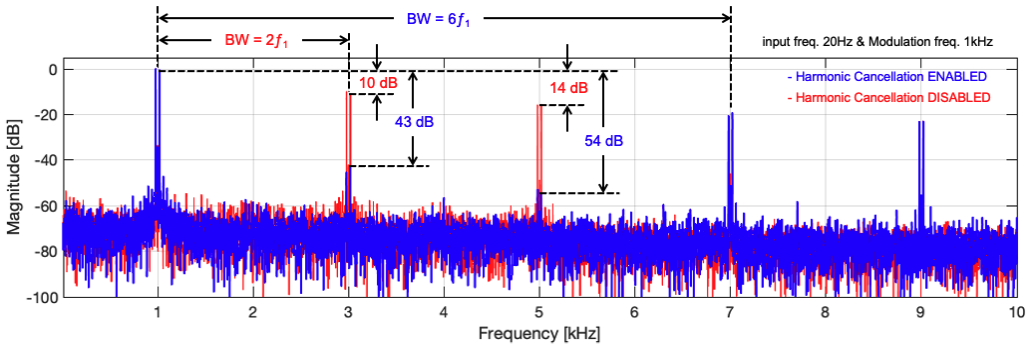
a 12-bit ADC internal to a bench-top logic analyzer was used for digitization of the TIA output. All essential digital signal processing was performed using MATLAB.

4.3.2 Measured cancellation for single-channel modulated signal

Fig. 4.7(a) presents measured transient waveforms of the single-channel differential IA outputs (V_{IAP} & V_{IAN}) and the modulated signal (V_M), when the harmonic rejection technique is enabled and disabled separately. The applied differential input (V_{INP} - V_{INN}) is a 5 mVpp, 20 Hz sinusoidal signal, and modulation frequency is 1 kHz. The measured average amplitude of the differential IA output is 254 mVpp as shown due to 35 dB IA amplification. As shown in the normalized FFT result, Fig. 4.7(b), the third and fifth harmonics of the modulation signal are reduced by 33 dB and



(a)



(b)

Figure 4.7: Measured cancellation for single-channel modulated signal: (a) transient waveforms and (b) frequency responses.

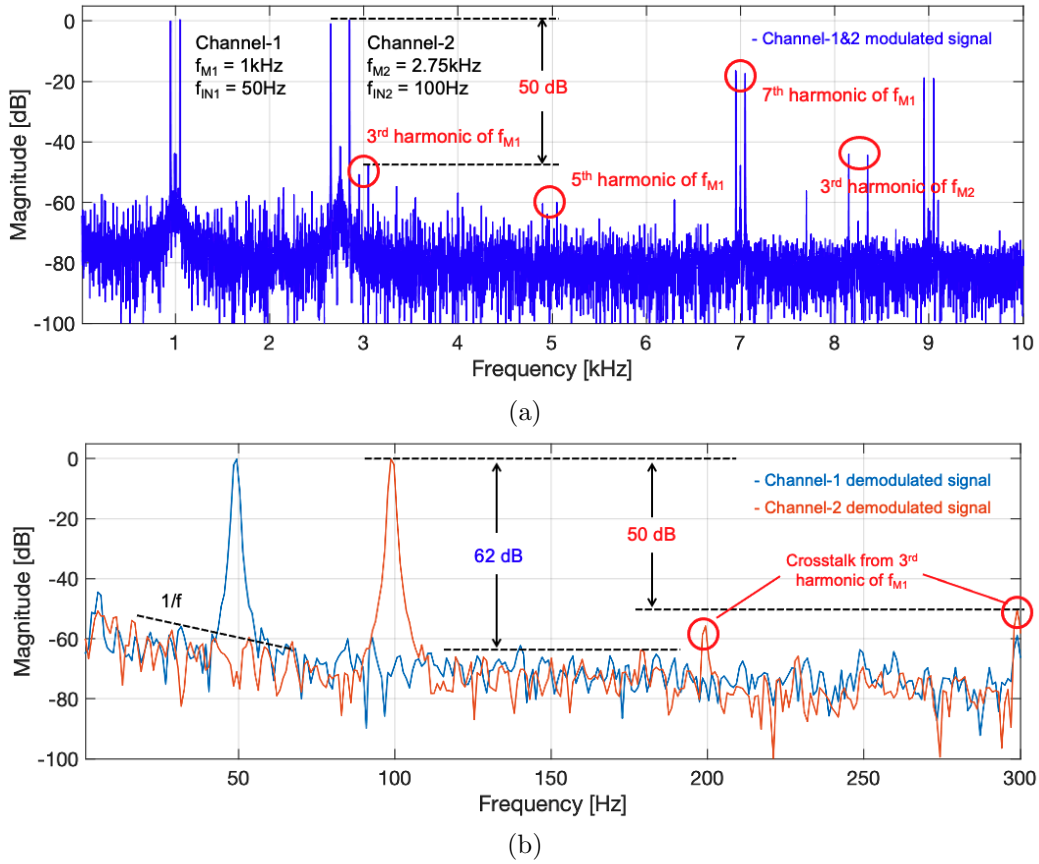


Figure 4.8: Measured two-channel system performance: (a) modulated signal and (b) demodulated output signals.

40 dB, respectively. Therefore, when the harmonic rejection is enabled, the available bandwidth for modulation frequencies is extended from $2 \cdot f_1$ to $6 \cdot f_1$.

4.3.3 Measured two-channel system performance

A 2-channel FDM system was demonstrated for proof-of-concept. The normalized FFT result of the measured modulation signal, applied using 50 Hz and 100 Hz input

Table 4.1: Performance comparison with state-of-the-art

	JSSC'19[40]	**TBCAS'19[41]**	**ISSCC'19[26]**	**CICC'20[30]**	**This work**
Application	ECG	ETI	EEG	EMG/ECG	**ExG**
Multiplexing type	AM-FDM	AM-FDM	FM-FDM	AM-FDM	**AM-FDM**
Number of wires	2N	2N	1	2	**1**
Modulation frequency BW	$2 \cdot f_{ch1}$	$2 \cdot f_{ch1}$	-	$2 \cdot f_{ch1}$	$6 \cdot f_{ch1}$
Process [nm]	130	130	65	180	**180**
Supply [V]	1.0	1.0	1.2	1.8	**1.8**
AE Gain [dB]	29.3	-	-	35	**35**
Area per ch. [mm^2]	0.525(only IA)	0.87	1	0.75	**0.3(AE IC)**
Power per ch. [μW]	7.5(only IA)	118	228	43.8	**12.3(AE IC)**

sine waves modulated by 1 kHz (f_1) and 2.75 kHz (f_2), is shown in Fig. 4.8(a). This demonstrates the worst-case operation, where the third harmonic of f_1 appears within the in-band region of the f_2 modulated signal. When applying identical input amplitudes for the two channels, the signal magnitude difference between the fundamental f_2 and the third harmonic of f_1 is 50 dB. The resulting crosstalk is present in the digitally demodulated output signals, as annotated in Fig. 4.8(b).

4.4 Conclusion

Table 4.1 summarizes the performance of the proposed FDM-based multichannel acquisition architecture employing harmonic cancellation and compares it to recent state-of-the art FDM-based biopotential readout systems. This work extends the available modulation frequency bandwidth 3X more than previous approaches, while

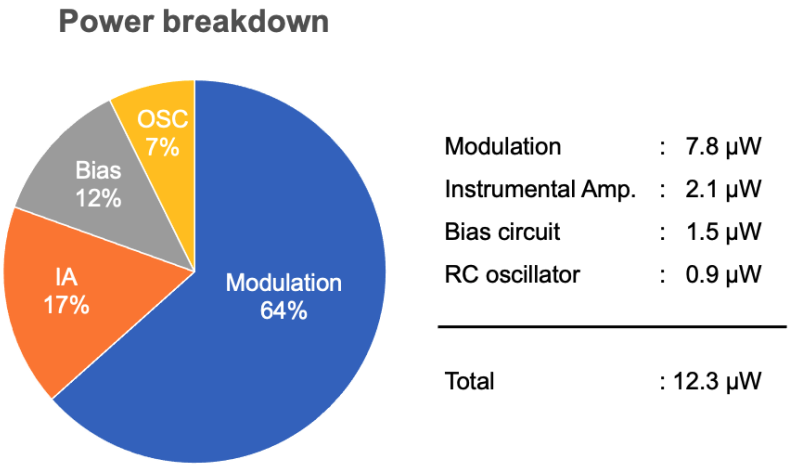


Figure 4.9: Power breakdown per AE-IC (per channel).

maintaining similarly low power operation. In addition, as compared with [30], by adding a local oscillator to each AE-IC and using a digitally demodulated architecture, the proposed system requires only a single data wire between multiple active electrodes and a back-end readout system. This approach addresses a fundamental challenge of limited bandwidth, critically needed for future scalability as applied to many-electrode measurement of EEG, ECoG, and other ExG applications.

Chapter 5: Frequency-Division Multiplexing with Graphene Active Electrodes for Neurosensor Applications

5.1 Introduction

Large-scale neural recording systems are crucial for understanding brain function at the level of neuron-to-neuron interactions [48]. These measurements are increasingly supported by IC-based readout for density, scalability, and localized signal processing [49, 50, 51, 52, 53, 54, 55]. However, high-signal-count recordings of a dense network of neurons is challenging due to physical limits of wiring density, which in turn limit spatial resolution [56, 57, 58]. For conventional electrical neural recording interfaces, recording sites are passive electrodes wired to read-out circuitry, where the number of access wires equals the number of recording sites. This one-to-one relationship between recording sites and access wires is a major obstacle to obtaining high-density recordings from large areas of the brain.

A second bottleneck for large-scale neural recording is the signal conditioning and digitization electronics, which for highly-parallel recording systems are typically integrated in a microchip located outside the brain. For such implementations, the number of wires that can connect to an individual IC is physically limited, which has constrained state-of-the-art external neural interface ICs to typically less than 1000 sensor channels [50, 51, 52]. Internal neural interface ICs bonded to an electrode

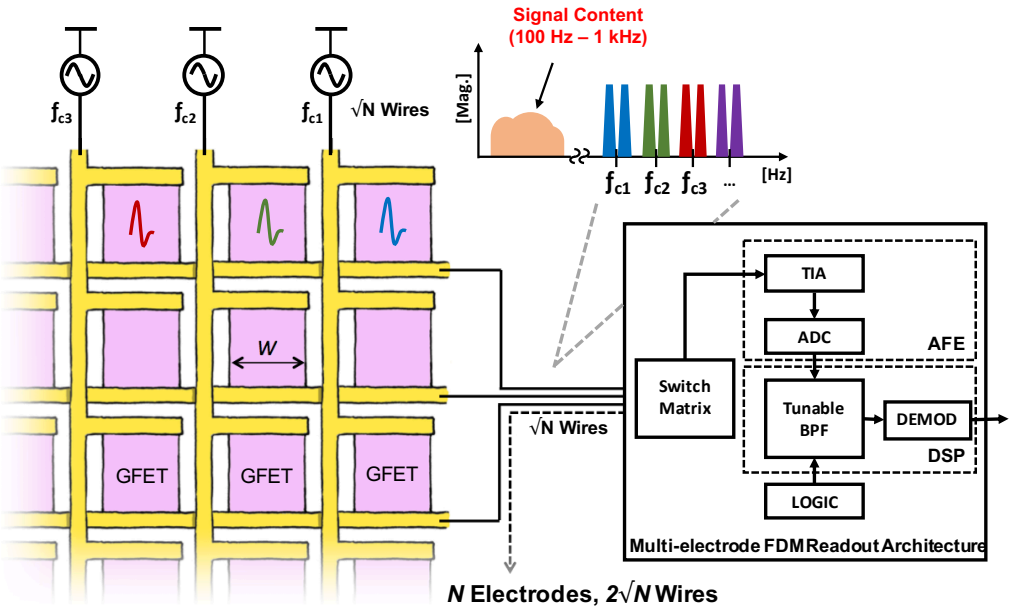


Figure 5.1: Proposed high-level architecture using graphene field-effect transistor (GFET) active electrode array with FDM for access wire reduction.

array [59, 60] can increase this density, but wire and packaging constraints may limit further scalability of such implementations. In some cases this can be addressed using IC-readout integrated into implantable electrode shanks [58], but for such approaches repeated relative micromotion between a rigid silicon probe and the surrounding brain tissue induces glial scarring and limits long-term use [61]. Electrode arrays that match the mechanical compliance of brain tissue and are stable in the biological environment have been demonstrated for both implantable [61] and brain surface [62] electrodes, but these material systems do not allow direct integration of electrical readout circuitry for wire reduction and still comprise passive, many-wire electrode arrays limited by wiring density.

In this chapter, I present and demonstrate proof-of-principle for the use of active graphene electrodes with a frequency-division multiplexing (FDM) architecture for use in neural recording and biosignal recording arrays. As illustrated in Fig. 5.1, each electrode is formed by a liquid-gated graphene field-effect transistor (GFET), which enables up-conversion of a local signal using a carrier frequency directly in the electrode. Using column-based FDM with shared-row readout, this GFET-FDM approach breaks the wire count limit of a conventional passive electrode array, without requiring the co-location of switches within the electrode array. In addition, the use of active GFET electrodes can enable flexible and compliant neural electrode arrays in future implementations.

5.2 Frequency-Division Multiplexing Approach using Active Graphene Electrodes

5.2.1 Overview of the approach

Compared to conventional passive electrodes, an active electrode provides gain or signal conditioning at the electrode itself. This can be accomplished for biological interfaces using fluid-gated FET devices, where the electrical resistance of the FET channel changes in response to local bioelectric signals, such as neuron firing[63, 64, 65]. Graphene, an atomically thin layer of sp^2 bonded carbon, can be used in this manner. A square of graphene has a baseline resistance on the order of $5\,\mathrm{k}\Omega$; this electrical resistance changes by approximately 1% when there is a local voltage

change of 1 mV at the gate. Previous work has demonstrated that bioelectric signals of 10 μV can be detected with a 15 μm x 15 μm sensor size and 10 kHz bandwidth [64]. Moreover, graphene is ultra-flexible, mechanically robust, biocompatible, and chemically inert, which makes it a promising material for use in future flexible neural interface arrays.

A key insight of my proposed approach is that graphene FETs allows direct mixing of a local biosignal at the gate with a higher-frequency carrier signal applied to the source or drain, providing frequency-based modulation directly in each electrode. As illustrated in Fig. 2.1.1, this enables frequency-division multiplexing (FDM), where column-modulated output from multiple sensors is summed, sharing a single row wire for multiple graphene FET sensor signals. While demonstrated here using a few sensors as a proof of concept, the approach is broadly scalable for large, multi-electrode arrays.

5.2.2 Graphene field-effect transistors

The basic structure of a graphene FET is shown in Fig. 5.2(a). A rectangle of CVD-grown graphene on an insulating glass substrate is contacted on either end by electrodes, forming source and drain connections. Electrodes are passivated using an insulating material (SU-8). A source-drain bias V_{sd} is applied across the graphene channel. A liquid electrolyte acts as the gate material, with a tungsten electrode applying a gate voltage V_g to the liquid and modulating the channel resistance. The electrolyte used for the data shown here is a combination of salts that closely repli-

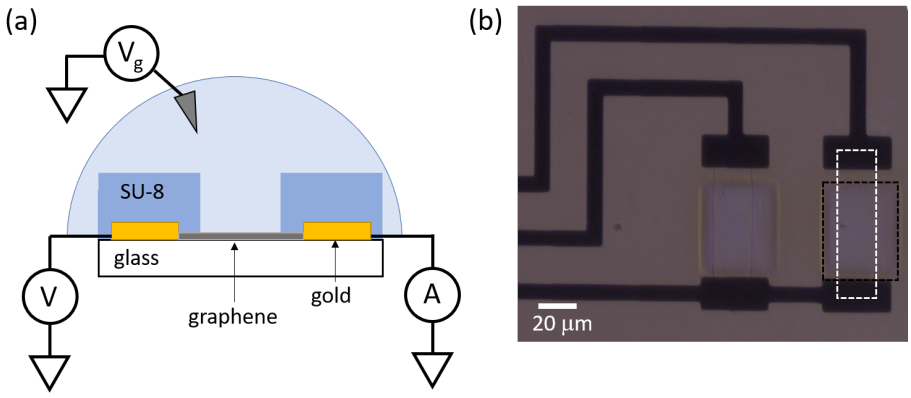


Figure 5.2: Basic operation and design of a liquid-gated graphene FET: (a) Schematic of the cross-section of a graphene FET device. The gate is a liquid with a voltage applied by a tungsten probe. (b) A microscope image of two fabricated graphene FETs that share a common drain. The graphene is outlined in white and the SU-8 opening is outlined in black for the device on the right. The SU-8 insulates the gold source/drain leads from the electrolyte gate.

cate the salt concentrations in cell culture medium; the total salt concentration is 125 mM, with the main component being NaCl at a concentration of 116 mM.

The proof-of-principle device design used in this work is shown in Fig. 5.2(b). Two graphene FETs share a common drain electrode. Each FET has its own source electrode which can be driven by an ac voltage source at a unique frequency. The area of graphene exposed to the liquid gate is 20 μm x 50 μm.

To fabricate the 2-by-1 array of graphene FETs, a pattern for the metal electrodes was created using photolithography on a glass substrate. The positive photoresist AZ 1512 (EMD Performance Materials) was spun onto the substrate, exposed, and developed with AZ 300 MIF developer. Next, approximately 10 nm of Cr followed by 60 nm of gold were deposited onto the chip with electron-beam deposition. The chip was soaked in Remover PG (MicroChem) overnight to remove the photoresist and

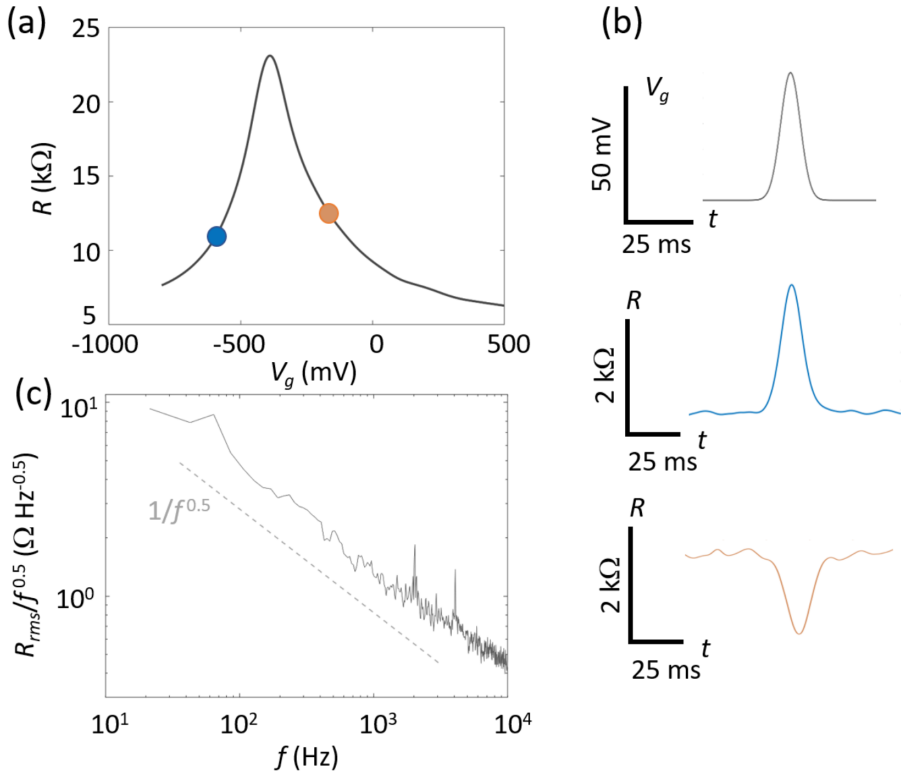


Figure 5.3: Measured electronic properties of a graphene FET: (a) Device resistance as a function of the gate voltage. (b) The Gaussian pulse shown (top) was applied to the gate, and the resistance response (center and bottom) was recorded. The operating points (i.e. DC offset of the Gaussian pulse on V_g) are -550 mV for the blue curve, and -215 mV for the orange curve. When the offset is in a region with $dR/dV_g > 0$, such as at the blue point, the change in resistance is the same sign as the change in gate voltage. Conversely, when the offset is in the region $dR/dV_g < 0$, the change in resistance has the opposite sign as the gate voltage change. (c) The noise spectrum for the device shows a characteristic $1/f^{0.5}$ shape typical to graphene FETs. The spectrum was measured at V_g = -215 mV. The root-mean-square resistance R_{rms} at this operating point is $\sim$95 Ω for the range 100 Hz to 10 kHz.

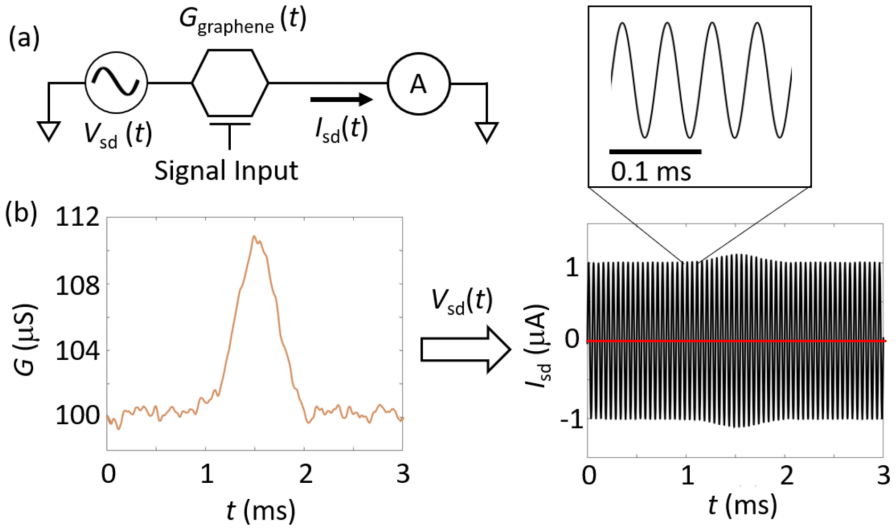


Figure 5.4: Modulation of a signal by a graphene FET. (a) The circuit representation of the measurement system. (b) The conductance of the graphene FET (left) and the resultant modulated current (right).

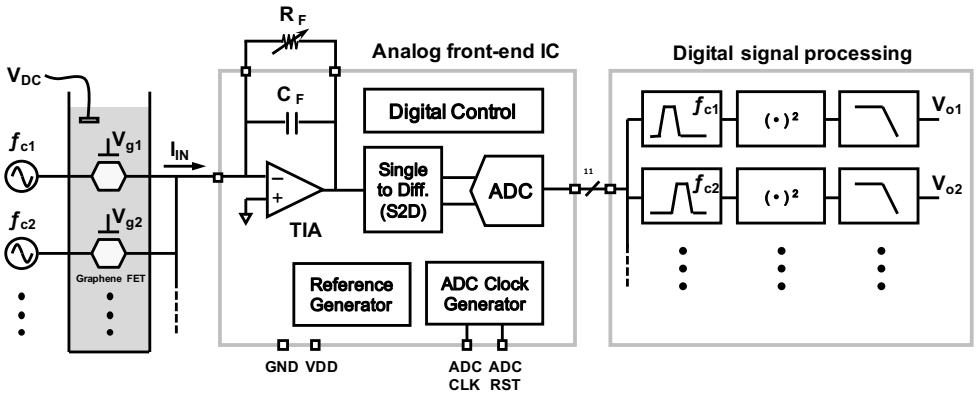


Figure 5.5: Proposed system architecture using a graphene FET active electrode array for amplitude modulation and signal summing, with analog signal conditioning, digitization, and fully-digital square law demodulation used to demonstrate the scalable FDM approach using active electrodes.

excess metal. CVD-grown graphene (ACS Materials) was then placed onto the chip using a wet-transfer process. Photolithography and oxygen-plasma etch were used to pattern the graphene. Then a layer of SU-8 was spun on and patterned to form a protective layer over the metal leads. Windows of size 50 μm x 40 μm are opened above the graphene to allow for exposure to the electrolyte gate. After development, the SU-8 layer is approximately 1.5 μm thick. Electrical characterization of a typical graphene FET device is shown in Fig. 5.3.

Graphene sensors can perform amplitude modulation directly at the sensor site (Fig. 5.4). A change in gate voltage from a biological signal of interest (such as a neuron action potential) creates a change in the conductance, $G(t)$. The ac applied bias, $V_{sd}(t)$, is driven at a frequency f_c that is much faster than the biological signal of interest. The resulting ac current, $I_{sd}(t)$, has a carrier frequency f_c and is amplitude modulated by $G(t)$.

5.2.3 Analog front-end integrated circuit architecture

The basic signal architecture is shown in Fig. 5.5; signal modulation is performed in each graphene FET active electrode, and the summed FDM output is read out by a custom analog front-end (AFE) integrated circuit (IC) and demodulated using off-chip digital signal processing (DSP).

In the AFE, a transimpedance amplifier (TIA) converts the input current signal, which contains multiple modulated and combined signal channels from the graphene FET array, to a voltage signal. The feedback resistor R_F, which determines the gain

of TIA, is externally placed for a flexible measurement setup; a feedback capacitor (C_F =500 fF) is added on-chip to improve stability. As R_F is not large (xx Ω), this can be included on-chip in future work without significant area requirements. A folded-cascode amplifier structure is implemented as the op-amp with 75 dB open-loop gain and approximately 1.2 MHz unity gain bandwidth; gain must be flat across the range of modulation frequencies, although slight differences in per-channel gain (due to GFET or AFE) can be calibrated. At the output of the TIA, and single-ended to differential converter is used prior to the analog-to-digital converter (ADC) and also provides low-pass filter behavior for anti-aliasing.

An 11-bit successive-approximation register (SAR) ADC is implemented to digitize the modulated signal. Since the minimized unit capacitance of capacitor array can reduce the power consumption and increase the sampling speed, we chose a 7 fF standard finger metal-oxide-metal (FMOM) capacitor provided by the foundry, instead of a metal-insulator-metal (MIM) structure with a bigger minimum unit capacitance. As switching of the capacitor digital-to-analog converter (CDAC) in the SAR ADC is one of the critical points for power consumption, a merged capacitor switching technique [34] is implemented to reduce switching energy in this work.

The AFE IC was fabricated in 0.18 μm CMOS, and a die photo is shown in Fig. 5.6; the AFE occupies 0.44 mm^2.

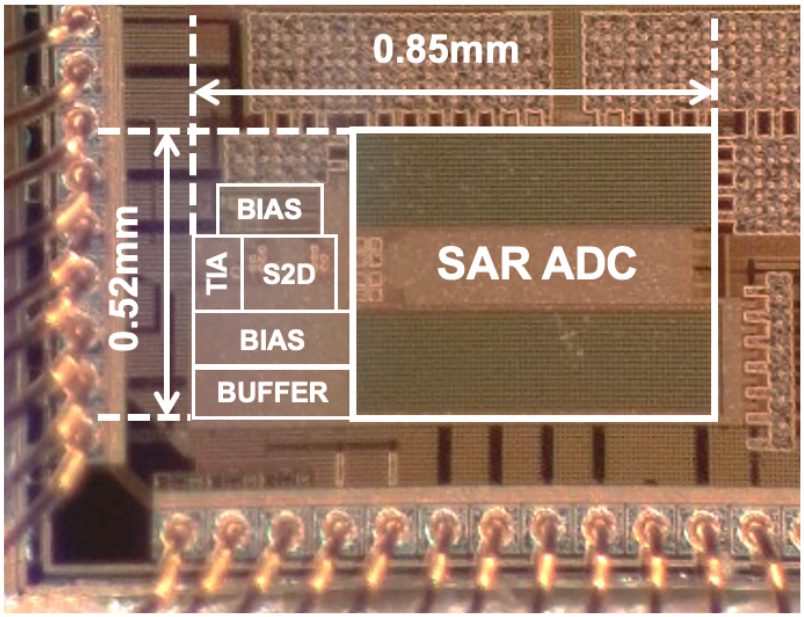


Figure 5.6: Micrograph of the analog front-end IC fabricated in 0.18 μm CMOS.

5.2.4 Digital signal processing for demodulation

For demodulation of the merged FDM signal, the back-end DSP chain contains a band-pass filter (BPF), a square operation block, and a low-pass filter (LPF). BPFs perform channel selection on the FDM waveform. Outputs of BPFs, each of which contains only modulated signal content at a particular carrier frequency, are demodulated using square law demodulation. Namely, the signal is self-multiplied before it is filtered by LPF. Square-law demodulation is chosen because it does not require accurate phase information about the carrier waveform and is computational requirement is not high. In our envisioned system, the number of DSP chains equals to the number of carrier frequencies aggregated in the FDM waveform, such that simultaneous

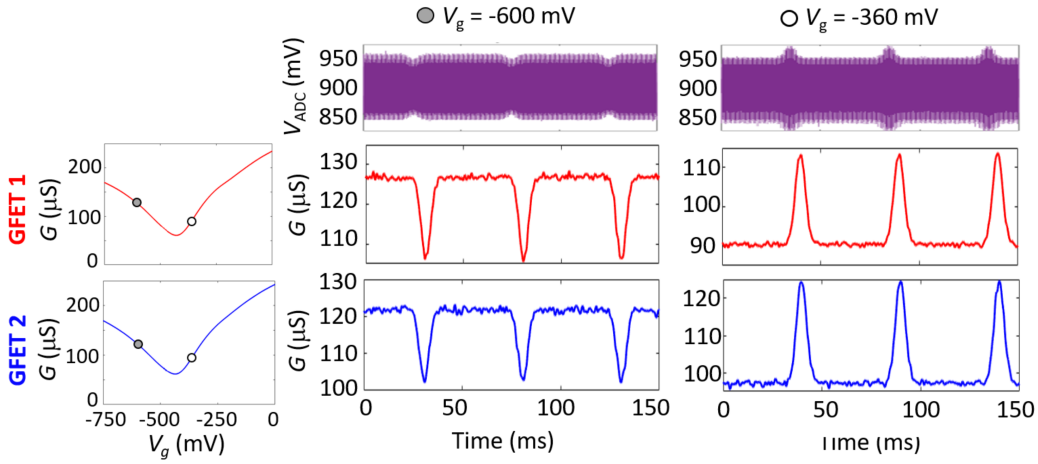


Figure 5.7: Measured transient waveforms of two-channel GFET-modulated signals and demodulated signals at different DC gate bias voltages (V_g); a Gaussian pulse on GFET liquid gates mimics local neuron firing. Operation on either side of the Dirac point (-480 mV) yields negative and positive conductance change.

parallel demodulation of multiple sensor signals can be achieved.

The DSP architecture was first simulated in MATLAB and then implemented in verilog and synthesized for a commercial off-the-shelf FPGA module (Opal Kelly XEM6310) to provide real-time demodulation. As implemented, each BPF is a digital FIR filter with 48 taps and a nominal bandwidth of 2 kHz. The digital LPF uses 32 taps, with a cut-off frequency of 1 kHz. Squaring operation is performed on FPGA, whereas the final square root operation is done on the computer. The number of DSP chains and filter parameters are all reconfigurable based on the need of front-end circuitry. This FPGA-based digital back-end provides fast computation and high flexibility.

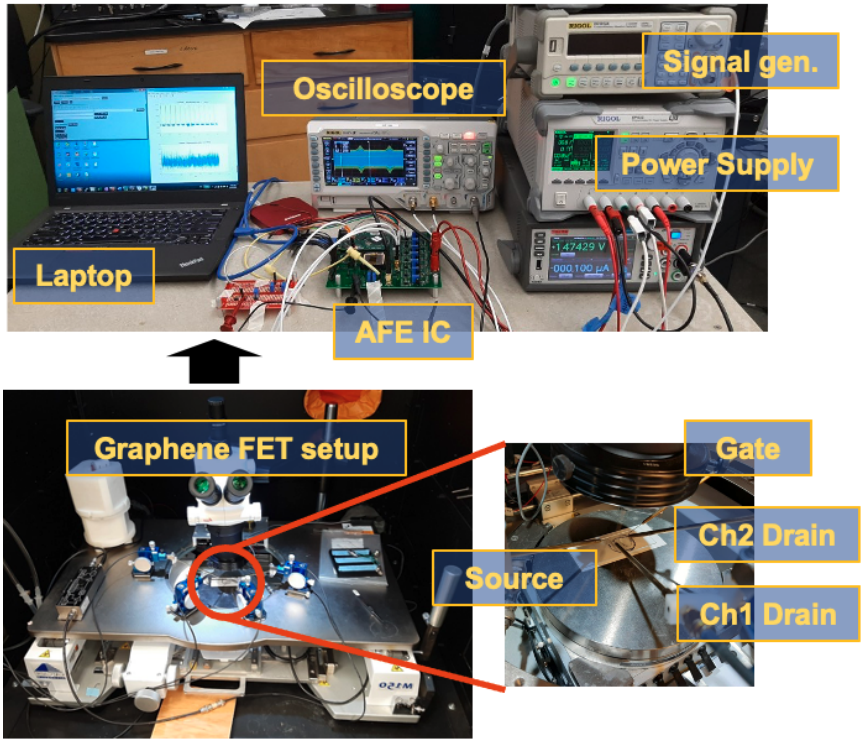


Figure 5.8: Measurement setup for complete GFET-FDM architecture.

5.3 Experimental Results and Discussion

5.3.1 Experimental Setup

The experimental setup is shown in Fig. 5.8. Two graphene FETs with common drain (Fig. 5.2) were driven as described in Section 5.2.2. A source-drain bias V_{sd} with frequency $f_{c1} = 5\,\text{kHz}$ was applied across device one, while V_{sd} with frequency $f_{c2} = 9\,\text{kHz}$ was applied across device two. The liquid gate was set to an operating point where device 1 and 2 are both sensitive to changes in gate voltage. A train of short voltage pulses, ΔV_g, was then added to the liquid gate to mimic a local

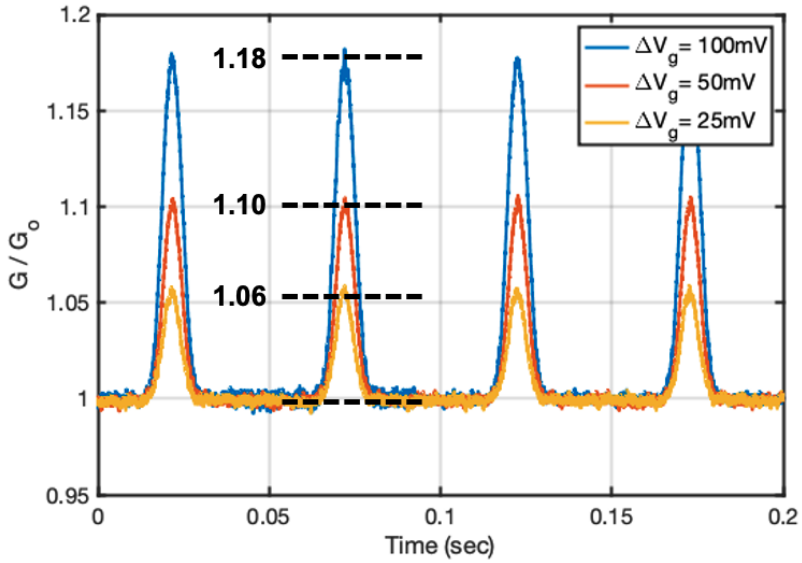


Figure 5.9: Measured transient showing different amplitude of demodulated outputs at different gate voltage of graphene FET (ΔVg).

bioelectric signal, such as a train of neuronal action potentials [64]. The total current was collected from the common drain. To achieve DC level-matching at the AFE IC input, an additional discrete amplifier, DC-blocking capacitor (0.9 μF), and series resistor (10 kΩ) were added at the AFE IC input (not shown in Fig. 5.5); these are not strictly required and are added to facilitate proof-of-concept while GFET devices are located on a probe station physically separate from the IC and PCB. In future, DC-coupled operation will be supported with correct DC level-matching. Data was either recorded at the ADC output (for subsequent digital signal processing using MATLAB, Fig. 5.7), or recorded at the output of the FPGA to demonstrate real-time DSP demodulation (Fig. 5.9).

5.3.2 Measured FDM Results from GFET-CMOS System

The top row of Fig. 5.7 shows the transient waveform recorded by the ADC, comprising the sum of 5 kHz and 9 kHz modulated signals from GFET 1 and GFET 2). The second and third rows show the demodulated output signals associated with GFET 1 and GFET 2 respectively. The experiment was performed at two different DC gate bias voltages. When $V_g = -600\,\text{mV}$, dG/dV_g is negative, therefore, the sensor inverts the transient pulse ΔV_g. When $V_g = -360\,\text{mV}$, dG/dV_g is positive and the sensor is non-inverting.

Fig. 5.9 shows 1-channel demodulated output as we vary the strength of the simulated signal, ΔV_g. When $\Delta V_g = 25\,\text{mV}$, the conductance of the GFET is modulated by 6%. Extrapolating to the smaller ΔV_g, and comparing to the noise floor, we estimate that a modulation depth of 1% is detectable with our prototype design. This change in conductance would correspond to a 4 mV bioelectronic signal. While this demonstrates proof-of-concept for the GFET-FDM approach, further work is required to fully characterize and further minimize the noise floor of our system. By optimizing GFET fabrication and both AFE IC and DSP settings in future work, we anticipate that our FDM system can approach the $10\,\mu\text{V}$ detection limit reported for direct measurements of a single GFET device [64].

5.4 Conclusion

An FDM-based biosignal recording system was presented, which uses an array of graphene FET active electrodes for signal up-conversion directly at the sensor site. The architectural approach was validated using custom fabricated GFET devices, an AFE fabricated in 0.18 μm CMOS, and a digital back-end for signal demodulation. Experimental two-channel results demonstrate proof-of-concept for the GFET-FDM approach. This scalable architecture promises to enable significant wire count reduction for large-scale neural recording, and it partitions higher power sampling and demodulation functions to the back-end readout circuitry, where power is less constrained.

The use of atomically thin sensors is also promising for flexible substrates to provide dense, conformal neural sensor arrays for surface recordings. As an inherent tradeoff, maximum channel count be a function of input bandwidth, input dynamic range, modulation frequency, as well as of ADC sampling rate for this ADC-first approach. Future work will include increasing experimental channel count and *in vitro* testing with cultured neurons for biosignal validation. Long-term, this approach can support high-resolution active electrode arrays that simultaneously achieve high signal count, high spatial resolution, and sufficient temporal precision to infer functional interactions between neurons.

Chapter 6: Duty-Cycled Resistor and Frequency-Locked-Loop-based Wheatstone Bridge Interface for Low-Resistance Sensing Systems

6.1 Introduction

With broad applications in environmental sensing of temperature / humidity [5, 6] and barometric pressure [7], the growing need for ubiquitous, ultra-low-power sensors has driven continuous advancement in low-power performance and energy efficiency for their associated read-out circuits. For large sensor resistances (5 kΩ - 500 kΩ), a Wheatstone bridge circuit provides balanced readout with minimal power consumption. As the current required by a Wheatstone bridge is inversely proportional to the resistance of the sensor being measured, measuring small sensor resistances (<1 kΩ) with low power consumption presents a fundamental challenge that is increasingly necessary for a growing class of sensors for strain [66] and force [67] in wearable devices and robotics.

6.2 Low-powered and low-resistance sensing system

6.2.1 Overview of the approach

For a Wheatstone bridge (Fig. 6.1), power consumption is inversely proportional to the magnitude of the reference resistors (R_1, R_2, R_3) and the resistive sensor (R_{SEN}).

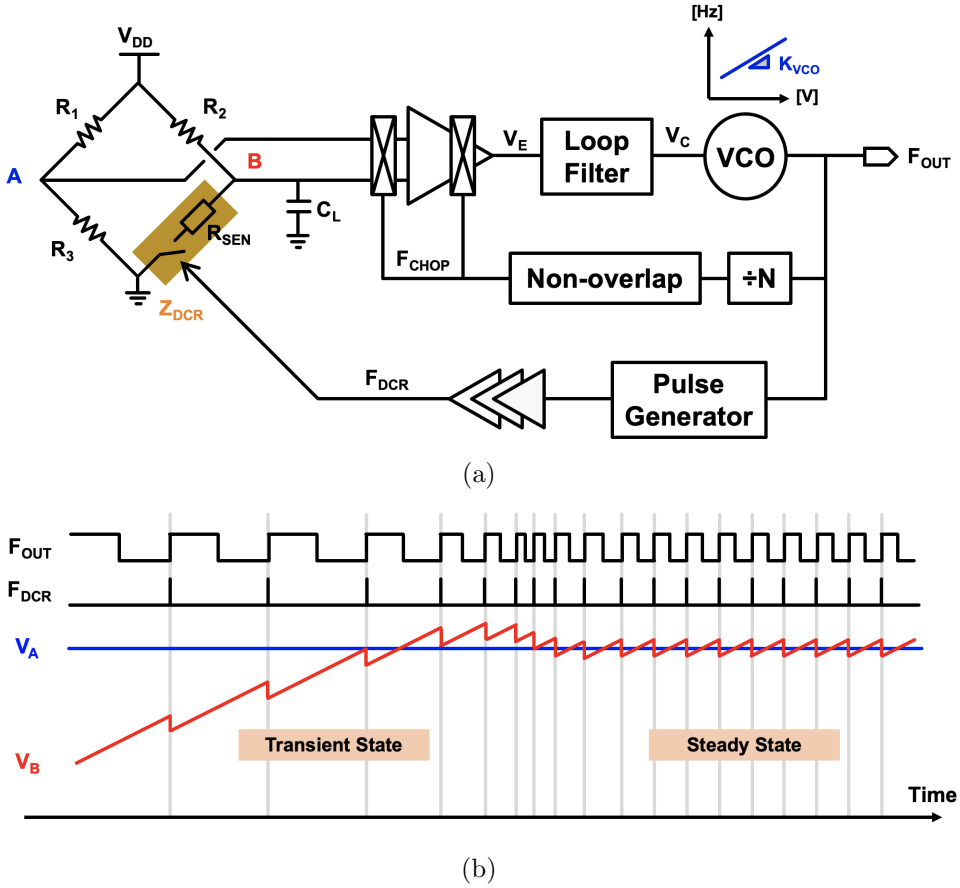


Figure 6.1: High-level architecture of the proposed DCR- and FLL-based low-resistance sensor: (a) Block diagram, (b) system operation waveforms.

For low resistance sensors ($\sim$ 1 Ω - 1 kΩ), a conventional Wheatstone bridge requires low-value reference resistors and a correspondingly large current to induce measurable voltage changes, increasing power consumption. In this dissertation, we boost the effective resistance of the resistive sensor branch using a duty-cycled resistor (DCR), which allows the use of large reference resistors even for small sensor resistance to minimize average power consumption. The Wheatstone bridge-based DCR is balanced using a frequency-locked loop (FLL) to automatically vary the output frequency as the value of the resistive sensor changes.

Fig. 6.1(a) shows the proposed architecture, comprising a switched Wheatstone bridge balanced by closed-loop feedback using a frequency-locked loop (FLL). This system consists of DCR-based Wheatstone bridge, error amplifier with chopping, loop filter, voltage-controlled oscillator (VCO), and a pulse generator. Bridge balance is controlled using fixed-width pulses of varying frequency. R_1, R_2, and R_3 use internal poly resistors (800 kΩ, 800 kΩ, and 400 kΩ). The ratio of R_1 and R_3 sets voltage of node A (V_A) to 0.6 V. A regular NMOS (Width/Length = 1000μm/0.18μm) is used as the DCR switch to achieve a low on-resistance ($\sim$1 Ω). A high switch on-resistance (R_{ON}) will increase the nonlinearity of the system when the sensor resistance (R_{SEN}) is small and DCR operation boosts both R_{SEN} and R_{ON}. An external load capacitor (C_L, 10 nF) is used to determine the average error voltage at V_B introduced by DCR. The error amplifier captures and amplifies the voltage difference between V_A and V_B.

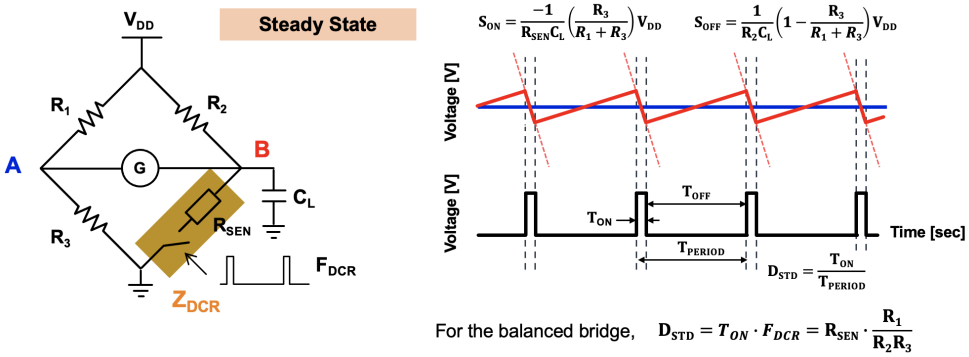
This error voltage (V_E) is converted to a control voltage (V_C) through a loop filter to stabilize the feedback system. The VCO converts the input, V_C, from the voltage domain to an output, F_{OUT}, in the frequency domain with corresponding VCO gain

factor (K_{VCO}). The pulse generator creates the pulse signal, F_{DCR}, with a fixed pulse width from F_{OUT}, where the frequency of F_{DCR} is equal to F_{OUT}. Lastly, digital buffers are placed at the output of the pulse generator to drive the gate capacitance of the DCR switch. A chopping technique is applied to the error amplifier to reduce the flicker noise of the amplifier itself. The chopping frequency, F_{CHOP}, is generated by dividing F_{OUT} by N (F_{CHOP}=F_{OUT}/N) without an additional clock generator to save area and power. Fig. 6.1(b) illustrates the waveforms of the system operation. By repeatedly charging and discharging C_L, V_B tracks towards the reference voltage, V_A, in the transient state. In steady-state, the average value of V_B matches V_A, and the charge and discharge time of C_L are balanced. The setting time to the steady state is designed to be less than 20 ms.

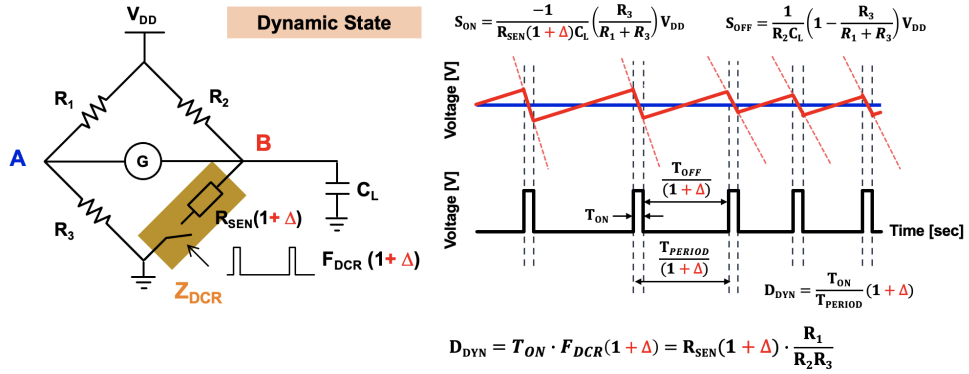
6.2.2 Implementation

Fig. 6.2 illustrates the key operation of the proposed architecture as applied to low-resistance measurements. Fig. 6.2(a) shows the behavior of a Wheatstone bridge when R_{SEN} is a fixed value. In steady-state operation of the balanced bridge, node A and B are held at the same value making the effective impedance of DCR (Z_{DCR}) equal to R_2R_3/R_1. To maintain a fixed voltage at B, C_L is charged when a DCR switch is turned on for a period (T_{ON}) and discharged equally to the amount of the charge during off-time (T_{OFF}). This can be written as:

$$\frac{1}{R_{SEN} \cdot C_L} \cdot (\frac{R_3}{R_1 + R_3}) \cdot V_{DD} \cdot T_{ON} = \frac{1}{R_2 \cdot C_L} \cdot (1 - \frac{R_3}{R_1 + R_3}) \cdot V_{DD} \cdot T_{OFF} \quad (6.1)$$



(a)



(b)

Figure 6.2: The balanced Wheatstone bridge circuits and waveforms showing its operation: (a) Steady state, (b) Dynamic state.

From (6.1), we can derive that $T_{ON}/T_{OFF} = R_{SEN}R_1/R_2R_3$. Since $T_{ON} << T_{OFF}$, we can assume that the period of a DCR switching (T_{PERIOD}) is approximately equal to T_{OFF}. Eqn. (6.1) can be simplified as $D_{STD} = R_{SEN}R_1/R_2R_3$, where D_{STD} is the duty cycle of the DCR in steady state. Fig. 6.2(b) describes an operation in the dynamic state, where R_{SEN} varies over time. The voltage slope of node B during on-time (S_{ON}) is inversely proportional to a change of R_{SEN}. Since the voltage slope of node B during off-time (S_{OFF}) is a fixed value, TOFF proportionally increases or decreases to keep the average voltage of node B to be same as node A. Under the same assumption, a change of T_{OFF} is equivalently achieved as a change of frequency for a fixed-width DCR pulse signal (ΔF_{DCR}). As $R_{SEN} = F_{DCR}T_{ON}R_2R_3/R_1$, by detecting this change in F_{DCR}, we can measure changes of a low-resistance R_{SEN} with low average power consumption due to low T_{ON}.

Fig. 6.3 describes the circuit implementation of key architecture blocks. The error amplifier is implemented using a PMOS-input folded-cascode single-ended OTA with chopping to achieve low-noise and high-gain (69 dB) operation. The VCO is implemented using a 9-stage current-starved ring oscillator to achieve low power consumption. A tunable capacitor (250 fF, 500 fF, and 750 fF) attached to each node of the ring oscillator enables a wide dynamic range (from 1 kHz to 100 kHz) of operation. The pulse generator, using a RC delay line, creates a pulse signal with few-nanosecond pulse width, which can be adjusted by programmable capacitors (from 32 fF to 256 fF).

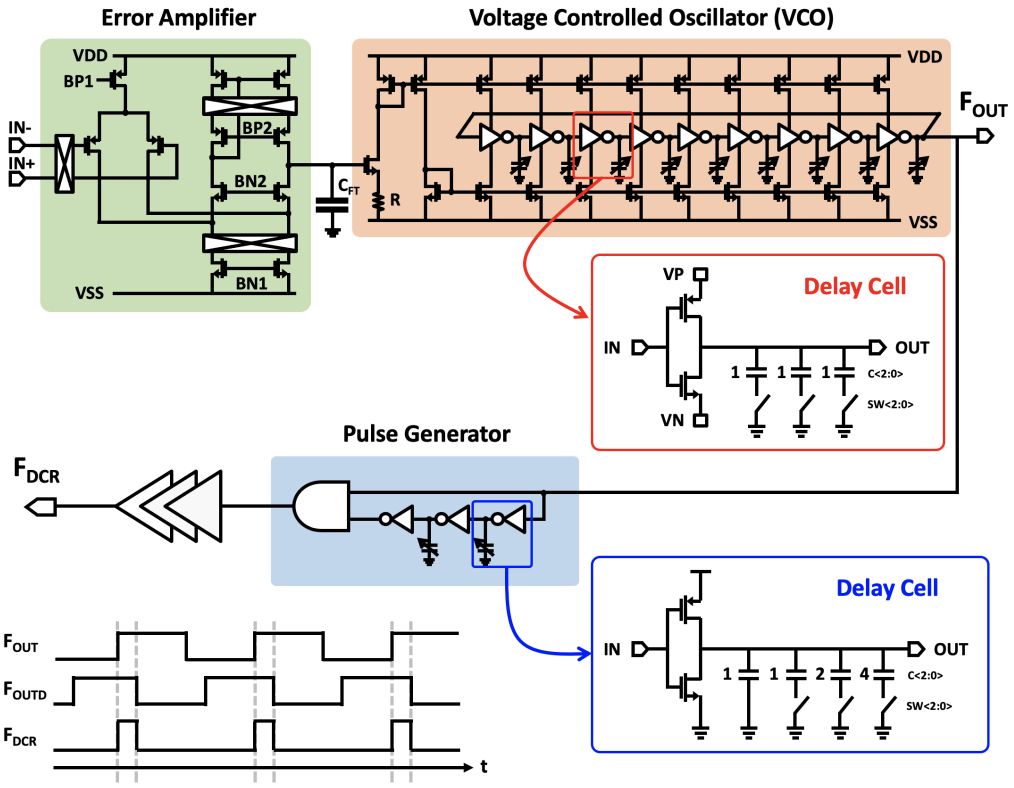


Figure 6.3: Schematic of implemented key building blocks: Error amplifier (top left), voltage controlled oscillator (VCO, top right), and pulse generator (center).

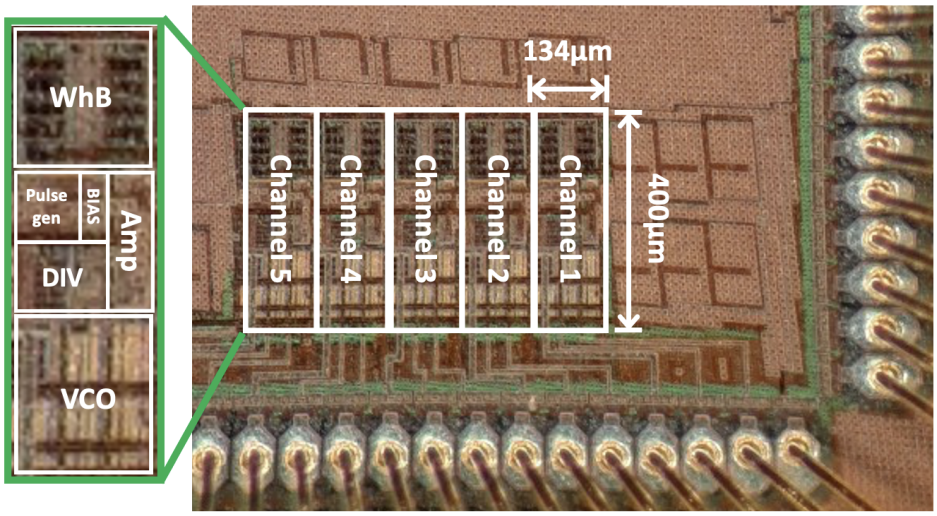


Figure 6.4: Die micrograph.

6.3 Measurement Results and Discussion

Five instances of the low-power, low-resistance measurement circuit were implemented in a prototype IC to make a five-channel low-resistance sensor system. Each channel occupies a die area of 134 μm x 400 μm, using an 0.18 μm silicon CMOS process; an annotated die micrograph is shown in Fig. 6.4. Finished ICs were packaged in two formats: an 84-pin Plastic Leaded Chip Carrier (PLCC) package for system characterization and performance testing, and a 44-pin quad flat package (QFP) to demonstrate a simultaneous five-channel readout system for a "smart glove" with a low-resistance strain sensor on each finger.

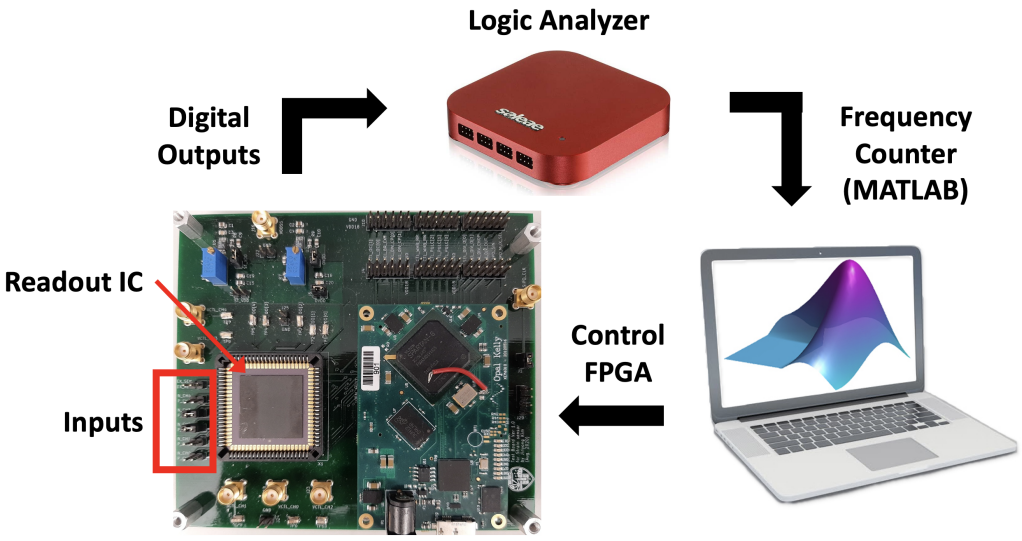


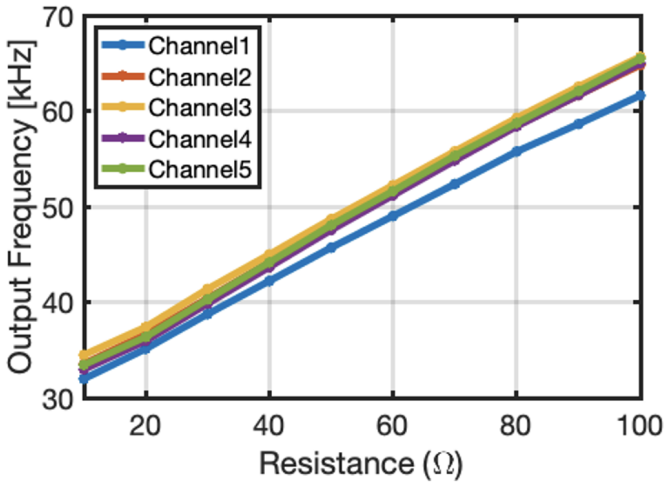
Figure 6.5: Experimental setup for resistance measurement system.

6.3.1 System characterization setup

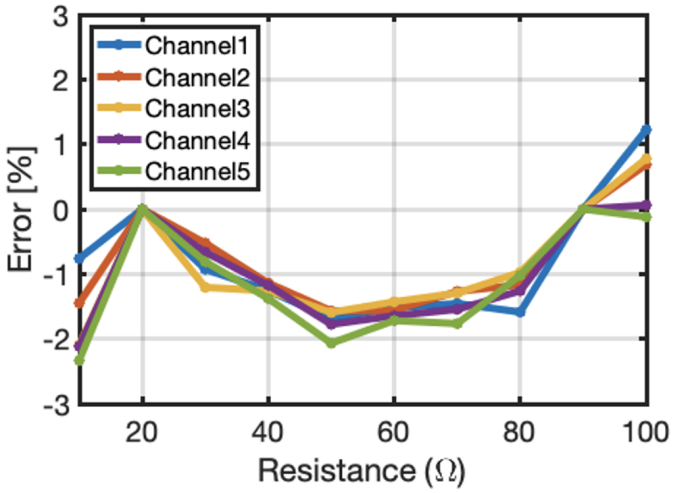
The experimental setup for the resistance sensor characterization is shown in Fig. 6.5. Control and digital interfacing is provided using a custom printed circuit board (PCB) with an on-board FPGA module (Opal Kelly XEM6310) and the five-channel readout IC packaged in a PLCC. A logic analyzer (Saleae Logic Pro 16) records the digital output data from IC and sends them to a host PC for analysis using a MATLAB interface.

6.3.2 Resistance measurement system characterization

Fig. 6.6(a) shows measured linearity, which is input resistance versus output frequency. Each channel has a unique offset due to variance in on-chip reference poly



(a)



(b)

Figure 6.6: Measured input resistance versus (a) output frequency and (b) output error.

resistors (R_1, R_2, and R_3). Fig. 6.6(b) describes frequency error following 2-point trimming for all 5 channels. A peak-to-peak inaccuracy of 3.5 % is achieved from 10 Ω to 100 Ω.

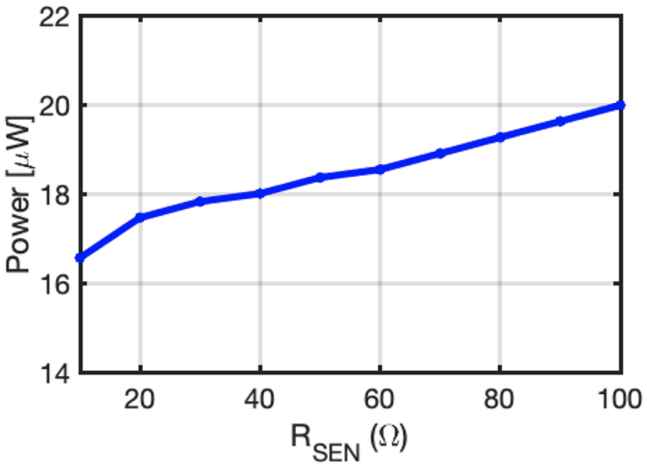
Fig. 6.7 shows the power consumption per channel. The largest portion of the power breakdown, nearly half of all power used, is the output-frequency-dependent VCO. Since the output frequency increases with sensor resistance, the total power consumption is proportional to the resistance, as shown in Fig. 6.7(a).

6.3.3 Demonstration of a single-channel resistance measurement system

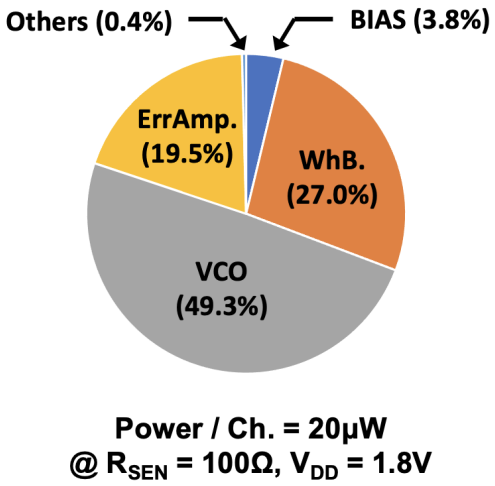
Fig. 6.8 illustrates a system-level demonstration using 5-30Ω stretchable strain sensors. The sensor resistance is varied by physically stretching the sensor, as might occur when used as a wearable sensor. The three measured cases of deformation, labeled in Fig. 6.8(a), correspond to three different output frequencies, shown in Fig. 6.8(b). Further, Fig. 6.9 shows a single channel demonstration for proof-of-concept of a "smart glove" with a strain sensor for each finger. The sensor resistance, and thus the output frequency of the circuit, increases as a finger is bent.

6.3.4 Demonstration of a robotic hand controlled by wearable glove

A hand-shaped, silicone- and liquid-metal-based five-channel strain sensor (Fig. 6.10, Left) was used as the sensor glove to demonstrate the utility of simultaneous five-

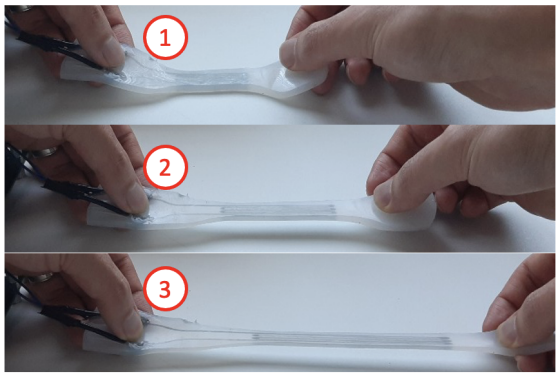


(a)

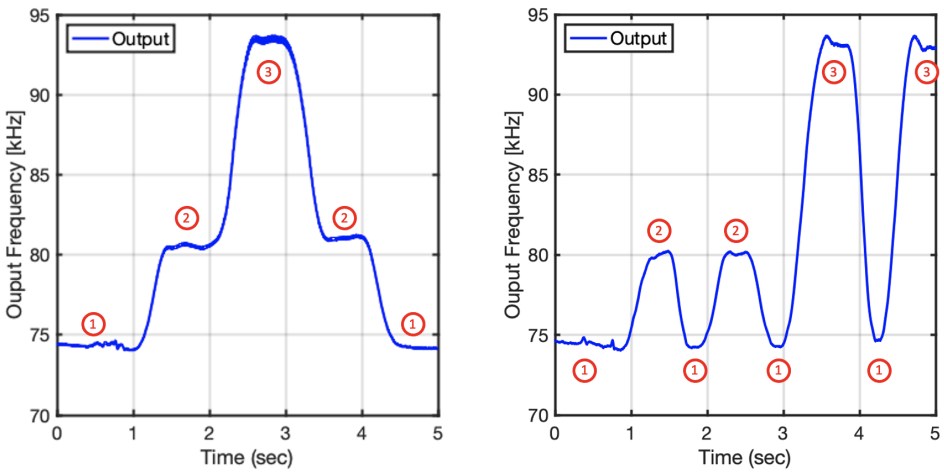


(b)

Figure 6.7: Measured (a) input resistance versus power consumption per channel and (b) power breakdown.

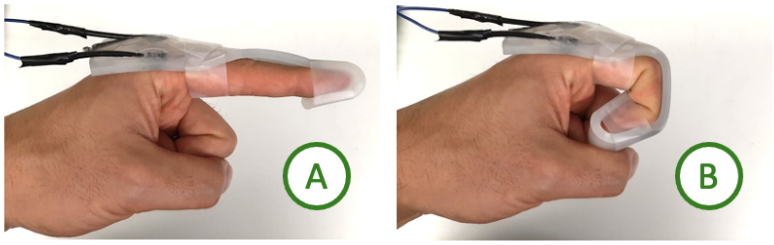


(a)

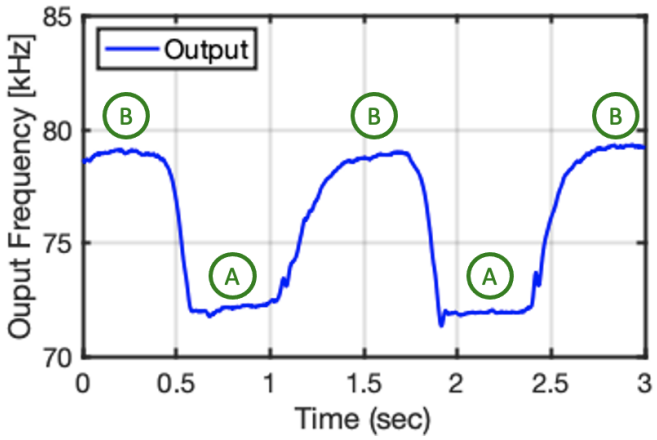


(b)

Figure 6.8: Demonstration of the implemented resistance measurement system using low-resistance, highly stretchable strain sensors.



(a)



(b)

Figure 6.9: Demonstration of the implemented resistance measurement system using low-resistance, highly stretchable strain sensors.

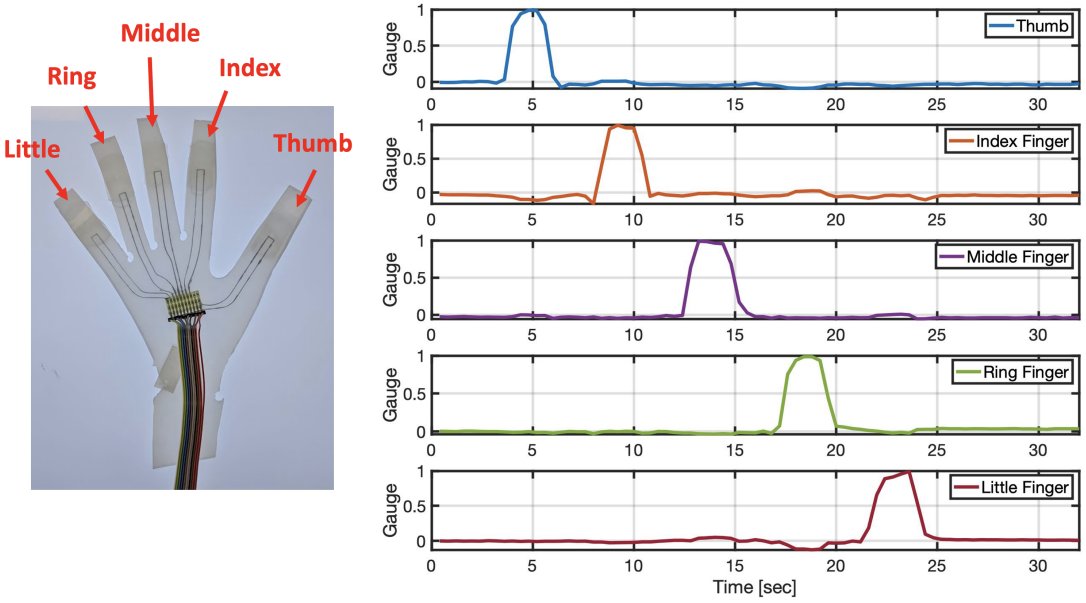


Figure 6.10: Demonstration of strain sensor glove fabricated using silicone and liquid metal paste

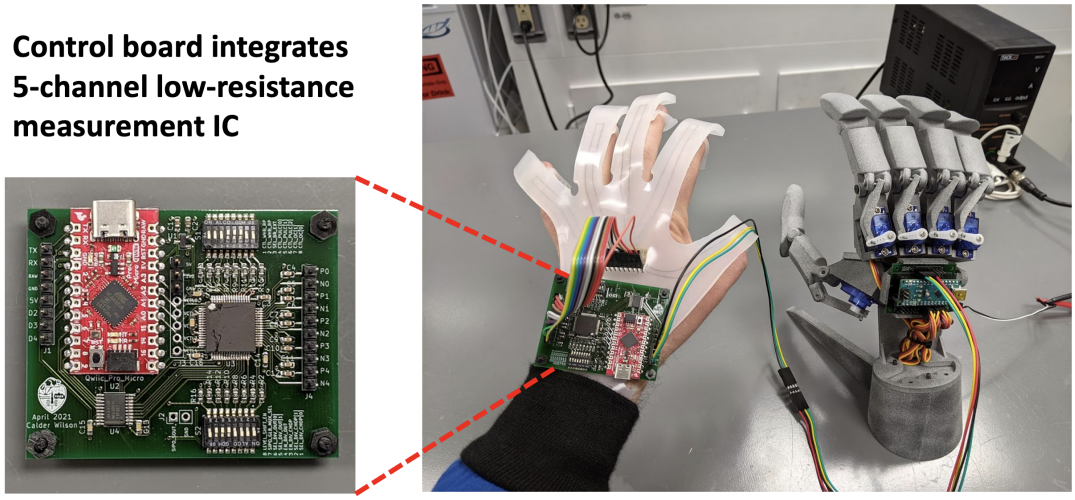


Figure 6.11: Demonstration of combined "smart glove" for controlling robotic hand or AR/VR visualizations

Table 6.1: Performance comparison with state-of-the-art

	ISSCC'20[6]	**CICC'19[7]**	**ISSCC'18[66]**	**Sens J'19[5]**	**This work**
Application	Temperature	Humidity/Temperature	Pressure	Strain	**Strain**
Architecture	WhB w/DSM	WhB w/SC+FLLe	WhB w/DCR	WhB	**WhB w/DCR+FLL**
Process [nm]	180	180	180	Off-chip	**180**
Supply Voltage [V]	1.8	1.5-2.0	3.6	5.0	**1.8**
Nominal Resistance [Ω]	370000	330000	6000	470	**10**
Dynamic Range [Ω]	-	-	-	10	**90**
Inaccuracy [%]	0.11	2.2/0.32	-	-	**3.5**
Power [μW]	55	15.6	0.52	50000	**20**
Area [mm^2]	0.11	0.72	1.7	-	**0.05**

WhB - Wheatstone Bridge DSM - Delta-Sigma Modulation DCR - Duty Cycle Resistor
FLL - Frequency Locked Loop SC - Switched Capacitor

channel readout by the five-channel, low-resistance, low-power (20 μW/channel) measurement IC. Fig. 6.10, Right shows output data from all five channels after digital processing by a microcontroller; each output corresponds with a finger of the sensor glove. This output can then be mapped to a servo position to control an associated robotic hand, as shown in Fig. 6.11. The mechanical fingers mimic the movement of each of the operator's fingers in real time.

6.4 Conclusion

Table 6.1 summarizes the performance of the implemented and tested DCR- & FLL-based Wheatstone bridge sensor readout IC and compares it to state-of-the-art resistive sensing using a conventional Wheatstone bridge. The presented sensor read-out architecture achieves similar power consumption as [7], despite a 33,000x smaller

nominal sensor resistance; conversely, compared to [5], the DCR-based architecture consumes 2,500x less power despite a 47x larger sensor resistance. This approach thus addresses the fundamental challenge in measuring low resistance sensors: power consumption of the measurement circuit generally increases as sensor resistance decreases. Minimal power consumption, as demonstrated here, is critically needed to increase the portability and battery life of future classes of intrinsically low-resistance sensors in wearable devices and soft robotic systems.

Chapter 7: Conclusions

This dissertation focused on new system-level architectures and circuit implementations for readout and multiplexing in multi-channel sensor systems.

The first presented approach was a frequency-division-multiplexing (FDM) technique, an approach used most coomonly in communication networks. The approach applied here to biosignal acquisition systems provides crucial benefits, such as wire count minimization and cable noise reduction, while recording all channels simultaneously. For proof-of-concept, in this dissertation, I described two FDM-based applications leveraging custom FDM front-end and back-end IC architectures: 1) biopotential signals (ECG and EMG) readout system and 2) neural recording system. A four-channel EMG system was demonstrated for a hand gesture recognition. Future work will include increasing channel count and demonstrating more complicated gesture recognition. Also, for neural sensing array, testing more channels and interfacing with cultured neurons will be included. This approach can achieve high-resolution and large-scale neural recording.

The second presented approach was a duty-cycled resistor (DCR) and auto-balancing frequency-locked-loop (FLL) for low-power, low-resistance measurement systems. The approach allows multi-channel, low resistance sensors to be implemented while significantly reducing the power consumption. As a proof-of-concept, a custom readout IC was combined with a motorized robotic hand controlled by five-channel stretchable

sensors implemented as a “smart glove” was demonstrated. Future work will include combining a physical robotic hand with smart glove and wireless/RF sensors, where it can perform wake-up and authentication functions as proof-of-principle for future secure, wearable, and batteryless sensor systems.

Bibliography

[1] W. Yu, M. Aslan, and G. C. Temes, "82 db sndr 20-channel incremental adc with optimal decimation filter and digital correction," in *IEEE Custom Integrated Circuits Conference 2010*. IEEE, 2010, pp. 1–4.

[2] X.-F. Teng, Y.-T. Zhang, C. C. Poon, and P. Bonato, "Wearable medical systems for p-health," *IEEE reviews in Biomedical engineering*, vol. 1, pp. 62–74, 2008.

[3] Y. M. Chi, T.-P. Jung, and G. Cauwenberghs, "Dry-contact and noncontact biopotential electrodes: Methodological review," *IEEE reviews in biomedical engineering*, vol. 3, pp. 106–119, 2010.

[4] S. J. Bensmaia and L. E. Miller, "Restoring sensorimotor function through intracortical interfaces: progress and looming challenges," *Nature Reviews Neuroscience*, vol. 15, no. 5, pp. 313–325, 2014.

[5] S. Pan and K. A. Makinwa, "3.6 a cmos resistor-based temperature sensor with a 10fj· k2 resolution fom and 0.4° c (30) inaccuracy from- 55° c to 125° c after a 1-point trim," in *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2020, pp. 68–70.

[6] H. Jiang, C.-C. Huang, M. Chan, and D. A. Hall, "A 2-in-1 temperature and humidity sensor achieving 62 fj· k 2 and 0.83 pj·(% rh) 2," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2019, pp. 1–4.

[7] S. Oh, Y. Shi, G. Kim, Y. Kim, T. Kang, S. Jeong, D. Sylvester, and D. Blaauw, "A 2.5 nj duty-cycled bridge-to-digital converter integrated in a 13mm 3 pressure-sensing system," in *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2018, pp. 328–330.

[8] H. Wang, Y. Chen, A. Hassibi, A. Scherer, and A. Hajimiri, "A Frequency-Shift CMOS Magnetic Biosensor Array with Single-Bead Sensitivity and No External Magnet," pp. 438–440, 2009.

[9] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE Journal of Solid-State Circuits*, 2007.

[10] G. Jung, M. W. Rashid, T. M. Carpenter, C. Tekes, D. M. J. Cowell, S. Freear, F. Levent Degertekin, and M. Ghovanloo, "Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography," in *IEEE International Solid-State Circuits Conference*, 2018, pp. 188–189.

[11] A. V. Jagtiani, J. Carletta, and J. Zhe, "A microfluidic multichannel resistive pulse sensor using frequency division multiplexing for high throughput counting of micro particles," *Journal of Micromechanics and Microengineering*, vol. 21, no. 6, 2011.

[12] H. Ouh, S. Member, and M. L. Johnston, "Code-Division Multiplex Encoding Analog Front End for Current-Mode Sensor Arrays," *IEEE Solid-State Circuits Letters*, vol. PP, no. c, p. 1, 2018.

[13] N. Wang, R. Liu, R. Khodambashi, N. Asmare, and A. F. Sarioglu, "Code-division multiplexed resistive pulse sensor networks for spatio-temporal detection of particles in microfluidic devices," in *Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, 2017.

[14] Y. Luo and C.-H. Heng, *An 8.2 μW 0.14 mm 2 16-Channel CDMA-Like Period Modulation Capacitance-to-Digital Converter with Reduced Data Throughput.*

[15] V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Márkus, J. Silva, and G. C. Temes, "A low-power 22-bit incremental adc," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1562–1571, 2006.

[16] L. Edenbrandt and O. Pahlm, "Vectorcardiogram synthesized from a 12-lead ecg: superiority of the inverse dower matrix," *Journal of electrocardiology*, vol. 21, no. 4, pp. 361–367, 1988.

[17] K. R. Daniel, D. M. Courtney, and J. A. Kline, "Assessment of cardiac stress from massive pulmonary embolism with 12-lead ecg," *Chest*, vol. 120, no. 2, pp. 474–481, 2001.

[18] R. Trobec, "Computer analysis of multichannel ecg," *Computers in biology and medicine*, vol. 33, no. 3, pp. 215–226, 2003.

[19] F. Negro, S. Muceli, A. M. Castronovo, A. Holobar, and D. Farina, "Multi-channel intramuscular and surface emg decomposition by convolutive blind source separation," *Journal of neural engineering*, vol. 13, no. 2, p. 026027, 2016.

[20] M.-F. Lucas, A. Gaufriau, S. Pascual, C. Doncarli, and D. Farina, "Multi-channel surface emg classification using support vector machines and signal-based wavelet optimization," *Biomedical Signal Processing and Control*, vol. 3, no. 2, pp. 169–174, 2008.

[21] E. Maarsingh, L. Van Eykern, A. Sprikkelman, M. Hoekstra, and W. Van Aalderen, "Respiratory muscle activity measured with a noninvasive emg technique: technical aspects and reproducibility," *Journal of Applied Physiology*, vol. 88, no. 6, pp. 1955–1961, 2000.

[22] A. Montavont, A. Kaminska, C. Soufflet, and D. Taussig, "Long-term eeg in children," *Neurophysiologie Clinique/Clinical Neurophysiology*, vol. 45, no. 1, pp. 81–85, 2015.

[23] J. Xu, S. Mitra, A. Matsumoto, S. Patki, C. Van Hoof, K. A. Makinwa, and R. F. Yazicioglu, "A wearable 8-channel active-electrode EEG/ETI acquisition system for body area networks," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 2005–2016, 2014.

[24] M. Guermandi, R. Cardu, E. F. Scarselli, and R. Guerrieri, "Active electrode ic for eeg and electrical impedance tomography with continuous monitoring of contact impedance," *IEEE transactions on biomedical circuits and systems*, vol. 9, no. 1, pp. 21–33, 2014.

[25] J. Xu, B. Büsze, C. Van Hoof, K. A. Makinwa, and R. F. Yazicioglu, "A 15-channel digital active electrode system for multi-parameter biopotential measurement," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2090–2100, 2015.

[26] J. Warchall, P. Theilmann, Y. Ouyang, H. Garudadri, and P. P. Mercier, "22.2 A rugged wearable modular ExG platform employing a distributed scalable multi-channel FM-ADC achieving 101dB input dynamic range and motion-artifact resilience," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, 2019, pp. 362–364.

[27] R. R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *IEEE Journal of solid-state circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[28] H. Chandrakumar and D. Marković, "5.5 A 2μW 40mVpp linear-input-range chopper-stabilized bio-signal amplifier with boosted input impedance of 300MΩ

and electrode-offset filtering," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 96–97.

[29] ——, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, 2017.

[30] J. Kim, H. Ouh, and M. L. Johnston, "A 43.8muw per channel biopotential readout system using frequency division multiplexing with cable motion artifact suppression," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2020, pp. 1–4.

[31] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μw 60 nv/$\sqrt{}$hz readout front-end for portable biopotential acquisition systems," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, 2007.

[32] X. Liu, M. Zhang, T. Xiong, A. G. Richardson, T. H. Lucas, P. S. Chin, R. Etienne-Cummings, T. D. Tran, and J. Van der Spiegel, "A fully integrated wireless compressed sensing neural signal acquisition system for chronic recording and brain machine interface," *IEEE Transactions on biomedical circuits and systems*, vol. 10, no. 4, pp. 874–883, 2016.

[33] H. Ouh and M. L. Johnston, "Code-division multiplex encoding analog front end for current-mode sensor arrays," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 118–121, 2018.

[34] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon, "Merged capacitor switching based sar adc with highest switching energy-efficiency," *Electronics letters*, vol. 46, no. 9, pp. 620–621, 2010.

[35] A. Paidimarri, D. Griffith, A. Wang, G. Burra, and A. P. Chandrakasan, "An RC oscillator with comparator offset cancellation," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1866–1877, 2016.

[36] K. A. Ng and Y. P. Xu, "A compact, low input capacitance neural recording amplifier," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 5, pp. 610–620, 2013.

[37] ——, "A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 724–737, 2016.

[38] J. Kim, H. Ouh, and M. L. Johnston, "A sub-hertz bandpass low noise amplifier for biopotential signal acquisition with parasitic pole cancellation," in *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2020, pp. 13–16.

[39] T. Tang, W. L. Goh, L. Yao, and Y. Gao, "A tdm-based 16-channel afe asic with enhanced system-level cmrr for wearable eeg recording with dry electrodes," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 14, no. 3, pp. 516–524, 2020.

[40] L. Zeng, B. Liu, and C.-H. Heng, "A dual-loop eight-channel ECG recording system with fast settling mode for 12-lead applications," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1895–1906, 2019.

[41] B. Liu, G. Wang, Y. Li, L. Zeng, H. Li, Y. Gao, Y. Ma, Y. Lian, and C.-H. Heng, "A 13-channel 1.53-mw 11.28-mm 2 electrical impedance tomography soc based on frequency division multiplexing for lung physiological imaging," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 5, pp. 938–949, 2019.

[42] G. B. Moody and R. G. Mark, "The impact of the mit-bih arrhythmia database," *IEEE Engineering in Medicine and Biology Magazine*, vol. 20, no. 3, pp. 45–50, 2001.

[43] J. Xu, S. Mitra, C. Van Hoof, R. F. Yazicioglu, and K. A. Makinwa, "Active electrodes for wearable eeg acquisition: Review and electronics design methodology," *IEEE reviews in biomedical engineering*, vol. 10, pp. 187–198, 2017.

[44] A. Baba and M. Burke, "Measurement of the electrical properties of ungelled ecg electrodes," *Int. J. Biol. Biomed. Eng*, vol. 2, no. 3, pp. 89–97, 2008.

[45] J. Dawes, M. Brian, H. Bialek, and M. L. Johnston, "Wireless smartphone control using electromyography and automated gesture recognition," in *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. IEEE, 2018, pp. 5390–5393.

[46] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 200 μw eight-channel eeg acquisition asic for ambulatory eeg systems," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, 2008.

[47] B. K. Vasan, S. K. Sudani, D. J. Chen, and R. L. Geiger, "Low-distortion sine wave generation using a novel harmonic cancellation technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1122–1134, 2013.

[48] F. Gerhard, T. Kispersky, G. J. Gutierrez, E. Marder, M. Kramer, and U. Eden, "Successful reconstruction of a physiological circuit with known connectivity from spiking activity alone," *PLoS Computational Biologoy*, vol. 9, no. 7, p. e1003138, 2013.

[49] C. M. Lopez, "Unraveling the brain with high-density CMOS neural probes: tackling the challenges of neural interfacing," *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 43–50, 2019.

[50] C. M. Lopez, J. Putzeys, B. C. Raducanu, M. Ballini, S. Wang, A. Andrei, V. Rochus, R. Vandebriel, S. Severi, C. Van Hoof *et al.*, "A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13μm SOI CMOS," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 3, pp. 510–522, 2017.

[51] R. M. Walker, H. Gao, P. Nuyujukian, K. Makinwa, K. Shenoy, T. Meng, and B. Murmann, "A 96-channel full data rate direct neural interface in 0.13 μm CMOS," in *2011 Symposium on VLSI Circuits-Digest of Technical Papers*. IEEE, 2011, pp. 144–145.

[52] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation interface," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 3, pp. 149–161, 2010.

[53] A. Bagheri, M. T. Salam, J. L. P. Velazquez, and R. Genov, "Low-frequency noise and offset rejection in DC-coupled neural amplifiers: A review and digitally-assisted design tutorial," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 1, pp. 161–176, 2016.

[54] G. O'Leary, D. M. Groppe, T. A. Valiante, N. Verma, and R. Genov, "NURIP: Neural interface processor for brain-state classification and programmable-waveform neurostimulation," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3150–3162, 2018.

[55] S. Shekar, K. Jayant, M. A. Rabadan, R. Tomer, R. Yuste, and K. L. Shepard, "A miniaturized multi-clamp CMOS amplifier for intracellular neural recording," *Nature Electronics*, vol. 2, no. 8, pp. 343–350, 2019.

[56] K. D. Harris, R. Q. Quiroga, J. Freeman, and S. L. Smith, "Improving data quality in neuronal population recordings," *Nature Neuroscience*, vol. 19, no. 9, pp. 1165–1174, 2016.

[57] D. Khodagholy, J. N. Gelinas, Z. Zhao, M. Yeh, M. Long, J. D. Greenlee, W. Doyle, O. Devinsky, and G. Buzsáki, "Organic electronics for high-resolution electrocorticography of the human brain," *Science Advances*, vol. 2, no. 11, p. e1601027, 2016.

[58] J. J. Jun, N. A. Steinmetz, J. H. Siegle, D. J. Denman, M. Bauza, B. Barbarits, A. K. Lee, C. A. Anastassiou, A. Andrei, Ç. Aydın *et al.*, "Fully integrated silicon probes for high-density recording of neural activity," *Nature*, vol. 551, no. 7679, pp. 232–236, 2017.

[59] R. Shulyzki, K. Abdelhalim, A. Bagheri, M. T. Salam, C. M. Florez, J. L. P. Velazquez, P. L. Carlen, and R. Genov, "320-channel active probe for high-resolution neuromonitoring and responsive neurostimulation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 1, pp. 34–49, 2014.

[60] S. Wang, S. K. Garakoui, H. Chun, D. G. Salinas, W. Sijbers, J. Putzeys, E. Martens, J. Craninckx, N. Van Helleputte, and C. M. Lopez, "A compact quad-shank CMOS neural probe with 5,120 addressable recording sites and 384 fully differential parallel channels," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1625–1634, 2019.

[61] R. Chen, A. Canales, and P. Anikeeva, "Neural recording and modulation technologies," *Nature Reviews Materials*, vol. 2, no. 2, pp. 1–16, 2017.

[62] D. Khodagholy, J. N. Gelinas, T. Thesen, W. Doyle, O. Devinsky, G. G. Malliaras, and G. Buzsáki, "NeuroGrid: recording action potentials from the surface of the brain," *Nature Neuroscience*, vol. 18, no. 2, pp. 310–315, 2015.

[63] C. Hebert, E. Masvidal-Codina, A. Suarez-Perez, A. Bonaccini Calia, G. Piret, R. Garcia-Cortadella, X. Illa, E. Del Corro Garcia, J. M. De la Cruz Sanchez, D. Viana Casals, E. Prats-Alfonso, J. Bousquet, P. Godignon, B. Yvert, R. Villa, M. V. Sanchez-Vives, A. Guimera-Brunet, and J. A. Garrido, "Flexible

graphene solution-gated field-effect transistors: efficient transducers for micro-electrocorticography," *Advanced Functional Materials*, vol. 28, no. 12, pp. 1–15, 2018.

[64] B. M. Blaschke, N. Tort-Colet, A. Guimerà-Brunet, J. Weinert, L. Rousseau, A. Heimann, S. Drieschner, O. Kempski, R. Villa, M. V. Sanchez-Vives *et al.*, "Mapping brain activity with flexible graphene micro-transistors," *2D Materials*, vol. 4, no. 2, p. 025040, 2017.

[65] D. Kireev, S. Seyock, M. Ernst, V. Maybeck, B. Wolfrum, and A. Offenhausser, "Versatile flexible graphene multielectrode arrays," *Biosensors*, vol. 7, no. 1, pp. 1–9, 2017.

[66] C. Votzke, U. Daalkhaijav, Y. Mengüç, and M. L. Johnston, "3d-printed liquid metal interconnects for stretchable electronics," *IEEE Sensors Journal*, vol. 19, no. 10, pp. 3832–3840, 2019.

[67] Y. Wang, Y. Lu, D. Mei, and L. Zhu, "Liquid metal-based wearable tactile sensor for both temperature and contact force sensing," *IEEE Sensors Journal*, vol. 21, no. 2, pp. 1694–1703, 2020.