AN ABSTRACT OF THE DISSERTATION OF

Praveen Kumar Venkatachala for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on August 23, 2019.

Title: Design Considerations and Circuit Techniques for Robust ringamps

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Ring amplifiers (ringamps) have shown excellent power efficiency in the latest state-of-the-art analog to digital converters (ADCs). This thesis describes circuit techniques to ensure robust operation of ringamps using standard analog techniques and proportional-integral-derivative (PID) controller analogy. Large-signal and small-signal analysis of a ringamp are performed using simple RC settling and operational transconductance amplifier (OTA) based analysis.

Dead-zone regulation technique is discussed which employs replica biasing and current mirrors for PVT-tolerant operation of ringamp. A passive-compensation technique is discussed for improved large-signal response of ringamps.

Design Considerations and Circuit Techniques for Robust ringamps

by

Praveen Kumar Venkatachala

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APPROVED:

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Praveen Kumar Venkatachala, Author

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Chapter 1: Introduction

1.1 Ring Amplifiers As We Know So Far

The ring amplifier (ringamp) (Fig. 1.1) was first introduced by Ben Hershberg [1] as a power efficient and scalable alternative to traditional operational transconductance amplifiers (OTAs) in switched capacitor (SC) circuits and systems such as Analog to Digital Converters (ADCs).

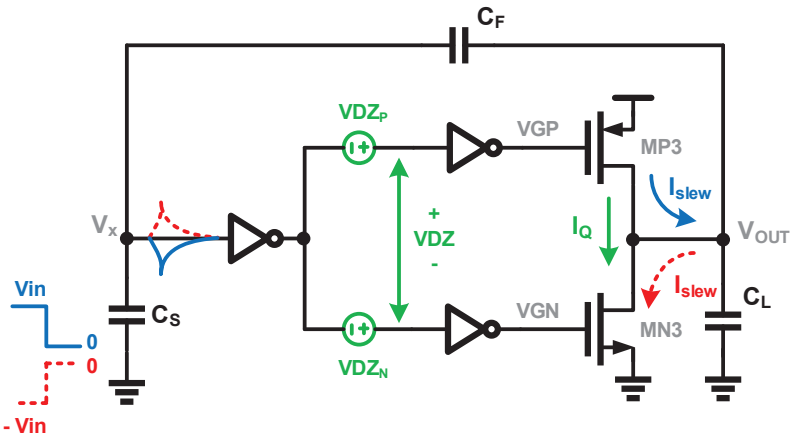

Figure 1.1: Ringamp: Basic structure and operation

A ringamp in steady-state is a multi-stage transconductance structure with the first two stages boosting the transconductance of the output stage. The feedback loop is compensated by biasing the output stage with a very low quiescent current. Typically this bias is defined as the deadzone voltage as depicted in Fig. 1.1. The

low quiescent current ensures a dominant pole at the output that stabilizes the loop. However, when a step input is applied, the first two stages act as digital inverters that momentarily turn on the output stage. During this phase the ringamp operates in large-signal state causing the load capacitor to charge quickly. As the output voltage across the capacitor builds up and approaches close to the final steady state value, the negative feedback brings the ringamp back to its low quiescent current small-signal state.

Although several alternatives such as dynamic-amplifiers [2, 3], zero-crossing-detector (ZCD) based amplifiers [4], amplifiers with incomplete settling [5] have been trending over the years as scalable amplifier solutions, most of these solutions require calibration or timing control that increase their complexity. Ringamps are unique because they are self-regulated and perform similar to dynamic-amplifiers and ZCD based amplifiers. Ringamps also offer a multi-stage structure that can help them achieve higher gains in sub-micron CMOS process without any need for calibration. In addition, ringamps can be implemented with simple inverters which makes them more scalable. Thus, the power-efficient dynamic operation, self-regulated amplification, simple inverter-based structure, calibration-free and scalable architecture have resulted in increased popularity of ringamps over recent years.

Over recent years several state-of-the-art ADCs have demonstrated the use of ringamps for power-efficient residue amplification[6, 7, 8, 9]. A few ADCs have also utilized the behavior of the internal nodes of ringamps to enable system enhancements such as comparator-less flash ADC operation [6], averaging corrleted-level-shifting operation [10] and asynchronous pipeline ADC operation [11]. A recent work has

demonstrated fast-transient LDOs using a ringamp as the error amplifier [12].

With such increased popularity of ringamps, a systematic analysis and design flow of ringamps needs to be developed to understand the operation of the ringamps in terms of standard analog design parameters. This can help analog designers to assess the robustness of ringamps and their associated systems using fundamental circuit techniques.

1.2 Common Concerns About Ringamps

A few common concerns about ringamps are summarized below.

Concern 1. PVT variations: Given the fact that ringamps are inverter-based amplifiers, a common concern is their sensitivity to PVT variations. This thesis discusses simple techniques in Chapter 3 and Chapter 4 to address this concern.

Concern 2. Ringing in large-signal step response: A discussion on transient response in [6] shows that even with a 70 degree phase margin depicted by small-signal analysis, the step response of a ringamp shows oscillations. The alternate ringamp structure in [6] offers to minimize these oscillations. However, the ringing in the transient response of a traditional ringamp remains unexplained as the standard small-signal analysis fails to capture the large-signal response. Another alternate ringamp structure in [9] offers to minimize these oscillations by combining a low-threshold-voltage (LVT) and high-threshold-voltage (HVT) transistors. The LVT-HVT combination in [9] ensures smooth I-V characteristics to minimize abrupt large-signal transients. This thesis discusses large-signal and small-signal responses

of a ringamp in a general sense irrespective of specific ringamp strucures in Chapter 2. The discussion aims to distinguish the small-signal and large-signal operations of a ringamp and establish guidelines for reduced overshoot and ringing in a ringamp transient response. A large-signal compensation technique is discussed in Chapter 4. This technique is generic to SC amplifiers and can be implemented independent of the ringamp architecture.

Concern 3. Is it an Oscillator based amplifier?: In the original literature where ringamp is introduced [1], the basic operation is described in comparison to ring-oscillators. The choice of the deadzone-voltage (defined in [1]) pushes the ring-oscillator behavior towards a self-regulating amplifier response. Although this provides a very simple and elegant way of describing the basic operation of ringamps, a common misconception is that ringamps are inherently oscillators. In this thesis we show that ringamps in their steady state are stable amplifiers by design. Although it is debatable that any amplifier in negative feedback could be turned into an oscillator if additional phase-shifts in the loop result in a net positive-feedback. However, ringamps in their natural steady state are stable amplifiers in negative feedback by design.

1.3 The Main Take-away and Organization of Thesis

Since the introduction of ringamps, several analog techniques considering small-signal analysis and architectural enhancements have lead to improved operation of ringamps. A few criteria can be identified in literature [13] for power-speed tradeoff, cmfb and

autozero noise. The work in [9] discusses noise-power tradeoff and bias-sensitivity. Most of these analyses are specific to the ADC systems where the respective ringamps are implemented and used. The work in [14] applies gm-over-id techniques for class-AB ringamps. However, the techniques in [14] do not discuss stability and large-signal analysis required to ensure robust ringamp operation. For fair comparison between OTAs and ringamps, a general analysis of what happens when OTAs are replaced by ringamps is necessary to understand the tradeoffs in accuracy-speed-noise-stability-power. In addition, to get a complete picture of ringamp operation an analysis considering both large-signal and small-signal operation of a ringamp is required so that designers can analyze the clear advantages or disadvantages of ringamps over OTAs.

This leads us to the story of this thesis. Here we take a step towards developing a general intuition to understand both large-signal and small-signal operation of ringamps in SC circuits. This intuitive understanding can be used to develop a systematic design procedure when ringamps are used as SC amplifiers. Simple RC models and proportional-integral-derivative (PID) controller analogy are brought together to understand the step-response of ringamps. Conventional OTA based analysis is used as a baseline to understand noise and small-signal response (few of these concepts can also be found in [9, 13, 14]).

The organization of the thesis is as follows. Chapter 2 compares the operation of a single-stage OTA, a single-stage class AB inverter-based amplifier and a ringamp in a SC amplifier. The qualitative differences in step-response and dc characteristics are discussed, followed by the use of simple RC models and small-signal models to

quantify the transient response of ringamps. These models help translate ringamp step-response parameters into transistor design parameters. Chapter 3 discusses the effect of transistor variations and a simple biasing technique to improve the robustness of ringamps to PVT variations. Chapter 4 discusses a simple compensation technique called passive-compensation to enhance the robustness of ringamps in the presence of large-signal delays in the loop. Chapter 5 concludes the thesis.

Chapter 2: Analyzing Ringamps Using Standard Analog Techniques

2.1 Qualitative Comparison of OTAs, Inverter-Based Amplifiers and Ringamps in a SC Amplifier

In this section the transient voltage/current responses in a SC amplifier, the dc I-V characteristics and the dc transfer characteristics are used to draw qualitative comparisons between a standard single-stage OTA [15], a single-stage class AB inverter-based amplifier (IBA) [16] and a ringamp [1].

Consider the SC amplifier as shown in Fig. 2.1. ϕ_S and ϕ_A are non-overlapping clock phases of the SC amplifier. The input is sampled across the bottom plate of the capacitor C_S at the end of the clock phase ϕ_{Se}. The feedback capacitor C_S and the OTA are reset during the sampling phase ϕ_S. During the amplification phase ϕ_A, the bottom plate of the capacitor is switched to common mode voltage V_{CM}. The sampled charge across the capacitor is now transferred to the feedback capacitor C_F. The OTA tries to keep the node Vx constant (maintains virtual ground through negative feedback) by supplying the required output current. This results in the output step voltage with a gain of C_S/C_F .

As shown in Fig. 2.2, the charge transfer operation can be viewed as a step input applied at the bottom plate of the capacitor C_S followed by the step response at the output of the closed loop amplifier. The rest of the section assumes that the OTA,

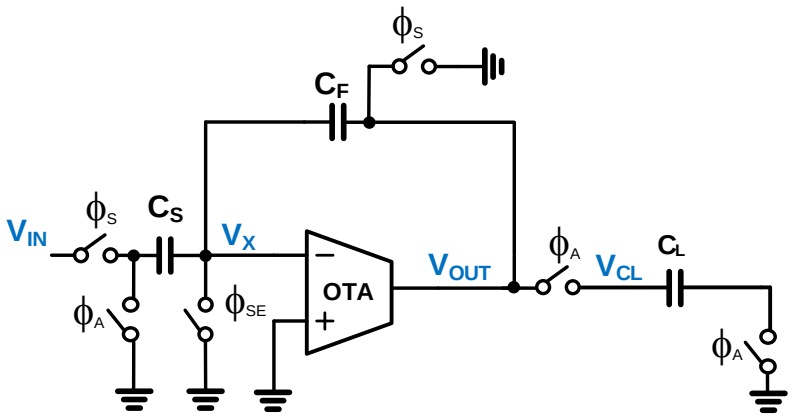

Figure 2.1: Switched capacitor amplifier setup

IBA and ringamp are used in a differential SC amplifier setup.

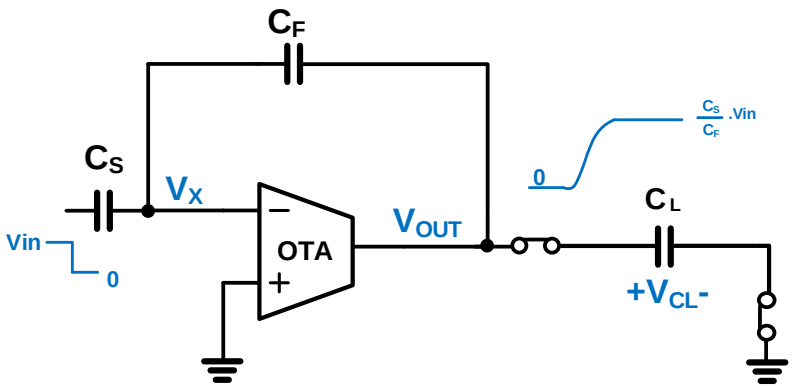

Figure 2.2: Charge transfer as step response

2.1.1 Operational Transconductance Amplifiers (OTAs)

Fig 2.3 shows the schematic of a differential OTA with NMOS input pair, ideal current source load and a tail current source I_{tail}. Fig. 2.4 shows the I-V characteristics of the

OTA. For small-signal input, the slope of I-V curve corresponds to the small-signal transconductance, gm. For large-signal input (greater than I_{tail}/gm), the output current saturates to I_{tail}.

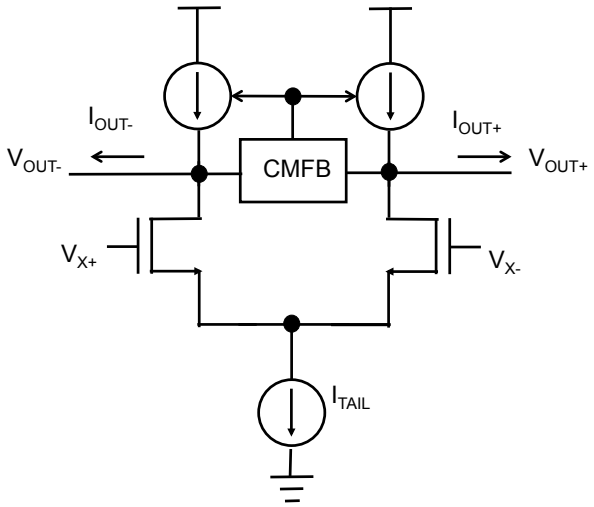

Figure 2.3: Schematic of a single-stage OTA

Fig. 2.5 shows the transient response of an OTA for a large-signal step input. For a large input step the speed of the OTA response is limited by slew-rate (SR) where the load capacitor is initially charged with a constant current, I_{tail} followed by a small-signal current for the rest of the settling. The small-signal current is a function of the transconductance (gm) of the input pair which results in a linear settling response.

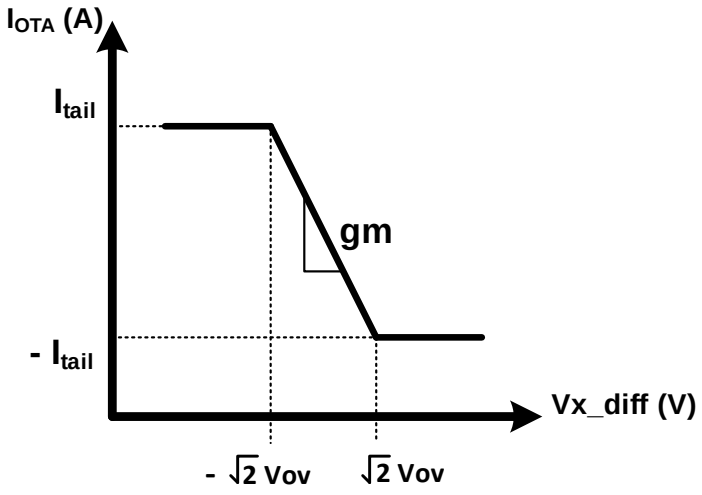

Figure 2.4: I-V characteristics of a single-stage OTA

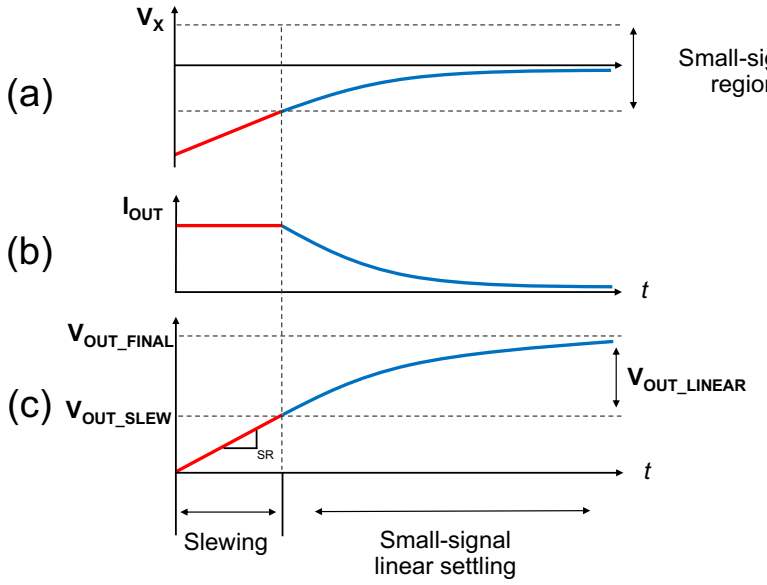

Figure 2.5: OTA transient response (a)Virtual ground node Vx (b) Differential output current I_{Out} (c) Differential output voltage

The slew rate is given by

$$SR = \frac{dV_{out}}{dt} = \frac{I_{tail}}{C_{out}} \tag{2.1}$$

where *Cout* is the total load capacitance as seen by the amplifier,

$$C_{out} = C_L + (1 - \beta)C_F \tag{2.2}$$

Faster settling response requires faster slew rate to reduce the slewing time. In addition, faster small-signal settling requires higher gm. Both of these conditions demand for higher current consumption to achieve faster settling response. These tradeoff discussions are found in standard text books [15, 17].

2.1.2 Inverter-based Amplifiers (IBAs)

Fig. 2.6 shows the schematic of an IBA (single-ended schematic shown for simplicity). Fig. 2.7 shows the I-V characteristics of the IBA with optimum bias voltages. The optimum bias voltages define the slope of the I-V curve (gm) for small-signal input. For large-signal input, the slope of the I-V curve is non-linear resulting in a non-linear large-signal transconductance denoted by Gm.

Fig. 2.8 shows the transient response of an IBA for a large-signal step input. The non-linear I-V characteristics results in a dynamic operation in the IBA. Due to the dynamic operation the load capacitor is initially charged with a high current (function of the large-signal Gm) followed by a small-signal current (function of the small-signal

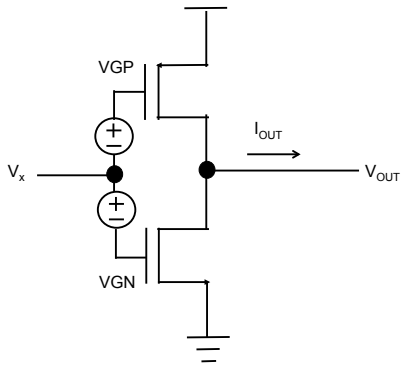

Figure 2.6: Schematic of a single-stage class-AB inverter-based amplifier (IBA)

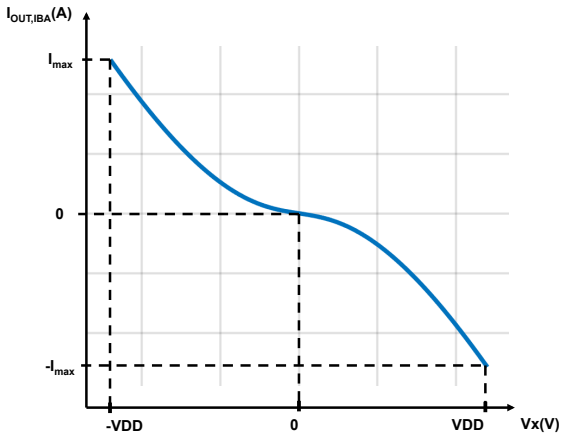

Figure 2.7: I-V characteristics of a single-stage IBA

gm) towards the end of the transient response. Thus for the same average current consumption of that of an OTA, the initial non-linear settling boosts the speed of the IBA. In other words, for the same settling time as that of an OTA, the initial non-linear settling reduces the average current consumption of the IBA.

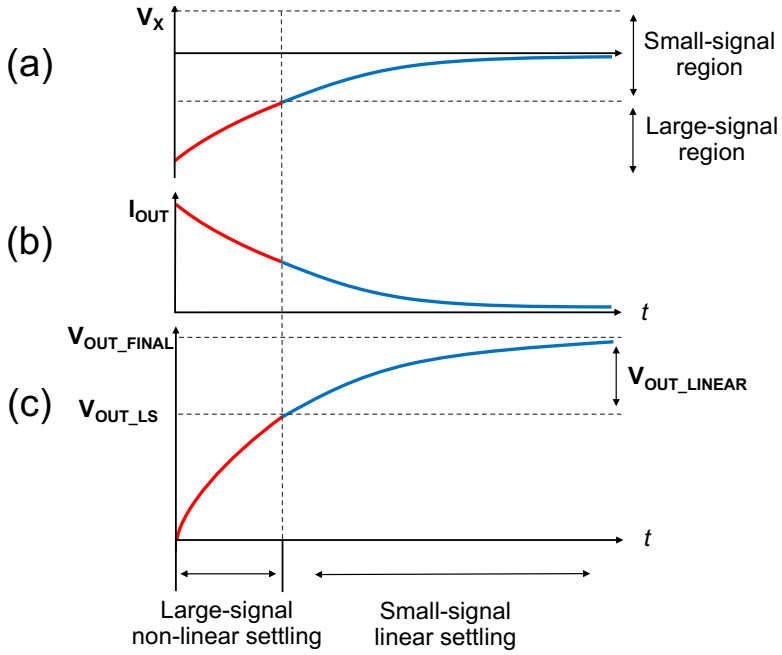

Figure 2.8: IBA transient response (a) Differential virtual ground node voltage (b) Differential output current (c) Differential Output Voltage

2.1.3 Ring Amplifiers (Ringamps)

Fig. 2.9 shows the schematic of a ringamp (single-ended schematic shown for simplicity). Fig. 2.10 shows the overall I-V characteristics of the ringamp with optimum bias voltages VDZ_P and VDZ_N. The optimum bias voltages define the slope of the I-V

curve (gm) for small-signal input. The larger the bias voltages, the wider the input range for which the output current is close to zero. For this reason, the bias voltages in ringamp are defined as the 'deadzone' control voltages [1]. For large-signal input, the slope of the I-V curve is non-linear resulting in a non-linear large-signal transconductance denoted by Gm. The overall I-V curve of the ringamp is a combination of the transfer characteristics of the first two stages shown in Fig. 2.11 and the I-V characteristics of the third stage as shown in Fig. 2.7.

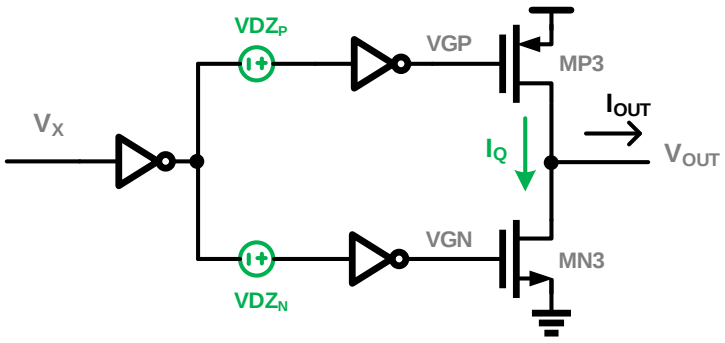

Figure 2.9: Schematic of a ringamp

The additional large-signal feature that distinguishes a ringamp from a single-stage IBA is seen by considering the initial transient response shown in Fig. 2.12. For a large-signal step input, the output of the second-stage (VGP in Fig. 2.12) reaches close to rail-to-rail voltage. This momentarily results in a large overdrive for one of the output-stage transistors (PMOS in this case), while the output voltage charges towards the final value. Since the gate-source voltage during this phase is constant while the drain-source voltage is changing, the output current during this

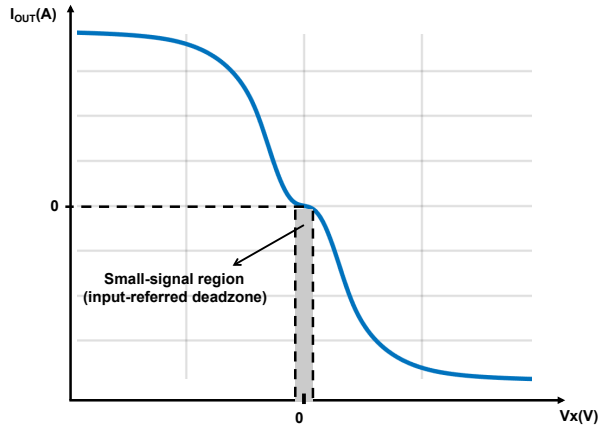

Figure 2.10: I-V characteristics of a ringamp

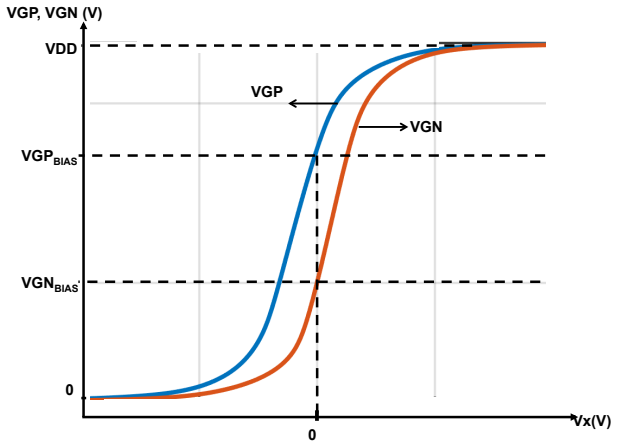

Figure 2.11: V-V transfer characteristics of the first two stages of a ringamp

initial settling is a function of the on resistance, R_{ON} of the output stage PMOS transistor. The R_{ON} is also a function of the fixed VGP during this phase. This initial RC settling phase charges the load capacitance with an impulse-like current.

Followed by the quick initial RC settling phase, when the feedback from the output reaches back to VGP, the gate-source voltage starts to change, while the drain-source voltage has almost settled closer to the final value. The output current during this phase is a function of the large-signal Gm of the ringamp, which is a function of the large-signal gain of the combined first two stages and the non-linear large-signal Gm of the output stage.

Finally, when the output voltage approaches close to the final value, small-signal operation completes the rest of the settling. To summarize, the overall transient response of a ringamp can be divided into a three-phase dynamic operation: the initial RC settling phase, the intermediate large-signal settling phase and the final small-signal settling phase. During the initial phase, the large output current decays similar to RC settling. During the intermediate phase, the output current decays as a function of the large-signal Gm. During the final phase, the output current is a function of the small-signal gm.

The speed of the ringamp is faster than a single-stage inverter-based amplifier (for the same power of an IBA) due to the three-phase dynamic operation. The initial phase of the dynamic operation charges the load capacitance with an impulse-like current, followed by a dynamic current during the intermediate phase and then followed by a small-signal current towards the end of the transient response. Thus for the same average current consumption of that of an OTA, the initial RC based settling

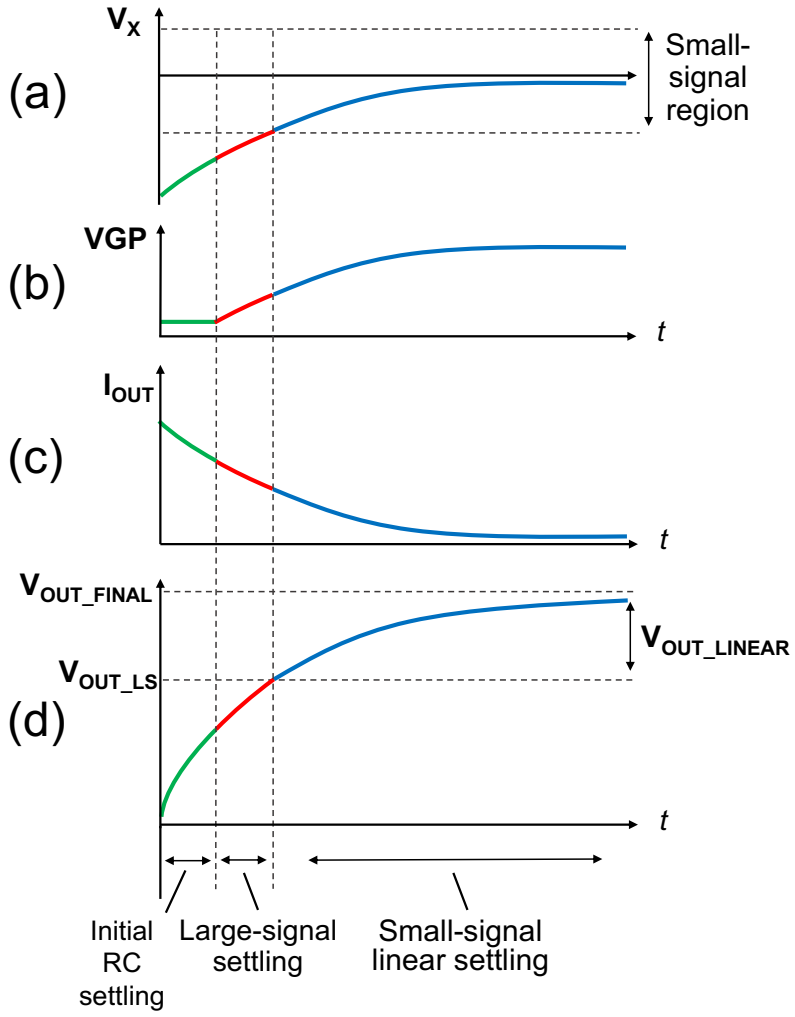

Figure 2.12: Ringamp transient response (a) Differential virtual ground node (b) Single-ended output voltage of the second-stage (b) Differential output current (c) Differential Output Voltage

and the intermediate non-linear settling boosts the speed of the ringamp. Or in other words, for the same settling time as that of an OTA, the initial RC based settling and the intermediate non-linear settling reduces the average current consumption of the ringamp.

Fig. 2.13 shows the transient response of a ringamp with overshoot. Due to the delay through the first two stages, the initial RC settling can last longer resulting in overshoot in the output voltage. Due to the overshoot that is fed back to the output of the second-stage, the large-signal Gm during the intermediate large-signal phase is now dominated by the Gm of the NMOS. This large-signal Gm from output NMOS provides an excess discharging current resulting in undershoot in the output voltage. The undershoot is fed back and the intermediate settling is now back to being dominated by the Gm of PMOS. The current due to the large-signal Gm of the PMOS decays and causes the output to enter the final small-signal settling.

In the presence of overshoot the transition of the output current between the different settling phases should be smoother to avoid instability and ringing in the transient response. The key to smooth transients is to ensure a smooth overall I-V characteristics of the ringamp. Since the overall I-V curve of a ringamp is a combination of the transfer characteristics of the first two stages and the large-signal I-V characteristics of the output-stage, two degrees of freedom exist to design a ringamp with smooth I-V characteristics. Various techniques exist in literature to ensure these smooth transitions. For example, [6] introduces a resistor based biasing for ringamp which degenerates the transfer characteristics of the second stage inverter. [18] introduces a composite ringamp to ensure overall smooth I-V characteristics of the output

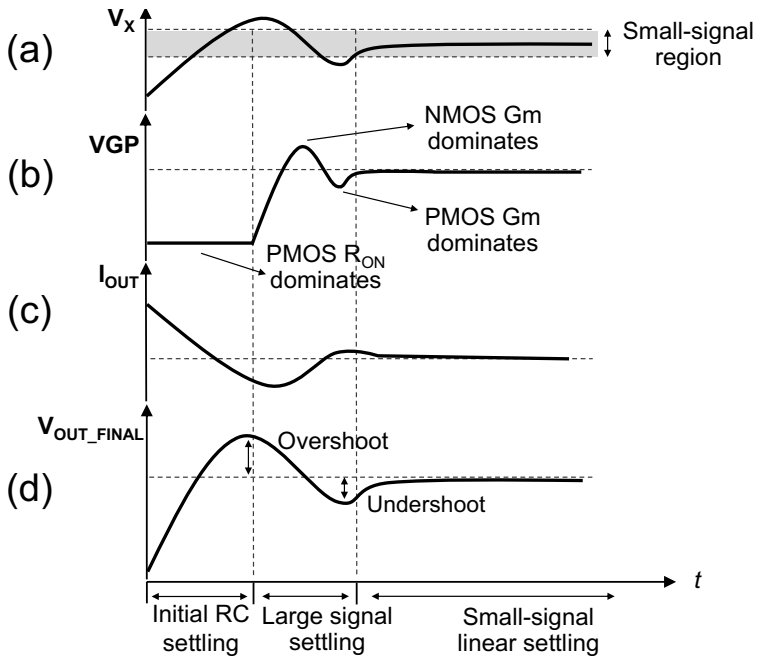

Figure 2.13: Ringamp transient response with overshoot (a) Differential virtual ground node (b) Single-ended output voltage of the second-stage (b) Differential output current (c) Differential Output Voltage

stage. [9] uses a combination of HVT and LVT transistors in the output-stage to ensure smooth I-V characteristics. [19] discusses a combination of degeneration in both first and second stages and a feedback based degeneration at the output stage.

In Chapter 4, passive compensation technique is proposed to reduce overshoot and ringing in the transient response by utilizing the ON resistance of the switches in the SC amplifier. This technique ensures smooth transition of output current in a ringamp independent of the ringamp architecture. The ON resistance of the switches provide an extra degree of freedom to degenerate the RC settling and the large-signal gm in addition to the two degrees of freedom discussed above.

In section 2.2, quantitative analysis of a single-pole step response of an OTA is reviewed. The step response analysis is then used as a baseline to quantify the ringamp step response in section 2.3. Small-signal step response of a ringamp is expected to be similar to that of a multi-stage OTA. The key difference between a traditional OTA and the ringamp will be evident from the large-signal step response.

2.2 Quantitative Analysis of The Step Response of a Single-Stage OTA: A Review

2.2.1 Small-signal Step Response in Laplace Domain

Fig. 2.14, shows the small signal model of an OTA during the charge transfer phase of a SC amplifier.

For a step input V_{in} at the bottom plate of C_S, the ideal step response reaches a

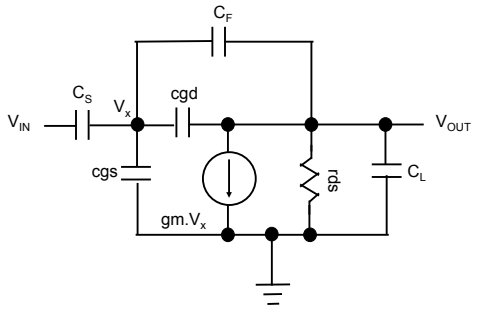

Figure 2.14: Small-signal model of an OTA during the charge transfer phase of a SC amplifier

final output voltage $V_{out,ideal}$ given by,

$$V_{out,ideal} = -G \cdot V_{in} \tag{2.3}$$

Here the ideal gain G is given by,

$$G = \frac{C_S}{C_F} \tag{2.4}$$

The transfer function of the closed-loop amplifier with a single pole is given by the following equation in Laplace domain,

$$A_{CL}(s) = \frac{v_{out}}{v_{in}} = -G \cdot \frac{L(0)}{1 + L(0)} \frac{1 - \frac{s}{z}}{1 + \frac{s}{p}} \tag{2.5}$$

where, $L(0)$ is the dc loop-gain, z is the RHP zero, p is the LHP pole.

The dc loop gain $L(0)$ is given by,

$$L(0) = \beta \cdot A(0) \tag{2.6}$$

where $A(0) = gm \cdot rds$ is the dc open-loop gain of the OTA. gm and rds are the transconductance and output resistance of the OTA.

The feedback factor β is given by,

$$\beta = \frac{C_S}{(C_S + C_{in1} + C_F)} \tag{2.7}$$

where $C_{in1} = c_{gs}$ is the input capacitance of the OTA. c_{gs} is the gate-source capacitance of the OTA.

The RHP zero is given by,

$$z = \frac{gm}{c_{gd} + C_F} \tag{2.8}$$

where c_{gd} is the gate-drain capacitance of the OTA. The RHP zero is usually neglected in a single-stage OTA as it is located at a very high frequency.

The pole p of the closed loop system is approximately equal to the frequency at which the loop-gain transfer function approaches a gain of 1 (0dB). The loop unity gain bandwidth or the gain-bandwidth product is denoted by GBW.

Thus the loop gain-bandwidth product GBW is given by,

$$GBW = \beta \cdot \frac{gm}{C_{out}} \tag{2.9}$$

Here, C_{out} is the total load capacitance,

$$C_{out} = C_L + (1 - \beta)C_F \tag{2.10}$$

Fig. 2.15 shows the bode plot for the open-loop gain, the feedback gain and the loop-gain.

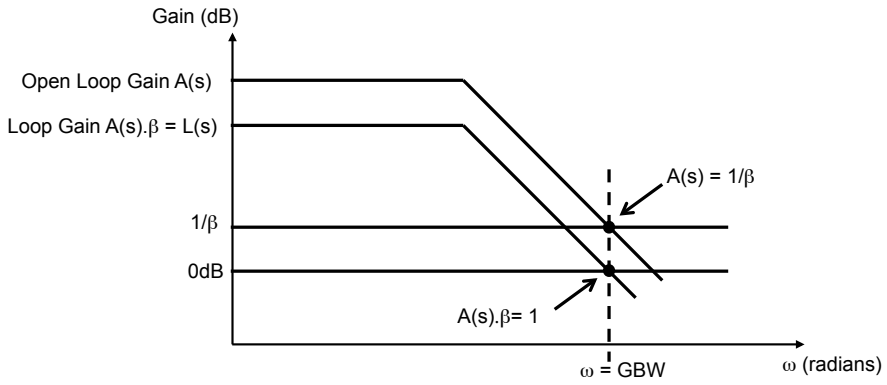

Figure 2.15: Bode plot showing loop-gain and GBW

2.2.2 Small-signal Step Response in Time Domain

Based on 2.5, the time domain representation of the step response is given by,

$$V_{out}(t) = V_{out\_FINAL}(1 - e^{-t/\tau}) \tag{2.11}$$

where: $\tau = \frac{1}{GBW}$

$$V_{out\_FINAL} = \frac{L(0)}{1 + L(0)} \cdot V_{out,ideal} = V_{out,ideal}(1 + \epsilon_{static}) \tag{2.12}$$

the static error is related to the loop gain by

$$\epsilon_{static} = \frac{L(0)}{1 + L(0)} - 1 = \frac{1}{1 + L(0)} \tag{2.13}$$

the dynamic error is related to τ by

$$\epsilon_{dynamic} = e^{-t/\tau} \tag{2.14}$$

From 2.11 we can see that faster settling time can be achieved with smaller values of τ. This translates to higher GBW or higher gm requirement for a given C_{out}. Thus high-speed small-signal settling requires higher gm making high-speed OTAs power hungry.

Now expressing dynamic error in (2.14) in log scale, we have

$$ln(\epsilon_{dynamic}) = -t/\tau \tag{2.15}$$

It is interesting to note that when dynamic error is expressed in log scale as in (2.15) , the error decays with time in a linear fashion with the slope of $\frac{1}{\tau} = GBW$ in radians.

To interpret the dynamic error in terms of percentage error, it is useful to express (2.14) in log scale with base-10.

$$log_{10}^{\epsilon_{dynamic}} = -t/\tau \cdot log_{10}^{e} \tag{2.16}$$

In this case the dynamic error decays with a slope of

$$slope = \frac{1}{\tau \cdot ln(10)} = \frac{GBW}{ln(10)} \tag{2.17}$$

The decaying dynamic error in powers of 10 is shown in Fig. 2.16. This figure can be used for fair comparison of dynamic error between a single-stage OTA and a ringamp.

To interpret the dynamic error in terms of number of bits in an ADC (powers of 2), it is useful to express (2.14) in log scale with base-2

$$log_{2}^{\epsilon_{dynamic}} = -t/\tau \cdot log_{2}^{e} \tag{2.18}$$

Note that during one time-constant of duration, $t = \tau$ the error reduces by $log_2^e = 1.44$. Since the error is now in powers of 2, we can say that in one τ the error reduces by 1.44 bits. So to achieve a dynamic settling accuracy of 14 bits, around 10 (= 14/1.44) time-constants are required. To achieve a dynamic settling accuracy of

10 bits, around 7 (= 10/1.44) time-constants are required.

Fig. 2.16 shows the small-signal settling response of the OTA. Fig. 2.17 shows the static and dynamic error during the transient response.

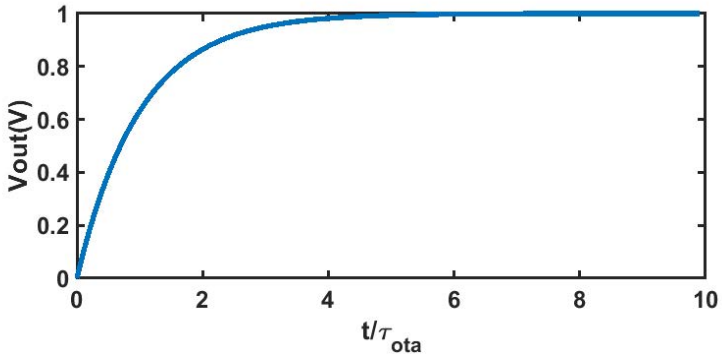

Figure 2.16: Settling response for a single-stage OTA (y-axis normalized to final value)

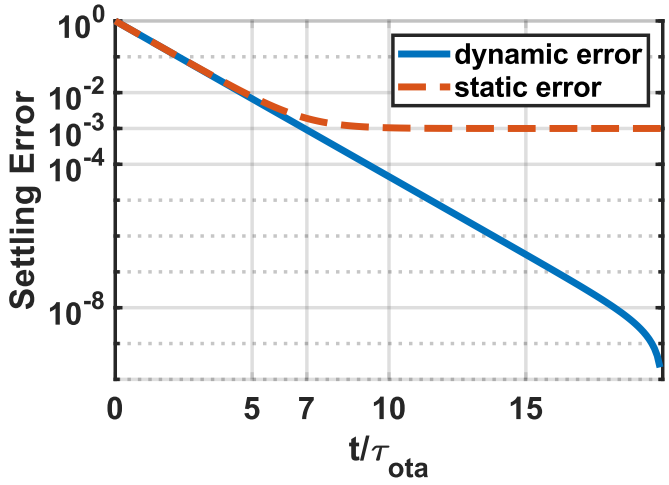

Figure 2.17: Dynamic settling error and overall settling error in log scale

2.2.3 Large-signal Step Response

With large-signal input step, part of the settling time is limited by the slew rate of the OTA. Slew rate (SR) of a single stage OTA with tail current I_{tail} is given by:

$$SR = \frac{dV_{out}}{dt} = \frac{I_{tail}}{C_{out}} \tag{2.19}$$

The slewing for large-signal input step is understood by considering the large-signal dc I-V characteristics of a single-stage differential OTA as shown in Fig. 2.4. For input differential voltage magnitudes larger than I_{tail}/gm, only one of the diff-pair in the OTA conducts and pulls all of the I_{tail} current through it. Due to this large-signal phenomenon, faster settling time requires higher bias current to minimize the slewing time. This can make OTAs power hungry for high-speed operation.

2.2.4 Transition between Slewing and Small-signal Response

To ensure a smooth transition from slewing to small-signal response as shown in Fig 2.5, the slope of the small-signal settling, at the transition time point, should match the slew rate [17]. This condition is given by,

$$\left[\frac{dV_{out\_Linear}(t)}{dt}\right]_{t=0} = \left[\frac{dV_{out}(t)}{dt}\right]_{t=tslew} \tag{2.20}$$

Here $t = 0$ for small-signal settling since $t = tslew$ is the beginning of small-signal response.

$$\left[\frac{d}{dt}(V_{out\_Linear}(1-e^{\frac{t}{\tau}}))\right]_{t=0} = SR \tag{2.21}$$

$$\frac{V_{out\_Linear}}{\tau} = \frac{I_{tail}}{C_{out}} \tag{2.22}$$

Thus, from 2.22, we can see that, when small-signal time-constant (τ) is reduced for faster small-signal settling, the slew rate needs to scale higher for smoother transition from slewing to small-signal settling.

2.3 Step Response of a ringamp

2.3.1 Small-signal Step Response Analysis in Laplace Domain

Fig. 2.18, shows the small signal model of a ringamp during the charge transfer phase of a SC amplifier.

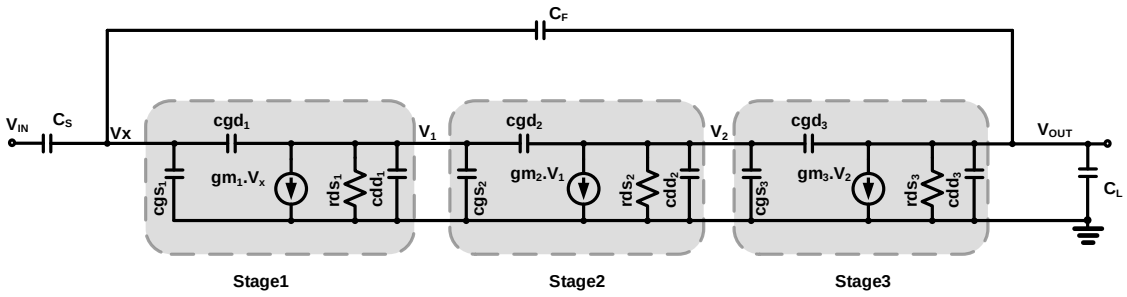

Figure 2.18: RC model for initial large-signal step response. (a) Positive output step (b) Negative output step

The small-signal transfer function of the closed-loop amplifier is given by the

following equation in Laplace domain. The non-dominant poles are ignored here for simplicity. A detailed small-signal analysis is presented in sec:ch2sec5.

$$A_{CL}(s) = \frac{v_{out}}{v_{in}} = -G \cdot \frac{L(0)}{1+L(0)} \frac{1-\frac{s}{z}}{1+\frac{s}{p}} \tag{2.23}$$

where, $L(0)$ is the dc loop-gain, z is the RHP zero, p is the LHP pole.

The dc loop gain $L(0)$ is given by,

$$L(0) = \beta \cdot A(0) \tag{2.24}$$

where $A(0) = A_1 A_2 A_3$ is the dc open-loop gain of the ringamp. A_1, A_2 and A_3 are the small signal gains of the first,second and third stages respectively.

The feedback factor β is given by,

$$\beta = \frac{C_S}{(C_S + C_{in1} + C_F)} \tag{2.25}$$

where $C_{in1} = c_{gs} + c_{gd} \cdot A_1$ is the input capacitance of the OTA. c_{gs} and c_{gd} are the gate-source and gate-drain capacitances of the first-stage of ringamp respectively. A_1 is the small-signal gain of the first-stage of the ringamp.

The pole p of the closed loop system is approximately equal to the frequency at which the loop-gain transfer function approaches a gain of 1 (0dB). The loop unity gain bandwidth or the gain-bandwidth product is denoted by GBW.

Thus the loop gain-bandwidth product GBW is given by,

$$GBW = \beta \cdot \frac{A_1 A_2 gm_3}{C_{out}} \tag{2.26}$$

where gm_3 is the transconductance of the output-stage. C_{out} is the total load capacitance,

$$C_{out} = C_L + (1 - \beta)C_F \tag{2.27}$$

The RHP zero is given by,

$$z = \frac{gm_3}{c_{gd3}} \tag{2.28}$$

where gm_3 and c_{gd3} are the transconductance and the gate-drain capacitance of the output-stage of the ringamp respectively. The RHP zero in a ringamp is usually located close to the GBW of the loop due to the low gm_3 (from dominant pole biasing) and high *cgd* (from large lengths to achieve high gain and from large widths to achieve faster settling). Hence RHP zero should be considered for small-signal phase margin calculations.

2.3.2 Small-signal Step Response in Time Domain

Based on 2.23, the time domain representation of the step response is given by,

$$V_{out}(t) = V_{out\_FINAL}(1 - e^{-t/\tau}) \tag{2.29}$$

where: $\tau = \frac{1}{GBW}$

$$V_{out\_FINAL} = \frac{L(0)}{1+L(0)} \cdot V_{out,ideal} = V_{out,ideal}(1+\epsilon_{static}) \tag{2.30}$$

the static error is related to the loop gain by

$$\epsilon_{static} = \frac{L(0)}{1+L(0)} - 1 = \frac{1}{1+L(0)} \tag{2.31}$$

the dynamic error is related to τ by

$$\epsilon_{dynamic} = e^{-t/\tau} \tag{2.32}$$

From 2.29 we can see that faster small-signal settling time can be achieved with smaller values of τ. This translates to higher GBW requirement for a given C_{out}. However, unlike OTA, here the gm_3 is boosted by A_1A_2 . This relaxes the static current requirement of the ringamp for small-signal settling.

In the following discussions it will be shown that when large-signal effects are considered, the GBW of ringamp can be further relaxed for the same settling time requirements as that of an OTA.

2.3.3 Large-signal Step Response

Fig. 2.9 shows the schematic of a ringamp (single-ended schematic shown for simplicity). Fig. 2.10 shows the overall I-V characteristics of the ringamp with optimum bias voltages VGP and VGN. The optimum bias voltages (deadzone voltage) define the

slope of the I-V curve (gm) for small-signal input. For large-signal input, the slope of the I-V curve is non-linear resulting in a non-linear large-signal transconductance denoted by Gm. The overall I-V curve of the ringamp is a combination of the transfer characteristics of the first two stages (Fig. 2.11) and the I-V characteristics of the third stage (similar to the IBA I-V curve as shown in Fig. 2.7).

As discussed in section 2.1 Fig. 2.12, the large-signal step response of the ringamp can be divided into a three-phase operation. The initial RC settling phase, the intermediate large-signal settling phase and the final small-signal settling phase.

2.3.3.1 Initial RC Settling Phase

The initial RC settling is the key feature that distinguishes a ringamp from a single-stage IBA or OTA. For a large-signal step input, the output of the second-stage reaches close to rail-to-rail voltage as shown in Fig. 2.12. This momentarily results in a large overdrive for one of the output-stage transistors, while the output voltage ($Vout$) charges towards the final value. Since the gate-source voltage during this phase is constant while the drain-source voltage is changing, the output current during this initial settling is a function of the on resistance, R_{ON} of the output stage PMOS transistor. The R_{ON} is also a function of the fixed VGP during this phase. This initial RC settling phase charges the load capacitance with an impulse-like current. Thus the ringamp in this phase can be modeled with a simple RC charging/discharging circuit as shown in Fig. 2.19. The resulting time-constant τ_L is given by,

$$\tau_L = R_{ON} C_{out} \tag{2.33}$$

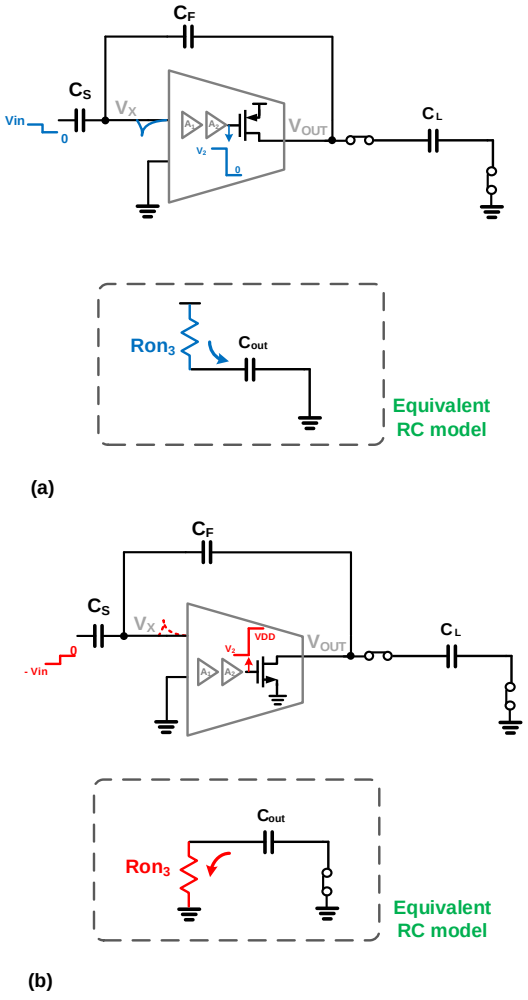

Figure 2.19: RC model for initial large-signal step response. (a) Positive output step (b) Negative output step

Accordingly, the initial phase of the step response can be defined as below:

$$V_{out,RC}(t) = V_{out\_FINAL}(1 - e^{-t/\tau_L}) \tag{2.34}$$

where: V_{out_FINAL} is defined by (2.30)

The charging/discharging current through the output capacitor is given by,

$$I_{out,RC}(t) = C_{out}\frac{dV_{out,RC}(t)}{dt} = \frac{V_{out\_FINAL}}{R_{ON}}e^{-t/\tau_L} \tag{2.35}$$

Note that the R_{ON} is a function of the fixed VGP and VGN during the initial phase. For step inputs that are larger than the small-signal step but small enough to not rail the second-stage output, τ_L can be redefined based on Ron-V characteristics of the third-stage for more accurate analysis.

Followed by the quick initial RC settling phase, when the feedback from the output reaches back to VGP, the gate-source voltage starts to change, while the drain-source voltage has almost settled closer to the final value as shown in Fig. 2.12. The output current during this phase is a function of the large-signal Gm of the ringamp, which is a function of the large-signal gain of the combined first two stages and the non-linear large-signal Gm of the output stage. Since the intermediate large-signal phase is a dynamic operation and is hard to quantify with closed form expressions, we first quantify the final small-signal response and then discuss the intermediate large-signal phase as a transition condition between the initial RC settling and the final small-signal settling.

2.3.3.2 Final Small-signal Settling Phase

Followed by the initial RC settling and intermediate large-signal settling, the remainder of the output step response is completed by the small-signal operation as shown in Fig. 2.12. This phase of the response is defined from time $t = t_{LS}$ and with a small-signal time-constant τ_S,

$$V_{out\_Linear}(t) = V_{out,LS} + (V_{out\_FINAL} - V_{out,LS})(1 - e^{-(t-t_{LS})/\tau_S}) \tag{2.36}$$

where, $V_{out,LS}$ is the output response that is already completed by the large-signal section within the time $t = t_{LS}$.

The small-signal time-constant tau_S is given by,

$$\tau_S = \frac{1}{GBW} = (\beta \cdot A_1 \cdot A_2 \frac{gm_3}{C_{out}})^{-1} \tag{2.37}$$

The overall settling response of a ringamp based on (2.34) and (2.36) is shown in Fig. 2.20 along with the settling response of a single-stage OTA described by (2.11). The initial fast settling response in the ringamp gives a head-start towards reducing the dynamic error in the output step response. This relaxes the GBW or τ_S requirement for the small-signal operation of a ringamp. Since GBW is associated with transconductance, relaxed transconductance implies reduced power consumption to achieve the same settling time.

In other words, for the same small-signal GBW or τ_S as a single-stage OTA (same

power), faster settling time can be achieved in ringamps due to the initial large-signal response.

2.3.3.3 Intermediate Large-signal Settling Phase

Since the intermediate dynamic operation of a ringamp is hard to quantify with closed loop expressions, we discuss it as a transition condition from initial RC settling to final small-signal settling. Modeling the dynamic operation phase with a transition condition provides a more intuitive insight into a ringamp operation. This is due to the fact that the transition condition between the different phases can be linked to the slope of the output voltage, which fundamentally corresponds to the current flowing through the load capacitor ($I = Cdv/dt$). In the initial RC settling phase, the current flowing through the load capacitor is a function of R_{ON} and in the final small-signal settling phase, the current flowing through the load capacitor is a function of small-signal gm of the ringamp. In the intermediate large-signal settling phase, the current flowing through the load capacitor is a function of the large-signal Gm of the ringamp.

The smooth transition from large-signal settling phase to small-signal settling phase can be ensured by design by considering the large-signal dc I-V characteristics of a ringamp. The smoothness of I-V characteristics can be quantified by the slope of the I-V characteristics which corresponds to the shape of the large-signal Gm of the ringamp. Since overall I-V curve of a ringamp depends on the V-V transfer characteristics of the first two stages and the I-V characteristics of the output-stage,

there are two degrees of freedom to control the smoothness of I-V characteristics of a ringamp.

The smooth transition from RC settling phase to large-signal phase depends on the time-constant of the RC settling. Hence sizing of the output stage can be used to increase or decrease the time-constant required for the output current to hand-off between the two phases.

The above methods ensure smooth transients in ringamps and are easily related to the dc characteristics of ringamps. However, the delays through the loop can distort the transient V-V characteristics of the first two stages. This in turn affects the smooth dc I-V characteristics which results in overshoot and ringing. Chapter 4 discusses a passive-compensation technique which uses the existing switches in the SC amplifier feedback to control the RC time constant of the initial settling and at the same time provides a way to degenerate the large-signal Gm. Thus an extra degree of freedom is added for smooth transition between the transient settling phases to control large-signal ringing.

Let us consider a few quantitative considerations to draw more insights into the transition between the phases. Assuming that the intermediate large-signal settling is short, for a smooth transition between large-signal and small-signal response, the slope of the small-signal response at the end of RC settling should match closely with the slope of the small-signal response at the time of transition $t = t_{LS}$. Thus, taking the derivative of (2.34) and (2.36) and equating the two we get,

$$\left[\frac{dV_{out,LS}(t)}{dt}\right]_{t=t_{LS}} = \left[\frac{dV_{out\_Linear}(t)}{dt}\right]_{t=0} \tag{2.38}$$

Here $t = 0$ for small-signal linear settling as $t = t_{LS}$ is the beginning of small-signal response.

$$\frac{V_{out\_FINAL}}{\tau_L} \cdot e^{-t_{LS}/\tau_L} = \frac{(V_{out\_FINAL} - V_{out,LS})}{\tau_S} \tag{2.39}$$

This equation represents a direct trade-off between RC time-constant and smooth transition in the response. For power efficient settling response we would desire that most part of the settling is completed by the large-signal response which then relaxes the requirement of the small-signal time-constant or GBW. For this desirable condition, the term on the right hand side of (2.39) represents a very small slope as $V_{o,LS}$ approaches close to $V_{o,FINAL}$. Which means that the slope of the large-signal step response is required to be lower for smooth transition which implies larger τ_L. Another interpretation of (2.39) is the condition for large-signal response during zero-crossings at the virtual ground node of the ringamp. Once again, for zero crossing condition, the term on the right hand side of (2.39) represents a very small slope. Thus to avoid abrupt zero crossings, the slope of the large-signal response at $t = t_{LS}$ needs to be lower which implies larger τ_L. In other words, for a given small-signal time-constant,output step voltage and $t_L S$ requirement, this equation (2.39) provides a way to find the minimum τ_L to avoid abrupt zero crossings that cause overshoot and ringing.

These equations also lead us to the analogy of a PID controller to qualitatively and intuitively interpret the step response of a ringamp.

In control systems, it is very common to use a combination of proportional, inte-

gral and derivative controls to successfully train and ensure stable negative feedback operation [20]. Analog systems such as PLLs also use PID control. A proportional control represents a direct feedback control without any memory. This represents only the "present" feedback response to any disturbance in the system. A proportional control is a really fast control. An integral control represents a feedback control with memory. This represents a collection of the "past" feedback responses and it ensures that the error in the system is minimized. An integral control is a very slow control but is necessary to ensure accuracy. Finally, a derivative control represents a feedback control that provides feedback by anticipating the response. This represents the feedback necessary for "future" response. Since derivative control is predictive feedback, it can result in large errors if the gain of the derivative control is large.

Based on this understanding we can draw similarities between the response of PID controllers and ringamps:

1) the RC settling operation dictated by τ_L can be considered as proportional control. 2) the small-signal operation dictated by τ_S can be considered as integral control. 3) the transition from large-signal to small-signal operation can be ensured by smooth transition of output current (derivative of output voltage). This condition can be considered as derivative control.

This analogy is utilized in Chapter 4 to control large-signal ringing when ringamps are used in high speed and high accuracy systems.

The three parts of the settling response discussed here are similar to the slewing, stabilization and settling parts of the ringamp response as described in [1]. However, the model shown in Fig. 2.19 differs from the traditional approach. The traditional

model [1] assumes that the large current remains constant similar to the slewing operation or similar to a zero crossing detector based operation. In reality, the output current through the capacitor peaks and decays exponentially before the ringamp transitions to the low quiescent current small-signal operation. The proposed RC based initial settling model captures this exponential decay of the output load current and is also useful in understanding stability concerns that could arise due to abrupt transitions between the large-signal and the small-signal response.

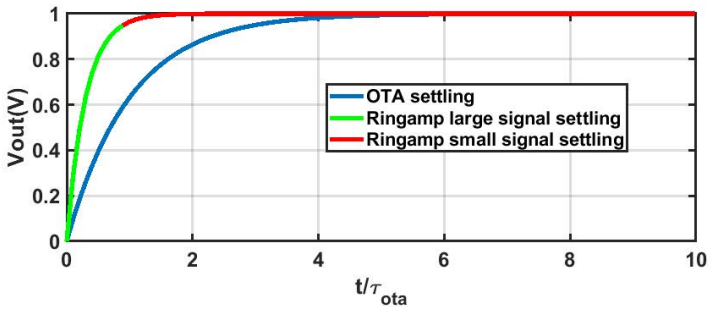

Figure 2.20: Settling response for a ringamp compared to single-stage OTA (y-axis normalized to final value)

2.4 Small-Signal Stability and Noise

2.4.1 Differential Loop Analysis

Fig. 2.18 shows the small signal model of a ring-amplifier. The small signal analysis is straight-forward and similar to a multi-stage amplifier.

The D.C. gain, poles, and zeros of a stage i is given as the following.

$$DC\,gain,\ A_i(0) = G_{m,i}R_{o,i} \tag{2.40}$$

$$G_{m,i} = g_{mp,i} + g_{mn,i} \tag{2.41}$$

$$R_{o,i} = r_{dsp,i}||r_{dsn,i} \tag{2.42}$$

$$Pole,\ \omega_{pi} = \frac{1}{R_{o,i}C_{p,i}} \tag{2.43}$$

The load capacitor for stage 1 and 2 are defined as:

$$C_{p,i} = C_{gs,i+1} + C_{gd,i+1} \cdot A_{i+1}(s), i = 1, 2 \tag{2.44}$$

$C_{gs,i+1}$ is the total gate-to-source capacitance of the stage $i+1$. $C_{gd,i+1}$ is the total gate-to-drain capacitance of the stage $i+1$. A_{i+1} is the gain of the stage $i+1$.

The total load capacitance at the output of the ring amplifier is defined by:

$$C_{out} = C_L + (1-\beta)C_F \tag{2.45}$$

The right half plane zero in each stage is given as:

$$RHP\,Zero,\ \omega_{zi} = \frac{G_{m,i}}{C_{gd,i}} \tag{2.46}$$

The small signal transfer function of the i^{th} stage inverter is given by:

$$A_i(s) = A_i(0)\,\frac{\left(1-\frac{s}{\omega_{zi}}\right)}{\left(1+\frac{s}{\omega_{pi}}\right)} \tag{2.47}$$

The overall small signal transfer function of the ring amplifier in steady state is given by:

$$A(s) = A_1(s)\cdot A_2(s)\cdot A_3(s) = \prod_{i=1}^{3}\left[A_i(0)\,\frac{\left(1-\frac{s}{\omega_{zi}}\right)}{\left(1+\frac{s}{\omega_{pi}}\right)}\right] \tag{2.48}$$

The feed back factor is

$$\beta(s) = \frac{C_S}{(C_S + C_{in1} + C_F)} \tag{2.49}$$

where C_{in1} is the input capacitance of the ring amplifier given by

$$C_{in1} = C_{gs,1} + C_{gd,1}\times A_1(s) \tag{2.50}$$

The loop transfer function ignoring high frequency poles and zeros is given as:

$$L(s) = \beta(s)A_1\,A_2\,A_3\,\frac{\left(1-\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \tag{2.51}$$

The loop unity gain bandwidth is given by:

$$GBW = \left(\frac{\beta(0)A_1A_2G_{m,3}}{C_{out}}\right) \tag{2.52}$$

For phase margin, the most dominant contributors for phase degradation are from

the non-dominant poles of the first two stages and the RHP zero from the output-stage. Compared to a single-stage OTA, the RHP zero in a ringamp is closer to GBW due to the low transconductance of the output-stage and the high gate-drain capacitance of the output-stage due to the large sizing of output stage (large length for gain, large widths for fast response).

2.4.2 Noise

In a SC circuit, one should consider the total integrated noise to perform noise analysis. An intuitive and elegant noise analysis for a single-stage OTA can be found in [21]. Using the results of the analysis from [21], the integrated output noise of a single-stage OTA in a SC amplifier setup shown in Fig. 2.1 is given by:

$$v_{o,OTA}^2 = \frac{\alpha kT}{\beta C_{out}} \tag{2.53}$$

where α is the excess noise term which corresponds to additional noise added based on OTA implementation. For example, the noise added by the active-loads.

Using similar noise analysis for a ringamp, the discussion in [9] shows that the integrated output noise is given by:

$$v_{o,ringamp}^2 = \frac{\alpha kT}{\beta C_{out}} \cdot \frac{A_1 A_2 gm_3}{gm_1} \tag{2.54}$$

Compared to an OTA where the noise floor and the noise bandwidth are set by the same stage, the noise floor in ringamp is set by the transconductance of the first-stage

of the ringamp and the noise bandwidth is set by the third-stage transconductance and the gains of the first two-stages. Thus ring-amplifier provides additional degree of freedom for noise optimization. The main take-away from this analysis is that the below design condition has to be satisfied to keep the noise level equal to or lower than that of a single-stage OTA.

$$gm_1 \geq A_1 A_2 gm_3 \tag{2.55}$$

2.5 Design Example

In this section, a current-starved-inverter based ring-amplifier is designed in 65nm CMOS to demonstrate the fast settling response of the ring-amplifier. It will be shown that the ring-amplifier designed with a τ_S of $1ns$ (GBW of 150MHz) can settle to an accuracy of 10bit level or 0.1% error at the output voltage in less than $4ns$. Based on (2.18), a traditional OTA would have taken 7ns ($7\tau_S = 10bit/1.44$) to achieve similar settling accuracy. Fig. 2.21 shows the schematic of a current-starved-inverter based ring-amplifier that is used for the design example. The SC amplifier is designed for a gain of 4. The capacitances C_L, C_F and C_S are chosen to be $600fF, 500fF$ and $2pF$ respectively.

The design flow for this example is as follows:

1) The lengths of stage1 and stage2 are chosen to be minimum length to ensure the non-dominant poles do not worsen phase margin. Stage3 length is chosen to be 10x min length to meet the loop gain of $> 60dB$ to achieve 10bit level (0.1%) output

settling accuracy.

2) Given τ_S is 1ns, this corresponds to 150MHz of GBW in Hz (Note: $GBW = 1/\tau_S$ in radians). Using (2.26) and (2.25) we can find gm_3 to be around $200uS$ (Here, $A_1 \cdot A_2$ is taken as 40-60 based on the intrinsic gain for min length transistors in 65nm CMOS).

Thus, $gm_3 = 200uS$. With a gm/Id of 20, the required quiescent current for stage3 is $10uA$ ($20uA$ total for differential structure). This bias current decides the gate voltages of stage3 transistors which then decides the deadzone control voltages.

Note: The choice of gm/Id of 20 biases output stage with a low overdrive and in sub-threshold region. This choice is made so that gm3 is only a function of the bias current and independent of the overdrive voltage or width of the transistor. This choice helps keep the GBW fixed for a given bias current while the sizing of stage3 can be chosen to vary the output drive strength. In terms of threshold voltage variations and variations across temperature, this may not be the best biasing choice. These tradeoffs are dicussed in Chapter 3 as design considerations for PVT tolerant biasing.

3) τ_L is found to be 500ps by sizing stage3 transistor to have an Ron of 500 ohms with a gate voltage drive of 1.1V. For this example, τ_L is chosen deliberately large to ensure very slow and smooth transition from large-signal to small-signal operation. However, since τ_L is still smaller than τ_S the design can still demonstrate the speed improvement over a single-stage OTA.

4) gm_1 for the first stage is designed using the condition in (2.55). This ensures that ring-amplifier doesn't produce any excess noise.

Thus $gm_1 > 12mS$. With a gm/Id of 20 again, the bias current for stage1 diff-pair

is 1.2mA. The choice of low overdrive here is due to the headroom requirement and for good input common mode range with a 1.2V supply.

5) The initial sizing of stage2 is done such that the trip point of the inverters without current starving are close to $VDD/2$. This maximizes the output common mode range and swing of stage2. The current starving transistors are sized to ensure wide range of deadzone-control to control the gate voltage of stage3. In addition, stage1 output common mode is designed to match the input common mode voltage of stage2 (in this case the trip point) so that there is no systematic offset. A local CMFB around stage1 also ensures this condition is met by using the CMFB reference from a replica that generates the second stage trip-point.

6) Finally stage2 is scaled to modify its drive strength and also to ensure good phase margin.

The transient response and the settling errors for an output differential step of 800mV is shown in Fig. 2.22. The dynamic error plot clearly demonstrates the initial fast decay of error followed by the slow decay set by the small-signal parameters. The drive strength of stage3 can be improved for this example for even faster large-signal settling. However care must be taken as described by (2.39) to avoid significant large-signal ringing and overshoot.

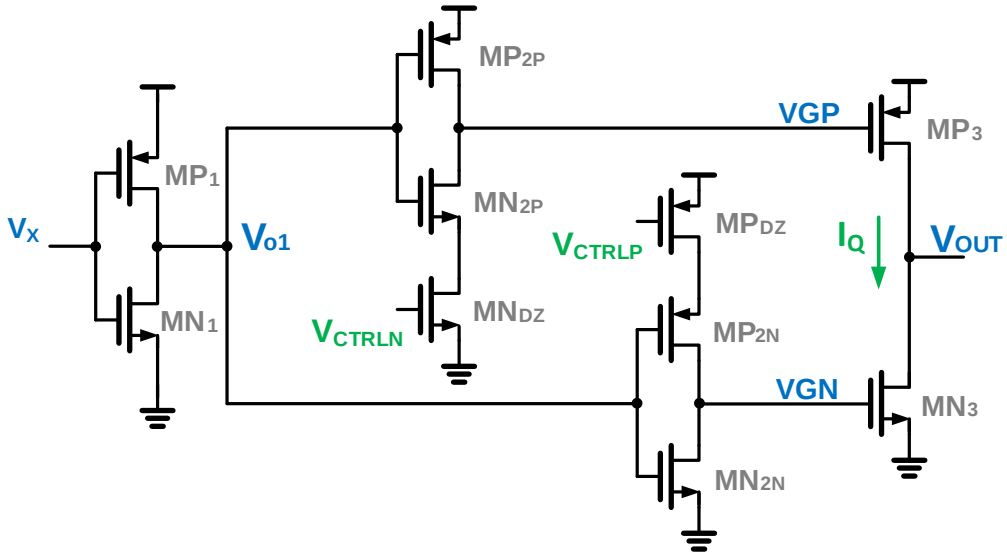

Figure 2.21: Current-starved-inverter based ring-amplifier used for design example. (Single-ended schematic shown for simplicity. First-stage biased with tail current sources for differential implementation)

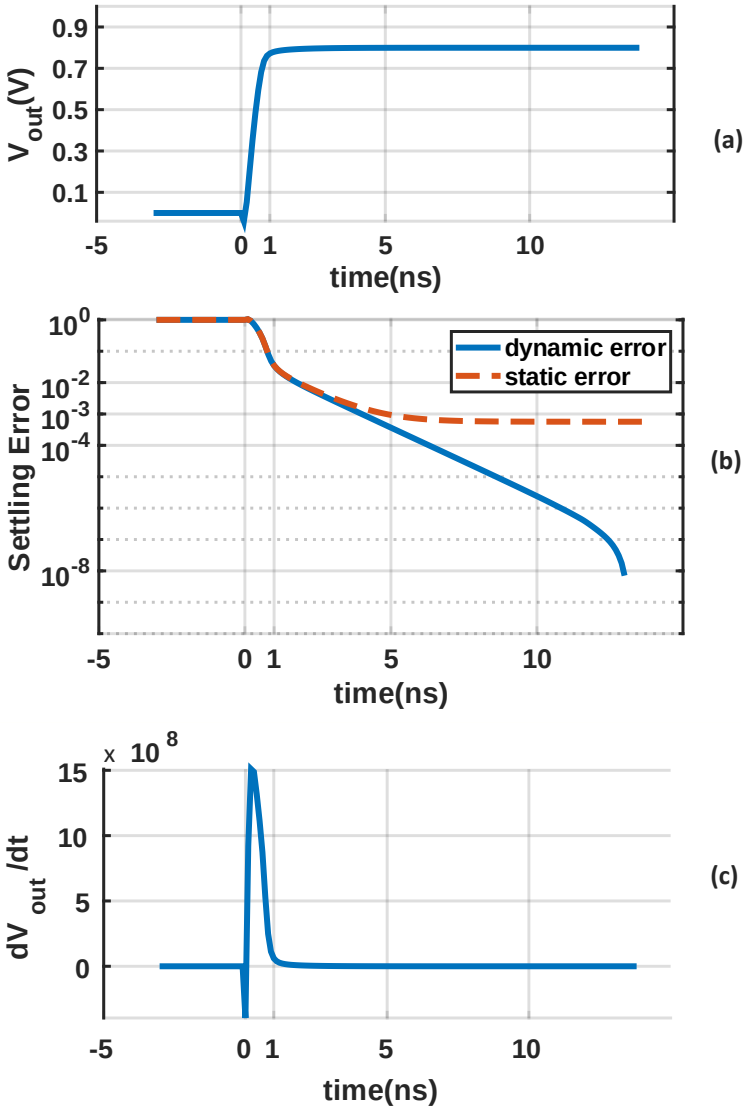

Figure 2.22: Settling response of the ring-amplifier. (a) Differential output voltage step of 800mV (b) Dynamic and static errors illustrating the fast large-signal slope and slow small-signal slope sections (c) Derivative of output voltage representing the exponential decay of current through the load capacitor

Chapter 3: PVT-tolerant Biasing Technique

3.1 Introduction

In this chapter, process invariant biasing is proposed for robust operation of ring amplifiers.

The traditional ring amplifier [1] requires external reference voltage, defined as the deadzone voltage, for optimum performance. Other structures of ring amplifiers have been proposed in [6, 7, 9]. The structure in [6] requires an on-chip resistor to create the deadzone voltage. The structure in [7] uses current-starved inverters to create the deadzone voltage. The deadzone voltage is used to optimally set the quiescent current in the output stage of a ring amplifier and it is a function of the threshold voltage of the transistors. This makes ring amplifiers susceptible to process variations.

In this chapter, a deadzone regulation circuit is proposed that utilizes a constant current source and a negative feedback loop to regulate the quiescent current of the output stage across process corners. Transistor level simulations are used to validate the operation of the proposed deadzone regulation technique across FF, TT and SS corners in a 65nm CMOS process. The design example uses a current-starved-inverter based ring amplifier in a switched capacitor amplifier to achieve a closed loop gain of 4 with a settling accuracy of $\leq 0.05\%$ and operated at a sampling rate of 125MHz. The

technique can also be applied to a traditional ring amplifier [1] and other structures of ring amplifiers [6, 7, 9, 8, 22, 23, 24, 25, 26, 27] in general.

The organization of the chapter is as follows. Section 3.2 provides a brief overview of the existing deadzone biasing structures. Section 3.3 describes the effect of process variation on the small signal ac response and transient response of a ring amplifier, with a current-starved-inverter based ring amplifier as a design example. Section 3.4 describes the proposed deadzone regulation circuit. Simulation results are discussed showing the effectiveness of the technique across TT, FF and SS process corners. Section 3.5 discusses additional considerations and tradeoffs among individual stages.

3.2 Existing Deadzone Biasing Structures

This section describes: A) The basic concept of the dynamic operation of a ring amplifier, B) The existing deadzone biasing structures for a ring amplifier.

3.2.1 Dynamic Operation of a Ring Amplifier

3.2.2 Deadzone Biasing in Existing Ring Amplifier Stuctures

Fig. 3.1 shows the structure of a traditional ringamp. The deadzone voltage is at the input of the second stage inverter (VDZ_P and VDZ_N in Fig. 3.1) [1]. With the appropriate deadzone voltage, the output stage inverter is biased with a very low quiescent current, I_Q. This results in a dominant pole at the output, that dynamically stabilizes the negative feedback loop.

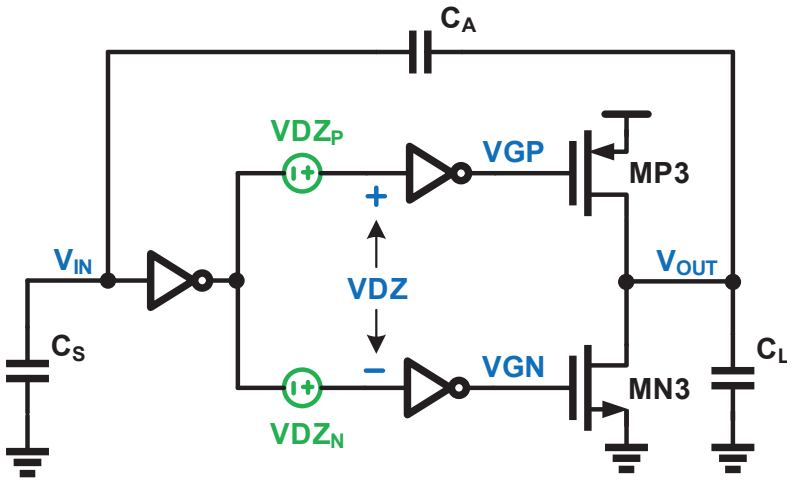

Figure 3.1: Traditional ringamp in a switched capacitor negative feedback

Fig. 3.2 [13] and Fig. 3.3 [7] show alternate ringamp structures that differ in the way deadzone biasing is implemented. The figures show single ended structure for simplicity. Differential structure is preferred for better supply and common mode rejection. The structure in Fig. 3.2 implements deadzone biasing using a resistor at the output of the second stage. The structure in Fig. 3.3 implements deadzone biasing using current-starved inverters in the second stage.

Irrespective of the structure of a ringamp, the deadzone voltage or the deadzone resistor is chosen such that, the steady state gate voltages (VGP and VGN) of the output stage inverter, bias the output stage to have a very small quiescent current, I_Q. Since the dominant pole of the ringamp is due to the output stage inverter, this quiescent current controls the loop gain bandwidth during the small signal operation of a ringamp. However, the quiescent current is a function of the threshold voltages of transistors in the third stage inverter.

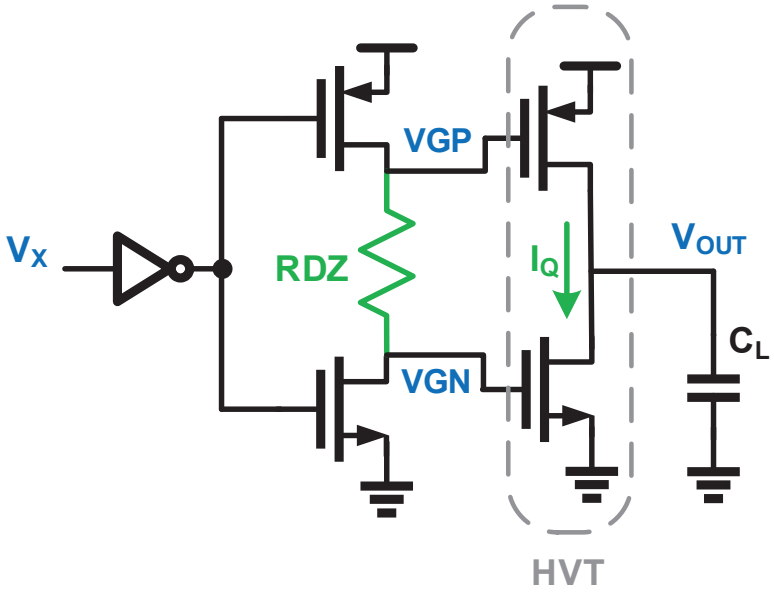

Figure 3.2: Ringamp using a resistor for deadzone biasing

Thus for a given value of deadzone voltage or deadzone resistor, the quiescent current, I_Q in the output stage can vary across process corners due to variations in threshold voltage. This significantly affects the loop gain bandwidth of the ringamp. The effect is discussed with a design example in the next section.

3.3 Effect of Process Variation on a ringamp Response

To illustrate the effect of process variation on the performance of a ring amplifier, consider the current starved inverter based ring amplifier in Fig. 3.3. A fully differential structure is designed in a 65nm CMOS process with a 1.2V supply voltage. A single ended schematic is shown in the figure for simplicity.

For the design example, the ring amplifier is used in the switched capacitor am-

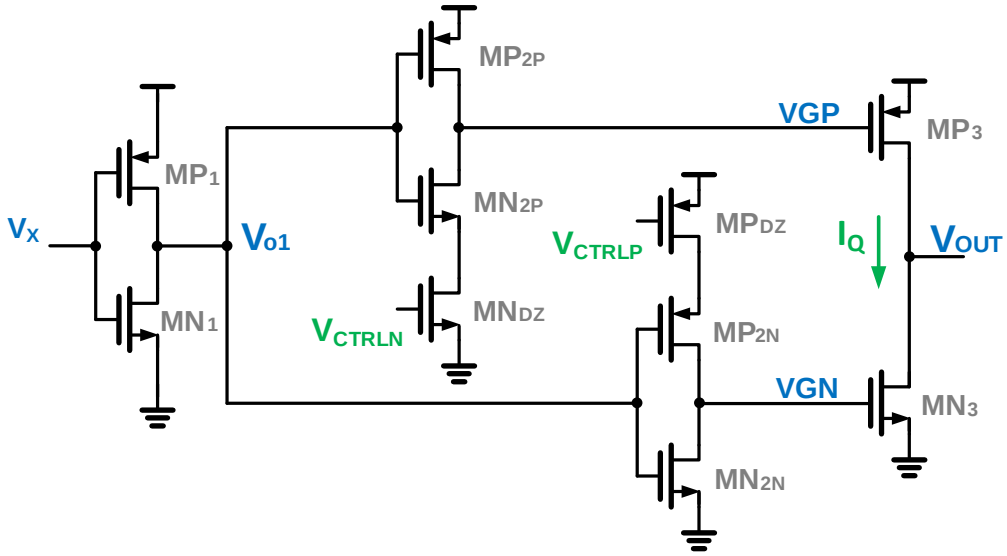

Figure 3.3: Ringamp using current starved inverters for deadzone biasing.

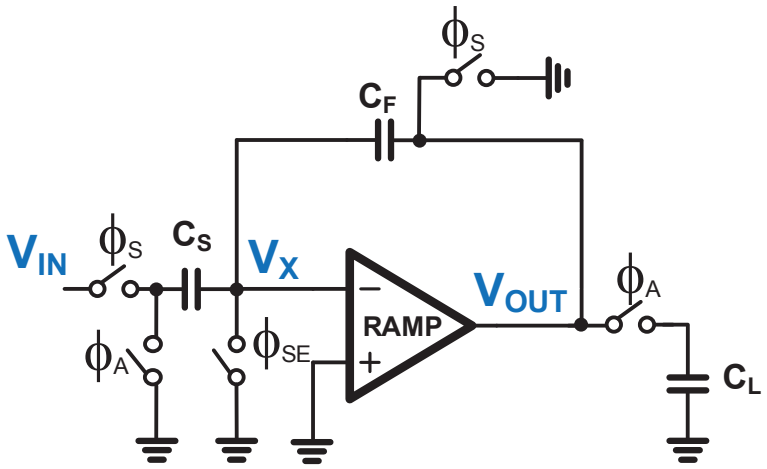

Figure 3.4: Switched capacitor amplifier setup

plifier shown in Fig. 3.4, which is setup for a closed loop gain of 4 and operated at a sampling rate (F_S) of 125MHz with $C_S = 2pF$, $C_F = 500fF$ and $C_L = 700fF$. The open loop gain of the ring amplifier is designed such that the settling accuracy of the output voltage is $\leq$0.05%.

Unlike OTAs, the choice of feedback factor can result in varying degrees of small signal and large-signal effects on the settling of ring amplifiers [28]. The discussion in this paper ignores the large-signal effects [29]. The control voltages V_{CTRLP} and V_{CTRLN} set the gate bias voltages VGP and VGN of the third stage inverter during the steady state. This in turn sets the quiescent current, I_Q and the transconductance, gm_3 of the third stage during the steady state.

For this example, the required GBW is $\geq$ 375MHz ($\approx 3F_S$) and a phase margin $\geq$ 60 degrees. The deadzone bias voltages are V_{CTRLP}= 795mV and V_{CTRLN} = 390mV to set a quiescent current of 3.5uA in the third stage inverter, at TT process corner. Table. 3.1 shows the drastic variation in the small signal parameters of the ring amplifier such as GBW and phase margin (PM) across TT, FF and SS corners, when the deadzone bias corresponds to that of the TT case.

Fig. 3.5 shows the transient response of the ring amplifier with a fixed deadzone bias, for a differential peak output swing of 800mV across FF, TT and SS process corners. The deadzone bias is fixed at the values corresponding to TT case. It can be seen that the settling accuracy requirements are not met for the SS case, due to the reduced GBW and slower response. Based on these observations, a robust deadzone biasing is required, that aims to maintain a constant quiescent current in the output stage across process variations.

Table 3.1: Variation in small signal parameters of the ring amplifier with a fixed deadzone bias.

Process Corners	**SS**	**TT**	**FF**
GBW (MHz)	9	415	1500
PM (degrees)	85	68	53

3.4 Proposed Deadzone Regulation Circuit

3.4.1 Circuit Description

Fig. 3.6 shows the proposed regulation circuit. As seen from the figure, the diode tied transistors and the constant current source set the gate bias voltages VGP_{REF} and VGN_{REF} of the third stage inverter for a given bias current I_{BIAS}. The voltages VGP_{REF} and VGN_{REF} track the threshold voltage variation across process corners for a fixed bias current.

A negative feedback loop is formed using the replica of the second stage inverters and the error amplifiers. Each error amplifier senses the steady state output of the replica of the second stage and sets the control voltages V_{CTRLN} and V_{CTRLP}, such that, the steady state value of the second stage output approaches the reference bias voltages VGP_{REF} and VGN_{REF}, respectively. This negative feedback action regulates the quiescent current I_Q in the third stage inverter. By appropriately choosing the value of I_{BIAS} as a factor of the required I_Q, the control voltages V_{CTRLN} and V_{CTRLP} obtained from this circuit can be used in the ring amplifier shown in Fig. 3.3 for process

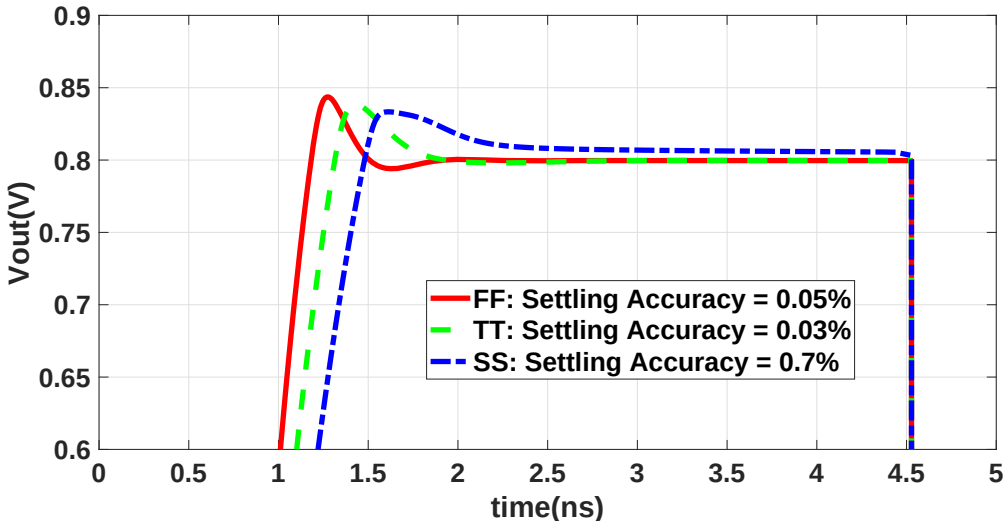

Figure 3.5: Transient response with fixed deadzone bias

invariant operation.

Although a constant current source is used in the design example, this current source can be potentially replaced with a constant transconductance based current source [15] to maintain the transconductance of the output stage constant over process, voltage and temperature (PVT) variations [15]. It should also be noted that the gain-bandwidth requirement of the error amplifier is relaxed as the deadzone regulation loop is a dc biasing network, independent of the signal path. The gain of the error amplifier used in this design is around 30dB.

3.4.2 Simulation Results

Table. 3.2 shows the consistency in the small signal parameters of the ring amplifier (GBW and PM) across TT, FF and SS corners, when the deadzone voltages are

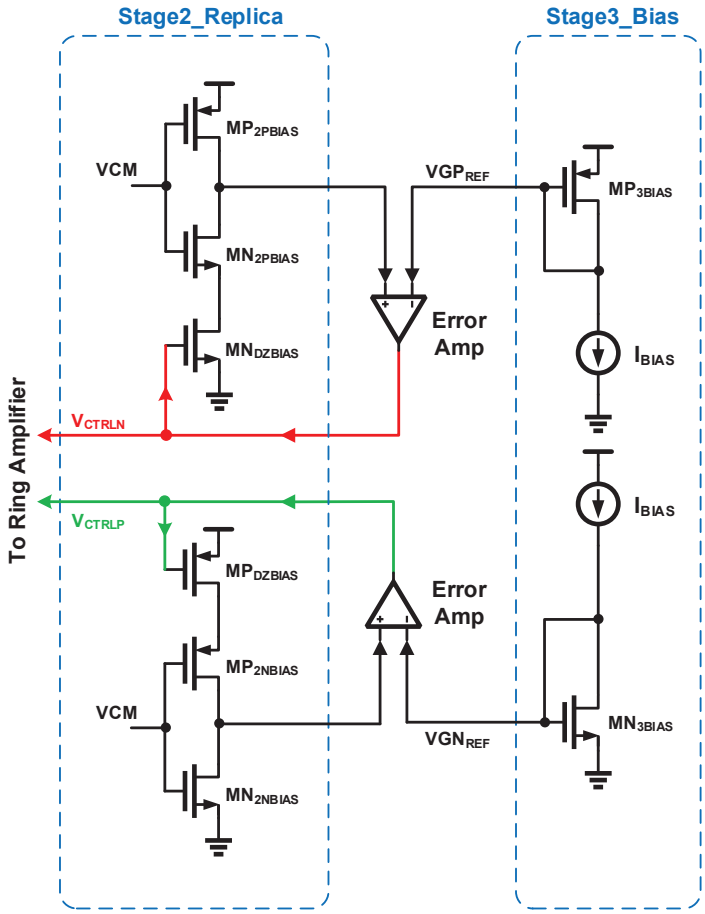

Figure 3.6: Deadzone regulation circuit for current starved inverter based ring amplifier

generated by the deadzone regulation circuit. The slightly higher value of GBW and reduced PM for SS case compared to FF case is due to the fact that, the dc gain from the first two stages are higher for the SS case compared to FF case. This is captured in the GBW equation shown in (2.43).

Fig. 3.7 shows the transient response of the ring amplifier with the deadzone regulation circuit, for a differential peak output swing of 800mV across FF, TT and SS process corners. The figure shows consistent results of $\leq$0.05% settling accuracy across TT, FF and SS corners.

Even though the proposed deadzone regulation technique is demonstrated for a current starved inverter based ring amplifier [7], the technique can also be adopted to other ring amplifier topologies [1, 6, 9, 13, 22, 23, 24, 25, 26, 27]. For example, in the traditional ring amplifier [1], shown in Fig. 3.1, the quiescent current, I_Q can be monitored in a similar fashion as in Fig. 3.6, while the feedback voltages control the deadzone voltage at the input of the second stage inverters. Similarly, in the resistor based ring amplifiers [6, 13, 22, 23, 24, 25, 26, 27], shown in Fig. 3.2, the resistor in the second stage can be replaced with a voltage controlled resistor, which can be automatically tuned by the feedback action described in 3.4.1.

Thus by using the proposed deadzone regulation technique, the ring amplifiers can be made less sensitive to process variations, irrespective of the topology being used.

Table 3.2: Consistent small signal parameters of the ring amplifier with deadzone regulation circuit.

Process Corners	**SS**	**TT**	**FF**
GBW (MHz)	475	415	380
PM (degrees)	61	68	72

3.5 Design Considerations Across Process Corners

3.5.1 Biasing for constant GBW

To design ringamps across process, voltage and temperature (PVT) variations, it is first important to understand what kind of biasing technique is required for each stage. Typically in a traditional OTA, constant-gm biasing results in constant gain-bandwidhth product (GBW) whereas constant-Id biasing results in constant current density and hence constant intrinsic gain (gm/gds) [17].

Now for a ringamp, we know that the GBW is a function of the gm of stage3 and the gains of stage1 and stage2. So to maintain constant GBW, stage3 can use constant-gm biasing and stage1 and stage2 can use constant-Id biasing.

From the analysis we can see that stage1 and stage3 control the key ringamp parameters such as noise and bandwidth, whereas stage2 so far appears to be contributing mainly in terms of additional gain in the loop and controls the stability. Stage1 design is similar to a single stage differential amplifier. Similarly stage3 design depends on its I-V characteristics, which once again is similar to that of a standard

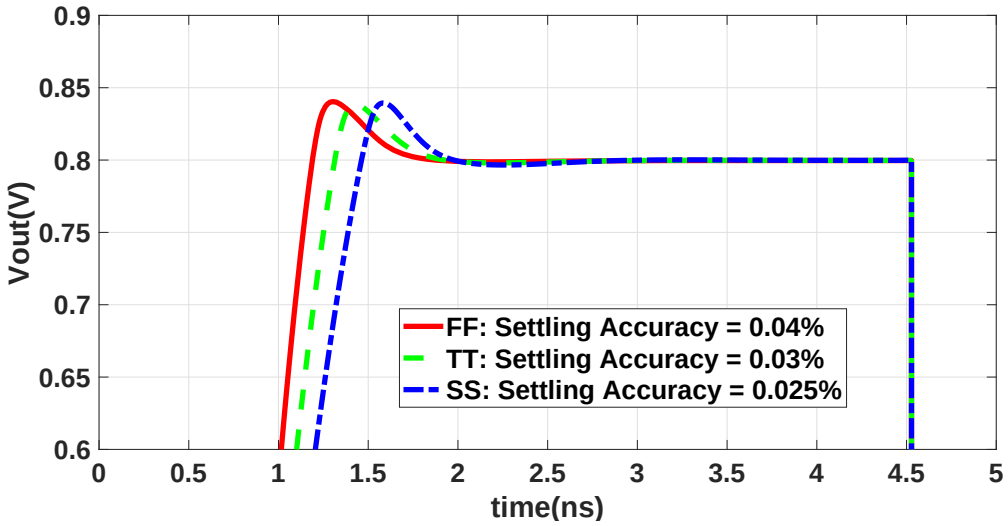

Figure 3.7: Transient response with the deadzone regulation circuit

class AB style OTA. The key difference in designing a ringamp across PVT variations comes from the design of stage2. In addition to standard OTA techniques for stage1 and stage3, the stage2 V-V input to output characteristics and the V-V deadzone control to output characteristics across PVT variations hold the key for a good design of a ringamp across PVT variations.

3.5.2 Tradeoff between Dc-gain, Noise and Phase-margin

Since stage3 is biased for constant gm, the intrinsic gain can have variations. This can result in varying dc gain across corners. Hence the dc gain specifications should be designed for worst case corners. In terms of noise specifications, since stage1 is biased for constant gain, its gm will vary. Hence to satisfy the noise requirements as dictated by (2.55), gm of stage1 should be designed for worst case corners. To

understand the impact on phase margin, the non-dominant poles from stage1 and stage2 can be simply defined as $gds/(cgs + cgd \cdot A) = f_T/(1 + \frac{cgd}{cgs} \cdot A)/A$. Since stage1 and stage2 contribute to non-dominant poles and since they are biased for constant gain, their f_T will vary across process corners resulting in varying phase margin. Since the biasing scheme aims to maintain constant GBW, the phase margin should be designed for worst case corners.

3.5.3 Simulation Results

Table. 3.2 shows the consistency in the small signal parameters of the ring amplifier (GBW and PM) across TT, FF and SS corners, when the deadzone voltages are generated by the deadzone regulation circuit. The slightly higher value of GBW and reduced PM for SS case compared to FF case is due to the fact that, the dc gain from the first two stages are higher for the SS case compared to FF case. This is captured in the GBW equation shown in (2.43).

Chapter 4: Improving Large-Signal Transient using Passive Compensation

4.1 Introduction

In this chapter, passive compensation technique is proposed to improve the settling performance of a ringamp and to minimize the power consumption of ring amplifiers in high speed applications. The ringamp is power efficient due to its dynamic operation. However, stability can be a concern for high speed applications due to the delay through the multi-stage structure of the amplifier. This need for stability results in increased static power consumption, which diminishes the power efficient benefits of the dynamic operation. Passive compensation technique is proposed that leverages the resistance of the switches in a switched capacitor feedback network to introduce LHP zeros in the negative feedback loop as shown in Fig. 4.1. Using the LHP zeros introduced by the switches R_{DAC} and R_{S2}, the proposed compensation technique can improve the large signal stability of a ring amplifier for high speed applications, while retaining the high accuracy and low power benefits that are inherent to ring amplifiers.

The organization of the chapter is as follows. Section 4.2 shows a design example showing large signal ringing in the transient response even with a sufficient phase margin in the ac response. Section 4.3 describes the proposed passive compensation

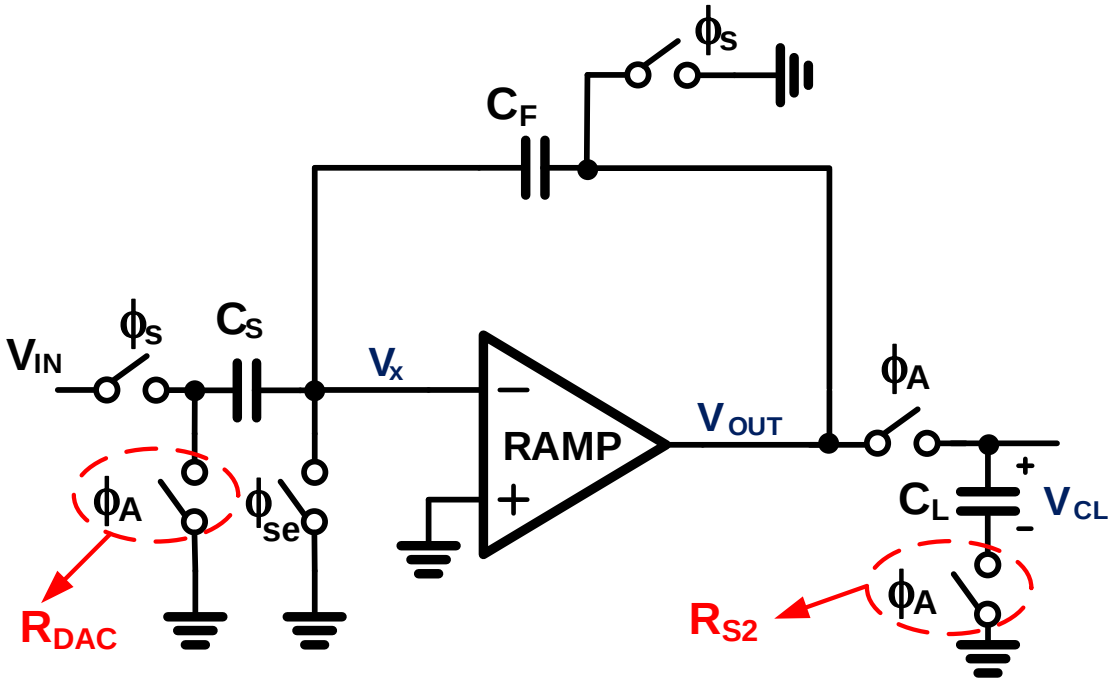

Figure 4.1: Passive compensation of ring amplifier using switches in the feedback network

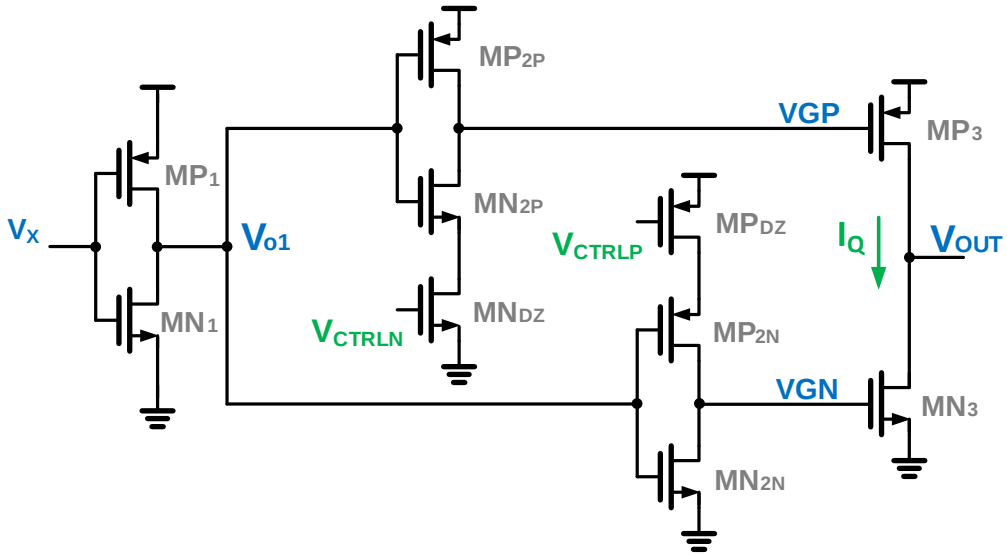

Figure 4.2: Ring amplifier using current-starved inverters. (Single-ended schematic shown for simplicity. First-stage biased with tail current sources for differential implementation)

technique, which is analogous to the derivative control in a PID controller. This section also demonstrates simulation results showing large signal stabilization of the ring amplifier using the proposed compensation technique.

4.2 Large-Signal Ringing in the Step Response

To illustrate with a design example, consider the current starved inverter based ring amplifier [7] shown in Fig. 4.2. In this structure the deadzone voltage is introduced using current starved inverters in the second stage. A fully differential structure is designed in 65nm CMOS process with a 1.2V supply voltage. Single ended schematic

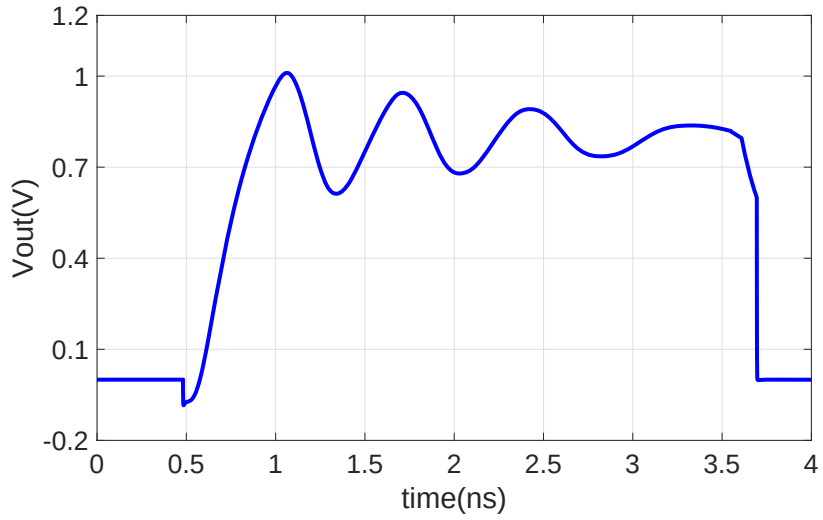

Figure 4.3: Large signal ringing even with a phase margin of 70 degrees from ac response

is shown in the figure for simplicity.

The switched capacitor amplifier in Fig. 4.1 is setup for a closed loop gain of 4 and operated at a sampling rate of 150MHz with $C_S = 2pF$, $C_F = 500fF$ and $C_L = 700fF$. The open loop gain of the ring amplifier is designed such that the settling accuracy of the output voltage is $\leq$0.02%.

The control voltages V_{CTRLP} and V_{CTRLN} set the gate bias voltage of the third stage inverter during the steady state. Hence they can be chosen to set the quiescent current I_Q and the transconductance gm_3 of the third stage during the steady state.

The GBW is designed to be 150MHz (GBW $\approx F_S$) with a phase margin of 70 degrees. From linear small signal analysis, a phase margin of 70 degrees should result in a stable settling response. However, the transient response in Fig. 4.3 shows large signal ringing even though the small signal analysis showed sufficient phase margin.

Alternative topologies have been proposed in the prior art [6, 13, 27] that use a resistor at the output of the second stage inverter at the cost of reduced slewing capability. [9] proposes dual-deadzone which alters the I-V characteristics of stage3 to smoother the large-signal to small-signal transition. [19] uses a combination of resistor based biasing and a feedback based degeneration. All the above mentioned solutions suggest architectural modifications to ringamps. A passive compensation technique described in the next section provides an architecture independent solution to reduce overshoot and ringing.

4.3 Proposed Compensation Technique

Fig. 4.1 shows the SC amplifier setup where the switches in the feedback network contribute additional poles and zeros in the loop transfer function. The switch R_{DAC} contributes to a pole-zero doublet in the feedback path. The effective frequency dependent feedback factor is thus given by (2.40),

$$\beta_z(s) = \beta(0)\left(\frac{1 + s\frac{R_{DAC}C_S}{\beta(0)}}{1 + sR_{DAC}C_S}\right) \tag{4.1}$$

$\beta(0)$ is the feedback factor at dc.

The switch resistance R_{S2} contributes to a zero in the forward path of the ring amplifier. The effective forward path transfer function of the ring amplifier is thus given by,

$$A_z(s) = A(s)\left(1 + sR_{S2}C_L\right) \tag{4.2}$$

$A(s)$ is the transfer function of the ring amplifier in the settling phase that excludes the switch resistance contribution.

With the proper choice of R_{DAC} and R_{S2}, appropriate derivative control is introduced to improve the large signal response of the ring amplifier.

The large signal stability can be improved by minimizing the delay through the first two stage inverters. However in a given technology, reducing the delay through the inverters, while maintaining the high gain, results in a large static power consumption. However, using passive compensation technique, the large signal stability can be improved without significant power penalty from the first two stages. In the following subsection, the effect of passive compensation is demonstrated for large signal ringing.

4.3.1 Large Signal Compensation

To observe the large signal ringing, slewing current is set to be large for faster slewing time, while the small signal phase margin is 70 degrees with steady state GBW approximately equal to the sampling frequency F_S. The response shows large signal ringing, which is equivalent to the response of an inverted pendulum to a large disturbance, when the derivative control is absent. Using passive compensation, appropriate derivative control is introduced using the LHP zeros resulting from R_{DAC} and R_{S2}. The LHP zeros introduced for large signal compensation are at frequencies higher than the GBW.

Fig. 4.4 shows the transient response with a differential peak output swing of

$800mV$ for different values of R_{DAC} and R_{S2}. For smaller values of R_{DAC} and R_{S2}, the derivative control introduced by the LHP zeros is too small and hence ineffective. For larger values of $R_{DAC}$and R_{S2}, the voltage drop across the resistors is too large resulting in incomplete charge across the sampling capacitor C_S and the load capacitor C_L, respectively as seen from Fig. 4.4.

Fig. 4.5 shows the transient response with and without the passive compensation. The low power implementation (3mW) with no compensation shows significant ringing. The high power implementation (11mW) with traditional compensation shows stable response. The high power consumption results from designing the the first two stage inverters to have lower delays. Finally, the low power implementation with passive compensation ($R_{DAC} = 40\Omega$ and $R_{S2} = 150\Omega$) shows stable response due to the appropriate derivative control from the LHP zeros.

4.3.2 Impact of Process Variation on Passive Compensation Technique

To realize the proposed passive compensation technique in silicon, it is important to consider the effect of process, supply voltage and temperature (PVT) variations on the operation of ring amplifiers. Since the LHP zeros are introduced at frequencies much larger than GBW of the loop, it can be shown that, even a 10% variation in the compensation resistance does not degrade the large signal stabilization. To accommodate for random mismatches, the resistances in the design are sized such that the 3σ variation in resistance is less than 5%. In addition, the use of the biasing technique proposed in Chapter 3 [30] can ensure PVT tolerant operation of the ring

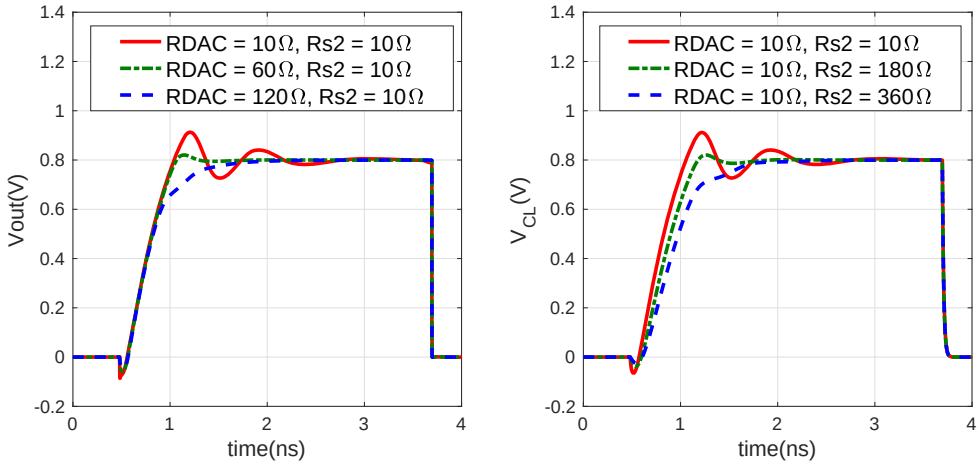

Figure 4.4: Transient response with large signal ringing. (a) Effect of R_{DAC} on the output voltage, V_{out}. (b) Effect of R_{S2} on the voltage across the load capacitor, V_{C_L}

amplifier.

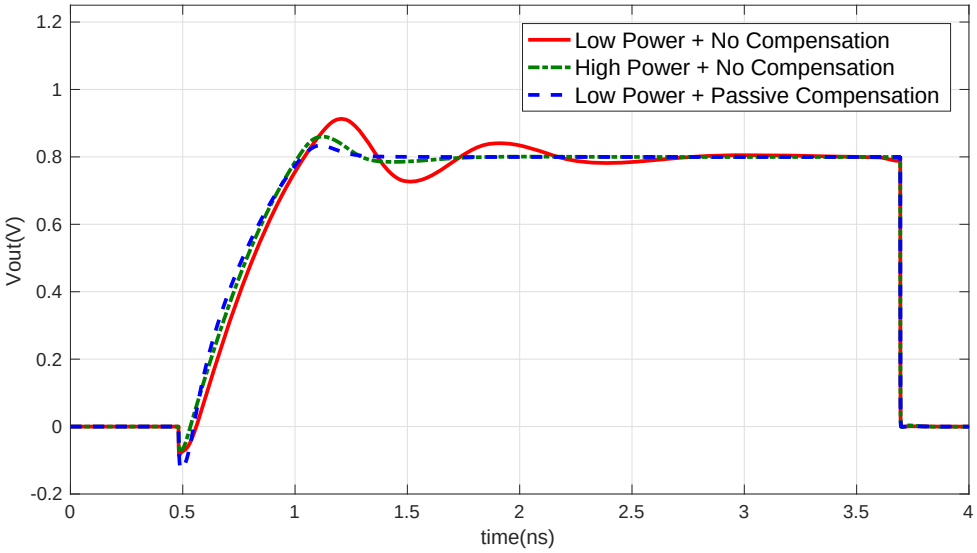

Figure 4.5: Transient response with and without passive compensation for large signal ringing

Chapter 5: Conclusion

In this thesis qualitative and quantitative analysis of ringamps were provided to develop a complete picture of the dc, ac and the large-signal operation of a ringamp. Simple RC models and OTA based analysis were used to intuitively understand the ringamp using standard analog techniques. An analogy to PID controllers is also provided to develop further intuitive understanding of ringamps. Circuit techniques are proposed to ensure robust operation of ring amplifiers.

A deadzone regulation circuit is proposed to realize process invariant biasing of ring amplifiers. Traditional ring amplifier topologies are susceptible to process variations as the the deadzone biasing is a function of the threshold voltage of the transistors in the output stage inverter. This results in variation in the quiescent current I_Q at the output stage and variation in GBW across process corners. The proposed regulation circuit uses a replica of the ring amplifier and a negative feedback loop to track the threshold voltage variations, while maintaining a constant quiescent current I_Q at the output stage of the ring amplifier. The proposed technique is validated using transistor level simulations, showing improved ac and transient response of a ring amplifier across TT, FF and SS corners. The circuit is designed in 65nm CMOS process with a 1.2V supply to achieve a closed loop gain of 4 with a settling accuracy of $\leq$0.05% and operated at a sampling rate of 125MHz. Compared to a fixed deadzone voltage, the proposed technique shows consistent ac and transient response.

The technique is demonstrated with a current starved inverter based ring amplifier. However, the technique can also be applied to other ring amplifier topologies as well.

Passive compensation technique is proposed to improve the settling performance of a ring amplifier for high speed applications, without losing its power efficiency and accuracy. The technique leverages the resistance of switches in the switched capacitor amplifier network to stabilize the amplifier response using LHP zeros. An inverted pendulum with a PID controller in feedback is used as an analogy to describe the large signal stabilization of a ring amplifier. The proposed technique is validated using transistor simulations, showing improved large signal settling response for a current starved inverter based ring amplifier. The circuit is designed in 65nm CMOS process with a 1.2V supply to achieve a closed loop gain of 4 with a settling accuracy of 0.02% and operated at a sampling rate of 150MHz. The proposed passive compensation technique saves the static power that would be required to reduce the delay through the loop, making the proposed technique highly power efficient for ring amplifiers used in high-speed applications.

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