AN ABSTRACT OF THE DISSERTATION OF

Pedram Payandehnia for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 19, 2018.

Title: Power Efficient Architectures for Low Noise Switched-Capacitor Filters and High Accuracy Analog-to-Digital Converters

Abstract approved: _____

Gabor C. Temes

Filters and data converters are key analog-and-mixed-signal (AMS) building blocks in communication systems, such as software-defined radios and internet-of-things. In this dissertation, novel switched-capacitor filter and analog-to-digital converter (ADC) circuit configurations have been explored which are power efficient and are digital scaling friendly.

First, a novel switched-capacitor low-pass filter architecture is presented. In the proposed scheme, a feedback path is added to a charge-rotating real-pole filter to implement complex poles. The selectivity is enhanced, and the in-band loss is reduced compared with the real-pole filter. The output thermal noise level and the tuning range are both close to those of the real-pole filter. A fourth-order filter prototype was implemented in a 180-nm CMOS technology. The measured

in-band loss is reduced by 3.3 dB compared with that of a real-pole filter. The sampling rate of the filter is programmable from 65 to 300 MS/s with a constant DC gain. The 3-dB cut-off frequency of the filter can be tuned from 0.490 to 13.3 MHz with over 100-dB maximum stop-band rejection. The measured in-band third-order output intercept point is 28.7 dBm, and the averaged spot noise is 6.54 nV/Hz. The filter consumes 4.3 mW from a 1.8 V supply.

Next, an opamp-free noise shaping successive-approximation register (SAR) ADC is presented. Third-order noise shaping is achieved by implementing a second-order passive filter and a passive error feedback topology. In the proposed scheme, the SAR error signals (including quantization noise, comparator thermal noise, and DAC settling error) are subjected to third-order noise shaping. Therefore, the thermal noise specifications of the comparator can be relaxed. Also, since no active element is used, the proposed scheme achieves a higher power efficiency than earlier SAR ADCs.

Finally, a novel 0-2 Multi Stage Noise Shaping (MASH) ADC is presented. The first stage is implemented using a 4-bit SAR ADC. The second stage uses a VCO-based quantizer (VCOQ). Unlike earlier VCOQs which provide first-order noise shaping, the proposed VCOQ achieves second-order noise filtering. To implement this noise shaping, the quantization noise of the VCOQ is extracted as a pulse-width-modulated (PWM) signal, and it is fed back to the VCO input using a charge pump circuit. Any error related to the charge pump circuitry will be first-order shaped at the output. Simulation results confirm the second-order noise shaping of the output of the ADC, and an excellent (14-bit SNDR) performance

with oversampling ratio (OSR) of 16.

Power Efficient Architectures for Low Noise Switched-Capacitor Filters and High Accuracy Analog-to-Digital Converters

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Pedram Payandehnia, Author

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> “ There are ladders that are hidden amidst the universe
> step by step leading towards the summit of the sky
> each cohort embraces their ladder
> there is a unique sky for every explorer’s path. ”
>
> — *Rumi (1207-1273)*

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For my parents,

Parivash and Mahmoud

Chapter 1: Introduction

A simplified high-level block diagram of a heterodyne receiver is shown in Figure 1.1. The input signal is received through an antenna. The input signal is received through an antenna. The band-select filter (or pre-select filter), which is a band-pass filter, selects the desired signal band while providing some image rejection. The linearity, noise figure, and selectivity required by this filter usually dictates passive off-chip implementation [1].

After the band-select filter, a low-noise-amplifier (LNA) amplifies the input signal. The LNA output is applied to two mixers to down-convert the signal and generate the in-phase and quadrature-phase signal components [8]. The in-phase and quadrature signal components are applied to two channels-select filters. The channel-select filters, which are low-pass filters, select the desired channel and also provide anti-aliasing filtering before the signal is sampled by analog-to-digital converters (ADCs). The outputs of channel select filters are quantized using two ADCs. The digital outputs of ADCs are processed using a digital signal processor (DSP) to extract the desired data. In this chapter, some of the design considerations of the low-pass filters and ADCs are discussed.

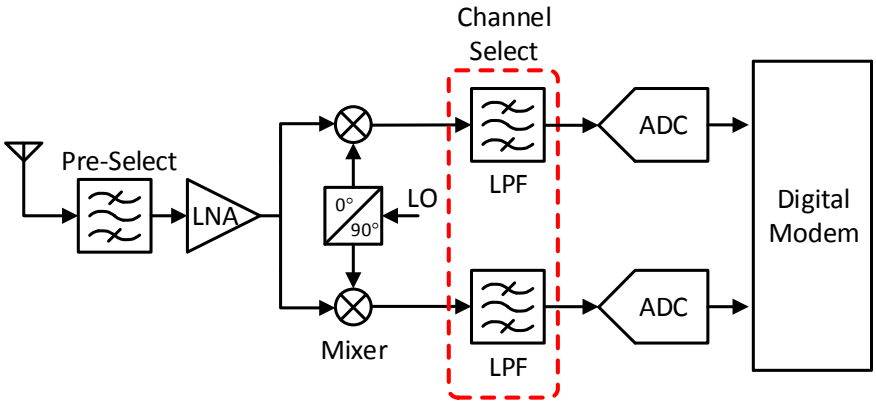


Figure 1.1: Simplified high-level block diagram of a heterodyne receiver.

1.1 Introduction to Filter Design

Filters are essential components in communication systems [9, 10, 11] to separate wanted and unwanted signals. The quality of the wanted signal is expected not to get degraded as it passes through the filter, while the unwanted signals get rejected. The desired properties of a filter include high selectivity, low pass-band ripple, low power consumption, good linearity, low thermal noise level, and a wide tuning range. In practice, there are trade-offs between these filter characteristics which depend on the architecture and order of the filter, and also on the filter application. In the following subsections, these filter characteristics are briefly explained along with some of the filter applications. Also, several design trade-offs are highlighted.

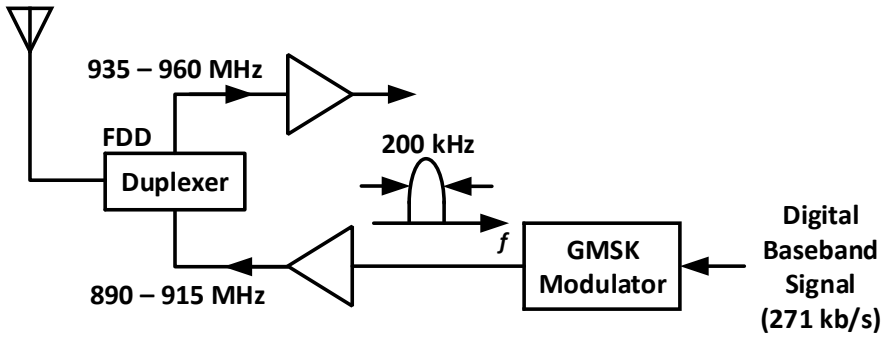


Figure 1.2: GSM900 air interface [1].

1.1.1 Selectivity

Selectivity is a measure of the ability of a filter to respond only to the desired signal and to reject unwanted signals, such as another broadcast on an adjacent channel. Selectivity is usually measured as a ratio in decibels (dBs), comparing the signal strength received against that of a similar signal at an adjacent frequency. The selectivity requirement of the filter depends on the application. For example, in global system for mobile communication (GSM), the blocking requirements of the receiver are set by the protocol standards. The GSM standard is a time-division multiple access (TDMA) system, with frequency-division duplexing (FDD. It uses gaussian minimum shift keying (GMSK) modulation [1]. Figure 1.2 shows the transmitter and the receiver bands for GSM900.

The bandwidth of the transmitted signal and the received signal is 25 MHz, while the bandwidth of each channel is 200 kHz. The blocking requirements of GSM are shown in Figure 1.3. The blocking test applies the desired signal at 3 dB above the sensitivity level, which is -102 dBm, along with a single (unmodulated) tone.

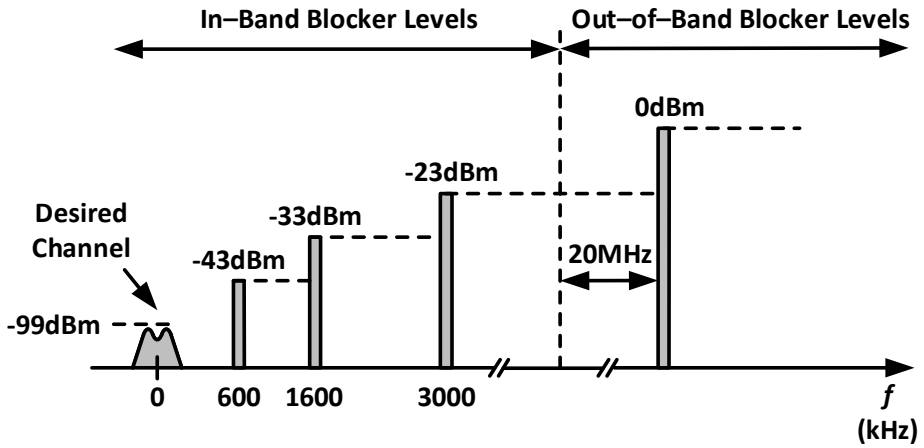
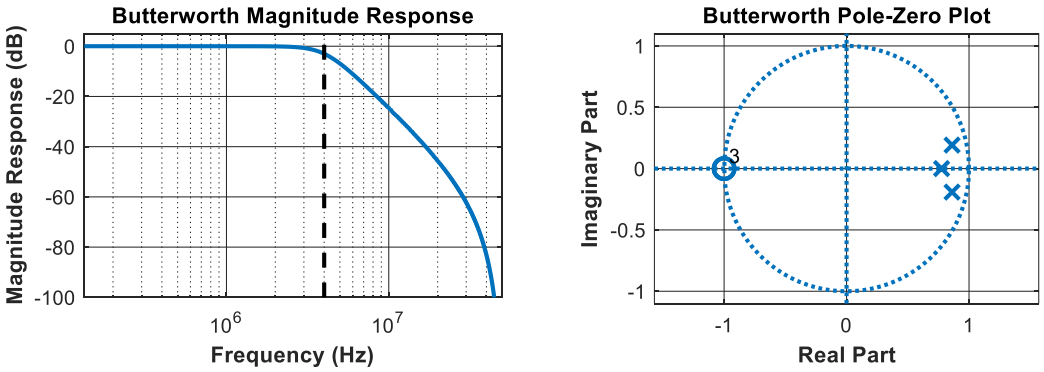
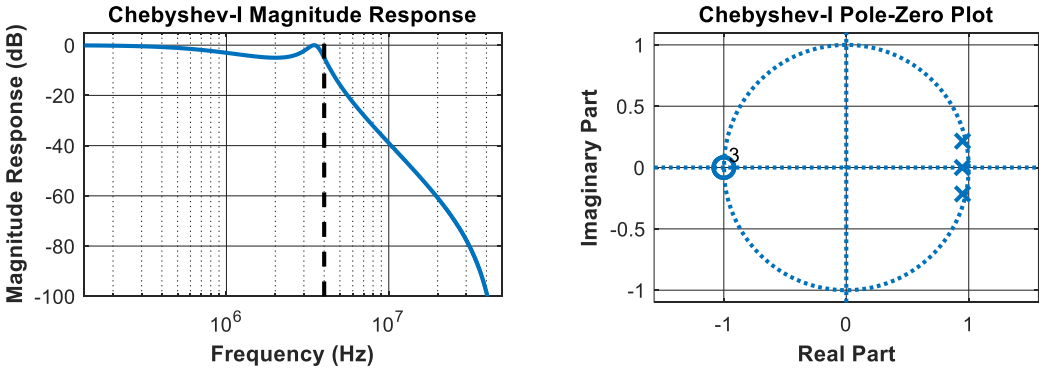


Figure 1.3: GSM receiver blocking test [1]. (The desired channel center frequency is denoted by 0 for simplicity.)

Only one blocker is applied at a time. The tolerable in-band blocker level jumps to -33 dBm at 1.6MHz from the desired channel and to -23dBm at 3MHz. The out-of-band blocker can reach 0dBm beyond a 20MHz guard band from the edge of the receiver band. The receiver is required to meet a specific bit-error-rate (BER) in the presence of the blocker. The selectivity required for the channel select filter in GSM application can be found using Figure 1.3 [1]. Since these requirements might be challenging to be implemented by one stage, usually multiple filters are implemented along the signal chain in the receiver side to provide the required blocker filtering.



(a)



(b)

Figure 1.4: Magnitude response and pole-zero locations of (a) Butterworth filter, and (b) Chebyshev-I filter. The $3dB$ bandwidth of both filters is $4MHz$.

1.1.2 Ripples in Filter Magnitude Response

In the gain response of the filters there might be ripples inside or outside the signal bandwidth. The magnitude of the ripples depends on the filter type and the locations of poles and zeros in the filter transfer function. It also depends on the circuit non-idealities.

The magnitude response of a sampled-data Butterworth filter is maximally flat

at DC. It does not have any ripple and it is monotonic. It decreases smoothly from DC to $F_S/2$, where F_S is the sampling frequency of the filter [12] [13]. The magnitude response and pole-zero locations of a 3^{rd}-order sampled-data Butterworth filter are shown in Figure 1.4a.

The magnitude response of a sampled-data Chebyshev type-I filter has ripples inside the signal bandwidth, but it is maximally flat in the stop-band. In this filter, the absolute difference between the ideal and the actual frequency response over the pass-band is minimized. The transition from pass-band to stop-band is sharper in a Chebyshev type-I filter compared to a Butterworth filter [12] [13]. The magnitude response and pole-zero locations of a 3^{rd}-order Chebyshev type-I filter are shown in Figure 1.4b.

The magnitude response in Chebyshev type-II is maximally flat in pass-band but has ripples in stop-band. The maximally flat pass-band response may be an advantage over Chebyshev type-I but the transition from pass-band to stop-band is not as sharp as that of in Chebyshev type-I. In this filter, the absolute difference between the ideal and actual frequency response over the entire stop-band is minimized [12] [13]. The magnitude response and pole-zero locations of a 3^{rd}-order sampled-data Chebyshev type-II filter are shown in Figure 1.5a.

The magnitude response of elliptic filters has ripples both in pass-band and stop-band. Compared to the other filter types, elliptic filter has the sharpest pass-band to stop-band transition. Therefore, the filter requirements can be met with the lowest order compared to the other filter types [12] [13]. This is often an important advantage as it leads to lower power consumption. The magnitude

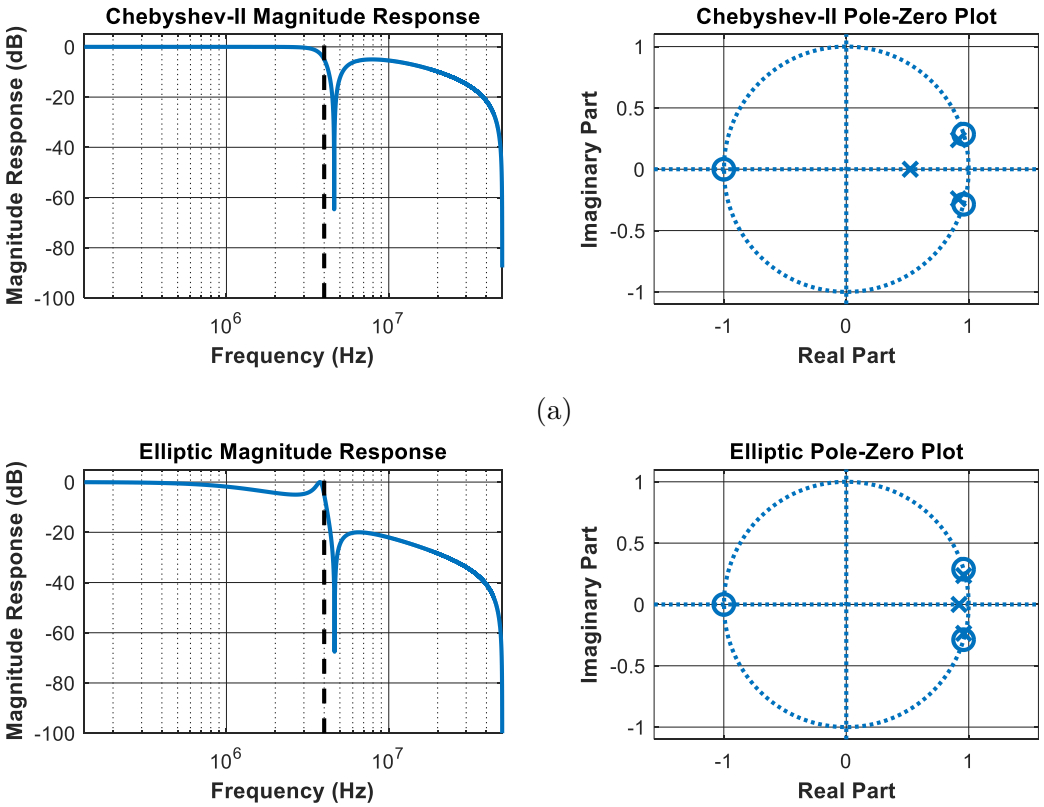


Figure 1.5: Magnitude response and pole-zero locations of (a) Chebyshev-II, and (b) Elliptic filter. The $3dB$ bandwidth of both filters is $4MHz$.

response and pole-zero locations of a 3^{rd}-order sampled-data Elliptic filter are shown in Figure 1.5b.

1.1.3 Linearity

In ADCs and RF blocks [14], the linearity is measured differently. Signal-to-noise-and-distortion-ratio (SNDR) and spurious-free-dynamic-range (SFDR) are used to measure the non-linearity in an ADC. The non-linearity in RF-blocks are usually measured using the 1dB-compression point and the $2^{nd}-$order and the $3^{rd}-$order output intercept point ($OIP2$ and $OIP3$). By referring $OIP2,3$ to the input, $IIP2,3$ can be measured. In this sub-section, we are mostly focused on non-linearity of RF-blocks.

The nonlinearity in communication systems causes harmonic distortion, gain compression, inter-modulation, and cross modulation. In this sub-section, these effects are explained briefly.

For a memoryless and nonlinear system, the input-output transfer function can be approximated with a polynomial [1]

$$y(t) = \alpha_1 \, x(t) + \alpha_2 \, x(t)^2 + \alpha_3 \, x(t)^3 + \dots \tag{1.1}$$

If a single tone $x(t) = A.cos(\omega t)$ is applied to a non-linear system, at the output, integer multiples of the input signal frequency show up, which cause harmonic distortion [1]. Assuming a 3^{rd}-order polynomial transfer function, the output can be written as

$$\begin{aligned} y(t) =& \frac{\alpha_2\ A^2}{2} + \Big(\alpha_1\ A + \frac{3\alpha_3\ A^3}{4}\Big)\cos(\omega t) + \Big(\frac{\alpha_2\ A^2}{2}\Big)\cos(2\omega t) \\ &+ \Big(\frac{\alpha_3\ A^3}{4}\Big)\cos(3\omega t) \end{aligned} \tag{1.2}$$

As (1.2) shows, the gain experienced by $x(t) = A.cos(\omega t)$ is equal to $\alpha_1 A + 3\alpha_3 A^3/4$. Therefore, the gain varies as A gets larger. If $\alpha_1.\alpha_3 < 0$, the gain absolute value decreases as A increases. This effect is quantified by 1dB compression point, defined as the input signal level for which the gain is dropped by 1dB [1]. Assuming a 3^{rd}-order polynomial transfer function, the 1dB compression point can be calculated as

$$A_{in,1dB} = \sqrt{0.145|\frac{\alpha_1}{\alpha_3}|} \tag{1.3}$$

If a large interferer signal accompanies the received signal, the receiver gain might get reduced by the large excursions produced by the interferer, even though the desired signal itself is small. This effect is called *desensitization*, and it reduces the signal to noise ratio at the receiver output [1].

The other effect of non-linearity in communication systems is cross-modulation. When a relatively weak signal and a strong modulated interferer passes through a non-linear system, modulation is transferred from the interferer to the weak signal. This phenomenon is called cross-modulation. Cross-modulation is more important in amplifiers that process several independent signal channels simultaneously, such

as orthogonal-frequency-division-multiplexing (OFDM) systems [1].

If two interferers at ω_1 and ω_2 are applied to a nonlinear system, some of the frequency components at the output are not harmonics of ω_1 or ω_2. These frequency components are generated because of the mixing (multiplication) of the two frequency components ω_1 and ω_2. This phenomenon is called inter-modulation (IM) [1]. Assuming $x(t) = A_1.cos(\omega_1 t) + A_2.cos(\omega_2 t)$ is applied to a non-linear system with a 3^{rd}-order polynomial transfer function, the inter-modulation frequency components are

$$\begin{aligned} \omega = 2\omega_1 \pm \omega_2 : \ & \Big(\frac{3\alpha_3 {A_1}^2 A_2}{4}\Big)cos(2\omega_1 + \omega_2)t + \Big(\frac{3\alpha_3 {A_1}^2 A_2}{4}\Big)cos(2\omega_1 - \omega_2)t \\ \omega = 2\omega_2 \pm \omega_1 : \ & \Big(\frac{3\alpha_3 A_1 {A_2}^2}{4}\Big)cos(2\omega_2 + \omega_1)t + \Big(\frac{3\alpha_3 A_1 {A_2}^2}{4}\Big)cos(2\omega_2 - \omega_1)t \end{aligned} \tag{1.4}$$

If ω_1 and ω_2 are close to each other, then $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are close to ω_1 and ω_2. This has a significant importance in communication systems, as demonstrated in Figure 1.6 [1]. As it shown in this figure, the desired signal at ω_0 along with two large interferers at ω_1 and ω_2 are applied to a non-linear block. If $\omega_0 = 2\omega_1 - \omega_2$, then one of the 3^{rd}-order inter-modulation frequency components fall onto the desired signal, which causes signal corruption.

To quantify the 3^{rd}-order inter-modulation, 3^{rd}-order intercept point ($IP3$) is introduced, which is measured using two-tone test. In the two tone test, two sinusoidal signals with equal magnitudes are applied at the input of the nonlinear block. The input signal level, for which the magnitude of the 3^{rd}-order inter-

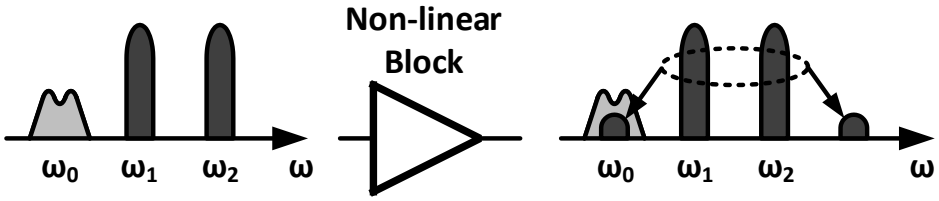


Figure 1.6: Effect of 3^{rd}-order inter-modulation [1].

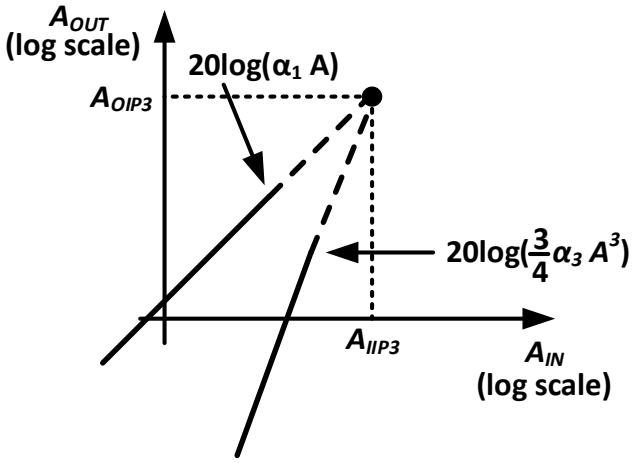


Figure 1.7: $IIP3$ and $OIP3$ [1].

modulation terms ($3/4\alpha_3 A^3$ in 1.4) becomes equal to the input signal level, is called the input 3^{rd}-intercept point ($IIP3$). Similarly, the corresponding output is represented by $OIP3$ [1]. This is shown in Figure 1.7.

The $IIP3$ can be calculated by equating the fundamental and the $IM3$ amplitudes.

$$\begin{aligned} |\alpha_1 A_{IIP3}| &= \left|\frac{3}{4}\alpha_3 {A_{IIP3}}^3\right| \\ A_{IIP3} &= \sqrt{\frac{3}{4}\left|\frac{\alpha_1}{\alpha_3}\right|} \end{aligned} \tag{1.5}$$

To measure $IIP3$ and $OIP3$, two tones with very low signal level should be applied to the device under test such that the $IM3$ is higher than the noise floor (the $IM3$ shouldn't be comparable with the noise floor). Then, the input signal level should be increased slightly. By plotting the signal levels of $IM3$ products and the fundamental tone on a log-log scale and extrapolating these plots accordingly, $IIP3$ and $OIP3$ can be measured. To make sure that the higher-order harmonics are negligible, it should be observed that for 1dB increase in A_{IN}, $IM3$ increases by 3dB [1].

1.1.4 Thermal Noise

In the filters, as for other analog-and-mixed signal circuits, there are trade-offs between output thermal noise level, power consumption, filter order and the number of active blocks used in the filter, as well as chip area.

In passive filters which are implemented using capacitors, resistors, and switches, lower output thermal noise level can be achieved compared to active filters, for the same power consumption. This is one of the advantages of passive filters over active filters. This is achieved usually at the cost of larger area. To reduce the thermal noise, it is necessary to increase the size of the capacitors which causes

larger chip area. Also, in passive filters, the transition between pass-band to stop-band cannot as sharp as in classic filters such as Butterworth or Chebyshev, which causes in-band loss. This issue will be explained in more details in the following sections.

Active filters can be implemented using different building blocks, such as active-RC stages, active switched-capacitor (SC) stages, and Gm-C blocks. The thermal noise in active filters is generated by the resistors, switches, and also by transistors. By increasing the filter order, the increased number of the active blocks will results in higher output thermal noise level. To reduce the output thermal noise level, the power consumption of the active block should be increased.

1.1.5 Bandwidth Tunability

One of the filter design requirements in the most applications is the bandwidth tunability. Depending on the bandwidth of the desired signal, the 3dB bandwidth of the filter must be adjusted accordingly. It is desirable that the shape of the in-band magnitude response of the filter, such as the ripple magnitudes or the gain of the filter, should not change as the 3dB bandwidth is changed.

In discrete-time filters, there are two main approaches to tune the filters 3dB cut-off frequency. The first approach is sampling clock frequency tuning. By changing the sampling clock frequency, the z-domain pole and zero locations of the filter transfer function do not change. The second approach is tuning the circuit component values. This can be implemented by tuning the capacitors or tuning

the trans-conductances of the transistors, depending on the filter architecture. In this approach, the locations of the poles and zeros in the filter transfer function might change, which might affect the in-band response of the filter.

In continuous-time filters, only the second approach is applicable as no clock is used.

1.2 Anti-Aliasing Filters

Anti-aliasing filters (AAF) are continuous-time filters which are essential components in sampling circuits, such as ADCs and discrete-time filters. Assuming the highest frequency component of the analog continuous-time signal is F_A, based on Nyquist Theorem, the sampling frequency (F_S) should be at least $2F_A$ to be able to recover the whole signal information in digital domain.

With no input signal filtering at the ideal sampler, any frequency components which can be in the form of signal, interferer, or noise that falls outside the Nyquist bandwidth in any Nyquist zones, will be folded back into the first Nyquist zone (signal bandwidth) [2].

To design an AAF, the first step is to know the characteristics of the signal at the input of the sampler. These characteristics include the level and the bandwidth of the desired channel, and the level and the frequency of the interferers. These characteristics are usually specified in the protocol standards.

Assuming that the highest frequency of the desired channel is F_A, the anti-aliasing filter passes signals from DC to F_A, while attenuating signals above F_A.

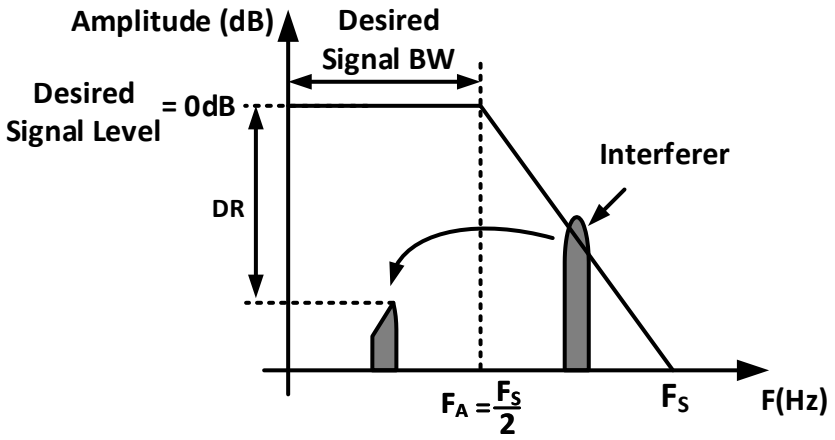


Figure 1.8: Anti-aliasing-filter (AAF)[2].

The finite transition from minimum to maximum attenuation has a significant effect on the dynamic range of the system [2]. This effect is shown in Figure 1.8.

As it is shown in Figure 1.8, any interferer with frequency components higher than $F_S/2$ will be folded-back into the signal band. These aliased components are indistinguishable from the desired channel and therefore limit the dynamic range to the value shown as DR. The required system dynamic range is usually chosen based on the requirement for bit error rate (BER).

The requirements for the AAF may include a sharp transition from pass-band to stop-band, minimal in-band ripples, and a linear phase response. Elliptic filters are one of the popular choices in designing AAF. Also, there is a trade-off between the order of AAF and the sampling rate of the ADC (or any discrete-time block after the AAF). Choosing a higher sampling rate reduces the requirements on the AAF order and the power consumption at the expense of needing a faster ADC [2].

Chapter 2: Low-power Switched-Capacitor Low-Pass Filter Design

> "Not everything that can be counted counts, and not everything that counts can be counted."
>
> — *Albert Einstein*

In this chapter a novel switched-capacitor low-pass filter architecture is presented. In the proposed scheme, a feedback path is added to a charge-rotating real-pole filter to implement complex poles. The selectivity is enhanced, and the in-band loss is reduced compared to the real-pole filter. The output thermal noise level and the tuning range are both close to those of the real-pole filter. These features make the filter suitable for high speed, low noise, and low power applications. A 4^{th}-order filter prototype was implemented in a 180 nm CMOS technology. The measured in-band loss is reduced by 3.3 dB compared to that of a real-pole filter. The sampling rate of the filter is programmable from 65 MS/s to 300 MS/s with a constant DC gain. The 3-dB cut-off frequency of the filter can be tuned from 490 kHz to 13.3 MHz with over 100 dB maximum stop-band rejection. The measured in-band 3^{rd}-order output intercept point (OIP3) is 28.7 dBm, and the averaged spot noise is 6.54 nV/$\sqrt{}$Hz. The filter consumes 4.3 mW from a 1.8 V supply.

2.1 Introduction

Integrated filters are essential components in various applications such as channel select filtering in radio frequency receivers [15, 3], anti-alias filtering before sampling [16, 6], magnetic disc read channel filtering [17, 18], etc. The desired properties of these filters include high selectivity, low passband ripple, low power consumption, good linearity, low thermal noise level, and a wide tuning range. Integrated-circuit low-pass filters (LPFs) can be implemented using Gm-C blocks [15, 19], active-RC stages [20, 21, 22], active switched-capacitor (SC) stages [23, 24, 25], source follower blocks [26, 27], ring-oscillator-based integrators [28], and passive-SC circuitry [3, 29, 30, 5, 31]. Active-RC and active-SC filters, as well as self-coupled source follower based designs, can provide high linearity. Active-RC and active-SC filters are usually implemented using opamps. Due to the need for high-quality opamps in these topologies, implementations of such filters are becoming increasingly difficult in deep submicron technologies. On the other hand, Gm-C filters and ring oscillator based filters are more power efficient and scale well with technology [32], but offer lower linearity.

Passive-SC circuits can realize power efficient high-order filters [3, 29, 30, 5]. They can provide low thermal noise level and good linearity. By making the capacitances tunable, a wide tuning range can be achieved. Passive SC-filters can be utilized to implement real poles [3, 29], as well as complex poles [30, 5]. In [3], a 7^{th}-order passive LPF is described which uses rotated charge sharing. Although a high-order filter response can be achieved using this technique, all the poles of the

filter are real, resulting in a slow roll-off between passband and stopband. Hence, it has higher in-band signal loss than classic filter topologies such as Butterworth filters, for a given stopband rejection. The in-band loss increases by increasing filter order. Also, if the same 3-dB bandwidth is considered, a higher filter order is needed to achieve the required stop-band rejection, due to the slow roll-off. Higher filter order increases the chip area, which is undesirable. In [30], a 3^{rd}-order LPF was proposed with one real pole and a pair of complex conjugate poles. However, this topology has issues in implementing higher order filters, with only one feedback path.

In this paper, a novel 4^{th}-order complex-pole LPF is presented. By adding a feedback path to the 4^{th}-order version of the real-pole filter proposed in [3], the in-band loss is reduced compared to the real-pole filter. Also, a sharper transition between pass-band and stop-band is achieved, resulting in higher stop-band rejection for the same bandwidth. These improvements are achieved by adding minimal complexity and power to the real-pole filter. The low output thermal noise level, high linearity, and wide tuning range of the proposed scheme are close to those of the real-pole filter. By using pipelining technique of the sampling capacitor [3],[31], the sampling rate is increased to 300 MS/s. These features make the filter suitable for high-speed, low-noise, and low-power applications.

The rest of this paper is organized as follows. Two prior art high-performance LPF architectures [3, 4] are reviewed in Section 2.2, to provide the background for the proposed filter. In Section 2.3, the proposed LPF is described. The circuit implementation of the filter is explained in Section 2.4. Measurement results are

summarized in Section 2.5. Finally, the conclusion is provided in Section 2.6.

2.2 Prior Art Review

In this section, two prior art high performance LPFs including a real-pole filter [3] and a complex-pole filter [4] are reviewed. Also, the features and the design issues of them are explained.

2.2.1 Real-pole LPF topology

A 4^{th}-order real-pole passive-SC LPF is shown in Fig. 2.1. It is based on the architecture reported in [3], operating in charge-sampling mode. Here a single-ended architecture is shown for simplicity, but the actual implementation is pseudo-differential. The filter operation is as follows. The input signal is continuous time, while the output signal is discrete time. The input voltage is connected to the input Gm-block, with voltage to current gain of $G_{M,IN}$, and its output current is integrated on C_{H1}. During clock phase ϕ_1, the sampling capacitor C_S, which was earlier reset, is connected to the first history capacitor C_{H1}. During the following clock phases $\phi_{2,3,4}$, C_S is connected to capacitors $C_{H2,3,4}$, sequentially. The history capacitors C_{H1-4} operate as memory elements. In the last clock phase ϕ_5, C_S is discharged, and the cycle is repeated.

The input-to-output transfer function of the filter is

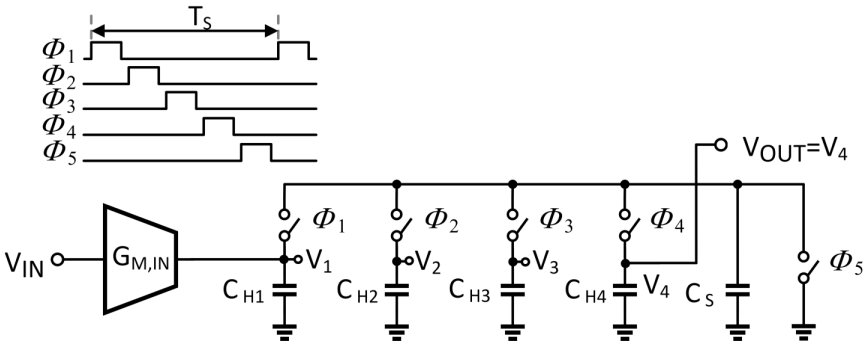


Figure 2.1: A 4^{th}-order real-pole passive-SC LPF [3].

$$\frac{V_4(z)}{q_{IN}(z)} = \frac{1}{C_S}\prod_{i=1}^{4}\left(\frac{1-\alpha_i}{1-\alpha_i z^{-1}}\right) \tag{2.1}$$

where

$$q_{IN}[n] = \int_{(n-1)T_S}^{nT_S} G_{M,IN}V_{IN}(t)\,dt \tag{2.2}$$

Here T_S represents the length of one cycle form ϕ_1 to ϕ_5. The DC gain of the filter is $G_{M,IN}.T_S/C_S$. The constants α_i are defined as

$$\alpha_i = \frac{C_{Hi}}{C_S + C_{Hi}} \qquad for\ i = 1\ to\ 4 \tag{2.3}$$

The input Gm-block and the first history capacitor C_{H1} realize a windowed integration (WI) function, which provides a continuous-time first order antialiasing filtering prior to sampling [3]. The transfer function of the antialiasing filter is

$$H_{WI}(f) = \frac{G_{M,IN}}{C_S F_S}\frac{\sin(\pi f/F_S)}{\pi f/F_S} \tag{2.4}$$

This function provides notches at kF_S (k = 1,2,3,..), which attenuates out of band signal components before they fold back into the signal band.

In this filter structure, the overall linearity is limited only by the linearity of the input Gm-block, as the linearity of the switched capacitor circuit is higher [3]. The filter also features a relatively low output thermal noise level. The output noise has two main contributors: the noise of the input Gm-block and the kT/C noise of the passive switched-capacitor network. As measurement results in [3] show, the in-band output noise level is dominated by the noise of the Gm-block. Since only one active block is used in this filter, the output thermal noise level is very low.

The main drawback of the real-pole filters is the slow roll-off between passband and stopband. In Fig. 2.2, the normalized gain response of a 4^{th}-order Butterworth filter with a BW of 6 MHz is compared with those of two real-pole filters with different specifications. Real-pole filter-1 has the same stop-band rejection (54 dB) as the Butterworth filter at 30 MHz, while real-pole filter-2 has the same 3-dB BW as the Butterworth filter (6 MHz). To minimize the in-band loss, all poles are at z = 0.826 in real-pole filter-1. The poles of the Butterworth filter are located at z = 0.917 $\pm$ j0.162 and z = 0.837 $\pm$ j0.061. The average in-band loss (within a 6 MHz BW) of the real-pole filter-1 is 6.05 dB, much higher than that of the Butterworth filter (0.39 dB). A typical application of this filter is in a receiver signal chain [3, 33, 16], as shown in Fig. 2.3. In [3], the filter loss is compensated after the ADC by using an equalizer in digital domain. To implement this compensation technique, the ADC dynamic range needs to be

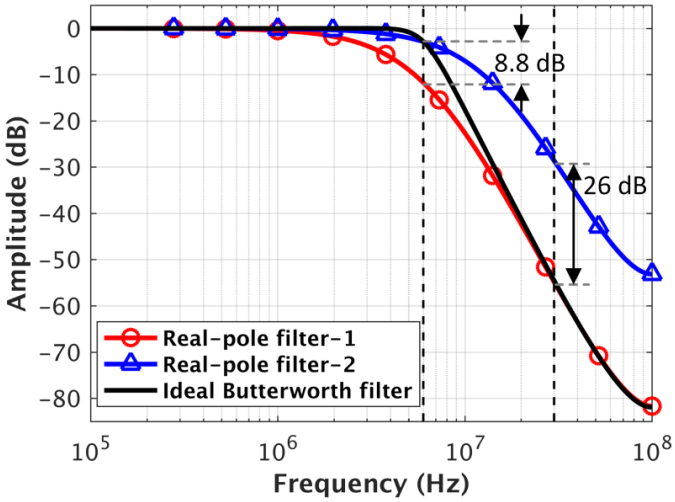


Figure 2.2: Normalized frequency response of a 4th-order Butterworth filter compared to two real-pole filters (of Fig. 2.1): filter-1 with the same out of band rejection, and filter-2 with the same 3 dB bandwidth. The sampling rate of the filters is 200 MS/s.

increased to compensate for the filters droop. For example, as mentioned in [3], the ADC requires up to 1.8 additional effective-number-of-bits (ENOB) in a 7^{th}-order filter. Based on the Walden figure-of-merit (FOM) [34], the ADC power consumption increases by 248% when the ADC resolution is increased by 1.8 ENOB for a constant FOM. This approach has thus considerable power and area overhead.

Fig. 2.2 shows also the gain response of real-pole filter-2, designed to have the same 3-dB BW as the Butterworth filter. All poles of real-pole filter-2 are located at $z = 0.644$. These two filters have almost the same average in-band loss. However, the stop-band rejection of the real-pole filter-2 is 26 dB lower than that of the Butterworth filter at 30 MHz.

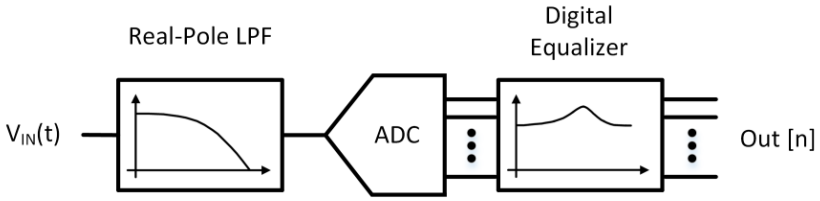


Figure 2.3: The system for equalizing the in-band loss of the real-pole filter in digital domain [3].

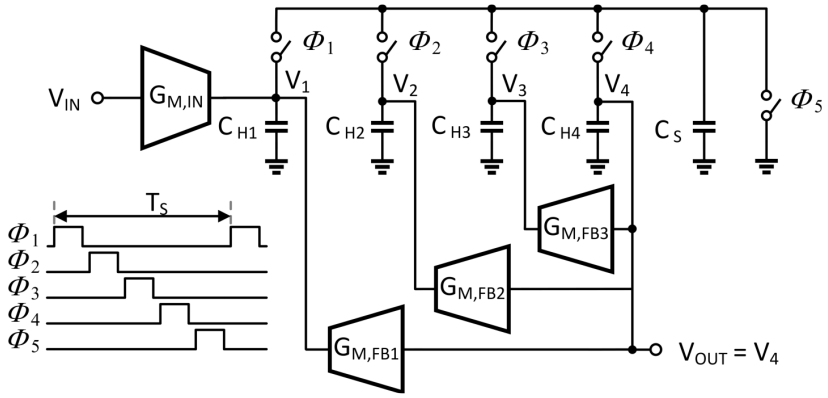


Figure 2.4: A 4^{th}-order complex-pole filter [4].

2.2.2 Complex-pole LPF

Another filter topology is introduced in [4] in which the in-band loss is mitigated by implementing complex-poles. A 4^{th}-order version of this filter is shown in Fig. 2.4. Three feedback paths are added to the real-pole filter [3] to implement the complex-poles.

The filter shown in Fig. 2.4 is designed to realize a Butterworth response with a 3-dB cut-off frequency of 2 MHz, and a sampling rate of 200 MHz. The locations of the complex-conjugate poles, which are those of an ideal Butterworth LPF, are

$$\alpha_{1,2} = 0.9746 \pm \text{j}0.0566$$
$$\alpha_{3,4} = 0.9433 \pm \text{j}0.0227 \tag{2.5}$$

The filter parameters are listed in Table 2.1. The average in-band loss for the Butterworth filter is 0.45 dB, while for the real-pole filter is 6.2 dB for the same stop-band rejection (56 dB at 10 MHz).

Another 4^{th}-order LPF is introduced in [35], which is implemented as the cascade of biquads. To implement complex-poles, two Gm-blocks are added.

Although the in-band loss is reduced, the LPF architectures reported in [4],[35] have some shortcomings.

As mentioned in Section 2.2. A, the output-referred thermal noise is dominated by the input Gm-block in the real-pole filter in Fig. 2.1. Adding three more Gm-blocks in [4], and two more Gm-blocks in [35] increases the output thermal noise significantly. Since one of the main advantages of the real pole filter is the low output thermal noise [3], the higher noise level in the LPF shown in Fig. 2.4 is a

Table 2.1: Design parameters of the LPF shown in Fig. 2.4

Parameter	**Value**
F_S	200 MHz
C_S	1 pF
C_{H1-4}	23.85 pF
$G_{M,FB1}$	-214.2 A/V
$G_{M,FB2}$	-277.2 A/V
$G_{M,FB3}$	-404.6 A/V

major drawback. To lower the output thermal noise level, the power consumption of the $G_{M,FB}$ blocks needs to be increased. Furthermore, the linearity of the filter is degraded due to the nonlinearity of the $G_{M,FB}$ blocks.

The normalized signal swings at the internal nodes of the filter shown in Fig. 2.4 are simulated in Fig. 2.5. As the figure shows, the maximum signal swing on the first history capacitor is 13 dB higher than that of the output node. This limits the dynamic range of the LPF. In the real-pole filter shown in Fig. 2.1, the maximum signal swings at the internal nodes of the filter are the same as that of the output node.

Unlike in the opamp-based LPF topologies, in the topology shown in Fig. 2.4, the maximum signal swing on the internal nodes of the filter cannot be reduced by adjusting the values of the capacitors. Specifically, to scale down the voltage swing on C_{Hi} by n times, either C_{Hi} value must be increased by n times, or $G_{M,FBi}$ should be reduced by n times (i=1-3). Since both the C_{Hi} and the $G_{M,FBi}$ values are dictated by the pole locations, there is no such freedom.

The LPF topology in Fig. 2.4 reduces the in-band loss, but does not keep some of the attractive features of the real-pole filter, such as low thermal noise level, good linearity and low power consumption. In the next section, an alternative LPF topology is proposed which reduces the in-band loss, while minimizing the performance degradations due to the feedback paths.

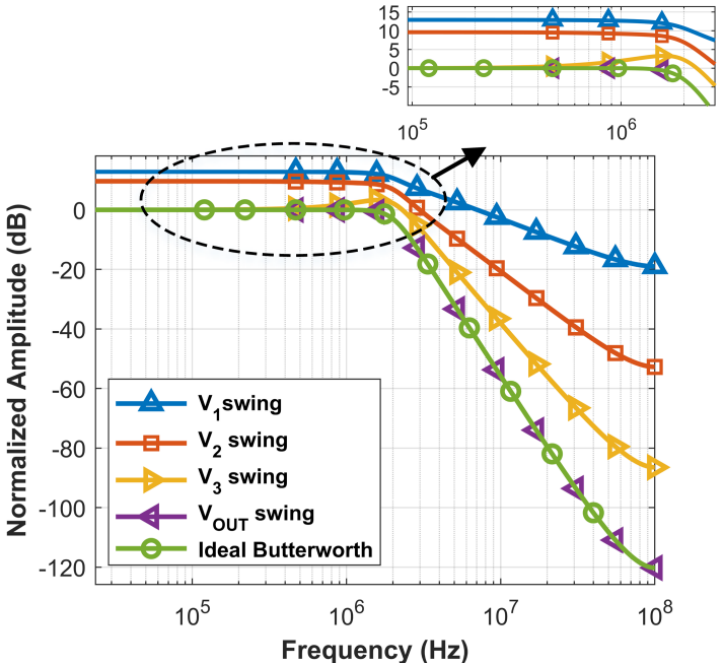


Figure 2.5: Frequency responses of the filter shown in Fig. 2.4.

2.3 Proposed Filter Topology

In this section, the proposed LPF with complex poles is presented. The scheme is shown in Fig. 2.6. In this figure, a single ended architecture is shown for simplicity, while the actual implementation is pseudo-differential. In the proposed scheme, a feedback path is implemented by adding the $G_{M,FB}$ block between C_{H4} and C_{H1}. Unlike in the architecture reported in [4], a single feedback path is added here. As explained in the following subsection, complex conjugate poles are implemented using this feedback path, and the in-band loss is reduced. As in [3], $G_{M,IN}$ and C_{H1} form a first-order anti-aliasing filter with the transfer function given in (2.4). Due to this feature, the unwanted tones with frequencies higher than F_S are attenuated

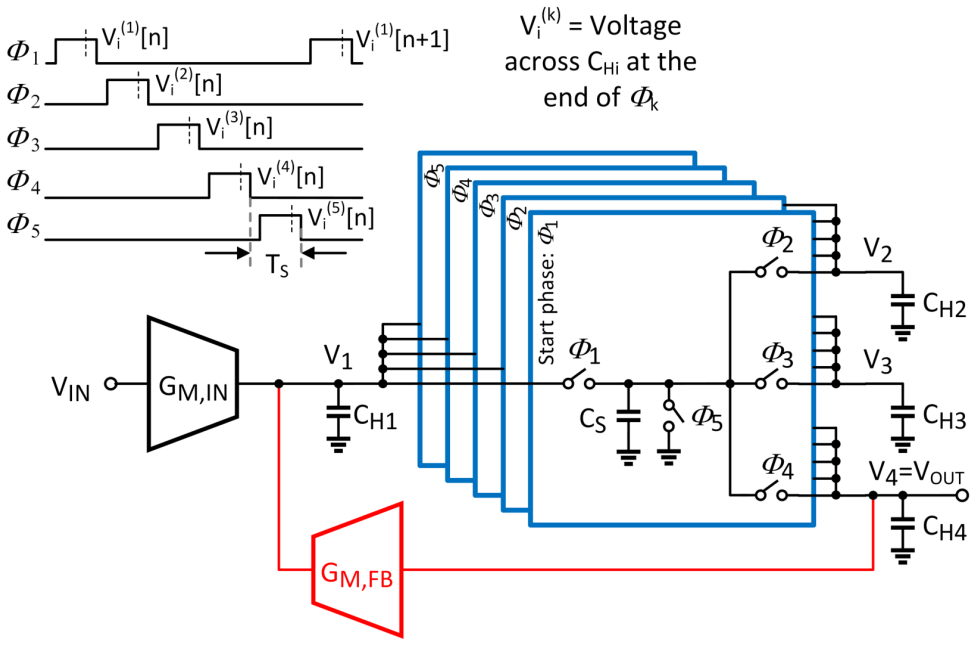


Figure 2.6: The proposed filter architecture.

before folding back into the signal band. Moreover, to speed up the operation, pipelining technique is used, similar to the filter in [3]. This is implemented by using five C_S capacitors in place of the single C_S of the real-pole filter shown in Fig. 2.1. The timing of the clock phases is also shown in Fig. 2.6. In the following subsections, the filter operation is explained, and the features of the filter are discussed.

2.3.1 Frequency-domain analysis

The input-output transfer function of the filter can be calculated by using the charge conservation principle. As it is shown in Fig. 2.6, $V_i^{(k)}$ represents the

voltage across C_{Hi} at the end of ϕ_k, in the discrete-time domain. For example, $V_2^{(5)}$ represents the voltage across history capacitor C_{H2} at the end of ϕ_5. To simplify the analysis, it is assumed that an input charge packet $q_{IN}[n]$ injected by $G_{M,IN}$ arrives in every cycle at ϕ_1. Then $q_{IN}[n]$ is given by

$$q_{IN}[n] = \int_{(n-1)T_S}^{nT_S} G_{M,IN} V_{IN}(t)\, dt \tag{2.6}$$

Here T_S represents the length of each clock phase. The parameters α_{1-4}, g_1 and v_{FF} are defined as follows

$$\alpha_i = \frac{C_{Hi}}{C_{Hi} + C_S} \qquad for\ i = 1, 2, 3, 4 \tag{2.7}$$

$$g_1 = \frac{G_{M,FB1}}{(C_{H1} + C_S)F_S} \tag{2.8}$$

$$v_{FF}[n] = \frac{q_{IN}[n]}{(C_{H1} + C_S)} = \frac{(1 - \alpha_1)}{C_S} q_{IN}[n] \tag{2.9}$$

Using the charge conservation principle, the voltage across C_{H1} at the ends of phases ϕ_{1-5} can be found:

$$V_1^{(1)}[n] = \alpha_1 V_1^{(5)}[n-1] + g_1 V_4^{(1)}[n] + v_{FF}[n] \tag{2.10}$$

$$V_1^{(k+1)}[n] = \alpha_1 V_1^{(k)}[n] + g_1 V_4^{(k+1)}[n] \tag{2.11}$$

where $k = 1, 2, 3, 4$. Similarly, the voltage across $C_{H2,3,4}$ at the ends of ϕ_{1-5} are

$$V_m^{(1)}[n] = \alpha_m V_m^{(5)}[n-1] + (1-\alpha_m) V_{m-1}^{(5)}[n-1] \tag{2.12}$$

$$V_m^{(k+1)}[n] = \alpha_m V_m^{(k)}[n] + (1-\alpha_m) V_{m-1}^{(k)}[n] \tag{2.13}$$

where $m = 2, 3, 4$ and $k = 1, 2, 3, 4$. By using (2.6) to (2.13), the input-output transfer function can be calculated in the z-domain. The output signal is the voltage across C_{H4} which can be calculated using $V_4^{(1-5)}[n]$. By expanding $V_4^{(1-5)}[n]$ in the time domain, and shifting them with proper delays, $V_4(z)$ can be found.

$$\begin{aligned} V_4(z) =& V_4^{(1)}(z^5) + z^{-1} V_4^{(2)}(z^5) + z^{-2} V_4^{(3)}(z^5) \\ &+ z^{-3} V_4^{(4)}(z^5) + z^{-4} V_4^{(5)}(z^5) \end{aligned} \tag{2.14}$$

Assuming all history capacitor are equal, $V_4(z)/q_{IN}(z)$ is found to be:

$$\frac{V_4(z)}{q_{IN}(z)} = \frac{1}{C_S} \frac{(1-\alpha)^4 z}{((z-\alpha)^4 - g_1(1-\alpha)^3 z)} \tag{2.15}$$

From (2.6) and (2.15) the DC gain of the filter is

$$A_V = \frac{V_4}{V_{IN}} = \frac{G_{M,IN} T_S}{C_S - G_{M,FB} T_S} \tag{2.16}$$

The resulting normalized gain response of the proposed filter is compared to

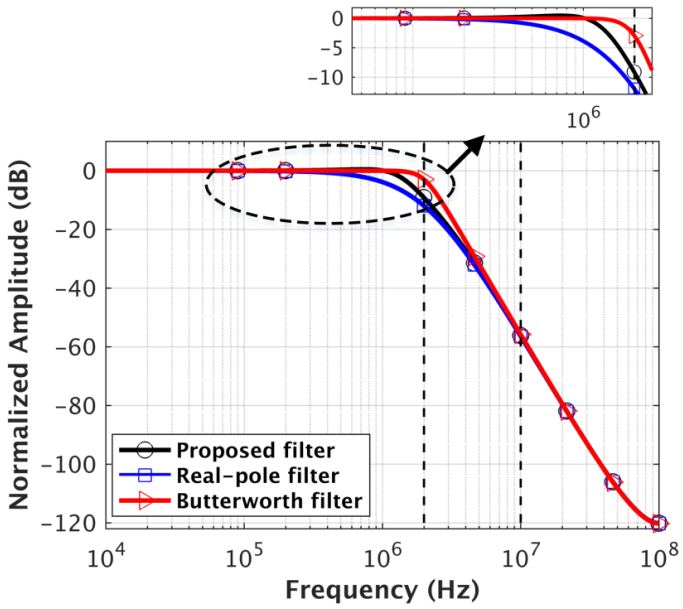


Figure 2.7: Frequency response of the proposed 4^{th}-order LPF filter, the 4^{th}-order real-pole filter, and the ideal Butterworth filter, with sampling frequency of 200 MS/s.

those of an ideal Butterworth filter and a real-pole filter in Fig. 2.7. The stop-band rejection of all three filters is 56 dB at 10 MHz. The peaking in the pass-band for the proposed filter is 0.45 dB. In Fig. 2.7, the poles of the Butterworth filter are given by (2.5) and the poles of the real-pole filter are all located at $z = 0.939$. The pole locations of the proposed filter are discussed in the next section. The design parameters of the proposed topology are listed in Table 2.2.

As Fig. 2.7 shows, the proposed filter has a sharper roll-off than the real-pole filter, but not as sharp as that of the Butterworth response. Also, the average in-band loss is reduced compared to the real-pole filter.

The gain responses related to the internal nodes of the proposed filter are

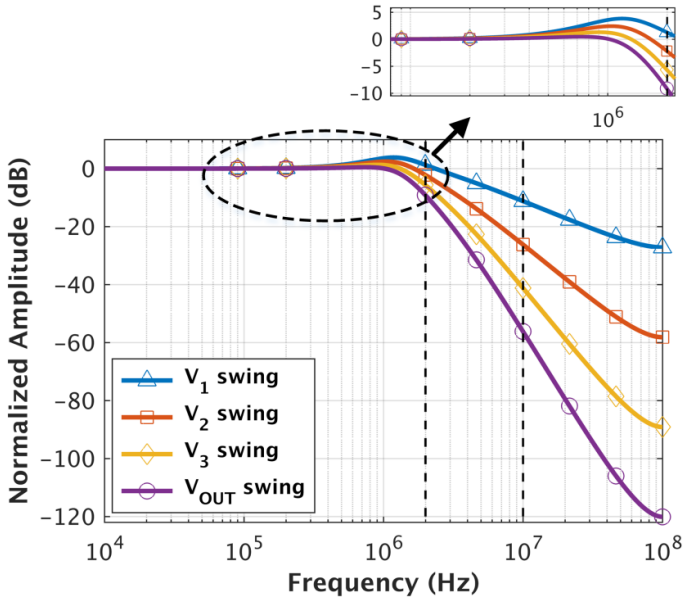


Figure 2.8: Frequency responses of the internal nodes of the proposed 4^{th}-order LPF with sampling frequency of 200 MS/s.

simulated in Fig. 2.8. The maximum signal swing of V_1 is 3.8 dB which is higher than that of the other internal nodes of the filter.

In the following subsections, the pole locations and the average in-band loss are discussed in more detail.

2.3.2 Root locus of the poles as a function of $G_{M,FB}$

As can be seen from (2.15), by tuning the value of $G_{M,FB}$ the pole locations can be adjusted. In Fig. 2.9, the root locus of the proposed LPF based on the design parameters shown in Table 2.2 is plotted as a function of $G_{M,FB}$.

In this plot, the value of $G_{M,FB}$ is swept from 0 to -3.63 mA/V while C_H

Table 2.2: Design parameters of the proposed LPF

Parameter	**Value**
F_S	200 MHz
C_S	1 pF
C_{H1_4}	17.18 pF
$G_{M,FB}$	-109.1 μA/V

and C_S have fixed values. For $G_{M,FB} = 0$, the poles are located on the real axis at $z = 0.945$, as expected. By increasing the value of $|G_{M,FB}|$ the poles become complex conjugate. For $G_{M,FB}$ = -760 μA/V, one pair of the poles crosses the unit circle and the circuit becomes unstable. Therefore, to keep the circuit robustly stable, $|G_{M,FB}|$ should be much less than 760 μA/V.

In Fig. 2.9, the pole locations of an ideal Butterworth LPF with the same stop-band rejection (56 dB at 10 MHz) are also shown. Clearly, by using just one feedback path in the proposed LPF (as opposed to the three feedback paths in the LPF shown in Fig. 2.4) the ideal Butterworth poles given by (2.5) cannot be realized. However, for well-chosen values of $G_{M,FB}$, the pole locations can get close enough to those of the Butterworth filter. For $G_{M,FB}$ = -109.1 μA/V the pole locations are

$$\begin{aligned} \alpha_{1,2} &= 0.9780 \pm \mathrm{j}0.0335 \\ \alpha_{3,4} &= 0.9120 \pm \mathrm{j}0.0324 \end{aligned} \tag{2.17}$$

close to those given in (2.5). The in-band peaking in the gain response of the filter is 0.45 dB which is the desired value in this design.

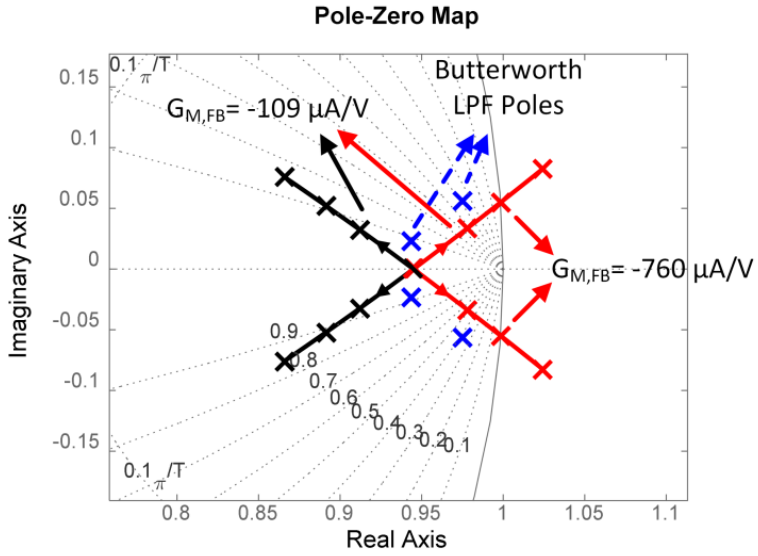


Figure 2.9: Root locus of the proposed LPF as a function of $G_{M,FB}$.

2.3.3 Frequency response and in-band loss reduction as a functoin of $G_{M,FB}$

To investigate the effect of increasing $|G_{M,FB}|$ on the in-band peaking, and the average in-band loss, five filters were designed with different values of $G_{M,FB}$ and C_{H1-4}. All filters were designed using (2.6, 2.15) to provide the same stop-band rejection (56 dB at 10 MHz). The filter design parameters are shown in Table 2.3. The C_S value is 1 pF and the F_S value is 200 MHz for all the filters.

The simulated frequency responses of the filters are shown in Fig. 2.10. Larger in-band peaking results for higher $|G_{M,FB}|$. As $G_{M,FB}$ changes from 0 to -237.6 μA/V, the in-band peaking varies form 0 dB to 3.46 dB. Increasing $|G_{M,FB}|$ will move one pair of the poles close to the unit circle, thus the in-band peaking in-

creases.

Among the internal nodes of the filter, V_1 has the highest signal swing. The swing of V_1, normalized to the output voltage and assuming all history capacitors are equal, is given by

$$\frac{V_1(z)}{V_4(z)} = (\frac{z - \alpha}{1 - \alpha})^3 \tag{2.18}$$

As can be seen in (2.18), V_1/V_4 is a function of C_H and C_S. The simulated average in-band loss and the maximum signal swing of V_1 normalized to $V_4(DC)$ is shown in Fig. 2.11. By increasing $|G_{M,FB}|$, the average loss is reduced from 6.2 dB (for $G_{M,FB} = 0$) to 0.75 dB (for $G_{M,FB}$ = -237 μA/V). At the same time, the maximum signal swing on C_{H1} increases, since both $G_{M,FB}$ and C_{H1-4} are changed.

Table 2.3: Design parameters for five different LPFs.

C_{H1-4}	$G_{M,FB}$
15.39 pF	0 μA/V
16.20 pF	-51.7 μA/V
17.18 pF	-109.1 μA/V
17.90 pF	-169.8 μA/V
18.80 pF	-237.6 μA/V

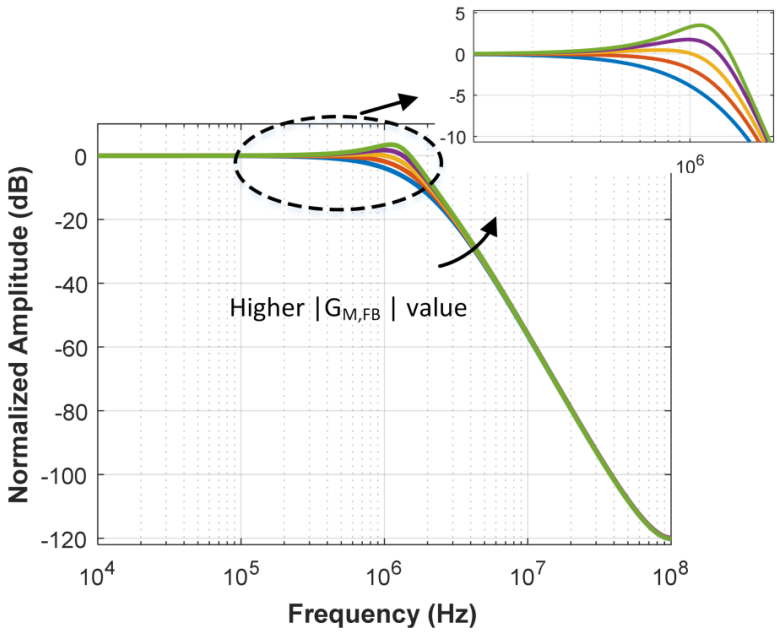


Figure 2.10: Frequency response of the proposed LPF for different values of $G_{M,FB}$ and C_{H1-4} based on the Table 2.3. Sampling frequency is 200 MS/s.

2.3.4 Trade-off between noise, power, linearity and the number of feedback paths

As discussed above, by adding a feedback path to the real-pole filter the in-band loss can be reduced significantly. The value of $G_{M,FB}$ should be determined by the desired in-band peaking in the frequency response of the filter. By adding just one feedback path to the real-pole filter, as compared to three feedback paths in the filter topology shown in Fig. 2.4, the increase in the output thermal noise is minimized. Also, since only one feedback path is added, the linearity degradation caused by active blocks is small. Specially, the feedback path is from the 4^{th}-order

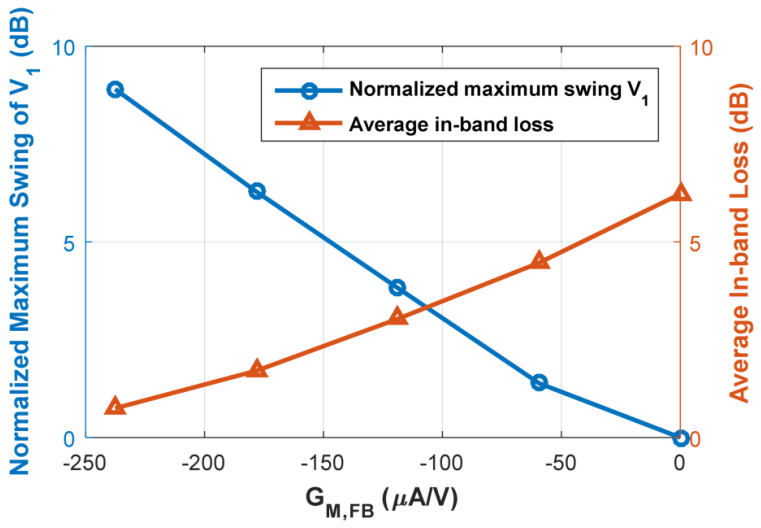


Figure 2.11: Average in-band loss and maximum signal swing of V_1 normalized to $V_4(DC)$ for different values of $G_{M,FB}$ and C_{H1-4} (based on the Table 2.3).

output of the filter, where out of band blockers are heavily attenuated before reaching to the $G_{M,FB}$ block. Therefore, nonlinearity effect of this block is minimized. These are the main features of the proposed scheme.

As an example, for the proposed filter with the parameters shown in Table 2.2, the average in-band loss is 3 dB, while for the real-pole filter it is 6.2 dB, for the same stop-band rejection at 10 MHz. Thus, the average in-band loss is reduced by 3.2 dB. The in-band output peaking is 0.45 dB, and the maximum swing on C_{H1} is 3.8 dB higher than at the output. Compared to the filter topology shown in Fig. 2.4, the maximum signal swing at the internal nodes (across C_{H1}) is reduced by 9.2 dB.

2.3.5 Feedback path implementation approaches

The feedback path can be implemented using active or passive circuitry [30],[5], [36]. A differential implementation of the filter reported in [5] is shown in Fig. 2.12, where eight clock phases are used. The C_S capacitor is not reset during ϕ_5. Instead, it is switched to C_{H1} in the other differential half circuit. Since the initial voltage of C_S, while it is connecting to the other differential half circuit, is the output voltage, a feedback path is implemented between C_{H4} and C_{H1} passively. The feedback value can be controlled by setting proper value for C_{RST} [5]. A similar approach is used in [30] in a 3^{rd}-order filter. Using passive circuitry to implement the feedback path, the output thermal noise level is lower. Also, the circuit needs less power [30], [5].

A typical application of this filter is the channel select filter in the receiver signal chain [3], [33], [16]. A drawback of the feedback approach in [30], [36], [5] is that a buffer is usually needed between the LPF output and the next stage. For example, in [3] the LPF output is connected to an ADC input, as shown in Fig. 2.3. To drive the ADC input capacitance, an analog buffer should be added between the two blocks. Considering the low thermal noise level and high linearity requirements of the buffer, the buffer may introduce considerable power overhead. By using active circuitry in the feedback path, as in the proposed architecture, the buffer can be omitted. The circuit can be implemented as shown in Fig. 2.13. The C_S capacitor is not reset after it got connected to V_4. Instead, it is used to provide the sampled voltage of the filter output for the following stage. If a SAR ADC [37]

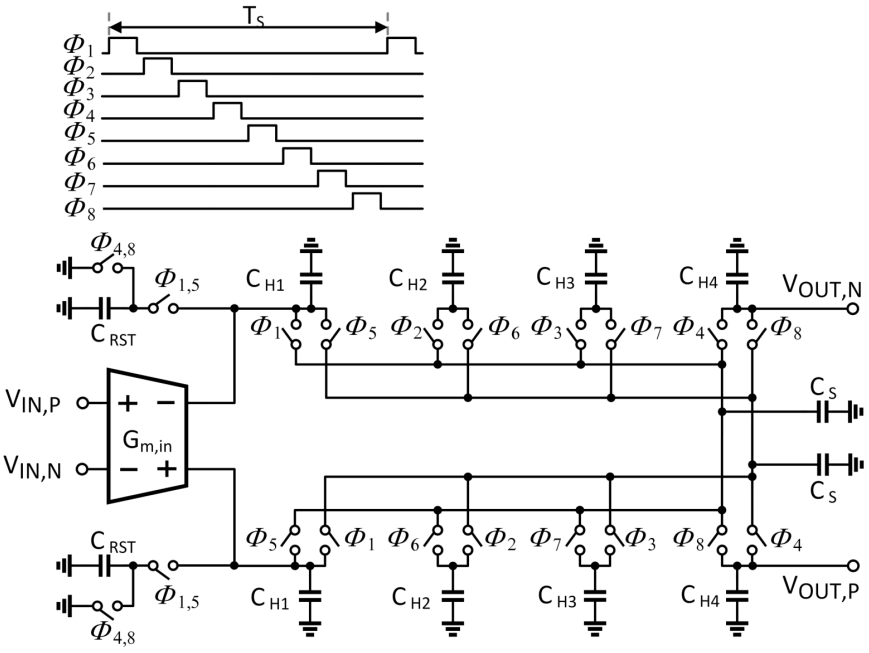


Figure 2.12: Passive feedback path implementation in [5].

is used in the next stage, C_S can be used to charge up the DAC capacitor inside the SAR ADC through passive charge sharing. Next, C_S is reset to ground. Since one more pipeline stage is used compared to Fig. 2.6, an added C_S capacitor is needed in this architecture. In the experimental work described in this paper, we used active circuitry to implement the $G_{M,FB}$ block.

2.3.6 Matching accuracy requirements

In the proposed LPF scheme, there are four different mismatch error sources: 1) inaccurate $G_{M,IN}$ value, 2) inaccurate $G_{M,FB}$ value, 3) mismatch among the C_H

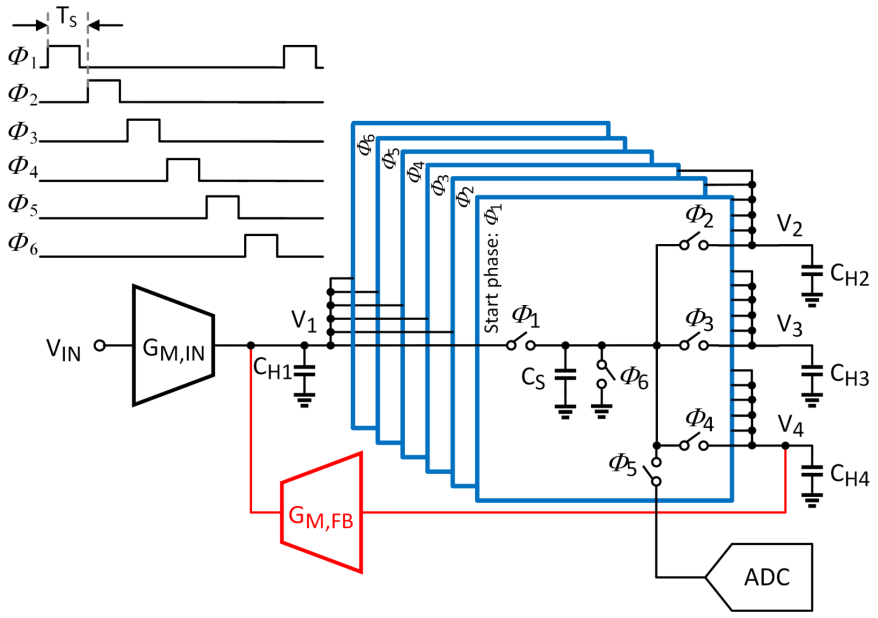


Figure 2.13: Proposed technique for removing the buffer between filter output and the next stage input in the proposed LPF.

capacitors, and 4) mismatch among the C_S capacitors. The deviation of $G_{M,IN}$ from its ideal value only changes the DC gain. This is acceptable in most of the systems where an automatic gain control (AGC) loop exists. Error in $G_{M,FB}$ value can cause some changes on the in-band peaking and pole locations. However, as can be seen in the root-locus in Fig. 2.9 and the frequency response of the filter in Fig. 2.10, the sensitivity of the filter response to the changes in the value of $G_{M,FB}$ is low. Matlab simulations show that $\pm 20\%$ variations in the $G_{M,FB}$ value causes $\pm$ 0.8 dB change in the average in-band loss and $\pm 7\%$ change in the filter bandwidth. Therefore, it has negligible effect on the filter transfer function. The mismatch between different $C_H s$ shifts the pole locations, but does not cause

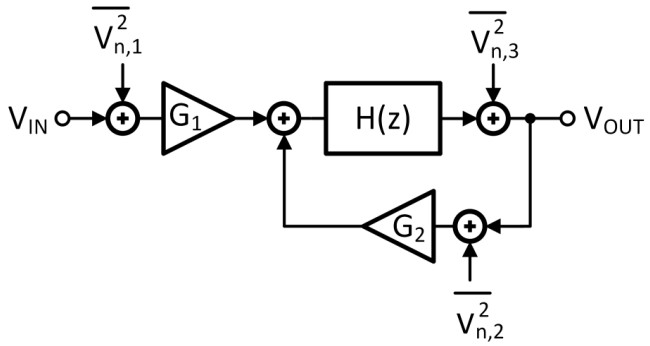


Figure 2.14: The noise model for the proposed filter.

nonlinearity. Also, these capacitors have typically a large value and are of the same type. Therefore, they can be well matched. However, the mismatch between different $C_S s$ in the pipeline structure can cause folding of the harmonics of $F_S/5$ into the passband. But any signal around the harmonics is filtered before folding back, and in practice this non-ideal effect is too small to be observed [3].

2.3.7 In-band noise

The output noise of the proposed filter has three main contributors which are the noise of the input Gm-block, the noise of the feedback Gm-block, and the noise of the passive switched capacitor network.

Due to the antialiasing property at the input stage of the filter, the thermal noise components of the input Gm-block and the feedback Gm-block get attenuated around kF_S frequencies. Thus, the fold back effects of these noise sources can be ignored in the following analysis. Also, since the bandwidth of the filter is much

less than the sampling rate, the in-band input referred noise of the filter can be approximated using the simplified model shown in Fig. 2.14. A single ended architecture is assumed in this model for simplicity. In this figure, $\overline{V_{n,1}^2}$ and $\overline{V_{n,2}^2}$ are the input referred noise voltage of the input Gm-block and the feedback Gm-block respectively. Also, $\overline{V_{n,3}^2}$ is the output referred noise voltage of the passive switched capacitor network. The values of the noise voltages $\overline{V_{n,1}^2}$ and $\overline{V_{n,2}^2}$ can be found based on their respective circuit topologies. Also, the in-band value of $\overline{V_{n,3}^2}$ is $4kT/(C_S F_S)$ [3].

The $H(z)$ is the transfer function of the passive switch capacitor block and is given by

$$H(z) = (\frac{1-\alpha_i}{1-\alpha_i z^{-1}})^4 \tag{2.19}$$

where α_i is given in (2.7). The G_1 and G_2 values are given by

$$G_1 = \frac{G_{M,IN}}{F_S C_S} \tag{2.20}$$

$$G_2 = \frac{G_{M,FB}}{F_S C_S} \tag{2.21}$$

Since the noise sources are uncorrelated, the in-band input referred noise voltage $\overline{V_{n,in,in-band}^2}$ can be found by adding the power of each noise source. Since at in-band $H(z) \approx 1$, $\overline{V_{n,in,in-band}^2}$ can be approximated by

$$\overline{V^2_{n,in,in-band}} = \overline{V^2_{n,1}} + (\frac{G_2}{G_1})^2\overline{V^2_{n,2}} + (\frac{1}{G_1})^2\overline{V^2_{n,3}} \tag{2.22}$$

Assuming G_1 is much higher than G_2, the input referred in-band noise is dominated by input Gm-block.

2.4 Integrated circuit implementation

The proposed filter shown in Fig. 2.6 was implemented in a pseudo-differential architecture, and fabricated in a 180 nm CMOS technology. The integrated filter includes the Gm-blocks, clock circuitry, capacitor banks and switches. Also, for measurement purposes, analog buffers were used to isolate the chip internal nodes from the outside. The designs of these blocks are discussed in this section.

The input Gm-block ($G_{M,IN}$) was implemented using an inverter-based topology, shown in Fig. 2.15(a). Inverter-based Gm-blocks have several advantages. They scale well with technology and they are capable of operating with low supply voltages. Also, as shown in [38], inverter-based Gm-blocks offer good linearity when the NMOS and PMOS transistors are sized properly (for square-law transistors). Specifically, by making the output load of the block much less than the r_{out} of the transistors, the linearity can be improved. In this design, the transistor lengths in the $G_{M,IN}$ block have been chosen many times of the minimum length allowed in the technology. This makes the transistor characteristics close to the square law, and increases the r_{out} of the transistors. To provide the proper bias voltages for the transistors, switched-capacitor level shifters were used. The level

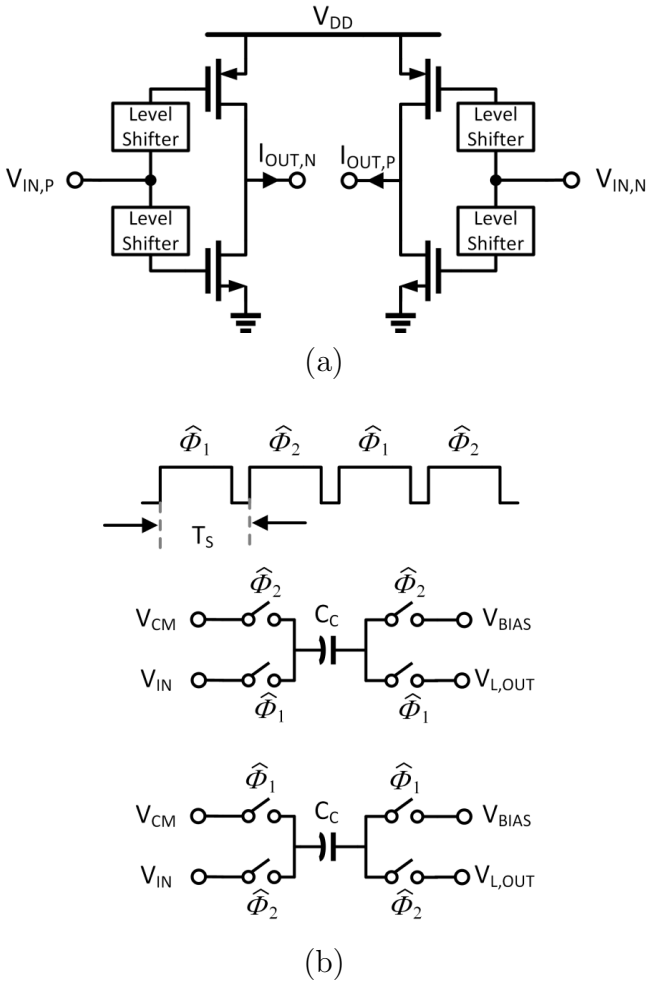


Figure 2.15: (a) Inverter-based Gm-block, (b) switched capacitor level shifter.

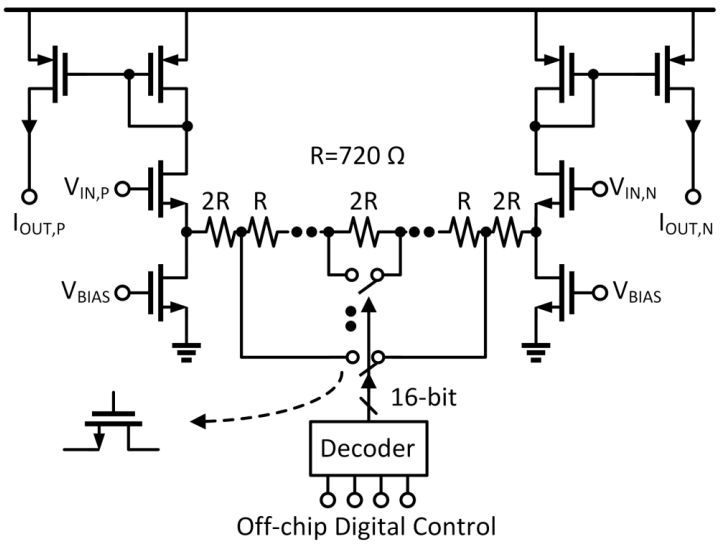


Figure 2.16: $G_{M,FB}$ circuit implementation.

shifter block is shown in Fig. 2.15(b). During clock phase ϕ_1 one of the coupling capacitors C_C is charged to the desired bias voltage, while the other capacitor is connected between the input voltage and the gate of the transistor. During clock phase ϕ_2 the roles are interchanged. MIM capacitors are used in the level shifters. The capacitors C_C should be much larger than the gate capacitances of the transistors, to reduce the input voltage drop at the gate of the transistors. C_C was chosen to be 1 pF in this design.

The feedback Gm-block was implemented using a source degenerated differential pair, as shown in Fig. 2.16. This block feeds back from the output node V_4 to the node V_1. To control the value of $G_{M,FB}$, a tunable resistor is used at the source of transistors. Polysilicon resistors were used here. By using a decoder, the value of the source resistor, and thus $G_{M,FB}$, can be controlled off-chip. To

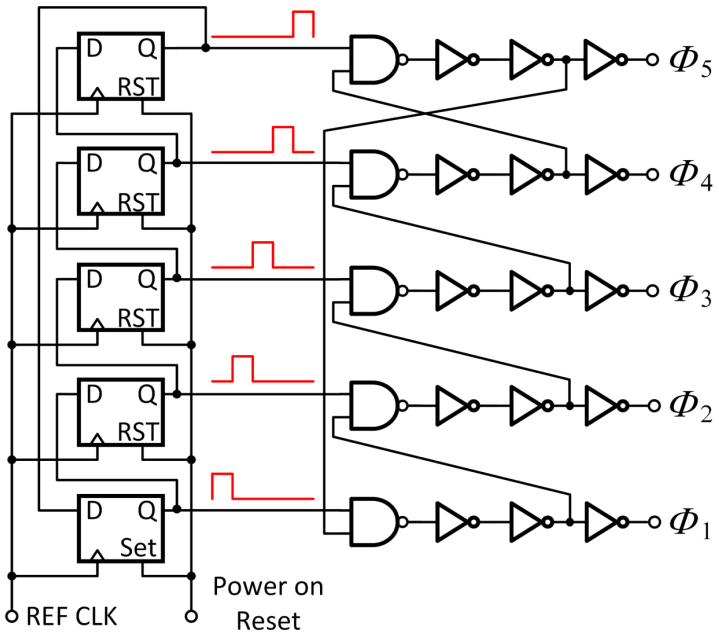


Figure 2.17: Clock phase generator block [6].

get the proper transfer function, the $G_{M,FB}$ block should provide a non-reciprocal path from V_4 to V_1 in Fig. 2.6. If the V_1 signal leaks back to V_4 through the $G_{M,FB}$ block, the stop-band rejection of the filter gets degraded. In this design, a current mirror is used in the $G_{M,FB}$ block to reduce the signal feed-forward leak from V_1 to V_4.

The history capacitors C_Hs and sampling capacitors C_Ss are implemented using MIM capacitors. The C_H values range form 1 pF to 68.5 pF, digitally selectable by a 4-bit control signal. The C_S capacitors range from 0.5 pF to 4 pF, digitally selectable by a 3-bit control. To adjust the filters 3-dB cut-off frequency, C_S and $G_{M,FB}$ are kept fixed while C_H is changed. This way, the gain and linearity of

the filter remain unchanged. To change the sampling rate while keeping the DC gain constant, C_H and $G_{M,FB}$ are kept fixed while C_S is changed inversely to the sampling frequency. For example, if the sampling rate is doubled, C_S should be halved. The switches are implemented using transmission gates. The NMOS and PMOS switches are sized equally to minimize the clock feedthrough and charge injection. The switches are sized such that the settling time constant of the signals are 7-times smaller than the clock pulse width for the fastest sampling rate. To minimize the on-resistance of these switches, low V_{th} transistors are used. With this design consideration, signals settlings are similar to step-like settling.

Fig. 2.17 shows the waveform generator block used to generate the non-overlapping clock phases ϕ_{1-5}. At power-on the true single phase clocked (TSPC) DFFs outputs are set to 10000. After that, at each rising edge of REF CLK the code is circularly shifted by one bit. The delay of the NAND gates and the two following inverters sets the non-overlap time. Similar networks used to generate the phases for the level shifters in the input Gm-block.

For measurement purposes, and to keep the chip internal signals isolated from outside, two analog buffers are also implemented. A low-noise source follower (SF) buffer is used for noise measurements. Also, a pseudo-differential opamp in unity-gain configuration is used to measure the frequency response and linearity.

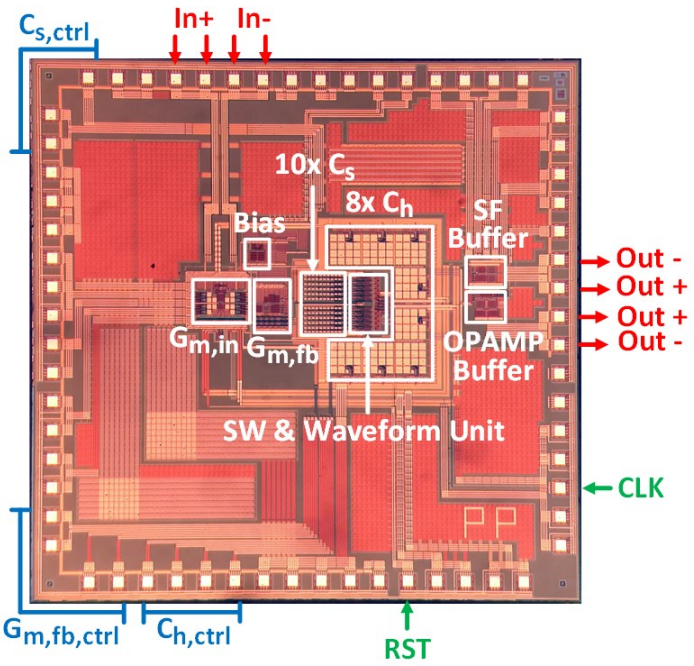


Figure 2.18: Chip micrograph of the proposed filter implemented in 1P4M 180 nm CMOS technology. Die size is 4 × 4 mm.

2.5 Measurement results

The proposed filter was implemented in a 1P4M 180 nm CMOS technology with an active area of 2.9 mm^2. The chip micrograph is shown in Fig. 2.18.

A test setup was realized on a printed circuit board (PCB) for measurements. The input and output signal paths on PCB are designed as follow. The input signal is converted to differential form using a Balun transformer. The secondary terminals of the transformer are terminated by a 50 Ω resistor, and connected to the input signal pins of the chip. As mentioned earlier, to measure the output

Table 2.4: Performance summary and comparison with the-state-of-the-art

	This work	**ISSCC'13 [2]**	**VLSI'16 [13]**	**JSSC'17 [9]**	**VLSI'17 [17]**	**JSSC'11 [1]**	**JSSC'10 [27]**
Topology	Charge sampling	Charge sampling	Source follower	Active-RC/Active Gm-RC	Voltage Sampling	Gm-C	Gm-C
Type	Complex-poles @ 300 MS/s	Real-poles @ 800 MS/s	Complex-poles (Chebyshev)	Complex-poles (Butterworth)	Complex-poles (Butterworth) @ 160 MS/s	Complex-poles (Butterworth)	Complex-poles (Butterworth)
Technology	180 nm	65 nm	180 nm	180 nm	130 nm	90 nm	90 nm
Order	4^{th}	7^{th}	4^{th}	4^{th}	3^{rd}	6^{th}	4^{th}
VDD (V)	1.8	1.2	1.35	1.8	1.2	1.0	2.5
Power (mW)	4.3	1.98	0.62	12.6	0.15	4.35	1.25
3-dB BW (MHz)	0.49-13.3	0.4-30	30.8	22.5	0.54	8.1-13.5	2.8
Gain (dB)	17.6	9.3	0	0.5	N.A	-2.7	15
Max stopband rejection (dB)	>100	> 100	76	54	40	90	55
In-band / Out-of-band OIP3 (dBm)	28.7* / 32.63†	31 / 21	29.1	22	N.A	19	25
In-band / Out-of-band OIP2 (dBm)	46.7* / 73.48‡	64.3 / 69.3	55.4	N.A	N.A	49.2	N.A
$P_{1dB,out}$ (dBm)	12.93	10	8.6	N.A	N.A	3.9	N.A
IRN (nV/$\sqrt{}$Hz)	6.54§	4.57	22.8	18.3	23.3	75	22.6
SFDR (dB)	67.9	68	67.1	59.8	91.7	54.3	58
1% HD3 DR (dB)	74.9	81	71	N.A	N.A	63	67
Area (mm^2)	2.9	0.42	0.1	0.35	0.06	0.239	0.5

* Input tones at 950 kHz and 1 MHz † Input tones at 10 MHz and 19 MHz ‡ Input tones at 10 MHz and 11 MHz § Averaged from 100 kHz to 4.4 MHz

signal of the LPF, two on-chip buffers are used (SF buffer and opamp buffer in Fig.2.18). Since these buffers are not designed to drive the 50 Ω input resistance of the measurement instruments, four off-chip low-noise and wideband analog buffers with unity gain are also used. These analog buffers are implemented using AD8045 chips. The output signals of the analog buffers are converted to single-ended form using a Balun transformer, and then are applied to the measurement instruments.

The performance of the filter is summarized in Table 2.4, which also compares it to that of the state-of-the-art designs. The chip consumes 4.3 mW at 300 MS/s from a 1.8 V supply. The input Gm-block and the feedback Gm-block consume

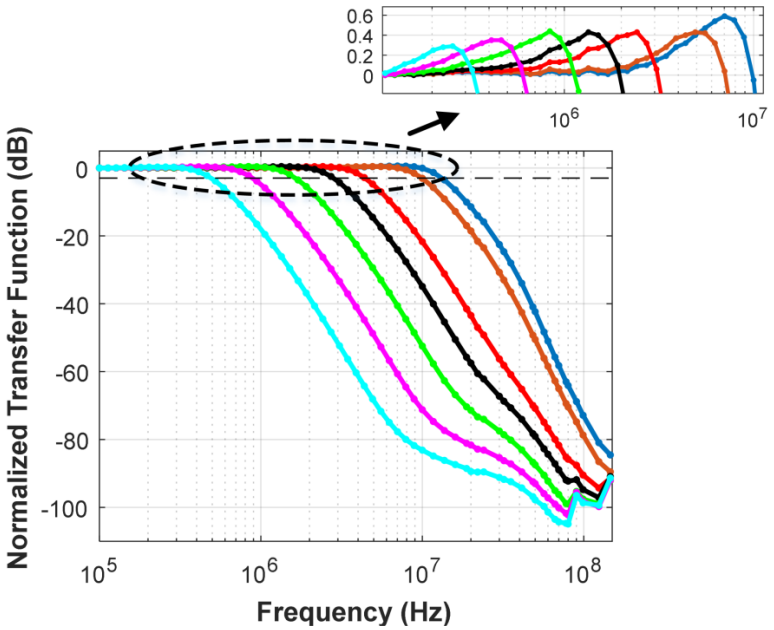


Figure 2.19: Measured BW tuning range of the filter. The filter is clocked at 300 MS/s.

0.86 mW and 1.04 mW respectively. The digital blocks consume 2.4 mW. In this design, the inverter based Gm-block and the clock generation circuit consume 76% of the total power consumption. Thus, the total power will scale by implementing the filter in smaller technology nodes.

The input-output gain response of the filter was measured by sweeping the frequency of input sinusoid signal and measuring the magnitude of the output tone using RSA6120B spectrum analyzer. The normalized input-output transfer function of the filter is plotted in Fig. 2.19. In these measurements C_S was 0.5 pF, and C_H was changed from 1 pF to 68.5 pF to tune the bandwidth form 0.49 MHz to 13.3 MHz. The filter achieves more than 100 dB maximum stopband rejection

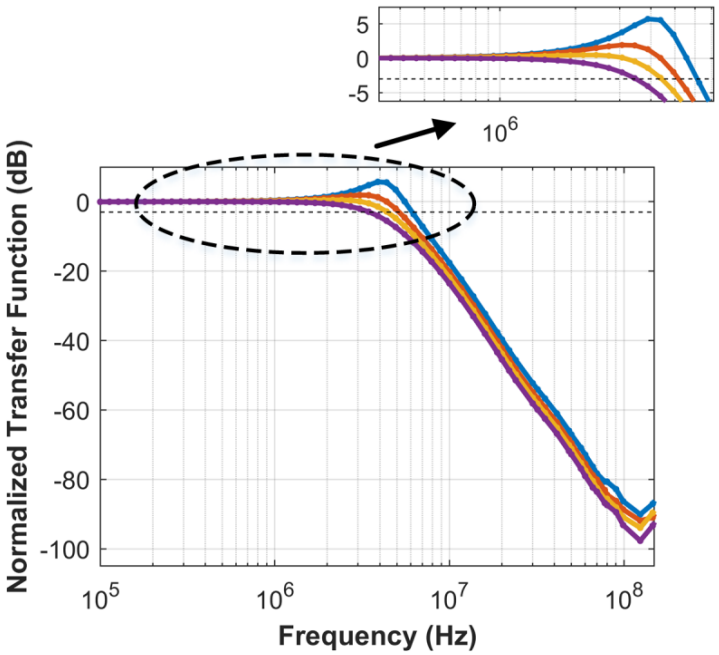


Figure 2.20: Measured transfer function of the filter for different values of $G_{M,FB}$ (F_S=300 MS/s).

for the lowest BW setting. Also, for the highest BW setting, it achieves more than 80 dB stop band rejection. The shape of the input-output transfer function remains nearly constant as the BW is changed. By changing the value of $G_{M,FB}$, the in-band peaking can be adjusted.

The value of $G_{M,FB}$ can be controlled by changing the resistor value as shown in Fig. 2.16. As mentioned earlier, by increasing the value of $G_{M,FB}$, two poles get closer to the unit circle, and therefore the in-band peaking increases. Fig. 2.20 shows the normalized input-output transfer function for different values of $G_{M,FB}$. The in-band peaking can be tuned from 0 dB to 6 dB. The sampling rate is set to 300 MS/s in this measurement.

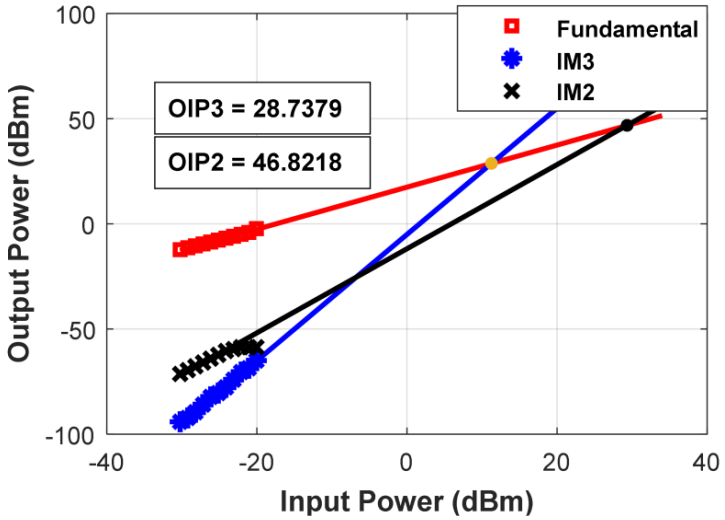


Figure 2.21: Measured OIP2 and OIP3 with respect to a 50 Ω resistor (F_S=300 MS/s).

To measure the linearity of the filter, a two-tone signal was fed to the filter, and the output was measured by an RSA6120B spectrum analyzer. For the in-band and the out-of-band linearity measurements, the BW was set to 4.4 MHz. For the in-band linearity measurements, the input tones frequencies were at 950 kHz and 1 MHz. Fig. 2.21 shows the measured output-referred 2^{nd}- and 3^{rd}-order inter-modulation products versus the input power. The measured in-band 2^{nd}-order output intercept point (OIP2) and the in-band 3^{rd}-order output intercept point (OIP3) were at 46.7 dBm and 28.7 dBm respectively. For the out-of-band OIP2 measurement, two tones at 10 MHz and 11 MHz were used. Also, for the out-of-band OIP3 measurement, two tones at 10 MHz and 19 MHz were used. The out-of-band OIP2 and OIP3 were measured at 73.48 dBm and 32.63 dBm

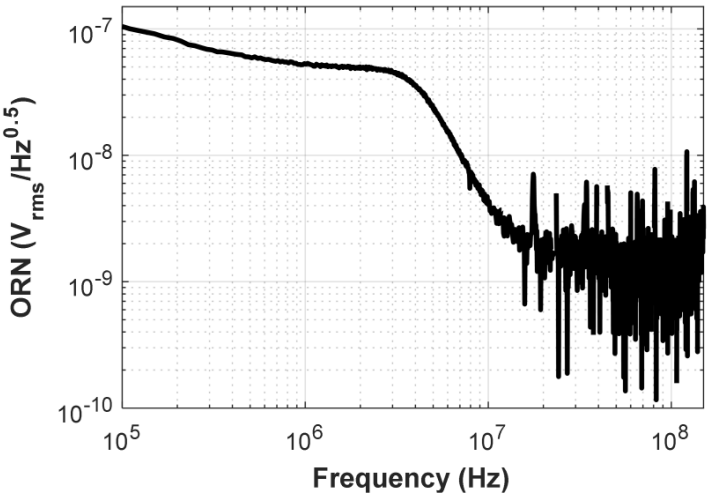


Figure 2.22: Measured noise PSD (F_S=300 MS/s).

respectively. As can be seen, the out-of-band linearity is improved compared to the in-band linearity. Since the out-of-band tones were filtered by the filter transfer function, the signals magnitudes at the input of the feedback Gm-block were less for the out-of-band tones compared to those of the in-band tones. Therefore, the nonlinearity effects of the feedback Gm-block were less for out-of-band tones.

The 1 dB output compression point ($P_{1dB,out}$) was measured based on $P_{1dB,out} = P_{1dB,in} + Gain$ 1. For the proposed filter the $P_{1dB,out}$ was found to be 12.9 dBm.

The noise power spectral density (PSD) of the filter was measured using the approach reported in [3]. The measurement was performed in two steps. In step 1, the total output noise PSD was measured. This noise included the noises of the filter, on-chip SF buffer, and off-chip buffer. In step 2, the filter was disabled, and

the noise PSDs of the buffers were measured. Since the noises of the buffers and the filter are uncorrelated, the filter noise PSD could be calculated by subtracting the buffer noise PSD from the total noise PSD.

The measured output-referred noise (ORN) PSD of the filter is shown in Fig. 2.22. The filter BW was 4.4 MHz, and it was sampling at 300 MS/s (C_S=0.5 pF and C_H=5.5 pF). As can be seen, the low frequency noise is dominated by the flicker noise of the Gm-blocks. The noise between 600 kHz to 4.4 MHz is mostly the thermal noise of the Gm-blocks, shaped by the filter transfer function. The switched-capacitor circuit noise dominates the noise at higher frequencies. There are also some spurs at higher frequencies. The amplitude of these spurs are less than -102 dBm. They may originate from the clock network, or other noise sources in the laboratory. The averaged input-referred noise (IRN) from 1 MHz to 4.4 MHz is 5.93 nV/$\sqrt{}$Hz (excluding flicker noise). Also, the average IRN from 100 kHz to 4.4 MHz is 6.54 nV/$\sqrt{}$Hz (including flicker noise). The average spot noise is in this work is slightly higher than in [3], mainly because one more active block is used in this work.

The spurious-free dynamic range (SFDR) is calculated based on the method reported in [1]. The SFDR value is 67.9 dB. To measure the 1% HD3 DR, a -9.3 dBm single tone was applied at the input with a frequency of 500 kHz. For this input signal magnitude the 3^{rd}-order harmonic was measured to be 40 dB lower than the main tone, giving a 74.9 dB dynamic range.

2.6 Conclusion

A novel switched-capacitor low-pass filter topology is presented. The selectivity of the filter is enhanced compared to a real-pole filter by implementing complex poles. Also, higher stop-band rejection is achieved for the same bandwidth. Therefore, the filter order can be reduced. These improvements were achieved by adding an active feedback path to the real-pole passive filter. The output thermal noise level and the tuning range is close to that of a real-pole filter, while the in-band loss is significantly reduced. These features make the filter suitable for high-speed, low-noise, and low-power applications.

Chapter 3: Fully Passive Noise Shaping SAR ADC

In this chapter, an opamp-free noise shaping successive-approximation register (SAR) ADC is proposed. 3^{rd}-order noise shaping is achieved by implementing a 2^{nd}-order passive filter and a passive error feedback topology. In the proposed scheme, the SAR error signals (including quantization noise, comparator thermal noise, and settling error) are subjected to 3^{rd}-order noise shaping. Therefore, the thermal noise specifications of the comparator can be relaxed. Also, since no active element is used, the proposed scheme achieves a higher power efficiency than earlier SAR ADCs.

3.1 Introduction

The successive-approximation register (SAR) analog-to-digital converter (ADC) is a popular architecture for medium-resolution medium-speed applications [39, 40, 41, 42, 43, 44]. For higher resolution applications, several design issues, including comparator thermal noise, DAC settling error and thermal noise, limit the performance of the SAR ADC. To resolve these issues, a 1^{st}-order noise shaping technique was introduced in [39] where an FIR filter and an opamp-based IIR filter were used to reduce the quantization noise and comparator thermal noise within signal band. To save power, passive filters [45, 3] can be used in the loop filter. In [7], a 1st-

order noise shaping SAR was introduced in which the loop filter is implemented using a passive integrator. In [46], a passive error feedback architecture was used to implement a 1st-order noise shaping SAR. In this Letter, a novel fully passive 3^{rd}-order noise shaping SAR ADC is proposed. Compared to prior works, higher order noise shaping is achieved by implementing a passive error feedback topology and a 2^{nd}-order passive filter. Using higher-order passive filters, higher-order noise shaping can be achieved without significant power overhead. Using the proposed scheme, the thermal noise of the comparator and DAC, and DAC settling error as well as quantization noise are filtered out of signal band.

3.2 Prior Art Review

Figure 3.1 shows the passive 1st-order noise shaping SAR ADC presented in [7].

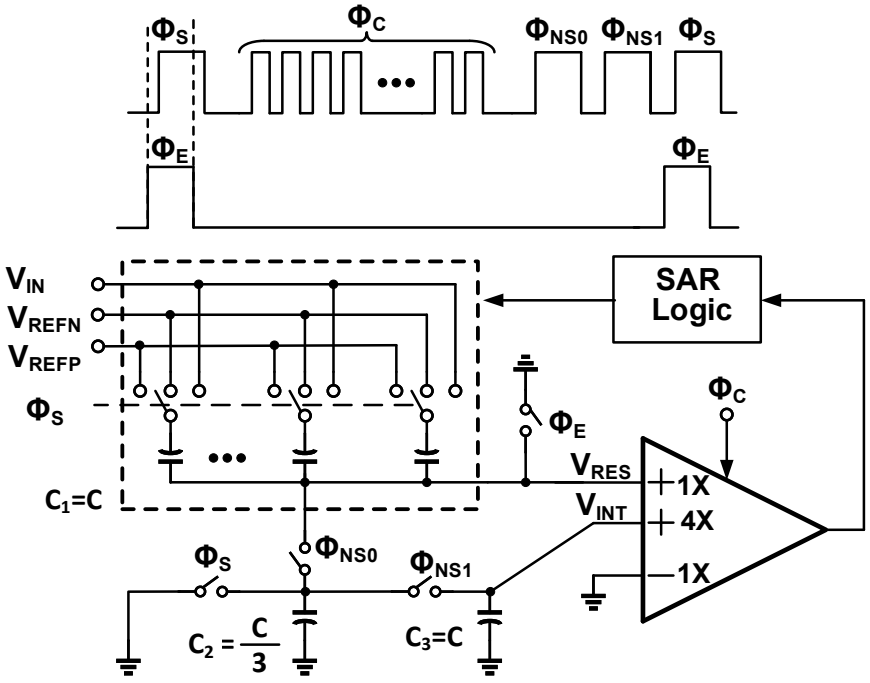


Figure 3.1: Passive noise shaping SAR ADC in [7].

During sampling phase, ϕ_S, the input signal is sampled on the bottom plate of DAC capacitors (C_1). Next, during the conversion cycle, ϕ_C, the SAR logic generates the proper controlling signals, and output bits are extracted. At the end of the conversion cycle, the residue voltage V_{RES} is stored on C_1. During the following clock phases V_{RES} is applied to a passive integrator implemented by C_2 and C_3. Next, during ϕ_{NS0}, C_2 which has been earlier reset, is connected to C_1 to sample the residue voltage. In the next phase, ϕ_{NS1}, the voltage on C_2 is passively integrated on C_3. The comparator used in this scheme needs an additional scaled input path compared to the comparator used in conventional SAR ADCs. The passive integrator output V_{INT} is connected to the second input

of comparator. The voltage V_{INT} provides an offset for comparator in the next conversion cycle. In the comparator design, the size of input differential pair of preamp stage connected to V_{INT}, is 4-times larger than the input differential pair connected to V_{RES} [7]. This way, a gain of four is implemented at the passive integrator output. By choosing the capacitor sizes shown in Figure 3.1, the signal transfer function (STF) and noise transfer function (NTF) become:

$$STF(z) = 1 \tag{3.1}$$

$$NTF(z) = 1 - 0.75z^{-1} \tag{3.2}$$

In this scheme, the quantization noise, comparator thermal noise, and DAC settling error are all filtered with a 1^{st}-order noise shaping [7]. Since the comparator thermal noise requirement is relaxed, a more power efficient comparator can be used. Moreover, since DAC settling error is shaped, a higher sampling rate can be achieved.

3.3 Proposed Scheme

The proposed noise-shaping SAR ADC is shown in Figure 3.2 [47].

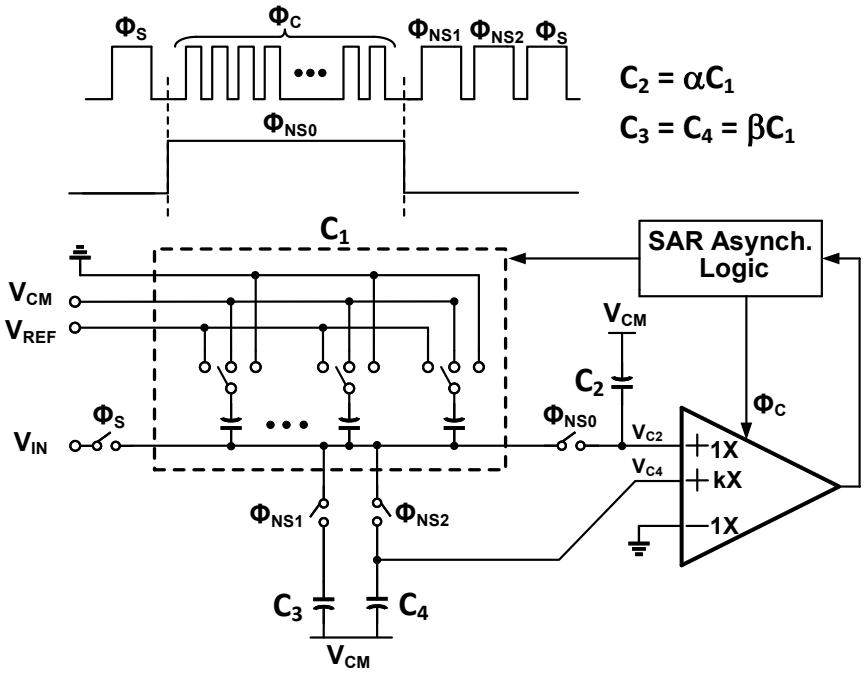


Figure 3.2: Proposed fully passive third-order noise shaping SAR ADC.

In this figure, a single-ended architecture is shown for simplicity. The actual implementation is differential. Compared to conventional SAR ADC operation, three more clock phases, $\phi_{NS0,1,2}$ are added. During the sampling phase, ϕ_S, the input signal is sampled on the DAC capacitors (C_1). After that, ϕ_{NS0} goes high and the initial voltage on C_2, which is the residue voltage from the previous conversion, is added to the sampled voltage on C_1 passively. Thus, passive error feedback is implemented. Next, the SAR conversion cycle ϕ_C begins, and the output bits are extracted while the SAR logic generates the proper controlling signals. During ϕ_C, ϕ_{NS0} remains high. At the end of ϕ_C, the residue voltage is stored on both C_1 and C_2, and ϕ_{NS0} goes low. The voltage V_{C2} stored on C_2 remains unchanged until the

next sampling phase. The voltage stored on C_1 which is equal to V_{C2}, is applied to a 2^{nd}-order passive filter which is implemented using C_3 and C_4. During ϕ_{NS1} and ϕ_{NS2}, C_1 is connected to C_3 and C_4, respectively. The V_{C4} voltage stored on C_4 provides an offset for comparator during the next conversion cycle. The comparator used in this scheme has a similar architecture to that used in [7], where the gain of input path related to V_{C4} is k. The passive filter used here is similar to the passive filter reported in [3] where C_1 is functioning as charge rotating capacitor and $C_{3,4}$ are functioning as history capacitors. This passive filter features low thermal noise level and high operating speed. By increasing the number of history capacitors, higher order of filtering can be implemented with a minimal thermal noise and power overhead. Other passive filter topologies similar to [45] could also be used here. The signal flow graph of the proposed ADC is shown in Figure 3.3.

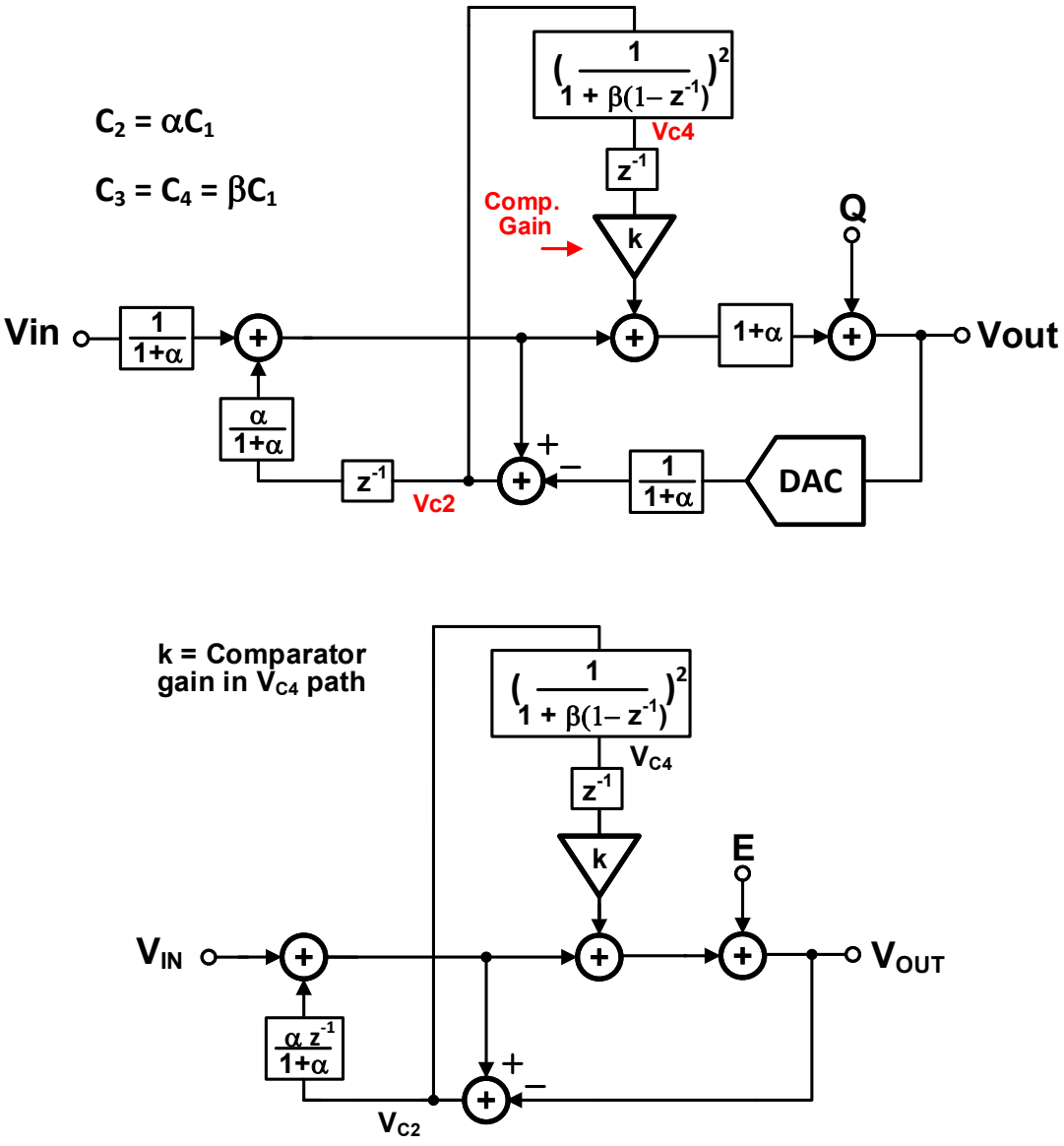


Figure 3.3: Signal flow graph of proposed architecture.

In this figure, E represents the combination of quantization noise, DAC settling

error, and DAC and comparator thermal noise. Using this signal flow graph, the STF and NTF can be found:

$$STF(z) = 1 \tag{3.3}$$

$$NTF\,(z) = \frac{\left(1 - \frac{\alpha}{1+\alpha} z^{-1}\right)\left(1 - \frac{\beta}{1+\beta} z^{-1}\right)^2}{1 + \left(\frac{k}{(\beta+1)^2} - \frac{2\beta}{1+\beta}\right) z^{-1} + \left(\frac{\beta}{1+\beta}\right)^2 z^{-2}} \tag{3.4}$$

where α and β are capacitor ratios, as shown in Figure 3.2. To keep the loop stable, the poles should be located within the unit circle in the z-plane. The stability condition of the loop is therefore:

$$-1 < k < (2\beta + 1)^2 \tag{3.5}$$

As (3.4) shows, the proposed scheme provides 3^{rd}-order noise shaping. The zero positions can be set by choosing desired values for α and β. The magnitude of NTF at zero frequency is equal to:

$$NTF\,(z = 1) = \frac{1}{(1 + \alpha)\,(1 + k)} \tag{3.6}$$

To increase the DC attenuation in the NTF, the values of α and k should be increased. Increasing α results in a larger C_2 size. The maximum value of k is determined by the stability requirements in (3.5). Using similar circuitry, it is also possible to get a 2^{nd}-order NTF by using a 1st-order passive filter with somewhat reduced performance. In Figure 3.4, the NTF of the proposed scheme is compared

with an ideal 3^{rd}-order response $NTF(z) = (1 - z^{-1})^3$, and the NTF plot of the scheme reported in [7].

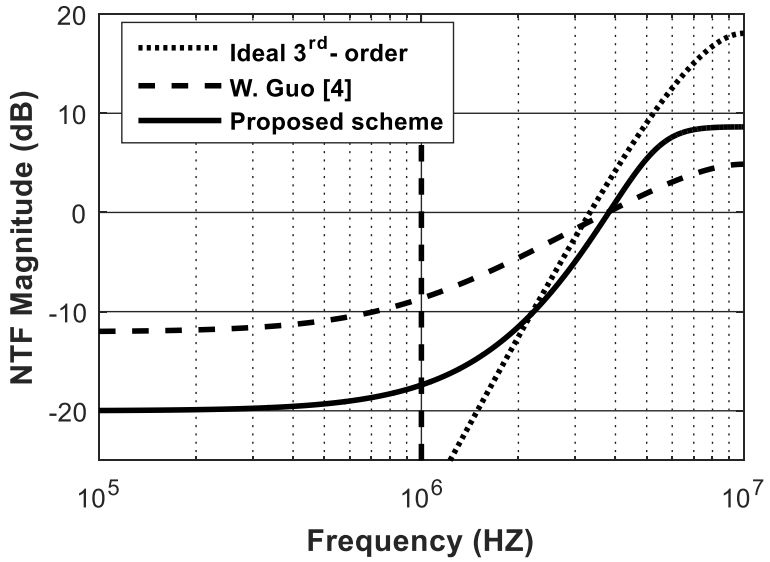


Figure 3.4: NTF comparison for $\alpha = \beta = 1$, $k = 4$, $F_S = 20$ MHz, $BW = 1$ MHz.

In this simulation, $\alpha = \beta = 1$. For a fair comparison, the comparator gain in V_{C4} path in Figure 3.2 is chosen to be same as the comparator gain in V_{INT} path in Figure 3.1 ($k = 4$). As Figure 3.4 shows, the NTF at DC is improved by 8 dB in the proposed scheme as compared to [7]. Also, by increasing the value of k, the NTF attenuation at DC can be improved even more in the proposed scheme.

3.4 Simulation Results

The 3^{rd}-order passive noise shaping SAR ADC of Figure 3.2 was designed and simulated using Cadence SPECTRE assuming a 0.18 m 1P4M CMOS technology. The SAR logic and switches were represented by macro-models. The comparator was simulated on the transistor level, but without thermal noise. The comparator had the same architecture as the one used in [7] but the gain of input path related to V_{C4} in Figure 3.2 is increased to 6 ($k = 6$). Based on (3.5), the maximum value of k for keeping the loop stable is 9. A 10-bit DAC was implemented using the merged capacitor switching (MCS) architecture [48]. The capacitors C_{1-4} were all chosen to be equal to 3 pF ($\alpha = \beta = 1$). The output power spectral density (PSD) of the proposed scheme is shown in Figure 3.5.

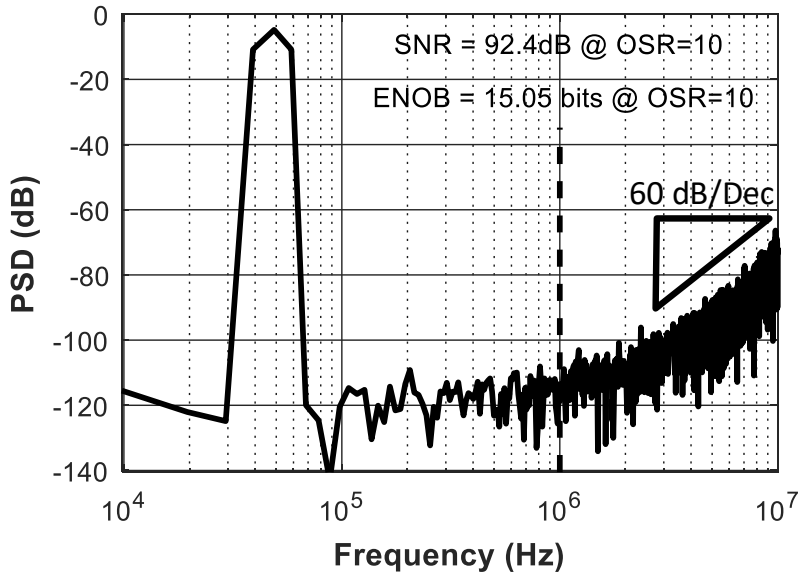


Figure 3.5: Simulated PSD with 1 dBFS input signal and $\alpha = \beta = 1$, k= 6, F_S = 20 MHz, BW = 1 MHz.

The input signal magnitude applied to the ADC is 1 dBFS, OSR is 10, and the sampling frequency is 20 MHz. The $SQNR$ and $ENOB$ of the proposed scheme within a 0 - 1 MHz band is compared to that of an ideal 3^{rd}-order noise shaping $NTF = (1 - z^{-1})^3$ and of the schemes reported in [7, 46] in Table 3.1. A 10-bit MCS DAC is used in all the architectures.

Table 3.1: $SQNR$ for different filter topologies in the 0-1 MHz band with a sampling frequency of 20 MHz

Architecture	**SQNR, dB**	**ENOB, bit**
Ideal 3^{rd}-order noise shaping	110	18
Guo [7]	82	13.3
Chen [46]	80	13
Proposed scheme	92	15.1

As the Table 3.1 shows, while the proposed scheme does not have as good $SQNR$ and $ENOB$ as an ideal 3^{rd}-order noise shaping, but it improves the $SQNR$ by 10 dB compared to [7] and by 12 dB compared to [46].

3.5 Conclusion

A novel fully passive noise shaping SAR ADC was presented. Using a 2^{nd}-order passive filter and a passive error feedback topology, 3^{rd}-order noise shaping was achieved. In the proposed scheme, DAC settling error and the thermal noise requirements of both comparator and DAC can be relaxed. This is achieved, since the quantization noise as well as the thermal noise of the comparator and DAC are shaped with the same NTF. These features make this architecture power efficient.

Chapter 4: A High-Linearity SAR-VCO MASH ADC with 2^{nd}-Order Noise Shaping

"If it's still in your mind, it is worth taking the risk"

— *Paulo Coelho*

In this section, a novel 0-2 Multi Stage Noise Shaping (MASH) analog-to-digital converter (ADC) is proposed. The first stage is implemented using a 4-bit SAR ADC. The second stage uses a VCO-based quantizer (VCOQ). Unlike earlier VCOQs which provide first-order noise shaping, the VCOQ proposed in this letter achieves second-order noise filtering. To implement this noise shaping, the quantization noise of the VCOQ is extracted as a pulse-width-modulated (PWM) signal, and it is fed back to the VCO input using a charge pump circuit. In the proposed scheme, the input signal to the VCO is small. Therefore, the linearity requirement of this block is relaxed. Also, any error related to the charge pump circuitry will be first-order shaped at the output. Simulation results confirm the second-order noise shaping of the output of the ADC, and an excellent (14-bit SNDR) performance with over-sampling ratio (OSR) of 16.

4.1 Introduction

High linearity is an important feature in analog and mixed signal circuits such as data converters [48, 49, 50, 51, 52, 53, 54, 55] and filters [56]. Time based quantizers such as voltage-controlled oscillator based quantizer (VCOQ) has been introduced as a power efficient alternative design choice for conventional voltage based quantizers [49, 57]. The VCOQ running as a voltage-to-frequency (V-to-F) converter features first order noise shaping and implicit data weighted averaging (DWA). However, the nonlinear V-to-F characteristic of the VCOQ causes distortion and limits the output signal-to-noise and distortion ratio (SNDR). In order to improve the linearity of the VCOQ, several techniques has been introduced. In [49], the VCOQ is used in a $\Delta\Sigma$ loop where the high in-band gain of the loop filter suppresses the harmonics in the signal band. However, to achieve sufficient distortion attenuation, the order of the loop filter has to be increased, which leads to higher power consumption and also stability issues. In [50], the VCOQ is used as a voltage-to-phase (V-to-P) converter. This approach solves the nonlinearity issue. However, it requires an explicit DWA. Also, to achieve higher order noise shaping, OTAs are used which are not process scaling friendly [58]. In [52], a 0-1 MASH architecture is proposed. A SAR ADC is used in the first stage, and the quantization noise of the SAR ADC is applied to a VCOQ. Since the signal amplitude at the input of the VCO is small, the VCO nonlinearity is suppressed without using OTAs. Furthermore, as long as VCOQ is not saturated and the SAR DAC has enough accuracy, any error caused by the comparator due to offset or

thermal noise would be absorbed by the VCOQ. Therefore, the comparator power consumption can be reduced [52]. However, the order of noise shaping is limited to one. In this letter, a new hybrid SAR-VCOQ is proposed, in which all the good features of [52] are kept, while the noise shaping is improved to second order.

4.2 Proposed Structure

Figure 4.1 shows the proposed 0-2 SAR-VCOQ MASH ADC architecture [59]. In this figure, a single-ended architecture is shown, but the actual implementation is differential. The ADC operates in three phases. During sampling phase ϕ_S, the input signal is sampled on the capacitors in the SAR DAC. Next, during the SAR conversion phase $\phi_{C,SAR}$, the sampled input signal is quantized by the SAR ADC. At the end of this phase, the SAR quantization error (E_{Q1}) appears across the SAR DAC. During the VCOQ conversion phase $\phi_{C,VCOQ}$, the E_{Q1} is applied to the VCOQ. The outputs of the SAR ADC and VCOQ are applied to the two noise cancelation filters NCF1,2. The outputs of NCF1,2 are added to generate the final output of the ADC (OUT).

The VCOQ consists of a VCO, a counter, a quantization noise extraction block, and an FIR filter ($1 - z^{-1}$). The VCO quantization noise extraction block consists of a SR latch, and a charge-pump circuit. The VCOQ ADC implements second order noise shaping. This is achieved by extracting the quantization noise of the counter (E_{Q2}) in the time domain, and feeding it back to the VCO input.

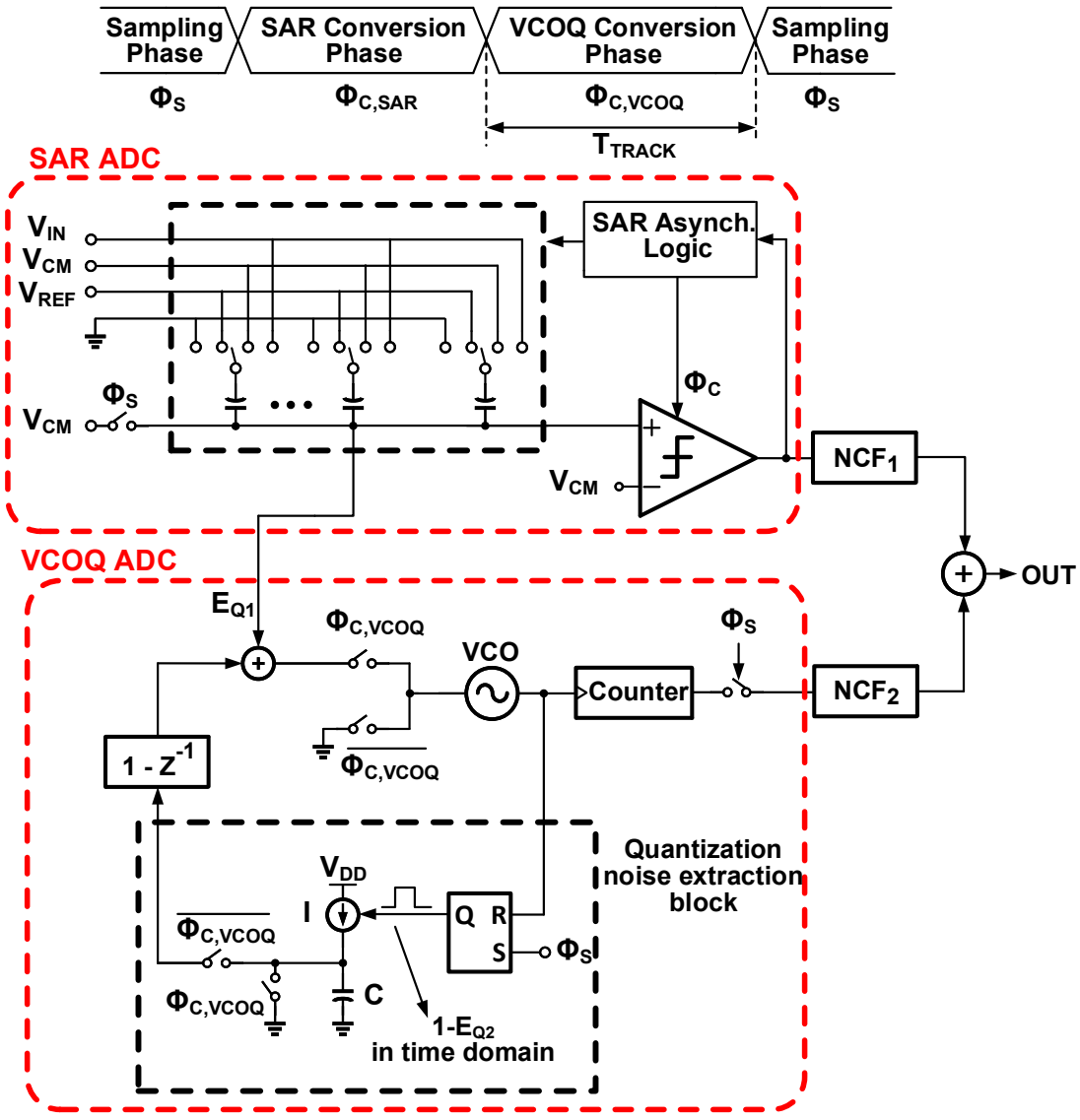


Figure 4.1: The proposed 0-2 SAR-VCOQ MASH $\Delta\Sigma$ ADC.

The counter quantizes the VCO output phase. The counter output increases by one unit for each rising edge at the VCO output, which is equivalent to 2π

phase increase. In other words, the counter is counting the number of 2π phase increase of the VCO output signal. The VCO output phase is continuous, while the counter output code has discrete values. The quantization noise that is added by counter E_{Q2}, is in the range of [0 1]. If the last rising edge at the VCO output is very close to the ϕ_S rising edge, then $E_{Q2} \approx 0$, and if the last rising edge at the VCO output happens much prior to the rising edge of ϕ_S, then $E_{Q2} \approx 1$. To extract the value of E_{Q2}, we need to calculate how much the VCO output phase has increased from the last rising edge at VCO output to the rising edge of ϕ_S. This is the amount of phase increase in the VCO output phase, which has not been added to the counter output code. The extraction of the E_{Q2} can be explained using the timing diagram shown in Figure 4.2 [53].

During $\phi_{C,VCOQ}$ which lasts T_{TRACK}, the SAR quantization noise E_{Q1}, is applied to the VCO input. When the sampling phase ϕ_S starts, the VCO input is connected to the common mode voltage. In this phase, the VCO is oscillating at free running frequency (F_{FR}). The period of the VCO output signal is T_{FR}. As it is reported in [53], since the VCO oscillation frequency is not signal dependent when the VCO input is connected to common mode voltage, the $1 - E_{Q2}$ can be extracted in time domain by measuring the time distance between the rising edge of ϕ_S and the first rising edge of VCO output. This can be implemented easily using a SR latch, as it is shown in Figure 4.1. As it is shown in Figure 4.2, the pulse width of the extracted pulse is $T_{FR}T_{EQ2}[n]$ where T_{EQ2} is the representation of E_{Q2} in time domain and is in the range of [0 TFR]. Therefore, $1 - E_{Q2}$ is extracted as a pulse width modulated (PWM) signal.

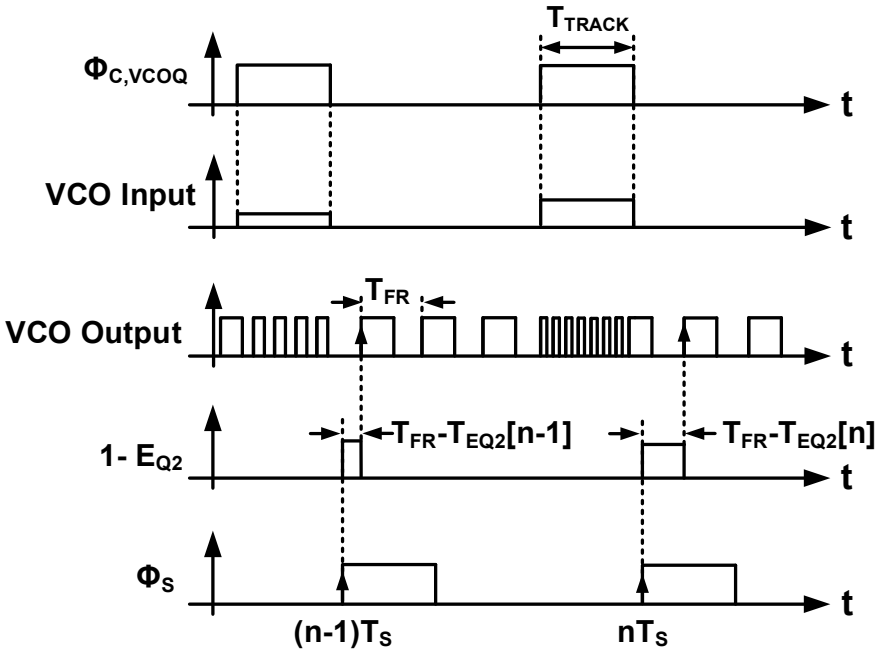


Figure 4.2: Timing diagram of the proposed ADC during ϕ_S and $\phi_{C,VCOQ}$.

In the proposed scheme in Figure 4.1, the PWM pulse is applied to a charge pump circuit to convert the pulse width to voltage. The value of the current source used in the charge pump circuit is

$$I_{CH} = \frac{C_{CH}}{K_{VCO} T_{TRACK} T_{FR}} \tag{4.1}$$

where C_{CH}, is the value of the capacitor used in charge pump circuit. The output of charge pump is applied to a FIR filter with the transfer function of $(1 - z^{-1})$ which is implemented using switched-cap technique.

In Figure 4.3, the signal flow graph of the proposed ADC is shown.

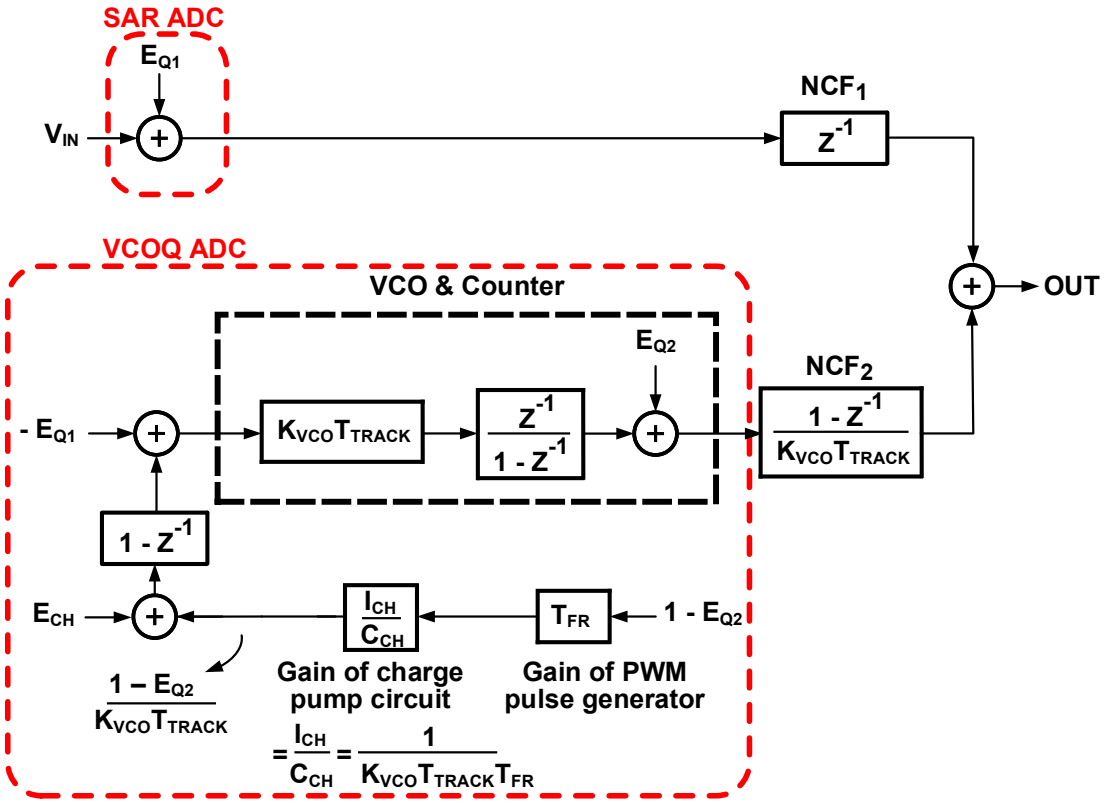


Figure 4.3: Signal flow graph of the proposed ADC in Figure 4.1.

The quantization noise of SAR ADC E_{Q1} is fed to the VCO input. The VCO is modelled as a discrete time integrator with the transfer function of $K_{VCO}T_{TRACK} \times z^{-1}/(1-z^{-1})$. The quantization noise of the counter is modelled as E_{Q2} at the VCO output. The input to the PWM generator block, which is the SR latch in Figure 4.1, is $1 - E_{Q2}$. The value of $1 - E_{Q2}$ changes from 0 to 1. The output of this block is a PWM pulse where the pulse width is $T_{FR}T_{EQ2}$. The pulse width is changing between 0 to T_{FR}. Therefore, the PWM pulse generator is modelled as

a gain stage with the gain of T_{FR}. This pulse is applied to a charge pump circuit. The charge pump circuit converts the pulse width to a voltage. The gain of this block (voltage/time) is $1/(K_{VCO}T_{TRACK}T_{FR})$. Also, the error related to charge pump and PWM generator E_{CH}, is added to the charge pump output. Using the signal flow graph shown in Figure 4.3, the ADC output OUT can be calculated as

$$OUT = z^{-1}V_{IN} + \frac{(1-z^{-1})^2}{K_{VCO}T_{TRACK}}E_{Q2} + z^{-1}(1-z^{-1})E_{CH} \tag{4.2}$$

As it can be seen, E_{Q1} is cancelled at the output and E_{Q2} is shaped by a second-order transfer function. Any error made by the charge pump and SR latch is first order shaped. Therefore, the design of SR latch and charge pump are relaxed.

4.3 Simulation Results

The 0-2 SAR-VCOQ MASH ADC of Figure 4.1 was designed and simulated using Cadence SPECTRE, assuming a $65nm$ CMOS technology using a $1V$ supply. The counters and switches and the latch in the VCOQ were represented by macro-models. The sampling frequency (F_S) was $20MHz$ and over sampling ratio (OSR) was 16. The simulated output spectral density (PSD) is shown in Figure 4.4.

In the simulation, a $4-$bit SAR ADC was used. The SAR DAC was implemented using merged capacitor switching architecture [48] with $30fF$ unit capacitors. Also, bottom plate sampling technique was employed. In the VCOQ, a $4-$bit counter was used. The rest of simulation parameters are summarized in Table 4.1.

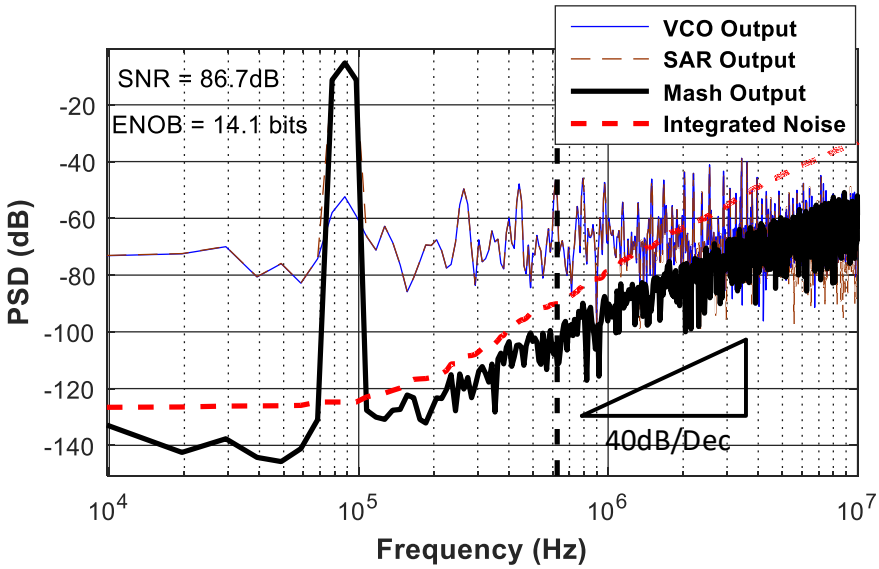


Figure 4.4: Output power spectrum density of the proposed ADC.

Table 4.1: Simulation parameters

Parameter	**Value**	**Parameter**	**Value**
K_{VCO}	$1GHz/V$	C_{CH}	$750fF$
F_{FR}	$155MHz$	I_{CH}	$3.7\mu A$
T_{TRACK}	$25nsec$		

As Figure 4.4 shows, second-order noise shaping is achieved at the output. The performance of the proposed ADC is compared to the architecture reported in [52] in Table 4.2. Although in the architecture reported in [52] multi-phase VCOQ is used, in the simulation results reported in Table 4.2, a counter-based VCOQ is

assumed to make it a fair comparison. For this simulation, same number of bits are used in the SAR ADC. Also, same VCO and same number of counter levels are used. The proposed ADC has higher SQNR due to its higher-order noise shaping. Also, compared to the approach introduced in [53], the proposed scheme in this letter needs one less counter and one less VCO, which reduces the complexity of design for the same order of noise shaping.

Table 4.2: Simulation parameters

Architecture	F_S	OSR	**Output** $SQNR$
ADC reported in [52]	$20MHz$	16	$73.5dB$
Proposed ADC	$20MHz$	16	$86.7dB$

4.4 Conclusion

A new 0-2 SAR-VCOQ MASH ADC was presented. A $4-$bit SAR ADC was used to implement the first stage, and a VCOQ was used in the second stage. The VCOQ proposed in this letter achieved second-order noise shaping, by extracting the quantization noise of VCOQ in the time domain as a PWM pulse, and feeding it back to the VCO input using a charge pump. Simulation results show superior performance of the proposed ADC over previously reported converters.

Chapter 5: Conclusion

> "Every ending is creating the space and opening for an amazing new beginning."
>
> — *Bryant McGill*

In recent years, with the broad growth of portable computers and smartphones market, there is an increasing demand for higher data rate wireless networks. This requires power efficient transceivers with wide bandwidth and sufficient dynamic range, linearity and bit-error-rate. Filters and data converters are among key building blocks in communication systems. In this dissertation, a novel switched-capacitor filter and two ADC configurations have been presented which are power efficient and digital scaling friendly. In this section a brief summary of the proposed scheme and future works are presented.

5.1 Summary

In chapter 1, a brief introduction to important design parameters in the filter design along with few of filter applications are presented.

In chapter 2, a novel switched-capacitor low-pass filter topology is presented. The selectivity of the filter is enhanced compared to a real-pole filter by imple-

menting complex poles. Also, higher stop-band rejection is achieved for the same bandwidth. Therefore, the filter order can be reduced. These improvements were achieved by adding an active feedback path to the real-pole passive filter. The output thermal noise level and the tuning range is close to that of a real-pole filter, while the in-band loss is significantly reduced. These features make the filter suitable for high-speed, low-noise, and low-power applications.

In chapter 3, an opamp-free noise shaping SAR ADC is presented. Third-order noise shaping is achieved by implementing a second-order passive filter and a passive error feedback topology. In the proposed scheme, the SAR error signals (including quantization noise, comparator thermal noise, DAC thermal noise and settling error) are subjected to third-order noise shaping. Therefore, the thermal noise specifications of the comparator can be relaxed. Also, since no active element is used, the proposed scheme achieves a higher power efficiency than earlier SAR ADCs.

In chapter 4, a new 0-2 SAR-VCOQ MASH ADC is presented. A 4-bit SAR ADC is used to implement the first stage, and a VCOQ is used in the second stage. The VCOQ proposed here achieved second-order noise shaping, by extracting the quantization noise of VCOQ in the time domain as a PWM pulse, and feeding it back to the VCO input using a charge pump. Simulation results show superior performance of the proposed ADC over previously reported converters.

5.2 Future Works

As it is discussed in chapter 2, by adding a feedback path to a real-pole filter the selectivity of the filter improves, and the in-band loss is reduced. The other approach to improve the selectivity, is by adding out-of-band zeros to the filter input-output transfer function. This can be implemented by adding feed-forward paths to the filter. The feed-forward paths can be implemented actively or passively.

In the proposed filter in chapter 2, the inverter based Gm-block and the clock generation circuit consume 76% of the total power consumption. Thus, the total power will scale by implementing the filter in smaller technology nodes.

In chapters 3 and chapter 4 two promising power efficient ADC architectures are presented which don't have silicon proof. Having silicon proofs of these ADC will be a better indicator of the performance of the proposed schemes.

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