AN ABSTRACT OF THE DISSERTATION OF

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Title: Ring Amplifier Optimized for High Resolution Analog-to-Digital Converter Applications

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Un-Ku Moon

In recent years, SAR ADCs have been shown to acheive faster conversion times and improved power efficiencies due to their simple building blocks that are digital in nature and scale favorably with technology. High resolution ADCs with stringent noise requirement has led to the adoption of hybrid ADC architectures such as the two-step SAR. The two-step SAR ADC, also known as pipelined SAR ADC, combine the concepts of SAR and Pipeline ADC architecture where a residue amplifier provides a critical amplification step. An amplifier architecture well suited for residue amplification known as Ring Amplifier (RAMP) has enabled power efficient two-step SAR ADCs. However, RAMP based ADCs with greater than 14 bits of resolution has not been attempted in previous literature. In this work, the design and measurement of a high-resolution two-step SAR ADC utilizing an enhanced RAMP is demonstrated. Additional circuit techniques are introduced that contribute to the energy-efficiency of the ADC. The ADC implemented in 0.18μm technology achieves a DR of 95dB and a Schreier FOM better than 180dB at both 2MS/s and 15MS/s.

Ring Amplifier Optimized for High Resolution Analog-to-Digital Converter Applications

by

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Chapter 1: Introduction

1.1 Overview

High resolution Analog-to-Digital Converters (ADC) find their way in many applications that require high accuracy such as medical imaging and instrumentation [1]. From the various ADC architectures, Successive-Approximation Register (SAR) ADCs have gained popularity in recent years due to their power efficiency and reduced complexity. This interest in research has further advanced the performance of SAR ADCs. [2]. Fig. 1.1 shows the basic building blocks of a SAR ADC. The SAR ADC comprises of a capacitive DAC, a single comparator that determines polarity of DAC top plate, and finally digital logic that sends controls to the DAC to perform reference voltage switching based on the comparator decision. Initially, the differential input signal, $inp - inn$, is sampled onto the DAC capacitance which spans a voltage range of $\pm FS$ where FS is the full scale differential input to the ADC. Following the sampling phase, the input is presented at the input of the comparator. The concept of successive approximation is that the loop made up of "DAC-comparator-logic-reference switch" attempts to search for the region where the input signal is. For the first decision, the comparator resolves whether the input is in the lower (0 to $-FS$) or upper (0 to FS) half of the input range. For example, if the input is in the upper half, the DAC switching performed re-centers the voltage at input of comparator such that

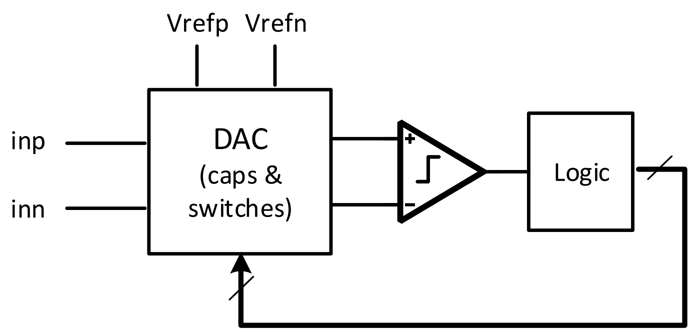

Figure 1.1: Basic SAR block diagram

the comparator determines in the next decision in which half is the input signal of the upper half of the input range. This process goes on for as many times as needed, each time, providing further information about the exact region where the input is, and hence, bits of resolution.

The process described above is usually referred to as the binary search where each decision cycle gives one additional bit of information. High resolution ADCs require more decisions to resolve higher number of bits. Each decision resolves a smaller region of the input range than the previous one. A qualitative illustration is shown in top of Fig. 1.2 for a Binary SAR, where the conversion starts with the most significant bit (MSB) decisions from the left and sequentially to the least significant bit (LSB) decisions on the right. The residue level refers to the signal magnitude present at the top plate of the DAC, i.e., input of the comparator, after each DAC switching operation. Typical input signal FS ranges in the order of few volts. As the conversion progresses, the residue level reduces and for resolutions of 16 to 20 bits,

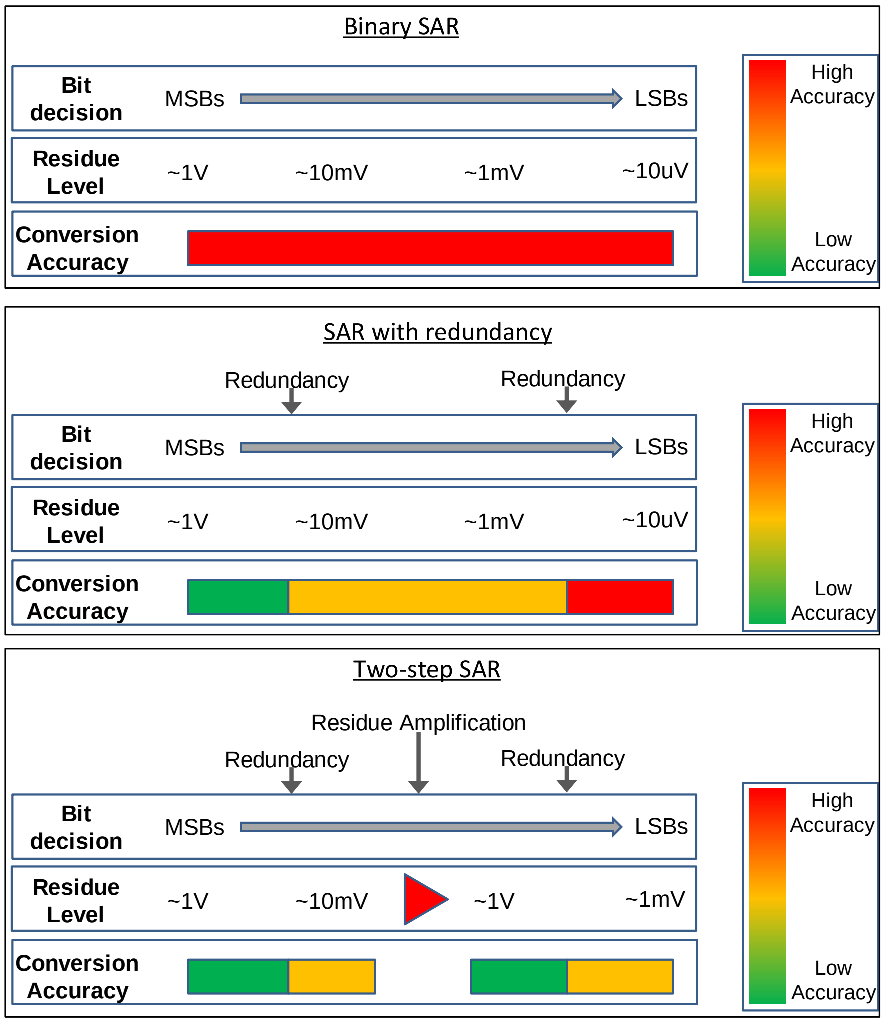

Figure 1.2: SAR residue levels and conversion accuracy comparison

the residue level reaches the μV level. The conversion accuracy of each cycle must be on the order of the entire ADC accuracy required for all bit decisions, referred to in Fig. 1.2 with color scale. This accuracy refers to the noise performance of the comparator, DAC reference voltage noise and DAC settling prior to new decisions. Hence, for high resolution ADCs, low noise requirement for the comparators lead to higher power consumption as well as longer resolving time due to DAC settling requirements.

Due to this stringent requirements, the SAR ADC has evolved in recent years to include concepts such as redundancy as well as hybrid architectures that include residue amplification to relieve the noise requirements from the comparator. The middle section of Fig. 1.2 shows the case where redundancy is introduced at intermediate points. Redundancy allows for inaccuracies to occur in earlier decisions that are absorbed by latter decisions. The magnitude of these inaccuracies are proportional to the amount of redundancy inserted. In general the later the redundancy is inserted, the smaller the amount of error that is accommodated. Hence, the LSB decisions still require full accuracy of the ADC.

The two-step SAR hybrid architecture [3] introduces residue amplification at an intermediate point that enlarges the residue level for the LSB decisions, completely alleviating the noise requirement of the latter decisions. As shown in Fig. 1.2, the entire conversion process is greatly relaxed in accuracy for a two-step SAR. Yet, the residue amplification step itself becomes the most critical step for the entire conversion process and requires special attention. This is due to the fact that any non-idealities such as noise or non-linearity introduced during the residue amplification step is

	Hershberg VLSI 2012 [4]	Hershberg VLSI 2013 [5]	Lim JSSC Oct 2015 [6]	Lim JSSC Dec 2015 [7]	Lim VLSI 2017 [8]	Lagos VLSI 2017 [9, 10]	Lagos CICC 2018 [11, 12]
SNDR (dB)	62	76	58	72	73	58	57
Fs (MS/s)	30	20	100	50	100	600	1000
Power (mW)	2.6	3	2.5	1	2.3	14	25

Table 1.1: Ring Amplifier based ADCs in previous literature

unrecoverable. Yet, the advantages obtained such as relaxing the requirements of SAR operation and speed improvement obtained due to pipelining the conversion process makes the two-step SAR architecture worthwhile.

1.2 Motivation

While amplifier structures are well established in literature [13, 14], a recent architecture that is particularly well suited for discrete-time switched-capacitor amplification known as Ring Amplifier (RAMP) has been shown to obtain good power efficiency and fast settling performance [15]. Nevertheless, all RAMP-based ADCs in literature, shown in Table 1.1, are limited to medium resolution with dynamic range (DR) less than 80dB. In this research, a Ring Amplifier structure named "Dual-Deadzone Ring Amplifier" is introduced that is optimized to meet the various requirements needed for a high resolution two-step SAR ADC with DR greater than 90dB.

1.3 Organization of Dissertation

Chapter 2 discusses the architectural choices and system level design flow. Chapter 3 covers the circuit level implementation of the two-step SAR ADC with emphasis on the Ring Amplifier. Finally, chapter 4 provides the measurement results and the dissertation concludes with chapter 5 where a comparison with the state-of-art is presented.

Chapter 2: Architecture and System Design

The initial phases of any design involves architectural design choices and noise budgeting. Such system analysis and the reasoning behind architectural decisions made for the two-step SAR ADC of this research will be discussed in this chapter.

2.1 System Analysis

Fig. 2.1 represents the basic configuration of the two-step SAR where two SAR ADCs are separated by a residue amplifier (RA). The timing diagram in the figure describes the phases of operation. SAR1 resolves M bits following the input sampling phase. Then the RA amplifies the residue with a gain of $RAgain$ at the end of SAR1 conversion onto SAR2 input. At the end of RA, SAR1 can return to sampling the input signal while SAR2, also referred to as the backend ADC, resolves the amplified residue and resolves an addition N bits. The pipelining allows for the ADC to run at a faster rate compared to a single stage SAR ADC where all M+N bits are resolved prior to returning to input sampling. An addition reset phase is shown for SAR1 prior to sampling which helps avoid non-linearity due to residue kickback onto the input signal.

The partitioning of required resolution in each stage is subject to multiple factors. For a good design, both SAR1 and SAR2 timing should have equal level of difficulty.

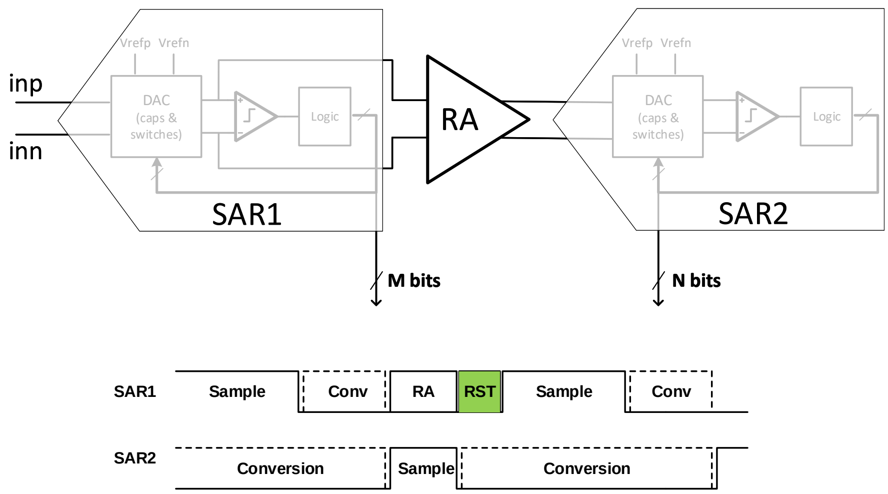

Figure 2.1: Two-step SAR basic block diagram with timing diagram

But SAR1 timing has more phases compared to SAR2, i.e., RA and RST phase, hence, it is expected to resolve more bits in SAR2. On the other hand, the number of bits in SAR1 is chosen such that a sufficiently high gain in RA is made possible which relaxes the thermal noise requirement of the backend ADC.

The target resolution for this ADC is 16 bits. That translates to Signal-to-Noise Ratio (SNR) of 98dB. The factors that contribute to the SNR of the ADC are:

- **Input sampling thermal noise** is set by the size of the input sampling capacitor which simultaneously is the switched-capacitor DAC of SAR1. This is usually referred to as " kT/C " noise.

- **Residue amplification phase thermal noise** is defined by the network formed of the SAR1 DAC and switches, the residue amplifier and the SAR2 input sampling capacitor and switches. Depending on the mentioned network,

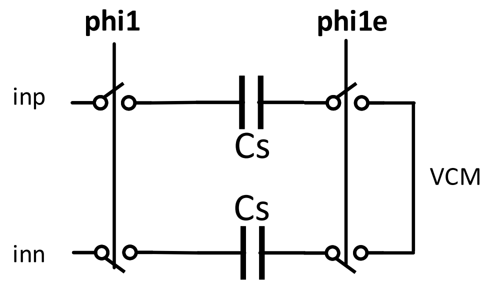

Figure 2.2: Input sampling capacitor network

this noise can usually be represented in a form that is proportional to " kT/C " noise.

- **SAR2 comparator thermal noise** is referred to the ADC input by dividing the comparator noise by the RAgain.
- **ADC quantization noise** is the errors due to the LSB size of the ADC. For a B-bit ADC, the quantization noise power is represented as $\Delta^2/12$ where Δ is $FS/2^B$.

The first step in any ADC design is to roughly estimate the noise budget for each of the major contributions for a given noise target. The SNR equation in dB can be shown as:

$$SNR = 10\log\frac{FS^2/2}{P_n}$$

where P_n is the sum of all noise power contributors. The technology used allows for 3.3V devices. Hence, to maximize SNR, the input FS is defined as 3.3V. Therefore, the differential input spans $\pm 3.3V$. The noise budget of a power efficient ADC should be thermal noise limited. This means that the major contribution to the noise power is a result of thermal noise and a small portion dedicated to quantization noise. Additionally, SAR2 comparator thermal noise is relaxed due to RAgain, hence, can be considered as a minor contributor. This leaves us with input sampling and residue amplification thermal noise power. The differential input sampling network is shown in Fig. 2.2. The total thermal noise of this network can be expressed as $2kT/C_s$. A rough estimate of thermal noise due to amplification phase is an additional $2kT/C_s$. Allocating 80% of the noise budget to $4kT/C_s$ and targeting a 16-bit SNR yields C_s of 21pF. In this design, a C_s of 16pF was chosen due to a miscalculation in the early design phase. This leads to a reduced SNR of 96.8dB. Quantization noise is allocated 10%, which yields a signal-to-quantization noise (SQNR) of 108dB, i.e., approximately 18 bits of resolution. The 18 bits of resolution can be described as the backend ADC effective number of bits (ENOB) improved by RAgain. Hence, for a 16x, 32x, 64x or 128x RAgain, the backend SQNR would require to be 14, 13, 12 or 11 bits respectively for an effective 18 bit quantization. In this design, an effective RAgain of 128x is chosen, requiring 11bits of SQNR from the backend and an ideal 7 bit resolution from first stage. In next section, the partitioning of the SAR1 and SAR2 DAC is discussed in more detail.

2.2 System Design

Fig. 2.3 shows the full architecture block diagram of two-step SAR ADC presented in this work. The raw bits of SAR1 and SAR2 are 9 and 13 bits respectively, yielding

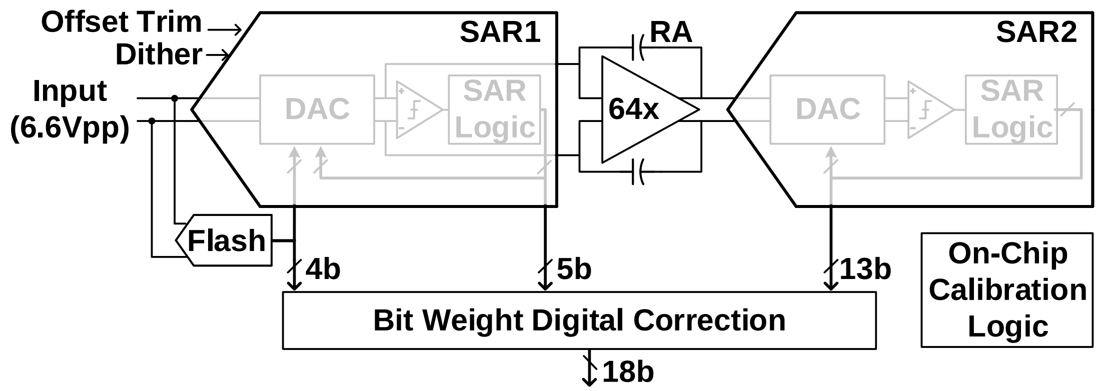

Figure 2.3: Complete two-step SAR block diagram

after redundancy 7 and 11 bits of SQNR respectively. A physical RAgain of 64x is implemented but an effective gain of 128x is realized through SAR2 DAC structure as will be shown later. A coarse Flash ADC resolves 4 MSBs of SAR1 allowing for even faster SAR1 conversion [16] . That is followed by 5 more bits of SAR operation to achieve the 9 raw bits of SAR1. Raw bits of both SAR1 and SAR2 are then captured externally and recombined to provide the reconstructed 18 bit ADC output. On-chip logic provides the means to measure the individual bit weights to account for any capacitive mismatch. Additionally, offset trim is introduced to trim out the offset of SAR1 comparator. Finally, dithering provides a means to randomize the residue propagating into the RA and the backend ADC which breaks the correlation between the input signal and the SAR1 residue. A strongly correlated residue results in harmonic distortion due to non-idealities of backend ADC. When dithered, the correlation is broken and the non-idealities result in an increased noise floor instead of spurious tones in the final ADC spectrum.

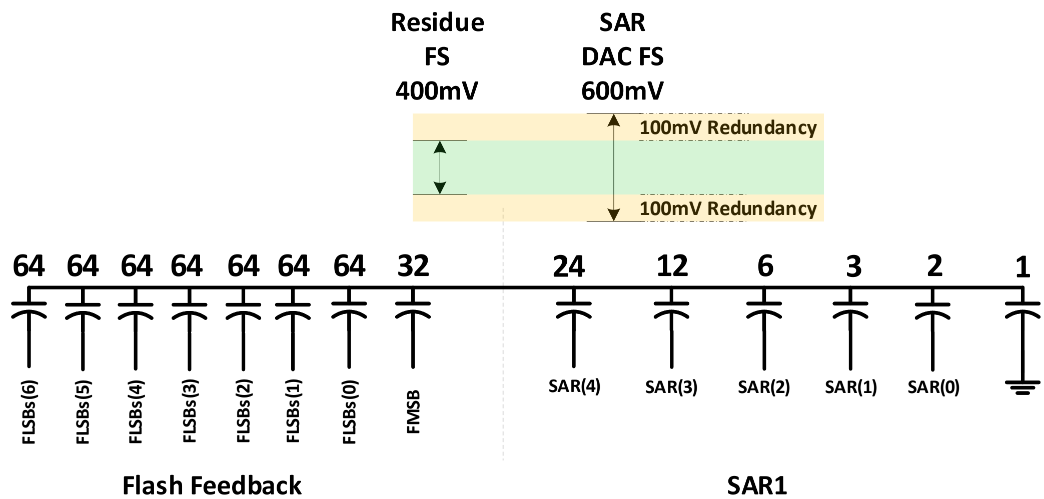

Figure 2.4: Single-ended representation of SAR1 DAC partitioning

2.2.1 SAR1 DAC

Fig. 2.4 shows the partitioning implementation of SAR1 DAC. The SAR1 DAC utilizes the well-known Merged Capacitor Switching (MCS) technique [17]. Flash feedback section comprises of 4 MSBs equivalent of a 512-unit DAC, i.e., 15 x 32-units, that utilizes three-level switching similar to [18]. Unlike MCS, three-level switching allows the utilization of common-mode voltage (VCM) as a valid feedback in addition to the typical two reference voltages, VREFP and VREFN. In [18], the MSB feedback is applied sequentially. For this work, the feedback is applied simultaneously once the Flash 4 bit decisions are made which results in improved reference loading and power savings.

In this technique, as shown in Fig. 2.5, input signals close to mid-scale input

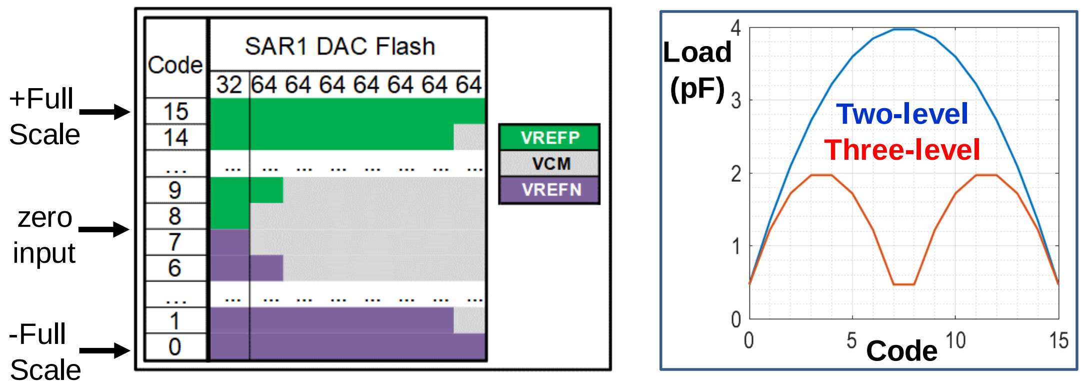

Figure 2.5: Three-level switching for Flash feedback section of SAR1 DAC

impose minimal loading on the reference voltages as they are mostly switched to VCM. Additionally, the peak loading seen at any code is half of that seen by two-level MCS simultaneous switching. Due to the nature of three-level switching, the transition from one code to the next requires switching two 32-unit capacitors from VCM to VREP/N. Hence, Every two 32-unit capacitors are paired into a single 64-unit capacitor, creating 7 64-units and a single 32-unit capacitor that switches with MSB decision. At the end of flash feedback, the full scale input of ± 3.3V is reduced to a residue of $\pm 3.3/16$V, i.e., $+/-200$mV. Three factors introduce errors between the flash and SAR ADC, namely, the Flash comparator offsets, the Flash resistor ladder and capacitors mismatch and finally the input sampling instance skew between Flash and SAR DAC. To account for these errors, redundancy is introduced between Flash and SAR section of the DAC [19–23]. The SAR section of the DAC for a non-redundant SAR should have been [16-8-4-2-1-1]. Instead, as shown in Fig. 2.4, adding 1.5x range for the SAR section results in units being [24-12-6-3-1.5-1.5]. Adding an

	STG1 DAC											
	Cunit: 32fF	Flash Section	SAR Section							Offset Trim		
	CAP Units	15 x 32	24	8	4	6	3	2	1	4	2	1
Phases	Sample	Input Signal			0	4b Dither				0		
	Conv	Flash 4 bits	b5	b4		b3	b2	b1	0	3b Offset		
	RA	Flash 4 bits	b5	b4		b3	b2	b1	0	0		

Figure 2.6: SAR1 DAC switching during different phases

addition redundancy in the last SAR decision leads to final shown units of [24-12-6-3-2-1]. This translates to a redundancy range of 100mV in either direction. In other words, all errors between Flash and SAR within 100mV can be tolerated without issue. The final redundancy provides 3mV of redundancy for errors due to any comparator noise or DAC settling of SAR operation of SAR1. The residue at the end of SAR1 operation translates to $\pm 3.3x2/512$,i.e., ± 12.9mV, equivalent to the residue of an 8 bit conversion.

Fig. 2.6 shows the SAR1 DAC units switching during the different phases of operation. During sampling, 512-units are tracking the input signal while a portion of the LSBs are simultaneously sampling a 4-bit dither sequence [24]. Due to the unit capacitor values, the dither generates 12 unique levels out of the 4-bit sequence. The dither references are scaled down with an odd fraction of $VREFP - VREFN$,

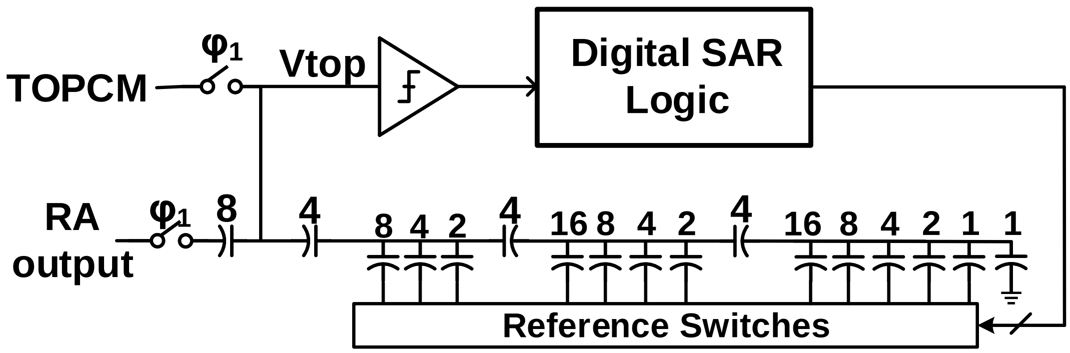

Figure 2.7: SAR2 DAC partitioning

11/24, resulting in a dither full-scale of ±35mV. This eats into the ±100mV redundancy range mentioned earlier, leaving ±65mV of redundancy between Flash and SAR section. This odd fraction allows the dither to still maintain 12 distinct levels inside the ±12.9mV of residue at end of SAR1 conversion [25]. At end of sampling, Flash feedback is applied as well as a 3-bit offset code. This offset is intended to tune out SAR1 comparator offset. It utilizes single-ended and three-level switching to have an effective tuning step of 3mV. Therefore, the comparator offset can be tuned to ±1.5mV. After SAR1 conversion, the offset code is returned to 0 (VCM) during residue amplification where the remaining residue on SAR1 DAC is transferred and amplified onto SAR2 input sampling capacitors.

2.2.2 SAR2 DAC

The residue amplifier implements an RAgain of 64x. For the residue range of ±12.9mV at the end of SAR1 conversion, this translates to ±0.825V at the input of SAR2. If

SAR2 were to utilize the same 3.3V references, this means that the RA output utilizes a mere 25% of SAR2 input range. One solution is to utilize a smaller reference voltage for SAR2. But in practice, it is costly in terms of power as well as footprint to provide multiple references to an ADC. The SAR2 DAC shown in Fig. 2.7 shares the same 3.3V references with SAR1 and scales the reference using bridged-capacitors [1]. As shown, the input is sampled onto an 8-unit capacitor. The DAC which consists of three bridged-capacitor sub-DACs of 3, 4 and 6 bits respectively is connected to the comparator through a 4-unit capacitor. Therefore the DAC feedback is scaled down by a factor of half. Therefore, the input range of ± 0.825V utilizes 50% of the input range of SAR2, leaving abundant headroom for residual errors in SAR1 operation. This scaling down of reference voltage can be interpreted as an extra 2x digital gain, making the digital gain from DAC1 top plate to SAR2 top plate an effective 128x. The three bridged-capacitor sub-DACs of SAR2 have redundancy in between them. For a non-redundant DAC, the optimum value for the bridge capacitor would have been slightly over 2-unit capacitors. Instead, by utilizing 4-units for the bridge capacitor, redundancy of approximately an entire bit is added between each sub-DAC. Therefore, out of the 13 bit decisions, 2 bits are overlapping, yielding an effective 11 bits of quantization. In practise, the parasitics at each sub-DAC attenuate the redundancy range, resulting in increased resolution at the cost of lost redundancy.

2.3 Calibration

So far, the effect of capacitor mismatch on ADC accuracy was not covered. For medium resolution ADCs, capacitor mismatch is usually handled by sizing up the unit capacitor until the maximum allowed mismatch is achieved, since mismatch reduces with increased unit area. For high resolution ADCs, however, following the same procedure would result in unrealistic capacitor values leading to excessively huge area and power consumption. Therefore, the common approach in recent literature [26–31] is to provide a means to measure the capacitor units mismatch and correct for them in the digital domain. While calibration techniques is not the scope of this work, on-chip programmability is required in order to configure the ADC in a calibration mode where individual capacitor weights are measured.

Fig. 2.8 illustrates the method utilized for calibration. The figure represents all the capacitor DAC units of both SAR1 and SAR2 combined. The idea of the calibration method is based on the assumption that the last 6 LSBs in SAR2 are sufficiently linear to operate as a backend calibration ADC whose mismatches are negligible. This is true since with good layout, 8-9 bits of matching can be achieved. Hence, the DNL of those 6 LSBs would be well below the target ADC quantization level. As shown in the top portion of the Fig. 2.8, the first significant capacitance unit after the 6 LSBs is is calibrated first. This unit is forced to have a VREFP perturbation for one ADC cycle and VREFN for the next cycle, in an alternating fashion. Simultaneously, all prior units are forced to VCM during the entire calibration process. Hence, the 6 bit LSBs are quantizing the weight of that alternating square wave. By demodulating

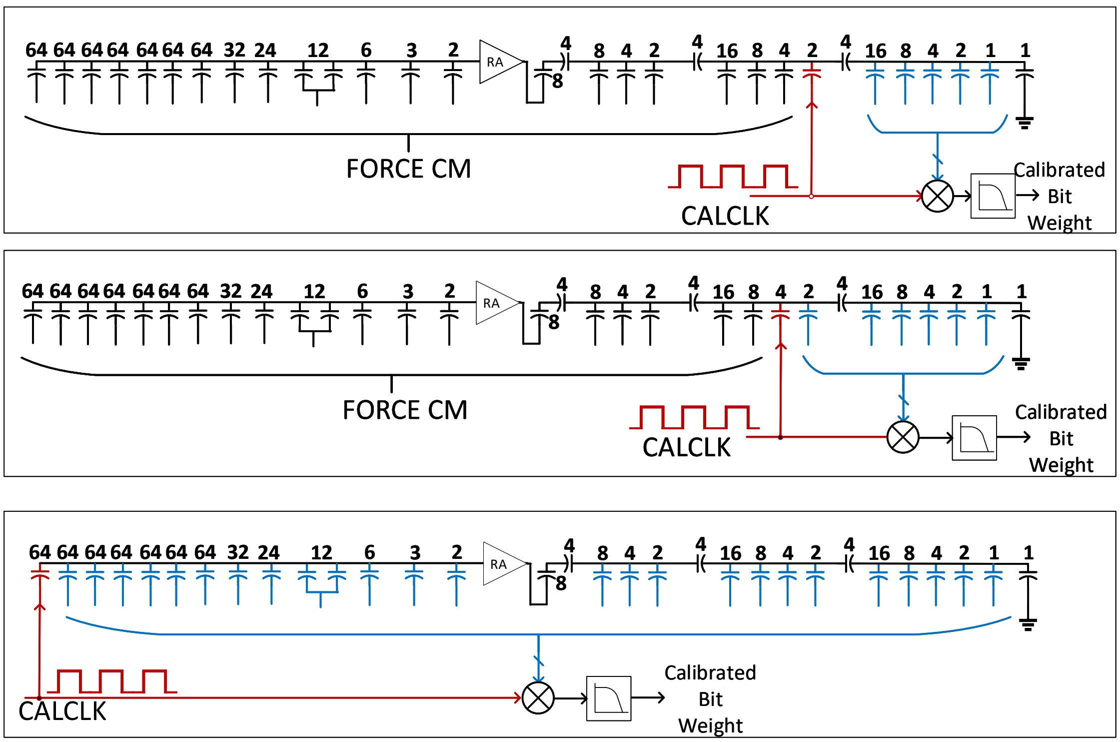

Figure 2.8: Method for DAC capacitor weights calibration

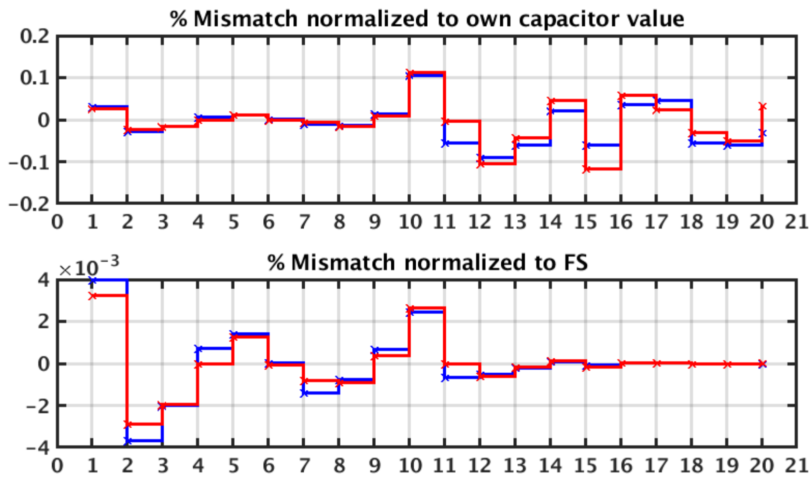

Figure 2.9: Measured mismatch in DAC capacitors

the output of those 6 bits, and averaging them, a digital word representing the weight of the alternating unit is measured. In the next step shown in the middle portion of Fig. 2.8, the calibrated unit is now added to the 6 LSBs forming a new backend calibration ADC that is used to calibrate the next significant capacitor unit towards the left. By performing this operation, all the capacitor weights are measured all the way back to the Flash section of SAR1 DAC. Those weights are stored and multiplied by their respective bits during reconstruction of the ADC output. Fig. 2.9 shows the measured capacitor weights for two chips normalized to their own capacitor value in the top graph and normalized to the ADC FS in the bottom curve. From the top graph, we can deduce that the 64-unit capacitors of Flash ADC achieves a matching on the order of ±0.25%, i.e., approximately 11 bits of matching while the backend units are on to order of 9 bits matching. But looking at the bottom curve, we realize that even with the better matching of MSBs, their larger absolute weight in compared to the LSBs, makes them have a larger mismatch percentage in terms of input signal range. It is interesting to note that both chips demonstrate similar mismatch behaviour which suggests systematic offset due to layout. In fact, during layout, very little effort was spent to ensure matching of DAC units since it was known before hand that calibration would correct sufficiently for such imperfections.

Chapter 3: Circuit Implementation

Following the system design phase in chapter 2, this chapter discusses some of the circuit implementation details with emphasis on the residue amplifier.

3.1 SAR

The SAR circuitry involves the comparator, SAR logic and reference switches. The SAR switching utilizes MCS switching and the SAR logic bit timing is asynchronous. The Logic and comparator is operated at 1.8V and levelshifters are used to interface the SAR Logic to the 3.3V reference switches. While the SAR logic implementation is conventional, for 0.18μm technology, a single 1x sized inverter loaded by it's own exhibits around 120ps of delay. In order to meet the 2ns bit cycle target for speed, 1ns was allocated to the SAR digital logic and DAC settling. Therefore, one thing worth noting here is that all SAR logic cells in the critical path of the SAR bit cycle were implemented in dynamic logic fashion.

3.2 Residue Amplifier

As discussed in chapter 1, the residue amplifier performs a noise-sensitive operation where the residue at the end of SAR1 conversion is amplified and sampled onto SAR2 for further conversion. The requirements of the residue amplifier can be listed as:

- **Accuracy** The charge transfer and amplification need to be as accurate as the entire ADC resolution. Any non-linearity introduced during the amplification directly add to the final ADC reconstructed output. While dithering helps with breaking down the harmonic distortion, such non-linearity could still limit the maximum achievable Signal-to-Noise-and-Distortion (SNDR). From the 18 bit SQNR requirement, this translates to approximates 110dB of amplifier open loop gain across the expected output swing.

- **Noise** The thermal noise sampled onto SAR2 during the amplification phase directly appear in the ADC output spectrum divided by the RA gain. Care must be taken to ensure all potential noise sources are considered. In chapter 2, noise budget of $2kT/C_s$ was allocated to the residue amplification phase.

- **Speed** The residue amplification is one of three major phases making up the ADC time period. Minimizing the RA phase allows the ADC to either allocate a larger portion for input sampling or increase the sampling rate of the ADC.

- **Power** Finally, given the previously mentioned accuracy, noise and speed requirements, the residue amplifier is expected to be a major contributor of the total power consumption.

To sum up, the residue amplifier is required to accurately transfer the charge to 18 bit accuracy in a relatively short amount of time with low noise and with minimal power consumption.

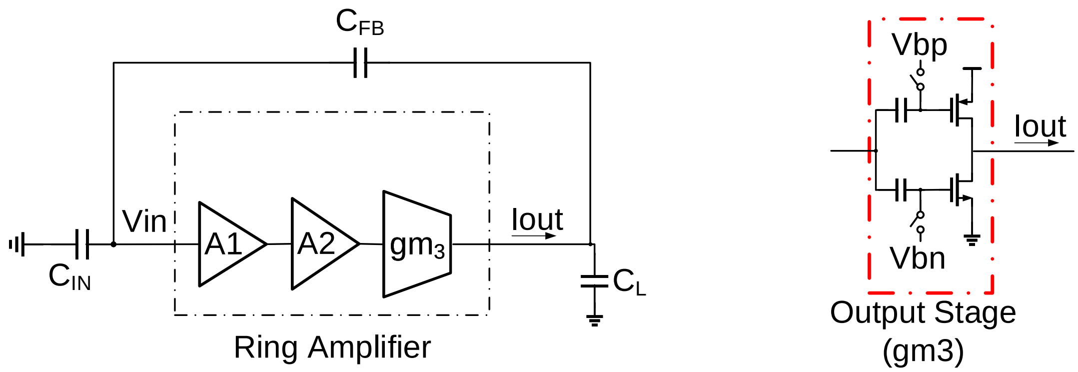

Figure 3.1: Ring Amplifier conceptual diagram and typical output stage implementation

3.2.1 Ring Amplifier

The Ring Amplifier architecture has been introduced in recent years as a power-efficient residue amplifier with moderate accuracy and fast settling [32–34]. Unlike general purpose amplifier applications, the discrete-time nature of the residue amplification phase has two unique characteristics that make the Ring Amplifier well-suited. First, the residue present at the input is static. Second, the value of the RA output at the end of RA phase is what matters. In other words, the output transients during RA phase is of no significance as long as the output reaches the desired final value at the end of RA phase.

Fig. 3.1 shows the conceptual structure of the Ring Amplifier configured in residue amplification phase, where C_{IN} represents the SAR1 DAC and C_L the input sampling capacitance of SAR2. The Ring Amplifier consists of three gain stages with the output C_L creating the dominant pole of the system. The output stage typical implementation is a push-pull output stage as shown in Fig. 3.1 where the sizing and seperate bias voltages, Vb_p and Vb_n, set the trans-conductance of the output stage, gm_3. These bias voltages are sometimes referred to seperately as the "deadzone bias", and play an important role in the dynamics of the Ring Amplifier.

It is of interest to analyze the Ring Amplifier in small-signal terms then discuss it's large signal transients. The small-signal gain-bandwidth product (GBW) in terms of gm_3 as well as the gain of the first two stages, A_1A_2, can be expressed as

$$GBW_{CL} = \frac{A_1A_2gm_3}{C_L + C_{FB} \parallel C_{IN}} \frac{C_{FB}}{C_{FB} + C_{IN}}$$

in radians, and can further be simplified as

$$GBW_{CL} = \frac{A_1A_2gm_3}{C_L(1 + \frac{C_{IN}}{C_{FB}}) + C_{IN}}$$

For noise calculations during the RA phase, a practical assumption is to assume the input referred noise of the Ring Amplifier, vn^2_{amp}, is dominated by first stage gm_1, as $\frac{4kT}{gm_1}(1 + x)$, where x represents an excess noise factor due to other noise sources in the amplifier. The noise floor at the output of the amplifier can be expressed as

$$vn^2_{out} = vn^2_{amp}(1 + A_{CL})^2$$

where $A_{CL} = \frac{C_{IN}}{C_{FB}}$. By multiplying the output noise floor by the closed loop noise bandwidth, the integrated noise at the output,$vn^2_{outintg}$, becomes

$$\begin{aligned} vn^2_{outintg} &= vn^2_{out} \times Noise\_BW\_\text{Hz} \\ &= vn^2_{out}\frac{\pi}{2}GBW_{CL}\_\text{Hz} \\ &= vn^2_{amp}(1+A_{CL})^2\frac{\pi}{2}\frac{1}{2\pi}\frac{A_1A_2gm_3}{C_L(1+A_{CL})+C_{IN}} \\ &= \frac{kT(1+A_{CL})^2}{C_{IN}+C_L(1+A_{CL})}\frac{(1+x)A_1A_2gm_3}{gm_1} \end{aligned}$$

And finally the noise referred to the input differential signal, vn^2_{inintg}, can be expressed as

$$vn^2_{inintg} = \frac{2kT}{C_{IN}+C_L(1+A_{CL})}\frac{(1+x)A_1A_2gm_3}{gm_1}$$

assuming $(1+A_{CL})/A_{CL} \approx 1$. The capacitors here represent the single-ended equivalent capacitance values. From the above noise equation, a few observations can be made. First, the noise can be expressed as a ratio of $2kT/C_{IN}$. This is useful to evaluate how much additional noise is added to the total noise due to the amplification phase. Other noise sources during amplification phase are SAR1 reference switch resistances and the SAR2 sampling switches. The former is made negligible by ensuring the RC time constant of the SAR1 DAC and reference switches are wider bandwidth than the GBW of the amplifier. For the SAR2 sampling switches, it introduces an addition $\frac{2kT}{C_L}\frac{1}{RAgain^2}$ at the input of the ADC. Due to the large RAgain, this noise is greatly attenuated.

Second, the equation of the input referred noise, vn^2_{inintg}, introduces a new ratio of $\frac{A_1A_2gm_3}{gm_1}$. The $A_1A_2gm_3$ can be referred to as the effective gm of the Ring Amplifier,

gm_{eff}. For a single-stage amplifier commonly used for SC amplification, such as the folded cascode, gm_{eff} is simply gm_1 and the noise equation is independant of gm terms. For the Ring Amplifier, this ratio requires extra attention for good noise design. For certain steady-state GBW, a certain gm_{eff} is required. In order to maintain noise performance as good as or better than a single-stage amplifier, $gm_1 \geq gm_{eff}$ is required, setting a minimum gm_1. Note that a large gm_1 implies a large current drawn in the first stage of the Ring Amplifier.

Typically the GBW requirement of the residue amplifier is derived from the settling time. However, a Ring Amplifier does not follow a conventional linear settling and can be shown to settle faster than single stage amplifiers given the same steady-state GBW. Here is where the Ring Amplifier shows improved power efficiency. Setting the steady-state GBW at a lower value than a single stage GBW, i.e. a lower gm_{eff}, power can be saved by reducing gm_1 respectively. A second important power saving featuring is that the first stage is implemented as a complimentary differential pair, which simply doubles gm_1 for the same current drawn. This advantage can be attributed to single stage amplifiers too, but severely limits their output swing. Due to the multi-stage structure of the Ring Amplifier, a small swing is expected at the first stage output.

Fig. 3.2 illustrates the large signal transients of the Ring Amplifier divided into three phases. At the start of the residue amplification phase, the residue is present at the input of the ring amplifier, V_{in}, which in turn gets amplified to a much larger value at the input of the third stage, $O2P$ and $O2N$, causing the appropriate output device to turn on strongly. This quickly charges the output capacitance, C_L, in the phase

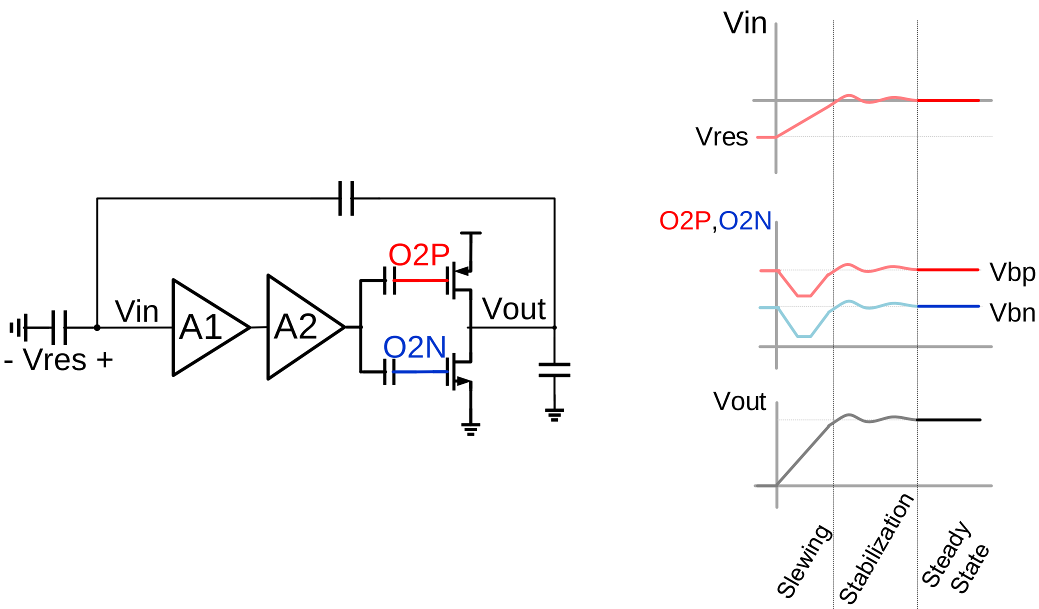

Figure 3.2: Ring Amplifier transients

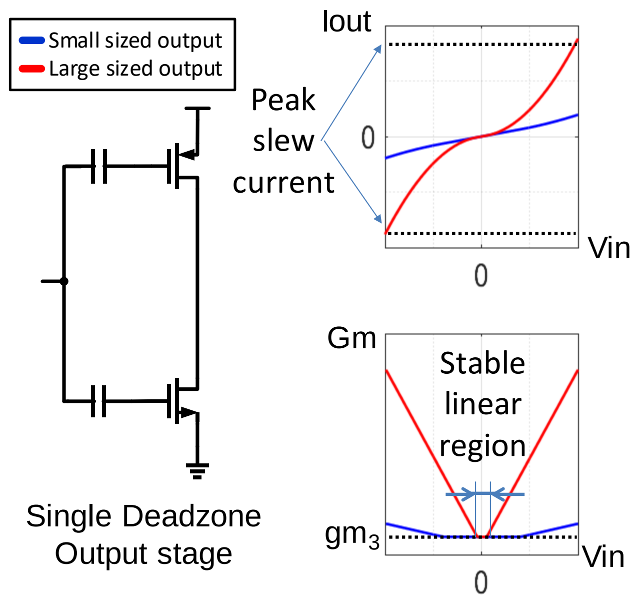

Figure 3.3: Ring Amplifier output stage sizing trade-offs

referred to as "slewing". During slewing, the output stage gm and bandwidth is much larger than that defined at steady state. During the "stabilization" phase, the output voltage approaches the final settled value and the amplifier begins to transition into the steady-state. Finally, the amplifier enters the "steady-state" phase where the small signal characteristics of the amplifier define the residue transients.

Therefore, it is desirable to have a fast slewing phase, followed by a short stabilization phase and finally a well-defined steady-state operating point for noise and settling accuracy. As discussed, to acheive a target GBW, a certain gm_{eff} and gm_3 is required. Considering the output stage shown in Fig. 3.3, we are left with only two design parameters, namely the sizing of the output devices as well as their bias voltages. Two cases are considered in Fig. 3.3 for qualitative analysis, small and large sized devices. The top and bottom curves represent the I-V characteristics and large signal gm of the output stage, respectively. As shown, the small sizing implies low peak slew currents from the I-V curves. On the positive side, the small sizing corresponds to a larger bias voltage for a given gm_3. Therefore, the gm of the output stage remains at the steady state gm value for a wide range of input indicated by the stable linear region. Such wide stable region implies a shorter stabilization phase as the amplifier locks into steady state. Additionally, the larger overdrive results in lower bias sensitivity. In contrast, utilizing large output device sizes provides for the large slew current as shown here in red. But that comes at the cost of a narrower stable region which extends the stabilization phase and causes higher bias sensitivity due to the small overdrive for a given gm_3. From the above trade-off, this work introduces a proposed output stage that overcomes such design limitation.

3.2.2 Proposed Dual-Deadzone Ring Amplifier

A "Dual-Deadzone" output stage is proposed that comprises of two branches, a large-sized branch made up of high threshold (HVT) devices and a small-sized branch made of low threshold (LVT) devices. Both branches share the same bias voltages, Vb_p and Vb_n. Fig. 3.4 illustrates the role of each branch and their combined effect. The large-sized HVT devices provide the high current during slewing. The bias voltage is set such that the HVT devices are completely turned off at steady-state, as indicated by the zero large signal gm for zero V_{IN}. On the other hand, for the same bias

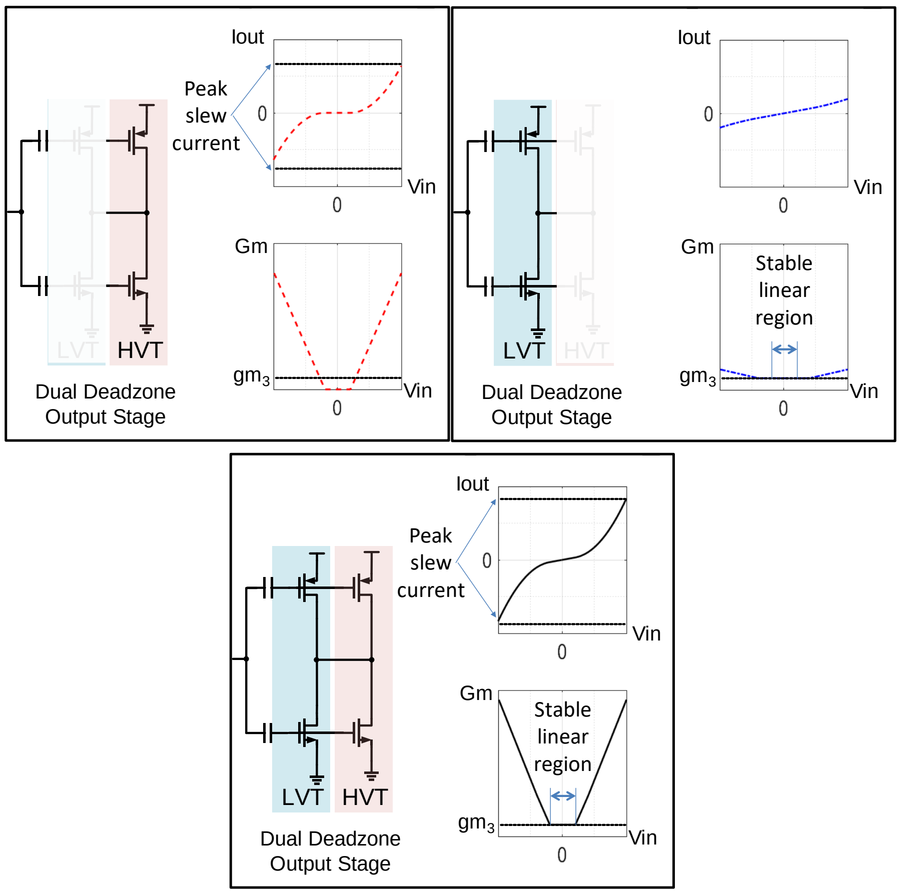

Figure 3.4: Ring Amplifier with Dual-Deadzone output stage

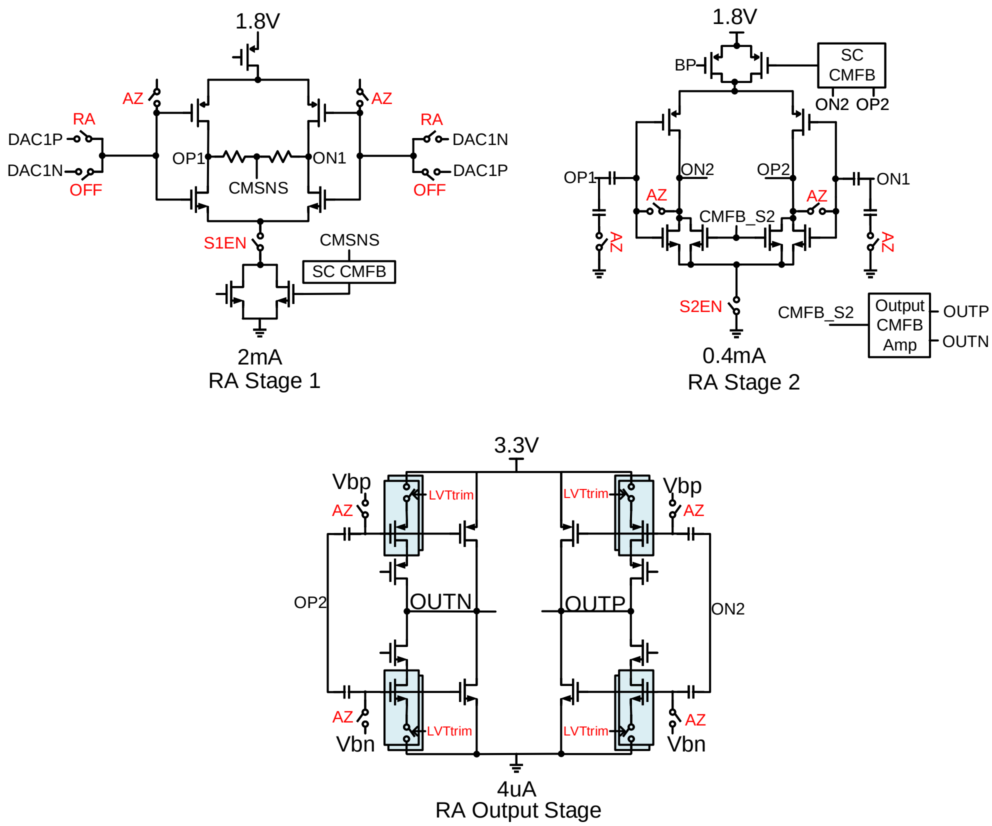

Figure 3.5: Transistor level schematics of Ring Amplifier

voltage, the small-sized LVT branch sets the gm at steady state, gm_3. Combined, the desirable properties of high slew current with shorter stabilization time and low bias sensitivity is achieved. Additionally, the LVT branch is cascoded to obtain a higher gain at steady state without compromising the peak slew current of the output stage.

3.2.3 Ring Amplifier schematics

A detailed schematic of the proposed Ring Amplifier is shown in Fig. 3.5. The first stage is comprised of a complimentary differential pair with 2mA of bias current from a 1.8V supply. Common-mode feedback (CMFB) is implemented locally for the first stage. An extra pair of OFF switches at the input provide cancellation to the differential activity at SAR1 DAC top plate. The second stage, which consumes 0.4mA from 1.8V supply, similarly consists of a complimentary differential pair with one tail current source for supply rejection and proper definition of current drawn. Global CMFB ensures that the amplifier output CM feedback is set to a desired CM level. The output CM level is fed back into the second stage through a CMFB amplifier. This CMFB loop comprises of the second stage, output stage and CMFB amplifier. The second stage presents a non-dominant pole to this loop. In order to relax the stability of the global CMFB loop, an additional local SC CMFB loop is added for the second stage amplifier. The stability is improved by presenting a reduced CM resistance at the output of second stage, extending the non-dominant pole there as well as reducing the gain and gain bandwidth of the global CMFB loop. Finally, the Dual-Deadzone output stage consumes are few μAs from a 3.3V supply. The higher supply allows for abundant swing at negligible power consumption penalty. Additionally the LVT branch is trimmable to all for programmability of gm_3.

For power reduction, the ring amplifier is powered off between amplification phases of each period. Prior to start of amplification (during SAR1 conversion), the ring amplifier turns on and utilizes auto-zeroing to set the bias voltages of the internal

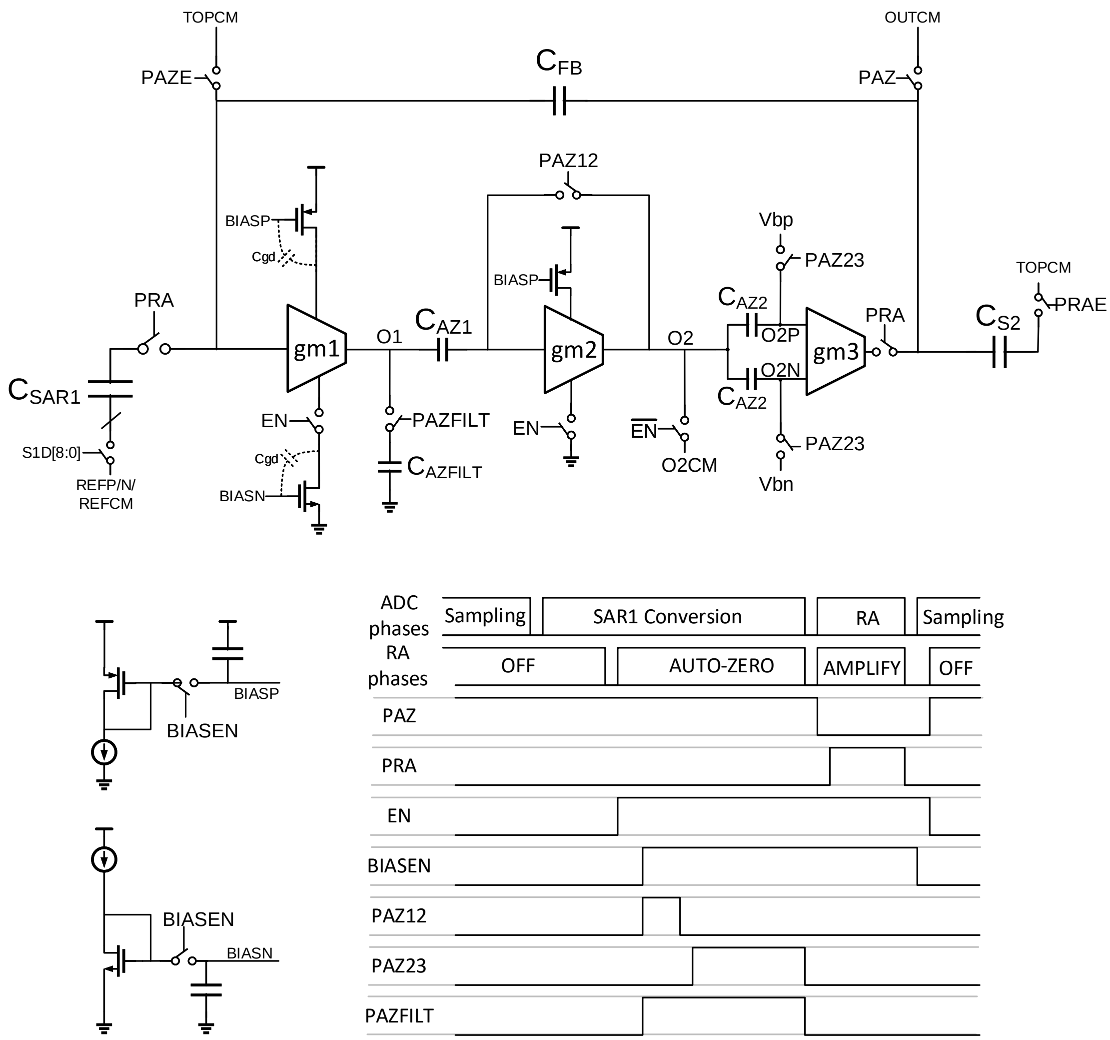

Figure 3.6: Ring Amplifier diagram showing critical switches and timing for auto-zeroing and power cycling

nodes as well as reject low frequency flicker noise. Inter-stage auto-zeroing (AZ) is favorable since it does not require the amplifier to be unity-gain stable or use large capacitors for noise/stability. Fig. 3.6 presents a simplified version of ring amplifier to illustrate the power up and auto-zeroing sequence prior to amplification. It is worth noting that the power on time of the ring amplifier consists of AZ phase and amplification phase. For power savings, it is desirable to reduce both time durations, i.e., a fast power-on plus AZ sequence followed by a fast amplification phase. Using short AZ durations implies incomplete settling across AZ capacitors. In order to achieve proper AZ, the main strategy is to ensure previous stored voltages across AZ capacitors is preserved from sample to sample. Hence, AZ settles across multiple cycles. For this strategy to work, precautions are taken to ensure AZ capacitors do not leak during power down as well as during power on sequence. Such precautions will be detailed next. First, BIASP/N provides tail current source biases for first two stages as well as the CMFB amplifier. During power-on, a large voltage step occurs at the drain of the tail current sources that feeds through the C_{gd} of those devices back onto BIASP/N. For the external bias to recharge and resettle the C_{gd}, large bias current mirror would be needed wasting unnecessary power, or allow more time for power on sequence, which again is a waste of power. Instead, a BIASEN switch shown in Fig. 3.6 disconnects the BIASP/N capacitors from the bias circuit prior to power off. As the circuit powers off and then powers on again for the next cycle, the drain voltage starts and end at the same voltage causing a net zero charge loss at BIASP/N. Therefore, the BIASEN switches are turned on with slight delay from EN signal to allow the drain nodes to resettle to their original level prior to connecting the bias current mirror. Second, AZ is delayed from EN signal to allow the internal nodes to recover on their own prior to any AZ updates. Third, AZ between first two stages (PAZ12) is performed for a short period during which AZ between second and third stage is not enabled. This allows the second stage to charge C_{AZ1} without being loaded by C_{AZ2}. Finally, it is important to carefully observe the internal nodes during power off. When first stage is disabled by EN switch on top of NMOS tail current source, the output is pulled to VDD. The CM level at O1 and the approximate input CM of stage 2 are the same. Therefore, the input to the second stage is similarly pulled to VDD, which shuts off the PMOS differential pair of the second stage. The EN switch of the second stage similarly shuts off the NMOS side, leaving the output of second stage (02) floating. The CM voltage at O2 during normal operation is $VDD/2$, while O2P/N are a mere Vgs away from their respective supply sides. If O2 is left floating and ends up drifting to VDD or GND, the voltages at O2P/N would exceed VDD or GND respectively and reverse-bias the drain-bulk junctions of the PAZ23 switches. If that was to happen, the charge across C_{AZ23} would leak during power off. Hence, to eliminate this issue, a replica bias voltage (O2CM) is connected to O2 during power off to hold the voltage at O2 in place.

3.2.4 On-chip Settling Characterization

Transient simulations of the settling of the proposed Ring Amplifier for full scale residue at input is shown in Fig. 3.7. For illustration, the LVT branch is disabled for one case (HVTonly) while the other case operates with both branches. Initially, the

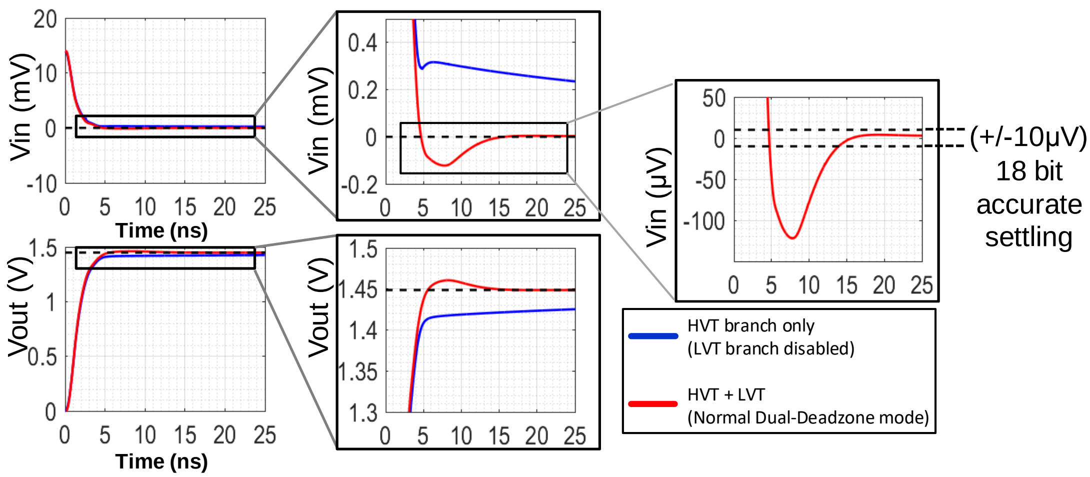

Figure 3.7: Transient RA comparison of typical output stage versus proprosed Dual-Deadzone output stage

output starts slewing for both cases. As the output approaches steady state value and the HVT branch shuts off, the HVTonly case falls short 50mV away from the ideal settled output value. For the normal case, the LVT branch takes over the residual transients and the virtual ground can be seen to settle to within $\pm 10\mu$V, equivalent to the 18 bit of settling accuracy.

A method for observing the Ring Amplifier transient response on-chip is shown in Fig. 3.8. The LSB capacitance of SAR1 is toggled while the remaining elements are forced to CM, similar the calibration mode described in section 2.3. SAR2 captures the RA output at the falling edge of SAR2 CLK. By having a programmable SAR2 CLK from 5 to 40ns with 1ns step, the RA output is sampled and averaged at each of those sampling instances. Therefore, the settling response of the Ring Amplifier is reconstructed. As shown in Fig. 3.8, the measured settling response for various

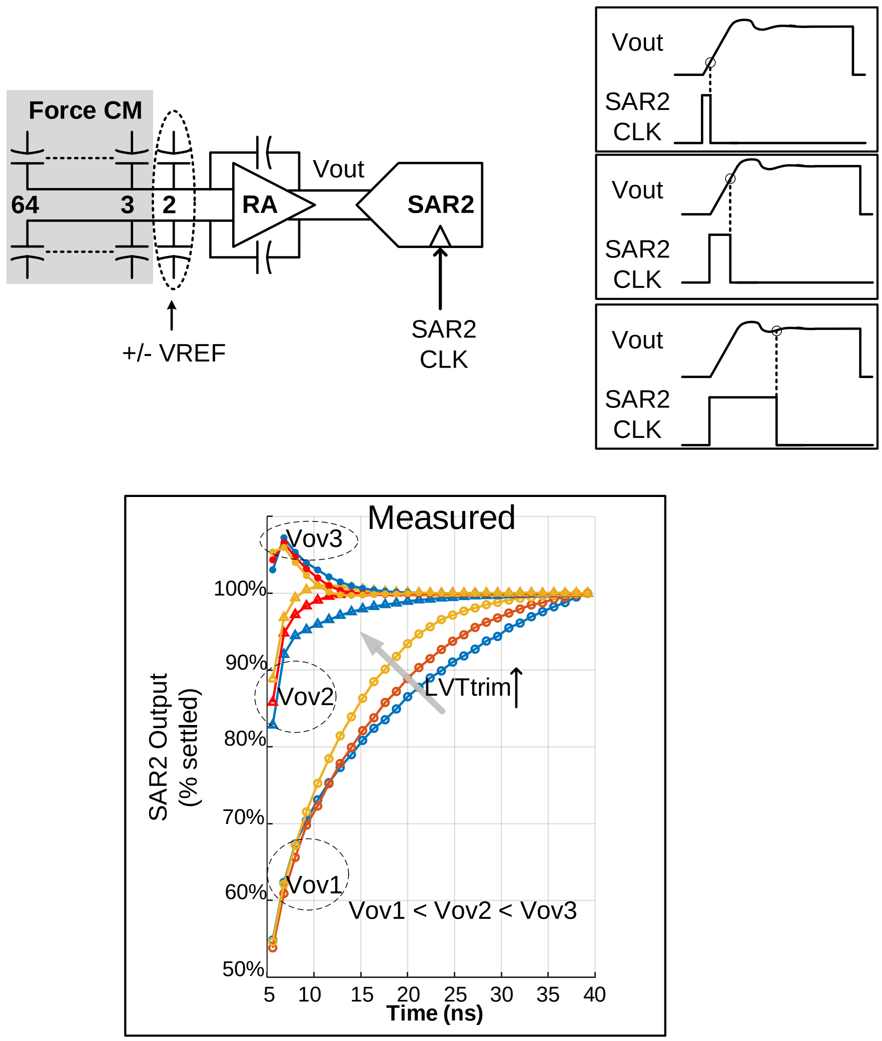

Figure 3.8: On-chip characterization technique for Ring Amplifier settling

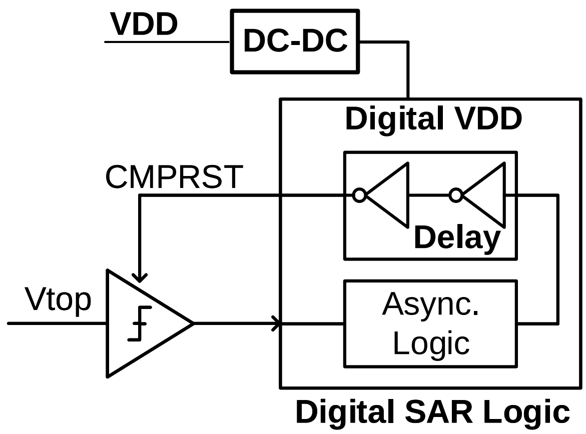

Figure 3.9: SAR block diagram with illustration of asynchronous operation

LVTtrim settings and deadzone bias voltages are captured utilizing this technique which gives good insight into the settling behaviour of the Ring Amplifier. The bias and LVTtrim settings can therefore be set accordingly to achieve the most optimum setting behaviour.

3.3 SAR2 Techniques

A few techniques were introduced in SAR2 to attempt faster conversion speed or reduced power consumption, which will be discussed in this section.

3.3.1 Dynamic VDD for variable bit clock

Fig. 3.9 shows the concept of asynchronous SAR logic. The asynchronous logic detects that the comparator has made a decision, and issues a comparator reset signal. The

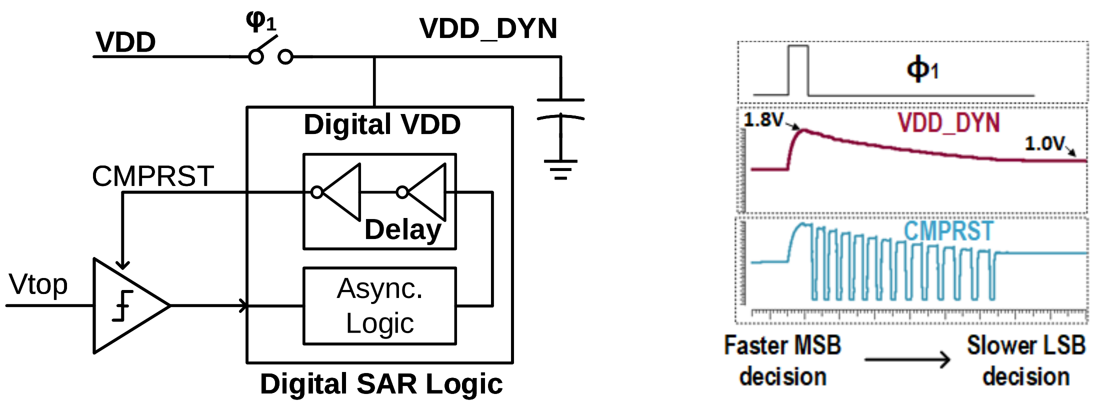

Figure 3.10: Dynamic VDD implementation and operation

comparator reset is delayed with a delay line. Once the comparator reset is completed, the asynchronous logic once again releases the comparator reset for the comparator to make a new decision. The period between a comparator decision and the next defines the bit cycle. The delay is inserted to allow for comparator decision to propagate in the SAR logic to the reference switches and then allow the completion of DAC settling prior to the next comparator decision. Redundancy in the SAR allows for larger margins of error for MSB decisions compared to LSB decisions. To optimize the conversion time, it is therefore favourable to have shorter bit cycles for MSB decisions and extending those of the LSB decisions. That would require the delay in the SAR logic to be programmable as a function of the bit under conversion.

In literature, it was suggested to have the digital delay line digitally tuned for that purpose. For this work, an analog approach is introduced where the supply of the delay line is reduced gradually with each bit decision. As the supply reduces, the delay line gets slower and gives LSBs more time to resolve. This is accomplished as

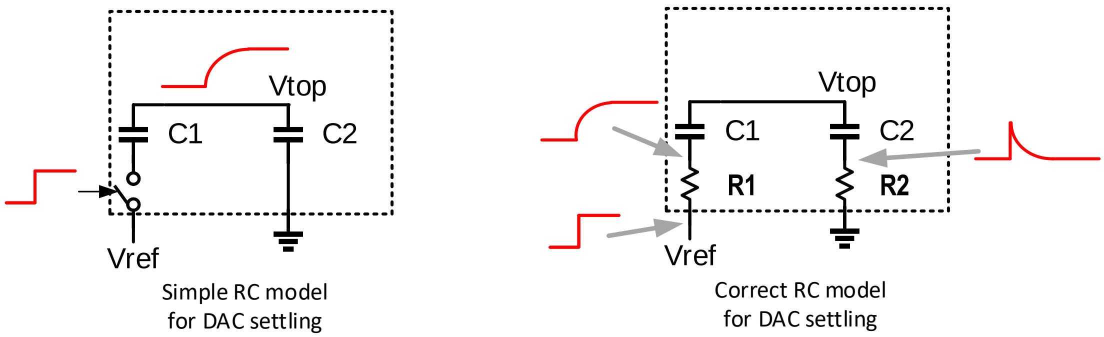

Figure 3.11: Typical and actual DAC settling dynamics

shown in Fig. 3.10 by simply adding a switched capacitor for the digital SAR logic supply. During sampling $\Phi 1$, the capacitor is pre-charged to VDD. During conversion, switch is disconnected and the capacitor serves as a charge reservoir for the digital SAR logic. The voltage on the capacitor reduces gradually with every bit decision. Additionally, power saving is obtained as the switched capacitor provides an effective step-down DC to DC converter operation.

3.3.2 Matched Impedance DAC

The second enhancement introduced to SAR2 for conversion speed improvement is the Matched Impedance DAC concept. Fig. 3.11 shows a simplified example of DAC settling where reference switch at C1 is switched on. In literature, DAC settling is usually discussed as a simple RC settling as shown on the left of Fig. 3.11 where a simple single pole RC time constant defines the DAC settling. In practice, as shown on the right, the remaining DAC capacitors lumped as C2 have their own switch

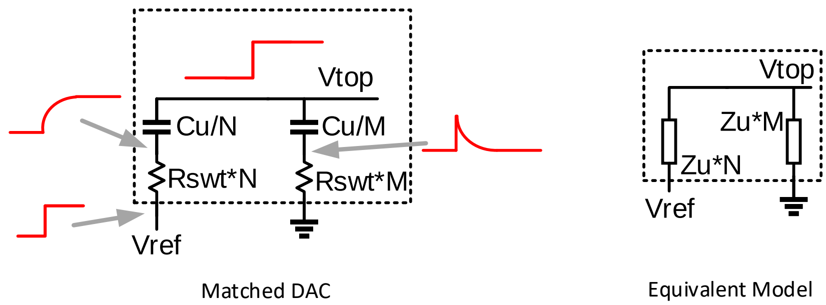

Figure 3.12: Matched Impedance DAC concept

resistances which in turn causes the transfer function to the top plate to be more complex.

The concept of Matched Impedance DAC, as shown in Fig. 3.12, is that if each DAC capacitor branch with their associated switch resistance is treated as a multiplier of a fixed impedance, Z_u, whose value is $R_{swt} + 1/(sC_u)$, the transfer function from any reference point to the top plate becomes a ratio of the multipliers and becomes independent of frequency. In time domain, that translates to instantaneous settling of the top plate. For the example shown in Fig. 3.12, the transfer function of $Vtop/Vref$ can be written as

$$\frac{V_{top}}{V_{ref}} = \frac{M}{M+N}$$

For a bridged-capacitance DAC, as shown in Fig. 3.13, the bridge impedance itself needs to be a multiplier of Z_u too to achieve Matched Impedance DAC concept. This is achieved by inserting a series resistance with the bridge capacitor. Hence, for the

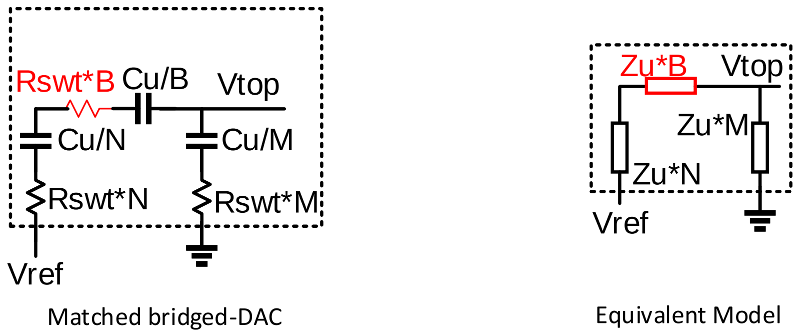

Figure 3.13: Matched Impedance concept for a bridged DAC

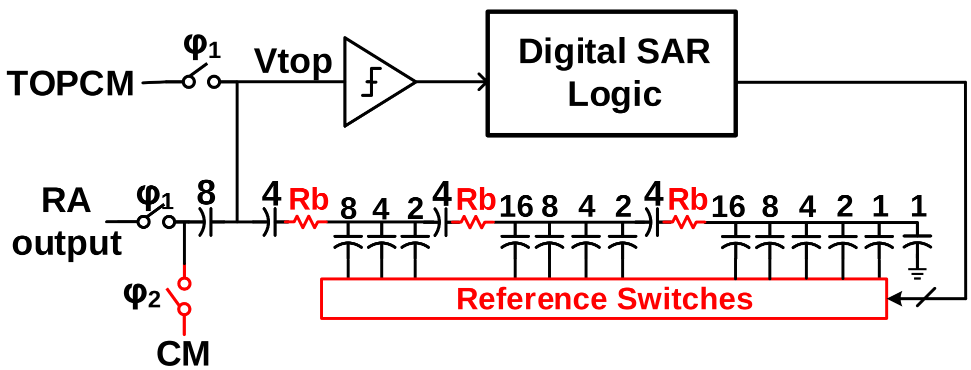

Figure 3.14: Matched Impedance DAC implementation for SAR2

example of Fig. 3.13, the transfer function becomes

$$\frac{V_{top}}{V_{ref}} = \frac{M}{M+B+N}$$

Fig. 3.14 shows the SAR2 DAC implementation of the Matched Impedance DAC where reference switch resistances are scaled with their respective capacitance units as well as bridge resistances, R_b, are added. The simulation results for the SAR2 DAC

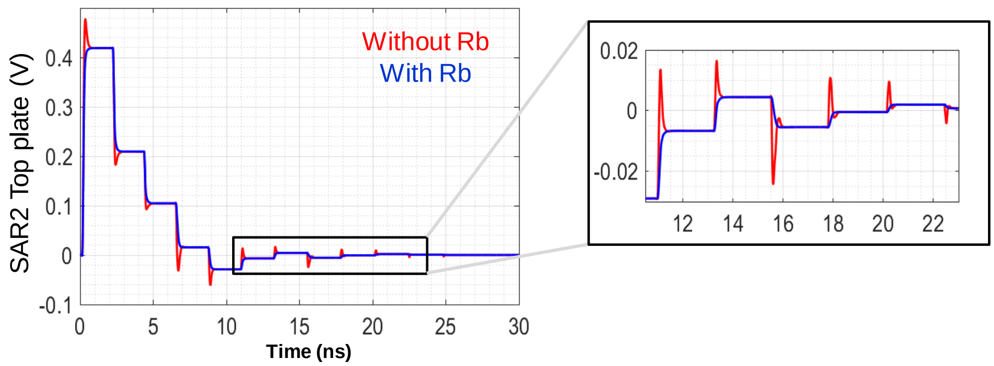

Figure 3.15: Simulation results with and without SAR2 Matched Impedance DAC

settling, with and without R_b, is shown in Fig. 3.15 where significant improvement to the settling behaviour is observed with the addition of R_b. This near instantaneous settling allows the bit cycle to be minimized to achieve a faster conversion rate.

3.4 Timing

Fig. 3.16 gives timing information for the various phases of the two-step SAR ADC. The falling edge of an external clock with low jitter is used to directly define the sampling instance of SAR1. Following that edge, on chip clock generation circuits create the fixed timing pulses for the remaining phases prior to returning to the input sampling phase. SAR1 conversion, which includes Flash and SAR operation of SAR1, consumes 21ns, followed by 21ns for residue amplification and finally, 5ns are dedicated to the reset phase. This translates to a fixed 47ns of conversion time. Depending on the external clock frequency, the remaining time left in the clock period

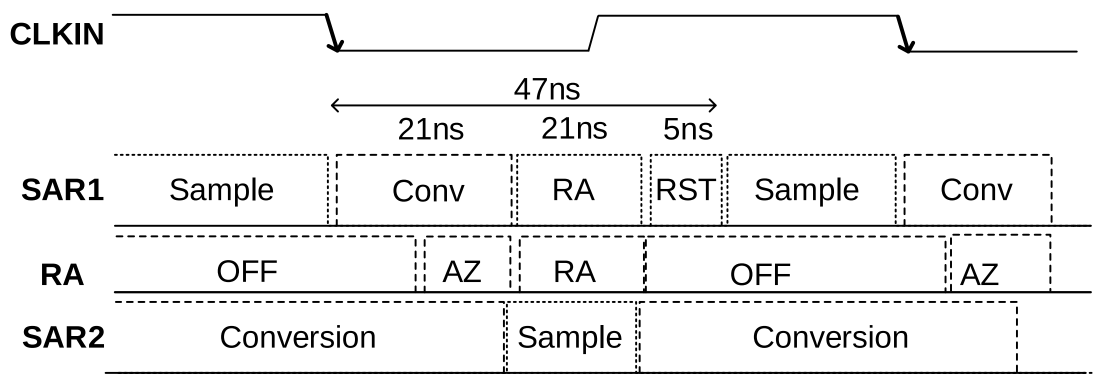

Figure 3.16: Detailed Timing diagram for the final two-step SAR ADC

goes towards input sampling. At the highest tested sampling rate of 15MS/s, this leaves the ADC with approximately 20ns for input sampling.

Chapter 4: Measured Results

4.1 Layout and Measurement Setup

The ADC is fabricated using AKM 0.18μm technology with 1.8/3.3V devices and occupies an area of 1.82mm^2. The die photo with floor plan indication is shown in Fig. 4.1. A few good practice precautions were taken to ensure minimal noise coupling from aggressive signals onto noise-sensitive nodes. The input signal, the reference voltage and analog supplies are all routed from the top side. The DACs of SAR1 and SAR2 are oriented towards the upper section of the floor plan while their respective digital logic as well as clock generation are placed towards the lower section. The residue amplifier is placed between SAR1 DAC and SAR2 DAC. SAR1 DAC top plate signals are routed to the RA inside a tunnel grounded shield. The Flash ADC is placed near the input signal to avoid long distance routing for the input signal.

Obtaining high linearity and low noise inputs with 3.3V swing for testing is a challenging task on its own. Fig. 4.2 shows the setup that obtained the best results for low and high frequency input signals. The Audio Precision source is a signal source able to provide signals with 20 bits of resolution and swing greater than 6V up to 200kHz frequency. To further reduce the noise of the signal source, a passive RC filter is introduced on board. It is important to mention to only use C0G/NP0 capacitors

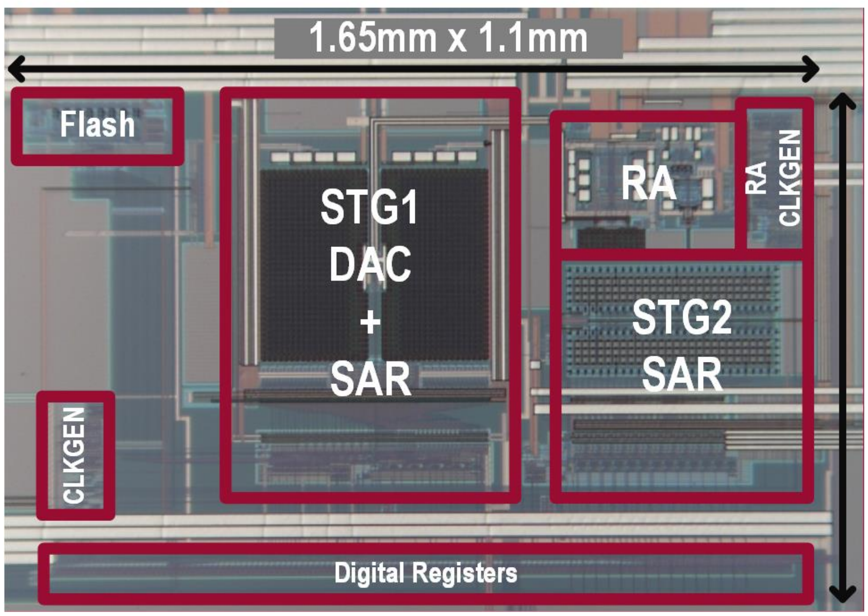

Figure 4.1: Die photo showing floorplan of main blocks

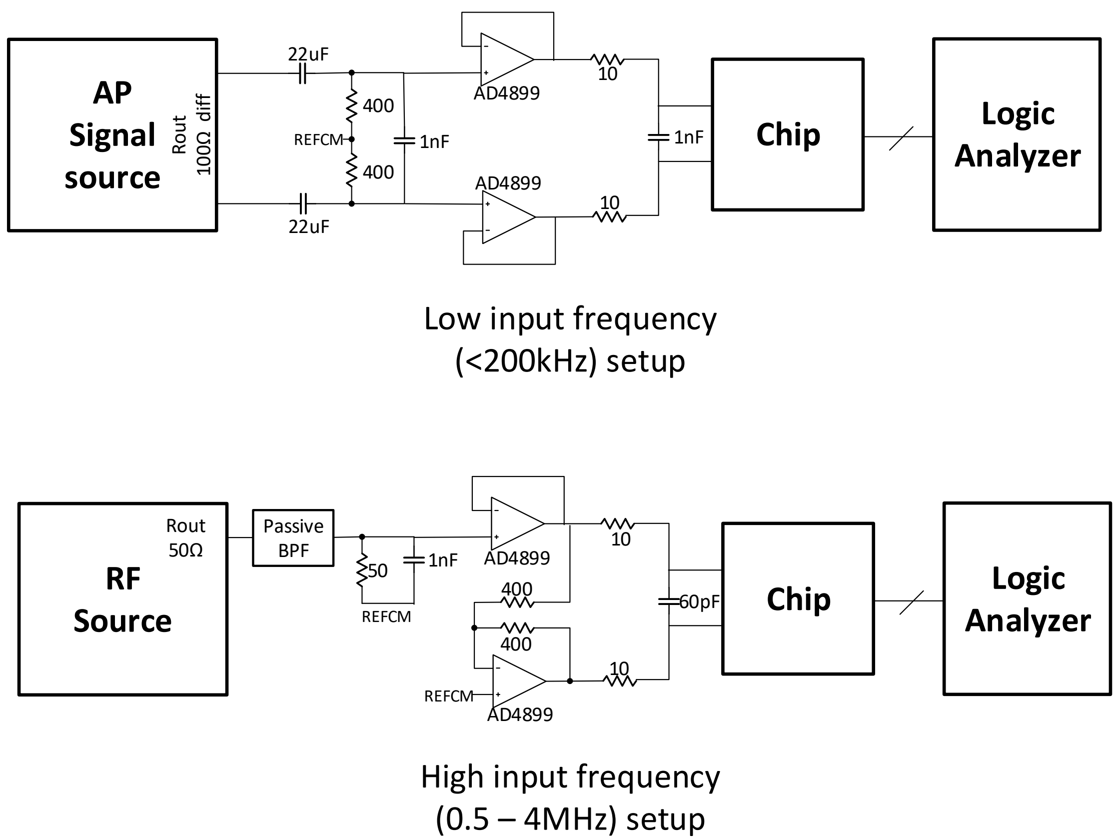

Figure 4.2: Measurement setup and input network for high linearity testing

for filtering the signal. These capacitor types exhibit zero voltage co-efficient, maintaining the linearity of the input signal. The filtered signal is then buffered using unity-gain buffers, AD4899, which have an excellent low noise performance and very wide bandwidth. They also act to isolate the signal source from the ADC input sampling network. The RC network between the buffers and the ADC limits the noise bandwidth of the buffers and further provides an extra layer of kickback isolation between signal source and ADC.

For input frequencies higher than 200kHz, RF sources are used. RF sources provide a single-ended sinusoidal output that is at best 10-12 bit linear. In order to create a 16-bit linear input, passive bandpass filters are connected in series with the RF filter. In order to the drive the ADC differentially, the bandpass filtered output is buffered with one AD4899 and the inverted version is created by inverting configuration of a second AD4899. Once again, an RC filter following the AD4899 opamps are inserted for the same reasons explained earlier.

4.2 Static and Dynamic Performance

The measured static performance (DNL/INL) of the ADC after capacitance weight calibration is shown in Fig. 4.3. The DNL indicates that the ADC has no missing codes while the INL shows that the ADC is linear to within ±1LSB of 16 bit level. It is interesting to note that the linearity is dominated by a third order transfer function which indicates that the source of such linearity is charge injection due to the input sampling switches.

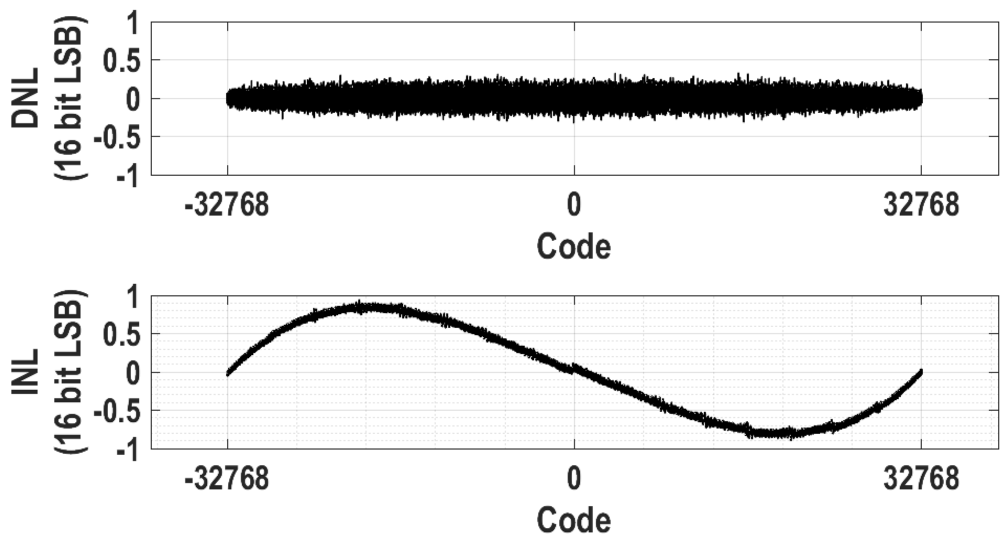

Figure 4.3: DNL/INL performance using sinusoidal histogram method for 1kHz 0dBFS input

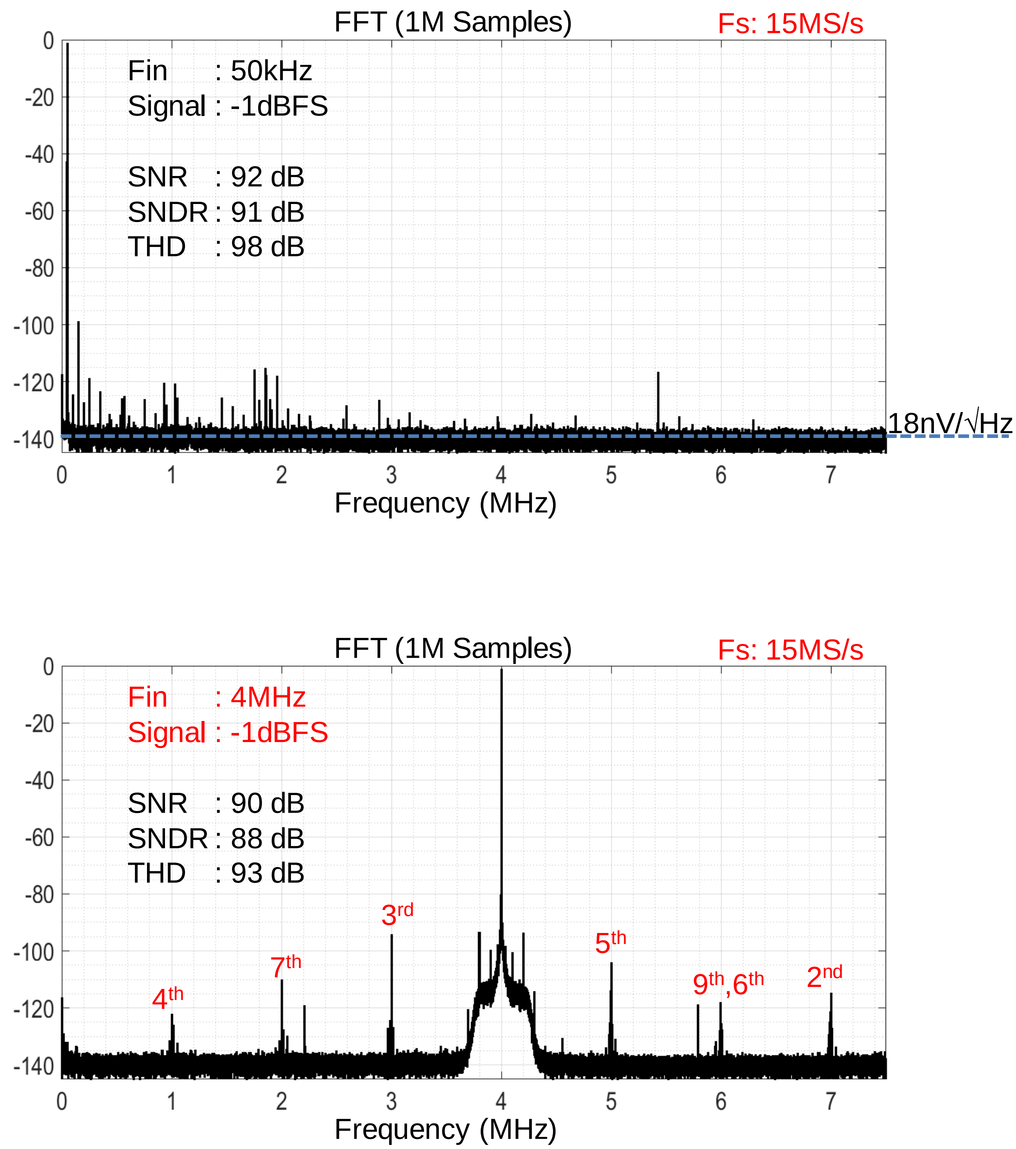

Figure 4.4: Dynamic performance at -1dBFS and input frequency of 50kHz and 4MHz at 15MS/s

The ADC dynamic performance at 15MS/s for a medium frequency input of 50kHz and a high frequency input of 4MHz is shown in Fig. 4.4. The ADC achieves a peak SNR of 92dB for a -1dBFS input. Even at -1dBFS, the ADC achieves a total harmonic distortion (THD) of 98dB. As seen from the spectrum, excluding the 3^{rd} harmonic, all other spurious activity is below the 120dB level. At 4MHz input, the harmonic distortion is degraded to 93dB which is expected due to non-linearities in the input buffer as well as input sampling network. The noise floor around the input tone is higher by around 30dB. This represents the noise floor of the RF source, which is then abruptly filtered by the sharp bandpass filter. Similarly, tones around the signal due to clock spurs or AM modulation in the RF source are filtered by the bandpass filter. The input signal is chosen such that all harmonics up to the 11^{th} are folded back in unique frequency bins as shown in Fig. 4.4. The SNR degradation by 2dB is speculated to be attributed to jitter in the input clock.

Fig 4.5 shows the SNDR and THD for input signal frequency swept from 1kHz up to 4MHz at two sampling rates, 10MS/s and 15MS/s, with -2dBFS inputs. For each frequency range, the input driving network is optimized for best performance. The 1dB SNDR difference between 10MS/s and 15MS/s is attributed to the different noise filtering bandwidth at the output of the input driver opamps. At 10MS/s, since the input signal is allowed more time for settling, the noise filtering bandwidth is reduced giving an extra 1dB of SNR.

The dynamic range (DR) is measured at 2MS/s and a very narrow input noise filtering bandwidth to used to ensure that only the ADC noise is dominating. The ADC achieves a DR of 95dB as shown in Fig. 4.6. The ADC is off the design target

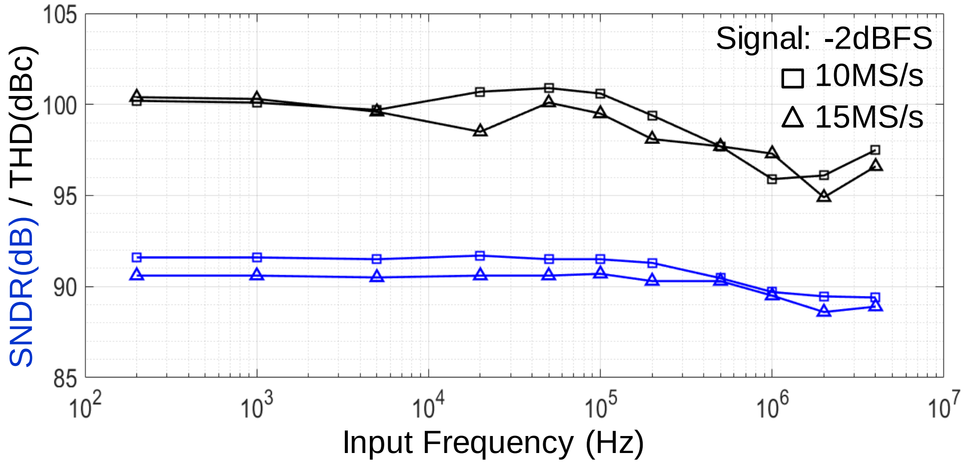

Figure 4.5: Input frequency sweep at -2dBFS for 10MS/s and 15MS/s

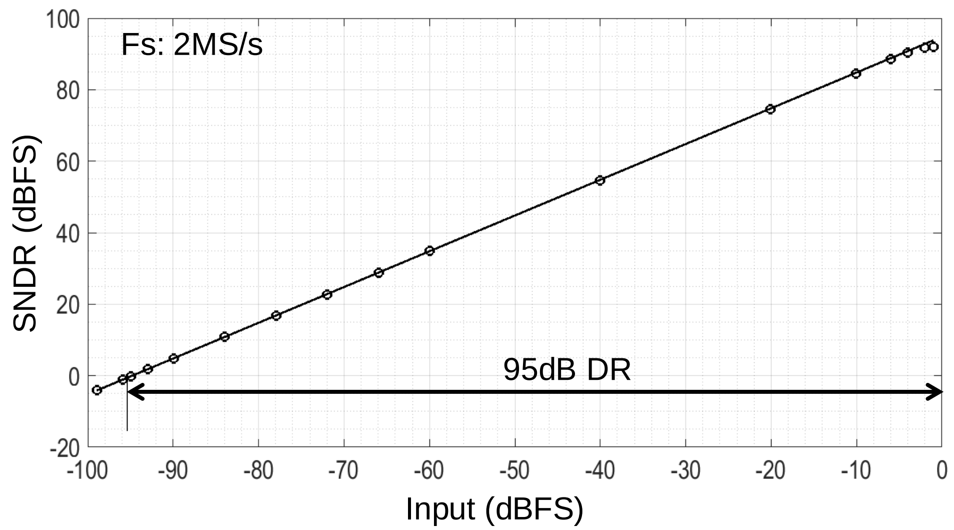

Figure 4.6: Dynamic range measurement at 2MS/s

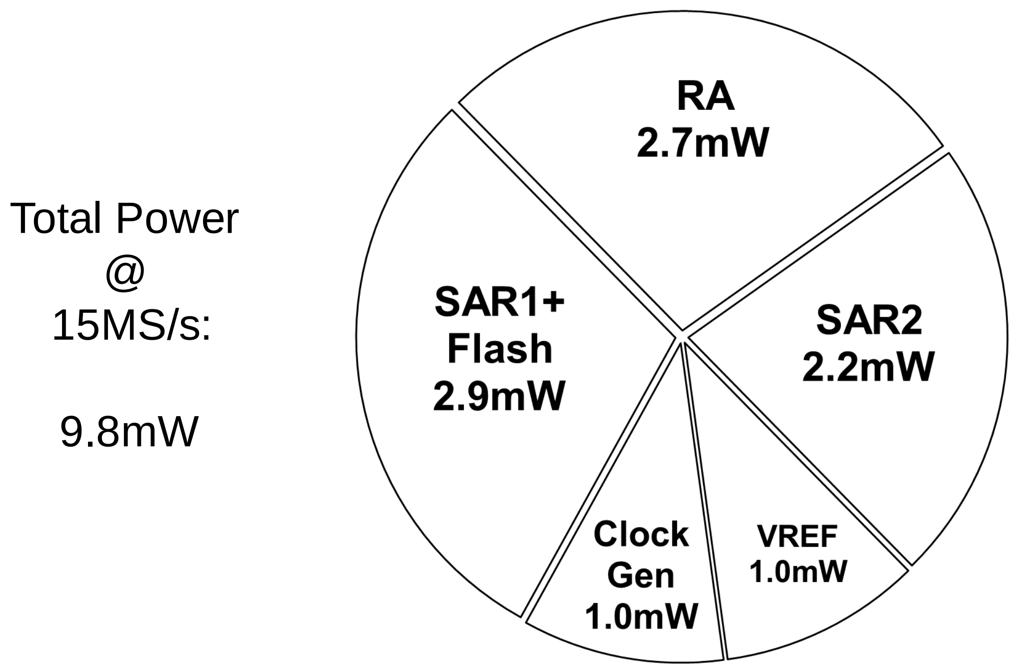

Figure 4.7: Power consumption and contribution of major blocks at 15MS/s

of 98dB by 3dB due to a couple of known reasons. A miscalculation in the initial system design under estimated the required size of SAR1 DAC capacitance leading to approximately 2dB degradation in SNR. Additionally, noise from the auto zero phase as well as increased parasitic capacitance due to layout at the top plate of SAR1 DAC, contributed towards an extra 1dB of SNR degradation. Nevertheless, the DR of 95dB achieved in this work proves that the optimized Ring Amplifier structure is capable of providing residue amplification for high resolution ADCs.

At the highest sample rate of 15MS/s, the ADC consumes 9.8mW as shown in Fig. 4.7. The fact that the residue amplifier power consumption is on the same level

Technology	180nm		
Resolution, Max. fs	16bit, 15MS/s		
ADC Area	1.82mm^2		
INL (16 bit)	+/-1 LSB		
Sampling Rate	**2MS/s**	**15MS/s**	
Power	1.6mW	9.8mW	
DR (dB)	95	93.9	
Input Signal Frequency	**LF**	**LF**	**HF**
Peak SNDR (dB)	92.3	91	88
FOM$_{SNDR}$ (dB) [SNDR + 10log10(fs/(2*P))]	180.2	179.8	177.8
FOM$_{DR}$ (dB) [DR + 10log10(fs/(2*P))]	182.9	182.7	

Table 4.1: Measurement summary at 2MS/s and 15MS/s

as SAR1 and SAR2 is sufficient evidence of the power efficiency of the Ring Amplifier structure. The ADC draws 1mW of power from the external reference voltages and an additional 1mW is consumed to create the various clock phases of the two-step SAR ADC.

4.3 Measurement Summary

Table 4.1 summarizes the measurement results discussed so far. The results show that the power consumption scales with sampling rate, maintaining the Schreier Figure-of-Merit (FOM_{DR}) in the range of 183dB.

Chapter 5: Conclusion

In this work, the design and measurement of a 16 bit two-step SAR ADC using Ring Amplifiers was presented. The Ring Amplifier was shown to be a well-suited residue amplifier for two-step SAR architecture in terms of power and speed. An optimized Ring Amplifier structures was proposed, i.e. Dual-Deadzone Ring Amplifier, which adds an additional degree of freedom to optimally achieve speed and accuracy. Furthermore, design techniques were introduced in SAR operation that improve on conversion speed and power savings. The system design flow with rational behind architectural decisions were discussed in chapter 2. Circuit implementation details with emphasis on the Dual-Deadzone Ring Amplifier was covered in chapter 3. Finally the measurement results were presented in chapter 4.

Table 5.1 compares the performance achieved in this work with that of other two-step SAR ADCs in recent literature [1, 8, 16, 35–38]. For ADCs with SNDR greater than 90dB, this work demonstrates the lowest power consumption per MS/s.

Fig. 5.1 represents the Schreier figure-of-merit versus nyquist sampling rate of ADCs published in ISSCC and VLSI since 1997 to date [39]. The dotted line represents a fitted empirical upper level envelope of performance. For nyquist frequencies lower than approximately 20MS/s, the FOM envelope is flat around 180dB. It can be argued that this limit is related to a fundamental thermal noise limit. The ADC presented in this work maintains a FOM of 180dB or slightly higher across the nyquist rate of 2MS/s to 15MS/s. This is made possible by ensuring noise budget is mainly thermal noise limited and power consumed by all blocks is dynamic. For analog power, duty cycling ensures power scales with sampling rate while remaining digital power is dynamic by nature. For higher nyquist sampling rates, the roll off in the envelope is driven by jitter in the sampling clock which imposes a limitation to the maximum achievable SNDR at certain input frequency.

For future work, obtaining higher dynamic range could be made possible by utilizing technology with higher voltage such as 5V devices and targeting larger input sampling capacitance of SAR1 DAC. Second, for improved linearity at higher input frequency and larger sampling capacitance, integrating an on-chip input buffer that adapts to the ADC sampling rate and input frequency range of interest would add significant benefit to the ADC usage model.

	This Work [29]				Ring Amplifier Based			
	2MS/s	15MS/s	Li [30] ISSCC 18	Hummerston [31] VLSI 17	Lim [7] VLSI 17	Lim [32] ISSCC 15	Bannon [13] VLSI 14	Hurrell [1] ISSCC 10
Technology [nm]	180		180/500	180	40	65	180	250
Reference [V]	3.3		5.0	5.0	1.1	1.2	5.0	5.0
RA Gain	64		32	64**	64	32	64	42.66
Calibration	Foreground		Background	Trimmed**	None	None	Trimmed	Measured
Speed [MS/s]	2	15	1	2	100	50	5	12.5
SNDR [dB]	92.3	90.8†	101.5	99.2††	73.2	71.5	98.6	92.7
SFDR (THD) [dB]	96.8	100.7	132.0	-107.0	90.4	87.0	109.2	104/-100
SNR/DR [dB]	94.2/95.0	91.3†/93.9†	101.5††/102.7	100.0/100.5	73.3/-	71.9/-	99.0/100.2	93.0/93.0
ADC Power [mW]	1.61*	9.82*	12.9	11.35	2.3	1.0	30.52	105
Area [mm^2]	1.82		4	3.87	0.068	0.054	5.74	5.74
$FOMs_{SNDR}$	180.2	179.6†	177.4	178.6††	176.6	175.5	177.7	170.4
$FOMs_{DR}$	182.9	182.7†	178.6	179.9	–	–	179.3	170.7

* Not including digital output drivers.
** Information reported in table is based from previous design
† Actual performance is better by 1.1dB. Reported number is limited by ADC driver.
†† Information reported is calculated based on other performance numbers provided

Table 5.1: Comparison between this work and state-of-the-art

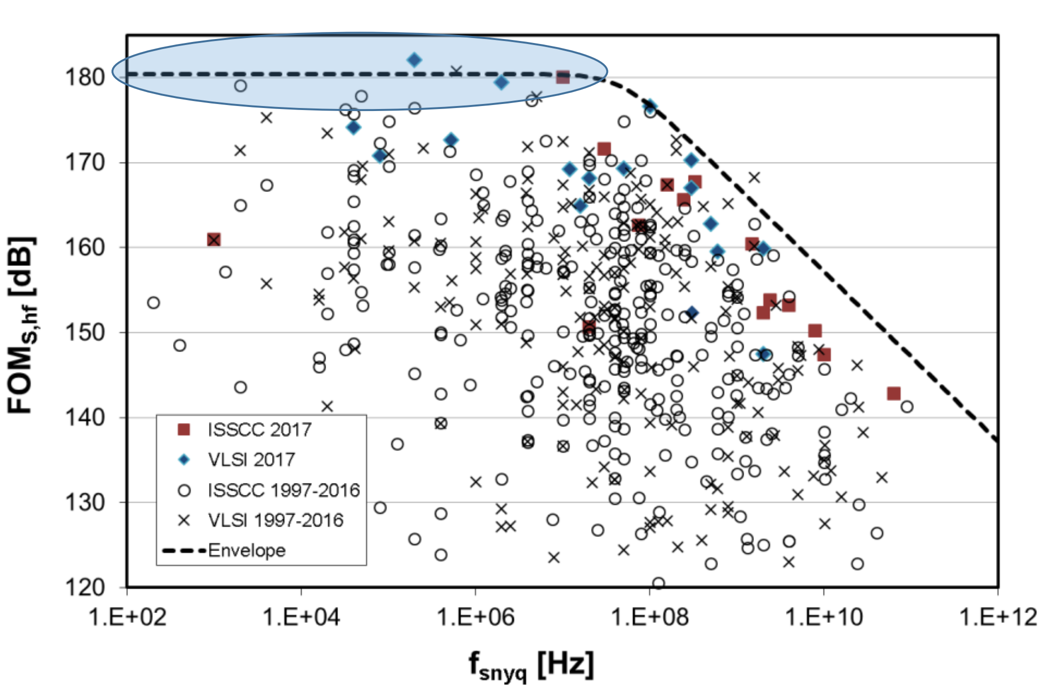

Figure 5.1: Chart showing Schreier FOM versus nyquist bandwidth of ADCs published in ISSCC and VLSI

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