AN ABSTRACT OF THE DISSERTATION OF

Boyu Shen for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on December 2, 2020.

Title: Imepdance Sensing Techniques for Integrated Circuits Sensor Applications

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Matthew L. Johnston

Impedance measurements are increasingly utilized in modern integrated circuit sensing systems, as impedance is the most common electrical signal obtained from sensors, delivering physical, chemical and biomedical signals of interest from different sensor types. Impedance sensing for wide frequencies of interest, broad dynamic range, and various sensor interfaces present numerous challenges, especially for targeted implementation in CMOS for miniaturization, which presents power and area limitations. In this thesis, first, a low power impedance-based cytometer architecture for cell analysis applications is presented. Fabricated in 0.18m CMOS process with 6pArms input-referred noise over 200Hz bandwidth at 0.5 MHz modulation frequency, the impedance sensor demonstrates in detecting 3m diameter particles. Secondly, a low-noise, front-end sensor IC that includes both AC impedance spectroscopy and DC amperometric measurement capabilities for electrochemical and biosensor applications is presented. Implemented using a 0.18 µm CMOS process, this work achieves 45 fA/$\sqrt{\text{Hz}}$ input current noise density at 1 kHz, and a maximum of 104 dB dynamic range at 10 Hz. Finally, using an impedance sensing technique, a

low-power RC oscillator based on IQ-balanced impedance sensing frequency-locked loop is designed and demonstrated, achieving 25.4ppm/°C across temperature variation and 0.27%/V across supply variation at 650kHz output frequency.

Imepdance Sensing Techniques for Integrated Circuits Sensor Applications

by

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

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Boyu Shen, Author

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It has been a great journey since I came to Corvallis in 2015 after I graduated from my bachelor degree in University of Science and Technology of China (USTC) in China. I would first thanks to my advisor, Dr. Matthew Johnston, who brought me here when I was still a fresh man in circuit design with no extra experience and taught me numerous knowledge in conducting, writing, and presenting the research. It is also him who gave all the freedom and support for me to perform research that I am interested in. Secondly, I would like to thank all the people in my research group SIM lab, Soumya, Hyunkyu, Shaan, Kyle, Jinyong, Jacob, Callen, and all the other new members I have not got a chance to works with. Special thanks to Soumya: your encouragement and guidance during the five years mean a lot to me, and working with you for me is really a honor, and Hyunkyu: you are a such good senior colleague and friend who taught me so much in research and in life. Then, I would thanks to all my friends in Kelly and Corvallis during this amazing journey: Yutao, Yang, Yao, Kai, Yanchao, Lukang, Xuanyi, Bo, Jialin, and everyone who helped me. Besides, I want to thank my parents who have always relentlessly supported me for what I want to do. I want to thank my girlfriend, Jianing, who is still in China and has been separated with me in the past four years, but constantly supported me and stood by me to share with my joy and sadness. I love you and wish we can reunite soon. Finally, I want to thank Corvallis where has been a fantastic place for me to live and study. I love every inch of the ground in Corvallis and will never forget the people, the view, and the serenity of Corvallis. See you Corvallis! Zaijian OSU!

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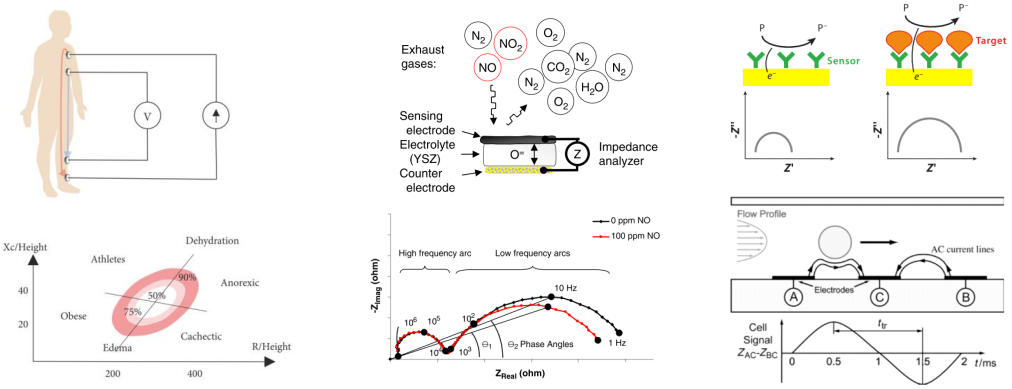
Chapter 1: Introduction

1.1 Impedance Measurements in Sensors

Impedance measurements are increasingly utilized in modern integrated circuit sensing systems, as impedance is the most common electrical signal obtained from sensors, delivering physical, chemical and biomedical signals of interest from different sensor types. Impedance sensing for wide frequencies of interest, broad dynamic range, and various sensor interfaces present numerous challenges, especially for targeted implementation in CMOS for miniaturization, which presents power and area limitations. Fig. 1.1 shows several sensing applications using impedance sensing techniques such as bioimpedance sensing, gas sensing, DNA sensing, and cell sensing. Bioimpedance analysis Fig. 1.1a is a low-cost and noninvasive for body composition measurements and assessment of clinical condition. By accessing the tissue electrical resistance and reactance across the electrodes on the body at different frequency, the body composition can be predicted and analyzed. Gas sensing Fig. 1.1b using impedance spectroscopy is also a popular and well-developed approach, which is attractive to industry and personal use due to its low-cost in production. Electrochemical impedance sensing Fig. 1.1c is also a promising biosensing technique because of its label-free, low-cost and ease of miniaturization.

Alternating-current (AC) impedance sensing technique has its several intrinsic advantages compared with its direct-current (DC) counterpart: 1) AC stimulus over



(a) (b) (c)

Figure 1.1: Impedance sensing technique used in (a)bioimepdance sensing [1]; (b)gas sensing [2]; (c) Biosening (DNA, cell) [3], [4]

various frequency can access recatance more than pure resistance information, representing more comprehensive understand in sensor analysis; 2) AC measurement can employ small stimulus amplitude, which is able to preserve the linearity of the sensor, and will not cause heat dissipation with high-DC current; 3) Another important feature for AC impedance measurement is AC operation normally hardly change the characteristics of the electrode, yielding a more stable and predictable measuring environment in long term.

Most of the impedance sensing applications can be classified into two category in terms of how the impedance is accessed and analyzed. The first one is impedance spectroscopy (IS), where impedance of the sensor across the whole interested frequency band are required by sweeping the frequency. This approach is often considered as the most sophisticated and informative because the overall impedance band over frequency can be obtained, however, it requires hardware to be sophisticated as

well, extra post-processing, and sweeping period, which makes it hard for real-time processing. On the other hand, the second approach is fixing the operating frequency at one interested frequency and sensing the change in electrical signal. This is approach is low-cost and easy for circuit miniaturization and multiplexing. However, it is relatively low accuracy and requires calibrating and analysis to select a reliable operating frequency. Both approaches are broadly adopted depending on the applications, and an intermediate approach which uses 2-point or 3-point operating frequencies is also favored.

Implementing impedance sensing technique by integrated circuits and building a on-chip impedance sensing systems have numerous challenges in terms of sensitivity, accuracy, dynamic range, frequency range, interface-compatibility, multi-channel extension, power and chip area based on specific applications and design limitations. This thesis will analyze some of the above-mentioned challenges and propose particular system and circuit techniques to overcome them.

1.2 Scope of the Thesis

In this thesis, three projects related to impedance sensing techniques are presented.

In Chapter 2, a low-power, impedance-based cytometer architecture is presented for cell analysis applications. By adopting a 3-electrode layout and a differential excitation voltage, baseline current is cancelled before the sensor front-end to achieve high sensitivity. The difference current is sensed by a closed-loop, impedance sensing

circuit architecture, which employs a hybrid-RC feedback network to overcome the SNR degradation seen over a wide operating frequency range when using purely capacitive feedback; this is especially critical when a microfluidic flow channel is used as the input sensing element, which includes a resistive component. The effect of phase shift on the closed-loop system gain and noise performance are analyzed in detail, and optimization strategies are presented. The impedance sensor was fabricated in a 0.18 μm CMOS process and consumes 9.7 mW with an operating frequency from 50 kHz to 40 MHz and provides adjustable bandwidth. Measurements demonstrate that the impedance sensor achieves 6 $\mathrm{pA_{rms}}$ input-referred noise over 200 Hz bandwidth at 0.5 MHz modulation frequency. Combined with a microfluidic flow cell, measured results using this source-differential measurement approach are presented using both monodisperse and polydisperse sample solutions and demonstrate single-cell resolution, detecting 3 μm diameter particles in solution with 22 dB SNR.

Chapter 3 presents a low-noise, front-end sensor IC that includes both AC impedance spectroscopy and DC amperometric measurement capabilities for electrochemical and biosensor applications. A common-gate current buffer topology is proposed that supports both current-mode and voltage-mode sensor signals to allow an input frequency range from DC to 100 kHz. Low-noise operation is achieved across a wide input frequency range using tunable high-pass and low-pass frequency response. In addition, an incremental delta-sigma modulator with embedded frequency response analysis serves as both on-chip impedance analyzer and current-driven analog-to-digital converter. Implemented using a 0.18 µm CMOS process, this work achieves 45 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ input current noise density at 1 kHz. Input dynamic range exceeding

80 dB is achieved up to 10 kHz bandwidth, with a maximum of 104 dB dynamic range at 10 Hz.

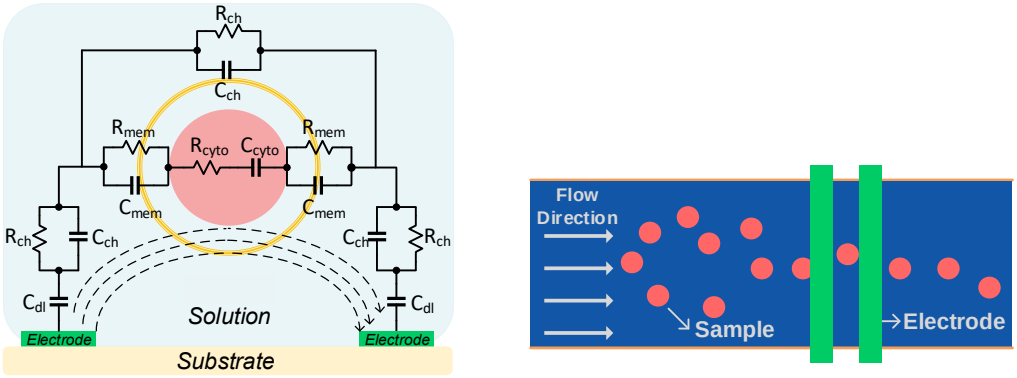
In Chapter 4, although particular impedance sensor is not presented, the impedance sensing technique has been applied into the low-power RC frequency generator, and a novel impedance IQ-balanced frequency locked-loop (FLL) is proposed and demonstrated. With alternative phase mixing technique, the proposed FLL achieves 1.26 pJ/Cycle energy efficiency with 25.4 ppm/°C temperature coefficient and 0.27%/V line sensitivity at 650 kHz. A excellent long-term frequency stability with measured 16 ppm Alan deviation is also demonstrated for this work.

Chapter 2: A Impedance Sensor for Source-Differential Flow Cytometry

2.1 Introduction

Flow cytometry plays a vital role in microbiology and medical diagnostics for counting and classifying heterogeneous cell populations, as well as for measuring single-cell physical properties. Conventional optical flow cytometers provide high throughput counting and cell subtyping, but complex optics drive cost and size for the instruments [6]. Moreover, fluorescent labels are required for some subtyping and downstream cell sorting, including fluorescence activated cell sorting (FACS), which further limits viability for point-of-care (POC) applications. Purely electrical Coulter-counters eliminate optical components, but these have a limited ability to assess cell structure, composition, or type. For a variety of clinical diagnostic applications, there remains a critical need for a miniaturized and label-free flow cytometer.

Impedance spectroscopy (IS) can be used to characterize the dielectric properties of cells in solution, providing details of cell membrane structure and cell composition (Fig. 2.1) [7, 8]. Combining advances in microfluidic systems with impedance spectroscopy techniques has enabled lab-on-chip flow cytometers with single-cell resolution; prior work has successfully demonstrated micrometer-scale particle detection using microfluidics-based devices and a commercial bench-top impedance analyzer [4, 9–12]. Further enhancing the limit of detection (LOD) and throughput for



(a) (b)

Figure 2.1: (a) Equivalent circuit model of a single cell in solution, and (b) top-down illustration of IS electrodes in a microfluidic flow channel.

such systems motivates the integration of sensor and sensing electronics into a single chip, which also enables low-noise and multi-channel operation.

General impedance spectroscopy has been demonstrated previously using complementary metal-oxide-semiconductor (CMOS) silicon integrated circuits, primarily for measuring electrochemical reactions at electrode-electrolyte interface [13–16]. These applications typically require operation from 1 Hz to 1 MHz, where a full-span frequency sweep is required to analyze the electrochemical behavior, and thus the dynamic range specification of the IS instrument is essential. Impedance-based flow cytometry, in comparison, requires real-time measurement and is typically performed at one or two fixed operating frequencies to analyze specific cell physical properties in real time. In this case, noise performance is more critical, as the cell dimension is small compared to the channel.

For impedance-based cell analysis, megahertz operating frequency minimizes double-layer capacitor impedance ($C_{\mathrm{dl}} \approx 100\,\mathrm{pF}$) to enhance SNR; the properties of channel

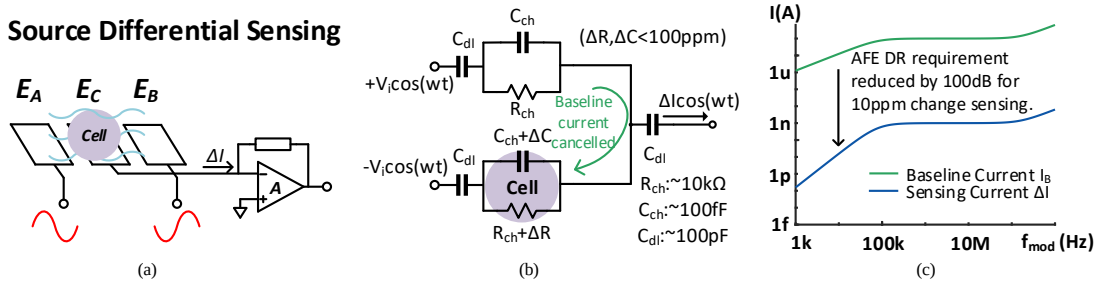


Figure 2.2: (a) Source-differential impedance cytometry topology, (b) equivalent circuit model of source-differential sensing scheme, and (c) frequency response of sensing current versus baseline current magnitude for source-differential sensing scheme.

resistance (R_{ch}), cell membrane capacitance (C_{mem}), cell cytoplasm resistance (R_{cyto}) and cell cytoplasm capacitance (C_{cyto}) can be accessed and analyzed at frequency of 0.5-5 MHz, 5-10 MHz, 10-100 MHz and >100 MHz, respectively [4]. It is important to note that the physical size of the cell primarily induces the R_{ch} variation, similar to current exclusion in Coulter counting. A closed-loop modulation/demodulation architecture for generalized capacitive sensing applications was introduced in [17] that achieves sub-aF capacitance resolution operating up to 150 MHz. However, this approach uses purely capacitive feedback, which limits closed-loop gain as well as SNR performance for cytometry applications specifically, where microfluidic channel resistance, R_{ch} (Fig. 2.1a), remains dominant in the megahertz range.

In this paper, we present a modulation/demodulation impedance sensor architecture on chip with hybrid feedback that maintains closed-loop gain across cytometry-relevant operating frequencies with low (<10 mW) power consumption. The impact of loop-gain phase shift on system gain and noise is analyzed and optimized. Following electrical characterization of the architecture implemented in a 0.18 µm CMOS process, the impedance sensor is experimentally characterized using a custom mi-

crofluidic flow cell to demonstrate real-time flow cytometry. A source-differential electrode layout and impedance sensing scheme cancels out baseline current to increase sensitivity. The system demonstrates detection of 3 µm beads and separation of polydisperse beads in solution, demonstrating single-cell resolution under flow conditions.

2.2 Hybrid-feedback IS for Source-Differential Impedance Cytometry

2.2.1 Source-differential sensing scheme

Source-differential impedance sensing, illustrated in Fig. 2.2a, is commonly used to measure small changes in a large bulk impedance [18]. This is a particularly relevant approach for impedance based cytometry, where cells are typically small compared to the overall microfluidic channel volume. As is shown in Fig. 2.2a, for source-differential readout, anti-phase AC excitation signals are applied to the outer electrodes E_{A} and E_{B}, and only sensing current ΔI is incident on the middle electrode. This source-differential measurement is advantageous in comparison to single-ended and single-source differential approaches, where without baseline current cancellation, the current output superimposes small cell-induced changes with a large baseline current, and hence a majority of the input dynamic range of the downstream measurement electronics is used for the baseline channel signal, limiting usable gain and achievable measurement sensitivity for the small cell signal.

An equivalent circuit model is shown in Fig. 2.2b, where complex channel impedance and cell impedance are lumped into a parallel RC model for simplicity. If the

impedance between two electrode pairs without a cell present are perfectly matched, the baseline current will flow between each excitation source, with zero current flowing into the sensing electronics. As a cell crosses either electrode pair, the corresponding change ΔC in channel capacitance, C_{ch}, and and ΔR in channel resistance, R_{ch}, yields unbalanced channel pairs, inducing a small difference current at the readout electronics, while balanced baseline current is neutralized.

A current magnitude frequency response of the source-differential equivalent model is shown in Fig. 2.2c, assuming 10 ppm change in both R_{ch} and C_{ch}. With baseline current cancelled, the source-differential sensing scheme achieves a 100 dB relaxation in required analog front-end (AFE) dynamic range. In addition to relaxing input dynamic range, additional benefits are gained: correlated noise and fluctuation from the excitation source will be mitigated, two-wire input for measurement electronics is replaced by a single wire, which reduces circuit and system complexity and increases scalability for multichannel applications.

2.2.2 Hybrid-feedback Impedance Sensor

A closed-loop impedance sensing architecture suitable for high frequency operation was used, and a high-level block-diagram is illustrated in Fig. 2.3. Unlike a more conventional coherent detection scheme that uses a transimpedance amplifier (TIA), down-converter, and low-pass filter, this architecture integrates down-conversion and up-conversion into the feedback loop, which alleviates the gain-bandwidth limitation of the conventional TIA-first topology [17].

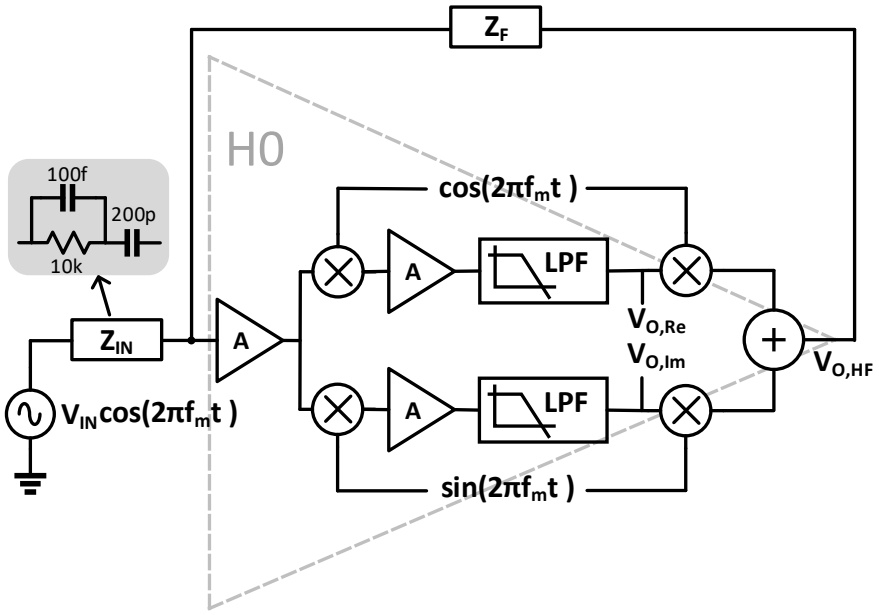


Figure 2.3: Generalized circuit model for a modulation/demodulation impedance measurement architecture with an impedance model cell at the input.

If we treat the down-converter, low-pass filter, and up-converter chain as a composed amplifier $H0$, the closed-loop gain from the input, V_{IN}, to the high-frequency output, $V_{\mathrm{O,HF}}$, can be obtained as

$$A_{\mathrm{CL}} = \frac{V_{\mathrm{O,HF}}}{V_{\mathrm{IN}}} = \frac{Z_{\mathrm{F}}}{Z_{\mathrm{IN}}} \frac{LG}{1+LG} \tag{2.1}$$

where LG is the loop gain of the feedback system. If LG is large enough at the modulation frequency, the output of the impedance sensor $V_{\mathrm{O,HF}}$, as well as its low-frequency baseband component V_{O}, is purely dependent on Z_{IN} if V_{IN} and Z_{F} are known in advance. Assuming the gain of up-converter is unity, the real and imaginary components of Z_{IN} can be calculated as follows, if modulation clock $cos(2\pi f_{\mathrm{m}} t)$ is in

phase with the excitation source,

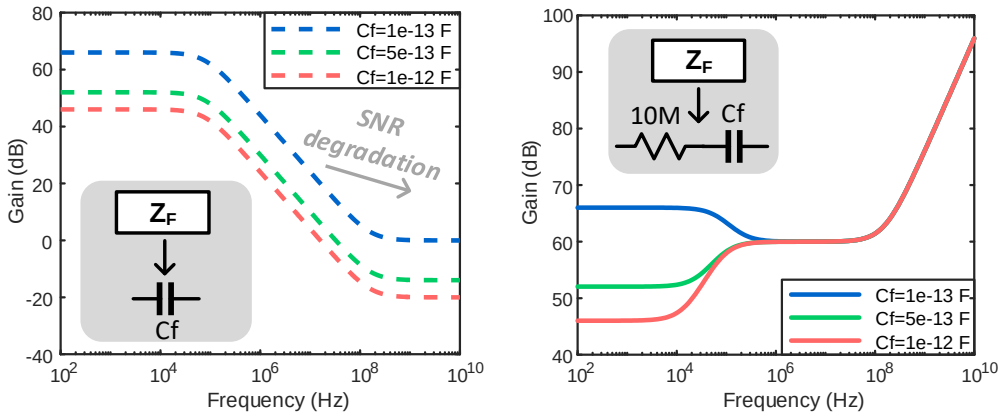
$$\mathrm{Re}\{Z_{\mathrm{IN}}\} = -\frac{V_{\mathrm{IN}} \cdot Z_{\mathrm{F}}}{V_{\mathrm{O,Re}}}, \quad \mathrm{Im}\{Z_{\mathrm{IN}}\} = \frac{V_{\mathrm{IN}} \cdot Z_{\mathrm{F}}}{V_{\mathrm{O,Im}}} \tag{2.2}$$

where $V_{\mathrm{O,R}}$ and $V_{\mathrm{O,I}}$ are the impedance sensor voltage outputs of the real and imaginary baseband components.

In [17], the feedback element Z_{F} is realized solely by a capacitor (100 fF), which is suitable for a purely capacitive sensing elements at Z_{IN}. However, the cell model given in Fig. 2.3 (Z_{IN}) is more typical for cytometry, where the resistive impedance component is dominant in the megahertz range; as such, the closed-loop gain A_{CL} will decrease as frequency increases, as shown in Fig. 2.4a. This decrease of A_{CL} leads to a degradation of the impedance sensor noise performance, where signal-to-noise ratio (SNR) at the output of the impedance sensor is given as

$$\mathrm{SNR}_{\mathrm{out}} = \frac{V_{\mathrm{IN}}}{\overline{v_{\mathrm{n,tot}}} \cdot BW_{\mathrm{EN}}} \frac{A_{\mathrm{CL}}}{1 + A_{\mathrm{CL}}} \tag{2.3}$$

if only noise from $H0$ is considered, where $\overline{v_{\mathrm{n,tot}}}$ is the input-referred noise density of $H0$ and BW_{EN} is the equivalent noise bandwidth of the impedance sensor. As A_{CL} is no longer much greater than unity at high frequency in this case due to the resistive impedance component, the output SNR will degrade based on the series capacitance ratio between Z_{IN} and Z_{F}. As the series capacitance for a micron-size particle is smaller than 100 fF [19], in order to avoid SNR degradation at high frequency using purely capactive feedback, one must implement C_{f} <10 fF, which is impractical due to minimum unit capacitors in CMOS processes as well as parasitic capacitances.



(a) (b)

Figure 2.4: Closed-loop gain A_{CL} frequency response when feedback element is (a) capacitor (b) capacitor series with resistor, assuming loop gain is sufficient.

In this work, to overcome the limitations of capacitive feedback for resistive sensor inputs, a resistor R_{F} is added in series with C_{F} in the feedback loop (Z_{F}) to maintain closed-loop gain at high frequency. High gain across frequency is necessary to leverage the benefits afforded by source-differential impedance sensing; as described in Sec. 2.2.1, an important feature of source-differential sensing is the small input difference current following baseline cancellation, which enables a high-gain downstream measurement system without input saturation due to baseline current. The resulting frequency response is shown in Fig. 2.4b, where R_{f} =10 MΩ. Due to this always-high closed-loop gain, the thermal noise introduced by adding R_{f} is mitigated and has negligible effect on output SNR.

2.3 System Analysis

2.3.1 Loop dynamic analysis

A system loop dynamic analysis is essential to translate system specifications such as bandwidth and noise into individual block specifications and design targets. In order to simplify this analysis, we assume that H_{LPF} is the transfer function of the low-pass filter (DC gain of low-pass filter is assumed to be unity), and the remaining combined gain from the low-noise pre-amplifier, down-converter, intermediate gain stage, and up-converter are lumped into $A_0(s)$. The loop gain of the feedback system can then be written as

$$LG(s) \approx A_0(s)\beta(s)H_{\mathrm{LPF}}(s - jw_{\mathrm{m}}) = \frac{A_0(s)\beta(s)}{1 + \frac{s - jw_{\mathrm{m}}}{p_{\mathrm{LPF}}}} \tag{2.4}$$

where w_{m} is the modulation frequency in radians, β(s) is the feedback factor based on Z_{IN} and Z_{F}, and p_{LPF} is the frequency of the low-pass pole generated by the integrator. Note that the $H_{\mathrm{LPF}}(s + jw_{\mathrm{m}})$ component arising from modulation is omitted due to its negligible effect on LG at frequencies of interest. Therefore, the closed-loop gain A_{CL} can be obtained as an extension of (2.1),

$$A_{\mathrm{CL}}(s) \approx \frac{Z_{\mathrm{F}}(s)}{Z_{\mathrm{IN}}(s)} \frac{1}{1 + \frac{s - jw_{\mathrm{m}}}{p_{\mathrm{LPF}}|LG_0(s)|e^{j\theta}}} \tag{2.5}$$

where $LG_0(s)$ is the loop gain product $A_0(s)\beta(s)$ without H_{LPF} shaping, and θ is the phase shift of LG_0 at each frequency.

In the ideal case where all blocks have infinite bandwidth, $LG_0(s)$ exhibits purely

DC behavior with DC gain of $LG_{0,\mathrm{DC}}$, and no phase shift is introduced. If $Z_{\mathrm{IN}}(s)$ and $Z_{\mathrm{F}}(s)$ are also frequency-independent at bands of interest, maximum A_{CL} is obtained at w_{m} with a 3-dB bandwidth (BW) calculated as

$$BW = p_{\mathrm{LPF}} LG_{0,\mathrm{DC}}. \tag{2.6}$$

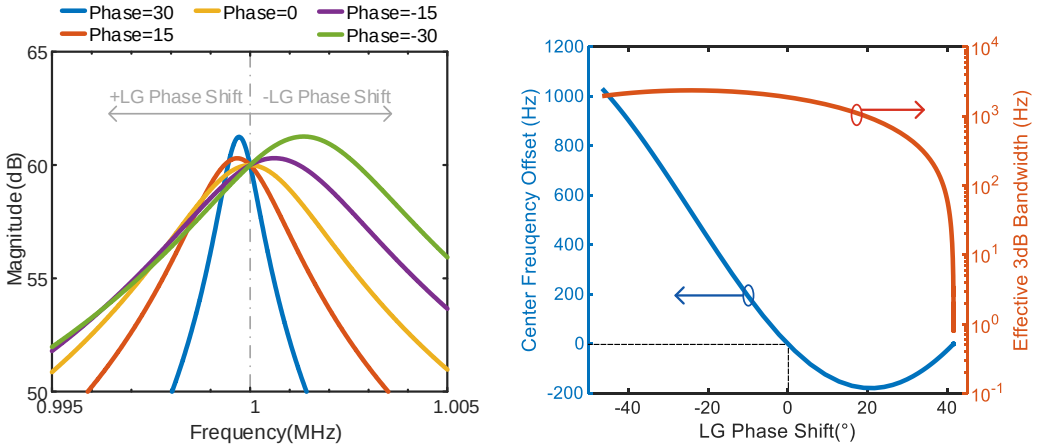
However, in practice, especially for high modulation frequencies, $LG_0(s)$ exhibits a phase shift due to finite high-pass and low-pass cut-off frequencies in the signal chain, which leads to a scenario where

$$\left| 1 + \frac{j(w_{\mathrm{c}} - w_{\mathrm{m}})}{p_{\mathrm{LPF}} |LG_0(jw_{\mathrm{c}})| e^{j\theta}} \right| < 1, \tag{2.7}$$

increasing the peak closed-loop gain A_{CL} greater than $Z_{\mathrm{F}}/Z_{\mathrm{IN}}$ and shifting the peak gain center frequency w_{c} away from w_{m}.

A system model was implemented in MATLAB to illustrate this behavior. As shown in Fig. 2.5a, the simulated closed-loop gain frequency response varies for different loop gain phase shifts. The simulation is performed for modulation frequency f_{mod}=1 MHz and assuming a feedback factor β of 1/1000.

If LG_0 exhibits no phase shift ($\theta = 0$), the center frequency w_{c} remains at modulation frequency w_{mod} with peak gain at w_{mod} ($w_{\mathrm{mod}} = 2\pi f_{\mathrm{mod}}$). If θ is positive (e.g. a zero near f_{mod}), w_{c} moves downward in frequency, and effective bandwidth for A_{CL} is reduced. If θ is negative (e.g. pole near f_{mod}), w_{c} moves upward in frequency and bandwidth increases slightly. Fig. 2.5b describes the detailed relationship between center frequency offset relative to f_{mod}, as well as effective 3 dB bandwidth as



(a) (b)

Figure 2.5: (a) Frequency response of system closed-loop gain, A_{CL}, at different LG_0 phase shift θ conditions when f_{mod}=1 MHz; (b) center frequency shift and effective 3-dB bandwidth at different loop-gain phase shifts.

a function of LG_0 phase shift, θ.

It is important to note that the signal gain is fixed by the closed-loop gain A_{CL} at f_{mod}, which is equivalent to baseband output DC gain following demodulation; this remains unaltered for non-zero θ. However, system bandwidth and noise gain are determined by θ, requiring specific design optimization for θ anticipated at a certain f_{mod}; this is discussed in detail in the following section.

The effect can also be seen in (2.3), where A_{CL} is fixed and independent of θ (e.g. 60 dB), but the effective noise bandwidth (BW_{EN}) changes as a function of θ (Fig. 2.5).

2.3.2 Noise analysis

The noise performance of the impedance sensor is critical for cytometry applications, where it directly determines the limit of detection (LOD). Comprehensive noise analysis of transimpedance amplifiers for low-current measurement applications has been discussed in previous literature [20, 21], but without considering the amplifier non-idealities. For the closed-loop architecture shown in Fig. 2.3, if we assume LG is sufficiently high and R_f dominantes Z_F at frequencies of interest, the closed-loop noise gain and input-referred noise current density can be derived as

$$\begin{aligned}\overline{i_\mathrm{n}^2} &\approx \frac{\overline{v_\mathrm{n,tot}^2}\cdot|A_\mathrm{CL}(s)|^2+4kTR_\mathrm{f}}{R_\mathrm{f}^2}\\ &\approx \overline{v_\mathrm{n,tot}^2}\left|\frac{1}{Z_\mathrm{IN}}\right|^2\left|\frac{1}{1+\frac{s-jw_\mathrm{m}}{p_\mathrm{int}|LG_0(s)|e^{j\theta}}}\right|^2+\frac{4kT}{R_\mathrm{f}}\end{aligned} \tag{2.8}$$

where Z_IN is the impedance of the input sensing element, typically dominated by input parasitic capacitance if the input is floating, and $\overline{v_\mathrm{n,tot}^2}$ is the input-referred noise voltage density of $H0$. Note $\overline{i_\mathrm{n}^2}$ in (2.8) is the input-referred noise current of the high frequency output $V_\mathrm{O,HF}$, which is treated as equivalent to its demodulated output counterpart in our analysis assuming unity-gain of the up-converter.

Equation (2.8) shows that the input-referred noise density is shaped by the band-pass characteristics of the signal chain, which are in turn dependent on θ. As such, loop gain phase shift θ not only causes bandwidth deviation (Fig. 2.5), it also directly impacts the SNR of impedance sensor, as noise bandwidth varies even with unaltered signal gain. Additionally, peak gain of A_CL will vary as well, resulting in a change

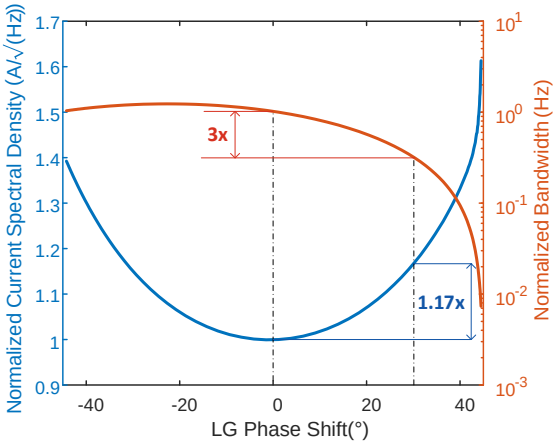


Figure 2.6: Normalized input-referred noise current spectral density and noise bandwidth versus LG_0 phase shift θ when f_{mod}=1 MHz.

in integrated noise.

To better illustrate this tradeoff, one can analyze the noise density as a function of θ rather than integrated noise, as bandwidth changes with phase shift as well. In Fig. 2.6, a simulation shows how loop gain phase shift θ effects the equivalent input-referred noise current spectral density and bandwidth; both are normalized to $\theta = 0$ condition. The best noise performance is obtained with $\theta = 0$, as expected. Of note, for positive θ, the noise bandwidth will decrease faster than the noise density increases, which provides a design opportunity to trade noise density for overall noise if a narrow bandwidth is difficult to implement. For instance, a +30° loop gain phase shift introduces a 1.17X increase in current spectral density and 3X reduction in bandwidth, leading to an effective 1.5X reduction in rms noise.

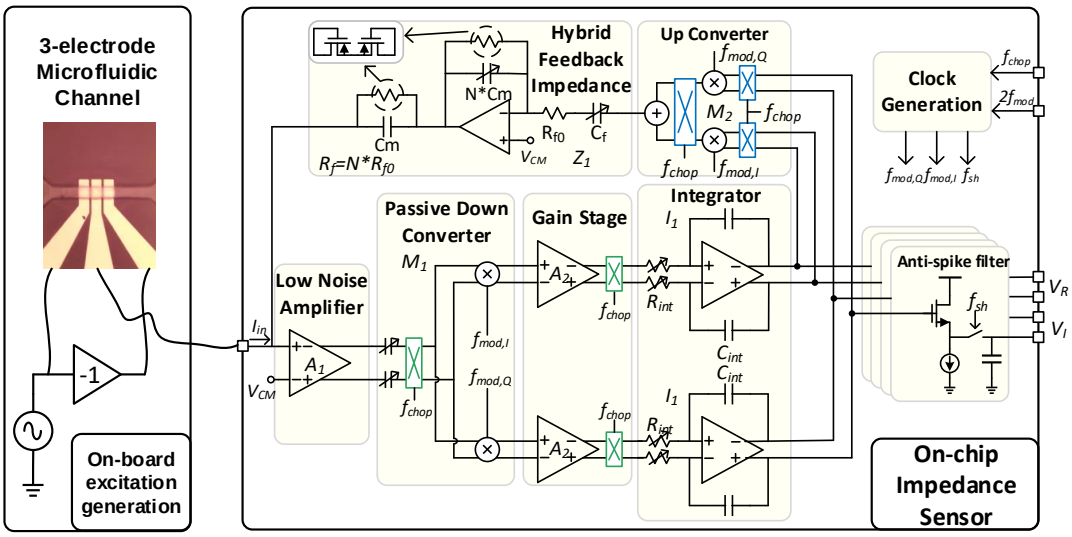


Figure 2.7: High-level source-differential architecture of on-chip hybrid-feedback impedance sensor and off-chip microfluidic flow channel.

2.4 Circuit Implementation

2.4.1 System overview

Fig. 2.7 depicts the high-level architecture of the CMOS-integrated impedance sensor readout electronics, as well as a microfluidic flow cell using a source-differential excitation scheme. The impedance sensor loop consists of a low-noise input buffer (A_1), a quadrature passive down-converter (M_1) for demodulation, gain stages (A_2) and integrators (I_1) in both IQ channels, an quadrature up-converter (M_2), and hybrid feedback impedance (Z_1) including an active feedback resistor in series with capacitor C_f. An anti-spike low-pass filter is used to remove high-frequency chopper artifacts, and modulation clock and chopping clock are provided externally.

As V_R and V_I are the extracted baseband real and imaginary voltage components, input current components are derived as

$$I_{\text{in,R(I)}} = V_{\text{R(I)}}/(R_f + \frac{1}{2\pi f C_f}). \tag{2.9}$$

Note that (2.9) assumes zero phase shift in the loop at f_{mod}, otherwise $I_{\text{in,R(I)}}$ should be calibrated by the phase shift, while magnitude remains the same. Any DC offset or harmonics generated by f_{mod} and f_{chop} will remain in the loop and be amplified until reaching the low-pass integrator, which may saturate certain stages and limit the dynamic range of the loop [17]. As this design employs a square-wave modulation source and does not include a dedicated bandpass filter around the modulation frequency, this issue must be addressed. Here, a current-driven passive down converter is adopted to enhance the dynamic range, and an active-feedback resistor is used to achieve high impedance (up to 10 MΩ) over a wide frequency range, without attenuation due to parasitic capacitance.

The noise performance of the impedance sensor can be obtained from (2.8), where $\overline{v_{\text{n,tot}}^2}$ referred to the input of A_1 can be approximated as

$$\begin{aligned}\overline{v_{\text{n,tot}}^2} \approx \overline{v_{\text{n,A1}}^2} + \frac{\overline{v_{\text{n,M1}}^2}}{G_{\text{A1}}^2} + \frac{2\overline{v_{\text{n,A2}}^2}}{G_{\text{A1}}^2 G_{\text{M1}}^2} + \frac{2\overline{v_{\text{n,I1}}^2}}{G_{\text{A1}}^2 G_{\text{M1}}^2 G_{\text{A2}}^2} \\ + G_{\text{M2}}^2 (\frac{Z_{\text{IN}}}{Z_{\text{IN}} + Z_{\text{F}}})^2 \overline{v_{\text{n,M2}}^2}\end{aligned} \tag{2.10}$$

where $\overline{v_{\text{n,A1}}^2}$, $\overline{v_{\text{n,M1}}^2}$, $\overline{v_{\text{n,A2}}^2}$, $\overline{v_{\text{n,I1}}^2}$, $\overline{v_{\text{n,M2}}^2}$ are the equivalent input voltage noise spectral density of A_1, M_1, A_2, I_1, M_2 and Z_1, referred to input modulation frequency. The

noise contribution of the feedback impedance can be treated as the equivalent thermal noise of $R_{\mathrm{f,eq}}$, which is included in (2.8). From (2.10), the total input-referred noise voltage ($2.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ from simulation) is mainly dependent on the noise performance of the input low-noise amplifier A_1 ($1.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 1.4 mA) and the second stage down-converters M_1 ($5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 0.225 mA) attenuated by G_{A1}=25. The noise from gain stage A_2 ($21\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 0.12 mA) and integrator I_1 ($557\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 0.1 mA) are effectively reduced by the previous gain of A_1 and M_1. Due to high transimpedance gain provided by the feedback impedance, the noise contribution of up-converter M_2 ($450\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, 2.5 mA) is insignificant when referred to the input. Two chopper sets are utilized to reduced the flicker noise contribution of M_1, A_2, and M_2. Chopping frequencies range from 75 kHz to 300 kHz based on the modulation frequency f_{mod}. The flicker noise from input amplifier A_1 and the active feedback resistor are less critical for overall noise performance due to the non-DC signal frequency of interest (f_{mod}).

2.4.2 Low-noise amplifier and passive down-converter

Fig. 2.8 shows a combined schematic of the low-noise input amplifier A_1 and the capacitive-coupled passive down-converter M_1. As discussed in the previous section, the noise performance of the impedance sensor is primarily dominated by the A_1. Therefore, a 1.2 mA bias current is used to reduce the input noise as low as $1.9\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Cascode transistors are added to shield the input virtual ground from subsequent chopping operation. Due to output capacitive-coupling to the next stage,

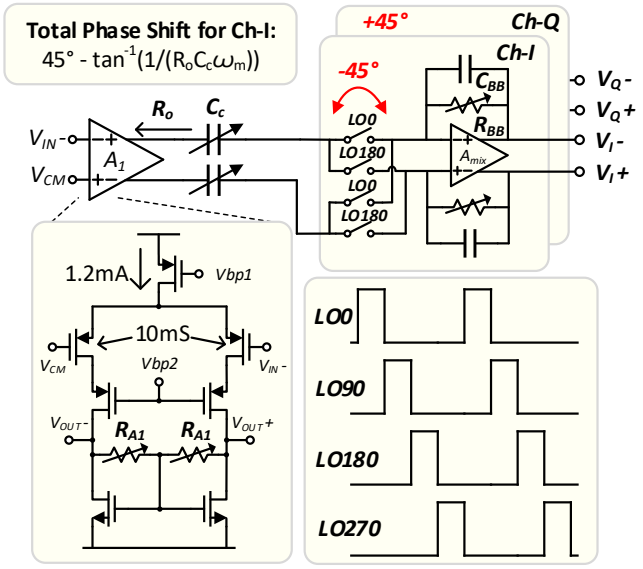


Figure 2.8: Schematic of low-noise input amplifier and capacitive-coupled current-mode passive down-conversion mixer driven by 25% duty cycle f_{mod} (chopper is not shown for simplicity).

a simple resistive CMFB sets the output common mode voltage. R_{A1} is adjustable for tuning the output resistance, R_0.

A current-mode passive down-conversion mixer [22] is used, providing multiple advantages: the capacitor C_{C} decouples any DC offset voltage at the output of A_1 introduced by DC leakage current, and, operating in current mode, the amplifier combined with the mixer has enhanced dynamic range to handle large harmonic components fed back from the up-conversion mixer. A 25% duty-cycle modulation clock is chosen for its superior linearity and noise performance to 50% duty-cycle modulation clock. The modulation clock f_{mod} is generated using an on-chip flip-flop driven by an external $2f_{\mathrm{mod}}$ clock that is synchronized with the off-chip source-differential excitation source. The combined conversion gain and phase shift including

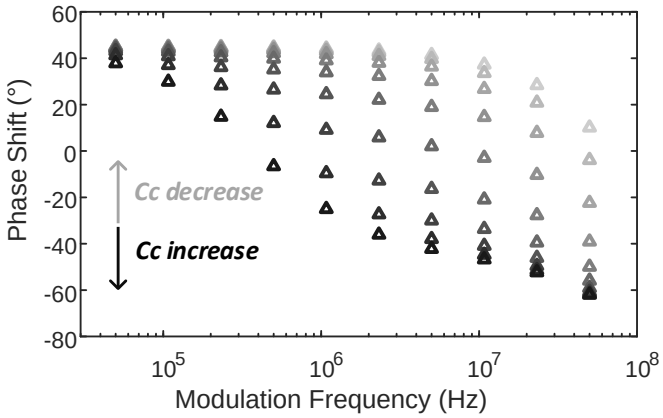


Figure 2.9: Phase shift coverage of A_1 and M_1 across 50 kHz to 50 MHz for given 50 fF and 15 pF C_c.

A_1 and M_1 at modulation frequency can be respectively derived as

$$A_{\text{LNA+Mixer}} = \frac{\sqrt{2}}{\pi} \frac{R_o}{\sqrt{Z_c^2 + R_o^2}} g_{m,A1} R_{BB} \tag{2.11}$$

$$\theta_{\text{LNA+Mixer}} = 45^\circ - \tan^{-1}\left(\frac{1}{R_o C_c \omega_m}\right) \tag{2.12}$$

where Z_c is the equivalent impedance of C_c at frequency ω_m, and $g_{m,A1}$ is the transconductance of A_1. As is described in (2.12), a 25% duty cycle clock introduces a -45° phase shift to the loop path, which requires a $+45^\circ$ phase shift compensated by R_o and C_c to obtain $\theta_{\text{LNA+Mixer}} = 0$, as required for optimal noise performance of the overall feedback loop, as discussed in Sec. 2.3. C_c can also be used to tune the overall LG phase to compensate for any other phase shift created in the loop. The nominal $+45^\circ$ phase shift created by R_o and C_c provides the additional benefit of sensitive phase shift tuning using a small C_c value over a wide range of operating frequency, f_{mod}.

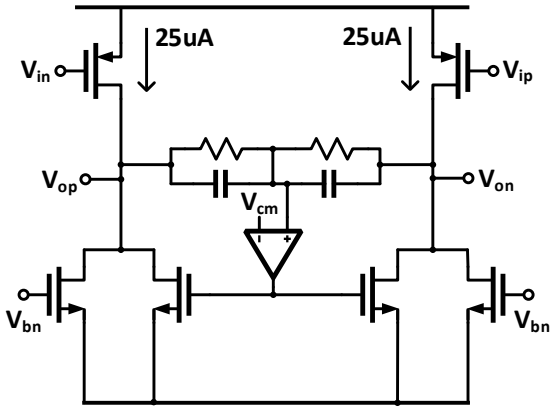


Figure 2.10: Schematic of the amplifier in integrator I_1.

To address a wide range of f_{mod}, C_{c} is implemented as a capacitor bank with a fine tuning step of 100 fF and a coarse tuning step of 1 pF, providing capacitance values from 50 fF to 16 pF. Fig. 2.9 shows the combined phase offset coverage from A_1 and M_1 for this adjustable C_{c} across frequency. Over the expected nominal operating frequency range from 1 MHz to 10 MHz, this provides broad coverage from phase -40° to 40°. The combined gain of A_1 and M_1 is adjustable from 45-55 dB using 4-step R_{BB} tuning.

2.4.3 Gain Stage and Integrator

Gain stage A_2 is implemented as a single-stage common-source amplifier with a resistive load and inserts 20 dB gain between mixer and integrator, reducing the noise contribution from the large resistor R_{int}. The integrator determines the closed-loop bandwidth of the impedance sensor, controlled by R_{int} and C_{int}. In this design, R_{int} is selectable as 1 MΩ or 10 MΩ to accommodate both high-resolution and high-speed applications, and C_{int} is 16 pF. Fig. 2.10 shows the transistor-level schematic of

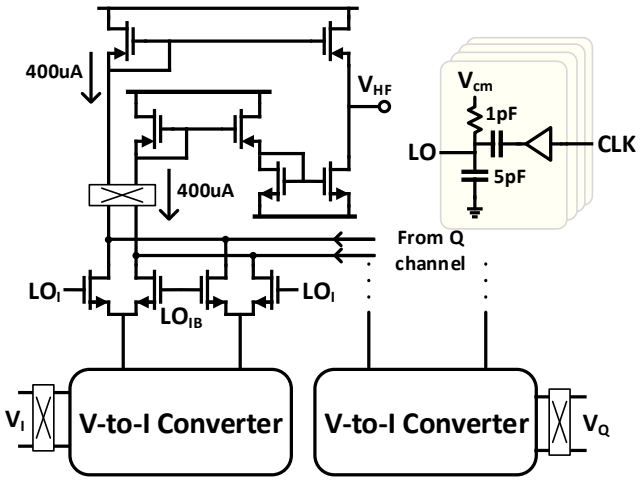


Figure 2.11: Schematic of up-conversion mixer M_2.

the integrator amplifier. A pseudo-differential common-source amplifier is adopted for its wide output voltage range, and input PMOS transistors are sized with long channel length to reduce flicker noise. The amplifier provides DC gain of 25 dB with UGB=15 MHz and consumes 75 µA, including CMFB.

2.4.4 Up-conversion mixer and hybrid feedback impedance

A quadrature up-conversion mixer upconverts the demodulated signal for closed-loop feedback operation. The topology of the converter is similar to [17], including a highly linear V-to-I converter [23], a quadrature Gilbert-cell driven by a 300 $\mathrm{mV_{pp}}$ square wave, and a current summation stage implemented using a current mirror. Chopping is used to mitigate flicker noise from the input transistors in the V-to-I converter.

The feedback element Z_1 (Fig. 2.7) must remain high impedance at high f_{mod} operation to maintain closed-loop gain, which is realized by resistance R_{f}. As imple-

menting a large resistance (>1 MΩ) at megahertz frequencies is challenging due to parasitic capacitance, an active resistor is implemented by a capacitive current divider with selectable capacitor ratio (1/5/50) to boost physical resistor R_{f0} (200kΩ), providing variable resistance (10MΩ/1MΩ/200kΩ). Pseudo-resistors provide a DC path in the active resistor, as well as input virtual ground for the input low-noise amplifier. Note we expect less than 100 pA input DC current due to the double layer capacitor from electrode-electrolyte interface.

The amplifier in the active feedback path is implemented as a two-stage amplifier with Miller compensation and consumes 500 µA current, supporting resistance multiplication up to 100 MHz. The capacitor C_f not only couples signal from the up-conversion mixer, but it also serves as the dominant feedback impedance when f_{mod} is low. C_f is adjustable from 100 fF to 3 pF, and it should be carefully chosen based on desired feedback impedance at the desired operating frequency, f_{mod}.

2.5 Verification and Measurement Results

This impedance sensor IC was fabricated in a 0.18 µm CMOS process and occupies 400 µm×700 µm area; a die photo is shown in Fig. 2.12. The chip operates from a 1.8 V supply, and modulation and chopping clocks are applied externally. A custom test PCB incorporates an FPGA module (Opal Kelly XEM6310) for providing adjustable chopper frequency and static digital controls to the chip, and a low-noise analog op-amp (ADA4896) is included for buffering differential I/Q analog outputs. An audio precision analyzer (Audio Precision APx555) is used to analyze

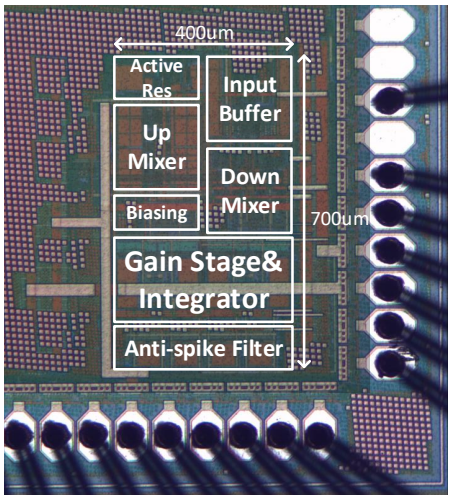


Figure 2.12: Micrograph of the fabricated 0.18 μm CMOS impedance sensor IC.

the demodulated I/Q output spectrum. Total average current consumption of the impedance sensor operating at f_{mod}=1 MHz is measured at 5.4 mA, including analog and digital power supplies at 1.8 V.

2.5.1 Electrical characterization of impedance sensor IC

Standalone electrical characterization of the impedance sensor IC was performed using a model cell with 10 kΩ resistance, representing channel resistance, in series with 10 nF capacitance representing double-layer capacitance (Fig. 2.13); while larger than a typical double-layer capacitance seen in practice, 10 nF ensures that the resistance value is dominant at frequencies of interest for the purposes of IC characterization. A 2 $\mathrm{mV_{pp}}$ sine wave input with frequency $f_{\mathrm{mod}}+\Delta f$ is input through the model cell to the impedance analyzer with synchronized f_{mod} as the modulation frequency. The demodulated sine wave output with frequency of Δf is analyzed to acquire the

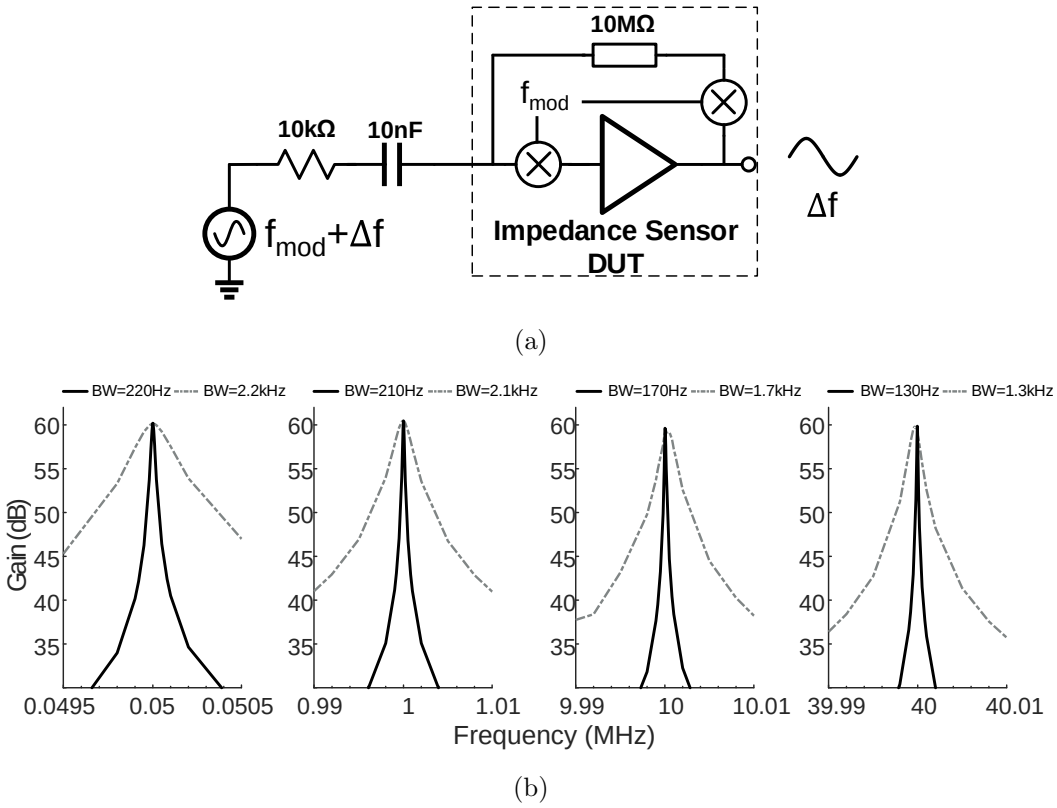
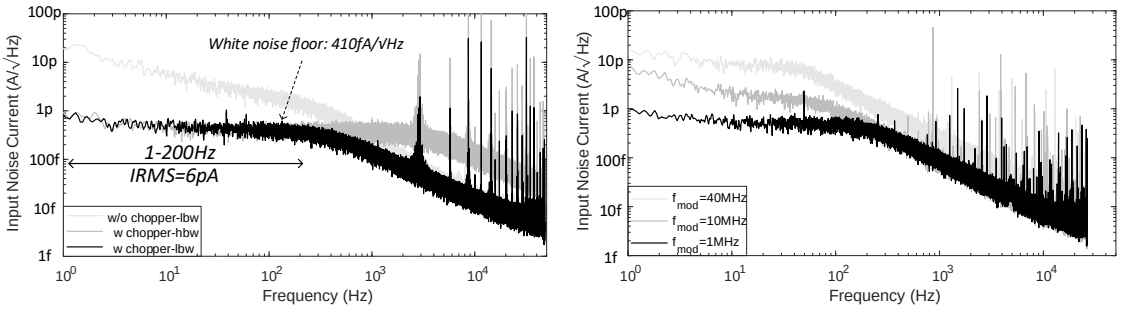


Figure 2.13: (a) Measurement setup using a model cell for voltage gain transfer function of impedance sensor, and (b) measured voltage gain transfer function at different f_{mod} (0.05/1/10/40MHz) using low and high bandwidth modes.

voltage transfer function. Measured closed-loop voltage transfer functions are shown in Fig. 2.13b for modulation frequencies of 50 kHz, 1 MHz, 10 MHz, and 40 MHz, evaluated with $R_{f,eq}$ set to 10 MΩ for a expected gain of 60 dB; measured gain of 59 dB with ±1 dB accuracy is obtained for all f_{mod} values. A consistent closed-loop 3-dB bandwidth of approximately 200 Hz in low-bandwidth mode (R_{int}=10 MΩ) and 2 kHz in high-bandwidth mode (R_{int}=1 MΩ) is obtained across 50 kHz-40 MHz. Note C_c is adjusted correspondingly with f_{mod} to avoid gain and frequency offset variations.

A key metric for an impedance sensor is its noise performance, which determines



(a) (b)

Figure 2.14: (a) Input-referred noise current spectral density when f_{mod}=500 kHz (Both chopper on and off; low-bandwidth and high-bandwidth cases are shown for comparison) (b) Input-referred noise current spectral density when f_{mod}=1 MHz, 10 MHz and 40 MHz.

achievable impedance measurement sensitivity and limit of detection. In this work, comprehensive noise performance of the impedance sensor IC at different frequencies was measured and analyzed. Output noise voltage spectral density was measured using an audio analyzer with the sensor input open, with only parasitic capacitance present. The audio analyzer internal ADC sampling frequency was set to 96 kHz, using a 1.2M-point FFT. The input-referred noise current spectral density is calculated as measured output voltage spectral density divided by mid-band gain.

Fig. 2.14a shows the noise performance of the impedance sensor down to 1 Hz, operating at $f_{\mathrm{mod}} = 0.5$ MHz. The current spectral density of both low-bandwidth and high-bandwidth modes are shown, demonstrating a noise floor of 410 fA/$\sqrt{\mathrm{Hz}}$. The measured noise floor under-performs the expected simulation results due to the parasitic capacitance introduced at the input node of the impedance sensing IC by the bond pad, IC packaging, and PCB. The noise performance without the chopper is shown as well, which demonstrates that the 75 kHz chopping frequency effectively

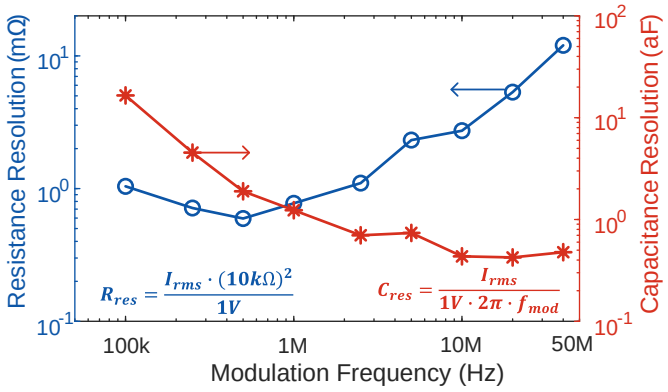
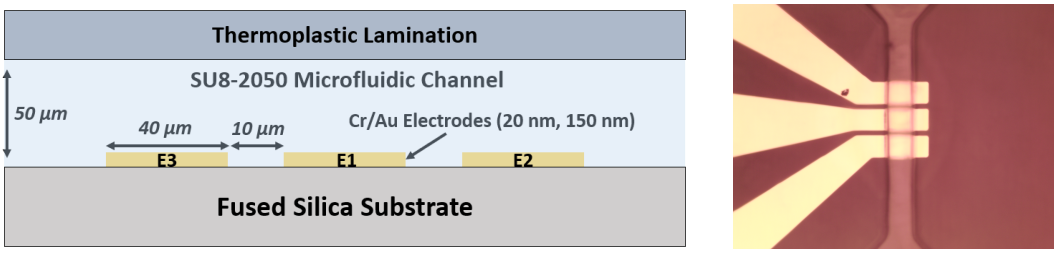


Figure 2.15: Effective resistance and capacitance measurement resolution across modulation frequency calculated from the input-referred rms current noise over 200 Hz bandwidth, when input voltage amplitude is 1 V.

reduces the flicker noise contribution frequency by more than 10X near DC. The input rms current at 0.5 MHz f_{mod} is calculated as 6 pA from 1 to 200 Hz for the given spectral density.

To investigate the noise performance at high frequency, the input-referred noise current spectral density at $f_{\text{mod}} = \{1, 10, 40\}$ Mhz and 300 kHz chopping frequency is shown in Fig. 2.14b. As expected, the noise increases at higher modulation frequencies, as the input parasitic capacitance decreases effective input impedance. The input-referred resistance and capacitance measurement resolution at different modulation frequencies is calculated from the input-referred rms current noise over 200 Hz bandwidth and presented in Fig. 2.15, assuming an input voltage amplitude of 1 V and a nominal input resistance of 10 kΩ. The minimum resistance resolution is achieved as 0.6 Ω at 0.5 MHz modulation frequency; this is limited primarily by the input-referred noise current below 500 kHz modulation frequency due to the maximum C_c value (16 pF). The minimum calculated capacitance measurement resolution



(a) (b)

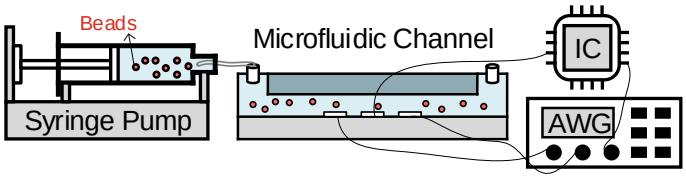
Figure 2.16: (a) Illustrated cross-section and (b) top view micrograph of fabricated microfluidic flow channel with 3-electrode sensor used in experiments.

achieved is 0.42 aF at 20 MHz.

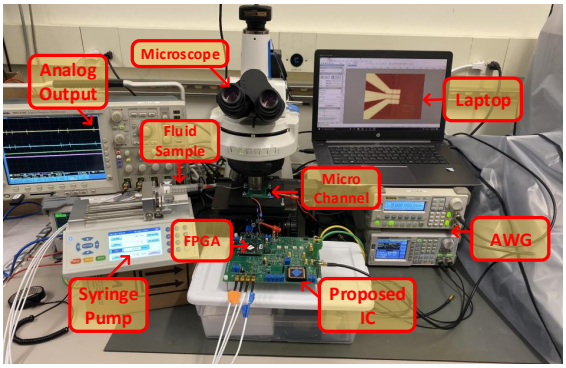
2.5.2 Microfluidic flow cell design and fabrication

A microfluidic flow cell was fabricated for testing the impedance cytometer, as shown in Fig. 2.16. Electrodes were lithographically defined and deposited (20/150 nm Cr/Au) on fused silica wafers. Following electrode fabrication, the chamber layer of the microfluidic channel was patterned using a 50 µm spin-coated layer of SU8-2050 (MicroChem). The microfluidic channel was sealed with a thermoplastic laminating process, and fluid ports were installed. As fabricated, the channel width and height are each 50 µm, and electrodes are 40 µm wide with 10 µm spacing.

After fabrication, the flow cell was fixtured to ensure reliable electrical contact between the electrodes and the IC, where pogo pins in contact with the flow cell wafer and connect by wire to the IC test PCB.



(a)



(b)

Figure 2.17: Illustration (a) and photograph (b) of experimental test setup for evaluating the impedance sensor IC with a microfluidic flow cell, including electrical, optical, and fluidic interfaces.

2.5.3 Flow cytometry measurement using micro-beads

The impedance cytometry IC and microfluidic flow cell were used in conjunction for a system-level demonstration of the complete sensor system; the experimental setup is shown in Fig. 2.17. Two differential anti-phase 1 MHz, 500 mV_{pp} excitation AC voltages were applied to the two outer electrodes, and a synchronized 2 MHz clock signal was supplied to the IC for lock-in operation. The resulting differential current through the middle electrode was measured by the impedance sensor with $R_{f,eq}$=10 MΩ and BW=200 Hz. It is important to note that due to any fabrication-related mismatch of the electrodes and the high gain of the impedance sensor, there will be a DC offset voltage at the impedance sensor output, which can limit the

measurement dynamic range. To address this, calibration is performed by adjusting the relative phase and amplitude of the excitation sources slightly to balance the source-differential excitation and compensate for any offset; this is typically less than $\pm 1^\circ$ from the ideal 180° source-differential offset.

For a fluid sample, micron-scale polystyrene beads (Polysciences) were suspended in 1X phosphate-buffered saline (PBS) solution and injected into the flow cell at 0.3 µL/min using a syringe pump. A microscope was used with attached camera is used to record video of the flow channel, providing synchronized optical verification of the electrical measurement. The differential analog I/Q voltage output of the impedance sensor was recorded at 2.5 kHz sampling rate by the oscilloscope and post-processed in MATLAB.

Dilute solutions of monodisperse beads were prepared to analyze single-cell resolution; a typical measured transient waveform is shown in Fig. 2.18 as a 10 µm diameter bead transits across the electrode. Three microscope images corresponding to the A, B, C moment in the transient waveform are provided, as a flowing bead enters the electrode set, in the middle of electrode set, and leaving the electrode set, respectively. Only the real component of the voltage recorded from the middle (I channel) electrode is plotted, as channel resistance change is dominate at this mid-band modulation frequency (1 MHz). From Fig. 2.18, the peak voltage change obtained is 0.9 V for a 10 µm bead passing electrodes, corresponding to a 9 Ω resistance change of approximately 5 kΩ static channel resistance (measured separately by the impedance analyzer chip using 1X PBS in the absence of poly beads).

Multiple measurements using 3 µm, 5 µm, and 10 µm diameter bead solutions

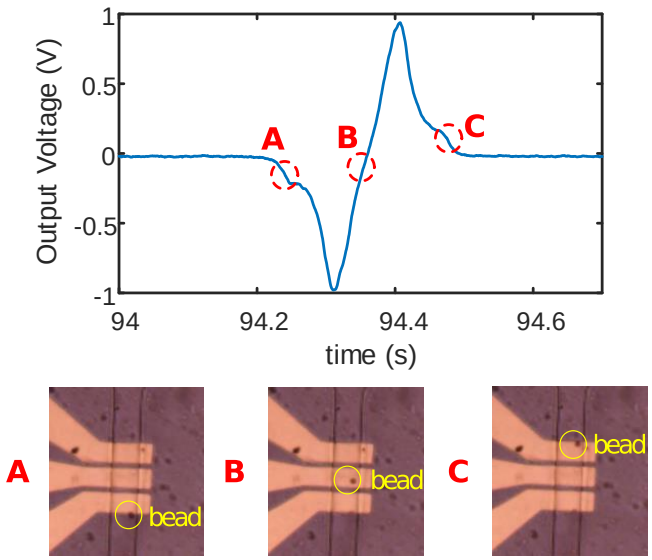
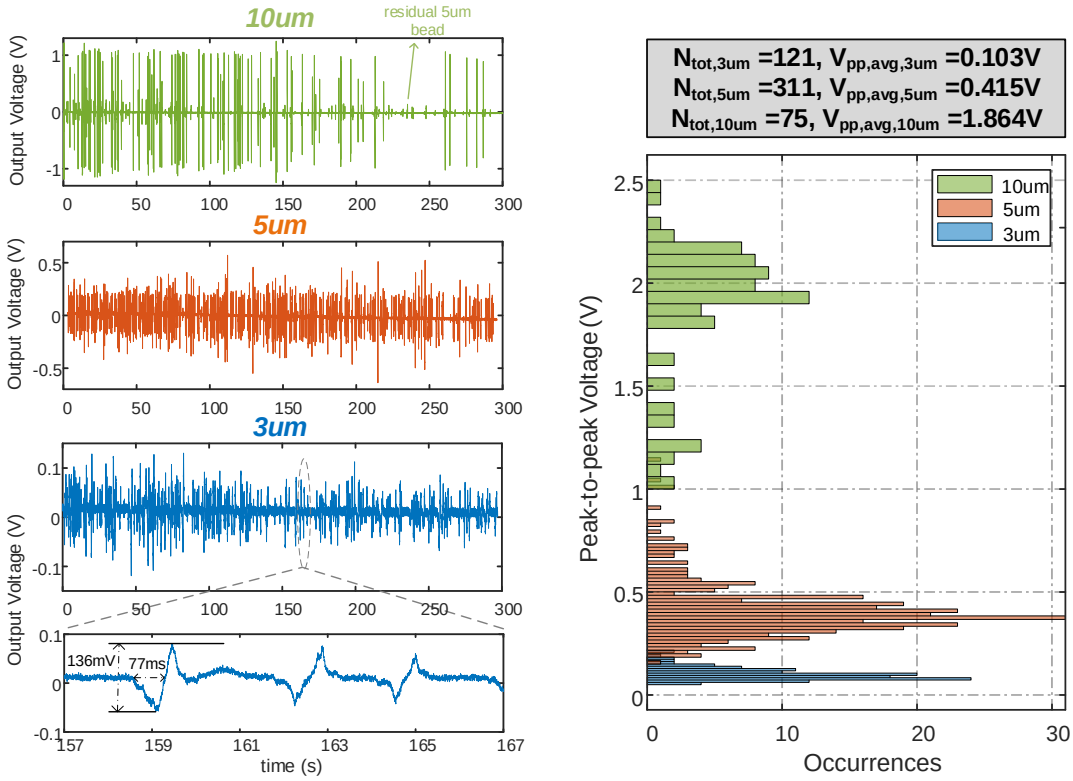


Figure 2.18: Measured voltage transient signal real component (I-channel) shown above real-time microscope images taken when a single 10 µm bead is transiting across the electrodes.

were performed to assess the resolution and size separation capability of proposed cytometer, and Fig. 2.19a shows measured transient results for a 5 minute recording of each sample solution. As in Fig. 2.18, only the real voltage component (I-channel) is shown and analyzed. The output voltage amplitude is relatively consistent for each crossing event for a given bead size, and it scales down as the bead size decrease, as expected.

A zoomed transient plot for the 3 µm bead measurement is also shown in Fig. 2.19a for analysis of detection limit of the proposed cytometry technique. The measured peak-to-peak voltage of given single-bead event is 136 mV, and the measured rms noise from the transient recording is approximately 3 mV. Approximating the crossing response waveform as sinusoidal, this yields a high detection signal-to-noise ra-



(a) (b)

Figure 2.19: (a) Measured 5-minute transient waveforms using the impedance-based sensor IC and a custom microfludic flow cell for flowing solutions of 3 µm, 5 µm, and 10 µm polymer microbeads, and (b) the peak-to-peak voltage histogram of each single-cell event, demonstrating clear separation by particle size.

tio (SNR) of 24 dB for 3 µm bead size. The response time for single bead event in this measurement is around 150 ms, corresponding a throughput of less than 10 beads/second. However, note that this experimental set uses an intentionally low flow rate for unambiguous single-bead verification, which is not limited by the actual impedance sensor bandwidth (200/2000 Hz).

Fig. 2.19b shows the peak-to-peak voltage histogram of 3 µm, 5 µm, and 10 µm particle measurements from the transient recordings in Fig. 2.19a. Due to the ex-

perimental measurement sequence, residual 5 µm beads remain in the channel during the 10 µm bead, which is annotated in Fig. 2.19a and confirmed in the associated microscope video recording. These events, as well as simultaneous multi-bead events, are excluded from the histogram in order to analyze isolated, single-bead peak-to-peak voltage distrubution. A distinct separation from 3 µm, 5 µm and 10 µm group is shown in the histogram.

The average peak-to-peak voltage for 3 µm, 5 µm, and 10 µm beads in Fig. 2.19b is 0.103 V, 0.415 V, and 1.8164 V, respectively, which matches the approximation that channel resistance change is proportional to the square of particle diameter, corresponding to change in cross-sectional area presented between the electrodes. These average peak-to-peak voltage amplitudes indicate channel resistance changes of 9.3 Ω, 2.1 Ω, and 0.5 Ω atop the nominal 5 kΩ channel resistance for 10 µm, 5 µm, and 3 µm beads, respectively. Assuming an approximately square relationship of signal amplitude with particle diameter along with the measured noise floor, the proposed impedance-based cytometer IC can achieve sub-1 µm cell diameter limit of detection.

Also visible in in Fig. 2.19b, deviation in peak-to-peak amplitude for a given bead size is due primarily to the nonuniform flow velocity profile in a microfluidic channel, where particles near the center move at higher velocity even under constant flow rate, as well as the random vertical position of a bead in the microfluidic channel as it crosses the electrodes. In future work, hydrodynamic focusing, such as sheath flow, can be used in the flow cell to decrease this distribution and further improve cell diameter measurement resolution.

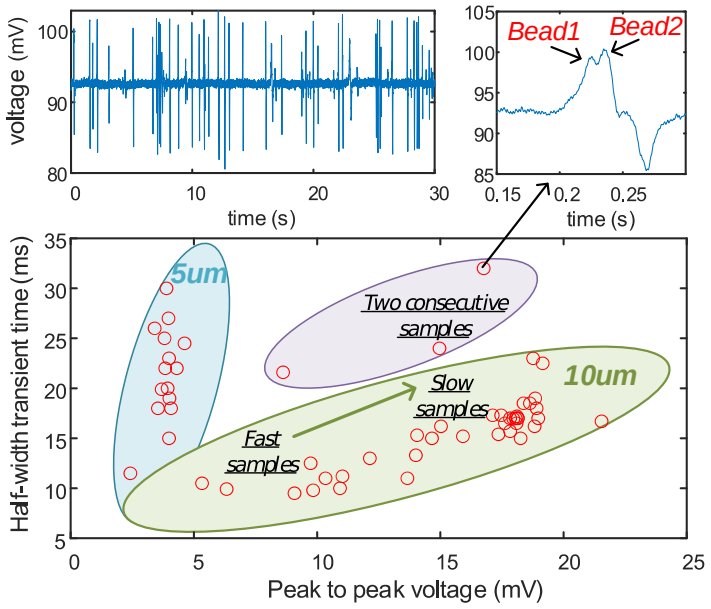


Figure 2.20: Measured voltage output V_{pp} versus half-width time; data extracted from 30s recording of 5/10 µm bead mixture.

Fig. 2.20 demonstrates single-cell measured resolution results from a recording of polydisperse beads using a 5 µm/10 µm diameter sample mixture. For this measurement, the flow rate is 1 µL/min and the impedance sensor gain is 100 kΩ. The peak-to-peak voltage and half-width time (FWHM) of each positive peak are extracted from the transient waveform. As shown, the 5 µm group (blue) and 10 µm group (green) can be clearly separated.

A comparison of the presented sensor system with related impedance-based CMOS sensor ICs is provided in Table 2.1, demonstrating state-of-the-art noise, power, and circuit area performance metrics for commensurate resolution. Specifically, this work achieves sub-attofarad capacitive resolution at megahertz modulation frequencies with considerable reduction in power consumption.

Table 2.1: Performance comparison with impedance sensor

References	**This work**	JSSC'14 [17]	TBCAS10 [15]	ISSCC'09 [14]	TBCAS'12 [16]	JSSC'16 [24]
Technology	**0.18 µm**	0.35 µm	0.35 µm	0.35 µm	0.13 µm	65 nm
Application	**Flow cytometry**	Capacitive sensing	DNA detection	Low current measurement	DNA detection	Flow cytometry
Topology	**Mod/demod**	Mod/demod	Lock-in	Lock-in	Dual-slope ADC	Oscillator-based
Frequency Range	**50k-40M Hz**	1k-150M Hz	10-50M Hz	100-2M Hz	0.1-10k Hz	6.5/11/17.5/30 GHz
Input Current Noise	**6 pA_{rms} @500 kHz (1-200 Hz)**	100 $fA/\sqrt{Hz}$ @1 MHz	557 pA_{rms} @2.5 MHz (1-1k Hz)	3 $fA/\sqrt{Hz}$ @10 kHz	-	-
Resistance Resolution*	**0.6 mΩ (0.5 MHz)**	-	24.9 mΩ† (2.5 MHz)	0.02 mΩ† (10 kHz)	0.4 mΩ† (10 kHz)	-
Capacitance Resolution**	**1.07 aF (2.5 MHz)**	1.56 aF (2.5 MHz)	93.9 aF† (2.5 MHz)	1.12 aF† (10 kHz)	22.8 aF† (10 kHz)	0.32 aF‡ (6.5 GHz)
Supply	**1.8 V**	3 V	3.3 V	3 V	1.2 V	1 V
Power	**9.7 mW**	112.5 mW	84.8 mW	60 mW	1.8 mW	65 mW‡‡
Area	**0.28 mm^2**	1.6 mm^2	4 mm^2	0.5 mm^2	1.68 mm^2	0.184 mm^2

*Calculated from noise value over 200 Hz, assuming amplitude V_{in}=1V, R_{nom}=10 kΩ;
**Calculated from noise value over 200 Hz, assuming amplitude V_{in}=1V.
†Estimated from reported noise(sensitivity) parameter;
‡BW=100 kHz; ‡‡4 channels and excitation source power are included.

2.6 Conclusion

This work presents an on-chip impedance-based sensor IC for flow cytometry capable of detecting and characterizing cells with single-cell resolution. A balanced, three-electrode source-differential sensing scheme eliminates the baseline current and amplifies only difference current. This enables the use of a high closed-loop gain impedance readout, which was designed using hybrid feedback impedance to maintain SNR across a wide modulation frequency range. The implemented modulation/demodulation sensing architecture supports an operating frequency from 50 kHz to 40 MHz with adjustable bandwidth. The system was demonstrated using a custom microfluidic flow cell and standardized 3-10 µm polymer microbead solutions for

analysis of counting and characterization sensivity and resolution under flow. As shown, 3 µm diameter beads are detected with 22 dB SNR, offering a theoretical detection limit for cell sizes below 1 µm diameter.

This work achieves sub-attofarad capacitive resolution at megahertz modulation frequencies with a considerable reduction in power consumption compared to the state-of-the-art. This scalable combination of high resolution and adjustable bandwidth at low power can support multiple future applications, including small-diameter cell counting as well as highly-parallelized multi-channel operation for high-speed or high-volumetric-throughput cytometry in future work.

Chapter 3: A Tunable Readout IC for Impedance Spectroscopy and Amperometric Measurement of Electrochemical Sensors

3.1 Introduction

Electrochemical sensing is increasingly used for measurements in chemical and biomedical applications, including noninvasive monitoring, DNA detection, and cell characterization [15, 25, 26]. As is depicted in Fig. 3.1, a variety of methods exist to extract information from an electrode-electrolyte interface, which can be categorized by the applied stimulation (constant or sinusoidal) and the measured electrical quantity (voltage, current, or impedance); each approach requires different readout circuits. For example, cyclic voltammetry (CV) employs a voltage ramp excitation, and a resulting current is measured. For electrochemical impedance spectroscopy (EIS), sinusoidal voltage (current) is applied, and the corresponding current (voltage) is measured to calculate the characteristic impedance of the sensor. As such, a multi-functional sensor interface circuit requires both wide input range and bandwidth selection.

CMOS-integrated EIS interfaces have been previously demonstrated with low-noise performance and wide input frequency range for biosensor applications, but these mixer-based architectures are unable to support very low frequency or DC amperometric sensing [15, 27]. A multi-functional system-on-chip (SoC) including both amperometric readout and impedance measurement was demonstrated in [26],

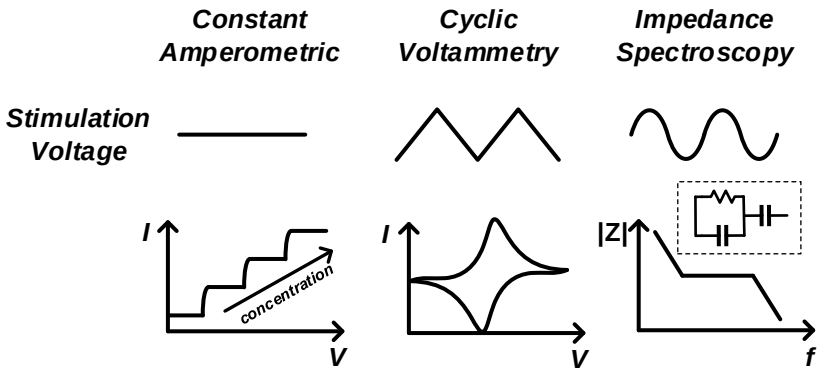


Figure 3.1: Stimulation electrode voltage and resulting response of three electroanalytical methods with amperometric readout.

however separate circuitry was used for each readout mode supporting different amplitude and frequency ranges, increasing both design complexity and power consumption. Such approaches have not demonstrated circuit re-use to support both operational modes using a combined, reconfigurable architecture.

In this work, we propose an integrated readout architecture that is reconfigurable to perform both general amperometric sensing and impedance analysis. A new common-gate current buffer with adjustable high-pass and low-pass corner frequencies is introduced to filter noise from outside the targeted frequency band, programmable for different input frequencies. An incremental delta-sigma modulator is designed to perform complex impedance extraction and signal digitization using the same circuitry. A complete current-to-digital sensor front-end interface is implemented in a 0.18 µm CMOS process, and measured results demonstrate low noise across wide input frequency range. The approach enables true DC to 100 kHz measurement to support EIS, CV, and amperometry.

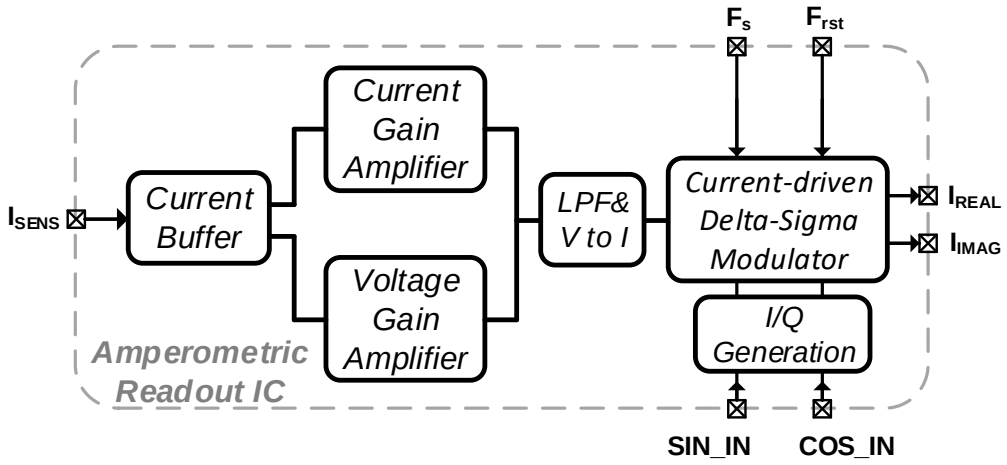


Figure 3.2: Architectural level block diagram.

3.2 System Design

Figure 3.2 shows the overall architecture of the proposed front-end interface for electrochemical sensors, including a current conveyor with selectable bandwidth, current and voltage gain stages for both operating modes, low-pass filter, and incremental delta-sigma modulator for electrochemical impedance analysis or amperometric digitization. The readout circuit is designed for an input frequency range of DC to 100 kHz for AC and DC analysis. A detailed schematic of the front-end architrcture is shown in Fig. 3.3.

3.2.1 Proposed Current Buffer

A schematic of the proposed current buffer circuit is shown in Fig. 3.4. Unlike a current mirror used in conventional current conveyors, a coupling capacitor C_C is used for current conduction. By designing C_C sufficiently larger than parasitic

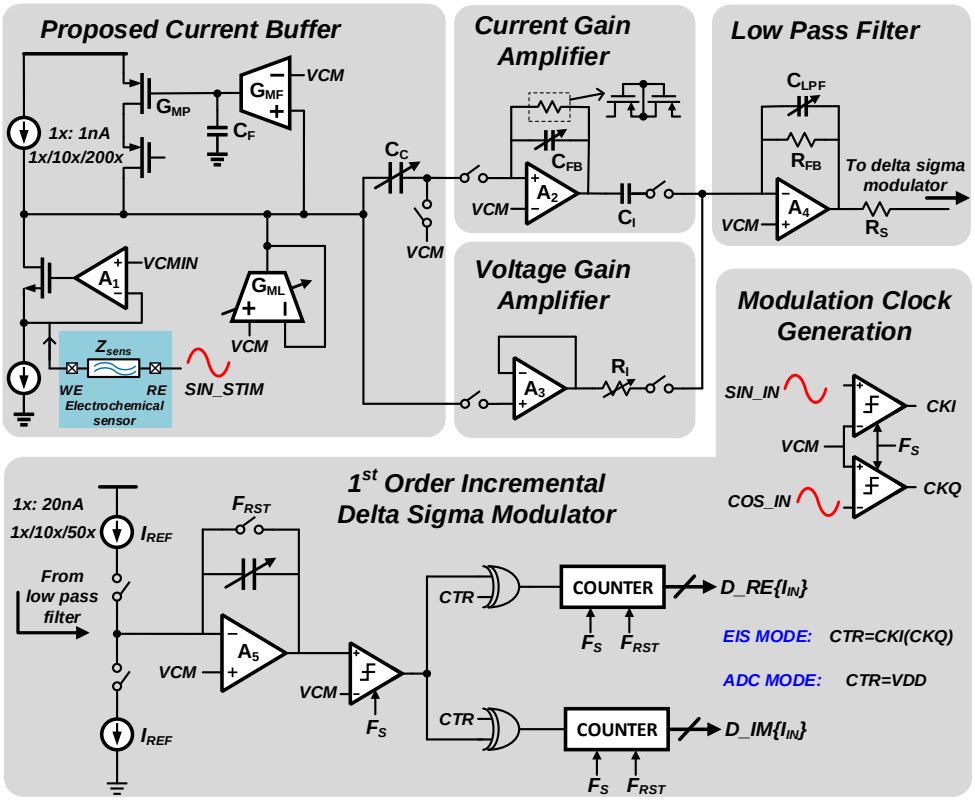


Figure 3.3: Block diagram of proposed amperometric sensing interface readout IC for electrochemical sensors.

capacitances, all AC current will flow through C_C to a low-impedance stage, which effectively adds a high-pass feature to the current transfer function, eliminating DC offset and reducing undesired low-frequency noise.

A unity-gain-feedback transconductance stage G_{ML} is added as the current buffer load to define and control the DC gain (equal to $1/G_{ML}$). To reduce the noise contribution from G_{ML}, a small G_{ML} value should be used, resulting in a large DC gain of the current buffer. For many biosensor and electrochemical applications, where leakage current may be in the nanoampere range, this may degrade stability of the DC operating point and reduce the dynamic range. Additionally, applications

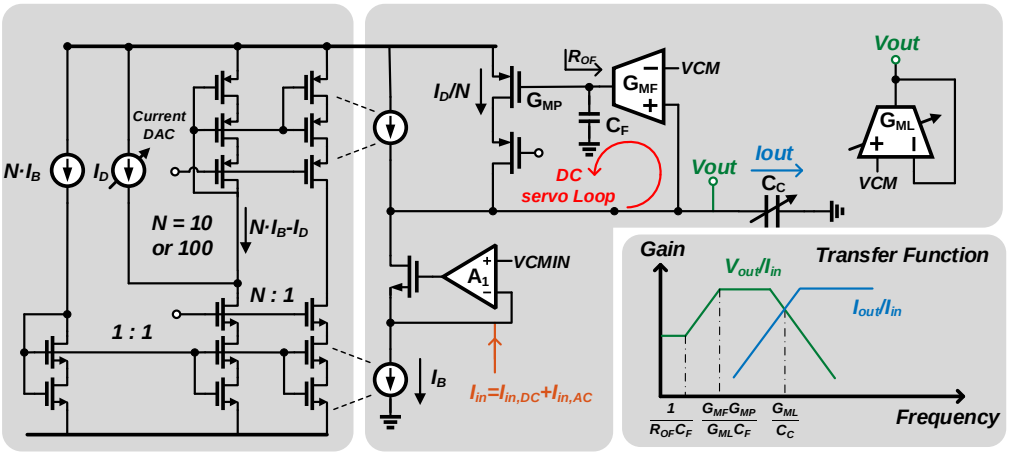


Figure 3.4: Schematic of proposed current buffer with current and voltage transfer function

such as EIS measure only a specific frequency range of AC current. Therefore, a DC servo loop with an inverting low-pass filter is added, and difference current provided by current source transconductance G_{MP} is summed at the V_{out} node. The transfer function for voltage gain can be derived as

$$\frac{V_{out}}{I_{in}} = \frac{1}{C_C} \frac{s + \frac{1}{R_{OF}C_F}}{s^2 + \frac{G_{ML}}{C_C}s + \frac{G_{MF}G_{MP}}{C_F C_C}}. \tag{3.1}$$

If pole p_1=$\mathrm{G_{ML}/C_C}$ can be designed to be much higher than pole p_2=$(\mathrm{G_{MF}G_{MP}})/(\mathrm{G_{ML}C_F})$, both high-pass and low-pass behaviors can be obtained for the voltage gain transfer function, as is shown in Fig. 3.4. For the current gain transfer function, the high-pass frequency is also set by $\mathrm{G_{ML}/C_C}$, the low-pass frequency of voltage gain transfer function. Therefore, high-pass frequency tuning can added by making G_{ML} and C_{C} adjustable.

The high-pass frequency $\mathrm{G_{ML}/C_C}$ will be bounded by the largest feasible on-chip

capacitor. This limits the detectable frequency range only for capacitively-coupled current I_{out}. For low input frequencies, the signal can alternatively be processed in the voltage domain, either using the feedback loop or by disabling the loop, enabling low frequency (and DC) input signals without requiring very large C_{C}.

In this design, C_{C} is designed as a 4-bit programmable capacitor bank with a maximum 15 pF total capacitance. Pole p_2 must also be tunable and sufficiently small compared to p_1, while avoiding large on-chip capacitor C_{F}. To achieve this aim, a difference current mirror topology is used, as shown in Fig. 3.4. The effective bias current flowing through transconductance G_{MP} is equal to the current difference between the top and bottom current source, which is generated by intentionally injecting a small current I_{D} into the current mirror. By using a large mirroring ratio, N, 10 or 100 in this design, a small current can be obtained in the G_{MP} branch. By designing I_{D} as a programmable current DAC, a sub-100 pA current can be generated, including compensating mismatch current from top and bottom sources. As a result, a small programmable G_{MP} value is achieved with a C_{F} value of 15 pF.

A regulated, common-gate input stage is adopted both to reduce input impedance and to set the DC potential voltage for the input working electrode (WE). As implemented, the feedback amplifier A_1 consumes 1.5 µA to maintain low power and low noise below 100 kHz with tens of pF input capacitance. As the current source is the major noise contributor of the current buffer stage, the N- and P-type current sources are designed to have 1/10/200 nA biasing current to support both low-noise and high-input-current applications. Instead of chopping, which would introduce charge injection and switching noise to the sensitive working electrode, long chan-

nel length devices (15 µm) are used for the current source to reduce flicker noise. Feedback stage G_{MF} is biased at 1 nA. G_{ML} is programmable, with a minimum bias current of 1 nA and a maximum of 100 nA; maximum bias current determines the maximum input DC current in voltage mode. Both G_{MF} and G_{ML} are designed as single-stage cascode amplifiers for simplicity and low noise.

3.2.2 Gain Stage and LPF

As depicted in Fig. 3.3, a variable gain stage is inserted in the signal chain following the front-end current buffer to minimize noise contributions from later stages and extend signal dynamic range. As both current and voltage domain signals can be processed based on the input signal frequency, a gain multiplexer for both current and voltage modes is designed. For the current amplifier, a capacitive programmable gain amplifier (PGA) is implemented using a pseudo-resistor to define the DC operating path. The current gain is set by $\mathrm{C_I}/\mathrm{C_{FB}}$. As designed, $\mathrm{C_I}$ is 10 pF, and $\mathrm{C_{FB}}$ is a programmable capacitor with a minimum value of 200 fF, for a maximum current gain of 50. The current gain stage can also be bypassed (switch not shown) for processing large input signal current.

The voltage gain amplifier is formed by a unity-gain buffer, A_3, followed by a inverting amplifier A_4 with feedback resistance R_{FB}. A_3 provides a large input impedance, such that the output impedance of node V_{out} is unaltered. Voltage gain is determined by the ratio between R_{FB} (1 MΩ) and R_{I}. In this design, the ratio is designed as 1 or 5. Variable voltage gain can also be provided by adjustable G_{ML} in

the first stage.

Amplifier A_4 with R_{FB} also serves as a transimpedance amplifier (TIA) for the output from the current amplifier, which is converted to the voltage. A programmable capacitor, C_{LPF}, is added in parallel to R_{FB} to provide a variable low-pass characteristic. $A_2 - A_4$ are all implemented as two-stage, folded-cascode amplifiers. A_2 and A_3 each consume 6 µA, and A_4 consumes 12 µA. The voltage signal at the output of the LPF is converted back to current by resistor R_{S} for subsequent current-driven delta-sigma modulator. R_{S} is designed identically to R_{FB} for good matching.

3.2.3 Delta-Sigma Impedance Analyzer

While delta-sigma-based impedance analyzers have been previously demonstrated [13, 28], in this work, the frequency response analysis algorithm is embedded directly in an incremental delta-sigma modulator. As shown in Fig. 3.3, a reset signal is added to clear all memory elements, which provides sample-by-sample conversion. Moreover, by moving the modulation signal CKI and CKQ from analog domain to digital domain using an XOR gate [29], the modulator can be easily reconfigured for amperometry and impedance analysis modes. If no modulation signal is applied, the modulator operates as a simple ADC with a Nyquist rate of F_{RST}, digitizing the input current signal. If a modulation signal is applied and F_{RST} is set equal to the input signal frequency, the modulator performs impedance analysis to obtain digitized real and imaginary components of the input signal. The relationship between output and

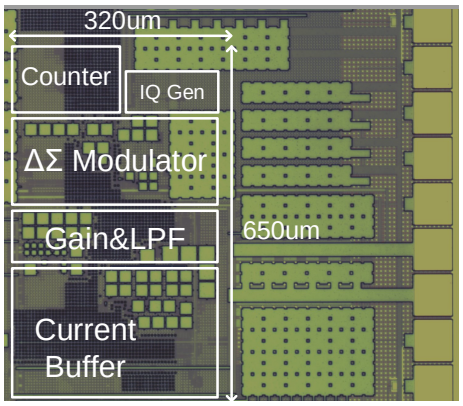
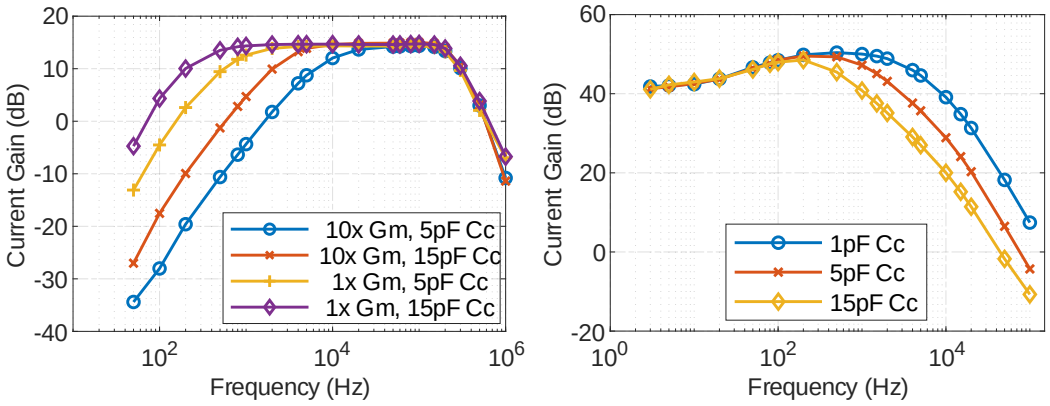


Figure 3.5: Die photo of fabricated EIS and amperometric measurement IC.

real (imaginary) input component is

$$I_{RE(IM)} = \frac{2}{\pi}\frac{D_{RE(IM)}I_{REF}}{OSR} \tag{3.2}$$

where OSR is the ratio between oversampling frequency F_{S} and reset frequency F_{RST}. The maximum F_{S} is chosen as 15 MHz to achieve sufficient resolution for 100 KHz input. A programmable current DAC with 20 nA/200 nA/1 uA current is designed to support a wide input signal range. A programmable integrating capacitor with minimum 50 fF and maximum 7.5 pF capacitance also enables a wide range of input currents and F_{S} values. The modulation signals CKI and CKQ are generated by comparator from SIN_IN and COS_IN and synchronized with input stimulation signal SIN_STIM.



(a) (b)

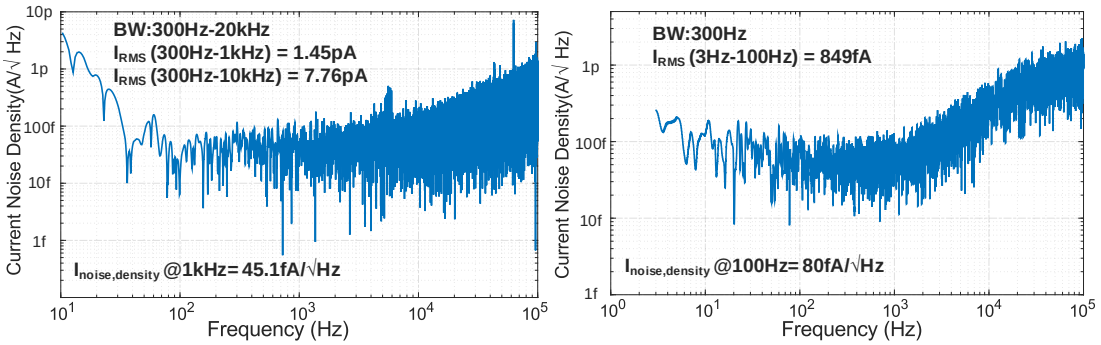
Figure 3.6: Measured tunable current gain transfer function for (a) current mode and (b) voltage mode for different values of G_m and C_C.

3.3 Measurement Results

The design was fabricated in a general purpose 0.18 µm CMOS process and occupies $320 \times 650\,\mu m^2$; a die photo is shown in Fig. 3.5. Standalone copies of analog front-end circuits were included to characterize individual block performance.

Figures 3.6a and 3.6b show the measured overall current gain transfer function for both current and voltage modes. In current mode, current gain was set to 5, and G_m and C_C enable programmable high-pass corner frequencies. In voltage mode, G_m was set to an equivalent current gain of ∼300.

The noise performance of the front-end circuit in both current mode and voltage mode was measured, as shown in Figs. 3.7a and 3.7b. For current mode, current gain was set to 50 and high-pass corner frequency was set to 300 Hz. The input-referred current noise PSD at 1 kHz is $45.1 fA/\sqrt{Hz}$, which gives 1.45 pA RMS current noise for 1 kHz bandwidth. For voltage mode, 300 Hz bandwidth with equivalent current



(a) (b)

Figure 3.7: Input-referred current noise density of proposed front end circuit in (a) current mode (b) voltage mode for 1 nA biasing.

gain of 420 was set. 80 fA/$\sqrt{}$Hz current PSD at 100 Hz and 849 fA RMS current are achieved. The bias current for the current buffer was set to 1 nA for minimum noise in both modes.

The complete readout IC combining analog front-end and delta-sigma modulator was also measured. With the modulator in EIS mode, the magnitude of real and imaginary digital output codes were obtained for varying input frequency; Fig. 3.8 summarizes measured output magnitude codes versus input sinusoid amplitude. Voltage and current modes were operated for 100 Hz and for 1, 10, 100 kHz, respectively. Minimum detectable signal level is higher than would be expected from only front-end RMS noise and is limited by quantization noise. More than 80 dB dynamic range is achieved up to 10 kHz, with a maximum of 104 dB dynamic range at 10 Hz.

An input DC current sweep was performed using source meter to demonstrate the amperometric measurement capability of the proposed readout IC. The measured

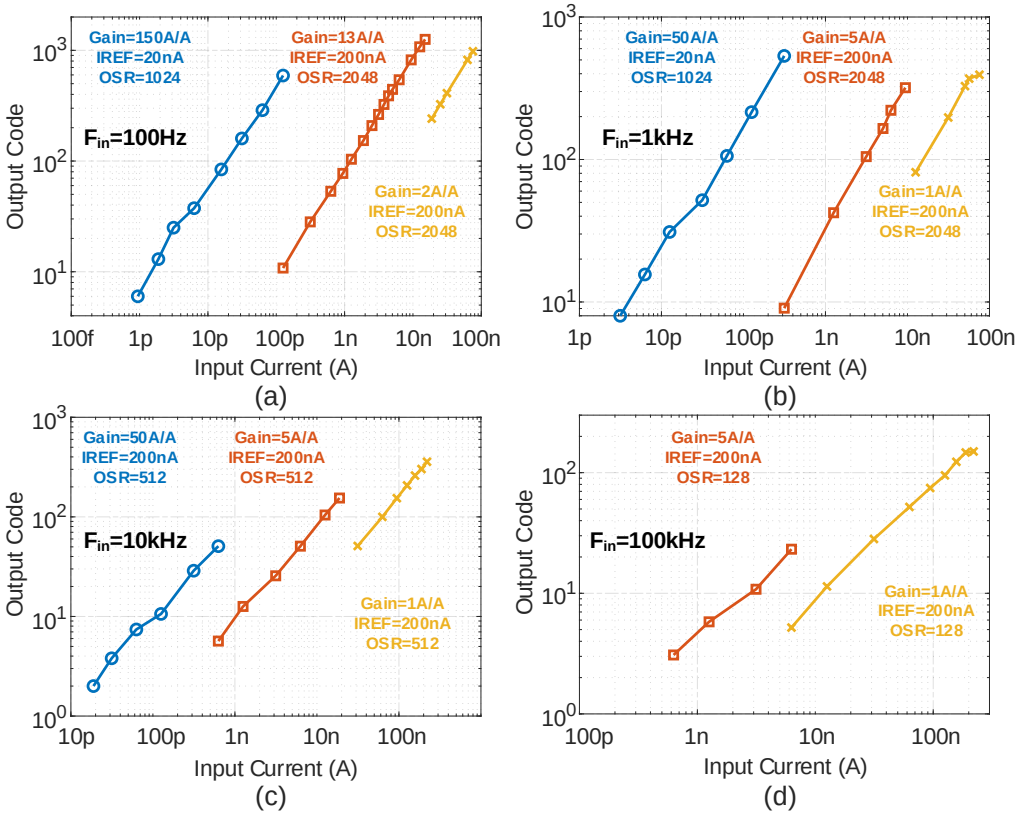


Figure 3.8: Linearity of output code versus input sinusoid amplitude for (a) voltage mode at 100 Hz, and current mode at (b) 1 kHz, (c) 10 kHz, and (d) 100 kHz.

transient waveform of ADC output is shown in Fig. 3.9, presenting a good low-current sensing capability with this work.

A discrete model cell was used to demonstrate the proposed architecture for EIS, as shown in Fig. 3.10a, following phase calibration. A 20 mV_{pp} sinusoidal signal was swept across frequncy as input stimulation. Impedance spectroscopy was conducted from 5 Hz to 500 Hz in voltage mode, and from 1 kHz up to 100 Hz in current mode. Measured results are shown for magnitude response in Fig. 3.10a and phase response in Fig. 3.10b compared to an ideal model. Relative error is also plotted, demonstrat-

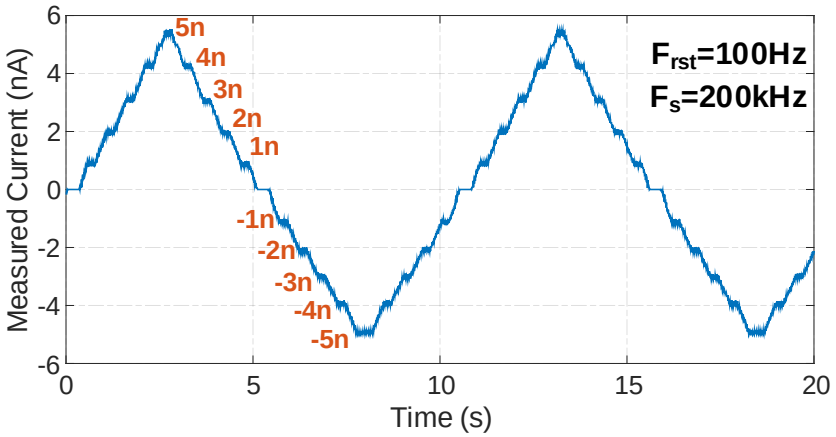


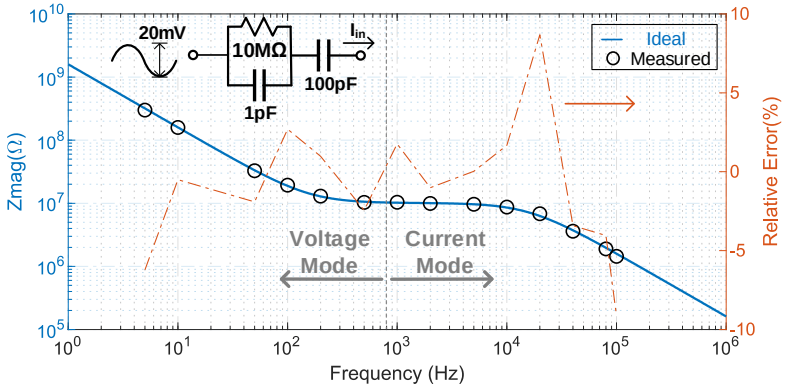
Figure 3.9: Transient waveform of measured ADC output with a swept, quasi-static DC current input using a source meter (Keithley 2450).

ing <10% error across wide frequency range for high impedance measurement.

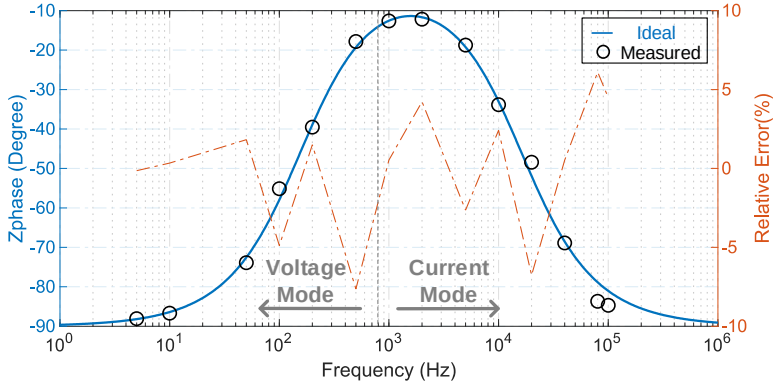
A comparison with related work is provided in Table 3.1. Leveraging a new current buffer topology, combined voltage and current processing, and a reconfigurable delta-sigma modulator, the proposed architecture enables wide input frequency range and dynamic range for both impedance-based and amperometric electrochemical sensing.

3.4 Conclusion

In this paper, we present a low-noise multi-functional readout IC architecture for electrochemical sensing. Leveraging the proposed current buffer topology and reconfigurable delta sigma modulator, the IC can perform a wide range of input frequency and magnitude sensing with both impedance and amperometric sensing ability, which appeals to various amperometric readout application such as EIS and



(a)



(b)

Figure 3.10: Impedance spectroscopy measurements using impedance model cell: (a) magnitude response and (b) phase response, both with relative error.

CV in chemical and biomedical sensors.

Table 3.1: Performance comparison of low current interface IC

Reference	[15]	[27]	[25]	This Work
Application	EIS	EIS	CV/CA	EIS/CV/CA
Process (µm)	0.35	0.18	0.18	0.18
Noise Floor ($fA/\sqrt{Hz}$)	-	51 (0.2nA)	46 (0.2nA)	45.1@1kHz (1nA)
RMS Noise	$577pA_{rms}$ (1kHz)	-	$0.48pA_{rms}$ (110Hz)	$1.45pA_{rms}$ (1kHz)
Frequency Range (Hz)	10-50M	10-10k	110-10k	DC-100k
Current Range	±25µA	±2µA	±50nA	±100nA*, ±200nA**
Dynamic Range(dB)	97@10Hz	152	104	104@10Hz 81@10kHz
Power Consumption	84.8mW @3.3V	144µW @1.8V	12.1µW*** @1.8V	311.4µW @1.8V
Area (mm^2)	4	0.48	0.03***	0.208

* Voltage Mode;** Current Mode;*** ADC not included.

Chapter 4: A RC Oscillator based on IQ-Balanced Impedance Sensing Frequency-Locked-Loop

4.1 Introduction

With the growing demand for on-chip, low-power clock references in emerging sensor and IoT systems due to extreme power limitations, the design constraints for these frequency references are increasingly limited in all aspects such as energy efficiency, area, frequency stability, and reconfigurability. Crystal and MEMS-based oscillator can provide low-power and accurate output frequency, however, it requires off-chip components. On-chip RC oscillator is favored because its fully-integrated implementation in these applications. Conventional RC relaxation oscillators are limited in frequency accuracy and stability by the continuous comparator which is PVT-sensitive.

4.1.1 RC Oscillator Based on Frequency-Locked-Loop (FLL)

An alternative closed-loop RC oscillator approach based on frequency-locked-loop (FLL) [5,30–41] gains more attention from people because its absence of the sensitive continuous time comparator enhances the frequency stability. Fig. 4.1 shows a simple block diagram of the FLL that explains its working principle. The FLL consists of four parts: 1) A frequency voltage converter (FVC) usually consisted by the

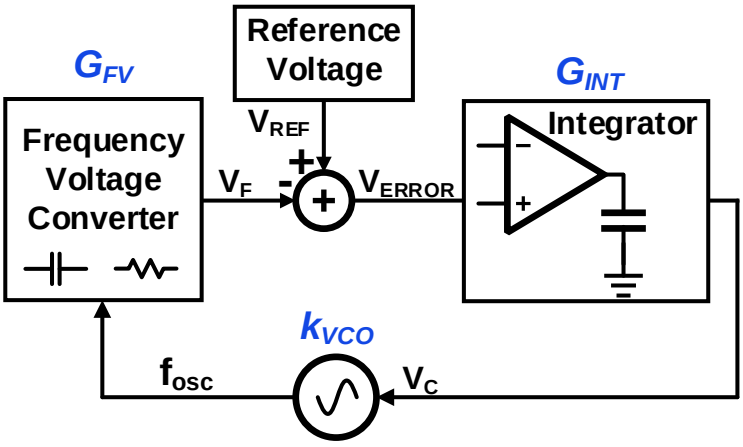


Figure 4.1: Block diagram showing the working principle of the frequency-locked-loop.

resistor and capacitor that translates the frequency information f_{osc} into voltage; 2) A reference voltage block generates a temperature and supply invariant voltage V_{REF}; 3) An error amplifier which is implemented by the integrator that integrates the error voltage V_{ERROR} from reference voltage V_{REF} and the output voltage of the FVC V_F, generating a high-time-constant control voltage V_C; 4) An voltage-controlled-oscillator (VCO) steered by V_C yielding variable output frequency. Operated in close-loop, the f_{OSC} can be written as,

$$f_{osc} = \frac{LG}{LG+1} \tag{4.1}$$

$$LG = G_{INT}G_{FV}k_{VCO} \tag{4.2}$$

$$f_{ref} = \frac{V_{REF}}{G_{FV}} \tag{4.3}$$

From (4.1), the output frequency f_{osc} merely relies on f_{ref} if loop gain LG is sufficiently high, and f_{ref} can achieve temperature- and supply-invariant once V_{REF} and G_{FV} is designed as temperature- and supply-invariant. (4.3) indicates that the frequency stability of a FLL system is considerably dependent on the design of FVC. Therefore, detailed investigations and discussions of various FVC approaches will be presented in the next section.

4.2 Frequency Voltage Converter (FVC) in FLL-based RC Oscillator

In this section, the design of FVC in FLL-based RC oscillator will be discussed including several designs in previous work and proposed new FVC design. The working principle of each topology is discussed, along with their performance analysis in gain, power, noise and area. In the end, a performance comparison between various FVCs is presented.

4.2.1 FVC design in previous work

Fig. 4.2 shows the schematic of current-driven FVC [31]. Two current sources injects current into a reference resistor R_{REF} branches and a switched-capacitor C_{REF} converter, generating a reference voltage and a frequency-dependent varying voltage, respectively. The integrator will force the voltage from both branches equal, yielding a nominal output frequency as,

$$f_{osc,nom} = \frac{1}{R_{REF}C_{REF}} \tag{4.4}$$

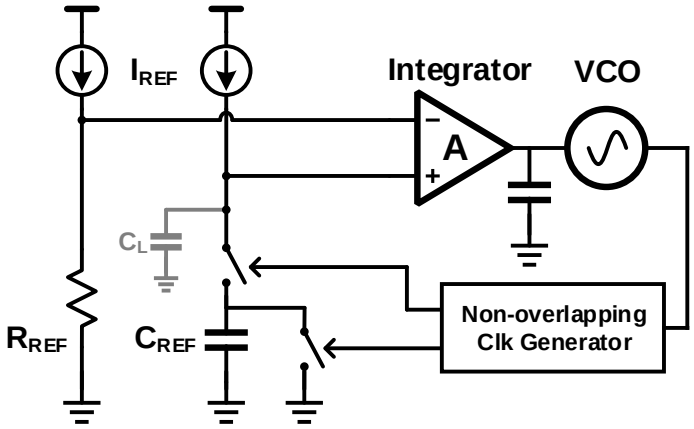


Figure 4.2: Current-driven FVC in FLL system.

A large filtering capacitor $C_L(>10C_{REF})$ is often required to filter out the ripple induced by the switched capacitor. There are several major error sources and design challenges in this topology: First, the current mismatch between two current sources will introduce a temperature- and supply-dependent offset voltage to the input of the integrator, which significantly reduced the frequency stability. In [31], a current chopping technique is introduced to overcome this issue; Second, as the input common-mode voltage is restricted by the input range of the integrator amplifier, the trade-off between power consumption from the current source and the area from bulky resistor cannot be broken, which limits the optimization freedom in design strategy. Furthermore, the DC common-mode is sensitive to the current source variation by supply and temperature, which again effects the frequency stability by effecting integrator dynamics. A performance summary table of the current-driven FVC is presented in Table 4.1.

Table 4.1: Performance Summary of Current-driven FVC

Gain	**Power**	$\mathbf{V}_{CM}$	**Area**
$\frac{I_{REF}R_{REF}}{f_{osc,nom}}$	$2I_{REF}V_{DD}$	$I_{REF}R_{REF}$	$1R_{REF}$

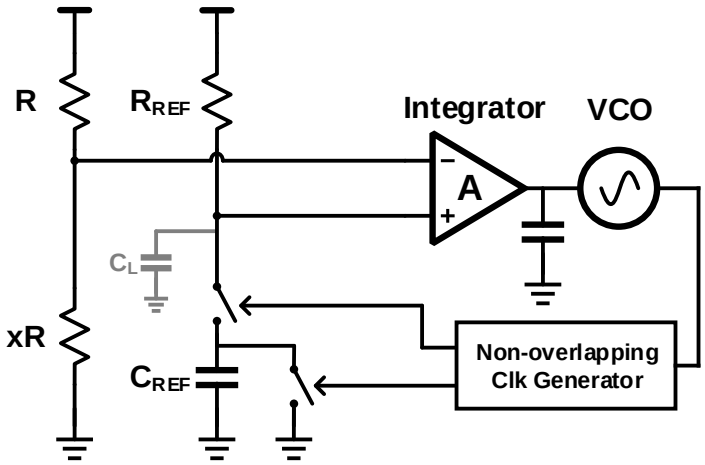


Figure 4.3: Wheatstone Bridge FVC in FLL system.

An alternative FVC [33, 38–40] that addresses the non-idealities from current source is presented in Fig. 4.3. Here, the current source is replaced with the resistors to generate the voltage. The reference voltage can be adjusted by the ratio x of the resistive divider. As a result, the nominal oscillation frequency can be derived as,

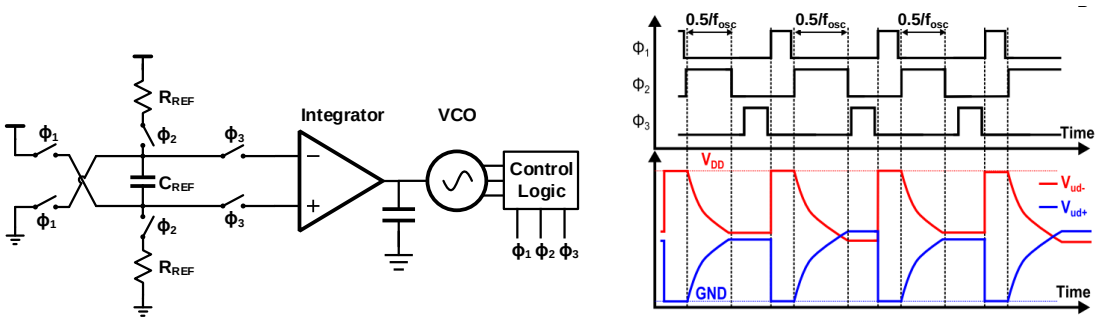
$$f_{osc,nom} = \frac{1}{xR_{REF}C_{REF}} \tag{4.5}$$

An obvious advantage of this topology is all-passive implementation achieves better matching across two branches if resistor type and layout is well-matched. Moreover,the flicker noise from transistors is also eliminated. The resistor R in

Table 4.2: Performance Summary of Wheatstone Bridge FVC

Gain	**Power**	$\mathbf{V}_{CM}$	**Area**
$\frac{xV_{DD}}{(1+x)^2 f_{osc,nom}}$	$\frac{V_{DD}^2}{(1+x)R_{REF}}$	$\frac{xV_{DD}}{1+x}$	$(2+x)R_{REF}$

Assume $R = R_{REF}$.



(a) (b)

Figure 4.4: (a)Schematic of the RC charging FVC, and (b) its operating timing diagram from [5]

reference branches can also be implemented with diode [39] to build the leakage-based voltage reference, which significantly reduces the power and area consumption of the reference branch. However, the input common-mode voltage varies notably with the supply voltage and supply rejection of the FVC degrades because of relative low-impedance of R. A performance summary table of the Wheatstone bridge FVC is presented in Table 4.2.1. Compared with Table 4.1, the gain and power performance of the Wheatstone bridge FVC is the same as current-driven FVC, both depending on the V_{REF}.

The last topology will be discussed in this section is first introduced in [30] and also adopted in [5,34]. Shown in Fig. 4.4, this fully-differential FVC works as follows:

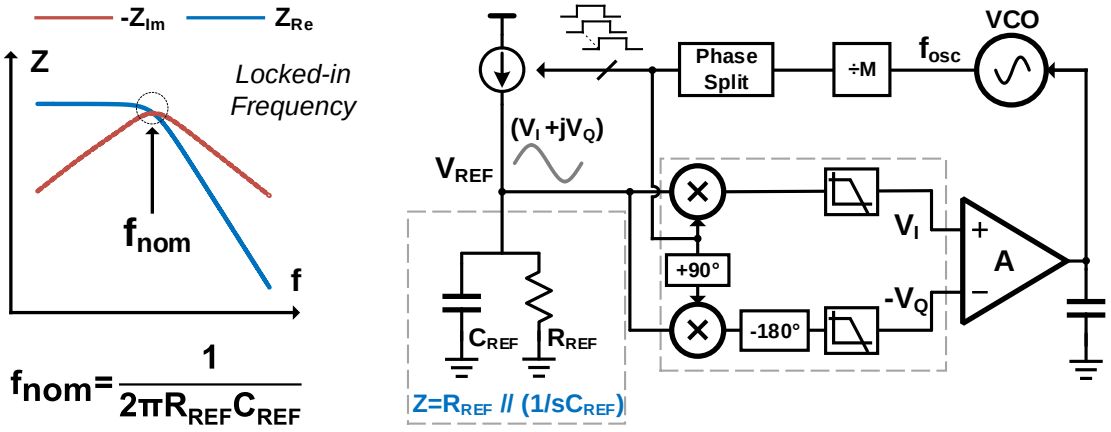
Table 4.3: Performance Summary of RC Charging FVC

Gain	**Power**	$\mathbf{V}_{CM}$	**Area**
$\frac{\ln 2 V_{DD}}{f_{osc,nom}}$	$\frac{V_{DD}^2}{2 \ln 2 R_{REF}}$	$0.5V_{DD}$	$2R_{REF}$

at ϕ_1, V_{ud+} and V_{ud-} are reset to GND and VDD, respectively; at ϕ_2, V_{ud+} and V_{ud-} will charge and discharge to VDD and GND for a fixed period (normally half cycle of the f_{osc}), and capacitor C_{REF} will hold the voltage until ϕ_3 is closed after ϕ_2 is open; at ϕ_3, V_{ud+} and V_{ud-} are sampled to the input of the integrator, which senses the error voltage, generate the VCO control voltage and close the feedback loop. After writing the first-order charging equation in time domain, a nominal oscillation frequency $f_{osc,nom}$ can be derived as,

$$f_{osc,nom} = \frac{1}{4 \ln(2) R_{REF} C_{REF}} \tag{4.6}$$

This topology has the advantages of Wheatstone bridge FVC as only fully-passive components including resistor, capacitor and switches are employed in the FVC, and no extra accuracy reference voltage is required. However, the oscillation frequency is strictly dependent on the charging period (half cycle of the FVC operating frequency) and switch control, which requires the frequency divider and extra control logic. A performance summary table of the Wheatstone bridge FVC is presented in Table 4.3. Compared with previous design, this topology has its intrinsic benefit in area.



(a) (b)

Figure 4.5: (a) Magnitude of the real and imaginary impedance of a RC pair (shown in log-scale), and (b) block diagram of FLL using proposed FVC.

Table 4.4: Performance Summary of Proposed Impedance Sensing FVC

Gain	Power	Noise	Area
$\frac{I_{REF}R_{REF}}{2f_{osc,nom}}$	$I_{REF}V_{DD}$	$I_{REF}R_{REF}$	R_{REF}

4.2.2 Proposed Impedance Sensing FVC

In this work, an alternative FVC composed by an AC current source and simple RC circuit ($R_{REF}\|C_{REF}$) is presented in Fig. 4.5. To illustrate its use in detection and frequency locking, the frequency response of both real and imaginary part of the RC pair impedance Z is shown. Due to the single pair RC network, Z_{Re} and Z_{Im} have only one intersection, located in f_{nom} at the 3-dB pole frequency of the complex impedance Z. Any frequency less (more) than f_{nom} will result in Z_{Re} greater (less) than Z_{Im}, which lets Z serve as a practical FVC that translates input frequency

deviation against f_{nom} into real and imaginary impedance differences. The proposed FVC allows frequency translation in single RC branch without additional accuracy reference, enabling a symmetrical fully-differential implementation. To quantitatively analyze the operation of proposed FVC, we first write the real and imaginary impedance expression of single RC pair,

$$Z_{Re}(f) = \frac{R}{1 + R_{REF}^2 C_{REF}^2 (2\pi f)^2} \tag{4.7}$$

$$Z_{Im}(f) = \frac{R_{REF}^2 C_{REF} 2\pi f}{1 + R_{REF}^2 C_{REF}^2 (2\pi f)^2} \tag{4.8}$$

By taking the derivative of Z_{Re} and Z_{Im} and assume the AC current amplitude is I_{REF}, the gain of the proposed FVC can be written as,

$$G_{Re} = I_{REF} \left. \frac{\partial Z_{Re}}{\partial f} \right|_{f=f_{nom}} = \frac{-I_{REF} R_{REF}}{2 f_{nom}} \tag{4.9}$$

$$G_{Im} = I_{REF} \left. \frac{\partial Z_{Im}}{\partial f} \right|_{f=f_{nom}} = 0 \tag{4.10}$$

$$G_{FVC} = G_{Re} - G_{Im} = \frac{-I_{REF} R_{REF}}{2 f_{nom}} \tag{4.11}$$

There are several advantages for proposed FVC: 1) Thanks to the self-reference of the real and imaginary part of the V_{REF}, no additional dedicated voltage reference is required. Moreover, as only single physical node is presented in the design, the interference to V_{REF} will be equal to both V_R and V_I, and be nullified during comparison. In other words, the proposed FVC is actually operated as an Frequency-to-Phase Converter (FPC), which is immune to any kind of interference in voltage domain. 2) Although I_{REF} is built with active transistor which contributes flicker

noise, thanks to AC operation in f_{nom} and demodulation, flicker noise will be moved to higher frequency band. 3) Phase-domain encoded frequency information in proposed FVC is easy to reconfigurable in oscillating frequency without altering operating point in voltage domain, which appears to be more sensitive. This reconfigurability will be further discussed in the next session. A performance summary table of the Wheatstone bridge FVC is presented in Table 4.4.

By adopting the proposed FVC in the loop, an IQ-balanced impedance sensing FLL architecture is presented. Shown in Fig. 4.5b, the proposed FLL consists of the following components: 1) FVC formed by an RC pair with the AC current reference translating frequency error into complex voltage domain; 2) a quadrature frequency down-converter with low-pass filter, which performs the lock-in operation to produce in-phase (V_I) and quadrature ($-V_Q$) DC components, indicating the real and imaginary part of the voltage signal at the FVC output; 3) an integrator integrates the error voltage between V_I and $-V_Q$ to build a high-time-constant control voltage VC; 4) a VCO steered by V_C yielding variable output frequency; and, 5) a frequency divider and phase splitting block to create multiphase clock driving AC current reference in feedback. In steady state, the FLL will force V_I=$-V_Q$, yielding a stable frequency f_{nom} in FVC.

4.2.3 FVC Summary

In this section, a comprehensive comparison table is introduced to compare four FVCs discussed in the previous sections. In order to fairly compare the performance,

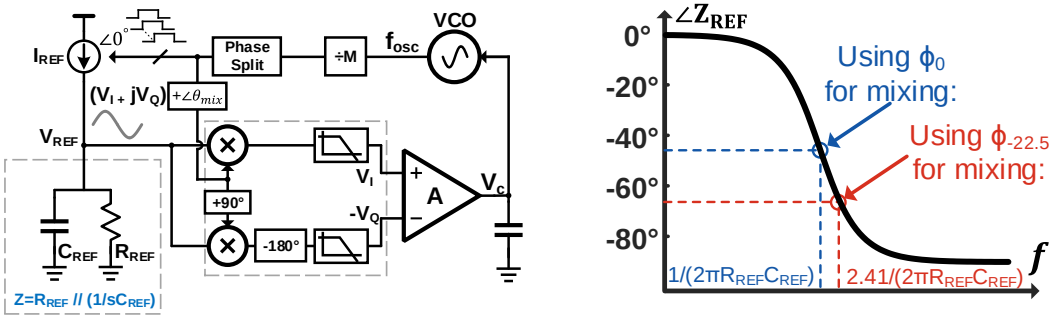
Table 4.5: Performance Comparison Between Different FVC topologies

FVC Type	$\boldsymbol{f_{nom}}$	$\frac{\boldsymbol{Gain}}{\boldsymbol{Power}}$	$\frac{\boldsymbol{f_{nom}}}{\boldsymbol{Power}}$	$\boldsymbol{Area * f_{nom}}$
Current-driven	$\frac{1}{R_{REF}C_{REF}}$	$\frac{R_{REF}}{2V_{DD}f_{nom}}$	$\frac{1}{2C_{REF}V_{CM}V_{DD}}$	$\frac{1}{C_{REF}}$
Wheatstone Bridge	$\frac{1}{xR_{REF}C_{REF}}$	$\frac{xR_{REF}}{(1+x)V_{DD}f_{nom}}$	$\frac{1+x}{x}\frac{1}{C_{REF}V_{DD}^2}$	$\frac{2+x}{x}\frac{1}{C_{REF}}$
RC Charging	$\frac{1}{4ln(2)R_{REF}C_{REF}}$	$\frac{2\ln(2)^2R_{REF}}{V_{DD}f_{nom}}$	$\frac{1}{2C_{REF}V_{DD}^2}$	$\frac{1}{2\ln(2)C_{REF}}$
Impedance Sensing	$\frac{1}{2\pi R_{REF}C_{REF}}$	$\frac{R_{REF}}{2V_{DD}f_{nom}}$	$\frac{1}{2\pi C_{REF}V_{CM}V_{DD}}$	$\frac{1}{2\pi C_{REF}}$

normalization to the gain, noise and area in power and frequency is adopted. As is presented in Table 4.5, RC charging has the best performance in FVC gain per power and the impedance sensing FVC occupies the least area at a given oscillating frequency.

4.3 Impedance IQ-balanced FLL

In this section, the impedance IQ-balanced FLL system based on the proposed impedance sensing FVC is presented, as is shown in First, the alternative phase mixing technique is introduced to perform a fully-digital frequency reconfigurability. Second, the linear system analysis of the proposed FLL including noise analysis is performed. Then, non-ideal effects with temperature- and supply- dependent error in the system which affects the frequency stability are analyzed. Finally, the power optimization of the system is performed.



(a) (b)

Figure 4.6: (a) Block diagram of impedance IQ-balanced FLL with alternative phase mixing. (b) Frequency reconfigurability with different mixing phase.

4.3.1 Alternative Phase Mixing

Fig. 4.6a shows the proposed impedance IQ-balanced FLL with alternative phase mixing. With a fixed phase shift θ_{mix} between stimulation clock for current source and the mixing clock in demodulation, the phase shift θ_{FVC} introduced by FVC as well as operating frequency f_{nom} can be shifted. Therefore, θ_{FVC} can be written as,

$$\theta_{FVC} = -(45^\circ - \theta_{mix}) \tag{4.12}$$

Still consider single RC pair model, a corresponded frequency $f_{nom,pm}$ with θ_{FVC} can also be calculated as,

$$f_{nom,pm} = \tan(45^\circ - \theta_{mix}) \cdot f_{nom} \tag{4.13}$$

Fig. 4.6b describes how the phase mixing works: If mixing clock is in phase with the FVC excitation source, a -45° phase shift of Z_{REF} will be required to achieve V_I=-V_Q,

yielding the operating frequency as f_{nom} in FD. If a -22.5° shift clock $\theta_{-22.5^\circ}$ is selected for mixing, an excessive phase shift (-67.5°) will be required to compensate the mixing clock $\theta_{-22.5^\circ}$ to maintain V_I=-V_Q, yielding an extended frequency 2.41*f_{nom}. An important reason that the phase mixing technique suits in the proposed architecture despite its digital overhead is that the multi-phase clock can be easily obtained from existing frequency divider. Besides, thanks to the identical clock source to perform sinusoid waveform generation and down-conversion mixing, the phase θ_{mix} is resilient to the temperature and supply fluctuation, which guarantees a consistent frequency stability performance with different mixing phase.

Compared to previous design [39] which requires adjusting reference voltage to reconfigure the frequency, proposed alternative phase mixing technique keeps the DC operating voltage. Furthermore, digital-intensive reconfigurability adds no design cost and complexity such as implementing extra resistor or capacitor bank.

4.3.2 Linear System Analysis

The small-signal linear analysis is essential to evaluate the loop dynamics and potentially investigate any non-idealities in the system. For the proposed impedance IQ-balanced FLL, the linear system model is shown in Fig. 4.7. From Fig. 4.7,

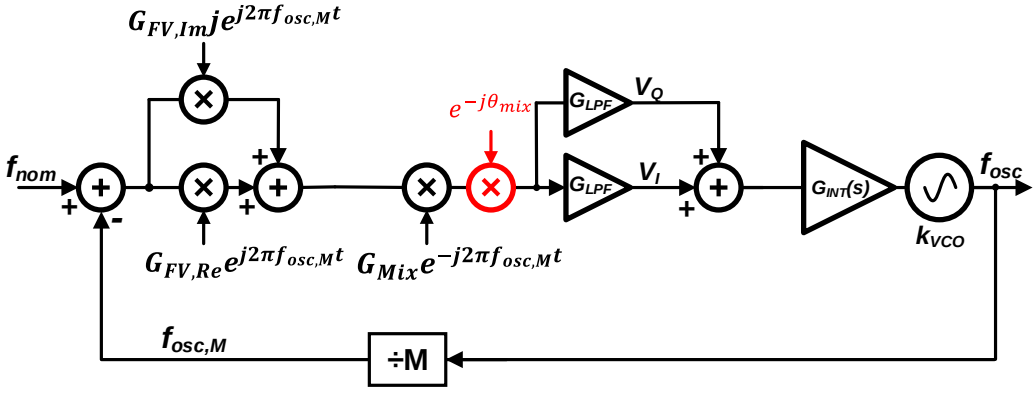


Figure 4.7: Linear system model of impedance IQ-balanced FLL.

combined with (4.11), we can write the loop transfer function of f_{osc} as,

$$f_{osc} = \frac{LG}{LG+1} \cdot Mf_{nom} \tag{4.14}$$

$$LG = -[G_{FV,Re}(cos(\theta_{mix}) - sin(\theta_{mix})) + G_{FV,Im}(cos(\theta_{mix}) + sin(\theta_{mix}))] \cdot G_{Mix} \cdot G_{LPF} \cdot G_{INT} \cdot k_{VCO} \tag{4.15}$$

LG is dimensionless, and if LG is sufficiently large, f_{osc} can be approximated as $M \cdot f_{nom}$. θ_{mix} is the mixing phase. If $\theta_{mix} = 0$, it means no alternative phase mixing

is presented. We can first calculate the FVC gain with phase mixing,

$$G_{FV,Re} = I_{REF} \left.\frac{\partial Z_{Re}}{\partial f}\right|_{f=f_{nom}} = -0.5\cos^2(2\theta_{mix})\frac{I_{REF}R_{REF}}{f_{nom}} \tag{4.16}$$

$$G_{FV,Im} = I_{REF} \left.\frac{\partial Z_{Im}}{\partial f}\right|_{f=f_{nom}} = -0.25\sin(4\theta_{mix})\frac{I_{REF}R_{REF}}{f_{nom}} \tag{4.17}$$

$$f_{nom} = \frac{1}{\tan(\theta_{pm})}\frac{1}{R_{REF}C_{REF}} \tag{4.18}$$

$$\tag{4.19}$$

From (4.16) to (4.18), a general expression for loop gain LG with phase mixing can be written as

$$LG(\theta_{mix}) = k \cdot \frac{I_{REF}R_{REF}}{f_{nom}} \cdot G_{Mix} \cdot G_{LPF} \cdot G_{INT} \cdot k_{VCO} \tag{4.20}$$

$$k = 0.5\cos^2(2\theta_{mix})[cos(\theta_{mix}) - sin(\theta_{mix})] + 0.25\sin(4\theta_{mix})[cos(\theta_{mix}) + sin(\theta_{mix})] \tag{4.21}$$

If $\theta_{mix} = 0^\circ$ with no phase mixing, $k = 0.5$. Fig. 4.8 shows how k is varying with different mixing phase. For FLL system, the static frequency error as is shown in (4.14) is not interested. The frequency error introduced by temperature and supply drift is more concerned. From, (4.14), two major error sources are identity: the first-order effect caused by f_{nom} instability and the second-order effect caused by LG. For the first case, as f_{nom} error is dominant by the linear part in the numerator, we can show

$$f_{nom}(T, VDD) = \frac{\tan(45^\circ - \theta(T, VDD))}{R_{REF}(T, VDD)C_{REF}(T, VDD)} \tag{4.22}$$

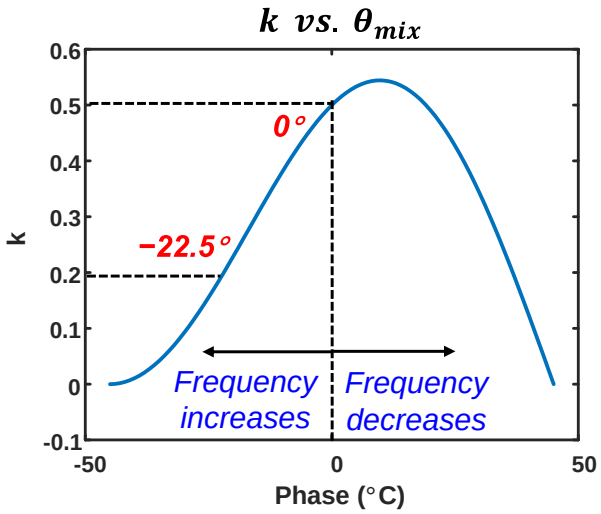


Figure 4.8: k versus different mixing phase

$\tan(\theta)$ includes both $\tan(\theta_{mix})$, which is the mixing phase and $\tan(\theta_{error})$ which is introduced by the limited bandwidth of the blocks. As is discussed in the previous section. $\tan(\theta_{mix})$ is determined by the frequency divider which is insensitive to the temperature and supply voltage. However, $\tan(\theta_{error})$ will vary over temperature and supply voltage because of the bandwidth variation. Fig. 4.9 shows how the phase variation will effect the frequency error. On-chip capacitor C_{REF} also has a negligible temperature coefficient (TC) and supply plays a minor role in altering the passive device R_{REF} and C_{REF}. Therefore, the TC of R_{REF} dominates the error in f_{nom}. For second-order effect, which mainly contributed by the LG, the following expression is performed,

$$\frac{\partial f_{osc}}{f_{osc}} \approx \frac{\partial LG}{LG_{nom}} \frac{1}{LG_{nom}} \tag{4.23}$$

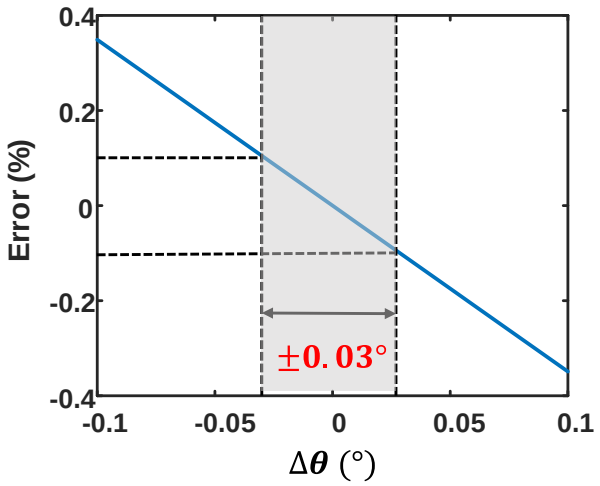


Figure 4.9: frequency error with phase variation

From (4.23), we can notice the second-order effect from LG will be attenuated by a factor of $\frac{1}{LG_{nom}}$ to impact the f_{osc}. As is shown in Fig. 4.10, assuming LG changes by 100%, $1/LG_{nom}$ should be designed to be higher than 120 dB to achieve less than 1 ppm error caused by LG variation. As almost every blocks in the loop contributes the LG, the design strategies will be both increasing the LG and design LG less sensitive to temperature and supply voltage.

4.3.3 Noise Analysis

In this section, the FLL noise analysis based on the linear system. The noise performance, especially the flicker noise in low frequency is deterministic to the oscillator long-term stability, which is essential for application such as wake-up timer. A comprehensive noise model is shown in Fig. 4.11, indicating four major random

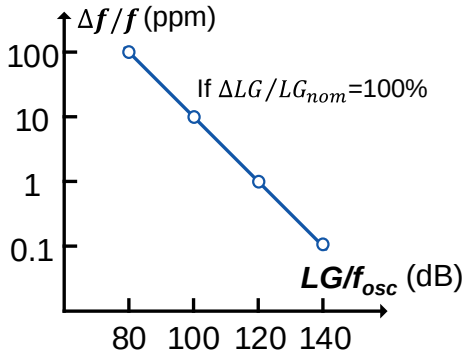


Figure 4.10: f_{osc} second-order error by LG at different LG/f_{osc} cases

noise sources in the proposed FLL: $V_{n,FVC}$, $V_{n,Mix}$, $V_{n,LPF}$, $V_{n,INT}$ and ϕ_{VCO} from FVC, mixer, low-pass filter, integrator and VCO. In order to simplify the analysis, the total voltage noise referred to the FVC output can be written as,

$$V_{n,t}^2 = V_{n,FVC}^2 + V_{n,Mix}^2 + \frac{V_{n,LPF}^2}{G_{Mix}^2} + \frac{V_{n,INT}^2}{G_{Mix}^2 G_{LPF}^2} \tag{4.24}$$

Using the model, the transfer function from the source $V_{n,t}$ and ϕ_{VCO} to the frequency fluctuations $S_{osc}(f)$ of the FLL can be calculated as,

$$\frac{S_{osc}(f)}{S_{V_{n,t}}(f)} = \frac{M \cdot G_{Mix} G_{LPF} G_{INT} f_{INT} k_{VCO}}{Ms + G_{FV} G_{Mix} G_{LPF} G_{INT} f_{INT} k_{VCO}} = \frac{M \cdot LG/G_{FV}}{Ms + LG} \tag{4.25}$$

$$\frac{S_{osc}(f)}{S_{\phi_{VCO}}(f)} = \frac{Ms^2}{2\pi(Ms + G_{FV} G_{Mix} G_{LPF} G_{INT} f_{INT} k_{VCO})} \tag{4.26}$$

From Fig. 4.12, the noise transfer function by voltage noise $V_{n,t}$ is first-order low-pass filtered and noise transfer function by phase noise of VCO is first second-order

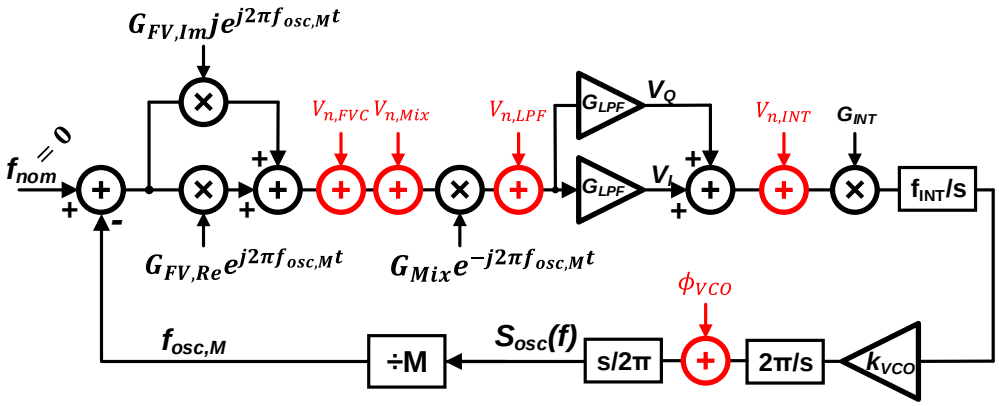


Figure 4.11: Linearized noise model of proposed FLL

high-pass filtered and then first-order high-pass filtered. In order to determine the long-term frequency stability, Allan Variance is adopted to characterize the noise performance base on the noise function in frequency domain. The Allan Variance $\sigma^2_{osc}(\tau)$ at gate time τ is given as,

$$\sigma^2_{osc}(\tau) = \int S_{osc}(f) \frac{2\sin^4(\pi\tau f)}{(\pi\tau f)^2}\, df \tag{4.27}$$

Fig. 4.13 shows a typical Allan deviation plot for an oscillator. With short gate time, Allan deviation σ_{osc} is inversely proportional to $\tau^{-0.5}$ dominated by the white thermal noise. With relative longer gate time, flicker noise dominates and Allan deviation becomes constant over gate time. Therefore, the Allan deviation floor is determined by the low-frequency flicker noise component in $S_{osc}(f)$. Observed from Fig. 4.12, noise transfer function of VCO phase noise has a +40 dB/dec high-pass characteristic in low frequency region, which will nullify the flicker noise (-30 dB/dec) contributed

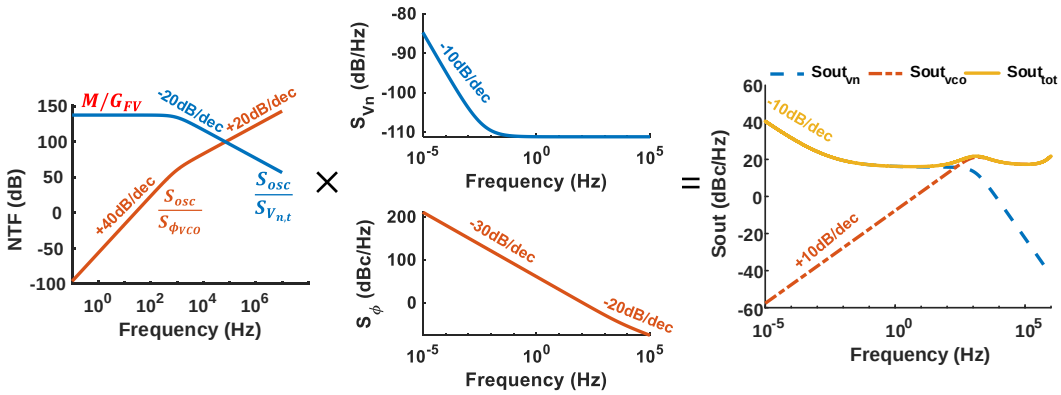


Figure 4.12: Noise transfer function plots according to (4.25) and (4.26); PSD of modeled voltage noise and phase noise; PSD of output frequency fluctuation

by VCO. Thus, the Allan deviation floor will be dominated by the flicker noise component in $V_{n,t}$. As the flicker noise contribution of $V_{n,FVC}$ and $V_{n,Mix}$ will be moved to higher frequency band by mixing, and the low-pass filter can be implemented in fully-passive approach which is free from flicker noise. The main contribution of flicker noise source is from $V_{n,INT}$ by the amplifier implemented in integrator. Fig. 4.14 shows how the Allan Deviation will vary with different integrator flicker noise.

4.4 Circuit Implementation

The detail circuit implementation of proposed impedance IQ-balanced FLL is shown in Fig. 4.15. The differential FVC includes a pair of differential harmonic-canceling current sources and RC parallel reference impedance. The current source is driven by 7 different clock phases at frequency of $f_{osc}/16$. The differential FVC

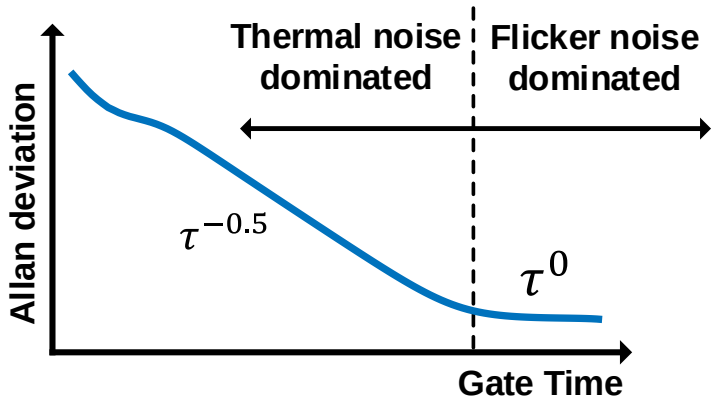


Figure 4.13: Allan deviation (log-log) plot at gate time τ.

output voltage V_{REF} is buffered through a source follower (SF) buffer and down-converted at $f_{osc}/16$. The in-phase and quadrature DC component down-conversion are performed by two parallel NRZ passive mixers driven by in-phase and quadrature clock, and then are summed in current-domain, yielding a differential output V^{+}_{MIX} and V^{-}_{MIX}. The down-conversion mixing phase can be selected by the digital MUX to enable alternative phase mixing. A RC filter performs low-pass filtering after mixer, preserving only DC component. A two-stage amplifier integrator with first-stage chopper-stabilized OTA. Chopping frequency is generated by dividing the mixing clock with a frequency of $f_{OSC}/256$. Capacitor C_{INT} determines the dominant pole of the FLL and C_{FILT} at the output is introduced to attenuate the chopping ripple. Integrator output voltage V_C serves the control voltage for VCO, generating output frequency as f_{OSC} in the closed-loop. f_{OSC} is divided by 16 and phase-split by the flip-flop-based frequency divider to generate the clock ($\phi_{-67.5}$ ϕ_{-45} ... $\phi_{67.5}$) for driving current source. The design details for each block will be provided in the

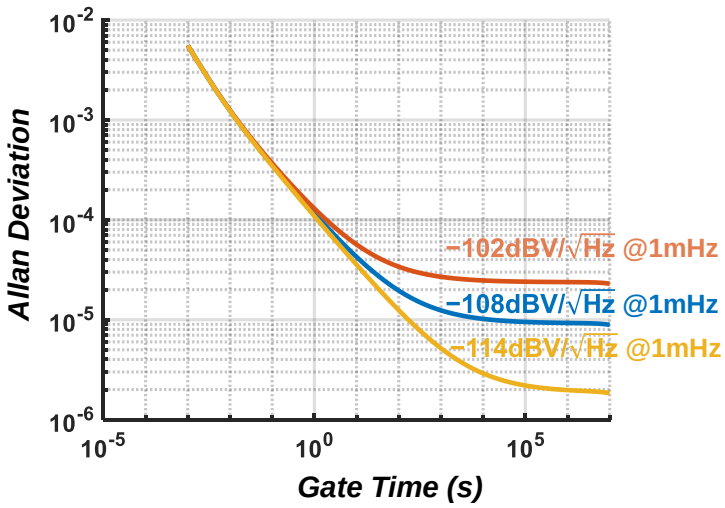


Figure 4.14: Allan Deviation with different integrator noise

following section.

4.4.1 Frequency Voltage Converter

The above-mentioned analysis with impedance IQ-balance all have the prerequisite that is the accurate extraction of both real and imaginary component of the impedance, which particularly requires a single-tone harmonics-free sinusoid waveform excitation. However, on-chip sine-wave generator with high spurious-free dynamic range (SFDR) is power-hungry and sophisticated to design. In this work, we take advantage of the existing frequency divider and multi-phase clock to build a harmonic-cancelling sine-wave current generator. As is shown in Fig. 4.16, 7 clock phases, each with 22.5° phase difference, are used to drive the switches for turning

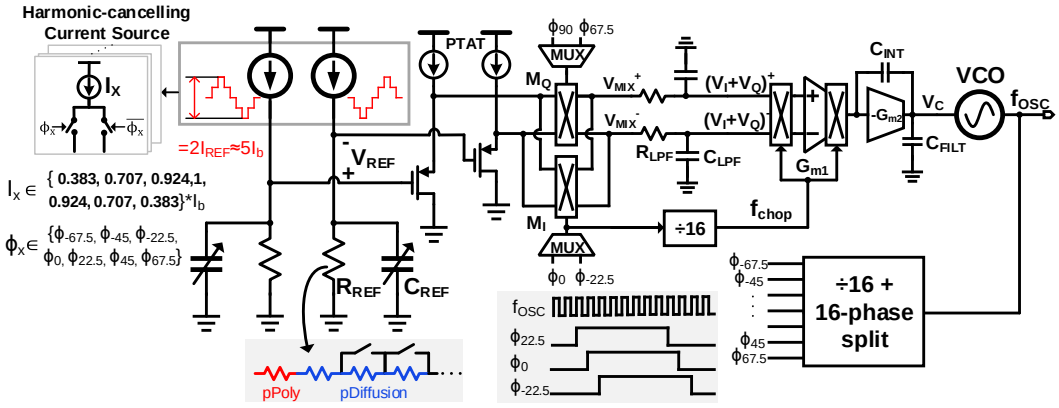


Figure 4.15: Schematic of impedance IQ-balanced FLL.

on the current source. Seven current source, which is properly weighted based on the phase sequence to cancel out the harmonics steers the current differentially into reference impedance pair. With 7-phase square-waves, up to 14^{th} harmonic can be effectively cancelled. The remaining 15^{th} harmonic theoretically has the magnitude of $-20\log(15)$ dBc. Fig. 4.17 shows the relative frequency error when $|Z_{Re}| = |Z_{Im}|$ holds. With pure square-wave excitation, the nominal oscillation frequency present 30% error; With 7-phase cancellation, the frequency error can be reduced less than 2%. Although, more finer phases used in this architecture lead to smaller static frequency offset, a higher divider ratio and output frequency will be required, which places extra limitation in design. Actually, the static frequency offset is not the main concern in this design as long as the offset is not temperature and supply voltage dependent. Fig. 4.18 shows the PSS simulation results of current source phase variation over temperature and supply voltage operating at 50 kHz with R_{REF}=2 MΩ and C_{REF}=1.59 pF. Across temperature -20°C to 80°C, the phase variation is only

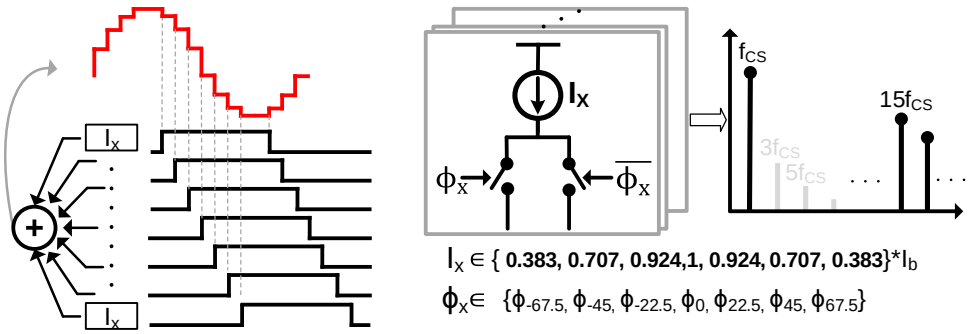


Figure 4.16: Harmonic-cancelled step-wise sinusoid waveform generation using phase-shifted square wave.

0.0036°(80 ppm in phase). The phase variation from supply voltage 1.2 V to 1.8 V is 0.053°(1177 ppm in phase), much significant than temperature effect due to the variation of switch-on time by the clock amplitude.

The reference impedance schematic including R_{REF} and C_{REF} is shown in Fig. 4.19a. C_{REF} is implemented by the MIM capacitor with negligible TC, and 3-bit digitally adjusted from 0.6 to 1.3pF. R_{REF} is designed with a 2.2 MΩ p+ polysilicon resistor (negative TC) and a 5-bit tunable p+ diffusion resistor (positive TC). The TC of the total R_{REF} is compensated in first order by properly rationing the p+ polysilicon resistor and p+ diffusion resistor. The temperature drift of both poly-resistor and diffusion resistor with their compensation simulation results are plotted in Fig. 4.19b. The simulation result shows with the ratio as 1 : 0.19 between R_{poly} and R_{diff}, the total R_{REF} presents a TC of 21 ppm/°C.

As is discussed in the previous section, large R_{REF} help reduce the power consumption of FVC. In conventional FVC design, it is a standard design choice to

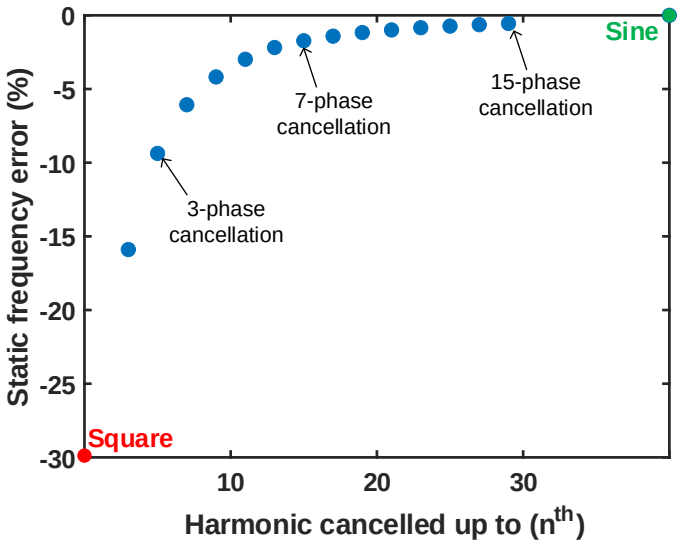


Figure 4.17: Static frequency error when $|Z_{Re}| = |Z_{Im}|$ holds by excitation with different harmonic cancellation.

trade area for power. However, for proposed phase-sensing FVC, implementing large R_{REF} will introduce extra excess phase delay as bulky-size polysilicon resistor adds parasitic capacitance between polysilicon and substrate. As is shown in Fig. 4.20, Z_{REF}(R_{REF}=4M Ω, C_{REF}=800 fF) phase with an ideal and actual poly-resistor implementation. With ideal resistor, -45° phase shift gives expected 50 kHz. However, with actual poly-resistor, -45° phase shift gives only 16.6 kHz. This issue can be solved by using alternative phase mixing, demonstrating another benefit of alternative phase mixing.

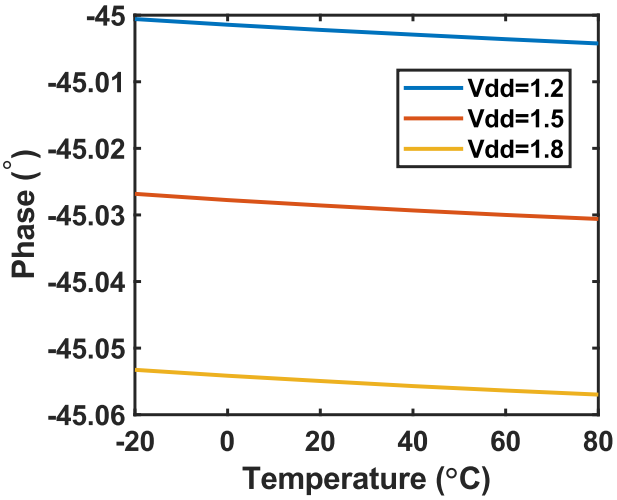
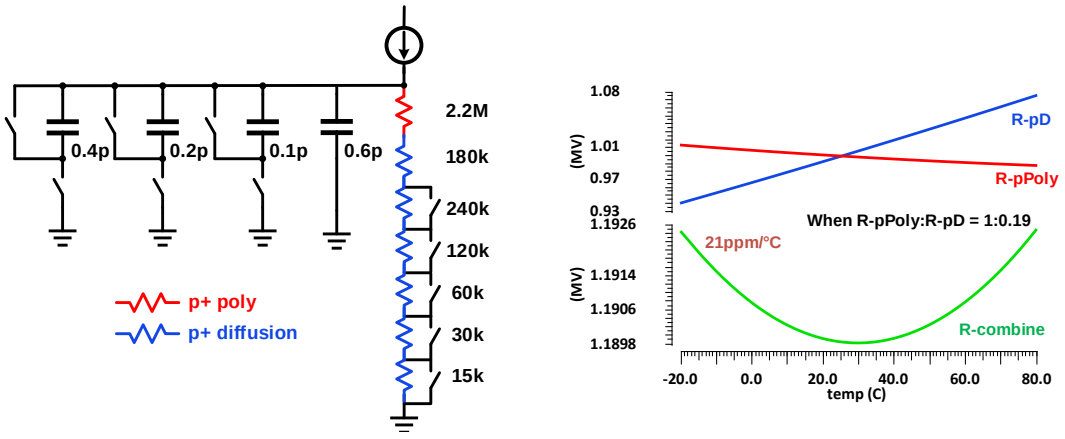


Figure 4.18: Output phase variation of current source over temperature and supply voltage.

4.4.2 IQ-Balanced Mixer

Fig. 4.21 shows the schematic of the proposed IQ-balanced mixer, which includes three parts: 1) the PMOS input source follower working as the buffer to decouple FVC from subsequent stages. 2) Double parallel NRZ passive mixers driven by in-phase and quadrature clock, serving the function of down-converting and voltage summation (V_I+V_Q); 3) the RC passive low-pass filter which filters out the high frequency component after frequency mixing. The final output of the IQ-balanced mixer is the differential version of V_I+V_Q.

As the buffer stage is still operated in frequency f_{nom}, the buffer stage bandwidth should be higher enough, avoiding to introduce any phase delay offset to V_{REF}, which directly effect the frequency stability of the FLL. The source follower is chosen be-



(a) (b)

Figure 4.19: (a) Schematic of reference capacitance and reference resistance. (b) Simulation results of TC compensation between R_{poly} and R_{diff}.

cause of its highest GBW and low-gain for the given current consumption. Besides, the input common-mode can be preserved with no extra common-mode control is required in source follower stage, which also saves the power. Because of its open-loop and two-transistor operation, minimum parasitic capacitance is associated with the source follower, which gives the highest GBW in various topologies. Furthermore, because of its low gain ($\approx 0dB$), maximum bandwidth can be achieved with minimum current consumption, increase the energy efficiency. However, extending bandwidth to the point that does not effect the V_{REF} phase still consumes considerable power. Therefore, PTAT current source is used for source-follower to reduce the bandwidth variation over temperature as main concern in this work is the frequency variation over temperature. The source follower is biased at 45 nA and 9 nA for biasing, yielding 99 nA current consumption in total.

The passive NRZ mixers are adopted for mixing due to its low-gain and simple-

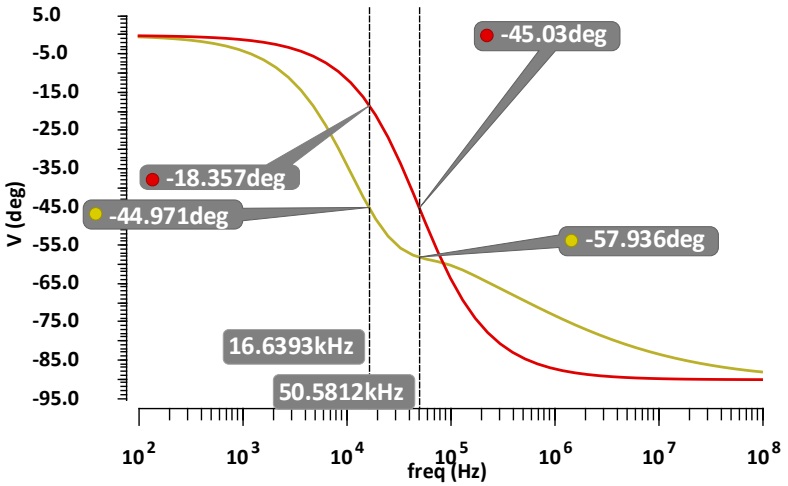


Figure 4.20: Parasitic capacitance in resistor implementation causes extra phase shift of Z_{REF}, limiting FVC maximum achievable frequency.

implementation as well. The mixing clock is reconfigurable by selecting the mixing phase using digital multiplexer. RC low-pass filter is added after mixer because its purely passive implementation for not introducing flicker noise. The resistor is 1 MΩ and the capacitor is designed as 16 pF. Fig. 4.22 presents the transient waveform of the key nodes in mixer during the frequency locking period, showing the operating principle of the mixer.

4.4.3 Integrator

The integrator in this work is implemented as two-stage amplifier with miller capacitor to increase the loop gain. The first stage is a chopper-stabilized fold-cascode OTA with PMOS input pair. The second stage is a common-source output

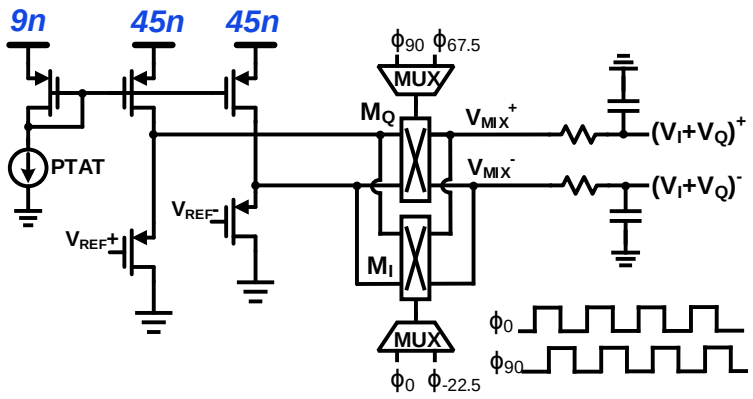


Figure 4.21: Schematic of IQ-Balanced mixer including source-follower, two NRZ passive mixers, and low-pass-filer.

stage. The PMOS pair in the first stage is biased at 4 nA current and sized as 1u/10u (W/L) to reduce the flicker noise. With 32 pF miller capacitor. The GBW of the integrator is approximated as 250 Hz. A 16 pF capacitor is introduced at the output of the integrator to attenuate the high frequency ripple introduced by chopping and the previous stage mixing. The output stage is bias with 18 nA current to push the zero introduced by the miller capacitor to higher frequency, avoiding flat gain in the ripple frequency.

Fig. 4.24a and Fig. 4.24b shows the simulation results of DC gain and GBW over temperature and supply voltage, respectively. Although the DC gain at 1.2 V has 3 dB variation (41.25%), large nominal integrator DC gain (>120 dB) contributes the FLL loop gain more than 150 dB, which makes the integrator DC variation negligible for output frequency variation. GBW variation in simulation is around 17.3% across temperature -20°C to 80°C and 16.4% across 1.2 V to 1.8 V supply voltage. The

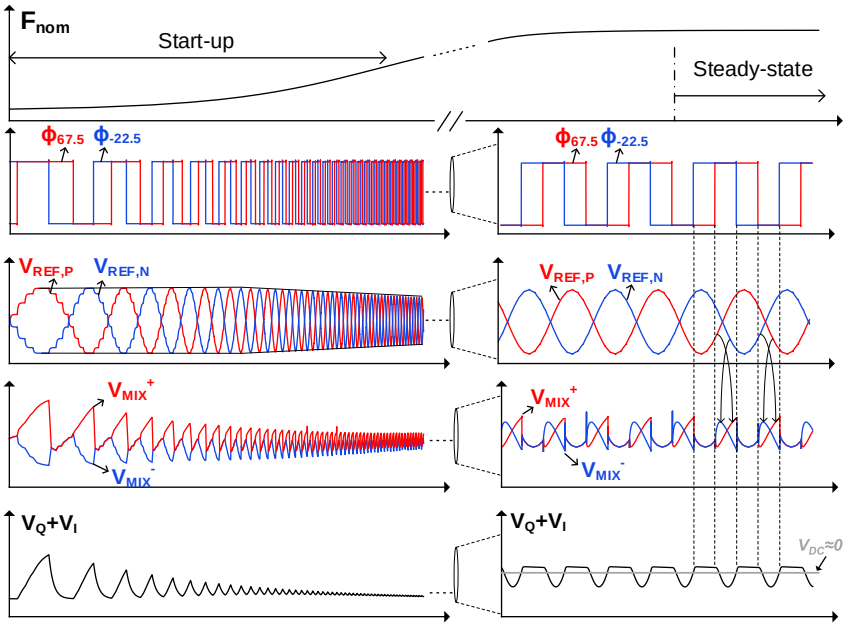


Figure 4.22: Simulated transient voltage waveform of the key nodes in mixer during frequency locking period.

GBW variation will not effect the frequency stability, but only change the settling time of the FLL. Fig. 4.24c shows the noise simulation results of the integrator in this work, showing a -116 dB $V/\sqrt{Hz}$ white noise floor and a -114 dB $V/\sqrt{Hz}$ noise at 1m Hz.

4.4.4 Voltage Control Oscillator

The schematic of VCO implemented in this work is shown in Fig. 4.25. The constant-energy-ring-oscillator (CERO) topology proposed in [42] is adopted to reduce the short-circuit power consumption. Three-stage CERO delay cell form the

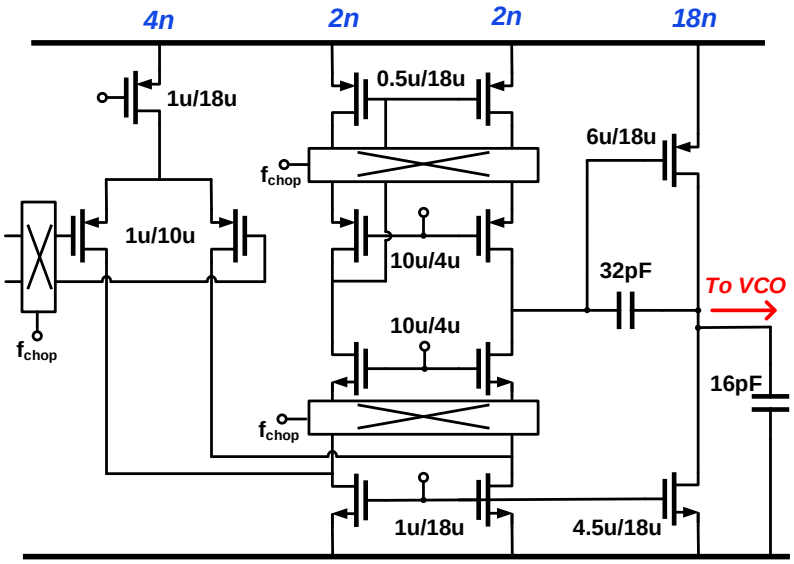


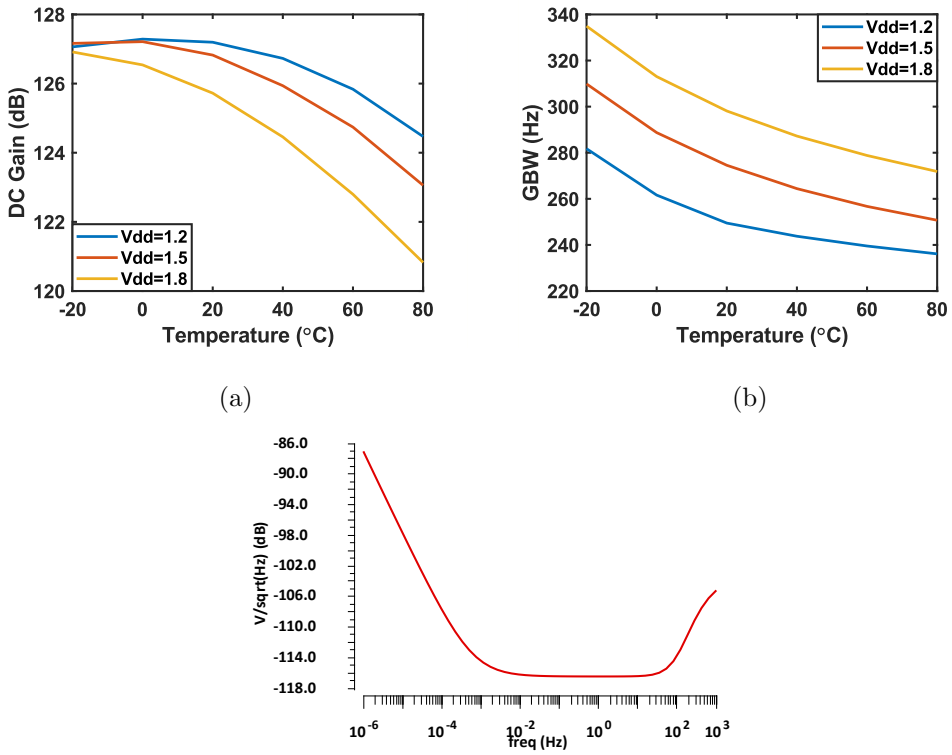
Figure 4.23: Schematic of integrator amplifier.

ring oscillator. Control voltage from the integrator V_{bn} generates the PMOS side control voltage V_{bp} to control the leakage-based current-source in the delay cell. The transistors in delay cell are all designed in minimum size to reduce extra capacitor.

Fig. 4.25 shows the simulation results of output frequency versus VCO control voltage at -20°C, 30°C, and 80°C. The VCO gain at 1.2 MHz output frequency in each cases are 27, 32, and 23.5 MHz/V, presenting a variation of 30% over the temperature. Fig. 4.26b presents the VCO phase noise when output frequency is 1.5 MHz.

4.5 Measurement Results

The prototype chip was fabricated in 0.18μm CMOS process with an area of 0.168 mm^2(die photon shown in Fig. 4.27).



(a) (b)

(c)

Figure 4.24: Simulation results of (a) DC gain and (b) gain-bandwidth-product (GBW) variation over temperature and supply voltage. (c) Noise simulation of the integrator.

Fig. 4.28 shows the measured frequency locking transient waveform of the prototype. The startup response is first shown and ¡10 ms locking time is obtained after the operating point is settled. The settling behavior of switching from mixing phase ϕ_0 to $\phi_{-22.5}$ is also presented, showing frequency switching from 790 kHz to 1.59 MHz in less than 4 ms.

Frequency stability measurement over temperature and supply are presented in

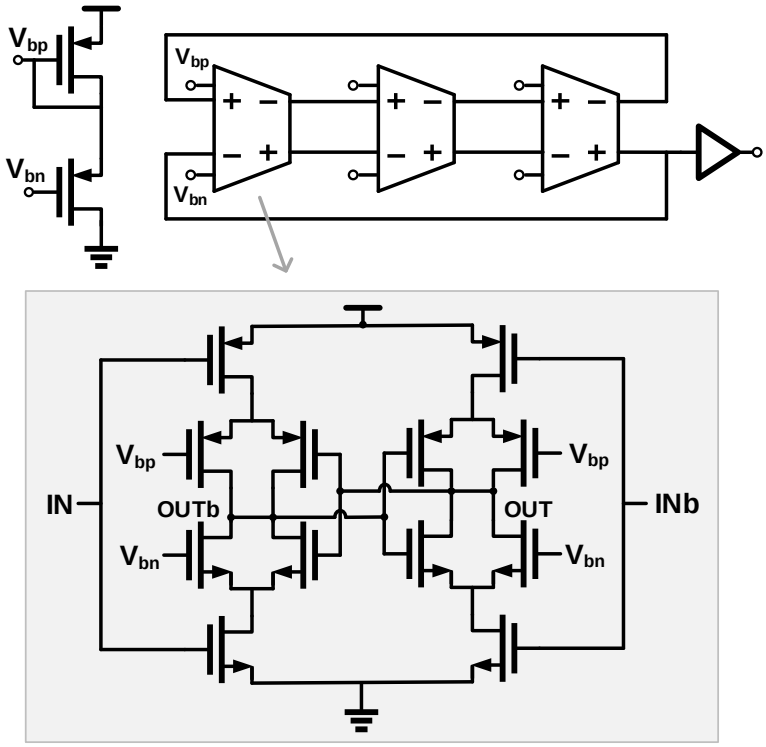
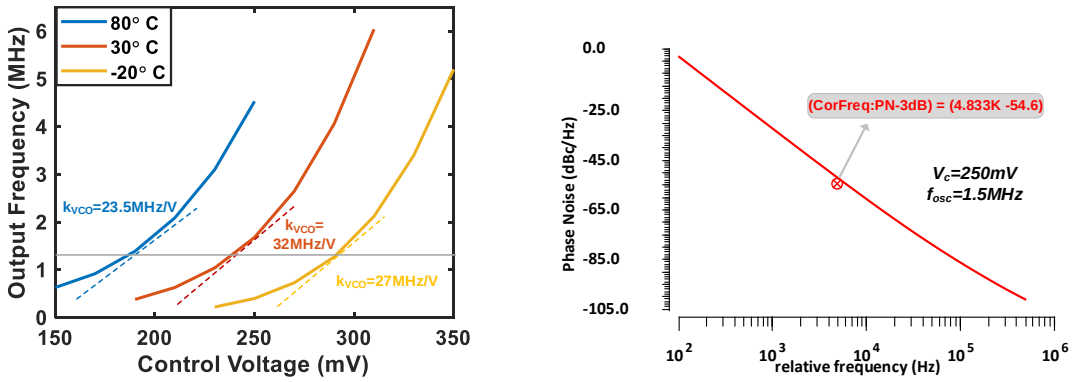


Figure 4.25: Schematic of voltage-controlled oscillator

Fig. 4.29 using both ϕ_0 and $\phi_{-22.5}$ mixing phase. For frequency over temperature measurement, on-chip two-point trimming is first performed to obtain the lowest TC. The nominal frequency after trimming is 650 kHz and 1.39MHz in ϕ_0 and $\phi_{-22.5}$, respectively. Frequency is measured from -20°C to 80°C at 1.2 V supply voltage. Results from two samples are averaged and presented. For ϕ_0 mixing phase, the frequency variation is 0.254%, indicating a TC of 25.4 ppm/°C; For $\phi_{-22.5}$ mixing phase, the frequency variation is 0.36%, indicating a TC of 36 ppm/°C; The FLL operated at ϕ_0 mixing phase shows a superior TC than operated at $\phi_{-22.5}$ mixing



(a) (b)

Figure 4.26: (a) VCO output frequency versus control voltage across various temperature. (b) Simulation result of VCO phase noise.

phase because of the lower operating frequency, is less sensitive to the phase variation. The frequency stability over supply voltage is measured at temperature of 25°C with supply voltage varies from 1.2 V to 1.9 V. For ϕ_0 mixing phase, frequency error across the voltage range is 0.19%, yielding a 0.27%/V line sensitivity. For $\phi_{-22.5}$ mixing phase, frequency error across the voltage range is 0.47%, yielding a 0.67%/V line sensitivity.

Long term stability measurement result is presented using Allan deviation in Fig. 4.30. This chip achieves 10 ppm operating in ϕ_0 mixing phase and 15 ppm operating at $\phi_{-22.5}$ mixing phase after 100 s gate time. The Allan deviation floor in $\phi_{-22.5}$ case is higher because higher operating frequency achieves more gain attenuation in FVC, worsening the noise performance.

Fig. 4.31 depicts the power consumption and power breakdown in both ϕ_0 and $\phi_{-22.5}$ mixing phase case, operating at 1.2 V and 25°C. For ϕ_0, the total power con-

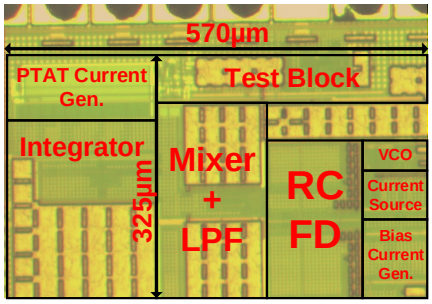


Figure 4.27: Die photo of proposed FLL prototype.

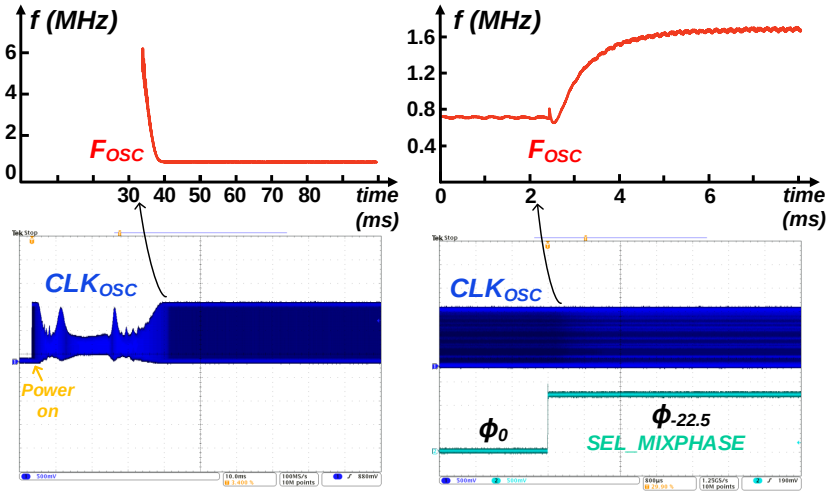
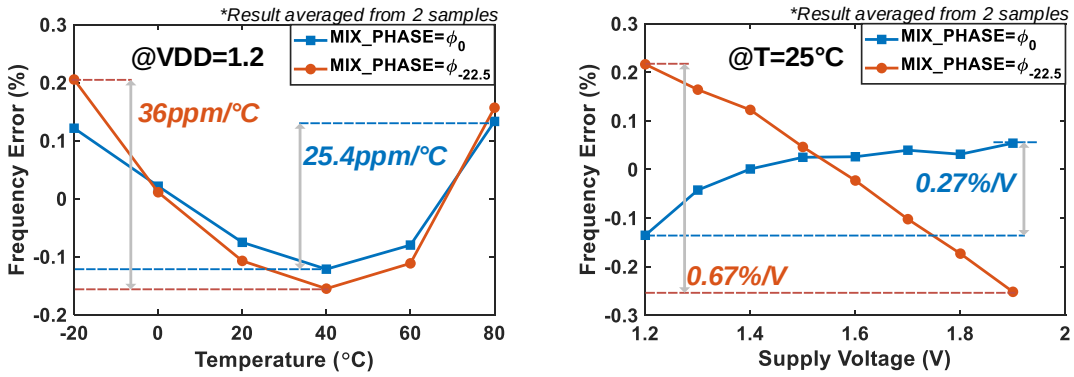


Figure 4.28: Transient waveform of proposed FLL.

sumption is 820.2nW and for $\phi_{-22.5}$, the power consumption is 1.23 uW. Because no extra static power is added in $\phi_{-22.5}$ case for higher output frequency, FLL operating at $\phi_{-22.5}$ achieves better energy-per-cycle (EPC) performance (0.89pJ/Cycle) than ϕ_0 case (1.26pJ/Cycle).

A comparison table between this work and state-of-art low-power RC oscillator is shown in Table 4.6.



(a) (b)

Figure 4.29: Frequency error over (a) temperature and (b) supply voltage for both ϕ_0 and $\phi_{-22.5}$ mixing phase.

4.6 Conclusion

In this section, we present a novel FVC which is based on the AC current source and impedance sensing technique. The new FVC is compared with traditional resistor and switch-capacitor FVC in terms of gain, noise, power, and area cost. By adopting the novel FVC, a impedance IQ-balanced FLL architecture is presented. The operating principle is introduced, followed by the linear system analysis with all the non-idealities. Then the circuit implementation for each block and design consideration is presented. Finally, a chip prototype fabricated in 180 nm CMOS process is presented and measured. The measurement results are performed.

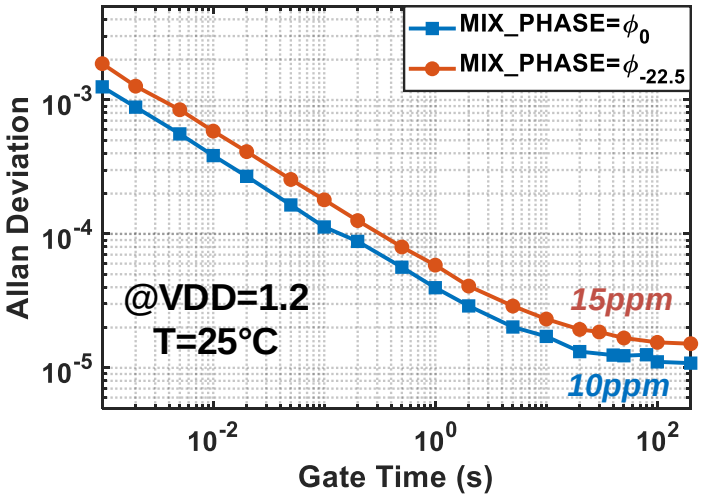


Figure 4.30: Allan deviation with gate time for both ϕ_0 and $\phi_{-22.5}$ mixing phase.

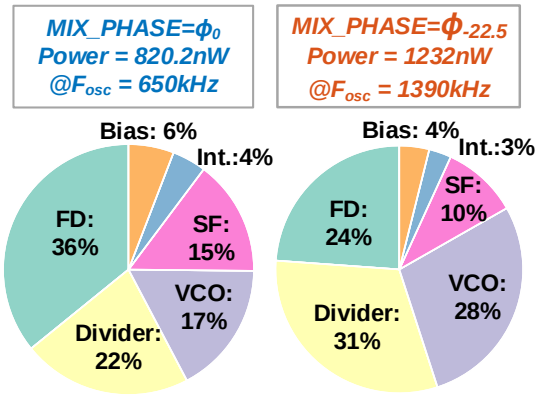


Figure 4.31: Power break down of FLL operating at 1.2 V for ϕ_0 and $\phi_{-22.5}$ mixing phase

Table 4.6: Performance comparison with state-of-art RC oscillators

References	**This work**		ISSCC'15	CICC'19	TCASI'20	JSSC'16	ISSCC'16	JSSC'18
Process (nm)	**180**		180	180	40	180	180	180
VDD (V)	**1.2**		1.4	1.2-1.9	0.8	1.3	0.85-1.4	1.2
Area (mm^2)	**0.168**		0.086	0.145	0.07	0.26	0.5	0.16
Frequency Locking Architecture	**Impedance Sesning FD + AFLL**		Diff. RC Charging FD + AFLL	SC-R FD+ AFLL	Diff. RC Charging FD + DFLL	SC-R FD+ AFLL	SC-R FD+ AFLL	SC-R FD+ AFLL
Frequency (Hz)	**650**	**1390**	4700	66.9	417	70.4	3	32.7
Power (nW)	**820.2**	**1232**	53000	56	240	110	4.7	35.4
Energy/Cycle (pJ/Cycle)	**1.26**	**0.89**	11.3	0.84	0.57	1.56	1.6	1.08
Line Sensitivity (%/V)	**0.27 @ 1.2-1.9**	**0.67 @ 1.2-1.9**	±0.1 @ 1.4-3.3	0.4 @ 1.2-1.9	1.06 @ 0.7-0.9	±0.23 @ 1.2-1.8	±0.14 @ 0.85-1.4	0.44 @ 1.2-1.8
TC (ppm/$^\circ C$)	**25.4 @ -20-80**$^\circ C$	**36 @ -20-80**$^\circ C$	42 @ -40-125$^\circ C$	9.8 @ -20-100$^\circ C$	33@ -20-80$^\circ C$	34.3@ -40-80$^\circ C$	13.8@ -25-85$^\circ C$	13.2@ -20-100$^\circ C$
Allan Deviation (ppm)	**10**	**15**	-	60	12	7	63	<10

Chapter 5: List of Contributions

This thesis presents 1) a impedance sensor for source-differential flow cytometry; 2) a tunable readout IC for impedance spectroscopy and amperometric measurement of electrochemical sensors. 3) a RC oscillator using impedance IQ-balanced frequency-locked-loop. Following is the contribution of each work:

- A hybrid-feedack impedance analyzer architecture is introduced which maintains high closed-loop gain as well as SNR in cell detection mid-band frequency range. The implemented modulation/demodulation sensing architecture supports an operating frequency from 50 kHz to 40 MHz with adjustable bandwidth. The proposed impedance analyzer IC achieves 5x better capacitance resolution as well as 10x less power consumption compared with previous work.

- The system is demonstrated using a custom microfluidic flow cell and standardized 3-10μm polymer microbead solutions for analysis of counting and characterization sensivity and resolution under flow. As shown, 3m diameter beads are detected with 22dB SNR, offering a theoretical detection limit for cell sizes below 1μm diameter.

- A low-noise multi-functional readout IC architecture for electrochemical sensing. Leveraging the proposed current buffer topology and reconfigurable delta sigma modulator, the IC can perform a wide range of input frequency and magnitude sensing with both impedance and amperometric sensing ability, which

appeals to various amperometric readout application such as EIS and CV in chemical and biomedical sensors.

- A novel frequency voltage converter (FVC) based on real and imagnary impedance difference is introduced and analyzed. By adopting the proposed FVC, a impedance IQ-balanced FLL architecture is presented with the advantage of phase-mixing frequency reconfigurability. A chip prototype is fabricated in 180nm CMOS process and measured.

Below is the publication list:

- S. Bose*, **B. Shen*** and M. L. Johnston, "A Batteryless Motion-Adaptive Heartbeat Detection System-on-Chip Powered by Human Body Heat," in IEEE Journal of Solid-State Circuits, vol. 55, no. 11, pp. 2902-2913, Nov. 2020.

- **B. Shen** and M.L. Johnston,"DC-100kHz tunable readout IC for impedance spectroscopy and amperometric measurement of electrochemical sensors,"2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, pp. 651-654, Aug. 2020.

- S. Bose*, **B. Shen***, and M. L. Johnston, "A 20W Heartbeat Detection System-on-Chip Powered by Human Body Heat for Self-Sustaining Wearable Healthcare," 2020 IEEE International Solid-State Circuits Conference (ISSCC).

- H. Ouh, **B. Shen**, and M.L. Johnston, "Combined in-pixel linear and single-photon avalanche diode operation with integrated biasing for wide-dynamic-range optical sensing," IEEE Journal of Solid-State Circuits (JSSC), vol. 55,

no. 2, pp. 392-403, 2020.

- **B. Shen**, S. Bose, and M.L. Johnston, "Fully-integrated charge pump design optimization for above-breakdown biasing of single-photon avalanche diodes in 0.13 m CMOS,"IEEE Transactions on Circuits and Systems I (TCAS-I): Regular Papers, vol. 66, no. 3, 2019, pp. 1258-1269.

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