AN ABSTRACT OF THE DISSERTATION OF

Shaan Sengupta for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on December 6, 2021.

Title: CMOS Transducers and Programmable Interface Circuits for Resource-Efficient Sensing Applications

Abstract approved: _____

Matthew L. Johnston

Modern sensors are complex systems comprising multiple sub-systems such as transducers, analog and mixed-signal interface circuits, digital processing circuits, and packaging. Over the last few decades, innovations in these sub-systems combined with their increased integration in complementary metal-oxide semiconductor (CMOS) processes have led to the rapid growth in sensors for the Internet-of-Things (IoT), wearable devices, and fundamental scientific instrumentation. This dissertation introduces novel ideas for various parts of a sensor signal chain.

First, CMOS-based transducers are introduced. Single-photon avalanche diodes (SPADs) fabricated in 0.18 μm and 0.13 μm standard CMOS processes are demonstrated and characterized for various optical sensing techniques. A resistor fabricated using standard CMOS-BEOL layers in a 0.18 μm process, is used to demonstrate a compact fully-integrated single-element flow sensor occupying less than 0.065 mm^2.

Second, front-end interface circuits for single-photon optical detectors are introduced. A fully integrated SPAD-based ambient light sensor using mostly digital circuits and fabricated in a 0.13 μm CMOS process is highlighted. It consumes 125 μW and achieves one of the lowest reported areas (0.046 mm^2) in the literature. A custom analog front-end (AFE) chip is fabricated in a 0.18 μm CMOS process for interfacing with a commercial silicon photomultiplier (SiPM) for gamma spectroscopy. It incorporates tunability of dynamic range and integration time, thus making it suitable for different detectors (i.e. SiPM and scintillator crystal combinations).

Third, non-linear analog-to-digital converters (NL-ADCs) are explored as a viable alternative to linear ADCs for information-aware non-uniform quantization and a widely programmable piecewise-linear ADC (PWL-ADC) prototype chip (0.18 μm CMOS) is used to validate this. With a 7-bit output word, it achieves 5.6-bit to 9.5-bit resolution in user-defined regions of the input full-scale range (FSR), while consuming 105 μW at a sampling frequency of 42kHz. Measurements with recorded ECG waveforms highlight the application-specific advantages of the PWL-ADC.

Finally, some of the aforementioned ideas are used at the system level in a gamma spectrometer realized on a printed circuit board (PCB). The PCB design includes the AFE and PWL-ADC IC chips, a commercial SiPM and scintillator crystal, and a field programmable gate array (FPGA) based digital back-end (DBE). Several linear and non-linear isotope spectra with variable energy bin-widths (ΔE/bin) are recorded and analyzed to demonstrate the utility of the proposed concepts for peak enhancement and improved peak discrimination in radiation spectroscopy.

CMOS Transducers and Programmable Interface Circuits for Resource-Efficient Sensing Applications

by

Shaan Sengupta

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APPROVED:

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Shaan Sengupta, Author

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Chapter 1: Introduction to Sensors

"First to fall over when the atmosphere is less than perfect; Your sensibilities are shaken by the slightest defect; You live your life like a canary in a coalmine"

– Gordon Sumner, *Canary In A Coalmine*

Humans, and indeed most living organisms, are constantly sensing their environments, both within and without. Sensing is a critical task that provides organic and inorganic systems with the information to take appropriate actions to accomplish their goals, which could be as diverse as threat detection and survival, regulating the temperature by turning a heater on or off, and closing the eyes in response to bright lights. While it is commonly believed that humans possess five senses: sight, smell, touch, hearing, and vision, as our understanding of the human body continues to evolve, this simplistic definition has been challenged. Nevertheless, irrespective of however many senses humans actually possess intrinsically, we have relied on additional sensors to augment or enhance our understanding of the world around us. An example of this is the canaries that were used in the mining industry until as recently as 1986, to detect colorless and odorless toxic gases such as carbon monoxide, which humans are not particularly good at detecting [1]. Fortunately, nowadays we have access to more humane, cheaper battery-powered gas sensors to do the same task.

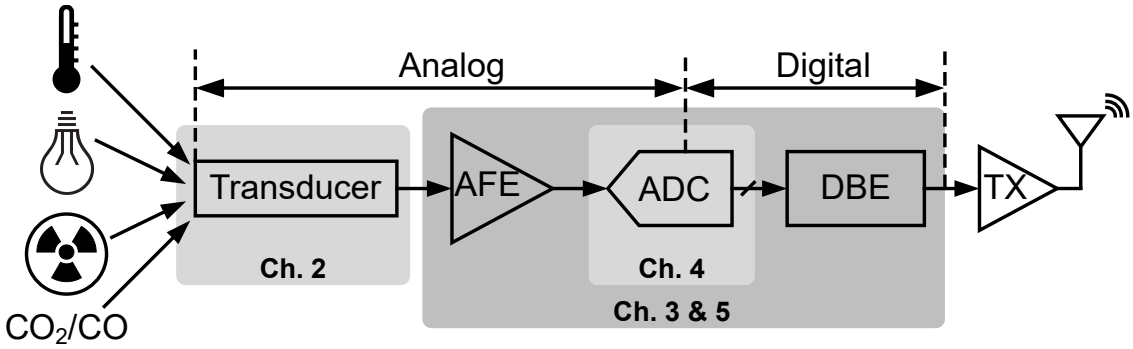


Figure 1.1: High-level illustration of an electronic sensor system with the major signal processing blocks highlighted. Chapters corresponding to specific sub-system(s) are annotated.

In the modern era, the word "sensor" is almost universally interpreted to be an electronic system as shown in Fig. 1.1. A typical sensor signal chain comprises the following sub-systems:

1. **Transducer**: This converts the physical quantity of interest (eg: temperature, light, etc.) into an electrical quantity such as charge, current or voltage. Typically, the transducer output is quite small (pC, nA or mV) and requires amplification. Additionally, the input-output relationship can be linear or non-linear, and this information can be exploited by the signal processing blocks.

2. **Analog Front-End (AFE)**: The primary task of this block is to amplify the input signal to obtain sufficient signal-to-noise (SNR) ratio and/or convert the input into a desired quantity, like current-to-voltage conversion in a transimpedance amplifier (TIA). Other tasks might include providing and controlling the appropriate bias for the transducer, and filtering and buffering prior to digitization.

3. **Analog-to-Digital Converter (ADC)**: The ADC samples and quantizes the AFE output into a digital word, which allows further digital signal processing using computers. This is a mixed-signal block since it translates between the analog and the digital domain. Successive-approximation-register (SAR) ADCs are a popular architecture used in sensor systems with resolutions ranging between 8 to 16 bits.

4. **Digital Back-End (DBE)**: The digital blocks comprise of a myriad of functions specific to the application of interest. These can range from simple ripple counting to histogramming to performing fast fourier transforms (FFTs). Increasingly, machine learning (ML) algorithms are also being implemented as part of the sensor's DBE.

5. **Wireless Transmitter (TX)**: Modern sensor systems typically include wireless communication blocks for the DBE output to be transferred to a host device like a computer or a smartphone.

Just as the adoption of complementary metal-oxide-semiconductor (CMOS) manufacturing processes revolutionized the computing industry with the integration of billions of transistors in a single chip, sensor systems have also witnessed similar benefits from the adoption of CMOS as an enabling technology. Particularly, the progress in integrated circuit (IC) implementations of signal processing and wireless blocks has been instrumental. These sub-systems are often integrated at the die or package level resulting in even lower cost, ease of system implementation, and improved performance. However, true system-on-chip integration where all the components are on the same CMOS substrate remains a challenge; specifically, the integration of novel transducers for new sensing modalities and emerging applications [2].

With increased integration and lowered costs, there has been an explosion of sensors in consumer and industrial applications. This has been fueled by the ever-growing influence of digitization in our lives, the automation of tasks and entire industries, and the insatiable appetite for more "information". Indeed, the sensors market, one of the biggest drivers in the semiconductor industry, is projected to grow to a value of more than $400 billion by 2026! With intelligent sensor nodes becoming ubiqutous, there has been a parallel growth in the amount of raw data generated by these nodes. According to a recent report [3], the number of sensors in the world will grow to ~ 45 trillion by 2032, corresponding to a data generation rate of $> 10^{20}$ bits/s. This is several orders of magnitude greater than the human data consumption rate of $\sim 10^{17}$ bits/s. Thus, there exists a very clear and obvious need to develop sensors that are more data-efficient by generating relevant and useful information that can be acted upon by intelligent systems.

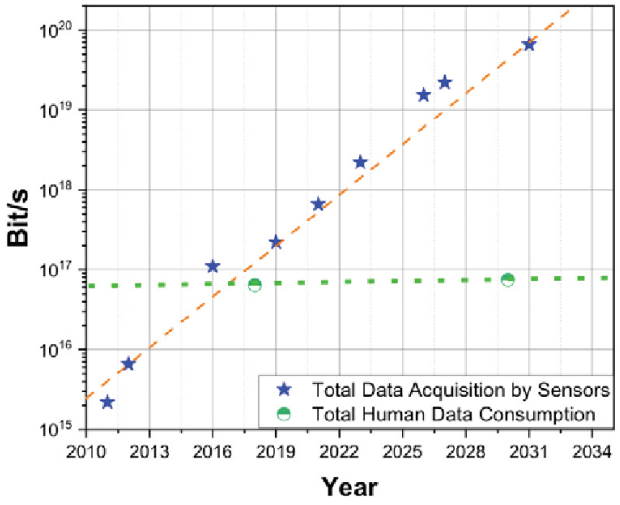


Figure 1.2: Sensor data projection from [3]

1.1 Dissertation Outline

Having established some key challenges in modern sensor systems, this dissertation aims to address some of these. The rest of this dissertation addresses two broad goals:

The first goal was the CMOS implementation of novel transducers that do not require additional post-processing. Several single-photon avalanche diodes (SPADs) and a resistive transducer were fabricated for optical sensing and flow sensing applications respectively. Chapter 2 focuses on their design, while Chapter 3 highlights how a particular SPAD design allows it to be used for ambient light sensinsg, leading to a massive reduction in area and system complexity. Highly digital interface circuits for SPAD readout are also introduced.

The second goal was the investigation of non-linear ADCs (NL-ADCs) for application specific quantization characteristics. This can lead to reduction in digital data and DBE resource utilization. Chapter 4 introduces the design of a new prototype piecewise-linear ADC (PWL-ADC) that incorporates programmability to extend the role of a single NL-ADC across a wide range of applications. To highlight system-level benefits, a gamma spectrometer with programmable energy bins and wide dynamic range is introduced in Chapter 5. The multichannel analyzer (MCA) in the spectrometer comprises the PWL-ADC IC and a custom programmable AFE IC (both fabricated in $0.18\,\mu$m. Besides the custom ICs, the spectrometer comprises a commerical silicon photomultiplier (SiPM) array and a FPGA-based DBE for recording linear and non-linear isotope spectra, demonstarting system level utility of the proposed ideas.

Chapter 2: Transducers in Standard CMOS Processes

A transducer is the first "processing" block in a sensor system, since it converts the physical quantity of interest into a variation of an electrical quantity like charge, current, voltage or impedance that can then be processed by readout electronics. Implementing the transducer of a sensor system in the same substrate as the interface and processing circuits has several benefits. Primary among these benefits are higher levels of integration resulting in reduced area, easier interfacing with readout circuits, and often, significantly improved performance (lower noise, higher bandwidth) owing to significantly reduced interconnect and packaging parasitics. Since CMOS processes are the de-facto standard for implementing integrated circuits, especially digital IPs,

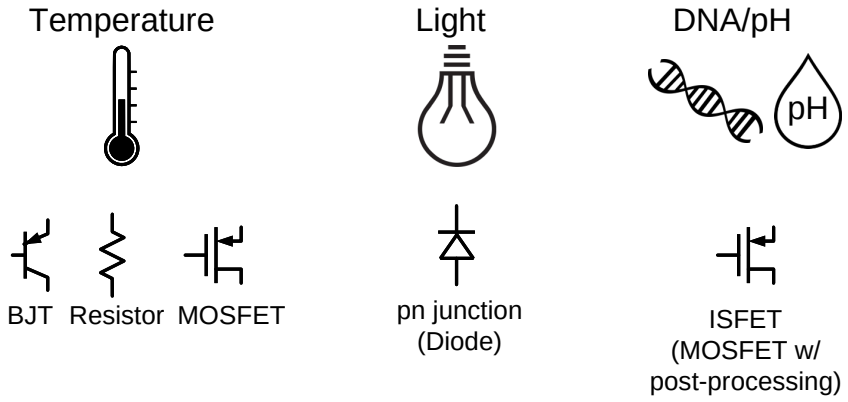


Figure 2.1: Examples of physical quantities and the corresponding CMOS-based transducer structures used to measure them in integrated sensors

it follows that realizing transducers in these processes is a highly useful exercise. Indeed, the widespread use of products like temperature sensors and image sensors in industrial, automotive, and consumer applications has been driven primarily by their CMOS implementations and continued innovations and improvements of these implementations. In the case of temperature sensors, the transducers are typically substrate *pnp* bipolar-junction transistors (BJTs), MOSFETs or a combination of polysilicon or diffusion resistors [4], while various flavors of reverse-biased p-n junction diodes are used as the pixels of image sensors [5]. In both cases, the structures are readily available in standard sub-micron CMOS processes and can be easily integrated with circuits. While specialized processes such as BiCMOS or dedicated CMOS Image Sensor (CIS) can be used to realize higher performance transducers, these tend to be more expensive, don't always scale well, and have limited IP vendors compared to standard CMOS processes.

Over the past couple of decades, novel CMOS-based transducers have not only continued to push the boundaries of existing sensing techniques, but have also given rise to entirely new types of sensors. For example, developments in CMOS single-photon avalanche diodes (SPADs) have pushed the boundaries of light detection and imaging, resulting in highly integrated imagers used in instrumentation for high-energy physics and the recent commercialization of Time-of-Flight (ToF) sensing for 3D imagers in smartphones. Similarly, Ion-sensitive field-effect transistors (ISFETs) realized in CMOS were instrumental in lowering the cost and processing time of DNA sequencing, and there is a growing body of work investigating their use in other electrochemical sensing applications.

The rest of this chapter focuses on two types of transducers implemented in standard CMOS processes: SPADs for optical sensing, and a resistive transducer for flow sensing. The goal here was to realize structures that can be used without any additional die-level post-processing. SPAD operation and design is particularly emphasized since Chapters 3 and 5 describe systems using SPAD-based sensors.

2.1 Single-Photon Avalanche Diodes for Optical Sensing

2.1.1 Background

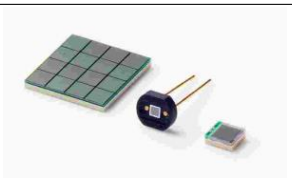
2.1.1.1 Brief History of Single-photon Detectors

Single-photon counting and time-correlated photon counting techniques have been used in a wide range of fields for several years now: cryptography, astronomy, optical communications, bio-medical research and laser ranging, among several others [6], [7]. More recently, single-photon counting has gained more attention than ever before. Bio-medicine is an area where it is finding increased usage for various imaging techniques like fluorescene lifetime imaging (FLIM), positron emission tomography (PET), and time-resolved Raman Spectroscopy [8], [9]. The other big area of thrust for single-photon detection is light detection and ranging (LiDAR). Specifically, the application of LiDAR in 3-D imaging for autonomous vehicles has rapidly accelerated the development of high-performance, low-cost single-photon detectors [10].

Single-photon detection was first developed in the 1960s by exploiting the high current gain performance of photomultiplier tubes (PMTs) [6], [11]. For photon count-

ing, PMTs are operated at high bias voltages ($> 100\,\text{V}$ and upto $1\,\text{kV}$) to achieve an average current gain of around 10^6 [11]–[13]. These devices exhibit moderate stability and low noise even at such high gain levels [11]. However, they are bulky, fragile and are sensitive to magnetic fields [7], [13], [14]. Additionally, the high bias voltages require expensive power supplies. Therefore, PMTs are expensive and somewhat limited in the scope of their applications. Solid-state single-photon detectors came to the fore in the 1990s [6], [8], [11]. These devices have been referred to in the literature as silicon photomultipliers (SiPMs) and are built from scalable arrays of single-photon avalanche diodes (SPADs). SPADs are sometimes also referred to as Geiger-mode avalanche photodiodes (G-APDs). This is because the operating principle of SPADs is similar to that of Geiger-Muller counters [11]. Compared to PMTs, SiPMs and SPADs require much lower bias voltages (10s of Volts), are much smaller, scalable, sturdier and are insensitive to magnetic fields [6], [7]. SPADs also have much

Table 2.1: Single-Photon Detectors Comparison [Image Source: Hamamatsu]

Device	Photomultiplier Tube (PMT)	Silicon Photomultiplier (SiPM)
Image		
Gain	$\sim 10^6$ - 10^7	$\sim 10^6$
Bias	$500\,\text{V}$ - $1\,\text{kV}$	$20\,\text{V}$ - $60\,\text{V}$
Size	Bulky	Compact & Scalable
Noise	Low	Medium
Magnetic Resist	No	Yes

higher detection efficiencies in the red and near-infrared (NIR) range [6]. A feature comparison of PMTs and SiPMs is shown in Table 2.1.

Until the early 2000s, silicon SPADs were fabricated exclusively through custom processes. This allows engineers to control dopant profiles and junction depths to tailor the device performance metrics like spectral response, detection efficiency, noise and timing jitter. SiPMs built from arrays such SPADs, continue to be manufactured in custom silicon processes by manufacturers for a variety of applications, particularly where large arrays and high fill-factors are required. Each pixel consists of a SPAD and an integrated quenching resistor in series with the SPAD. This type of SiPM is often referred to as "Analog" SiPM [15], since the output is an analog current pulse corresponding to incident photon flux. This is usually converted into a voltage by a transimpedance or charge amplifier, followed by digitization by an analog-to-digital converter (ADC) for computer recordings or digital signal processing (Fig. 2.2(a)). In these Analog SiPMs, the readout and processing electronics are external to the detector, which limits system integration, timing performance, as well as cost.

The next major milestone in SPAD design was the exploitation of CMOS processes to design planar SPAD structures. Standard CMOS processes constrain the development of fully customized structural features of SPADs such as doping levels, implant and diffusion depths, and well structures. The lack of access to specific process recipes from semiconductor fabs makes it almost impossible to perform reliable TCAD simulations to predict SPAD performance. As a result, CMOS SPADs typically perform worse when compared to fully customized SPADs. However, several groups have continued to work on developing better CMOS SPADs because of the

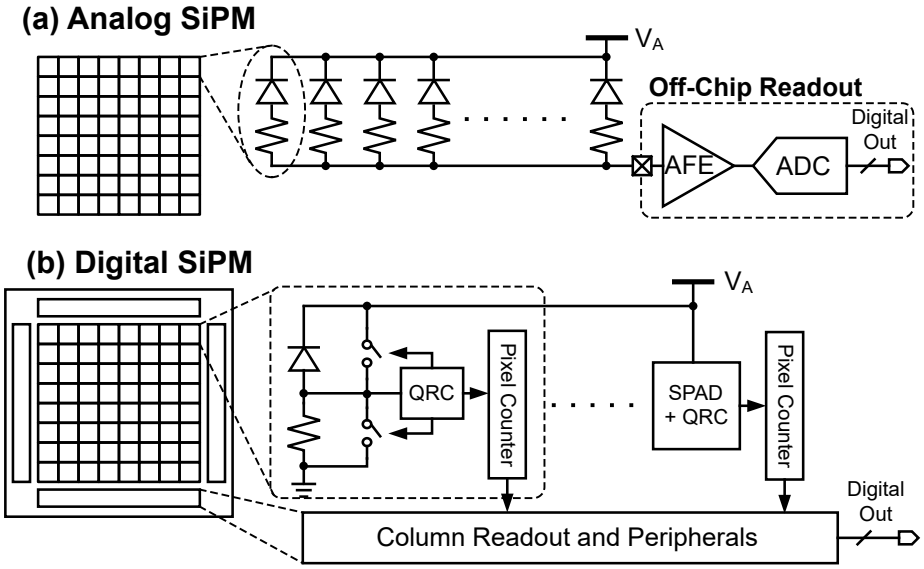


Figure 2.2: Conceptual views of (a) Analog SiPMs with off-chip readout and digitization circuits, and (b) Digital SiPMs with on-chip pixel-level integration of digitization and counting circuits.

ease of integration with other blocks on the same chip. These blocks include the analog/mixed-signal sensing circuits and the digital electronics for on-chip counting and photon timing processing [7]. In arrayed implementations, pixel-level integration of SPADs and circuits is made possible, resulting in digital outputs from each pixel (Fig. 2.2(b)). These arrays are sometimes referred to as "Digital" SiPMs [16] and can utilize counting-based techniques, greatly simplifying system complexity and cost. This makes CMOS SPADs a highly attractive low-cost and durable solution for a wide range of photon counting and timing based applications.

2.1.1.2 SPAD Operating Principle

A SPAD is a *p-n* junction operating in the Geiger mode, i.e. reverse biased beyond its breakdown voltage, V_B as shown in Fig. 2.3. Impact ionization is the mechanism by which the avalanche multiplication of charge carriers occurs in this mode. For the depletion region $z_0 - z_1$ in Fig. 2.4, the breakdown voltage is defined as the voltage at which the mean ionization per free carrier, $\langle\alpha\rangle$ equals unity [8], [17], [18]. Therefore, the condition for avalanche is defined by 2.1:

$$\int_{z_0}^{z_1} \langle\alpha\rangle dz > 1 \tag{2.1}$$

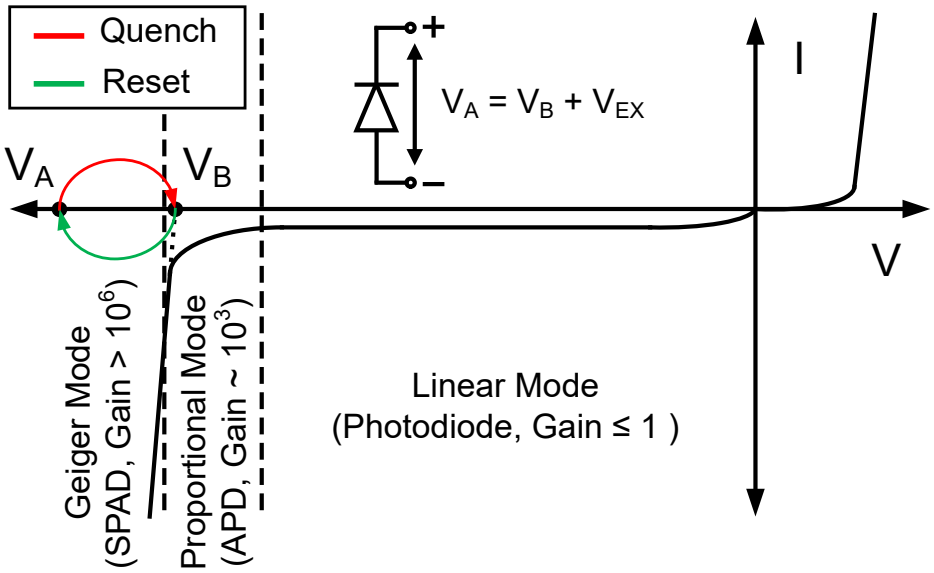


Figure 2.3: Different operating regions of a *p-n* junction diode based on applied reverse voltage. Photon sensitivity is maximized when the diode is operated in Geiger Mode as a SPAD.

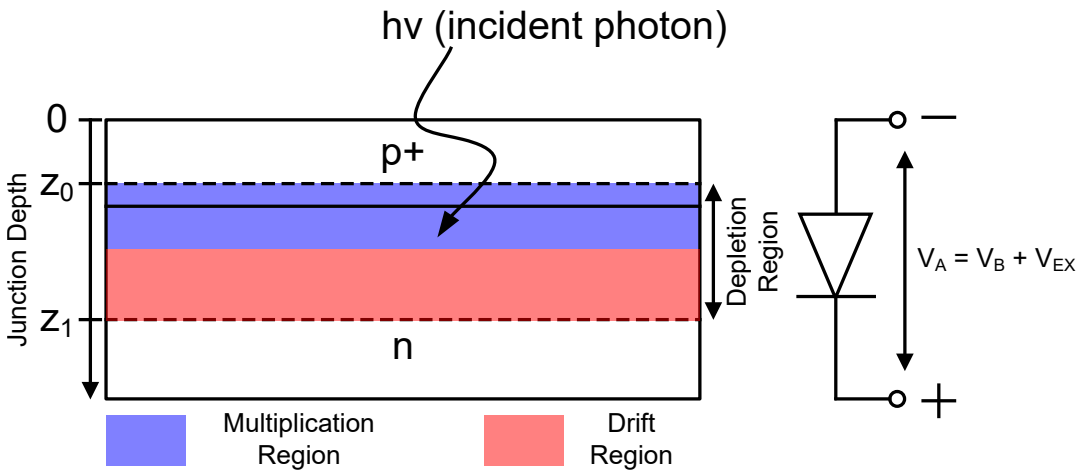


Figure 2.4: Cross-section of a planar p-n junction formed between $p+$ and n doped silicon. Photon absorption in the multiplication region triggers avalanche breakdown.

The depletion region (shown in Fig. 2.4) is divided into multiplication and drift regions. The multiplication region is defined as the depletion width which contributes to 95% of the integral in (2.1) [17], [18]. The remainder is defined as the drift region. Due to the difference in ionization rates of electrons and holes, for a given doping in silicon, $n+/p$ junctions have narrower multiplication regions compared to $p+/n$ junctions [18]. This influences the peak wavelength that can be detected by a SPAD.

When a p-n junction is biased at a voltage $V_{\mathrm{A}} = V_{\mathrm{B}} + V_{\mathrm{EX}}$, where V_{EX} is known as the excess voltage, the avalanche dynamics can be described as follows [19]: (i) an electron-hole pair is generated either by an absorbed photon or a thermal event; (ii) the number of electron-hole pairs rises exponentially around the primary carrier; (iii) the increase in current lowers the local electric field to the breakdown value due to the drop across the space-charge resistance; (v) the avalanche spreads to another part of the junction. This propagation can only occur in the multiplication region and

therefore, its sizing, relative to the drift region, is important. The mean propagation speed of the avalanche, v_p is given by

$$v_p = kI_f \tag{2.2}$$

where I_f is the final avalanche current and $k = 3\,\mu$m/(ns-mA); (vi) the avalanche spreads across the entire junction and reaches a steady state value in the milliampere range in nanoseconds or sub-nanosecond time. The high current, if uncontrolled, can heat up and destroy the device. This necessitates lowering V_A below V_B to make $I_f < 100\,\mu$A to ensure that the avalanche multiplication stops [6], [14]. This operation is known as quenching. In order to detect another photon, V_A needs to be brought back to above V_B and this operation is known as resetting or recharging. A large resistor (typically $\geq 100\,\mathrm{k}\Omega$) in series with the SPAD can be used as a simple quench and reset circuit as shown in Fig. 2.5. However, this scheme suffers from slow recharging, during which the SPAD can get triggered prior to a full reset, resulting

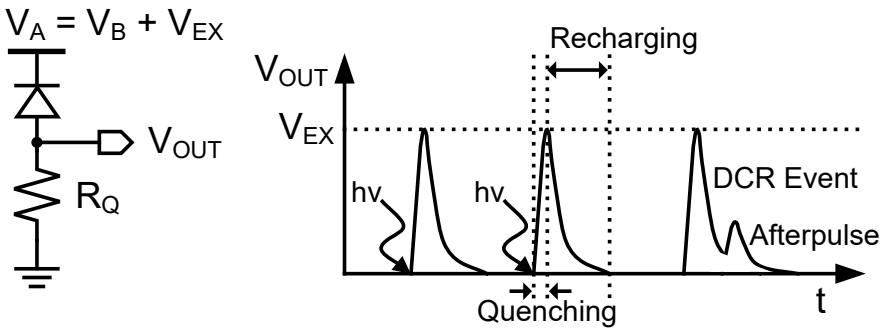


Figure 2.5: A resistor-based passive quench and reset scheme of a SPAD is shown in along with the transient behavior of the anode voltage during photon, DCR and afterpulse events.

in a lower amplitude pulse also known as an afterpulse, which is undesirable. For better timing control and performance, typically active circuits are used to speed up the quench and reset operation in CMOS SPAD pixels. These are explored in further detail in Chapter 3.

2.1.1.3 SPAD Parameters

Some of the most commonly used parameters for evaluating and comparing SPAD performance, as reported in the literature, are:

1. **Photon Detection Efficiency (PDE)**: This is defined as the ratio of the number of detected photons, i.e. the number of photons triggering avalanche events to the total number of photons incident on the active area of the SPAD [7]. As V_{EX} is increased, the electric field increases, which in turn increases the ionization rate and also the probability of the triggering of an avalanche [6]. Therefore, PDE increases as V_{EX} is increased. It is important to note that the nature and the depth of the junction plays an important role in determining which part of the electromagnetic (EM) spectrum is detected most strongly [17]. Therefore, PDE is reported as a function of the wavelength of incident photons.

2. **Dark Count Rate (DCR)**: An avalanche event triggered without the incidence of a photon on the active area contributes to the DCR of a SPAD. The DCR effectively sets the noise floor and therefore, lowering it is often one of the main objectives while designing SPADs. There are two types of contributors to DCR; uncorrelated and correlated to detected photons [7]. The uncorrelated sources are: (i) Trap-assisted

thermal generation, also known as Shockley-Read-Hall (SRH) generation; (ii) Trap-assisted tunneling; (iii) Poole-Frenkel emission and (iv) band-to-band tunneling [6], [7], [17]. Sources (i)-(iii) are strongly temperature dependent and (iv) is strongly dependent on electric field. Correlated sources include optical and electrical crosstalk between different pixels and afterpulsing in the same pixel.

3. **Area**: The active area of the junction that is sensitive to incoming photons impacts performance in several ways. Larger area obviously leads to a higher PDE, but at the cost of a higher DCR. Moreover, a larger area contributes to increased detector capacitance which degrades timing performance. In general, smaller area SPADs, typically with diameters of $\sim$10 μm are preferred, and arrays of such devices are used when large detection area is a requirement.

2.1.1.4 Design Considerations for CMOS SPADs

Standard sub-micron CMOS processes offer multiple implant layers and well structures, including $p+$, $n+$, p-well, n-well, deep-n-well, and p-substrate, any of which can be used to make planar SPAD junctions. Each pairwise p-n junction combination yields different performance characteristics for reverse-bias breakdown voltage, spectral response, DCR, and PDE.

While some SPAD implementations have leveraged high-voltage processes or specialized CMOS image processes to reduce dark count rate [20]–[23], many have used general purpose sub-micron CMOS processes [24]–[28]. Compared to conventional $p+$/n-well, an $n+$/p-well junction can be used to reduce parasitic capacitance [29]

and provide wider spectral response [30]. Junctions formed using lightly-doped layers, such as p-well/deep-n-well or $n+/p$-substrate, have also been demonstrated to reduce noise and improve quantum efficiency at longer wavelengths [22], [31], [32].

Aside from the selection of p-n junction layers, the choice of guard ring structure heavily influences SPAD performance as well [17]. The guard ring plays a key role in the prevention of PEB, and to a large extent it determines the total area of the SPAD detector, limiting overall fill-factor for a detector array [6]. Guard rings are frequently formed using p-well or n-well isolation for $p+/n$-well or $n+/p$-well high-field junctions, respectively. Placement of the guard ring around the junction plays a key role in SPAD performance, as does active area diameter [23]. A smaller active area has the benefits of improved timing resolution through faster impulse response, reduced DCR and after-pulsing, and minimal optical crosstalk, at the cost of lower sensitivity [17], [26].

In order to improve fill factor and density scaling, shallow-trench isolation (STI), standard in deep sub-micron CMOS processes, can be used as a guard ring [22]. The use of an STI guard ring may increase DCR and after-pulsing, attributable to increased trapped charges where the p-n junction edge abuts STI [26]. This increase in DCR due to STI can be mitigated using additional fabrication steps, such as hydrogen passivation or process stop masks to isolate the STI from the active area [29], [33]. Another approach uses the active mask to move the STI away from the $p+$ implant edge and uses a lightly doped p-well structure as a guard ring; these combined techniques enable a low DCR of 231 Hz [28].

Table 2.2: SPAD parameter variation with increasing independent variables (adapted from [17])

Dependent \ Independent	Junction Depth	Diode Area	Excess Voltage	Temperature
DCR		↑	↑	↑
Blue PDE	↓		↑	
Red PDE	↑		↑	
Jitter		↑	↓	↑

Clearly, there are several variables to consider when designing a CMOS SPAD device. These variables interact with each other and make the design process a non-trivial task. While TCAD simulations can provide some insight, empirical data is essential to characterize both existing and new designs. Thus, different planar CMOS SPAD structures were empirically characterized as part of this work and the results published in [34]. A few of these designs are highlighted in the next section. However, a few rules-of-thumb can still be useful to gain some intuition into the SPAD design/selection process and these are summarized in Table 2.2. An excellent detailed theoretical discussion of CMOS SPAD design can be found in [17].

2.1.2 Proposed CMOS SPADs

Several structural variants of varying sizes were implemented in a general purpose 0.18 μm CMOS process (TowerJazz CA18HD). Of these, a particular structure with a deep junction is further described in detail here. It is realized using the p-well and deep-n-well interface, as shown in Fig. 2.6, where a $p+$ contact provides the anode terminal of the device. In most CMOS processes, this structure will produce a lightly-doped active region, and subsequently the depletion region across the p-well/deep-n-

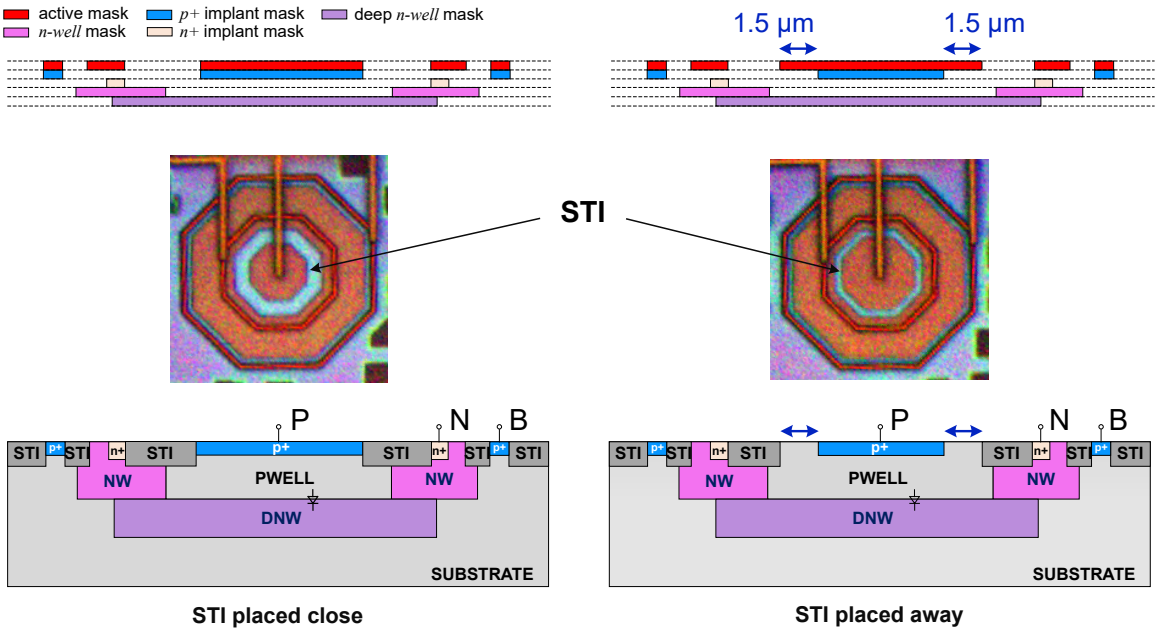


Figure 2.6: Cross-sections of variants of a p-well/deep-n-well SPAD implemented in TowerJazz CA18HD 0.18 μm CMOS process with variable distance between STI and active area to investigate impact on DCR [34].

well junction will be wider than in a $p+/n$-well structure [22]. The n-well acts as a guard ring and isolates the active junction from the p-type substrate. STI is located between the $p+$ and n-well for electrical isolation, using the active mask for defining STI boundaries, which may require a design rule waiver in some processes. Multiple size variants of this SPAD were implemented by varying the active junction diameter, including 10 μm, 20 μm, 50 μm, and 100 μm structures. A 10 μm variant of this device was also implemented in which the STI was placed at a distance of 1.5 μm further from the active $p+$ region to characterize the effect of STI proximity (Fig. 2.6). The final test IC die size measuring 2.4 mm $\times$ 2.4 mm, and an annotated die photo of the fabricated IC is shown in Fig. 2.7.

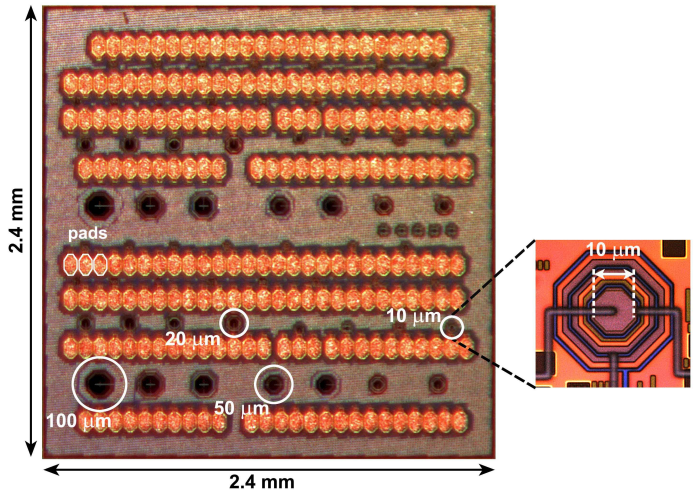


Figure 2.7: Test die with multiple planar SPAD variants, implemented in TowerJazz CA18HD 0.18 μm CMOS process [34].

The characteristics of the p-well/deep-n-well CMOS SPAD is summarized in Table 2.3. As expected, owing to the deeper and more lightly doped junction, the SPAD has a higher breakdown voltage of 16.4 V compared to that of variants with a shallower junction with higher dopant concentration (11.2 V for p+/n-well and 12.1 V for n+/p-sub). Additionally, because of the deeper junction, the PDE peaks at a lower wavelength of 400 nm compared to the usual ~500-550 nm for standard shallow junctions devices. Finally, the SPAD variant with the STI placed further from the junction edge has a significantly lower DCR for the same V_{EX}, thus validating the

Table 2.3: Proposed CMOS SPAD Performance Summary

Process	**Junction**	**Breakdown Voltage (V_B)**	**Active Area**	**DCR (V_{EX} = 0.5 V)**	**Peak PDE (V_{EX}, @λ)**
0.18 μm	pw/dnw	16.4 V	85 μm^2	STI Close: 32 kHz STI Far: 16 kHz	2.7 % (0.4 V, @400 nm)

impact of STI distance on DCR performance. For detailed characterization data of the implemented CMOS SPAD variants, the reader is referred to [34].

2.2 Resistive Transducer for Flow Sensing

2.2.1 Background

Volumetric flow rate and flow velocity of fluids is used in several automobile, environmental, and medical applications. Most flow sensors use thermal techniques and comprise a heater element which provides a known amount of heat, and a separate sensing element which is cooled at a rate depending on the fluid flow rate, thus providing flow related information. Modern low-power flow sensors are highly miniaturized chip-scale sensors (μm to mm scale) owing to techniques such as micro-electromechanical systems (MEMS) fabrication [35], and CMOS-compatible transducers such as metal heaters and silicon thermopiles [36], [37]. These techniques, however, almost always require dedicated custom fabrication processes or post-fabrication steps, increasing cost, complexity and difficulty of integration with other sensors.

2.2.2 Proposed Integrated Single-Element Flow Sensor

A novel single-element flow sensor is proposed and fabricated in a standard 0.18 μm CMOS process. Such a flow sensor that is integrated into a CMOS IC substrate, requires exposure of the heating and sensing elements at the top or bottom chip surface. The transducer used in the sensor is a single resistive element that is realized

in CMOS top metal layers and does not require any post-fabrication. This allows top-side interfacing of the flow sensor. Thus, sub-millimeter miniaturization is achieved, which combined with the top-side interface of the sensor enables integration with other CMOS-compatible optical sensors (such as the ones presented in Section 2.1) and micron-scale fluidic channels [38], for lab-on-chip and lab-on-CMOS applications. The choice of top-side interface limits the use of front-end-of-line (FEOL) CMOS layers, such as high-resistivity polysilicon, which could be otherwise used to realize small-area, large-value resistors to enhance sensitivity. Moreover, FEOL sensors would require flip-chip packaging for backside thermal interface, often using a thinned silicon substrate [39], [40].

For a top-side sensor interface, BEOL top metal layers can be used to implement the sensor element. The element must have low enough resistance to enable heating using CMOS-compatible voltage levels, and large enough resistance to measure useful changes in flow rate; this requires an element on the order of several hundred ohms for the proposed architecture. Implementation using exclusively CMOS top metal is area-inefficient, as this layer has low sheet resistance due to its primary intended use for power routing and I/O. In contrast, electrical vias in modern CMOS processes are typically micron-scale tungsten structures, which have significantly higher resistivity compared to metal routing layers, with 1-2 Ω per via for standard PDK via dimensions. A resistor structure that primarily comprises via resistance can achieve much higher resistance per area than using only planar metal layers.

The resistive transducer used in this work employs a vertically serpentine structure that alternates between the top metal layer and the next lower metal layer through

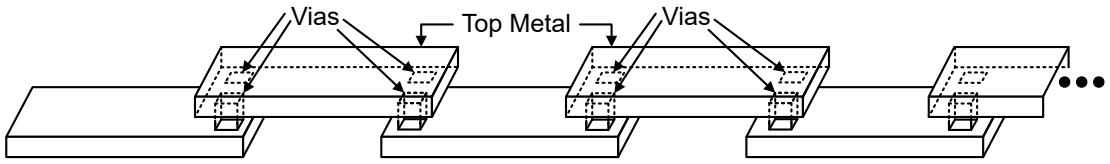


Figure 2.8: 3-D illustration of the structure of the on-chip resistive sensing element formed in the top CMOS routing layers, where each layer change consists of two electrical vias in parallel; this ensures support of sufficiently high current densities, while still maintaining a high resistance density [42].

electrical vias, as shown in Fig. 2.8, which is then arranged in a planar serpentine layout. Using this approach, a resistance of approximately $500\,\Omega$ is achieved within a sub-millimeter footprint, as shown in the chip photograph and the annotated CAD layout in Fig. 2.9. Almost all of the resistance can be attributed to the via resistance, which was validated by simulation using extracted parasitic resistances. Compared to the standalone discrete metallic element in [41], for the same resistance value, this CMOS-integrated approach reduces area by a factor of approximately 250. The entire flow sensor (resistor, and control and measurement circuits) occupies an active area of $0.065\,\mathrm{mm}^2$.

The resistor was heated using an off-chip current source, while integrated circuits employing thermal Σ-Δ techniques (highlighted in Fig. 2.9(b)) were used for heating control and sensor measurement. A $20.5\,\Omega$ change was observed over a range of $19\,^\circ\mathrm{C}$ to $64\,^\circ\mathrm{C}$ for a measured sensitivity of $0.45\,\Omega/^\circ\mathrm{C}$. Experimental results in a air flow chamber demonstrated the feasibility of the fully integrated CMOS anemometer for air flow rate measurements. Detailed explanation of the system and flow measurements is outside the scope of this chapter and the reader is referred to [42] for further details.

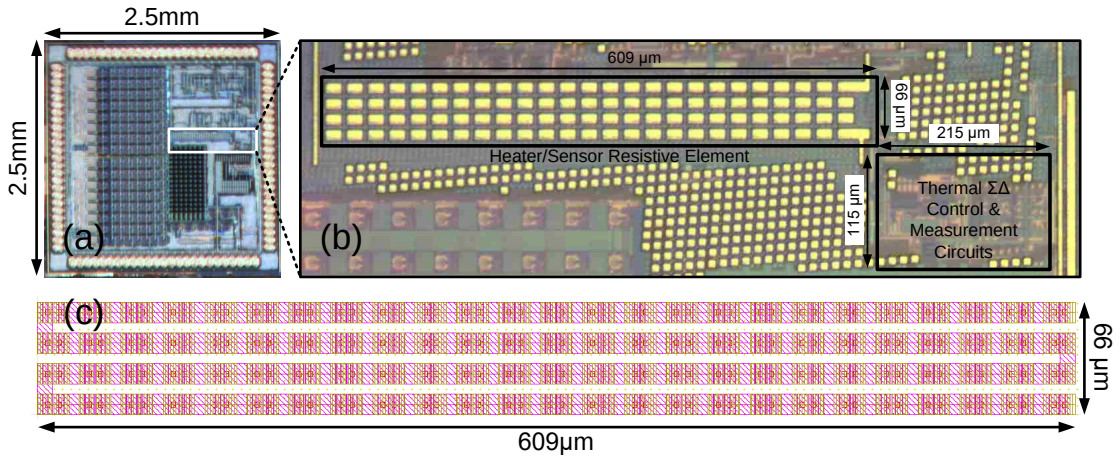


Figure 2.9: (a) Chip photo with integrated flow sensor highlighted, (b) zoomed view of flow sensor blocks, and (c) computer layout of heator/sensor resistive element.

2.3 Conclusion

The benefits of integrating transducers in CMOS substrates were highlighted in this chapter. Several SPAD variants and a novel top-metal resistor were implemented in general purpose CMOS processes, without any die-level post-processing. The SPADs were characterized standalone and various design trade-offs were explored and validated using measured data. An example of the system-level integration of CMOS SPADs is further explored in Chapter 3. The top-metal resistor was used as a transducer in a compact single-element integrated CMOS air flow sensor and chip measurements were used to validate the proposed idea.

Chapter 3: Front-End Interface Circuits

The output of a transducer is typically a weak analog (continuous-time and continuous-amplitude) signal in the form of charge, current or a voltage. It requires signal conditioning such as amplification, modulation, and filtering, before being read out as an analog value or being digitized by an analog-to-digital converter (ADC). These tasks are done by analog circuits such as amplifiers and filters. These circuits or others might also be responsible for providing appropriate bias conditions for the transducer, and also transform the input signal to a different form (eg: current-to-voltage or vice-versa). Collectively, the set of analog circuits that interface with the transducer are known as the analog front-end (AFE).

This chapter introduces a few popular AFE architectures followed by a brief overview of readout circuits for single-photon avalanche diodes (SPADs). A SPAD-based digital ambient light sensor is used as a case study to understand how transducers can impact the AFE and system design significantly. Additionally, a programmable AFE is also introduced for the readout of silicon photomultiplier (SiPM) arrays. This is covered in Chapter 5 since it forms part of a larger gamma spectroscopy system.

3.1 Readout Circuit Architectures

Two popular AFE circuit architectures are shown in Fig. 3.1(a-b). Current sensing is a popular technique used widely in biosensors for measuring very small currents ranging from few fA to several uA [43]. The most common readout scheme employed for this the classic continuous-time transimpedance amplifier, employing a feedback resistor (R_{F}) with an operational amplifier (op amp), as shown in Fig. 3.1(a). The output voltage can then be digitized by a conventional voltage-domain ADC. Discrete-time implementations replace the R_{F} with a parallel combination of a capacitor and a reset switch [43]. On the other hand, for a voltage reading such as the output of a wheatstone bridge measuring temperature, strain, etc., a popular technique is to use an instrumentation amplifier as shown in Fig. 3.1(b). The small input voltage is multiplied by by a gain factor prior to digitization by an ADC [44]. More recently, highly compact and digital implementations for both types of AFEs (highlighted in

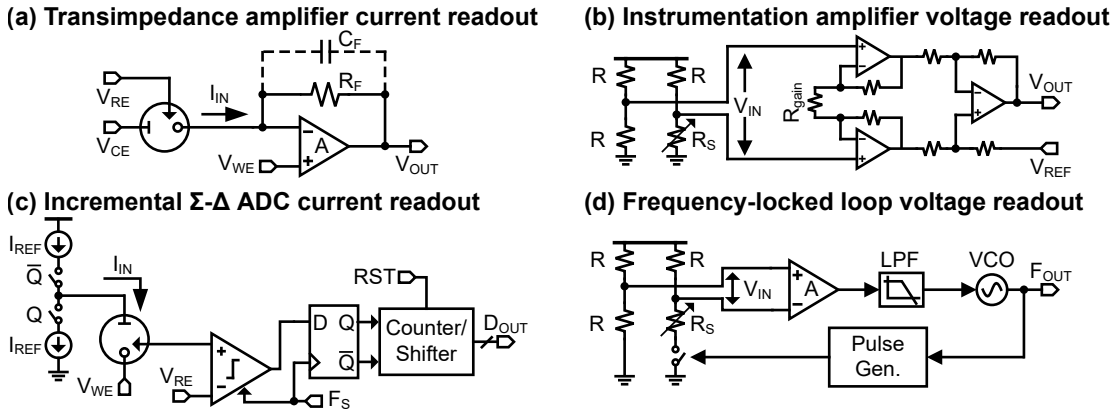


Figure 3.1: Common AFE architectures are shown in (a) and (b). Sensor-in-the-loop architectures with combined AFE and ADC functionalities are shown in (c) and (d).

Fig. 3.1(c-d)) have become popular in the literature where the AFE and ADC functionalities are combined in the front-end block, often also including the transducer in the loop [45], [46]. This results in early digitization resulting in programmable resolution and dynamic range performance with compact areas for easier system-on-chip (SoC) integration. These new architectures are also attractive from the perspective of CMOS technology node scaling, which inherently favors digital circuit performance.

Clearly, for highly integrated sensor SoCs, compact architectures that combine AFE and ADC functionalities are quite attractive. However, this trend is still reliant on an inherently analog input signal that is small and can be sensitive to issues such as switching-induced noise, jitter or mismatch in the readout circuits [45], [46]. As noted in Chapter 2, the output of a SPAD is a digital-like pulse when triggered by a photon. Over time, the output is a train of pulses with the average pulse rate corresponding to the incident photon flux. This output can be easily processed with digital counters and filters. Thus, the task of signal digitization is internal to the transducer, opening the door for use as highly digital sensors that are ideal for SoC integration. For proper SPAD operation, appropriate readout circuits are required and are introduced in the next section.

3.2 Readout Circuits for SPADs

As was noted in Chapter 2, a SPAD requires quenching and recharging, often done by a large series resistor $R_{\mathrm{Q}} > 100\,\mathrm{k}\Omega$. However, this limits the dead time, T_{DEAD}, during which no new photons can be detected. It also leads to noise in the form of increased

afterpulsing probability due to a slow recharge (up to several μs). To achieve faster quenching and recharging, active circuits are employed. These are often collectively labeled as active quench and reset circuits (AQRCs) or simply quench and reset circuits (QRCs). A purely active quench and active reset circuit is rarely used [14]. Most often, either a passive quench-active recharge scheme or a mixed active-passive quench and active recharge scheme is used as shown in Fig. 3.2. The SPAD anode is connected to a large impedance (large resistor or MOSFET in triode) for passive quenching, and also to the active quench and reset switches. This takes advantage of the inherently short quench time and focuses on minimizing the recharge (or reset) time, T_{RESET}. It is also beneficial in terms of area and fill-factor, when compared to purely active QRCs. When the SPAD is triggered, a large current flows through it and the large series impedance, bringing the anode voltage up. This operation is similar to passive quenching. After time T_{DELAY}, the voltage crosses V_{TH} and triggers the active quenching through S_{Q}. This accelerates SPAD quenching, bringing the bias voltage below breakdown. After a defined duration, T_{HOLD} during which the SPAD is held in quenched state, the SPAD is actively reset to its original pre-trigger bias condition through S_{R}. To ensure proper recharging, the SPAD is held in this state for

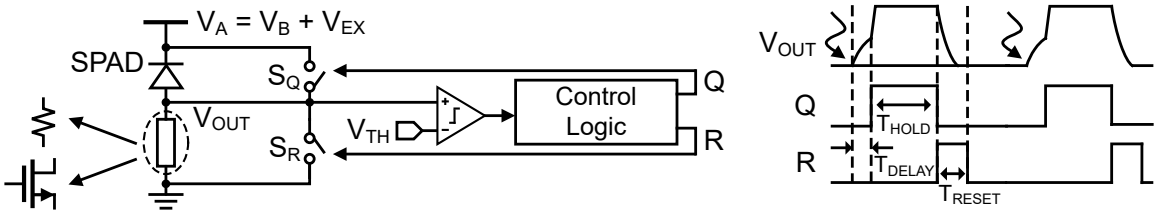


Figure 3.2: Mixed quench and reset scheme used with SPADs and associated timing diagram [14].

a sufficiently long time, T_{RESET}. T_{HOLD} and T_{RESET} are well determined parameters which the QRC is designed to control. For mixed QRCs, the dead time is therefore defined as $T_{\text{DEAD}} = T_{\text{DELAY}} + T_{\text{HOLD}} + T_{\text{RESET}}$ [47]. T_{HOLD} should be optimized to be long enough to minimize afterpulsing but not too long that the maximum count rate gets compromised [14]. For values in 100s of ns, $T_{\text{DEAD}} \approx T_{\text{HOLD}}$ is a reasonable approximation, since this dominates over the other two terms. With appropriate sizing and supply voltage, the comparator in Fig. 3.2 can be replaced with a simple inverter. Such a QRC is introduced as part of the following case study.

3.3 Case Study: Digital Ambient Light Sensor

3.3.1 Introduction

Ambient light sensors are used in a wide range of applications including display backlight control in portable devices, building interior lighting, proximity sensors, smart street lights, and automotive lighting control (Fig. 3.3). With the increasing adoption of automation in industrial and commercial applications, such sensors have become a critical component in control loops for automated systems to conserve power and perform their required tasks. Cost, ease of implementation, and power consumption drive the selection of such sensors.

A typical CMOS-integrated ambient light sensor uses one or more photodiodes for converting light intensity to a proportional current value. This photocurrent is then read out and digitized by one of the many available readout circuits. Some of

the commongly used techniques are highlighted in Fig. 3.4. One of the most popular techniques involves amplifying and converting the photocurrent, usually in the pA-nA range for reasonably sized photodiodes, to a suitable voltage using a continuous-time transimpedance amplifier (TIA). This voltage is then digitized by an analog-to-digital converter (ADC). Dual-slope ADC-based architectures, such as the one reported in, can provide excellent resolution at the cost of reduced bandwidth, which is an acceptable trade-off for ambient light measurements. Schemes with mostly digital circuits have also been demonstrated, such as a comparator-based light-to-frequency converter in [48] and a VCO-based readout in [49]. In all of these implementations, the intrinsically analog nature of the photodiode output puts stringent requirements on the interfacing analog or mixed-signal blocks with stability, noise, resolution, and matching being critical. Additionally, for sufficient signal-to-noise levels and dynamic range, the photodiodes have to be large enough, often $\geq 10^4\,\mu\text{m}^2$, to generate a large

Figure 3.3: Common applications for ambient light sensors

enough photocurrent. All of the aforementioned factors end up resulting in systems with large silicon area, design complexity, high power, and high cost. Optical filters are also often used leading to additional post-processing and packaging complexity.

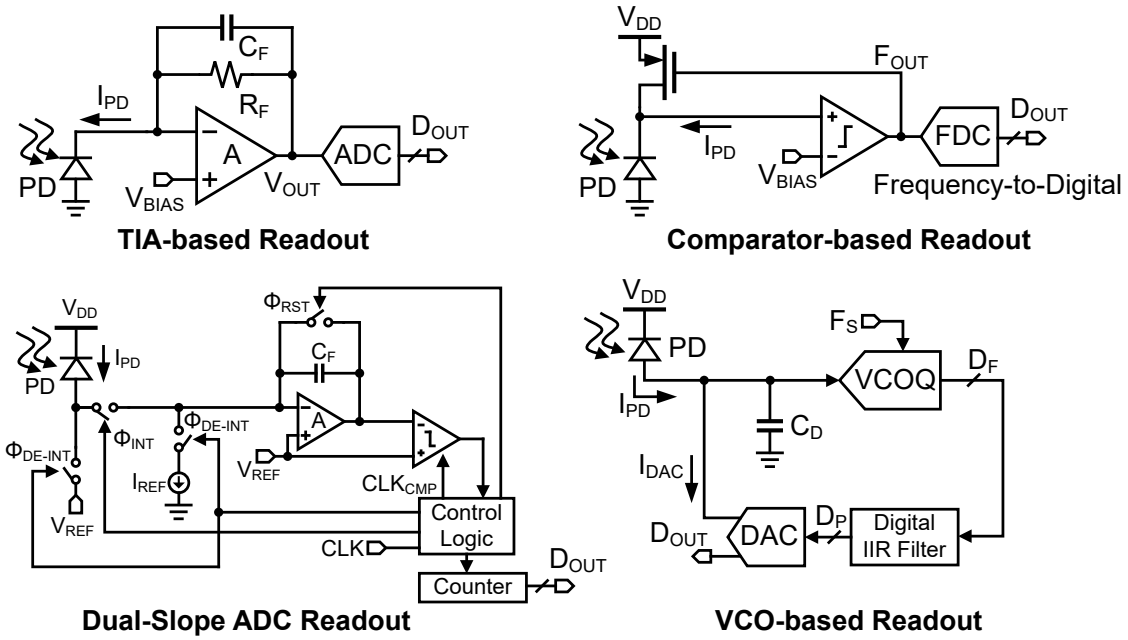


Figure 3.4: Example photodiode readout circuits

In this work, we present the design and measured performance of an all-digital ambient light sensor implemented in a standard CMOS process, which leverages the pulse-based, digital-like behavior of single-photon avalanche photodiodes. Combined with digital front-end and processing circuits, this approach achieves a significant reduction in circuit area and required photodiode area.

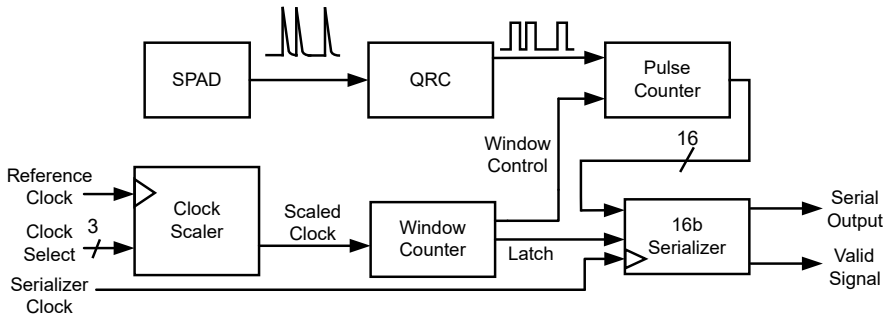


Figure 3.5: A high-level architecture schematic of the proposed all-digital ambient light sensor [50].

3.3.2 Proposed System

The high-level architecture of the all-digital CMOS ambient light sensor based on a single-photon avalanche diode (SPAD) is shown in Fig. 3.5. In contrast with a typical reversed-biased photodiode detector, which produces a steady current, a SPAD device outputs a train of current pulses proportional to incident light intensity, which can be used to charge the gate of an inverter to produce squared digital pulses. Used this way, a SPAD is a light-to-frequency converter with a digital output.

By exploiting the "digital-like" operation of an individual SPAD device, which eliminates the need for a TIA and general purpose ADC, design effort and circuit area for the sensor readout can be greatly reduced. The inherent signal amplitude noise immunity of the pulse-based SPAD output allows large-area, static power-intensive analog blocks to be replaced by simple dynamic CMOS digital circuits such as counters, registers, and control logic. In addition to the inherent decrease in area and power consumption, the ability to synthesize processing circuits using standard cells further decreases design complexity.

The following sub-sections briefly describe SPAD operation and its use as an ambient light sensor.

3.3.2.1 SPAD Operating Principle

A SPAD device is structurally similar to a standard photodiode. Both comprise a *p*-*n* junction diode with a reverse breakdown voltage, V_B. However, for the diode to function in Geiger mode as a SPAD, the applied reverse bias, V_A, must be greater than V_B. Under this condition, upon excitation by a photon, junction breakdown results in a runaway avalanche multiplication, which continues until a high current value is reached, limited only by V_A and the internal resistance of the diode. By employing passive or active quench and reset circuits (QRC), the bias across the diode can be brought quickly below V_B to protect from over-current, and the diode can be reset to detect another photon [51]. A stream of current pulses are produced, where pulse height carries no information; pulse current is the same whether one photon or multiple concurrent photons are absorbed. Since light intensity corresponds to the rate of photon arrival, the pulse rate is instead used to determine light intensity. An avalanche event can also be triggered by a thermal event, which contributes to the noise floor of the SPAD, or dark count rate (DCR).

Compared to standard photodiode detectors, SPAD structures must include a guard ring around the *p*-*n* junction to limit premature edge breakdown. In deep sub-micron CMOS processes, this can be implemented using shallow trench isolation and well structures [28], [51]. The layout and the cross-section of the SPAD structure

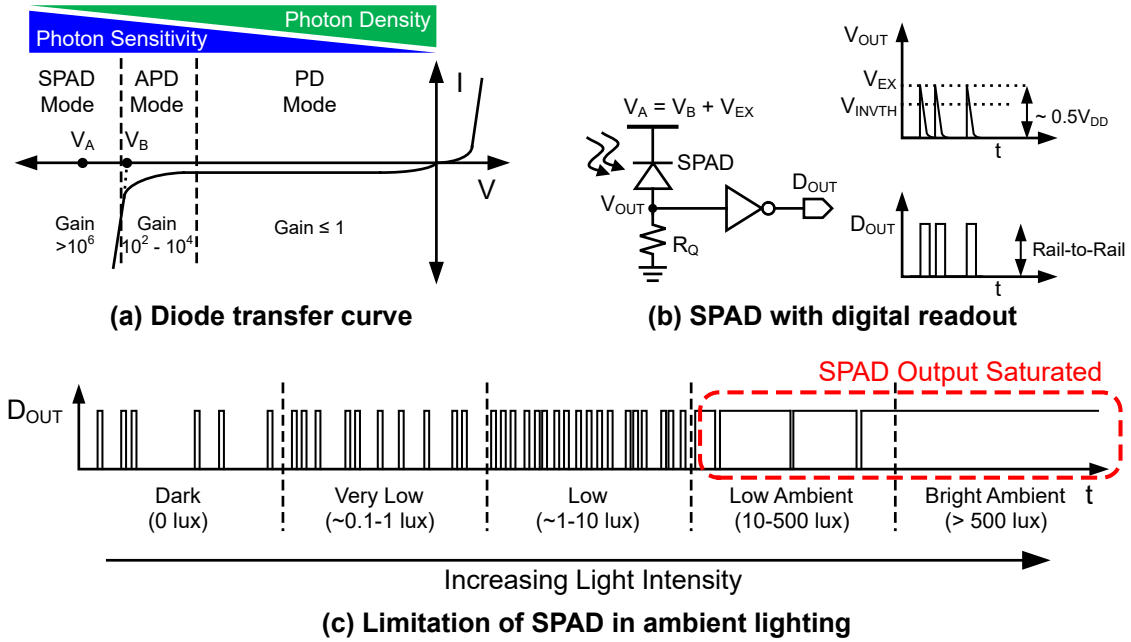


Figure 3.6: SPAD characteristics with a digital readout and operation across varying light intensity.

used in this work are shown in Fig. 3.7, which was implemented in a 0.13 μm CMOS process.

3.3.2.2 Using SPAD for Ambient Light Sensing

As the name suggests, SPADs can be triggered by single photons and are extremely sensitive devices. They are typically used in applications such as fluorescence lifetime imaging or time-of-flight and radiation detection, where extremely low visible light intensities are of interest ($<$ 0.1 lux). Due to the high sensitivity and inherent DCR, SPADs are easily saturated in light conditions greater than a few 10s of lux as shown in Fig. 3.6(c). For use in ambient light, V_A may be decreased to reduce the photon

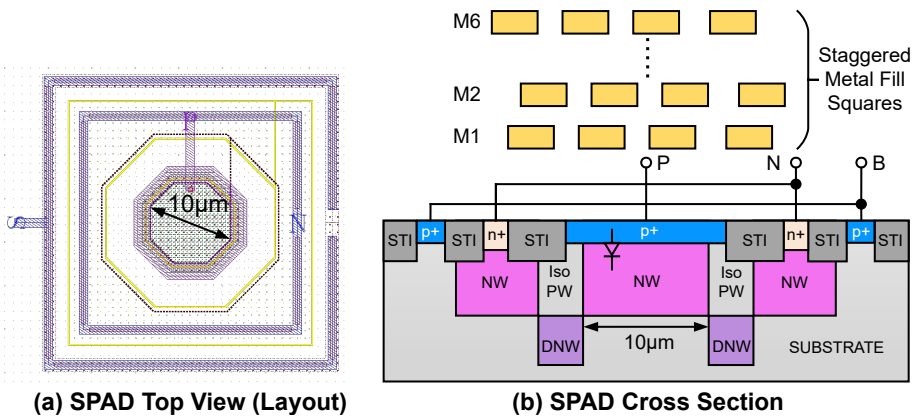


Figure 3.7: (a) Top view of SPAD layout in 0.13 μm CMOS process and (b) illustrated cross-section of the SPAD showing metal fill-based filter. [50].

detection efficiency, reducing the sensitivity of the SPAD. However, reducing V_A also reduces the final current value of a SPAD event, resulting in an output voltage pulse that is near to or less than the inverter threshold, resulting in unreliable or failed detection. In this case, detection requires a low-threshold comparator in place of an inverter, obviating the advantages of a digital-like output.

An alternative approach is to reduce the number of photons incident on the active area of the SPAD by physically blocking or filtering the incident light. Ambient light sensors often use optical filters on top of the photodiodes, which requires additional post-processing of the sensor.

In the presented work, we leverage available metal layers in a standard CMOS processes to filter incident light. Metal fill shapes, typically used to assure planarity for compatibility with chemical mechanical polishing during CMOS fabrication, typically comprise small (few μm), staggered floating metal squares. Placed over the diode active area through multiple layers, these can act as a broad-band optical filter.

This approach removes the need for CMOS post-fabrication, and it enables SPAD operation in ambient light without saturating the device.

3.3.3 System Overview

The complete signal chain of the proposed system is illustrated in Fig. 3.5, and it can be broken down into the following component parts:

3.3.3.1 SPAD and Quench and Reset Circuit

QRCs are broadly classified into passive, active, and mixed-mode types, and in most SPAD-based applications a mixed quench and reset scheme is preferred [14]. Fig. 3.8 shows the interface between the SPAD and a mixed-mode QRC in the implemented system. Prior to avalanche breakdown, node Y is high and Z is low, as set by the previous reset operation. Upon breakdown, a large current flows through the SPAD and R_Q. The voltage at X increases (passive quenching) until it crosses the threshold of INV1, flipping Y to low and starting the active quench operation. When M3 is turned on, X is forced to V_{DD} by M2 and M3. Because of the positive feedback, Y is forced low, turning M1 off. The double delay block acts as a delayed inverter with different rise and fall transition delays, determining the hold-off and reset times. The double delay block turns Z high after a fixed delay, or hold-off time, during which the bias voltage across the diode remains below V_B and Y stays low [52]. When Z goes high, M4 turns on and discharges X, and making Y high and pulling Z low after a

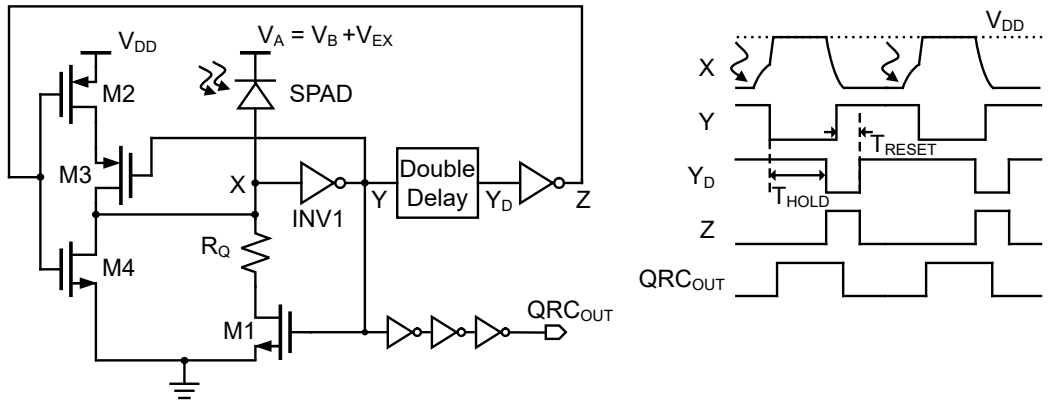


Figure 3.8: Schematic illustration of mixed passive-active quench and reset circuit, including self-timed hold-off and reset signals [50].

fixed reset duration. A single square output pulse is generated during a quench and reset cycle, corresponding to a single avalanche event.

3.3.3.2 Digital Logic

The digital blocks used in the ambient light sensor are illustrated in Fig. 3.5. Squared pulses from the QRC are counted asynchronously by a windowed 16-bit pulse counter. The window-control signal resets the pulse counter, while the latch signal latches the pulse counter output into a 16-bit serializer. The window counter is a 16-bit counter, which counts pulses from the clock scaler. When the window counter overflows, window-control and latch signals transition high, ending the sampling operation. The clock scaler provides down-scaled versions of the reference clock to set the sampling window in which the QRC pulses are counted. This approach allows the adjustment of window time to be large for error reduction or small for increased range of operation at

higher lux levels or high sample rate, without overflowing the fixed-size pulse counter.

3.3.4 Implementation and Measured Results

The ambient light sensor was designed and fabricated in a standard 0.13 μm CMOS process (GF/IBM 8RF). A die photograph of the chip, along with annotated outlines of the blocks used for the sensor, are shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. The single SPAD device used in the sensor has an active area of 72 μm^2. The total area of the SPAD, QRC, and digital circuit blocks was 0.046 mm^2. Control and data acquisition were implemented using an FPGA module (Opal Kelly) interfaced with the IC on a custom printed circuit board. A custom MATLAB GUI was used for

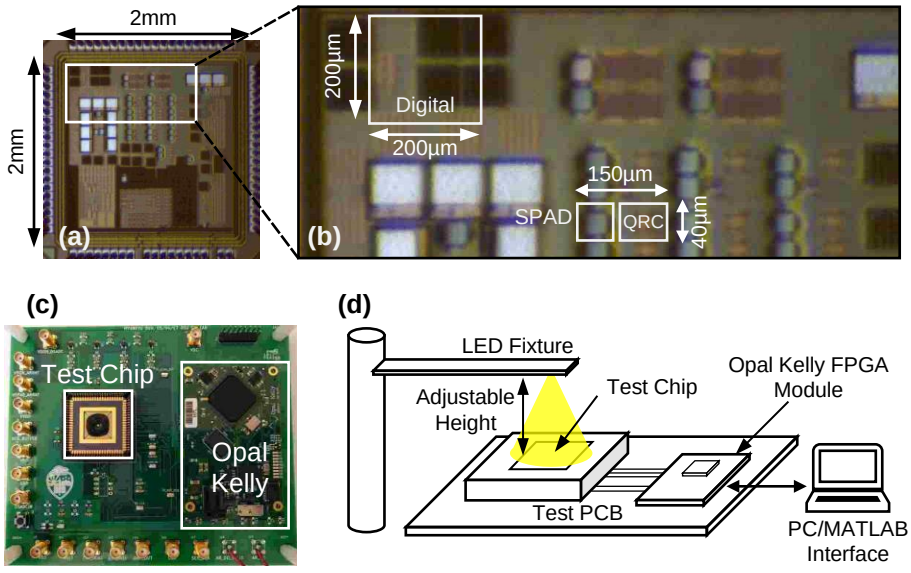


Figure 3.9: (a) Chip photograph of the test chip fabricated in GF/IBM 0.13 μm CMOS process, (b) zoomed view of the ambient light sensor blocks, (c) test PCB photograph, and (d) illustration of the test setup.

system control and data acquisition.

From initial characterization data, the breakdown voltage of the SPAD was measured as 10.0 V. On-chip circuits were powered by a single supply voltage, $V_{\mathrm{DD}} = 1\,\mathrm{V}$. This supply voltage was selected to lower the threshold of INV1 (Fig. 3.8) so that pulses could be sensed even for low values of excess voltage, V_{EX}. An excess bias, $V_{\mathrm{EX}} = 0.47\,\mathrm{V}$, was applied to the SPAD from a separate power supply. DCR was measured to be approximately 160 kHz. The applied V_{EX} was sufficient to generate pulse amplitudes higher than the threshold of INV1. A hold-off time of 100 ns was used for testing, resulting in a maximum SPAD pulse rate of 10 MHz. A system clock of 6.3 MHz was fed to the clock scaler and the serializer (Fig. 3.5). For light intensity measurements, all ambient lights were switched off and a white light emitting diode (LED) was used in a fixture, set at a variable height from the chip surface, as shown in Fig. 3.9(d). Light intensities from 100 to 25,000 lux were generated using this setup. A commercial lux meter (OPT3001EVM) was used to measure the lux levels.

Experimental results for varying light intensity are shown in Fig. 3.10. Each measurement consisted of a DCR measurement averaged over 200 consecutive samples in darkness, immediately followed by a light intensity pulse rate measurement averaged over 200 consecutive samples under illumination. An integration time window of 10.4 ms was used for each sample. '$\Delta Pulse\,Rate$' defines the difference between these two averaged values. Thus, baseline DCR was subtracted from each measurement, which corrected for DCR variation in real time and provided calibration for zero output in darkness. Maximum total power consumption (circuits and SPAD) was measured to be slightly less than 125 μW. Sensor performance is summarized in

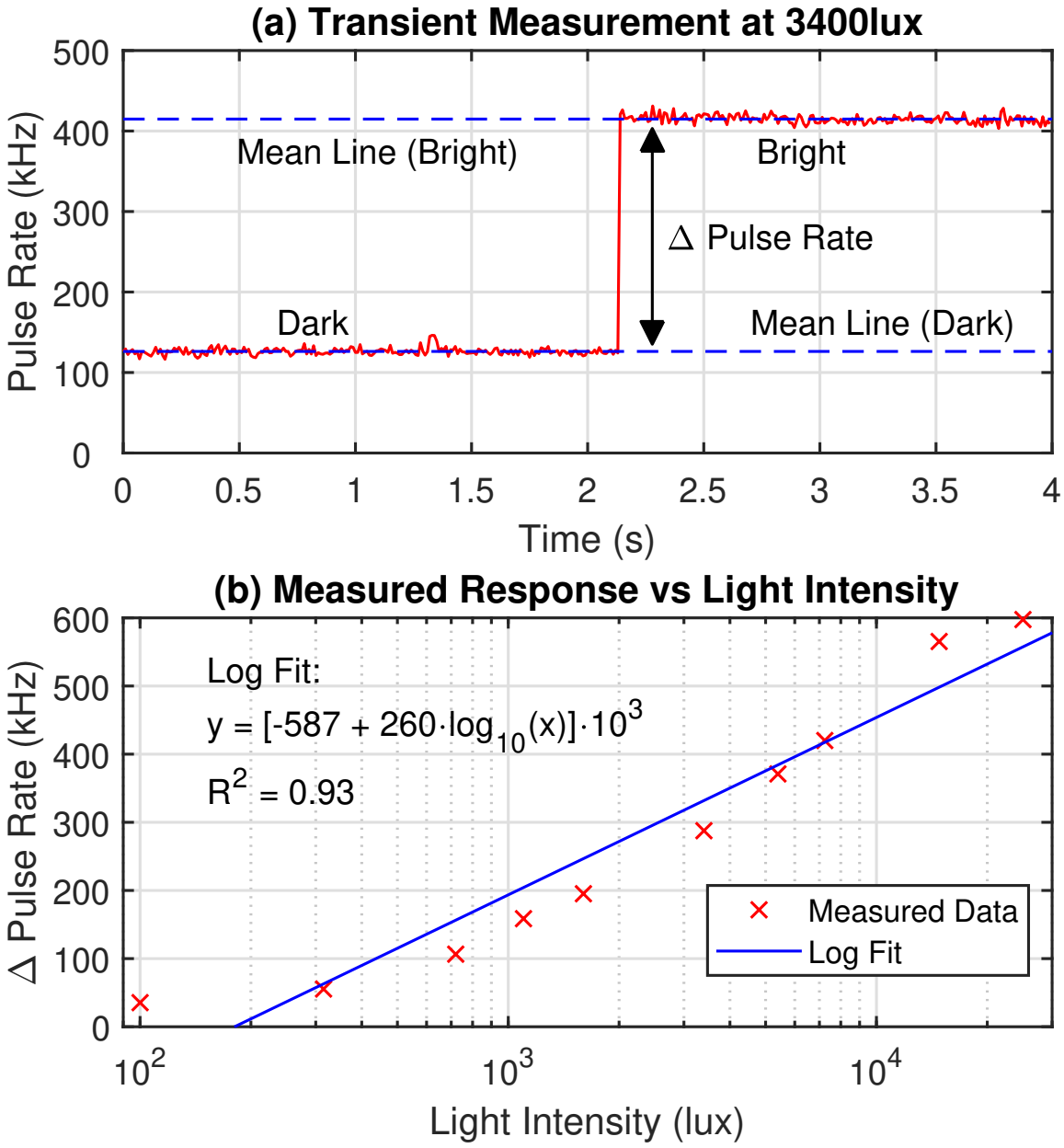


Figure 3.10: (a) Transient measurements showing transition between dark and bright (at 3400lux) pulse rates. (b) Measured response across varying light intensity, with logarithmic fitting curve.

Table 3.1: Comparison of proposed ambient light sensor with prior art

Reference	[48]	[53]	[54]	**This Work [50]**
CMOS Process (μm)	0.35	0.35	N.A.	**0.13**
Supply Voltage (V)	3.3	N.A	1.8-3.3	**Circuits: 1, SPAD: 10.5**
Ambient Light Range (lux)	0.15-37.3k	10-16k	0.3-10k	**100-25k**
Power	11.25 mW	150-245 μW[a]	30 μW[b]	**125 μW**
Diode Area (mm^2)	0.0144	0.0144	N.A.	**7.2×10^{-5}**
Total Area (mm^2)	1.28	0.3	4.2[c]	**0.046**

[a.] Calculated Power, [b.] Calculated power at 1 klux, [c.] Commercial package

Table 3.1, alongside specifications of related, published ambient light sensors.

3.3.5 Conclusion and Future Work

The presented ambient light sensor demonstrates measured, all-digital quantification from 100-25000 lux with less than 125 μW of active power. The output behavior (Fig. 3.10(b)) is comparable with published ambient light sensors but uses much less circuit area. In addition, the photodiode area in the present work is significantly smaller than typical, where multiple large-area photodiodes are often used. While SPAD-based sensors require high bias voltage, integrated solutions for on-chip high voltage generation such as [6] have been reported. In addition, future work could include on-chip temperature compensation of DCR drift, and on-chip linearization.

Chapter 4: Information Aware Analog-to-Digital Converters

An Analog-to-Digital Converter (ADC) translates analog signals (continuous-time, continuous-amplitude) to a digital signal (discrete-time, discrete amplitude) by sampling and quantizing the analog input signal. Since it straddles both the analog and digital domains, it is said to operate in the "mixed-signal" domain. Most ADCs operate on an analog input voltage, although charge and current input ADCs also exist. The ADC output is a N bit digital word, where N nominally determines the maximum achievable resolution (Full-Scale/2^N) of the ADC. This allows the digital representation of the input to be stored or processed by a digital computer. The quantization process inherently introduces noise known as quantization noise. Real-world limitations resulting from matching and circuit noise introduce non-idealities which show up as additional noise and lead to degradation of the resolution and the signal-to-noise Ratio (SNR) of the ADC. Thus a N bit ADC will have performance corresponding to a N' bit ideal ADC where $N' < N$. N' is referred to as effective-number-of-bits

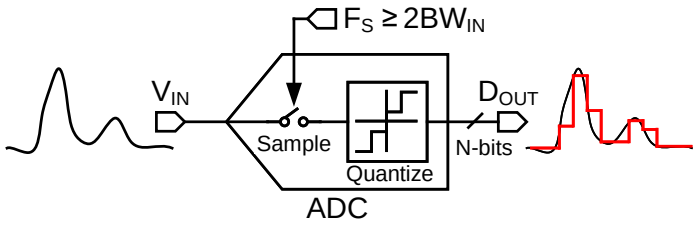


Figure 4.1: Simplified illustration of Nyquist ADC operation

(ENOB). Oversampling and noise-shaping techniques can be used to overcome some of these limitations as done in Σ-Δ ADCs. For ADCs following the Nyquist-Shannon sampling theorem, assuming a full-scale sine input, SNR(dB) = $6.02N$+1.76dB, while the actual maximum ENOB, N', is obtained by substituting SNR for the measured signal-to-noise-and-distortion ratio (SNDR or SINAD) in dB. Thus,

$$ENOB(N') = \frac{SNDR_{measured} - 1.76dB}{6.02} \tag{4.1}$$

It is important to note that the above relation assumes uniform distribution of quantization noise between -1/2 LSB and +1/2 LSB (where LSB refers to least significant bit), and an input signal distribution corresponding to a sine wave (hence the 1.76dB term). For many real-world signals that are non-sine inputs, this model does not always hold true. For a more detailed description of ADC operation and metrics, the reader is referred to [55].

4.1 Non-Linear ADCs

High linearity across the entire input amplitude full-scale range (FSR) is a typical design goal for an ADC. This assumes that for general purpose applications, information is uniformly distributed across the FSR, and all input values need to be converted with the same resolution. However, there exist a variety of applications where useful information is concentrated in specific sub-regions of the input FSR. In these scenarios, a non-linear ADC (NL-ADC) can be highly beneficial at the system-level,

providing reduced bit-rate, lower conversion time and energy, and increased dynamic range. For example, the use of logarithmic and exponential ADCs have been demonstrated in biomedical applications for bioelectrical signal recording [56]–[58]; other applications benefiting from the use of non-linear ADCs include telecommunications (μ-, and A-law), nuclear science, robotics, non-linearity correction in sensors and front-end amplifiers, and more recently, in machine learning [59]–[61].

4.2 Proposed Piecewise-Linear ADC

Most NL-ADCs have a fixed, non-linear transfer function, thus limiting their utility to specific applications. Programmability of a desired non-linear characteristic can redistribute the available quantization levels to have lower quantization error, emphasizing selectable regions of interest with higher information content. This can extend the use of such ADCs to a much wider range of applications.

Prior programmable NL-ADCs have been implemented using ramp or flash architectures [56], [59], which are generally inefficient in terms of power and area. Comparatively, successive approximation register (SAR) ADCs are ideal for moderate resolution and moderate sample rate applications due to their highly digital nature, power efficiency, and scalability. Both fixed [58] and programmable [60], [61] non-linear transfer curves have been demonstrated using SAR architectures, providing logarithmic, exponential, or quadratic conversion for targeted applications. Similarly, both linear and non-linear transfer characteristics can be implemented using a reconfigurable, binary-weighted capacitive digital-to-analog converter (CDAC) SAR ADC

[60]. However, non-linear transfer functions are limited to variations of $tanh$ and $tanh^{-1}$ functions using this approach due to the use of a binary-weighted DAC. In general, multiple high-resolution regions at arbitrary locations within the FSR cannot be defined using such approaches, severely limiting possible transfer functions.

In this work, a single-ended piecewise-linear ADC (PWL-ADC) is presented, which uses a two-step SAR architecture to realize arbitrarily programmable piecewise-linear (PWL) transfer functions with multiple, movable high-resolution regions. The core two-step architecture was first presented with a fixed exponential transfer function in [58], and simulated results from a programmable version were presented in [62]. This paper builds upon [58] and [62], providing a new approach for implementing the programmable non-linearity by controlling unit capacitor switching in the first stage. The primary benefits of this approach are: achieving higher resolution in user-specified regions allows using smaller word-length data to reduce data transmission volume, bandwidth, and storage resources in the system back-end; by employing non-linear transformations, regions of the signal can be emphasized and de-emphasized to aid feature extraction; and, allowing multiple, movable high-resolution regions in the FSR expands the scope of applications of NL-ADCs beyond conventional exponential and logarithmic converters.

4.2.1 PWL-ADC Architecture

Fig. 4.2(a) illustrates the high-level PWL-ADC architecture, which uses a synchronous SAR ADC approach. The conversion cycle is divided into two stages: a programmable

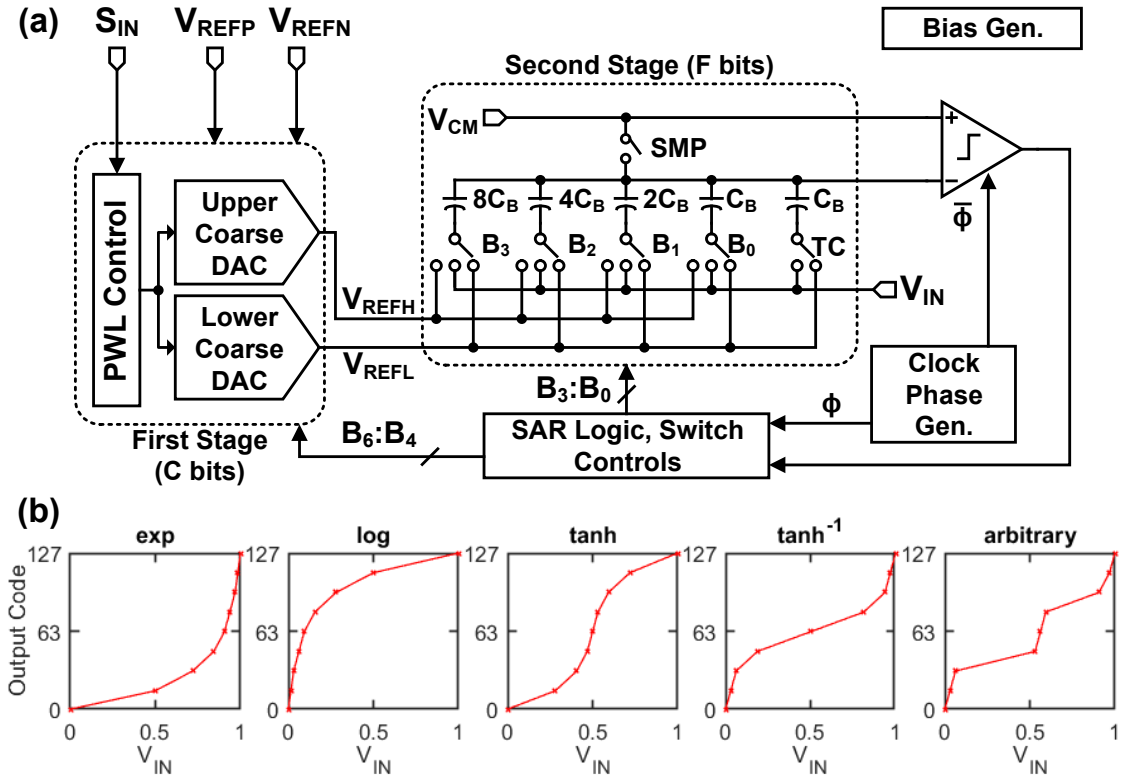


Figure 4.2: (a) High-level architecture of the proposed PWL-ADC. (b) Example nonlinear transfer functions from a behavioral model [63].

coarse-conversion stage and a fixed fine-conversion stage. For the programmable C-bit coarse-conversion stage, the full-scale range (FSR) (V_{REFP}-V_{REFN}) is divided into 2^C coarse segments of variable widths by generating 2^C+1 breakpoints; these can be spaced equally or unequally. This is implemented using two copies of a programmable, thermometer-encoded CDAC that provide a set of consecutive breakpoints, V_{REFH} and V_{REFL}, as output to the second ADC stage.

For the F-bit fine-conversion stage, each coarse segment is linearly interpolated using 2^F evenly spaced quantization levels between consecutive V_{REFH} and V_{REFL} break-

points, provided by the first stage at the end of coarse conversion. Fine conversion is implemented using a convetional binary-weighted CDAC, as shown in Fig. 4.2(a). At the end of a conversion, a B-bit digital word of variable resolution is obtained, where $B = C + F$; some regions have higher effective resolution, some lower. As implemented, B, C, and F are 7, 3, and 4 respectively. Thus, the entire FSR is divided into 8 coarse segments, defined by 9 adjustable breakpoints, and 16 linearly-spaced quantization levels within each coarse segment. The transient behavior of V_{REFH} and V_{REFL} during a conversion process is shown in Fig. 4.3, where the coarse regions can be unevenly spaced to provide enhanced resolution in selected regions of the FSR. Prior PWL-ADC architectures have been demonstrated using SAR architectures [58], [61]. While the ADC in [58] implemented a fixed, exponential transfer function, the architecture can be modified to support arbitrarily programmable non-linear transfer functions. Specifically, implementing the first stage as a thermometer-encoded CDAC [62] allows independent control over the width of each coarse segment due its inherent monotonicity, unlike binary-weighted encoding [60]. Using a thermometer-encoded DAC to define coarse-conversion segments provides increased flexibility for implementing programmable, piecewise-linear curves; representative transfer functions are shown in Fig. 4.2(b).

4.2.2 PWL-ADC Design Approach

The programmable first stage of the PWL-ADC is shown in Fig. 4.5(a). The design approach for choosing the number of unit capacitors and the number of coarse seg-

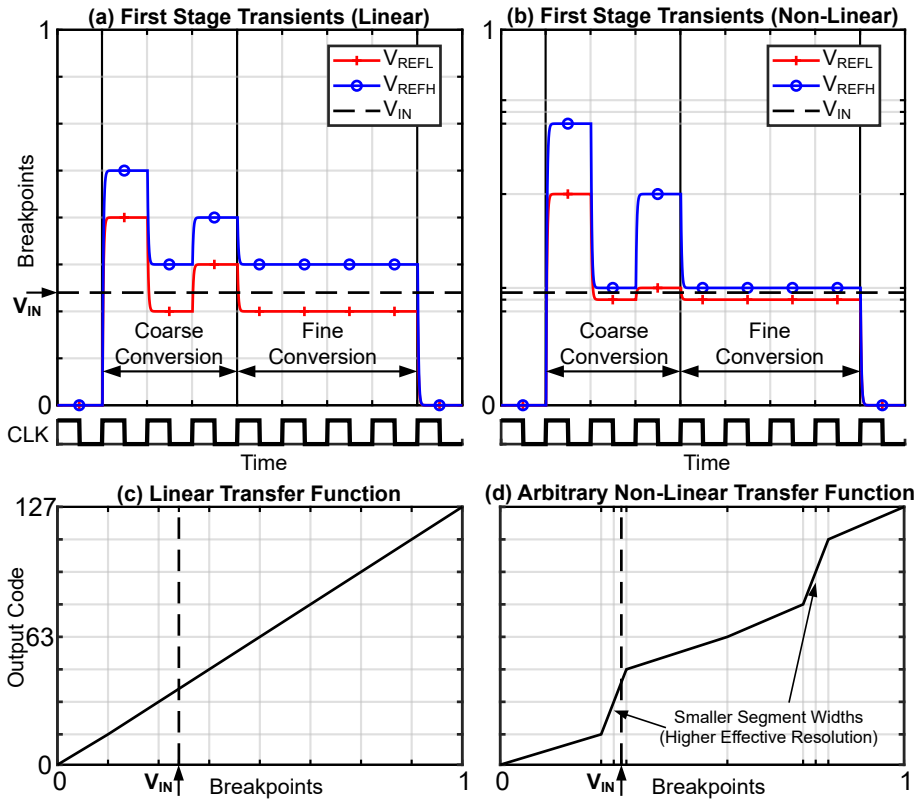


Figure 4.3: Coarse-conversion stage outputs (V_{REFH} and V_{REFL}) are simulated for linear (a) and piecewise-linear (b) operation, along with corresponding transfer functions in (c) and (d). V_{REFH} and V_{REFL} are fixed after coarse conversion, providing voltage references to the linear, fine-conversion stage [63].

ments is described here. Configuration flexibility of the programmed non-linearity and the accuracy of the PWL approximation are determined by the total number of unit capacitors used in each of the first stage DACs, N_{caps}, and the number of coarse bits, C. During coarse conversion, the effective resolution (ER) within the i^{th} coarse

segment is given by

$$ER_i = log_2\left(\frac{N_{caps}}{N_i}\right) + F \tag{4.2}$$
$$\text{where } N_{caps} = M \cdot 2^C;\ N_i \in \mathbb{N} : \sum_{i=1}^{2^C} N_i = N_{caps};\ C, F, M \in \mathbb{N}$$

where N_i is the number of capacitors switched to V_{REFP} in coarse segment i, and M is a multiplier.

To maximize available resources, we assume that all N_{caps} must be used to generate the 2^C+1 breakpoints. For $N_{caps} = 2^C$, only a linear transfer function may be realized, since the switching of each of the 2^C capacitors is controlled by exactly one of the 2^C thermometer-coded bits. By setting $N_{caps} > 2^C$ and varying the number of unit capacitors switched by each of the 2^C signals, different non-linearities may be realized. N_{caps} must still be an integer multiple of 2^C to allow a linear transfer function. From (4.2), there are broadly two possibilities for such architectures: for $M = 1$, only a single linear transfer function may be realized; and, for $M \geq 1$, both linear and PWL transfer functions may be realized.

Further, from (4.2), it is clear that ER_i is maximized when $N_i = 1$, representing the narrowest coarse conversion range. Maximum effective resolution can therefore be expressed as

$$ER_{i_{max}} = log_2\left(\frac{M \cdot 2^C}{1}\right) + F \tag{4.3}$$

which is in comparison to the effective resolution when the converter is configured as

a linear ADC, where the effective resolution is

$$ER_{i_{linear}} = log_2\left(\frac{M \cdot 2^C}{M}\right) + F \tag{4.4}$$

Subtracting (4.4) from (4.3) gives the "maximum gained bits" representing the additional bit-resolution in a coarse region:

$$Max.\ Gained\ Bits = ER_{i_{max}} - ER_{i_{linear}} = log_2 M \tag{4.5}$$

Relationship (4.5) allows the exploration of the trade-offs between PWL approximation accuracy provided by the coarse conversion regions (2^C), the number of required unit capacitors (N_{caps}), and maximum gained bits ($log_2 M$), as shown in Fig. 4.4. For a fixed C, each additional maximum gained bit requires an exponentially larger N_{caps}. It is also worth noting that increasing C results in a better PWL fit for a wider variety of non-linear curves. In practice, three to four coarse bits result in a good trade-off between accuracy, programmability, and resources, including required unit capacitors and required configuration logic [61]. As an additional design consideration, the matching of the capacitors and the performance of analog blocks such as amplifiers, switches, and comparators, need to satisfy the minimum requirements for the desired $ER_{i_{max}}$.

The targeted 0.18 μm CMOS process provides up to 10-bit capacitor matching, assuming good layout practices. Therefore, 10-bit performance was used as a target maximum effective resolution for the presented design. Thus, $C = 3$, $F = 4$, $M = 8$, and $N_{caps} = 64$ were chosen to maximize the number of bits gained (i.e. 3),

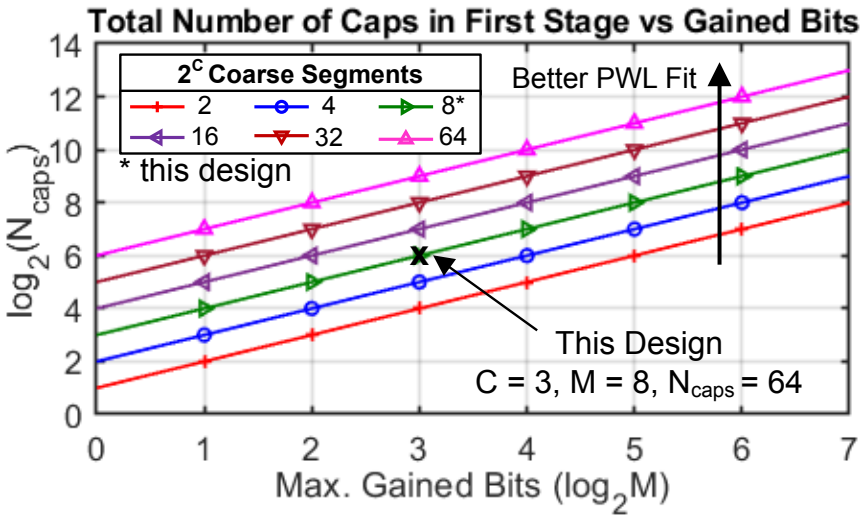


Figure 4.4: Varying N_{caps} and C results in varying number of maximum gained bits within a coarse segment. For a fixed number of coarse segments, for each additional gained bit, N_{caps} increases exponentially [63].

while also keeping N_{caps} relatively low. For the chosen values, with a total of 144 unit capacitors ($2\times64 + 16$), a theoretical maximum of 10-bit resolution can be achieved in selected regions of the FSR from a 7-bit PWL-ADC. Compared to 1024 unit capacitors required for a conventional 10-bit CDAC, this provides a significant reduction in capacitor area as well as improved matching due to this reduced area. Setting $N_i = 1$ in any 7 of the 8 coarse segments provides the maximum possible percentage of the FSR where 10-bit resolution can be achieved, which is $7/64 \approx 10.9\,\%$.

An important trade-off is the area overhead required for binary-to-thermometer decoding, and the logic and routing required to program the thermometer-encoded capacitor mapping to implement PWL transfer functions. However, as primarily

digital circuits, these will scale well with process node. The primary power overhead comes from the amplifiers used to buffer the first-stage DAC signals to the second stage.

4.2.3 Circuit Implementation

4.2.3.1 DACs and Switches

Each thermometer CDAC comprises 64 metal-oxide-metal (MOM) unit capacitors, $C_T = 10\,\text{fF}$ (Fig. 4.5(a)), for a total value of $0.64\,\text{pF}$ and occupies $194\,\mu\text{m}\times 15\,\mu\text{m}$. The binary CDAC, which is also the input sampling capacitor, comprises 16 metal-insulator-metal (MIM) unit capacitors, $C_B = 50\,\text{fF}$ (Fig. 4.2(a)), for a total value of $0.8\,\text{pF}$ and occupies $174\,\mu\text{m}\times 11\,\mu\text{m}$.

The capacitor types and sizes in each of the DACs were chosen as the minimum values for which foundry models are provided. As sized, the binary CDAC is conservative and exceeds 10-bit kT/C noise requirement ($> 52\,\text{fF}$ for FSR $= 1\,\text{V}$). As unit capacitor size directly impacts area and power consumption, smaller custom capacitors (eg: fringe capacitors) can be used in future implementations to improve power and area metrics, provided matching and noise limitations are met.

4.2.3.2 Digital circuits

The SAR logic core, binary-to-thermometer decoder, shift register, and multiplexer arrays are all synthesized using standard digital logic cells. The non-linearity is

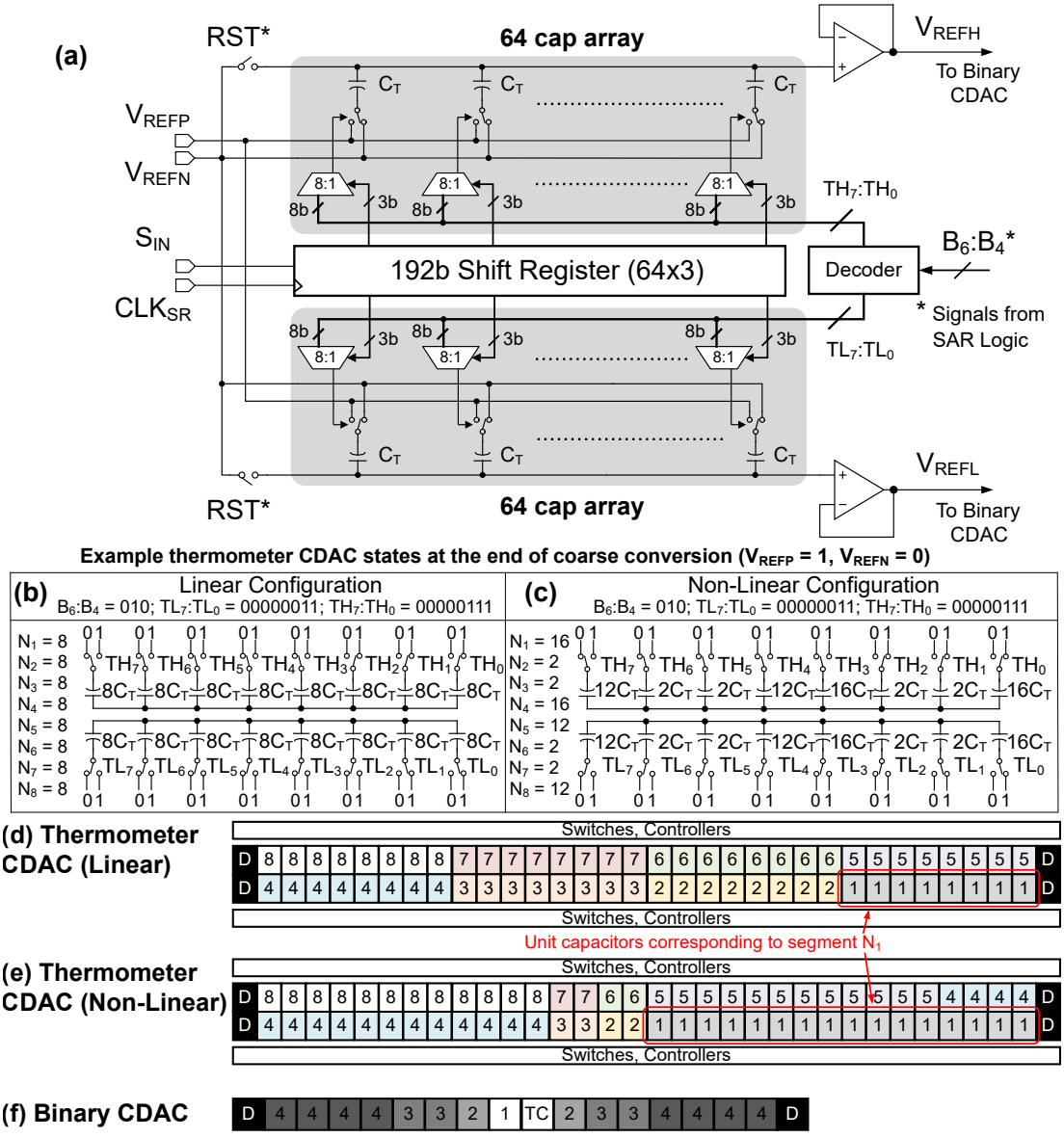


Figure 4.5: The core of the first stage as shown in (a), consists of two programmable thermometer-encoded CDACs with 64 unit capacitors (C_T = 10fF); (b) and (c) show the states of the thermometer CDACs at the end of the coarse-conversion examples as shown in Fig. 4.3(a-b) for linear and non-linear cases, respectively [63]. Corresponding DAC unit capacitor layouts are shown in (d), (e), and (f).

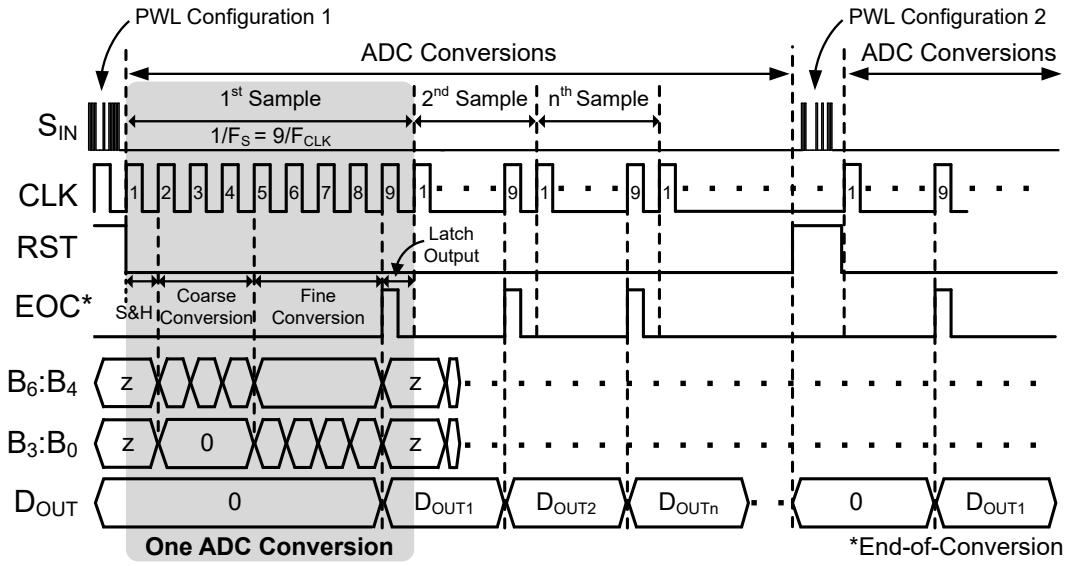


Figure 4.6: Varying N_{caps} and C results in varying number of maximum gained bits within a coarse segment. For a fixed number of coarse segments, for each additional gained bit, N_{caps} increases exponentially.

statically programmed prior to conversion by serially shifting in a 192-bit CDAC map via S_{IN}; this controls the routing of thermometer codes TH and TL via a 8:1 multiplexer for each unit capacitor in each coarse CDAC, with a 3-bit select word for each of the 64 multiplexers (Fig. 4.5(a)). This static programming need not be updated until an alternative transfer function is required. Note that both coarse CDACs receive the same 192-bit pattern; TH and TL are generated from the first 3 MSBs of the 7-bit binary code B_6:B_0, such that $TH = TL + 1$; this enables the generation of consecutive breakpoints. B_3:B_0, and TC control the switching of the binary-weighted, and termination capacitors in the second stage CDAC, respectively (Fig. 4.2(a)). The timing diagram of the control signals is shown in Fig. 4.6, with each ADC conversion taking 9 clock cycles.

4.2.3.3 Analog circuits

Two-stage Miller-compensated op-amps ($I_{\mathrm{BIAS}} = 4\,\mu\mathrm{A}$), shown in Fig. 4.7(a), are used in unity-gain feedback configuration to buffer the output of each first stage CDAC. The dynamic comparator design, shown in Fig. 4.7(b), was based on the Elzakker-comparator [64]. To minimize the effect of kickback, a continuous rather than dynamic pre-amplifier is used ($I_{\mathrm{BIAS}} = 0.1\,\mu\mathrm{A}$). Individual amplifier offset and comparator input-referred noise were simulated to be less than half of the target minimum 10-bit LSB ($< 0.49\,\mathrm{mV}$).

4.2.4 Measurement Results

The PWL-ADC was designed and fabricated in a $0.18\,\mu$m CMOS process; a die photograph is shown in Fig. 4.8. The ADC, including the 192-bit programming shift register, occupies an active area of $0.46\mathrm{mm}^2$ and uses a $1.8\,\mathrm{V}$ supply. The reference voltages, V_{REFP} and V_{REFN}, and the common-mode voltage, V_{CM}, are supplied externally. For all tests shown, $V_{\mathrm{REFP}} = 1.3\,\mathrm{V}$, $V_{\mathrm{REFN}} = 0.3\,\mathrm{V}$, and $V_{CM} = 0.8\,\mathrm{V}$. As configured, the PWL-ADC supports an input full-scale range of $0.95\,\mathrm{V_{PP}}$ and consumes $105\,\mu\mathrm{W}$ at a sampling frequency of $42\,\mathrm{kS/s}$.

4.2.4.1 Linear ADC characterization

The PWL-ADC was first characterized as an un-calibrated, 7-bit linear ADC, as shown in Fig. 4.10. To evaluate its dynamic performance, an audio analyzer (Audio-

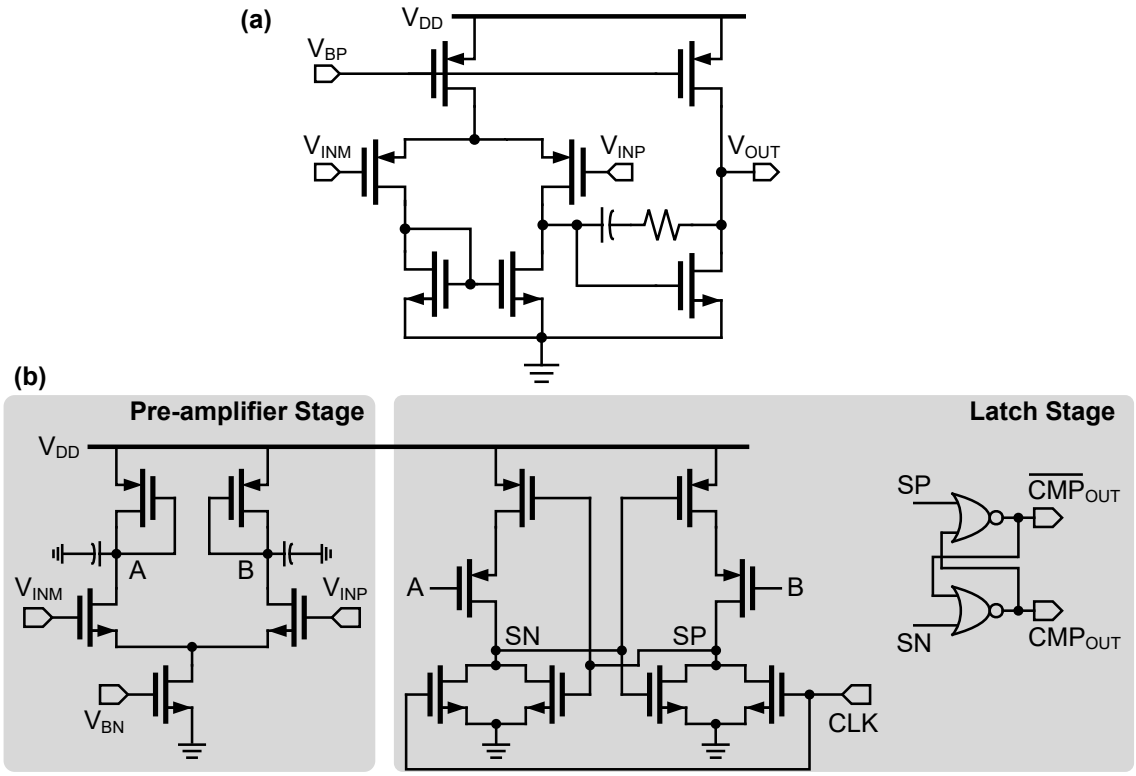


Figure 4.7: Schematics of the (a) two-stage Miller-compensated op-amp used as unity-gain buffer and (b) two-stage comparator based on [64].

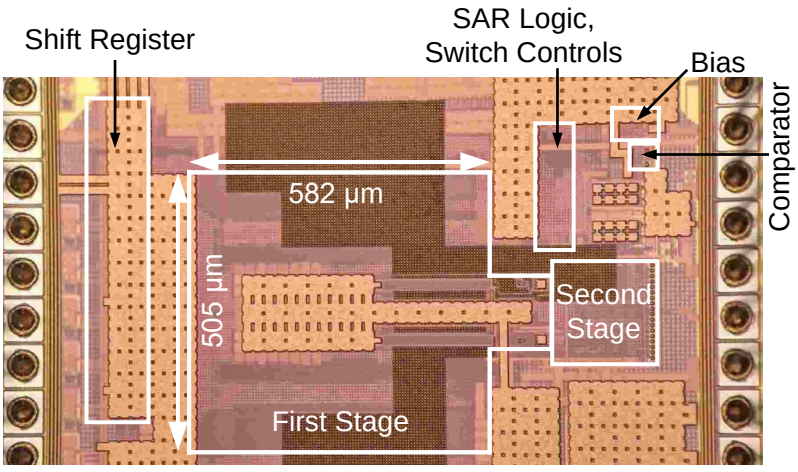


Figure 4.8: Die photograph of the prototype PWL-ADC 0.18 μm CMOS IC [63].

Precision APx555) was used to provide sinusoidal test input signals, and an arbitrary waveform generator (Rigol 1022A) was used to provide a ramp input for static tests. As a linear ADC, the converter achieves an ENOB of 6.6 bits across input frequency, which scales with input swing as expected. Transitions in the measured DNL and INL can be attributed to offset mismatch between the two buffer amplifiers, which leads to non-ideal alignment of quantization levels at the coarse segment boundaries. While less than 1 LSB across the FSR, the non-linearity due to this offset mismatch can be further minimized using offset-cancellation techniques in future work. As shown, analog power consumption is almost constant and dominates due to the the inter-stage buffers, which act as reference supplies for the fine CDAC. Digital power and total power consumption scale linearly with the sampling rate, as expected for a SAR ADC. As reference power consumption was negligible (tens of nanowatts) compared to analog and digital power, it was not included in the plot. In linear mode, the ADC achieves a FoM of 25.8 pJ/CS.

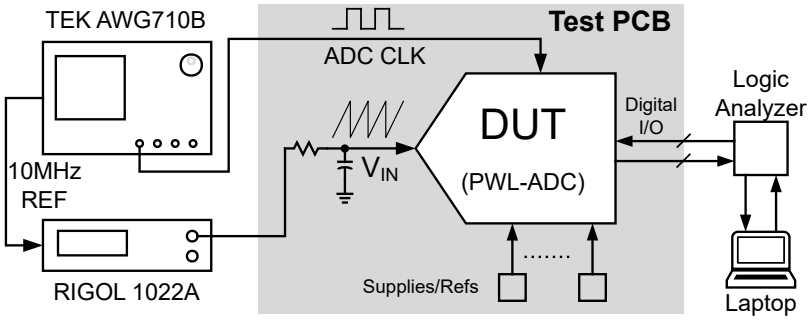


Figure 4.9: Schematic illustration of the ramp input code density test setup used to measure the various linear and non-linear transfer functions.

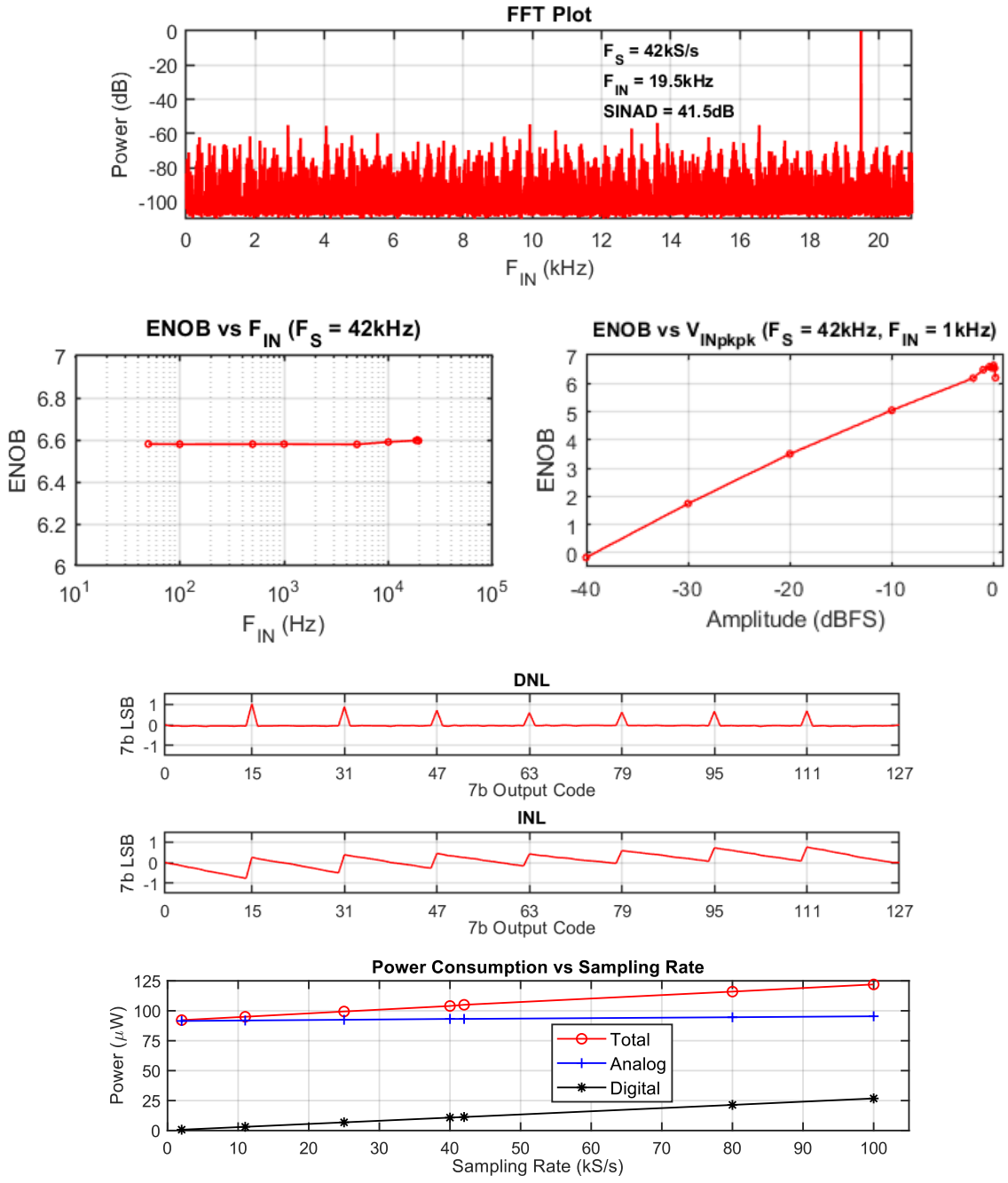


Figure 4.10: Measured static and dynamic performance of the PWL-ADC configured as an un-calibrated 7b linear converter [63].

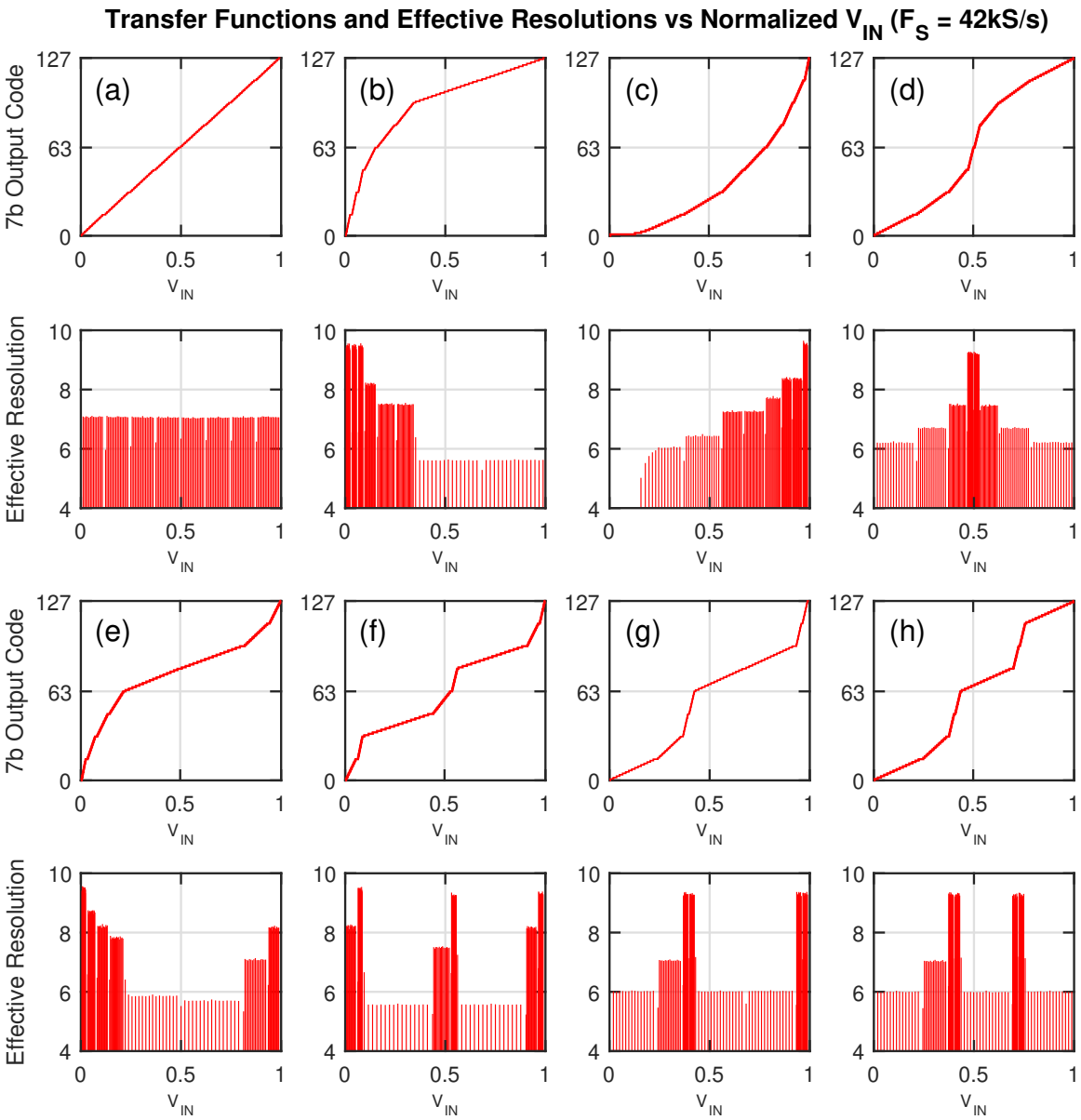


Figure 4.11: Measured transfer functions demonstrating the versatility of the reconfigurable PWL-ADC. Effective resolution within each coarse segment is shown below each corresponding transfer function [63].

4.2.4.2 PWL-ADC characterization

Multiple PWL transfer functions using the PWL-ADC were programmed and characterized, a subset of which are shown in Fig. 4.11. Ramp inputs from the Rigol 1022A were provided to the PWL-ADC, which was sequentially configured for linear and assorted non-linear transfer functions. It is evident that by using eight coarse PWL segments, a wide variety of non-linear transfer functions can be realized.

Figs. 4.11(f-h) demonstrate a primary benefit of using a thermometer-encoded CDAC for coarse conversion, which enables the realization of multiple regions of high ER across the entire FSR. This is a key improvement compared to prior implementations, where a maximum of two high-ER regions can be realized, and only near the lower and upper limits of the FSR [60]. The measured PWL-ADC has a minimum and maximum ER of 5.6-bit and 9.5-bit, respectively, demonstrating ∼4-bit adjustable effective resolution using a 7-bit output code word, a reduction of up to 26% of digital data compared to a general purpose ADC.

4.2.4.3 Reconstruction of analog input

While measured transfer functions in Fig. 4.11 are shown in the code domain, a measured analog input signal can be reconstructed in the voltage domain using the inverse transfer function. This is demonstrated in Fig. 4.12 for an input linear ramp signal. Using an ideal behavioral DAC with a transfer function equal to the inverse of the programmed non-linearity of the PWL-ADC, the measured input ramp waveform was reconstructed; regions of varying effective resolution are shown.

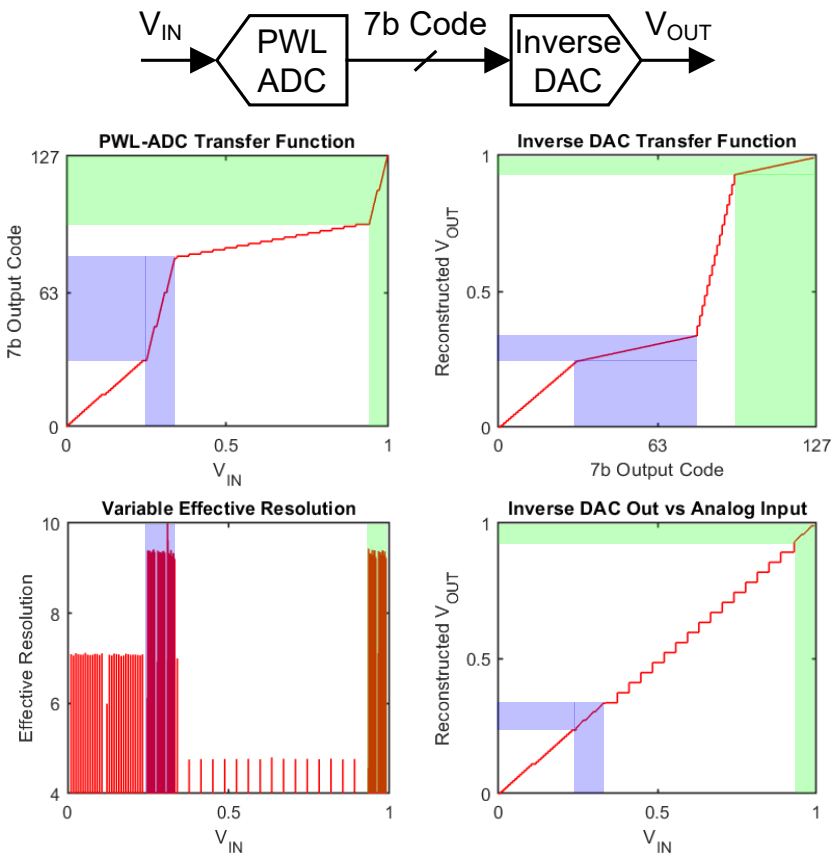


Figure 4.12: Reconstructed output of a measured input linear ramp by using an ideal DAC implementing the inverse of the PWL-ADC transfer function. The highlighted regions are regions of interest with higher effective resolution [63].

4.2.4.4 Example use case: ECG feature enhancement

Non-linear conversion provides the ability to emphasize and de-emphasize selected regions of the input signal in the digital domain. An example application is the selective enhancement of different peaks from an ECG recording: R-peaks can be emphasized for easier detection by automated algorithms, for insight into heart-rate related diagnostics, whereas for automated ischemia detection, ST episode detection

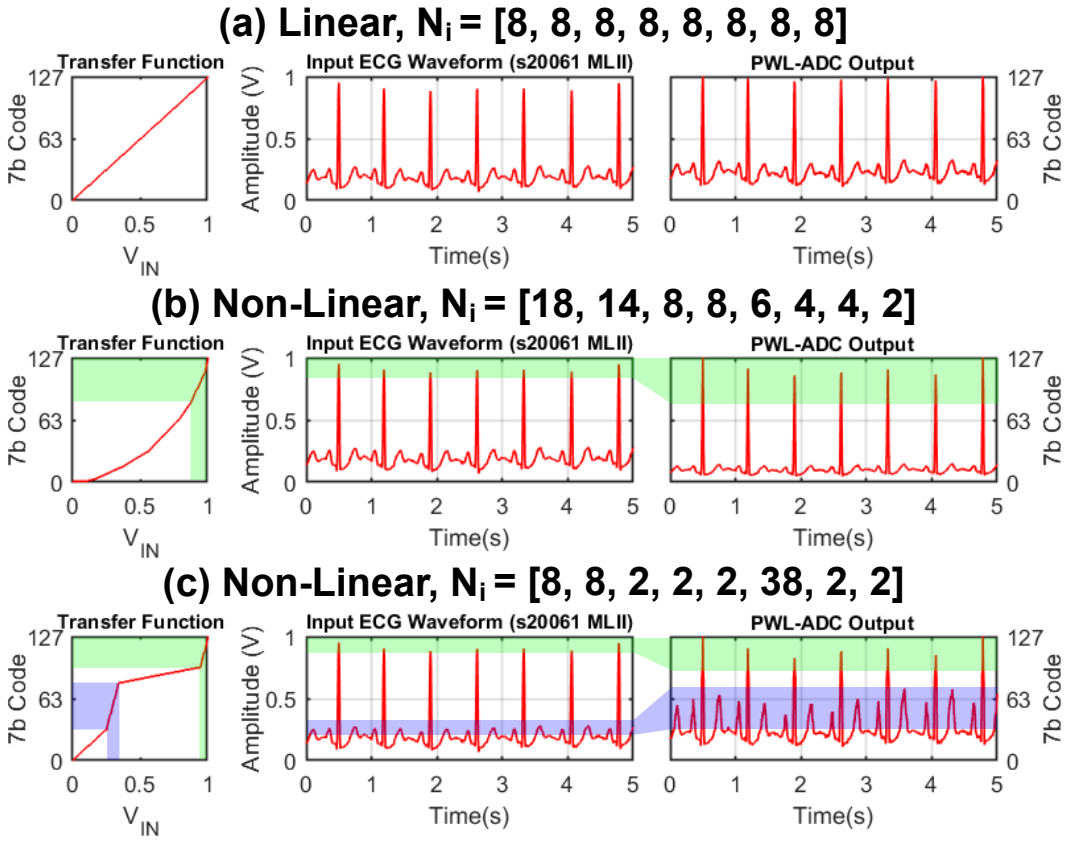


Figure 4.13: Measured ECG waveforms from the Long-Term ST Database [65], [66] digitized using linear and non-linear transformations to demonstrate enhancement of (b) R-peaks, and (c) both R-peaks and ST segments. Regions programmed for higher effective resolution are highlighted [63].

is important, and can benefit from the amplification of these segments [67]. As such, it may be beneficial to emphasize multiple regions of the ECG waveform. Fig. 4.13 compares the digital representations of an example ECG waveform from The Long-Term ST Database [65], [66] as measured by the PWL-ADC using linear and two non-linear transformations: enhancing only R-peaks (Fig. 4.13(b)), and enhancing both R-peaks and ST segments (Fig. 4.13(c)).

Table 4.1: Comparison of PWL-ADC with other recent non-linear ADCs

Reference	[57]	[58]	[60]	**This Work [63]**
CMOS Process (nm)	180	180	90	**180**
Programmable	No	No	Yes	**Yes**
Non-Linearity Type	Logarithmic	PWL Exponential	PWL Logarithmic Functions (log, exp, tanh, inv-tanh)	**PWL Arbitrary**
Output Word Length (bits)	8	8	5 - 9	**7**
Maximum Effective Resolution (bits)	13	10.5	9.5	**9.5**
Supply Voltage (V)	Analog: 1.62, Digital: 1.78	1.8	Analog: 1.2, Digital: 0.75	**1.8**
Input Range (V)	N.A.	1	1.8	**0.95**
Power @ Sampling Rate	2.54 mW[a] @ 22MS/s	40 μW @ 25kS/s	6.3 μW @ 33kS/s	**105 μW @ 42kS/s**
Active Area (mm^2)	0.56	0.036	0.7	**0.46**

[a.] Includes on-chip reference generation

4.3 Conclusion and Future Directions

A reconfigurable PWL-ADC was presented that extends the utility of non-linear ADCs to a wider range of data-constrained applications. Multiple, movable regions of high effective resolution enable PWL transfer functions for the ADC by employing a two-step SAR conversion process. Specifically, the use of a programmable, thermometer-encoded CDAC in the first stage enables arbitrary PWL configurations, in comparison with prior converters limited to exponential and logarithmic transfer functions. Measurements from a 0.18 μm CMOS IC demonstrate up to 2.5-bits

higher effective resolution in specific regions of interest. Multiple non-linear transfer functions were demonstrated to show the broad utility of the reconfigurable ADC for applications where information of interest is located in specific regions of the input FSR.

The proposed design provides motivation for multiple lines of future research work. As noted in the preceding sections, analog power consumption can be reduced with the use of small metal fringe capacitors in the CDACs [68]. Further power savings can be achieved by using dynamic and ring amplifier-based techniques in the inter-stage buffers [69]. Optimization of the arbitrary non-linearity logic mapping to the switching signals for the capacitors in the coarse DACs could result in significant reduction in routing overhead and total area. At the system level, simple histogramming could be used to estimate relative signal amplitude probability distributions. This can be used in feedback to set the desired non-linear curve based on maximizing the desired information content. This can be done with classical approaches such as maximizing Shannon entropy [70] or the Lloyd-Max algorithm [71], emerging machine-learning approaches, or more application-specific algorithms.

Chapter 5: A Programmable Gamma Spectrometer

5.1 Introduction

Scintillator crystal-based gamma spectrometers are extensively used to perform pulse-height analysis for radiation spectroscopy in nuclear applications including medicine, defense and security, environmental radioactivity monitoring, and fundamental research. A scintillator absorbs high-energy gamma ray photons and emits weak, fast light pulses requiring single-photon detector sensitivity. Silicon photomultipliers (SiPMs) have emerged as the preferred optical detector for such applications, owing to their advantages of size, scalability, ease of integration, cost, ruggedness, and low-voltage biasing (10s of volts) compared to photomultiplier tubes [72], [73].

In parallel, multichannel analyzer (MCA) electronic readout and processing systems with increasing levels of integration, programmability, and intelligence have been developed [72]–[74]. These systems typically target high-resolution performance and employ 10b-14b ADC resolution, requiring significant digital back-end resources for spectrum analysis. For battery-powered applications, such as distributed sensors for long-term nuclear safety monitoring, ADC resolution has been reduced as low as 6b for low-cost, low-complexity isotope identification [75]; while able to discriminate among certain isotopes, fewer, fixed energy bins limits minimum resolvable energy across the spectrum. A typical spectrometer based on a scintillator-SiPM detector and a MCA

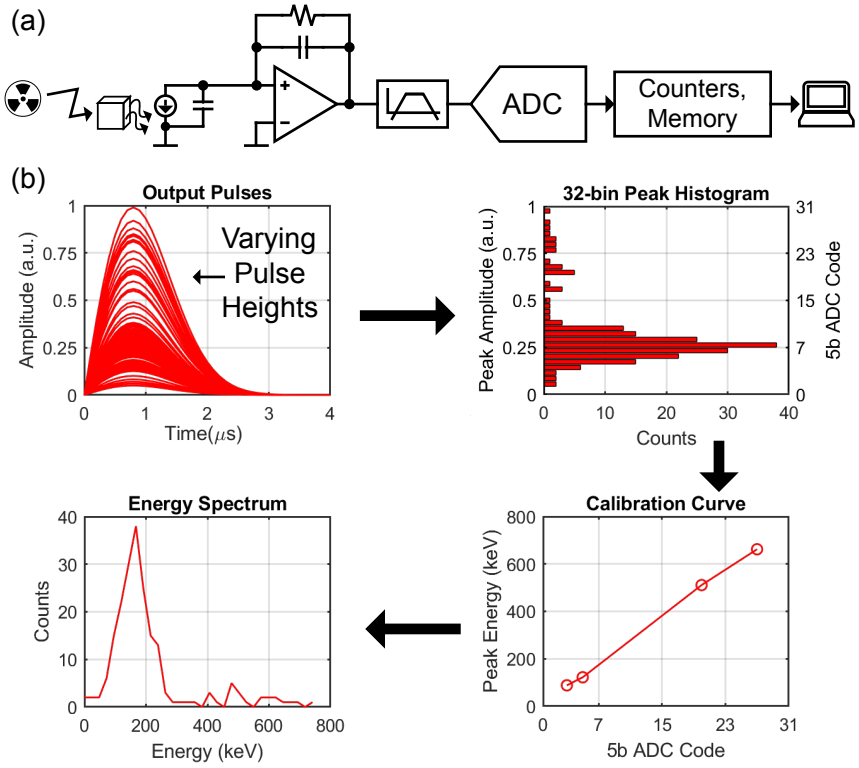


Figure 5.1: (a) A typical signal-chain for pulse-height analysis. (b) shows the steps involved in constructing an energy spectrum.

is shown in Fig. 5.1, and the concept of pulse-height analysis is highlighted as well.

In this work, we present a highly reconfigurable IC-based MCA to further the development of low-power radiation spectrometers. The implementated MCA has a programmable front-end enabling wide dynamic range, and a reconfigurable 7b piecewise-linear ADC with adjustable resolution, enabling variable channel width across a spectrum. Our approach allows for peak enhancement and easier discrimination while minimizing required back-end resources.

5.2 Proposed Reconfigurable Multichannel Analyzer

A detailed schematic of the MCA (as part of the spectrometer) is shown in Fig. 5.2, which broadly comprises 4 blocks: a scintillator crystal-SiPM assembly (detector/transducer), a programmable analog front-end (AFE) integrated circuit (IC) (analog domain), a programmable piecewise-linear analog-to-digital converter (PWL-ADC) IC (mixed-signal domain), and a FPGA-based digital back-end (DBE) (digital domain). A computer interfaced with the FPGA allows control of the MCA, as well as visualization and analysis of recorded spectra. While the overall signal chain is similar to that of conventional MCAs (Fig. 5.1) a primary contribution of this work is the high degree of programmability in both the AFE and ADC that allows for wide dynamic range and variable resolution across the dynamic range with a fixed digital word length, respectively. As shown in Section 5.2.3, this approach provides reconfigurable energy binning for isotope-specific resolution enhancement.

5.2.1 Detector

Upon absorbing a gamma ray photon with energy E, the scintillator emits a weak light pulse containing multiple ($\sim$10-40k per 1 MeV) visible-light photons with a crystal-specific wavelength distribution. The number of emitted photons, N, is approximately proportional to E. The SiPM absorbs these light pulses and discharges charge $Q \propto E$ as a current pulse, I_{IN}, with crystal-dependent decay time (few ns to μs).

As implemented, the detector is a 4-pixel SiPM (ONSemi ARRAYJ-600354P-PCB) with 2×2 6 mm pixels, each having 22,292 microcells (SPADs) [76]. Having a

high number of SPADs ensures that the SiPM does not saturate at higher gamma energy levels [72]. The SiPM was optically coupled to a $15\,\mathrm{mm}^3$ LYSO scintillator crystal with BC-630 optical grease.

5.2.2 Multichannel Analyzer

Upon gamma ray absorption in the crystal, the SiPM produces a current pulse, I_{IN}. The AFE (Fig. 5.2) integrates a scaled-down version of the current pulse, I_{CSA}, and converts it into a voltage pulse, V_{CSAOUT}, with a peak $V_{\mathrm{PEAK}} \propto Q$; therefore, $V_{\mathrm{PEAK}} \propto E$. The AFE holds V_{PEAK} which is converted into a digital word by the PWL-ADC.

The PWL-ADC is operated in triggered-mode and only samples peak values where $V_{\mathrm{PEAK}} > V_{\mathrm{TH}}$, thus rejecting low amplitude noise pulses. Each V_{PEAK} is converted to a digital output, $DOUT$, which is read by the DBE and binned into one of several bins (or digital codes). Over a period of time specified by the user, the DBE counts the number of occurrences in each bin (code) and saves these to memory.

Once the recording process is over, the memory contents can be accessed by a PC, and aggregated bin counts can be visualized as a histogram. After calibration with known gamma ray sources with well-defined energy peaks, the histogram can be visualized as an energy spectrum with each bin (code) corresponding to an energy $E \pm \Delta E$. By programming the PWL-ADC prior to recording a spectrum, the ΔE bin-width can be varied in specific regions of the full-scale range.

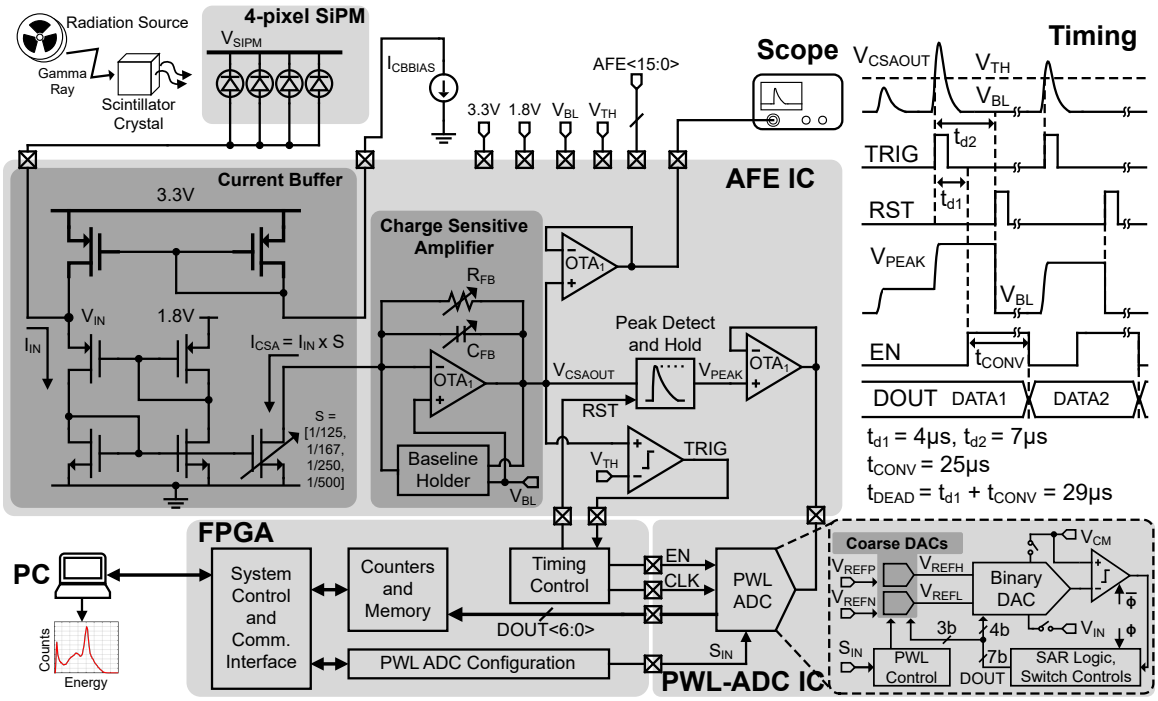


Figure 5.2: System-level schematic of the proposed MCA along with timing diagram of the internal signals [77]

5.2.2.1 Analog Domain: Analog Front-End IC

The SiPM output (anode) is connected directly to a current buffer, where a positive feedback loop sets the anode voltage (V_{IN} in Fig. 5.2) to a stable DC value, 1.8V in this design, ensuring stable SiPM biasing and gain [73], [78]. The current buffer also provides wide-bandwidth response and low input impedance. Additionally, the structure allows mirroring the input I_{IN} to the output I_{CSA} with an adjustable scaling factor, S (1/125, 1/167, 1/250, 1/500). This allows scaling I_{CSA} to accommodate the desired energy range for a constant integration time constant, $R_{\mathrm{FB}}C_{\mathrm{FB}}$, in the charge sensitive amplifier (CSA), to optimally use the ADC input full-scale range (FSR).

Mirroring also sets the polarity of I_{CSA} such that the CSA has positive output peaks. The current buffer operates with an externally supplied bias current I_{CBBIAS}, which can range from $10\,\mu$A to 15 mA, depending on desired performance.

A continuous time CSA was used, which allows observation of its output independent of any reset timing control. R_{FB} and C_{FB} can be tuned (25 kΩ to 1 MΩ, and 0.5 pF to 10 pF, respectively) for several gain and integration time constant settings. OTA_1 is implemented as a rail-to-rail folded-cascode amplifier with a class-AB buffer stage. A slow feedback loop provided by the Baseline Holder works to keep the baseline at an externally set voltage, V_{BL}, and it also performs dark current subtraction at the inverting terminal of OTA_1 [79].

The AFE also includes a continuous comparator [80] and a peak-detect and hold (PDH) circuit [81]. The comparator compares V_{CSAOUT} with externally set V_{TH} to generate a trigger signal $TRIG$. The PDH works as an envelope detector for V_{CSAOUT} and holds the peak value, V_{PEAK}, for ADC sampling. $TRIG$ is used to trigger timing control state machines in the DBE, including resetting the PDH with RST and enabling the ADC to sample and convert V_{PEAK}. V_{CSAOUT} and V_{PEAK} are buffered using OTA_1. The different AFE settings are digitally controlled via 16 control bits, $AFE_{15:0}$.

5.2.2.2 Mixed-Signal Domain: PWL-ADC IC

A programmable, piecewise-linear ADC is used for digitization of V_{PEAK}. While this can be operated as a linear ADC, it can also be configured to perform conversions with

a variety of non-linear transfer characteristics, allowing adjustable ADC resolution and thus adjustable conversion gain (i.e ΔE/bin) in specific regions of interest across the ADC full-scale range. An advantage of employing non-linearity is that a smaller or larger ΔE than allowed by a linear 7b ADC, can be obtained in specific regions with a 7b digital word, which serves to reduce the amount of digtial data to be processed in the DBE, while allowing optimal distribution of a limited number of ADC bins across different energy peak areas.

The PWL-ADC used in this work was detailed previously in [63]. When the AFE comparator generates a $TRIG$ signal, provided it is idle, the ADC samples V_{PEAK} and converts it into a 7-bit digital word, thereby binning V_{PEAK} into one of $2^7 = 128$ bins. By operating the ADC in a triggered mode, the sampling rate depends on the detection rate. Along with peak-height detection, this allows a drastic reduction in data transmission rate to the DBE when compared to MCAs where a constant sampling rate is used to digitize each pulse shape in its entirety for digital-post processing.

5.2.2.3 Digital Domain: FPGA-based Digital Back-End

The DBE comprises finite state machines (FSMs), counters, memory, and communication interfaces implemented on a Xilinx Spartan-6 FPGA (OpalKelly XEM-6310). The FSMs generate control signals for resetting the PDH, enabling ADC sampling and conversion, and performing histogramming. The histogrammer uses 128 32-bit wide counters to support long-duration recording. A USB3.0 link with a PC allows

the user to communicate with the FPGA for control and data acquisition.

5.2.3 Radiation Spectroscopy Measurements

5.2.3.1 Experimental Setup

The proposed MCA was validated using two prototype ICs (AFE and PWL-ADC) fabricated in a general purpose 0.18 μm CMOS process. The test setup and die photographs are shown in Fig. 5.3. Each IC package was placed in a separate test PCB enabling standalone as well as system-level characterization. The AFE was

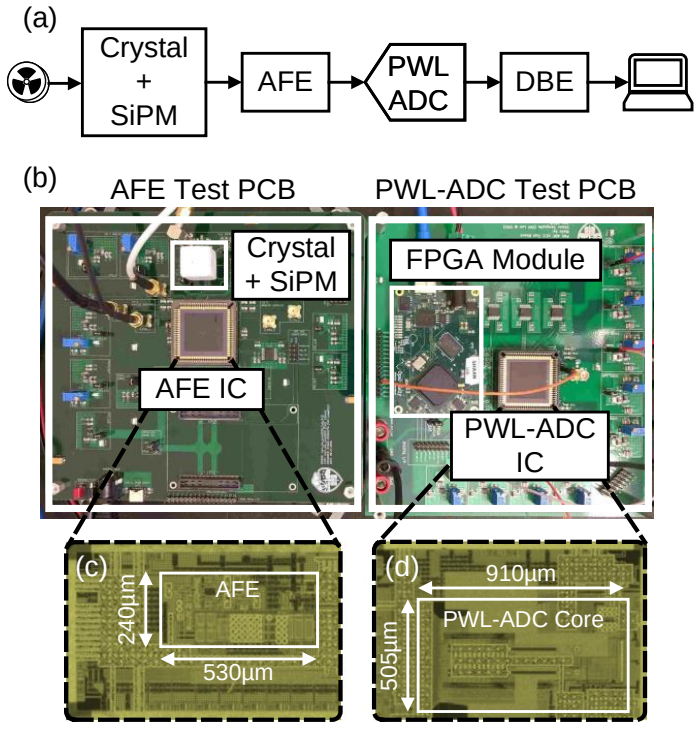


Figure 5.3: (a) A high-level block diagram and (b) photograph of the test setup. Die photographs of the prototype AFE and PWL-ADC 0.18 μm CMOS ICs are shown in (c) and (d), respectively.

supplied at 3.3 V and 1.8 V, and the PWL-ADC at 1.8 V. The SiPM cathode, V_{SIPM}, was set to 29.5 V, for $V_{\mathrm{BIAS}} = V_{\mathrm{SIPM}} - V_{\mathrm{IN}} = 29.5\,\mathrm{V} - 1.8\,\mathrm{V} = 27.7\,\mathrm{V}$, corresponding to an excess voltage of ∼3.3 V. The test setup was placed in a light-tight optical enclosure, and the crystal-SiPM assembly was covered with a 3D printed cover that also held the isotope check source at a distance of ∼6 mm from the crystal. In the CSA, $R_{\mathrm{FB}}C_{\mathrm{FB}}$ was set to 250 ns, ∼5× LYSO's decay time constant (40-50 ns). The AFE input scaling was set to $S = 1/167$, allowing optimal use of the ADC input FSR while accommodating peak energies of interest. The MCA was programmed for a dead-time of $t_{\mathrm{DEAD}} = 29\,\mu$s, during which the ADC samples and converts a peak value (Fig. 5.2). This results in a maximum counting rate of ∼33 kcps, which is sufficiently fast for most applications. Functional verification of the AFE operation is validated in the oscilloscope persistence capture in Fig. 5.4(a), while the overall system timing operation is shown in Fig. 5.4(b) validating operation at 33 kcps.

We note that of the 128 corresponding energy bins (7b), the first and last were omitted from data processing where out-of-range noise collects, as were the 7 evenly-spaced bins corresponding edges in the piecewise-linear transfer curve that have high DNL [63], resulting in a total of 119 energy bins used in the calculated energy histograms.

5.2.3.2 Linear-Mode Measurements

To characterize the MCA in linear mode, several energy histograms were recorded while maintaining constant AFE and SiPM settings. For calibration of the MCA,

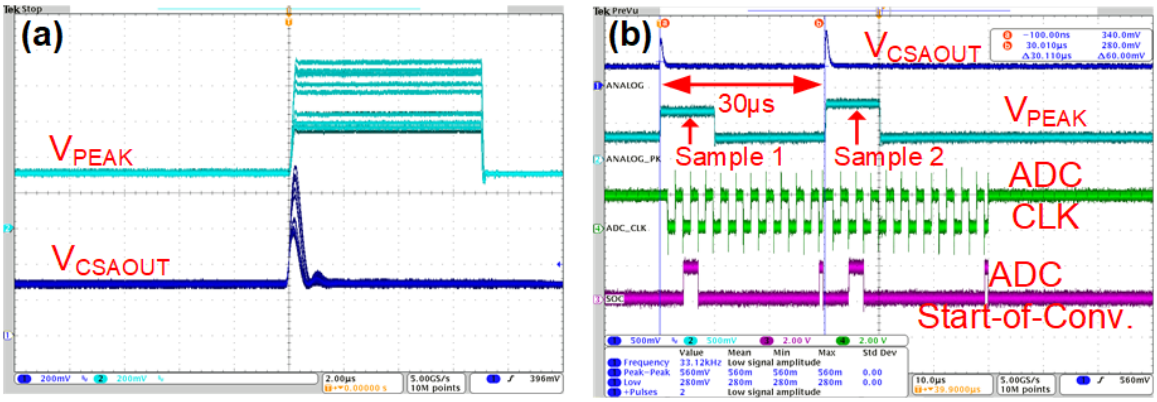


Figure 5.4: Oscilloscope images of (a) persistence capture of CSA and PDH outputs, and (b) MCA system timing validating maximum count rate of 33 kcps.

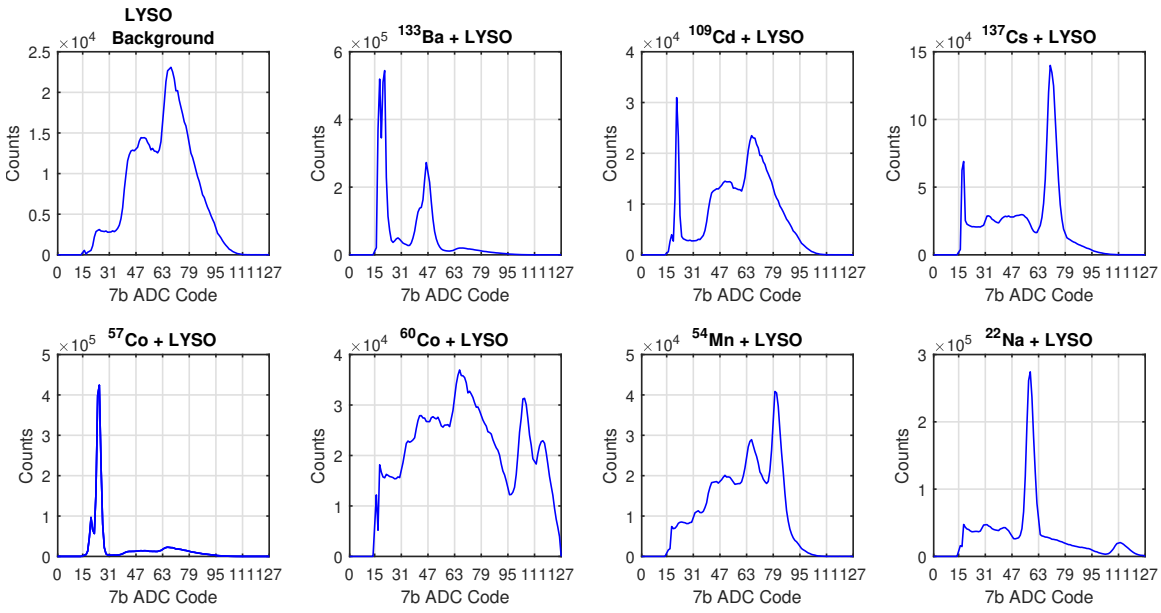


Figure 5.5: Measured histograms/spectra of LYSO background and calibrated isotopes. Each spectrum was recorded for a period of 15 minutes.

histograms of 8 calibrated isotope sources (see Appendix A for details) with characteristic energy peaks ranging from 32 keV to 1.33 MeV (^{133}Ba, ^{109}Cd, ^{137}Cs, ^{57}Co, ^{60}Co, ^{54}Mn, ^{22}Na, and ^{65}Zn) were recorded. Seven of these (all but ^{65}Zn) are shown in Fig. 5.5. Since LYSO has significant intrinsic activity, the LYSO background spectrum was recorded separately (Fig. 5.5) and subtracted from the isotope spectra prior to generating the calibration curve. This was followed by Gaussian curve fitting for each energy peak as shown in the ^{137}Cs example in Fig. 5.6. Additionally, a spectrum of a stack of ^{137}Cs, ^{22}Na, and ^{60}Co microcurie check sources is shown in Fig. 5.7(a) without any background subtraction, demonstrating the ability of the MCA to capture multiple energy peaks across a wide range in a single recorded spectrum. After Gaussian fitting, the peak location data from 356 keV to 1.33 MeV was used to generate a linear fit (Fig. 5.7(b)). From the calibration data, energy resolution was calculated as percentage full-width half maximum (% FWHM) as shown in Fig. 5.6, and is plotted across the measured energy peaks (Fig. 5.8). As expected, the curve is inversely proportional to $\sqrt{\text{Energy}}$ [82]. In this configuration, the energy resolution was observed to be 13.1% (FWHM @662 keV).

To demonstrate the programmability of the AFE current buffer scaling factor, S, histograms with ^{133}Ba and ^{54}Mn were recorded with varying S. The slope of the lines connecting the 356 keV (^{133}Ba) and 835 keV (^{54}Mn) peak locations was used to calculate the corresponding energy bin-widths (ΔE/bin). As shown in Fig. 5.9, the bin-width scales linearly with S^{-1}, validating the AFE programmability. This allows a direct trade-off between resolution and dynamic range in linear mode. The estimated maximum measurable energy is about 3.8 MeV based on extrapolation of

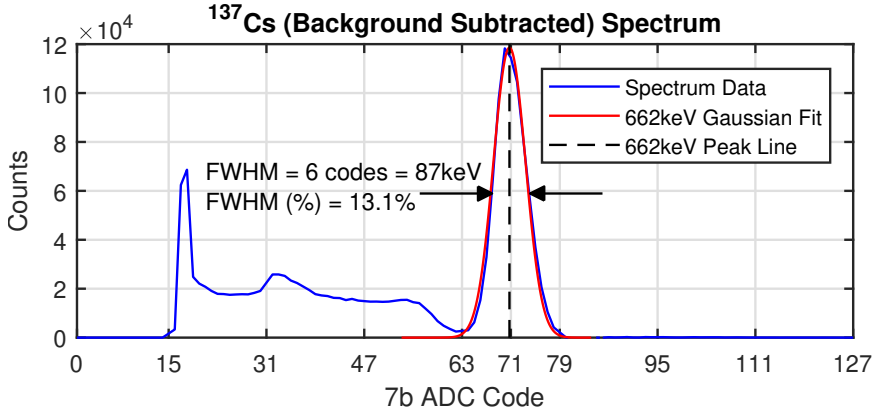


Figure 5.6: Example of Gaussian fitting in background subtracted ^{137}Cs spectrum to determine location of characteristic 662keV peak and full-width half maximum (FWHM).

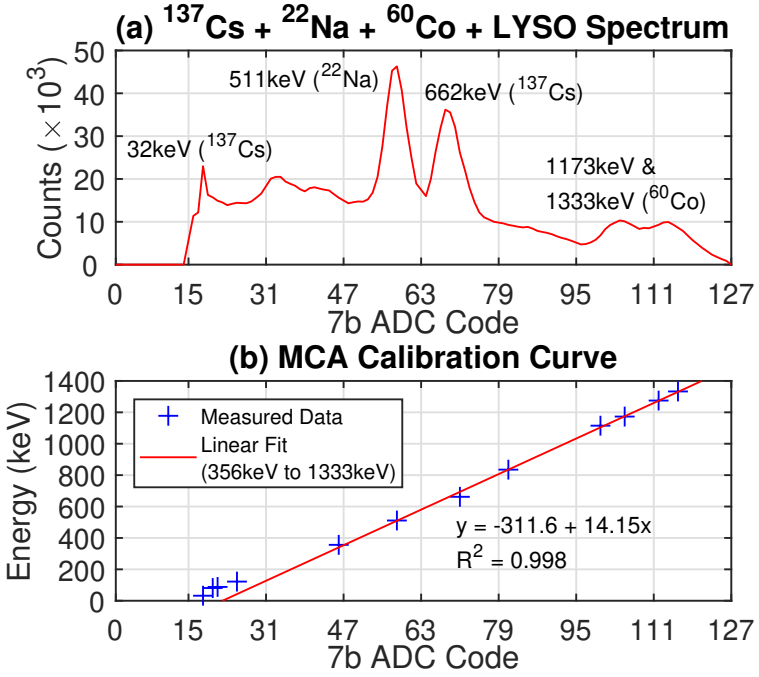


Figure 5.7: An example spectrum of a mix of sources with a wide range of peaks is shown in (a). Multiple measured peak locations used for a linear fit calibration are shown in (b) [77].

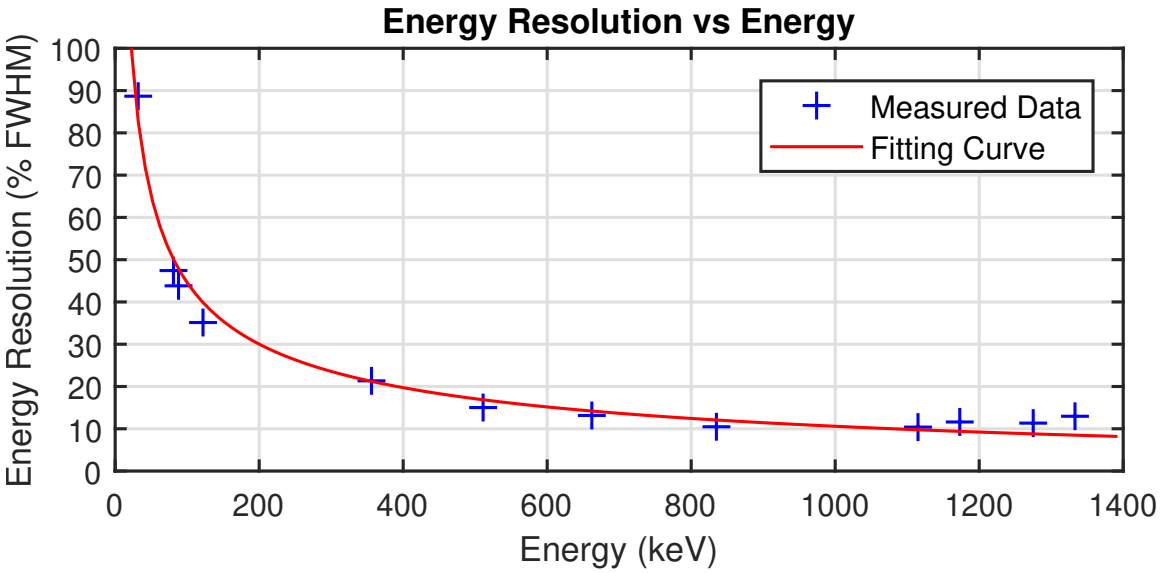


Figure 5.8: Energy resolutions across measured energy peaks when MCA is operated in linear-mode.

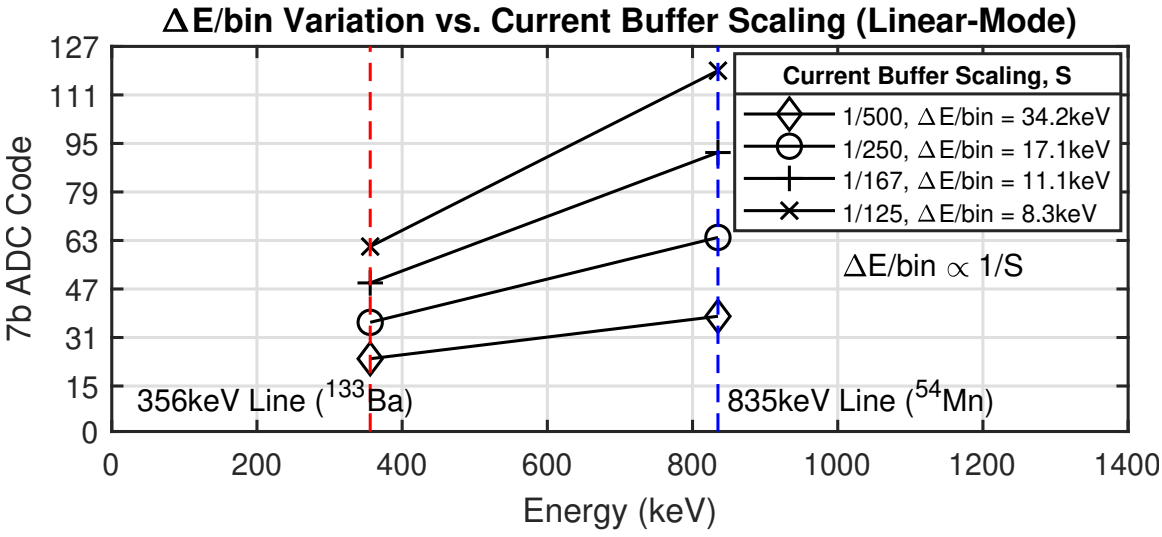


Figure 5.9: ΔE/bin across varying AFE current buffer scaling options, S, calculated from spectra containing 356 keV (^{133}Ba) and 835 keV(^{54}Mn) peaks.

the line corresponding to $S = 1/500$ at code 126.

5.2.3.3 Non-Linear-Mode Measurements

Several measurements were made to demonstrate the utility of the PWL-ADC reconfigurability in the MCA. A linear ^{22}Na spectrum was first recorded (Fig.5.10(a)) in which the 511 keV peak is clearly visible. However, the 1275 keV peak is less visible due in part to the relative intensities of ^{22}Na emissions, and in part to the expected broadening of peaks at high energies [82]. Especially in applications where the recording time is limited, this can result in missed peaks due to statistical noise. This can be mitigated by redistributing the number and width of bins assigned to each peak area more optimally. As shown in Fig.5.10(b), by assigning fewer bins to the 1275 keV peak, the underlying Gaussian nature of the peak is visible.

Figs. 5.11(a-b) show linear and non-linear spectra recorded from multiple sources with characteristic low-energy peaks (32 keV, 81 keV, and 122 keV). In the linear spectrum, the low-energy peaks are narrower than the higher energy peaks and are very closely spaced, making it difficult to discriminate among them. By increasing ADC resolution in this region, more, narrower bins are assigned to each peak, resulting in more distinguishable peaks. As a trade-off, fewer bins were assigned to the broader 662 keV peak, which is sufficiently far from other peaks; reducing ADC resolution here has little impact in identifying it in the corresponding non-linear spectrum.

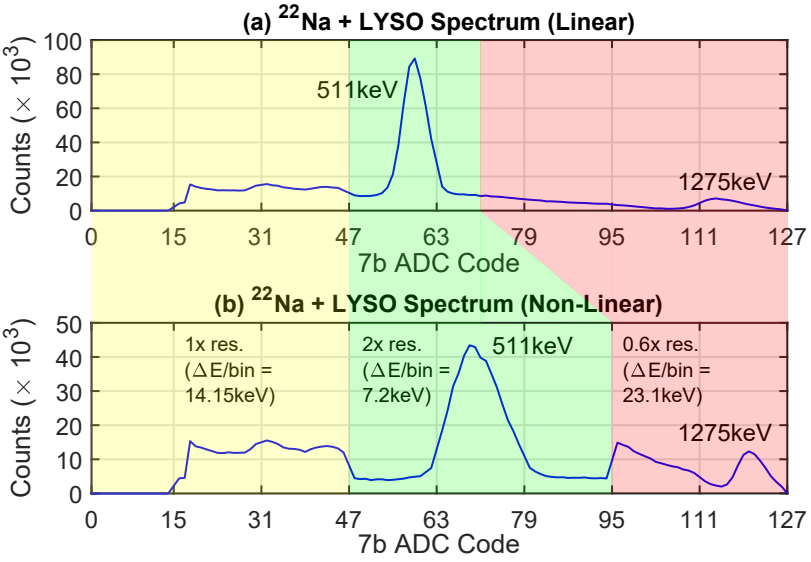


Figure 5.10: Measured ^{22}Na spectrum (with LYSO background) in (a) linear-mode and (b) non-linear-mode; corresponding regions in linear and non-linear measurements are shaded with the same color [77].

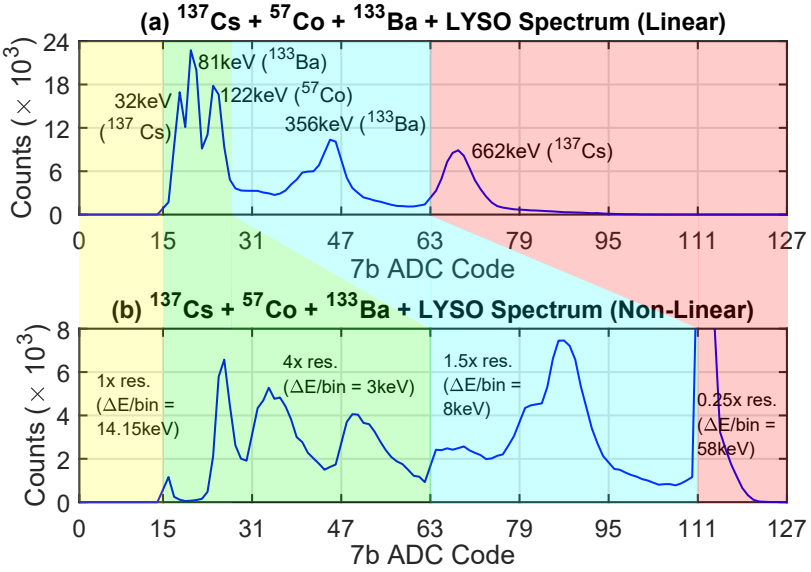


Figure 5.11: Measured spectrum containing ^{137}Cs, ^{57}Co, and ^{133}Ba (with LYSO background) in (a) linear-mode and (b) non-linear-mode; corresponding regions in linear and non-linear measurements are shaded with the same color [77].

Table 5.1: Performance Summary of Proposed Multichannel Analyzer

Ref.	**[72]**	**[74]**	**[73]**	**[75]**	**This Work [77]**	
CMOS Process (μm)	Discrete	0.13	0.35	0.5	**0.18**	
Detector Type	CsI(Tl) + SiPM	[NaI(Tl), LaBr] + PMT	LaBr + SiPM	[NaI(Tl), LaBr] + PMT	**LYSO + SiPM**	
ADC Res. (bits)	12	10	12	6	**5 - 9**	
Bins	2048	1024	1200	64	**128**	
Δ E[a] (keV)	0.4	1.46	0.6	20	**3 - 58**	
Power	460 mW[b]	4 μW[c,d]	16 mW[e]	N.A.	**AFE: 114 mW[c]**	**ADC: 0.1 mW[c]**
Area (mm^2)	N/A	0.24[d]	0.25[e]	N.A.	**0.13**	**0.46**

[a]Estimation based on slope of linear-fit of published results [b]System Power [c]@1kcps mean event rate
[d]AFE & ADC [e]AFE Only

5.2.4 Conclusion

As demonstrated by the reconfigurable MCA, by varying bin-widths in different regions of the spectrum by using a programmable non-linear ADC, limited ADC bins are utilized more efficiently. This provides proof-of-principle for the presented approach, which in future work will further the ability to provide low-power, portable radiation spectrometry.

Chapter 6: Conclusions

As part of this dissertation, novel block- and system-level designs were proposed across the signal chain of an electronic sensor system for a variety of application scenarios, with a particular emphasis on leveraging standard CMOS technology.

The first broad goal was to investigate transducers that can be implemented using standard CMOS fabrication processes, without any additional post-processing steps. To that end, several CMOS-based single-photon avalanche diodes (SPADs) were designed and characterized for a different optical sensing applications. A transducer for flow-sensing was also implemented using top-metal BEOL layers. Without any post-processing, it was used in a compact, fully integrated CMOS single-element flow sensor. The CMOS implementations of both transducers allow easier integration with on-chip microfluidic channels for bio-chemical applications. As an extension of this work, the interplay between transducers and readout circuits was explored. Specifically the digital-like SPAD output greatly simplifies readout circuits. These ideas were validated by measured results from a highly digital CMOS ambient light sensor which uses a single SPAD pixel with a metal-fill optical filter, resulting in one of the smallest reported areas in the literature. The massive reduction in area, particularly the diode, along with the synthesized digital readout circuits allows easy integration in system-on-chip (SoC) applications. Future work can include on-chip integration of SPAD biasing circuits, and linearization and DSP circuits.

The second broad goal was to investigate information-aware quantization for sensors. IC implementations of non-uniform quantization were explored as a step towards efficient utilization of limited bits and quantization levels. Existing work in static non-linear SAR ADCs was extended to design a widely programmable Piecewise-Linear ADC (PWL-ADC) IC which is able to achieve several arbitrarily defined non-linear transfer functions. This allows multiple user-defined regions of interest with variable resolutions and the following benefits: 1) Reduction of digital data and resource utilization in the back-end by reducing the bit-width; 2) Embedded feature enhancement or suppression by utilizing the non-linear characteristics of quantization; 3) Programmability can allow its usage in a multi-sensor SoC where multiple sensors and AFEs requiring different non-linearities could be multiplexed to a singular PWL-ADC. Measured linear and non-linear transfer curves as well as non-linearly quantized ECG waveforms were used to validate the proposed idea. Future work can incorporate histogramming-in-the-loop to monitor signal statistics, which can be used for non-linearity programming to maximize information entropy. Max-Lloyd algorithm is another approach that can be used to determine non-linearity, for minimizing signal distortion. To highlight system-level benefits, the PWL-ADC IC was used along with a custom-designed AFE IC and a FPGA-based DBE as a multichannel analyzer (MCA), for use in a silicon photomultiplier (SiPM)-based gamma spectrometer. Programmability in both the AFE and the PWL-ADC enable the recording of a wide dynamic range of gamma energies, variable integration times for different detector configurations, and variable energy bin-widths for better isotope peak identification and discrimination.

Chapter 7: Summary of Contributions

A list of the peer-reviewed publications resulting from this dissertation work is summarized below:

1. **CMOS Transducers**:

S. Bose, H. Ouh, S. Sengupta, and M. L. Johnston, "Parametric Study of p-n Junctions and Structures for CMOS-Integrated Single-Photon Avalanche Diodes," *IEEE Sensors Journal*, vol. 18, no. 13, pp. 5291–5299, 2018

M. Lindsay, K. Bishop, S. Sengupta, M. Co, M. Cumbie, C.-H. Chen, and M. L. Johnston, "Heterogeneous Integration of CMOS Sensors and Fluidic Networks Using Wafer-Level Molding," *IEEE Transactions on Biomedical Circuits and Systems*, no. 99, pp. 1–10, 2018

M. Lindsay, S. Sengupta, K. Bishop, M. Co, C.-H. Chen, M. Cumbie, and M. L. Johnston, "Scalable hybrid integration of CMOS circuits and fluidic networks for biosensor applications," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2017, pp. 1–4

K. Clocker, S. Sengupta, and M. L. Johnston, "A Fully-Integrated, Single-Element CMOS Anemometer," *IEEE Sensors Letters*, vol. 3, no. 2, pp. 1–4, 2019

K. Clocker, S. Sengupta, M. Lindsay, and M. L. Johnston, "Single-element thermal flow sensor using dual-slope control scheme," in *2017 IEEE SENSORS*, 2017, pp. 1–3

2. **CMOS SPAD Systems**:

S. Sengupta, H. Ouh, and M. L. Johnston, "An all-digital CMOS ambient light sensor using a single photon avalanche diode," in *2017 IEEE SENSORS*, 2017, pp. 1–3

H. Ouh, S. Sengupta, S. Bose, and M. L. Johnston, "Dual-mode, enhanced dynamic range CMOS optical sensor for biomedical applications," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2017, pp. 1–4

3. **Information-Aware ADC**:

S. Sengupta and M. L. Johnston, "A Widely Reconfigurable Piecewise-Linear ADC for Information-Aware Quantization," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1073–1077, 2021

S. Sengupta and M. L. Johnston, "Two-step, piecewise-linear SAR ADC with programmable transfer function," *Electronics Letters*, vol. 55, no. 8, pp. 444–446, 2019

4. **Gamma Spectrometer**:

S. Sengupta and M. L. Johnston, "A Multichannel Analyzer with Programmable Energy Bins for Gamma Ray Spectroscopy," in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2021, pp. 121–124

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APPENDICES

Appendix A: Calibration Isotope Peak Energies

Calibrated disk isotope sources were used for the characterization of the programmable spectrometer in Chapter 5. For each of the isotopes, the energy peaks of interest are listed in Table A.1. The prominent peaks are in bold and both X-Ray, and γ-Ray peaks are included.

Table A.1: Calibration Isotope Data

Isotope	**Original Activity (Calibration Date)**	**Half-Life**	**Activity in April 2021**	**Peaks of Interest (MeV)**
Ba133	1 µCi (06/2019)	10.5 years	0.89 µCi	**0.081**, 0.276, 0.303, **0.356**, 0.384
Cd109	1 µCi (08/2019)	463 days	0.4 µCi	**0.022**, **0.088**
Cs137	1 µCi (07/2019)	30.1 years	0.96 µCi	**0.032**, **0.662**
Co57	1 µCi (08/2019)	272 days	0.21 µCi	**0.046**, **0.122**, 0.136
Co60	1 µCi (08/2019)	5.27 years	0.8 µCi	**1.173**, **1.333**
Mn54	1 µCi (08/2019)	312 days	0.26 µCi	**0.835**
Na22	1 µCi (08/2019)	2.6 years	0.64 µCi	**0.511**, **1.275**
Unknown (Cs137 & Zn65)	0.5 µCi & 1 µCi (08/2019)	30.1 years & 244 days	0.48 µCi & 0.18 µCi	**0.662**, **1.115**