AN ABSTRACT OF THE DISSERTATION OF

Lukang Shi for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on December 3, 2019.

Title: Active Noise Shaping Analog-to-Digital Data Converters

Abstract approved:

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Gabor C. Temes

Successive-approximation-register (SAR) analog-to-digital converters are popular for medium accuracy, medium speed and low power applications, such as in biomedical applications. They have low latency and simple architecture compared with ΔΣ ADCs. This is because of SAR ADCs' binary searching scheme. Furthermore, SAR ADCs can apply oversampling and noise shaping schemes which are used in ΔΣ ADCs. As a result, the noise-shaping SAR ADC architecture has received more and more attention as a high resolution and power efficient solution for many sensor applications. In this

dissertation, novel configurations have been explored for noise-shaping SAR ADCs for power-efficient and high-accuracy data conversion.

Frist, a first-order noise-shaping (NS) SAR ADC using a two-capacitor based DAC (2-C DAC) is described and discussed. There are only two equal valued capacitors used in the DAC, so the total number of capacitors is much less than in conventional binary weighted DAC. Therefore, the 2-C DAC is good for capacitor matching. Furthermore, this 2-C DAC architecture only samples the reference once, so that the proposed NS SAR ADC doesn't need a reference buffer on or off chip. An active integrator is implemented and used to contribute an ideal first order noise shaping effect and can be extended to second order noise shaping by adding a few extra capacitors with only one integrator. The ADC was fabricated in 180nm CMOS technology. The prototype occupies 0.25mm^2. For a 2kHz signal bandwidth, it achieved 78.9dB SNDR and 87.6dB SFDR with a 32 oversampling ratio (OSR). It consumes 74.2 uW power from 1.5V power supply.

Next, a noise shaping SAR ADC with on-chip digital DAC calibration was proposed and implemented. Correlated double sampling (CDS) and correlated level shifting (CLS) are combined to implement the proposed architecture. With these two techniques, the design specifications for the op-amp used in integrator are relaxed. CDS minimized the effect of DC offset and flicker noise from the op-amp, and CLS boosted the effective DC gain of the op-amp. Therefore, the total power consumption of the op-amp can be decreased by about 50% compared with the same NS SAR ADC performance. Also, an incremental ADC (IADC) based on-chip DAC calibration scheme was proposed and implemented. The proposed calibration scheme will share

all blocks in the proposed NS SAR ADC, so it will not increase the complexity of the circuitry. The calibration, it gives a more than 13dB improvement on the SNDR. The proposed ADC was fabricated in 130nm CMOS technology. It achieved 85.1 dB DR, 82.6dB SNDR and 90.9dB SFDR with 32 OSR. It consumes 40uW power from 1.6V power supply which gives a 163dB Schreier Figure of Merit.

Active Noise Shaping Analog-to-Digital Data Converters

by

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APPROVED:

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Head of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Lukang Shi, Author

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DEDICATION

I will give my deepest gratitude to my family for their unconditional support and sacrifice. I would like to dedicate this dissertation to my parents, Lirui Shi and Yun'e Wang, my parents in law, Dawei Jin and Libo Zhou and my sister Luyan Shi. They gave me their endless love in my life. Finally, it is not possible to finish my study without the love from my treasured wife, Yixin Jin. It is you who always encourage and accompany me with these four years. By having you, my whole life is happiness.

1 Introduction

1.1 Motivation

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are very popular and widely used in medium to high resolution applications with a few mega-samples per seconds (Msps) speed. SAR ADCs usually have 8 to 16 bits resolution combined with different techniques and architectures, and also provide a low power consumption. Typical applications include biosensors, image sensors and lot of wearable devices, there are more and more demands in people's daily life. The ADC is a key part for these applications because sensors need to convert analog signals to digital signal to process. For most of these applications, accuracy and battery life are always of concern so that low power and high-resolution ADCs are needed. Therefore, the SAR ADC is a very good candidate. There are many techniques and architecture to improve the performance of SAR ADCs. One of them is noise-shaping (NS) SAR ADCs. It is getting more and more attentions recently because it not only has the same basic simple architecture and binary searching algorithm, but also borrowed the oversampling and noise-shaping concepts from Delta-Sigma (ΔΣ) ADCs which will give a significant improvement to the accuracy.

There are two basic ways to implement noise-shaping, which are realized by passive integrator and active integrator. For passive NS SAR ADCs, there is no active circuits in the ADC, so it is very power efficient in theory. However, one drawback is it has charge loss during the integration because of the passive integrator, therefore, the quantization noise attenuation effect is inferior compared to the same order noise shaping in an active integrator. On the other hand, in active NS SAR ADCs, there is at

least one active block, which consumes power, so they need to use some techniques to decrease power consumption. As mentioned before, active integrator can preserve all charge which results a significant noise suppression. The active NS SAR ADCs are suitable for low speed (few kHz) and high accuracy (above 14 bits) applications.

In this research, we focused on active NS SAR ADC architecture. There are novel NS SAR ADC architectures and techniques that we have developed to achieve high performance and low power consumption. A new DAC architecture and technique were developed for active NS SAR ADC. With the new DAC architecture, the total number of capacitors in DAC is reduced compared with conventional binary weighted DAC array. This is good for capacitor matching. Furthermore, a on-chip digital DAC calibration was proposed and implemented. It will reuse all circuits in the NS SAR ADC, so it will not increase circuit complexity, and is power efficient. Two prototypes were fabricated and measured, both of them achieved a high performance and appear to be a good solution for sensor applications.

1.2 Contribution of this Research

Major innovations and contribution of this research are summarized and described below:

- A first order active NS SAR ADC with 2-C DAC was proposed and implemented to achieve ideal first order noise shaping effect. The silicon result verified that this architecture and theory is correct. A relative high accuracy performance was measured. A potential second order noise shaping architecture which only needs some extra capacitors was verified by simulation.

- A NS SAR ADC with on-chip digital DAC calibration was designed and fabricated. With the DAC calibration, the ADC's performance can be improved 13dB based on the measurement results.
- A 2-C DAC was used in SAR ADC. With this 2-C DAC, the total number of capacitors and capacitance spread is reduced compared with a conventional binary weighted DAC array. Moreover, this DAC makes it is possible to remove the reference buffer which is usually required for traditional SAR ADC.
- Correlated double sampling (CDS) and correlated level shifting (CLS) techniques were combined to implemented to one chip at the same time. With these two techniques, the design specification of op-amp which is used as integrator is relaxed, so it can consume less power.
- A on-chip DAC mismatch error calibration was introduced and implemented. The calibration scheme reuses all existing circuits in the NS SAR ADC. Therefore, it is more power efficient and keeps the circuit architecture simple.

1.3 Organization

This dissertation is organized as follow: Chapter 2 illustrates the operation and design techniques of the active first order NS SAR ADC with 2-C DAC. Chapter 3 gives an improved NS SAR ADC with on-chip DAC error calibration. Chapter 4 draws the conclusion of this dissertation.

2 A 13b-ENOB 87.8dB SFDR 1st Order Noise-Shaping SAR ADC with Two-Capacitor DAC

This chapter presents an active noise shaping SAR ADC. Instead of binary-weighted capacitors array DAC, it uses two equal-valued capacitors as a digital-to-analog converter (DAC). Thus, the capacitance spread in the DAC is 1, much smaller than that of the conventional binary-weighted capacitor array, and hence the mismatch error can be greatly reduced. Furthermore, with this 2-C DAC, it will sample and hold the reference for whole conversion, therefore, it makes operation without reference buffer possible. The circuit provides first-order noise shaping, which can improve the ADC's linearity even for a small oversampling ratio (OSR). Moreover, the proposed architecture uses a monotonic switching procedure which allows fewer conversion steps than for a conventional SAR ADCs'. The ADC was fabricated in 180nm CMOS technology. For a 2kHz signal bandwidth, it achieved a 78.8 dB SNDR, 87.8 dB SFDR with 32 OSR. It consumes 74.2uW power from 1.5V power supply.

2.1 Introduction

There are more and more sensors that are used many different applications such as data acquisition instrument, biomedical and many wearable devices. Integrated sensor circuits convert the analog signal to digital for the digital processor. For these applications, low power and high accuracy are desired. Traditional SAR ADCs are widely used for medium accuracy in medium speed and low power fields shown in Fig. 2.1. The operation scheme of a SAR ADC is a binary searching algorithm to scale down the reference voltage.

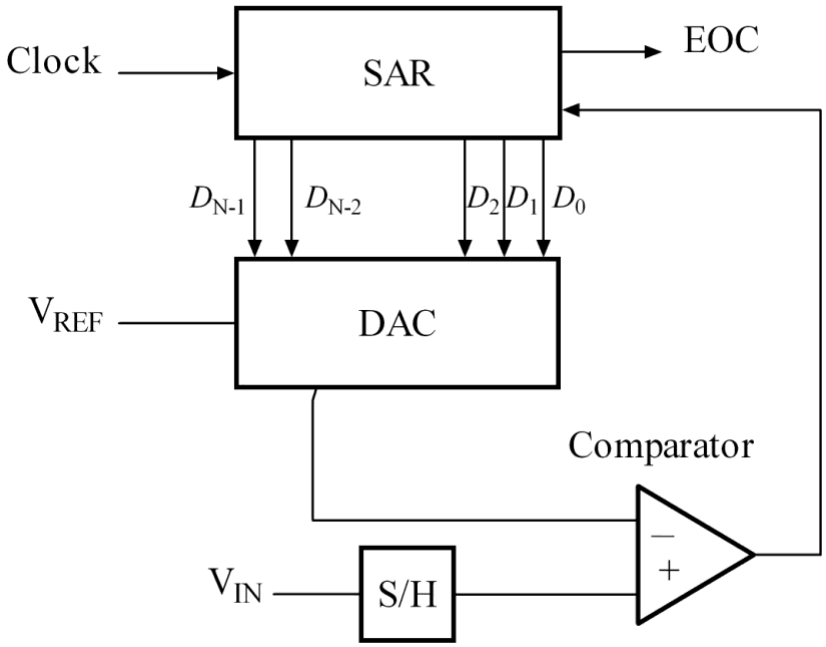


Fig. 2.1 Conceptual block diagram of SAR ADC

Figure 2.1 shows a basic SAR ADC architecture. It includes a sample & hold circuit, comparator, DAC and digital control circuits. The SAR ADC is very power efficient. The sample and hold circuit is usually integrated to the DAC. As mentioned before, a binary weighted capacitor array is used as DAC shown in Fig. 2.2.

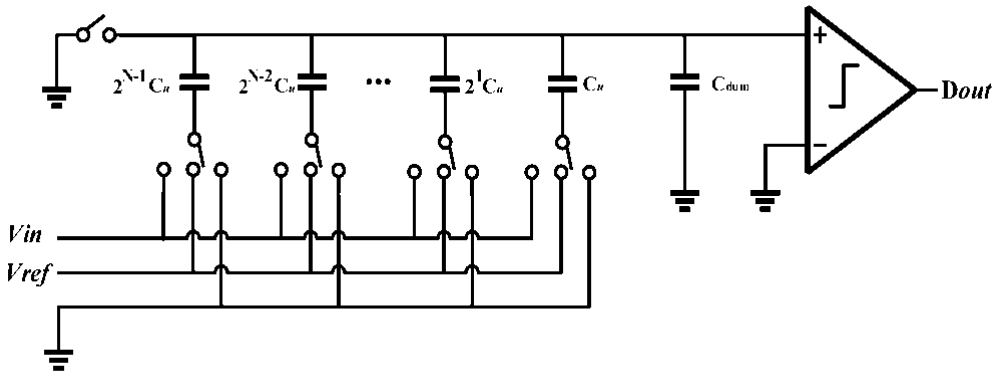


Fig. 2.2 SAR ADC with binary weighted DAC

The main drawback of binary weighted DAC is the area and power consumption. For example, a 10-bit SAR ADC, the total DAC capacitance is $2^{10} \cdot C_{unit}$ where C_{unit} is the unit capacitor. With a 10fF unit capacitor size, it needs a 1 pF total capacitance. However, with this so small unit size, the matching between the capacitor will be a challenge. Moreover, the capacitance spread from least significant bit (LSB) to most significant bit (MSB) is very large. In order to solve this problem, a binary weighted capacitive array with attenuation (BWA) DAC was proposed in [1]. Since this attenuation capacitor (called bridge cap), the DAC is split by two parts for a N-bit resolution SAR ADC: a k MSBs DAC and an m=N-k LSBs DAC. Hence, the total capacitance compared with conventional binary weighted DAC is reduced by 2^m [2].

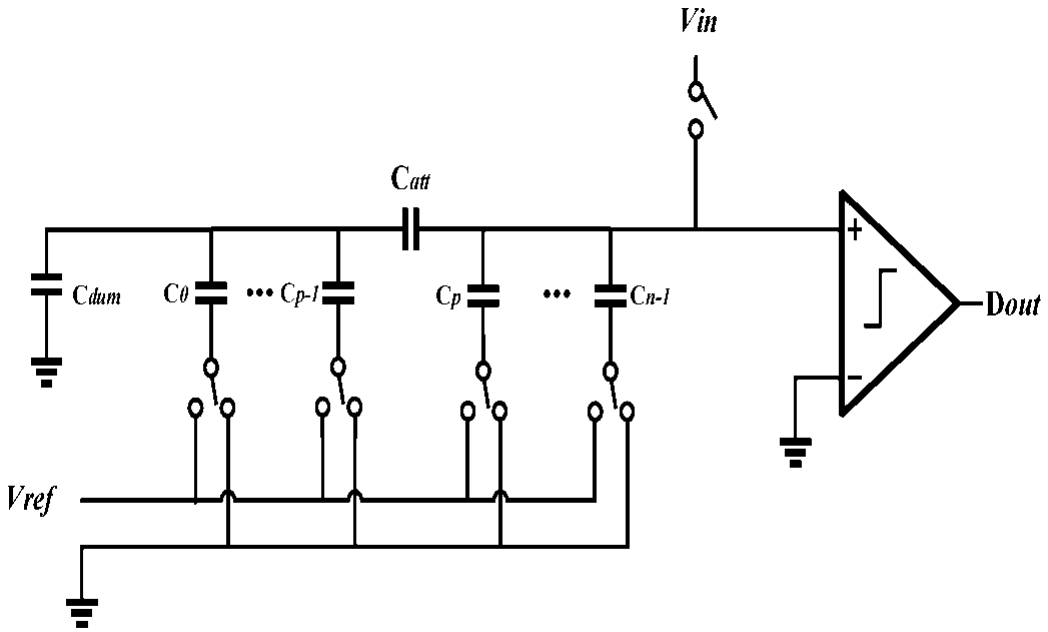


Fig. 2.3 SAR ADC with binary weighted DAC w/ attenuation cap

For high accuracy, the performance of a conventional SAR ADC suffers thermal noise, mismatch errors from the DAC, and comparator noise. Therefore, some techniques need to be introduced to overcome these problems. Oversampling and noise-shaping can be used in a SAR ADC, called noise-shaping SAR ADC.

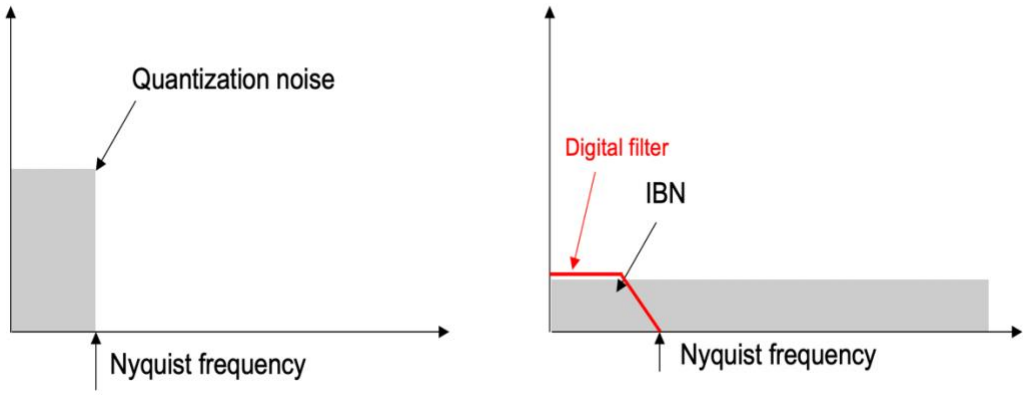


Fig. 2.4 Noise reduction with oversampling

The quantization noise in ADC can be treated as a wide-band noise, similar to the kT/C thermal noise from DAC. After oversampling, the whole noise will be distributed up to fs/2. Therefore, the in-band noise is decreased. Suppose the oversampling ratio (OSR) is N, then the in-band noise will be reduced by N. The signal to noise ratio (SNR) becomes:

$$SNR = 6.02 \cdot N + 1.76 + 10 \cdot \log(OSR) \quad (2.1)$$

Equation 2.1 shows the SNR will be increased 3 dB by double OSR. Therefore, with oversampling, the total capacitance of DAC is also can be reduced based on the design requirement.

Moreover, the noise-shaping technique can improve the ADC performance further. Figure 2.5 shows the concept of noise shaping. It creates a high pass loop filter by using

an integrator to shape the noise to high frequency, and then filter the noise out, and hence SNR is improved.

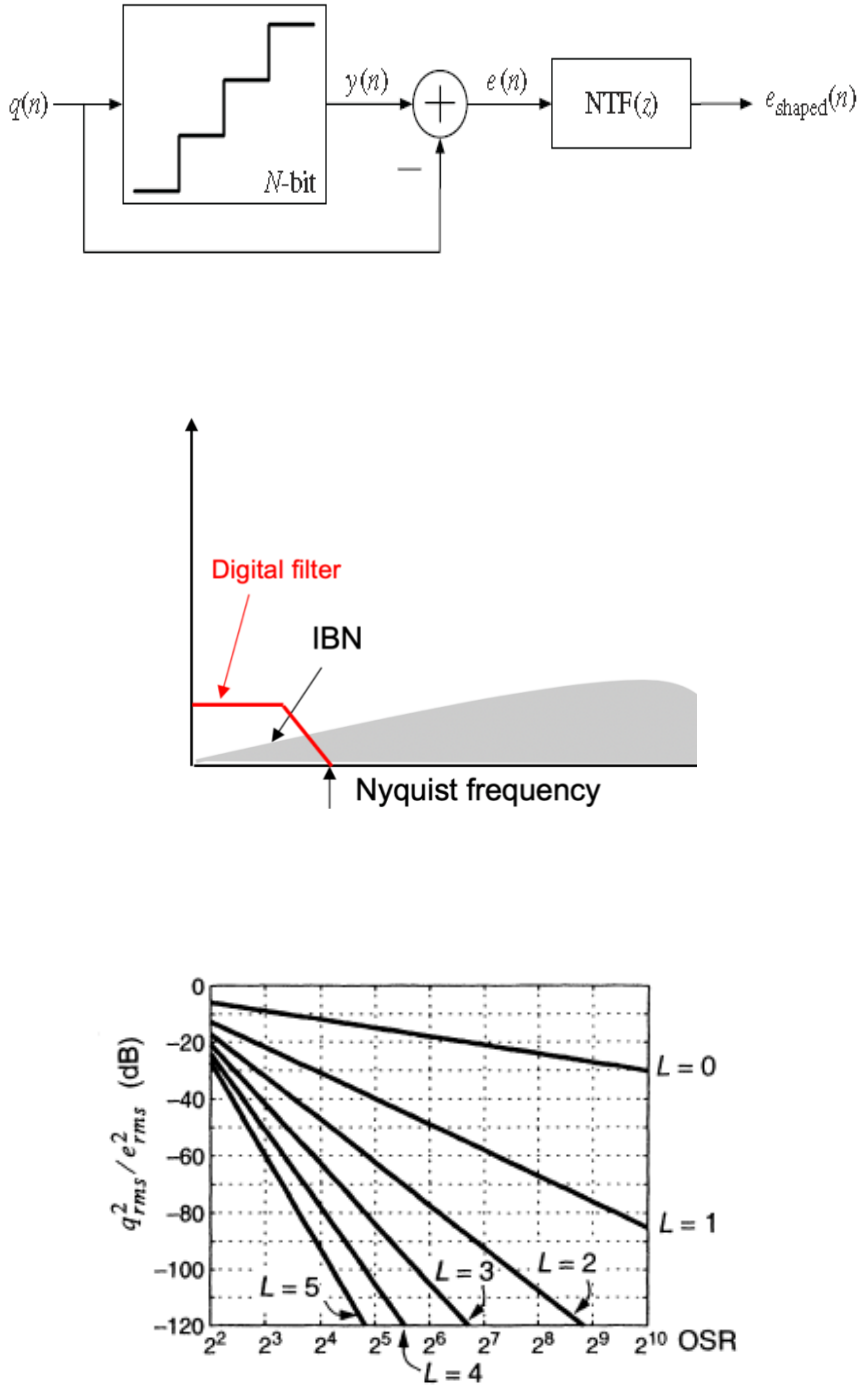


Fig. 2.5 (a) Concept of noise-shaping, (b) noise distribution with noise shaping, (c) noise attenuation versus OSR and order of noise shaping

Using these two schemes, recently some NS SAR ADCs have been proposed. These circuits achieved a relative high performance, but they used the conventional binary-weighted capacitor DAC array or split capacitor DAC. For both DAC types, they have large capacitance spread and hence mismatch issues. Moreover, several calibration methods were proposed to solve this problem, but these methods need extra circuitry, which increases the power consumption and circuit complexity. Furthermore, in a binary-weighted DAC the reference needs to present during the whole conversion process, which requires the DAC to settle to the desired accuracy in a limited time. This increases the reference buffer requirements.

This chapter presents a first order NS SAR ADC with a two-capacitor (2-C) DAC. The 2-C DAC minimizes the capacitance spread, and hence is good for matching. Furthermore, it relaxed the reference buffer design requirement. The reminder of this chapter discusses the details of this ADC.

2.2 Architecture

2.2.1 Overview of NS SAR ADC

Obtaining the residue error is the key step to achieve noise shaping. In a conventional binary weighted DAC array, the residue error information will be left in the DAC after the conversion is finished. Therefore, if this error can be stored and fed back in the next conversion cycle, then the whole system will perform a high filtering on the quantization noise. Typically, there are two ways to implement noise shaping in a SAR ADCs. One is using passive integrator and another one is realized by an active integrator. Figure 2.6 shows a first order NS SAR ADC in the passive method [3].

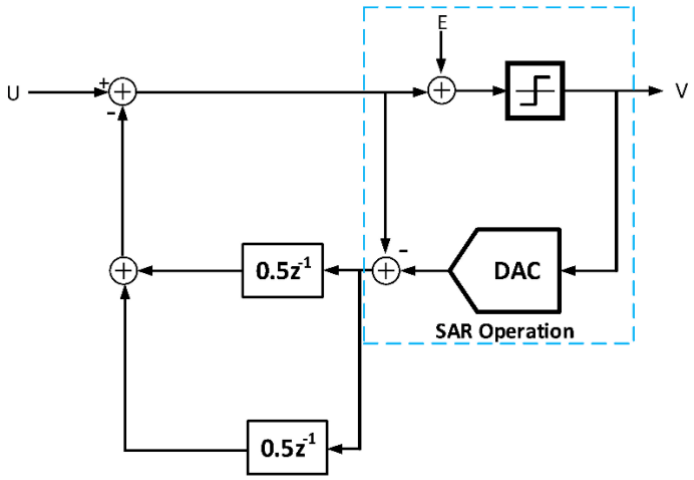


Fig. 2.6 First order NS SAR in fully passive [3]

As mentioned above, the quantization error is left in the DAC after one full conversion is done. It uses another capacitor to do charge redistribution with the DAC, therefore, the error information can be stored in this capacitor and it will be fed to the input of the comparator so that noise shaping is achieved. Since it is a fully passive circuit, its power dissipation is low. The noise transfer function (NTF) of it is $1-0.5z^{-1}$. Compared with an idea first order noise shaping NTF $1-z^{-1}$, the NTF in [3] only can achieve part of noise attenuation which because the passive integrator has charge loss during integration.

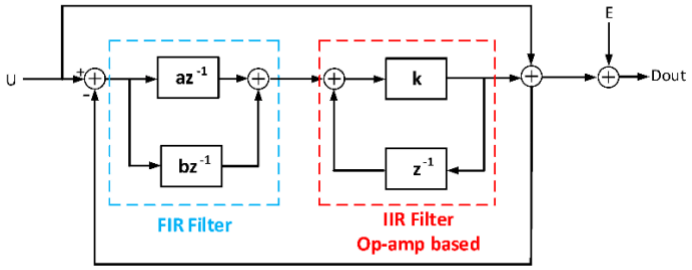


Fig. 2.7 Signal flow diagram of NS SAR with active integrator [4]

Figure 2.7 shows the concept of a conventional active NS SAR ADC [4]. It is implemented with a finite impulse response (FIR) filter and an infinite impulse response (IIR) filter which both of them are built on an op-amp. With the help of the FIR and IIR filters, the NTF is enhanced to $1-0.64z^{-1}$.

In both [3] and [4], they don't achieve an ideal first order noise shaping NTF. Moreover, both of them are implemented with conventional binary weighted DAC which results large capacitance spread.

2.2.2 Proposed Active NS SAR ADC with Two-Capacitor DAC

To obtain ideal NTF with active integrator and reduce the capacitance spread, a first order NS SAR with two-capacitor (2-C) DAC was proposed [5]. It is shown in Fig. 2.8. The circuit includes a 2-C DAC (C_1 and C_2), a fully differential op-amp used as an integrator with feedback capacitor C_3, a comparator and SAR logic control circuitry. Capacitors C_1, C_2 and C_3 have equal values. C_2 performs the sampling, so the circuit does not need an extra sample and hold stage. The residue error is stored in C_3. The details of the operation will be explained next.

C_1 is initially charged to reference voltage, and then it is disconnected from the reference during the conversion, so it will not introduce settling issues with the reference or reference buffer. The DAC consists of two equal-valued capacitors; therefore, the capacitance spread is much smaller than in a binary-weighted capacitor DAC array. From kT/C noise considerations, the total value of capacitors in the 2-C DAC is same as in a binary-weighted DAC array. However, the unit capacitor size in a binary-weighted DAC usually is dictated by mismatch error limits, which will increase

the total area. For the 2-C DAC, the two capacitors determine the kT/C noise, and will hence be large enough for excellent matching.

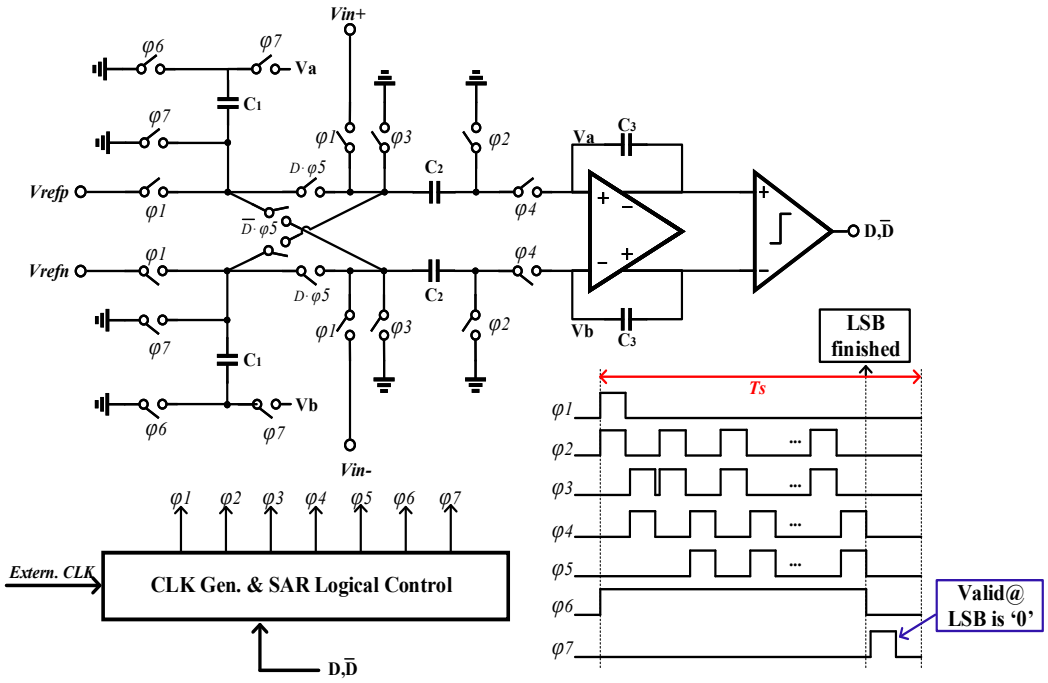
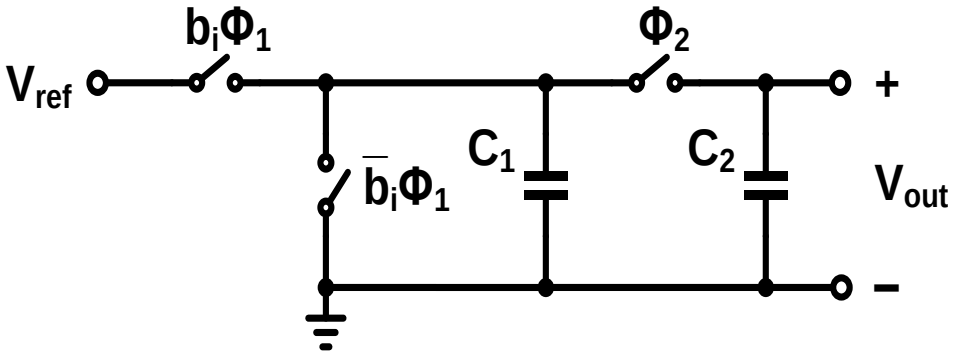
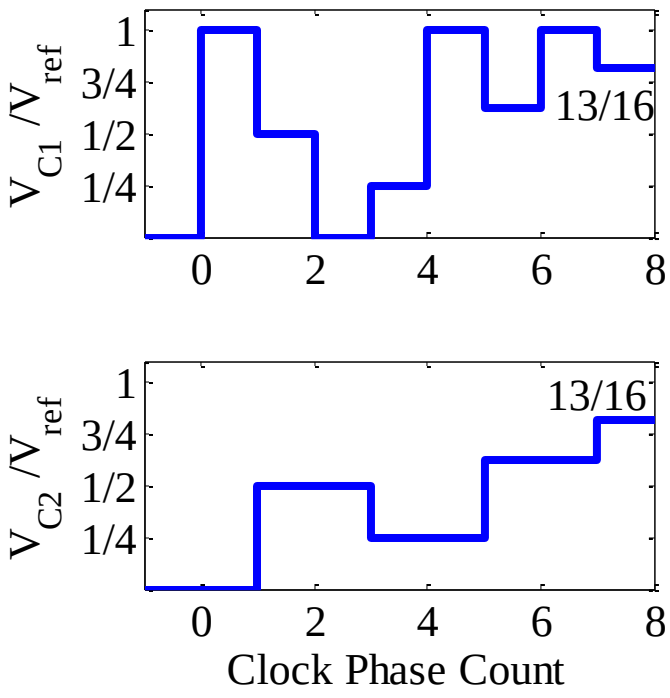


Fig. 2.8 Proposed NS SAR ADC architecture and operation timing

Figure 2.9 (a) shows a simplified 2-C DAC and (b) gives a 4-bit 2-C DAC operation example to explain how the 2-C DAC works.



(a)



(b)

Fig. 2.9 (a) Simplified 2-C DAC (b) 4-bit 2-C DAC operation

Suppose the input digital codes are $X(n) = 1,0,1,1$. Phase 1 and phase 2 are two non-overlapping clock phases. Based on the input codes, capacitor C_1 and C_2 will do charge sharing between them. Their value is equal to each other. Moreover, the input is in serial. The LSB will be fed in firstly and the MSB is last. The output voltage of the 2-C DAC is following the equation as below:

$$V_{out} = V_{ref} \cdot \sum_{i=1}^{N} b_i 2^{-i} \tag{2.2}$$

where N is the total number of bits of the DAC, and i is the ith bit of the conversion. Since the DAC only has two capacitors and serial input workflow, the operation is simple.

The proposed ADC was designed as a 10-bit conversion clock cycles and the OSR is 32. With a 2kHz signal bandwidth, the sampling frequency is 128kHz ($\varphi 1$). Therefore, the internal conversion clock frequency is 1.28MHz ($\varphi 2$). The clock logics were designed as synchronous clock to keep low complexity of the circuit. Both of analog and digital circuits operate with a 1.5V power supply. There are mainly three steps for the whole operation: sampling, conversion and noise shaping realization. They are the following:

Sampling: $\varphi 1$ and $\varphi 2$ go high to sample the input voltage V_{in} across C_2. At the same time $\varphi 6$ goes to high, so that C_1 is charged to reference voltage V_{ref} which is equal to $V_{refp} - V_{refn}$. Next, $\varphi 1$ and $\varphi 2$ turn low, and $\varphi 3$ and $\varphi 4$ go high, so the sampled input voltage and reference voltage are stored and held in C_3 and C_1 respectively. Figure 2.10 (a) shows the configuration of sampling step.

Conversion: $\varphi 3$ stays high, $\varphi 4$ goes to low and $\varphi 2$ goes to high to discharge C_2. At the same time, the MSB is determined, and $\varphi 2$ and $\varphi 3$ turn low, while $\varphi 4$ goes high. If the output of comparator is '1', phase $D \cdot \varphi 5$ will go high, and a charge $C \cdot V_{ref}/2$ will enter C_3. Therefore, the new output voltage of integrator is $V_{in} - V_{ref}/2$. If the output of comparator is '0', then phase $\overline{D} \cdot \varphi 5$ will go high so that the output voltage of the integrator is $V_{in} + V_{ref}/2$. The circuit will repeat these steps until the LSB conversion is finished. During this step, the reference is disconnected from the whole circuits shown in Fig. 2.10 (b). Therefore, it does not need a reference buffer to help the DAC settle to desired accuracy in a limited time. This not only avoids the limitation of the buffer accuracy, but also minimized the power consumption. Furthermore, unlike

in the switching scheme in [6], the proposed switching scheme is monotonic, so it is more power efficient.

Noise Shaping: Considering step 2, it does not need remove the charge from the output of the integrator if the decision of the comparator is '0'. This is the reason why it allows a monotonic switching for the proposed ADC. Therefore, after step 2, the converter can immediately begin to carry out the next conversion cycle without resetting C_3 because the whole residue error already observed in it. Therefore, an ideal first order noise shaping NTF can be achieved. However, if the last bit of the conversion is '0', it will give an incorrect residue error in the integrator due to the monotonic switching scheme. As a simple example, for a single bit proposed SAR ADC, after the conversion is finished, the voltage at the output of integrator is:

$$V_{out} = V_{in} - \frac{1}{2}V_{ref} \tag{2.2}$$

If the digital output of the comparator is '1', then the residue error is equal to the V_{out} which is correct. However, if the decision of the comparator is '0', the correct residue should be:

$$V_{res} = V_{in} - V_{dout} = V_{in} \tag{2.3}$$

where V_{dout} is the equivalent analog value based on the digital output code. In this case, the output voltage of the integrator, shown in equation (2), does not represent the correct residue error. Compared with equation (2) and (3), it shows a $V_{ref}/2$ difference, so in order to restore the correct residue error, it need add this voltage back to the output of the integrator for a single bit proposed ADC. The analysis can be extended to a n bit proposed SAR ADC. For a n bit converter, the output voltage of integrator is:

$$V_{out} = V_{in} \pm \frac{1}{2}V_{ref} \pm \frac{1}{2^2}V_{ref} \pm \cdots \pm \frac{1}{2^n}V_{ref} \quad (2.4)$$

Therefore, when the last digital bit is '0', the correct residue value will be:

$$V_{res} = V_{out} + \frac{1}{2^n}V_{ref} \quad (2.5)$$

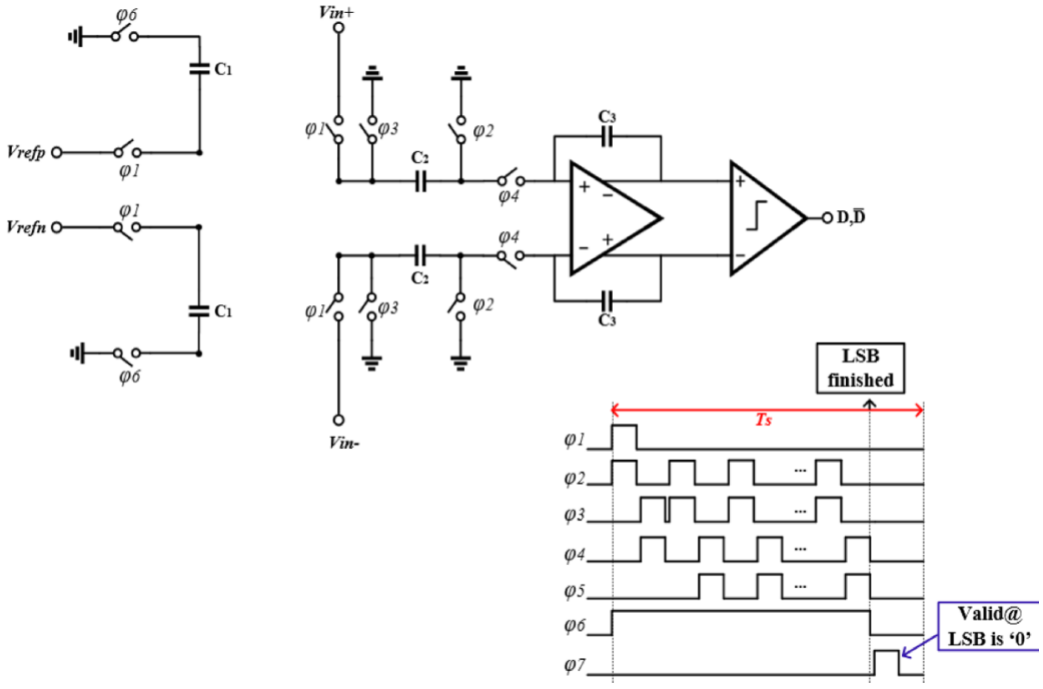
According above equations, if the last digital bit is '0', an LSB equivalent voltage needs to be added to the output of the integrator before the next sampling is started. Hence, how to generate and add this LSB is the extra step for this proposed SAR ADC.

The following shows how to generate this LSB. After the last bit is obtained from the conversion, the voltage left across C_1 is

$$V_{c1} = V_{ref} - \frac{1}{2}V_{ref} - \frac{1}{2^2}V_{ref} - \cdots - \frac{1}{2^{n-1}}V_{ref} = \frac{1}{2^n}V_{ref} = 1LSB \quad (2.6)$$

Then a test phase will go high to check if the last bit is '0' or '1', if it is '0', then $\varphi 6$ goes to low and $\varphi 7$ goes to high. As a result, this LSB voltage will be added back to the output of the integrator, and the correct residue voltage will be stored at the output of the integrator. This residue correction scheme only needs add a few extra switches to the whole circuits, so it will not increase the complexity and power consumption of the entire SAR ADC.

There is another potential advantage of the proposed NS SAR ADC is it can be extended to higher order noise-shaping by reusing the existing integrator. For example, for a second order noise-shaping implementation, the basic idea is to add some extra capacitors and switches at the output of integrator. Hence, it can use these extra capacitors to copy the residue error E(n-1) and hold it for one more conversion clock period, and then the residue error on C_3 becomes E(n-2) which results to a NTF as $(1 - z^{-1})^{-2}$.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C1
Vrefp
φ1
φ1
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C1
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φ1
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D,D̄
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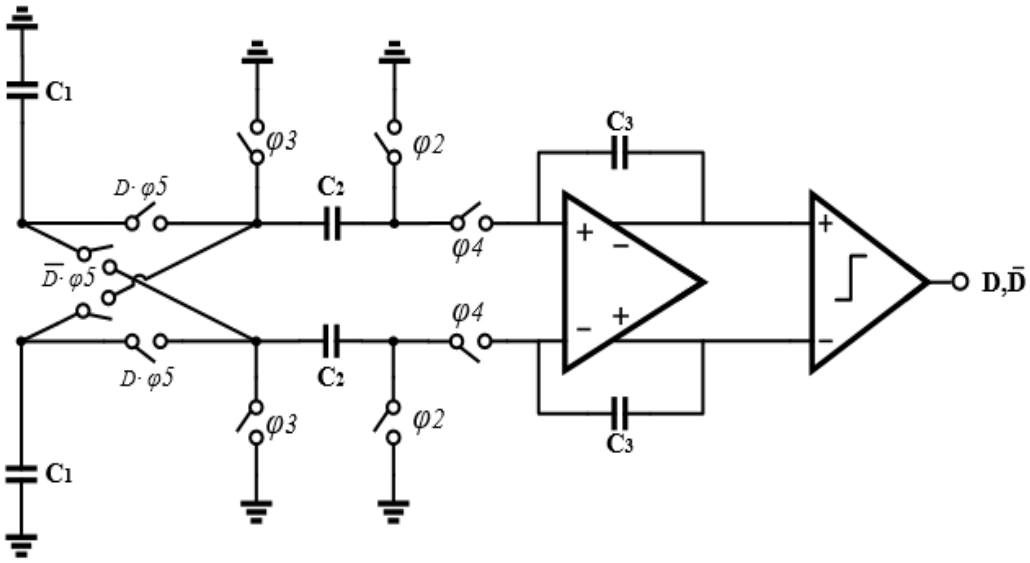
(a)


C1
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D̄·φ5
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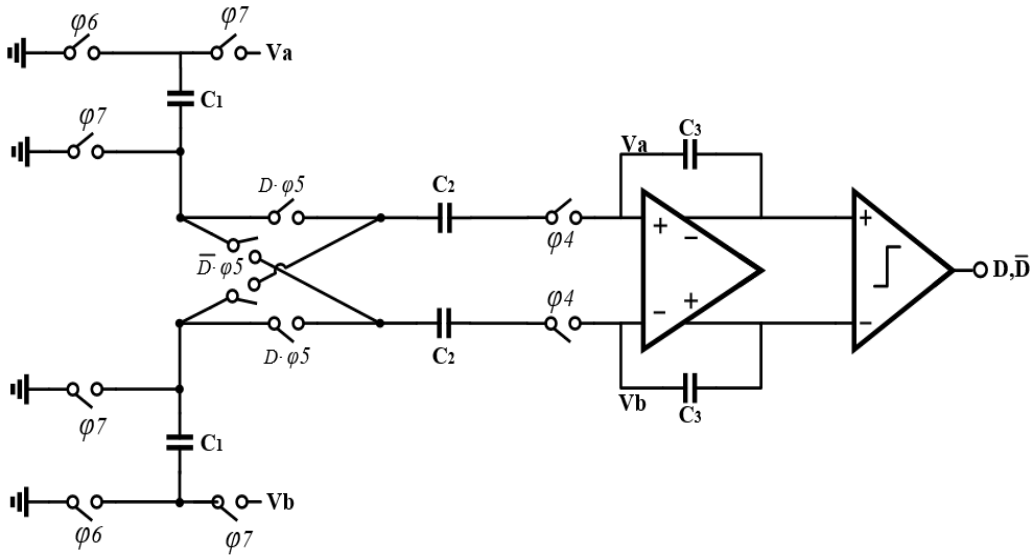
C2
φ3
φ2
C3
C1
D,D̄

(b)



(c)

Fig. 2.10 Conversion configuration for each step of the proposed ADC (a) sampling, (b) conversion, (c) noise-shaping

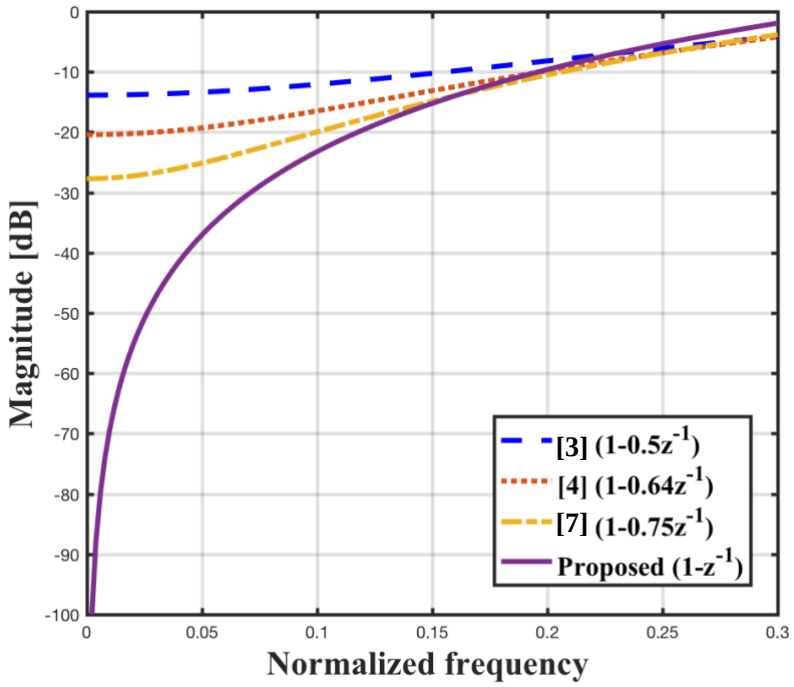


Fig. 2.11 Comparison of noise transfer functions

The signal transfer function (STF) is 1 and NTF is $1-z^{-1}$. The proposed converter achieves an ideal first order noise shaping. This is the advantage of active integrator which has a better in-band noise attenuation performance. Figure 2.11 shows the NTF comparison with the same order noise shaping effect under passive integrator. In [7], it enhanced the NTF in passive integrator with multiple input comparator, but it still can not achieve the ideal first order noise shaping. Besides, it used a multiple inputs comparator, so the design of comparator becomes more complicated and need care about the stability issue. With the good in-band quantization noise attenuation in the proposed circuit, it will have more noise margin for other noise such as kT/C thermal noise of DAC during design.

2.3 Circuits Implementation

2.3.1 Integrator Op-amp

For the proposed ADC, there is only one op-amp used as integrator and it may need process a very large range signal amplitude because it need hold the input signal and references which may go as high as power supply voltage. Therefore, it requires the op-amp with a large output swing. Moreover, in order to suppress the nonlinearity of itself and keep an accuracy charge transfer during the conversion, a high DC gain is desired.

Figure 2.12 shows the simulated finite DC gain effects on the SNDR. In order to achieve above 80 dB SNDR, a at least 70 dB DC gain is required. However, in real circuit implementation, the circuits may have unexpected nonlinearity, so to give enough design margin, 85 dB DC gain is designed in the proposed circuits. Based on above two factors, a two-stage op-amp architecture was selected shown in figure 2.13.

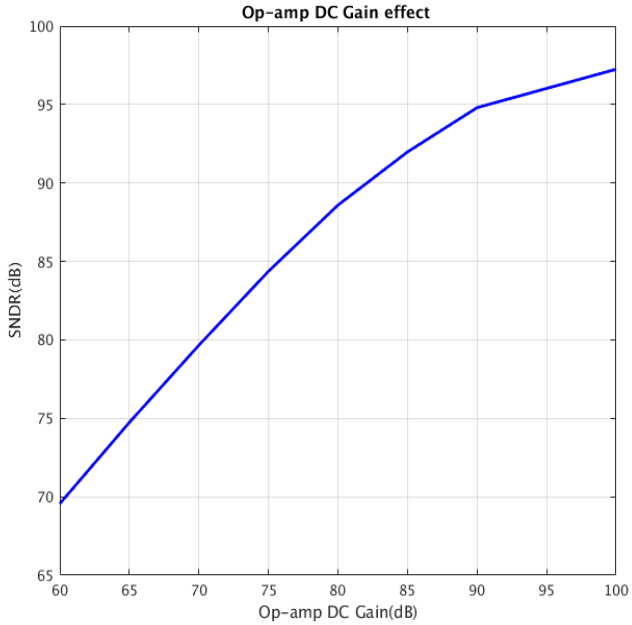


Fig. 2.12 Simulated SNDR versus op-amp DC gain

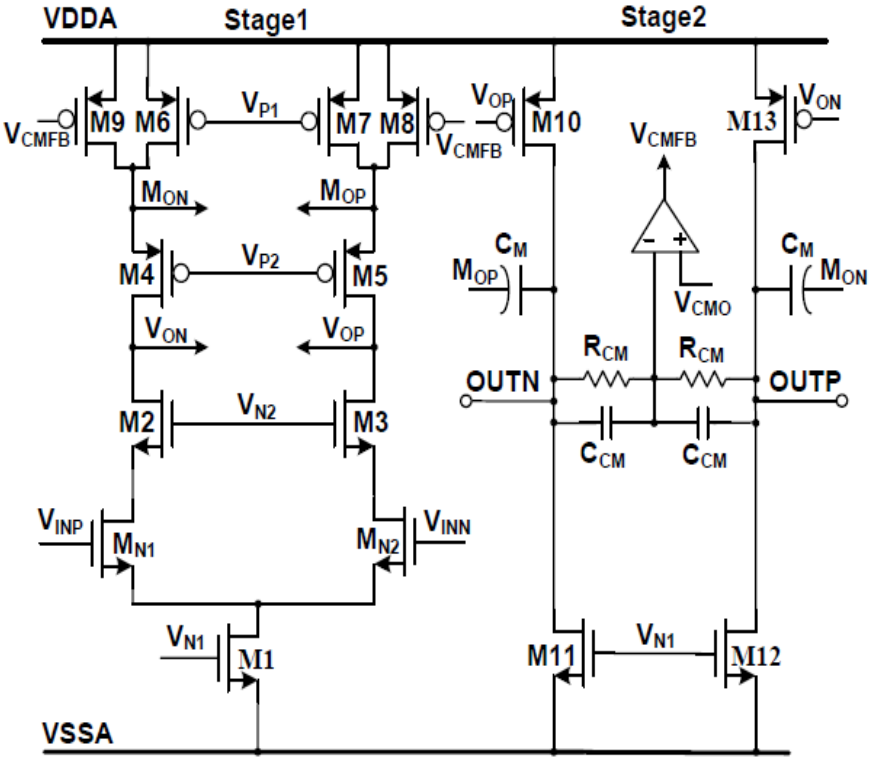


Fig. 2.13 Architecture of the op-amp used as integrator

The first stage of the op-amp is telescopic topology which can achieve a relative high gain. The second stage is a simple common source architecture which will give a large output swing. Since it is a two-stage architecture, a Miller compensation [8] technique was introduced to stabilize the op-amp. The internal conversion clock frequency is 1.28 MHz, a 10 times unit gain bandwidth (UGBW) is required for the design based on [9]. Hence, a 15 MHz UGBW was designed for this op-amp. It is a fully differential amplifier, so a continuous time based common-mode feedback (CMFB) circuit is used to control the output common-mode voltage. It used an RC network to sense the output common mode voltage, and then fed into an error amplifier to regulate the common mode voltage at the output. The op-amp operated under 1.5V power supply and draw a 40 uA total current. Another potential candidate architecture for the op-amp is to use a dynamic op-amp which likes in [10].

2.3.2 Comparator

There are mainly two types of comparators. One is static latch; another is dynamic latch. For the static latch, the core circuit is usually a static complementary latch [11]. It includes two cross coupled inverters with a positive feedback. On the other hand, the dynamic comparator uses a clock signal to control the regenerative latch in the comparator [12]. The drawback of static latch is that it is slow compared to the dynamic architecture comparator. Hence, a dynamic based architecture comparator was selected for this design.

The designed comparator includes two parts. First stage is a preamplifier which has a 40 dB DC gain with 1 uA current. The following stage is a regenerating latch with a RS latch. The schematic of the comparator is shown in Fig. 2.14.

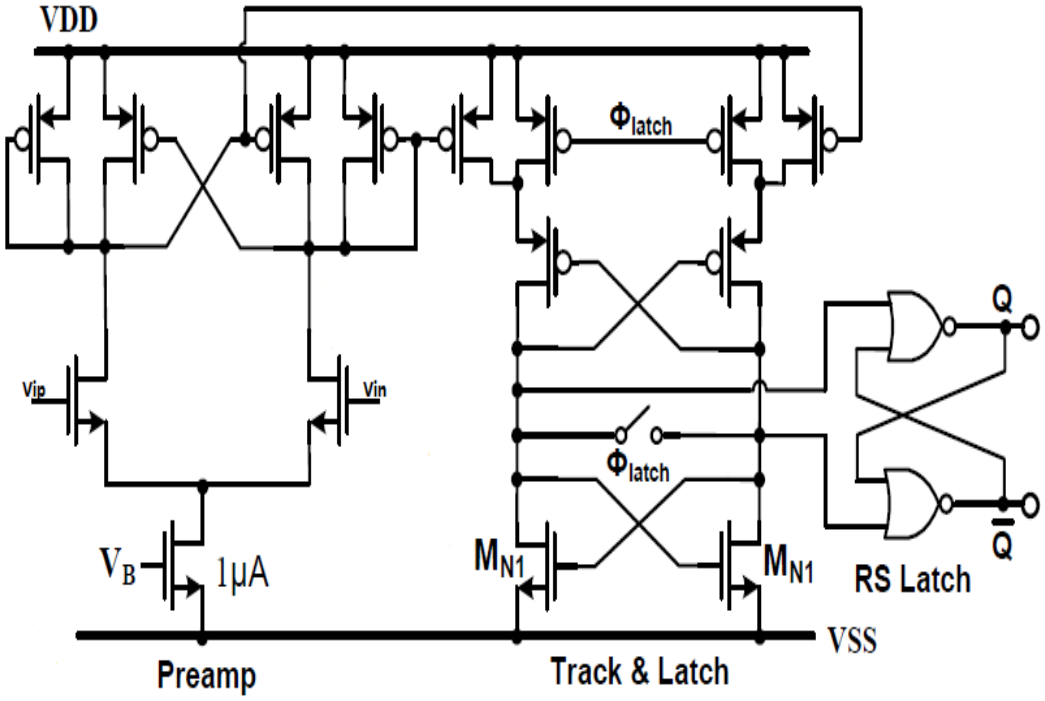


Fig. 2.14 Dynamic comparator used in proposed ADC

This comparator is connected to the integrator's output directly, and this output voltage will get smaller and smaller during MSB to LSB conversion. Therefore, a pre-amplifier can help to amplifier these small signals so that the latch stage can make a correct decision. Besides, the clocked latch stage will produce kick back noise and will fed back to the input of the latch through the parasitic cap. If there is no preamplifier, this noise will directly couple to the integrator which will cause distortion if the integrator doesn't have enough time to settle to original value before next conversion. With this preamplifier, the kick back noise can be absorbed by it and hence reduce the coupling to the integrator's output. An auto-zeroing technique [13] was used to the preamplifier to decrease the DC offset and input referred noise specifically is flicker noise.

The preamplifier is realized by a negative transconductance [14] and diode connected load to achieve a high gain. One thing needs to be addressed is it need carefully scale the transistor's size in the preamplifier to avoid a positive feedback loop which will cause latch up.

2.3.3 Switches and Capacitor Size

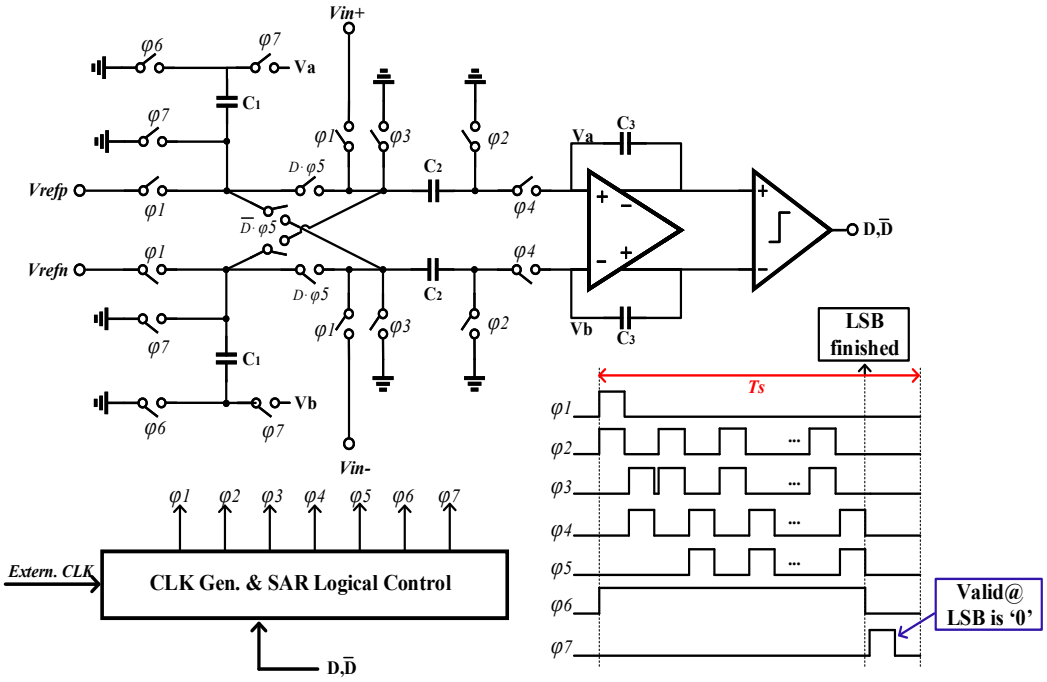


Fig. 2.15 Switches and capacitor implementation

The most important switches are the input sampling switches connected to Vin+ and Vin-. For a single CMOS switch, the turn-on resistance is changed with the input voltage because the gate-source voltage Vgs is changing. If it is used to do the sampling, this nonlinearity will be sampled into the whole system, and hence distortion is introduced. In order to keep the sampling linearity, bootstrapped NMOS switches [15] were used to sample the input signal. Figure 2.16 shows a conceptual diagram of the bootstrapped switch circuit. The idea is to connect the gate of NMOS to the input

through a fixed DC voltage source. For example, suppose this DC voltage source is 1V, the voltage between gate and source of the NMOS is always 1V which gives a fixed turn on resistance in theory. In real circuit, since the turn-on resistance is not only controlled by Vgs, there will be some degradation of the linearity of the switch, but it is still can satisfy the design requirement which is about 80 dB SNDR.

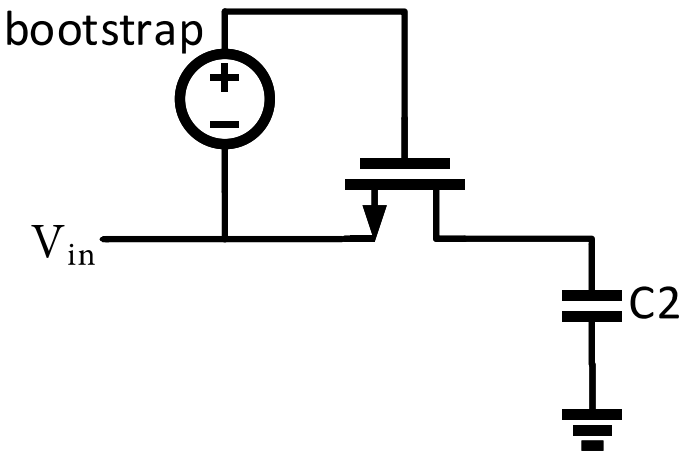


Fig. 2.16 Simplified bootstrapped switch

For this design, because the power supply is 1.5 V, the Vgs of bootstrapped CMOS switch is selected to this voltage. The input signal range is 0 to 1.3 V, so the highest voltage of Vgs is about 2.8 V which is still safe for the transistor. Figure 2.17 shows the schematic of the designed bootstrapped switch. The capacitor C_2 is acted as the DC voltage source which will be charge to the supply voltage. The size of it is 0.5 pF. The simulation shows this switch has a 100dB linearity. For the switch which is connected to the positive reference side V_{refp} is designed with a high threshold voltage PMOS device to reduce the leakage.

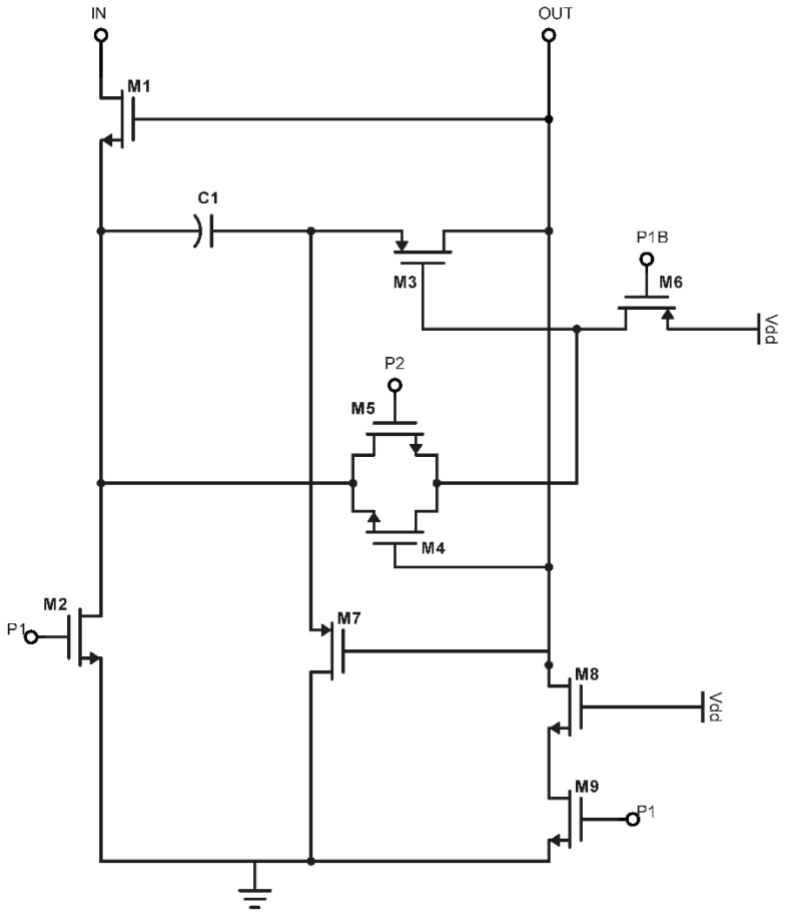


Fig. 2.17 Schematic of bootstrapped circuit

Other switches' sizes are designed to satisfy the settling speed requirement and at the same time keep small size to reduce the parasitics.

Capacitor C_1 and C_2 are selected 4 pF to meet the kT/C thermal noise requirement. Considering the size of C_3, if its value is larger than C_1 and C_2, the output range of integrator will become smaller which is good for relaxing the output swing of the op-amp design. However, it also attenuated the effective input signal value which will decrease the SNR, so to keep low noise, C_3 is also 4 pF. The matching between C_1 (C_2)

and C_3 is not important, but it is important between C_1 and C_2 because they are in the DAC.

2.4 Measurement Results

The prototype NS SAR ADC with 2-C DAC was fabricated in 0.18 um CMOS process. Its die microphotograph is shown in Fig. 2.18. It is packaged with a 48-pin with QFP. The active area of it is 0.25 mm^2. Capacitors and digital logic control circuits occupied most of the area. For the digital circuits, it can be well scaled down with advanced CMOS technology. The chip was clocked by 2.56 MHz externally and all other clocks are generated on-chip. The power supply is 1.5 V, and a 0.75 V common-mode voltage was used.

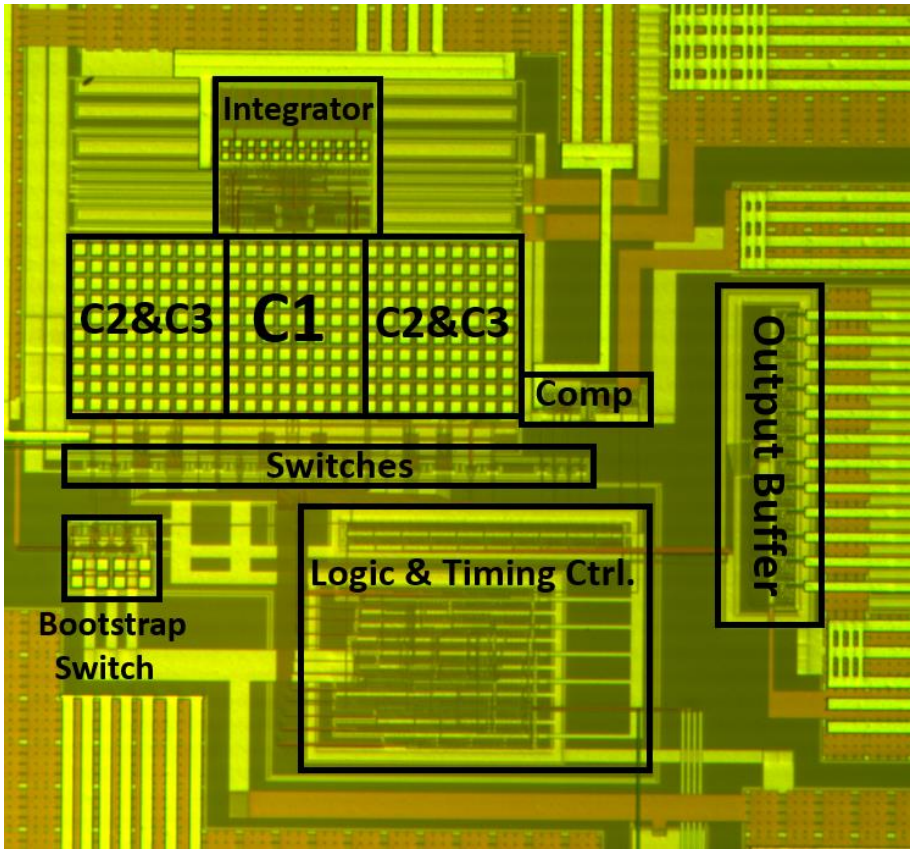


Fig. 2.18 Die photo of proposed NS SAR ADC

The differential input signal tone was produced by an Audio Precision Sys-555 instrument and sent to the chip directly without filter and buffer. Figure 2.19 shows the measured power spectral density (PSD). The input frequency is 690 Hz with -2.3dBFS amplitude. It shows the proposed ADC achieved a 78.8 dB SNDR and 87.6 dB SFDR within 2kHz signal bandwidth and 32 OSR. The performance is lower than the design requirements because of the DC offset of the op-amp. This issue was addressed and solved in the next test chip. Figure 2.20 (a) shows the performance with different input frequency, and figure 2.20 (b) shows the SNDR with different input amplitude. The total power consumption is 74.2 uW of which the analog circuits (integrator, preamp) consumed 60 uW, and the digital clock and logic control circuits consumed 14.2 uW.

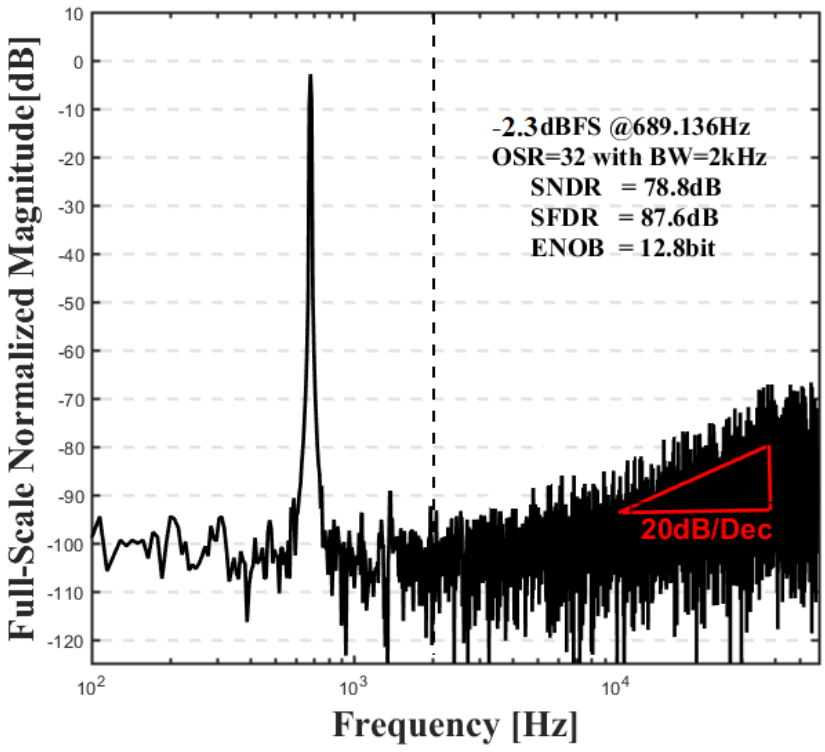


Fig. 2.19 Measured PSD

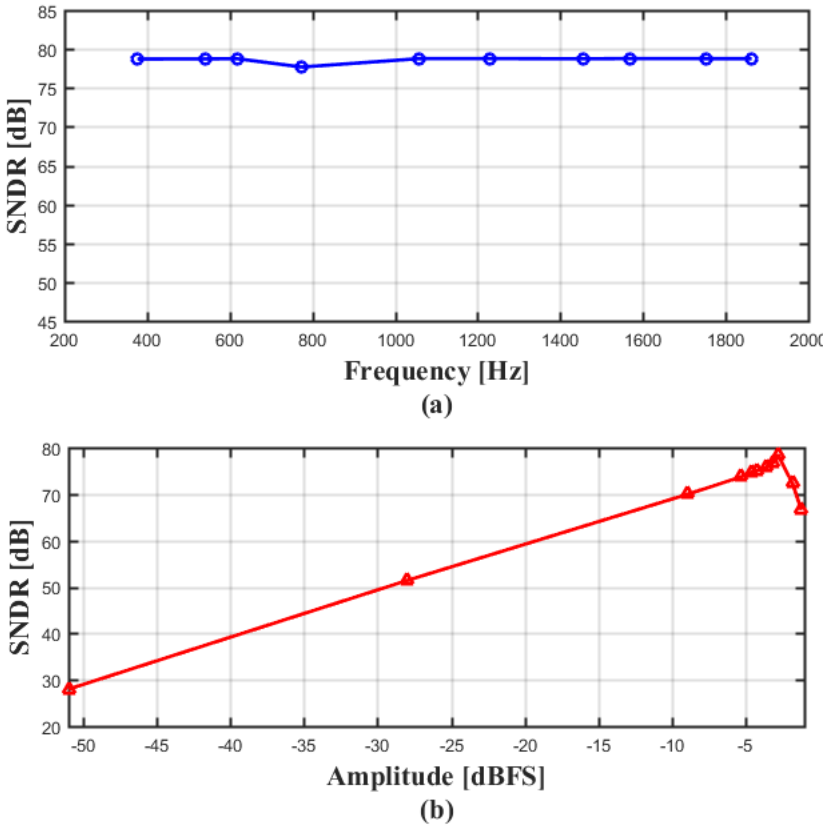


Fig. 2.20 (a) SNDR versus input frequency, (b) SNDR versus input amplitude

The converter achieved a 153.1 dB Schreier Figure of Merit (FoM_S). This value is lower than the state-of-art. One reason is mentioned above which is DC offset of the op-amp. Another reason is that the op-amp was designed for a very high DC gain which consumes most of the power of chip. Both of these two limitations from op-amp will be discussed in the next chapter, along with techniques used to eliminate these limitations.

Table 2.1 summarizes the measured performance and compares it with other previous works. The FoM_S was calculated as:

$$FoM_s = SNDR + 10 \cdot log \frac{BW}{Power} \tag{2.7}$$

Parameter	This Work	ISSCC 12, [4]	RFIT12, [16]	JSSC 02, [17]
Architecture	**NS-SAR**	NS-SAR	SAR	SD
Technology (nm)	**180**	65	180	180
Supply (V)	**1.5**	1.2	1.8	0.7
Area (mm)	**0.25**	0.03	0.24	0.082
Fs (kHz)	**128**	90e3	1e3	1024
Bandwidth (kHz)	**2**	11e3	500	8
Power (uW)	**74.2**	806	131	80
SNDR (dB)	**78.8**	62	58.9	67.0
SFDR (dB)	**87.6**	72	70	-
FoMs1* (dB)	**153.1**	163.5	154.7	149

**FoMs2 = SNDR+10log(BW/Power);

Table 2.1 Performance summaries and comparison with other works

2.5 Summary

A first-order active NS SAR ADC with 2-C DAC was proposed for bio-sensor interface. The 2-C DAC reduces the capacitance spread compared with conventional binary weighted DAC array and is good for matching. Moreover, it relaxes the reference buffer and save power. An ideal first-order noise shaping NTF was achieved by using an active integrator. The ADC was fabricated in 180nm CMOS technology. The prototype occupies 0.25mm2. For a 2kHz signal bandwidth, it achieved 78.9dB SNDR and 87.6dB SFDR with a 32-oversampling ratio (OSR). It consumes 74.2 uW power from an 1.5V power supply.

3 Noise-Shaping SAR ADC with 2-C Digitally Calibrated DAC

A NS SAR ADC with on-chip digital calibration is presented in this chapter. The main challenge in active NS SAR ADC is the power consumption of the op-amp used as integrator. For high linearity of ADC, it usually needs a very high-performance integrator to suppress nonlinearity in the circuit. This is similar to the first integrator design in a high order Delta-Sigma modulator. Therefore, to relax the design of the single op-amp used as an integrator, correlated double sampling (CDS) and correlated level shifting (CLS) were implemented. CDS minimizes the offset of the integrator and reduces the flicker noise, while CLS boosts the gain of the op-amp and reduces the power consumption. Also, a two-step incremental ADC based digital DAC calibration scheme was implemented to cancel the DAC mismatch errors and parasitics effects. The ADC was fabricated in 0.13um CMOS technology. It achieved 85.1 dB DR, 82.6 dB SNDR and 90.9 dB SFDR within a 2 kHz signal bandwidth with 32 oversampling ratio (OSR). It consumes 40.8 uW power using a 1.6 V power supply.

3.1 Introduction

The NS SAR ADC of [5] used a 2-C DAC with active integrator to achieve an ideal first order noise shaping NTF. It reduced the capacitance spread in the DAC and relaxed the design requirement of reference buffer. However, the op-amp used as integrator has a very high power consumption and its DC offset will introduce distortion into the system. Moreover, the parasitics in 2-C DAC will also degrade the linearity of the ADC.

This chapter presents a new version of NS SAR ADC with 2-C DAC. Compared to [5], it was implemented with correlated double sampling (CDS) [13] and correlated level shifting (CLS) [18] to relax the design requirements of the op-amp. Furthermore,

an incremental ADC based digital DAC calibration scheme was implemented to cancel the DAC mismatch and parasitics errors. For CDS and CLS, there are only two extra capacitors and few switches added, so it will not increase the circuit complexity. The digital calibration scheme will share all the blocks with NS SAR ADC and only needs to be performed once before the conversion, therefore, it will not increase the power consumption.

3.2 Architecture

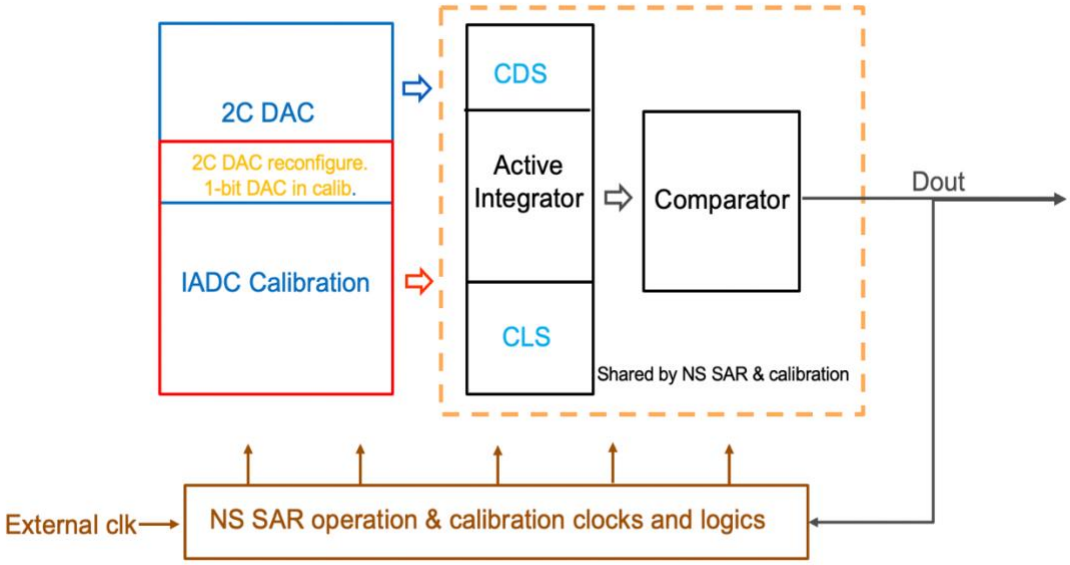


Fig. 3.1 System diagram blocks of the proposed NS SAR ADC

Figure 3.1 shows a top level description for the proposed converter with digital calibration scheme. It includes a 2-C DAC, CDS and CLS network, an op-amp as the integrator, a comparator and digital control circuits. There are two operation modes of proposed ADC. One is the normal ADC conversion step which can be performed with and without noise shaping. Another one is calibration mode which is used to calibrate the DAC error.

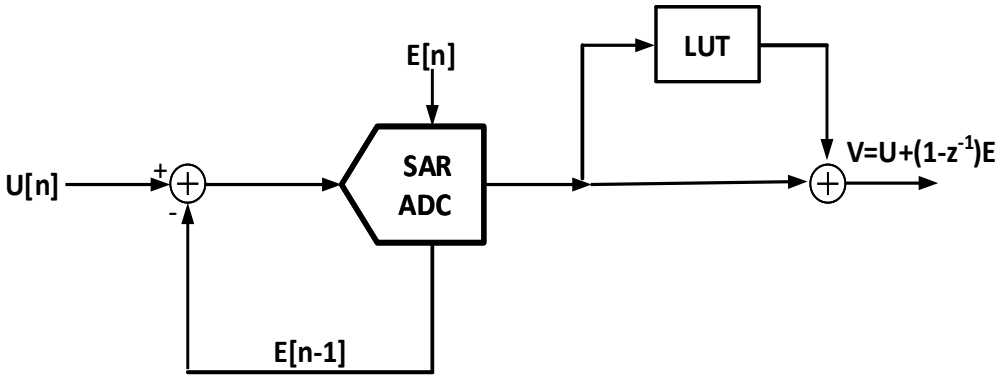


Fig. 3.2 Conceptual block diagram of normal NS SAR conversion step

During normal conversion, as shown in Fig. 3.2, it consists of a 2-C DAC based SAR ADC, and an error look up table (LUT) which is generated by the calibration step.

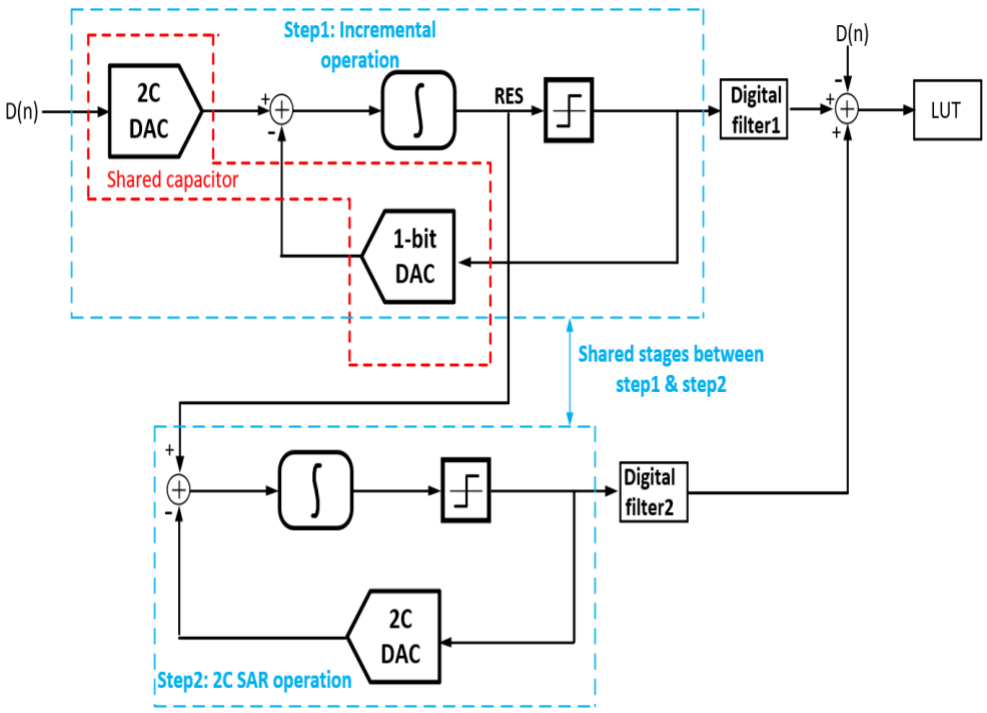


Fig. 3.3 Configuration in calibration mode

Figure 3.3 shows the diagram blocks in the calibration mode of proposed ADC. As mentioned before, it will share all major blocks with the normal conversion step, so it will not increase the complexity. It is operated as a two-step first order incremental ADC (IADC) to convert the DAC error. The details will be discussed later.

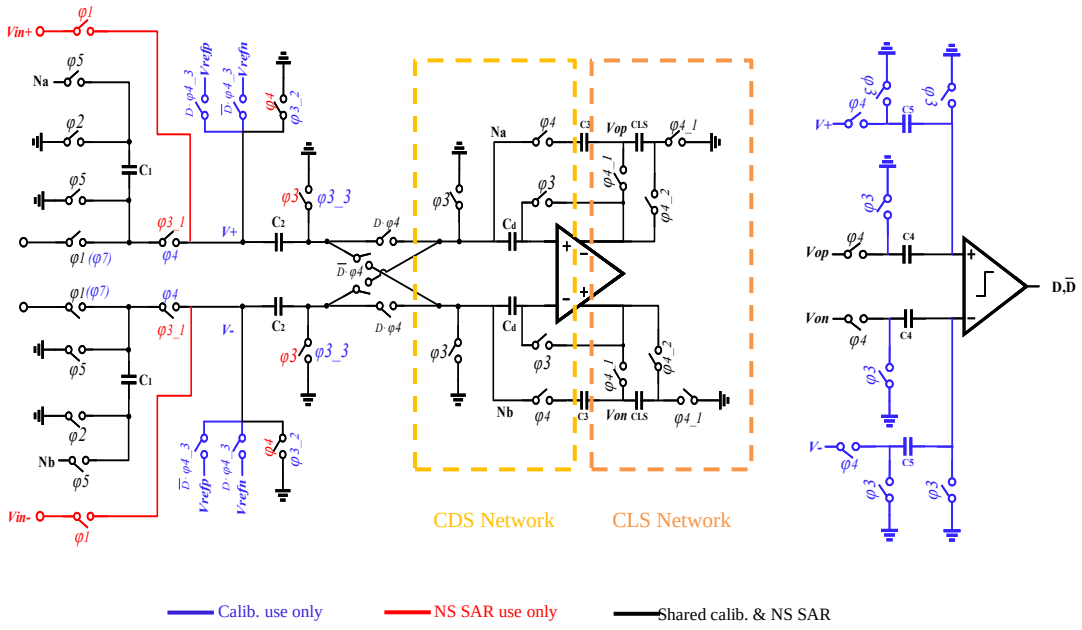


Fig. 3.4 Block diagram of proposed ADC

The proposed ADC architecture is shown in Fig. 3.4. Blue notation circuits and clock phases are only work during the calibration step. Red circuits are work only for normal operation step. All other circuits are shared between these two steps.

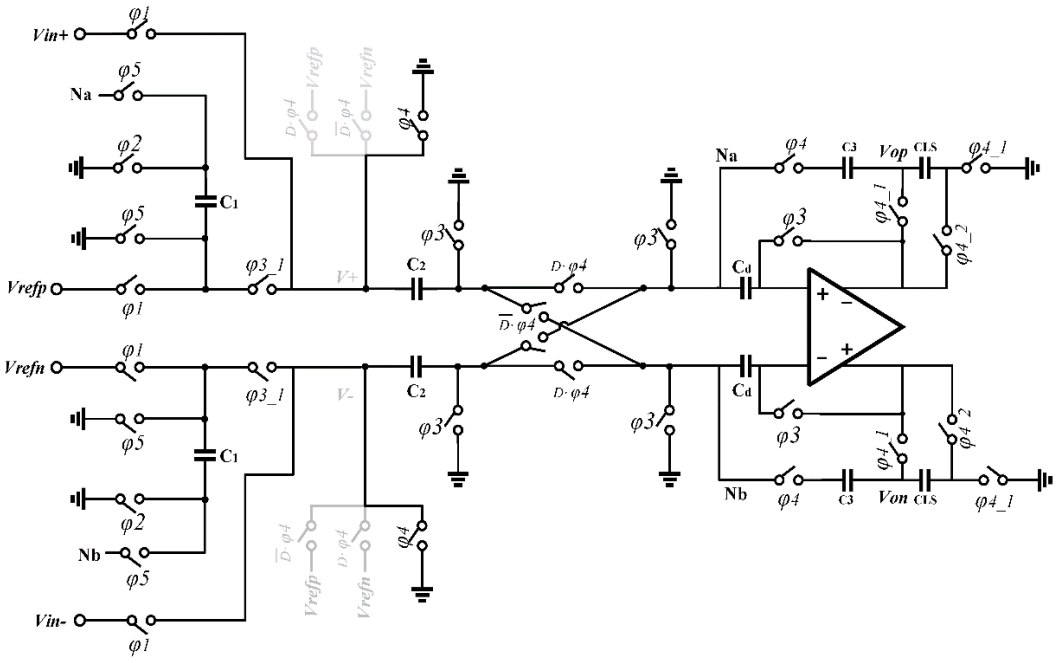
During normal conversion, the ADC will perform a 10-bit SAR conversion with a 32 OSR. With the active integrator, the NTF is $1-z^{-1}$. A CDS network is added at the input side of the integrator to reduce the DC offset and flicker noise from the op-amp. Similarly, a CLS network is added at the output of the integrator which can boost the DC gain of the op-amp. Therefore, the power consumption can be reduced with these two techniques. A single bit comparator is followed and hence can achieve high

linearity. After this 10-bit conversion finished, the converted digital codes will be combined with the errors in LUT which is generated by calibration to correct the errors from the 2-C DAC.

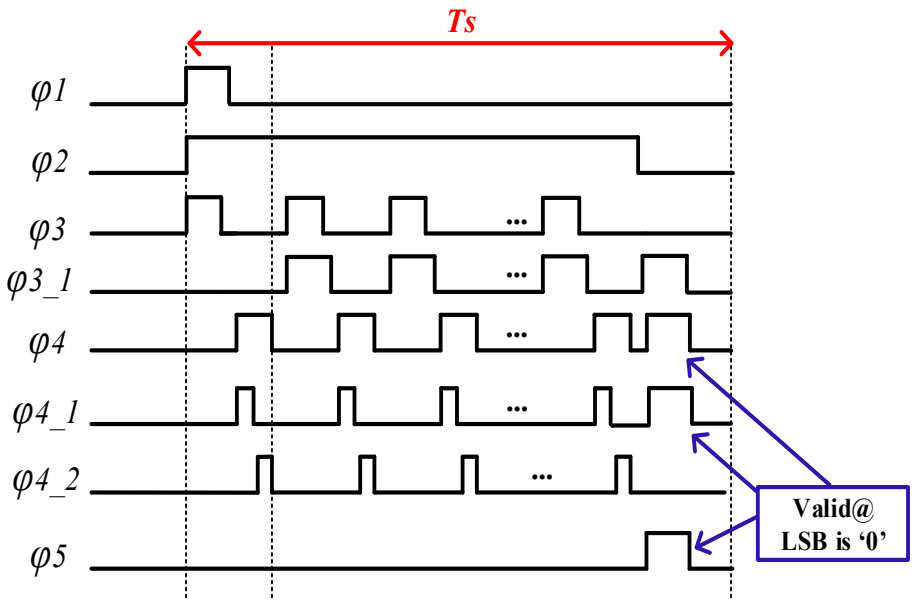
During the calibration step, the ADC will be reconfigured as a two-step first order IADC. The first step is an incremental ADC operation, and the second step is an 8-bit binary SAR operation. In this step, the input is a DC value, so there is no specific clock and speed requirement such as in [19] and [20]. Besides, it shares all circuits between step1 and step 2, so the power efficiency is improved.

3.3 Circuit Implementation

3.3.1 NS SAR Configuration



(a)



(b)

Fig. 3.5 (a) NS SAR conversion mode configuration, (b) Timing diagram

The switched-capacitor circuit implementation of proposed NS SAR ADC in normal conversion is shown in Fig. 3.5 (a), and the timing is shown in Fig. 3.5 (b).

Sampling: During the period when $\varphi1, \varphi2$ and $\varphi3$ are high, the input signal and reference voltage will be sampled on C_1 and C_2, respectively, and the input signal will be transferred and held in C_3. The reference will be stored in C_2 during all conversion cycles, so the reference buffer is disconnected from the DAC during conversion. This relaxes the requirements of the reference buffer, as compared to a conventional SAR ADC.

Conversion: When $\varphi3\_1$ goes high, C_1 and C_2 will share charges. The ideal values of C_1 and C_2 are the same, so after the first charge sharing, the voltages of both C_1 and C_2 are $\frac{1}{2}V_{ref}$. The charge in C_2 will be added or subtracted from that of C_3, depending of the output of comparator. This step is then repeated to get $\frac{1}{4}V_{ref}, \frac{1}{8}V_{ref}, \ldots$ resulting

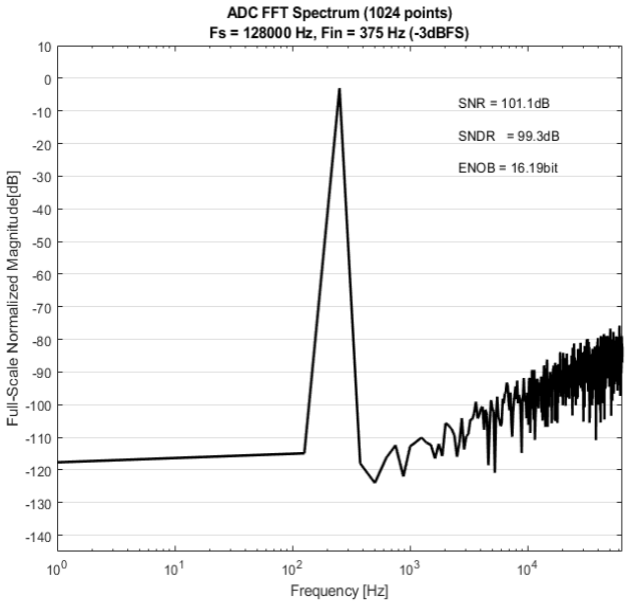
in a binary search. A 10-bit SAR conversion was targeted in this work. After the last bit was obtained, the quantization error charge is left in C_3, and the circuit proceeds goes to the next conversion without resetting C_3. Therefore, a first order noise shaping is achieved.

3.3.2 Correlated Double Sampling and Correlated Level Shifting

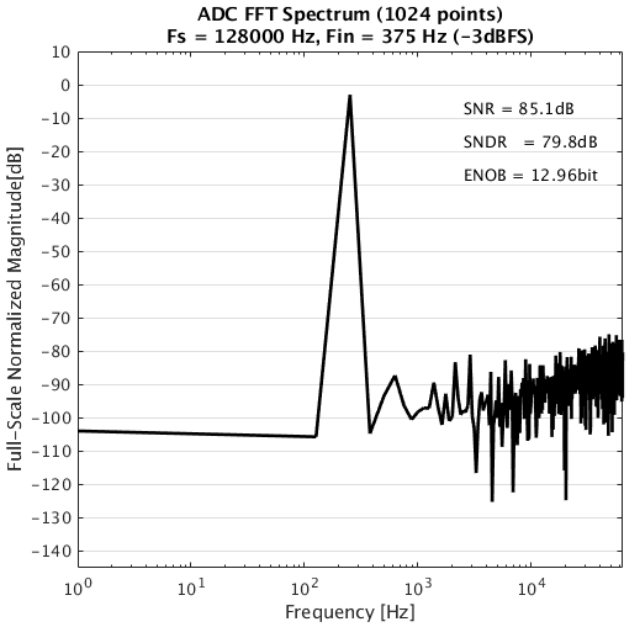
The DC offset of the op-amp will introduce harmonic distortion to the ADC. Suppose that Vos is the offset of op-amp. During the SAR conversion, the output voltage of integrator is:

$$Vout = Vin \pm \frac{1}{2}Vref + Vos \pm \frac{1}{4}Vref + Vos \cdots \pm \frac{1}{2^n}Vref + Vos \qquad (3.1)$$

According equation (3.1), this will add this fixed offset voltage to the conversion from MSB to LSB. The reference voltage is scaled by binary weighted and the SAR scheme should be a binary scaling, however, the offset voltage is not be binary scaled, therefore, it will cause distortion in the ADC.



(a)

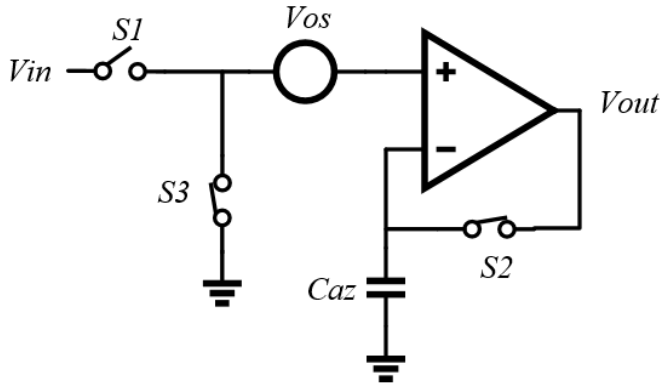


(b)

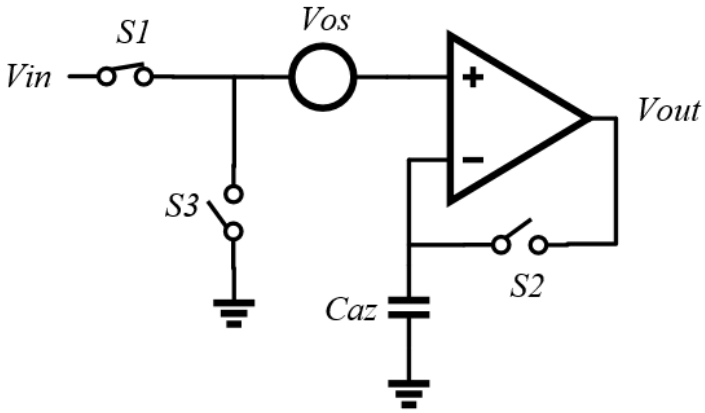
Fig. 3.6 (a) Simulated PSD of proposed NS SAR ADC with ideal circuit, (b) PSD with 0.7mV op-amp DC offset

Some simulation results are shown in Fig. 3.6. Figure 3.6 (a) was simulated with a macro model in which every block is ideal. With 32 OSR, the ideal SNDR is 99dB. In Fig. 3.6 (b), a 0.7mV offset is added to the op-amp macro model, and the PSD shows a 79dB SNDR which has a 20dB degradation compared to the ideal case. In 180nm process, it usually has a 5mV or larger offset for op-amp, and this offset is too large for the proposed NS SAR ADC. It has to be cancelled. In general, there two techniques to decrease the offset. One is chopping and another one is correlated double sampling (CDS). The scheme of chopping modulates the DC offset to high frequency and then use a filter to filter it out. However, based on equation (1), the offset has been already introduced to each bit, so the chopper can't work to reduce the DC offset effect in the proposed circuit. As a result, CDS is implemented to this work.

Correlated double sampling was proposed in [13] to improve the performance of the op-amp. It can reduce the DC offset and flicker noise of the op-amp. The basic architecture is shown in Fig 3.6.



(a)



(b)

A capacitor C_{az} is added to the input of op-amp. During the auto-zeroing phase shown as Fig. 3.6 (a). S2 and S3 are closed, while S1 is open. Suppose the DC offset

of the op-amp is Vos and hence this value will be sampled and held in Caz. For the next amplification phase shown as Fig. 3.6 (b), S1 is closed, S2 and S3 are open. Assuming the finite DC gain of op-amp is A, and since the offset already stored in Caz, the input referred DC offset residue becomes;

$$V_{res} = \frac{V_{os}}{A+1} \tag{3.2}$$

According equation (3.2), the effective offset is reduced, from equation (3.1), if the op-amp has gain of 1000 and 5mV offset, the output of integrator only can see a 5uV offset which will not decrease the linearity of the proposed ADC. Similarly, the low frequency noise (flicker noise) can also be reduced by this scheme. The CDS implementation is shown in Fig. 3.7, and capacitor C_d is added for it. The CDS can be done only during each sampling clock phase and also can be used for each bit. From kT/C thermal noise consideration, doing bit by bit conversion is better for lower thermal noise introduced by the CDS network. This will be discussed later.

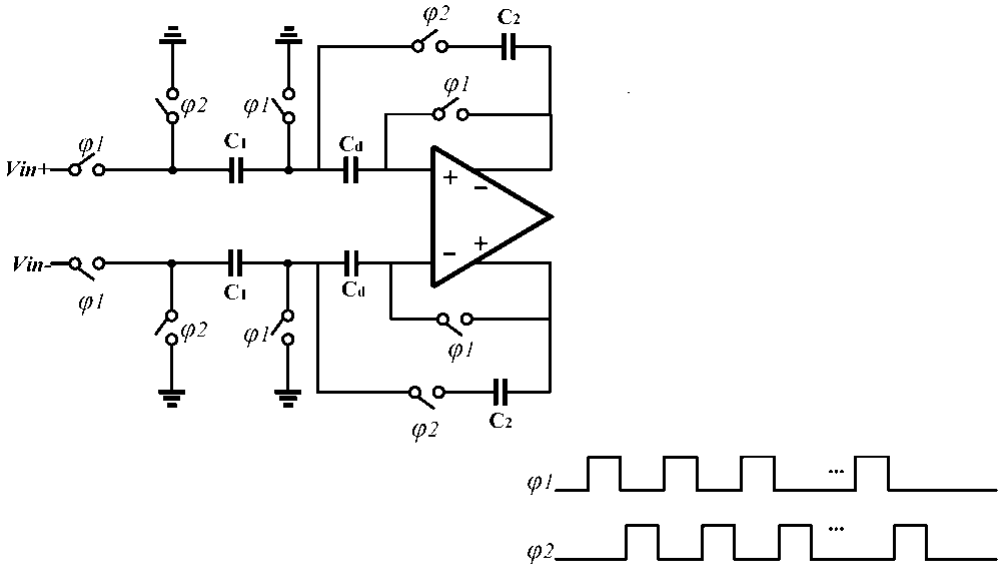
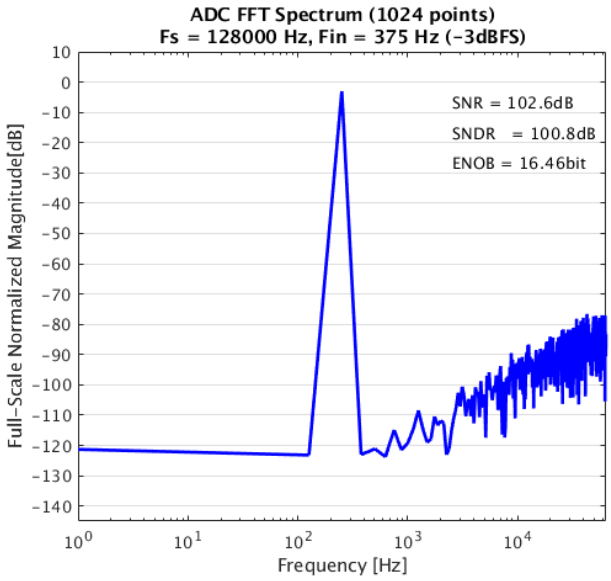
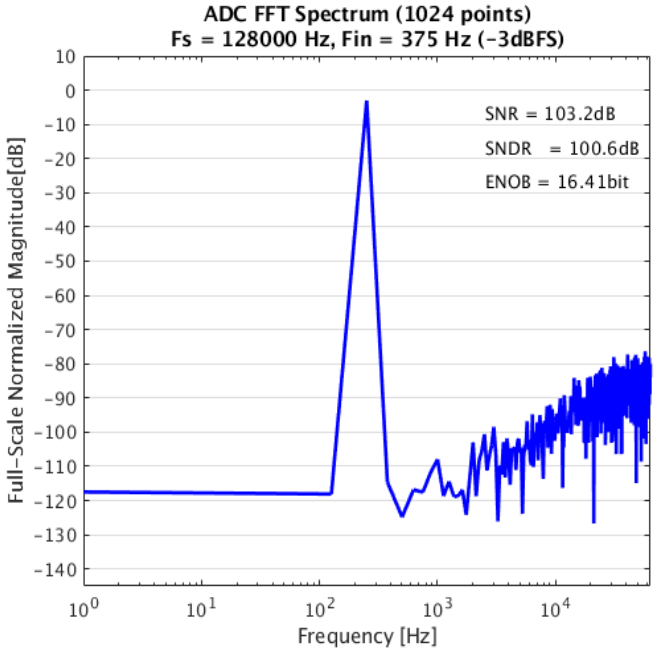


Fig. 3.7 CDS implementation in proposed ADC

Figure 3.8 shows the simulated results with and without CDS. With CDS, the ADC can still have nearly ideal performance with a 5mV op-amp offset.



(a)



(b)

Fig. 3.8 (a) Simulated PSD without op-amp offset (b) with 5mV offset

Moreover, the DC gain of the op-amp will also affect the linearity of the whole system. A simulated PSD with different DC gain values is shown below.

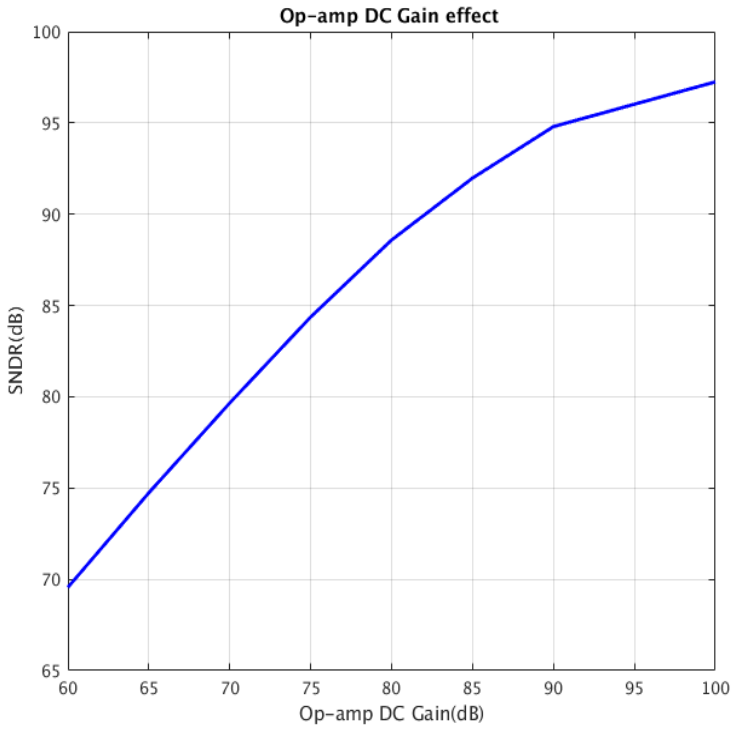


Fig. 3.9 Simulated op-amp finite DC gain effect

In one previous work [5], a two-stage op-amp with Miller compensation was designed to achieve a high DC gain. However, it draws about 40uA current which is too high for a low frequency ADC design.

To achieve a high DC op-amp gain and keep a low power consumption, CLS technique was implemented to this work. Similar to CDS, CLS needs one extra capacitor and some switches. However, the CLS network will be added at the output of the op-amp. CLS can improve the gain from A to (almost) A^2. This effect will be degraded in real circuit implementation, but it still boosts the DC gain significantly.

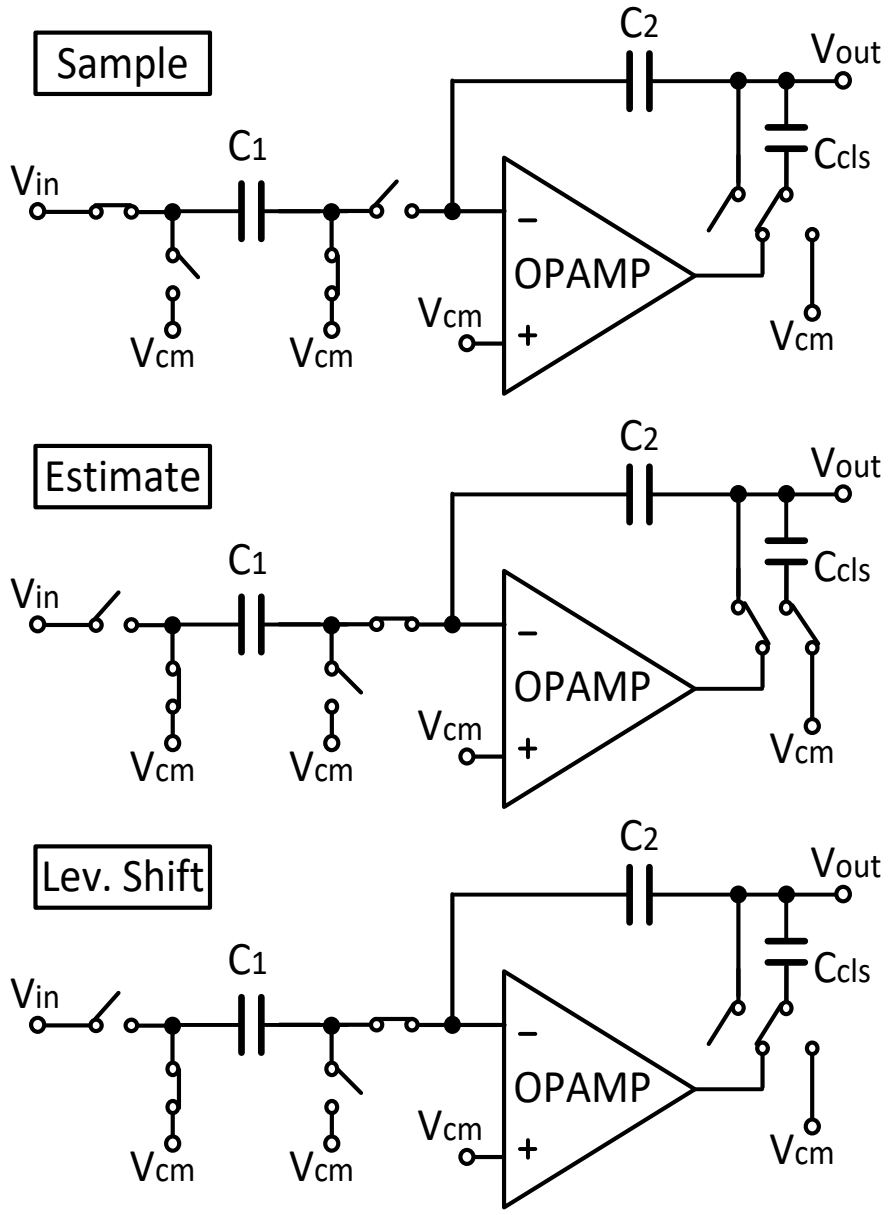


Fig. 3.10 Operation of CLS [18]

There are three steps in the CLS operation: sampling, estimation and level shift.

CLS sampling: During the sampling phase, the entire CLS network is disconnected from the op-amp output which means it will not work during the sampling phase. The input signal will be sampled on capacitor C_1.

CLS estimation: In the estimation phase, the sampled input will be transferred to the output of the op-amp. At the same time, the CLS capacitor C_{LS} will also be connected to the output. Therefore, the sampled input information can be tracked and stored in C_{LS}. The voltage left in C_1 is:

$$V_{c1,est} = -\frac{V_{out,est}}{A_{est}} \tag{3}$$

where subscript 'est' stands for estimation phase. If the voltage left in C_1 is smaller, then the charge transfer is more accurate. In general, people will increase the gain of op-amp to minimize this value. According to equation (3), there is another way to decrease the value of V_{c1} which is to decrease the numerator. In other word, one can make the output of op-amp as small as possible. This is the theory of CLS.

CLS level shifting: In this phase, C_{LS} will be disconnect from common mode voltage port and is connected into the feedback loop of the op-amp to perform a fine integration. Since it already has the information from the previous estimation phase, it will use this estimated value to remove the signal from the output of the op-amp. The output voltage of op-amp becomes:

$$V_{c1(ls)} = -\frac{V_{out(ls)} - V_{out(est)}}{A_{LS}} \tag{3.4}$$

The numerator in equation (3.4) is much smaller than in equation (3.3). As a result, the equivalent DC gain is improved significantly by CLS. One concern is the CLS adds one capacitor at the output so that it loads the op-amp directly. However, this is will not slow the op-amp. During the level shifting phase, this CLS capacitor will be included in the feedback loop which does not load to the op-amp [18]. The CLS implementation is shown in Fig. 3.11.

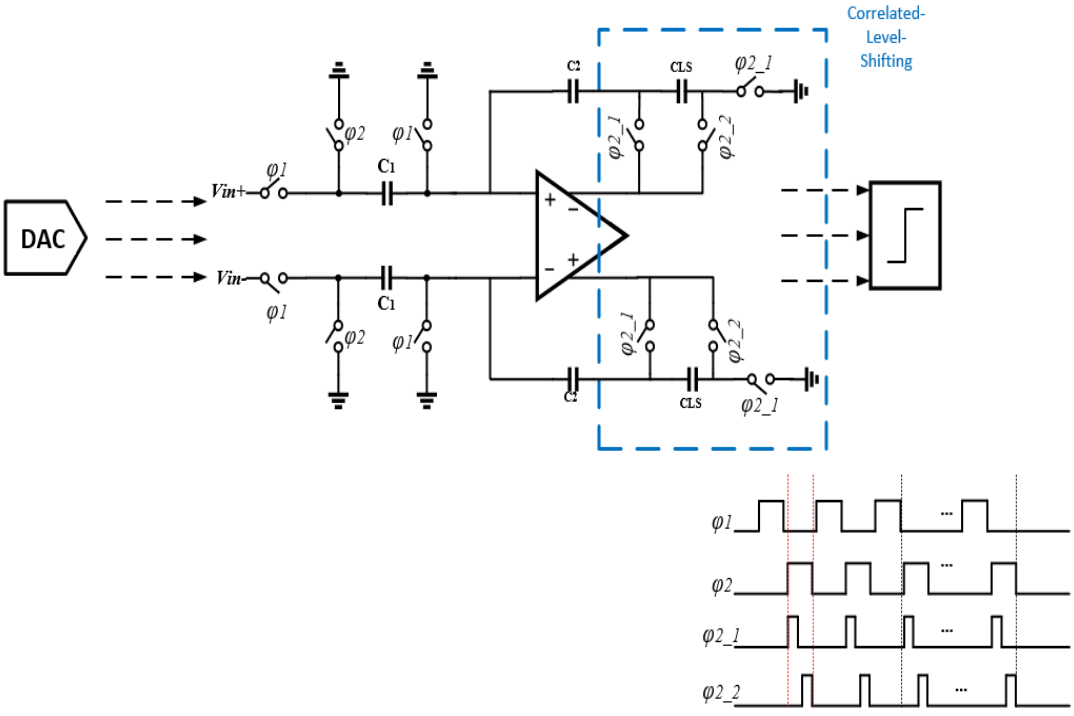
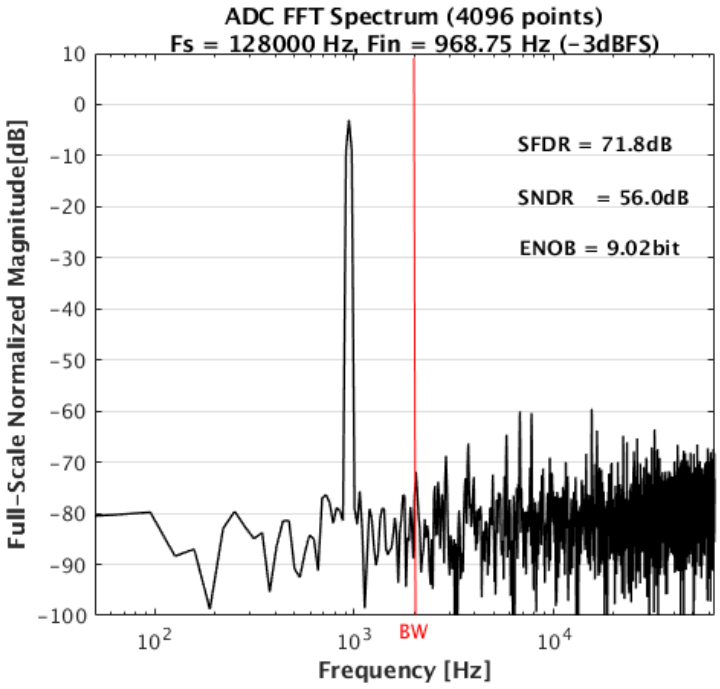
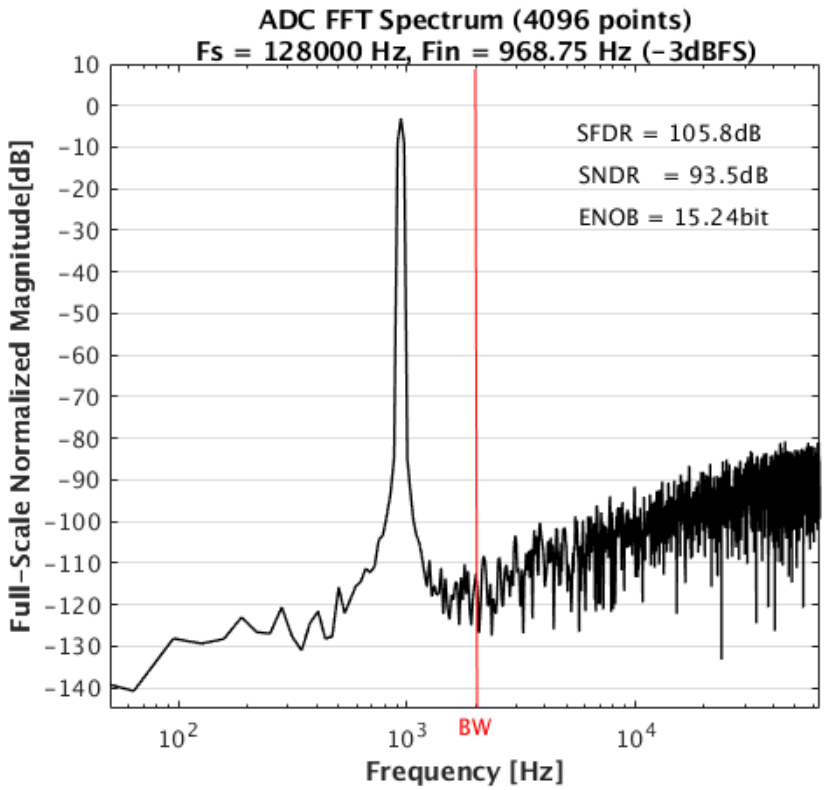


Fig. 3.11 Implementation of CLS



(a)



(b)

Fig. 3.12 (a) Simulated PSD without CLS, (b) with CLS

A gain of 40dB in the op-amp macro model was used in this simulation. For a 40dB gain op-amp, the DC gain is too low to suppress the nonlinearity and the noise, so the SNDR is only about 56dB without the CLS. After enabling the CLS network, it has a more than 30dB improvement in SNDR even with a very low op-amp DC gain. Based on Fig. 3.9, if there is no CLS, it needs a around 85dB op-amp DC gain to achieve over 90dB SNDR. This means that the CLS can achieve the same performance with only half DC gain of the op-amp. Assume the op-amp has same bandwidth, the power of the op-amp can be reduced by 50 percent. In the real circuits implementation, there will be parasitic and capacitance variation which may degrade the performance of CLS, but it can have a significant improvement [18].

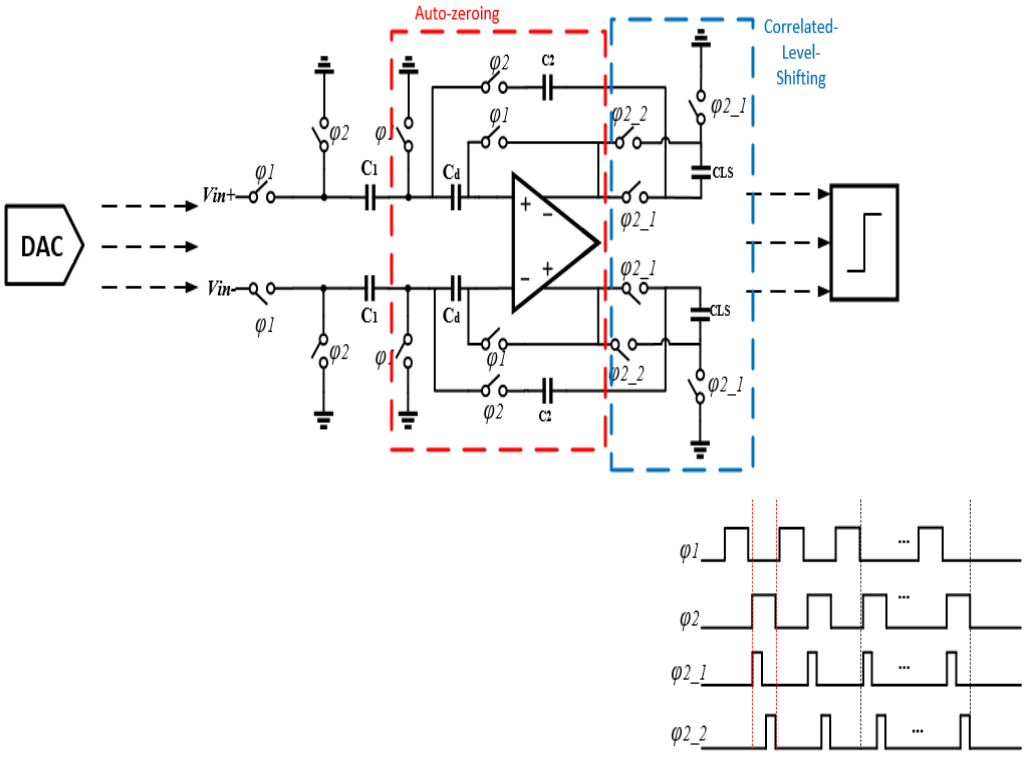


Fig. 3.13 Combination CDS and CLS to proposed NS SAR ADC

Figure 3.13 shows the implementation of CDS and CLS in one op-amp at the same time. The simplified timing is also given in it. First, it will perform auto-zeroing and then to perform the CLS. For CLS operation, phase 2 will be divided as two half clock cycles to perform the estimation phase and level shifting phase.

A simulated performance of proposed NS SAR ADC with CDS and CLS is shown in Fig. 3.14. The op-amp was designed with a 40dB DC gain and 20MHz unity gain bandwidth. A fixed 5mV offset is added to the op-amp input by adding a DC voltage source. With this low performance op-amp, if there were no CDS and CLS assistance, there would be serious harmonic distortion. With both CDS and CLS enabled, it can achieve an over 90dB SNDR performance with this op-amp.

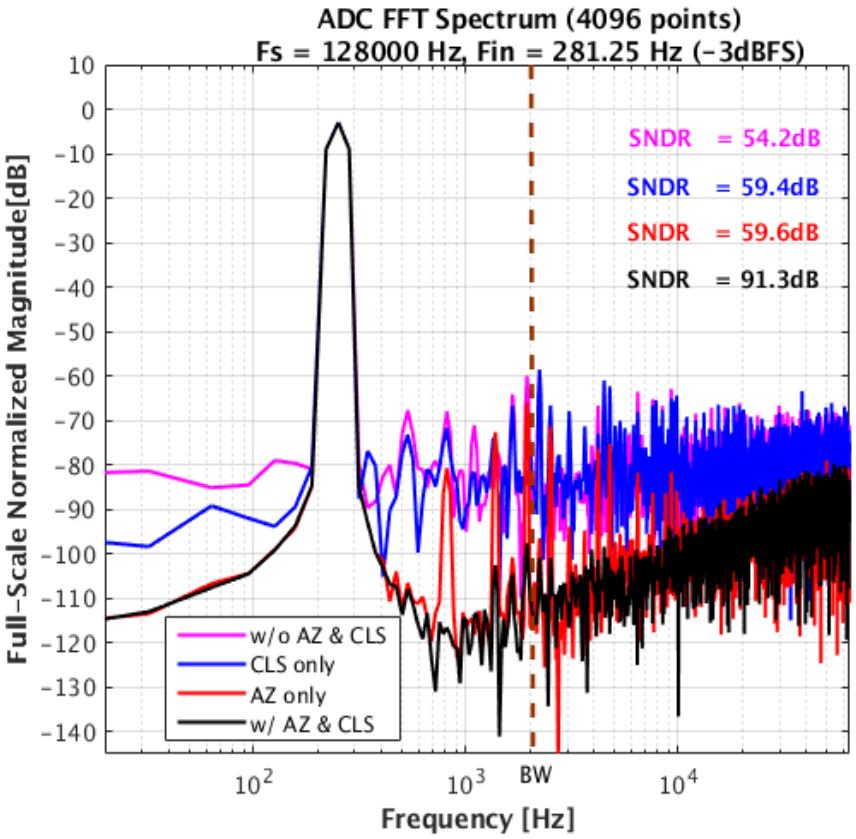


Fig. 3.14 Performance comparison w/ and w/o CDS and CLS

Because both of CDS and CLS add extra capacitors to the input and output of op-amp, these capacitors will introduce thermal noise to the ADC during the conversion.

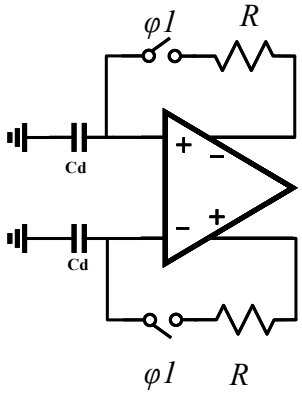
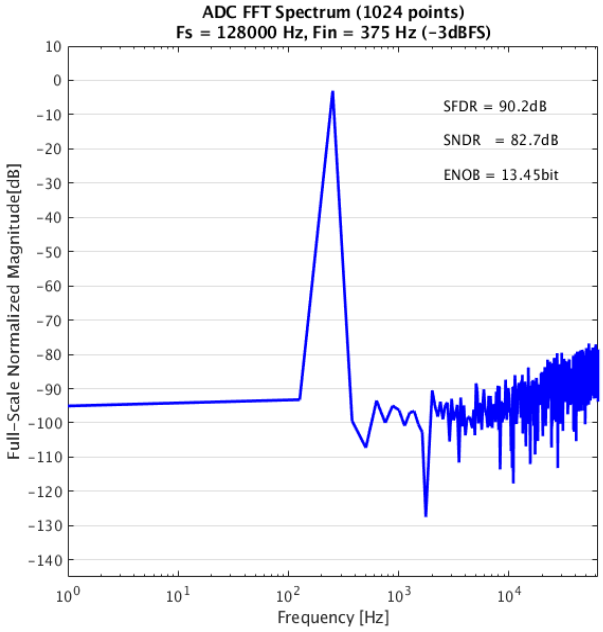
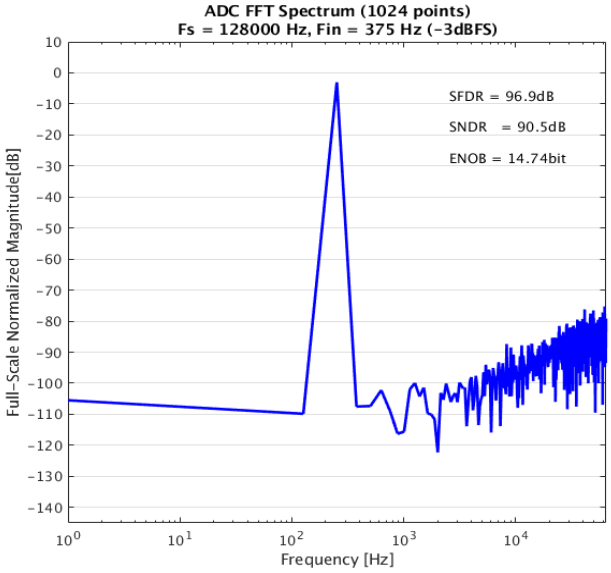


Fig. 3.15 Noise of CDS

The main difference between CDS and CLS on noise is that CDS adds noise directly to the input of op-amp, while CLS adds noise at the output of the op-amp. For the correlated double sampling shown in Fig. 3.15, the switch can be modeled by an ideal switch and a noisy resistance. For one CDS operation cycle, there is a kT/C thermal noise that will be held in the capacitor C_d, and this noise will be added to the signal directly without any attenuation. This has a significant effect to the SNR of the proposed ADC. To reduce the noise from CDS, the CDS will be done for each bit conversion. In Fig. 3.5 (b), phase 1 is the sampling clock and phase 3 is used for CDS. There are two options, one is it can make phase 3 is exactly same with phase1 which means CDS is done only during sampling. Another one is, phase 3 is clocked 10 times faster so that CDS is done for each bit conversion. With 10 times faster, the idea is the same with oversampling, the noise from CDS is getting oversampled and so the signal band noise is reduced. The simulated noise differences are shown in Fig. 3.16.



(a)



(b)

Fig. 3.16 CDS noise simulation (a) CDS only works in sampling phase, (b) work in each bit conversion

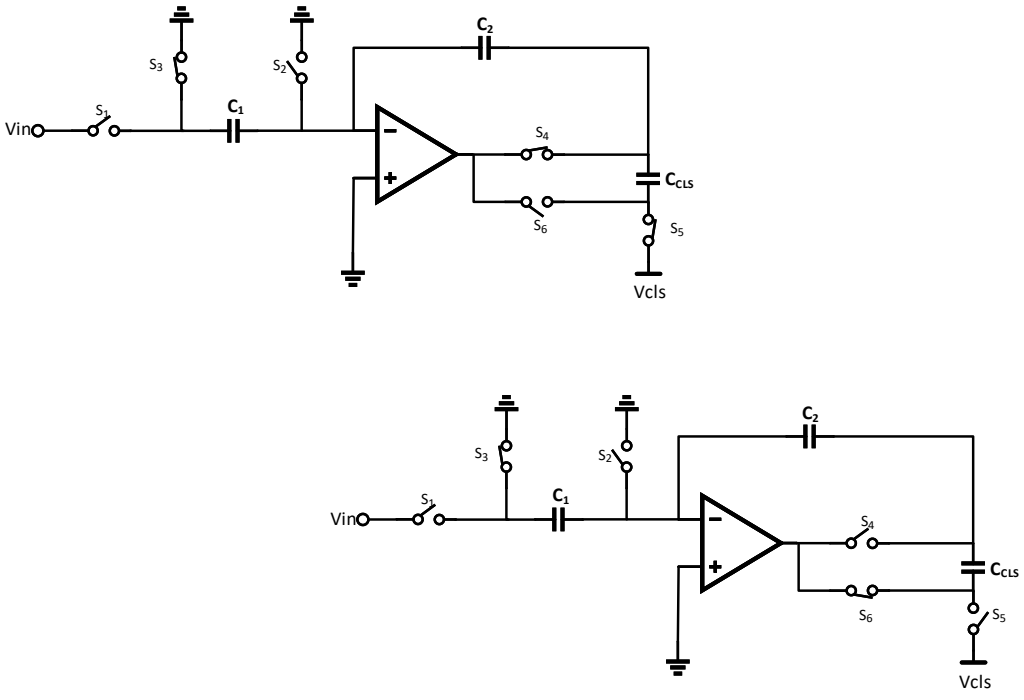


Fig. 3.17 Two operation phases of CLS

The correlated level shifting also needs to add a capacitor and some switches to the stage. However, these circuits are at the output of the op-amp, so the input referred noise from the CLS capacitor will be attenuated by the gain of the op-amp. Suppose the op-amp loop gain is A_{LS}, so the thermal noise from the CLS capacitor is $\frac{kT}{A_{LS} \cdot C}$. Compared with the thermal noise from CDS with same capacitor size, it is much smaller because of the loop gain attenuation. While noise of CDS will be added to signal directly without attenuation, the op-amp noise of CLS is decreased by the loop gain.

3.3.3 2-C DAC Mismatch and Parasitics

The errors due to capacitor mismatch and parasitics in the DAC are critical to the ADC design. In this work, a 2-C DAC was implemented. They have a 4pF capacitance value which is good for matching, but the parasitics of the top plate and switches junction capacitors are also an error source. Moreover, due to the process variations, the matching error may be larger under some conditions. Therefore, a digital calibration was implemented to cancel these errors. The analysis of 2-C DAC mismatch and parasitics is given below.

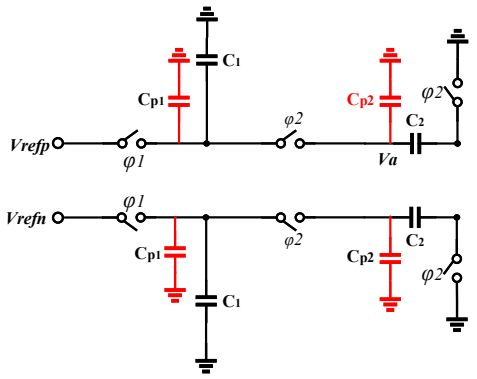


Fig. 3.18 Mismatch and parasitics in 2-C DAC

In Fig. 3.18, C_1 and C_2 perform as 2-C DAC and have ideally equal values. C_{p1} and C_{p2} are parasitics from top plate and switches in 2-C DAC. When $\varphi 1$is high, the total charge sampled on C_1 is

$$Q_{total} = (C_1 + C_2) \square V_{ref} \tag{3.5}$$

During the first charge sharing phase when $\varphi 2$ is high,

$$V_a = \frac{C_1 + C_{p1}}{C_1 + C_{p1} + C_2 + C_{p2}} \square V_{ref} \tag{3.6}$$

The corresponding charge will be transferred to the output of the integrator, and there will be no charge left in C_2. The total charge left in C_1 is

$$Q_{total} = a(C_1 + C_{p1}) \square V_{ref} \tag{3.7}$$

where $a = (C_1 + C_{p1}) / (C_1 + C_{p1} + C_2 + C_{p2})$.

In the second charge sharing phase,

$$V_a = a^2 \square V_{ref} \tag{3.8}$$

This step will be repeated until the last bit conversion. Therefore, the voltage at node A for the n_{th} charge sharing will be

$$V_a = a^n \square V_{ref} \tag{3.9}$$

The mismatch has a similar effect. Based on above calculation, for ideal 2-C DAC and switches, there is no parasitics and mismatch and C. Then a will be equal to ½, and the radix is 2 for a binary weighted SAR ADC. When mismatch and parasitic errors are added to the 2-C DAC, it means the actual radix will be changed. If there is a way to obtain these errors, then we will know the radix of the proposed converter in conversion. Therefore, it can be calibrated based on this. Simulation was done to verify the calculation, and the simulated results are shown in Fig. 3.19.

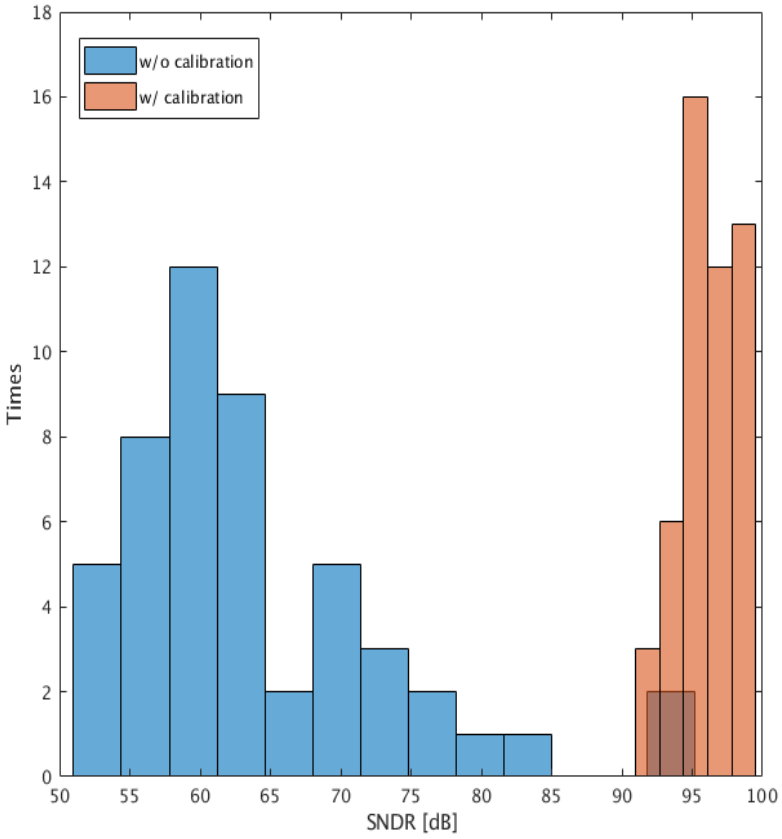
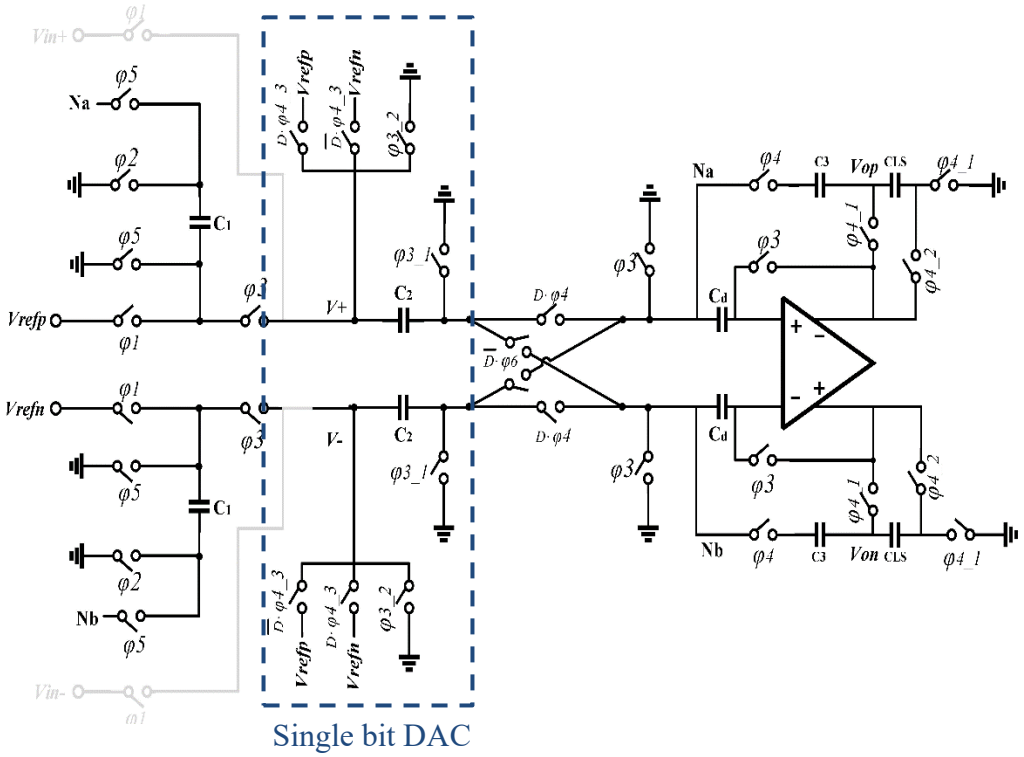


Fig. 3.19 Monte Carlo simulation of DAC mismatch

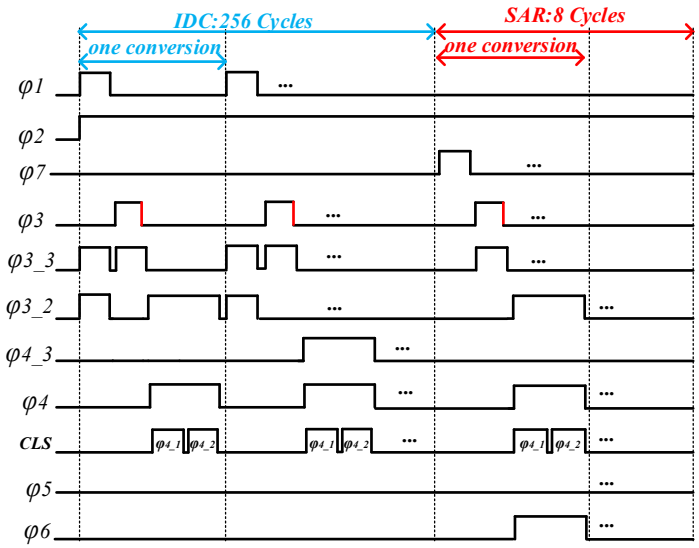
0% ~2% random mismatch and 5%~8% random parasitics capacitor were added to the 2-C DAC, and using MATLAB swept the radix to find the peak SNDR.

3.3.4 Digital Calibration

Based on the previous analysis, a two-step IADC based calibration scheme was implemented in this work to cancel the errors of the 2-C DAC. The goal of this digital calibration is to convert mismatch and parasitic errors to digital codes and store these codes in a look up table (LUT). When the proposed ADC is working in normal operation, these codes in LUT will be combined with the converted codes and processed in the digital domain to cancel these errors.



(a)



(b)

Fig. 3.20 IADC based calibration for the proposed NS SAR ADC

In the calibration mode, the inputs V_{in+} and V_{in-} are disconnected from the circuits. Vrefp and Vrefn become new inputs for the calibration. Initially, the refence voltage will be sampled on C_1, and then it will replica to the operation of the normal NS SAR mode which will do charge sharing between C_1 and C_2. Since the reference voltage and 2-C DAC circuits are the same compared with normal operation mode, so mismatch and parasitics errors will be same when they do charge sharing in calibration step. Therefore, this stored error value will be converted by the designed two-step IADC. The input for calibration is a DC value, so using IADC to convert it will give a very good accuracy. The clock frequency for calibration is not necessary to be the same as for normal operation. A 32kHz sampling frequency was chosen for this work. Capacitor C_2 will also be used as a single bit DAC for the calibration. Hence, the calibration will share all the blocks with normal operation and does not increase the complexity and power consumption of the converter.

It is a two-step operation. To achieve enough calibration accuracy, the first step was designed as 256 cycles incremental operation, and the second step was a 8-bit SAR operation which totally gives a 16-bit calibration accuracy.

As mentioned above, the first step is a first order IADC operation with single bit DAC and single bit quantizer which is shown in Fig. 3.21. To simplify the description, single ended architecture is shown. The actual implementation is a fully differential circuit. In order to relax the output swing requirement of the integrator, a feedforward path was added so that the output range of integrator will be limited to the reference voltage.

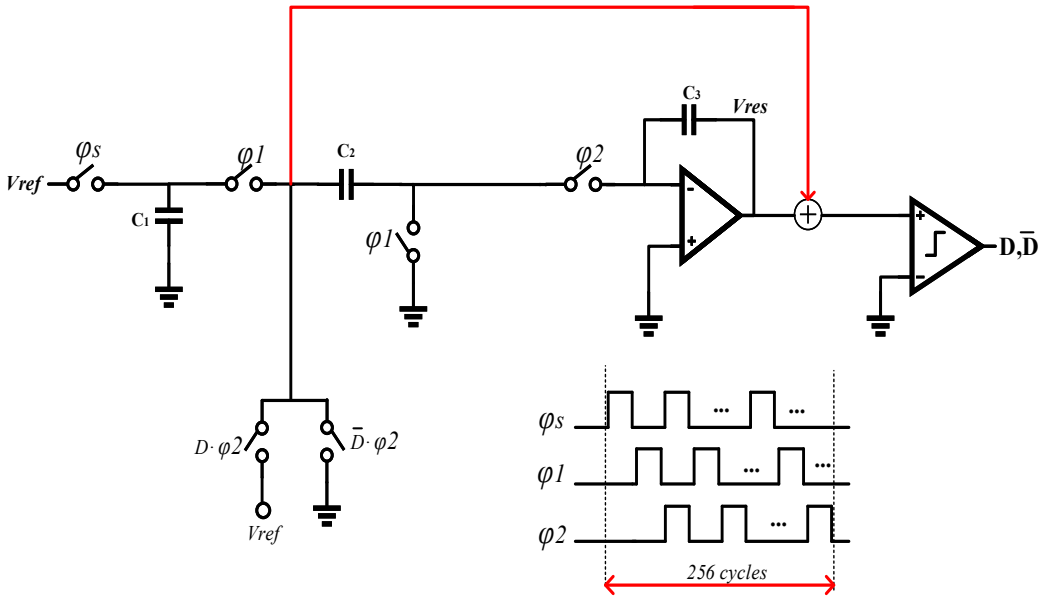


Fig. 3.21 First step of calibration

Sampling: φs goes high to sample the reference to C_1

Conversion: φs turns low and $\varphi 1$ goes high, so it will perform charge sharing with C_2, and based on the digital output of comparator a reference voltage will be added or subtracted from the output of integrator. The circuits will repeat this step 256 times. Then the residue will be stored at the output and sent to the next step.

$$V_{res} = \sum_{i=1}^{M1} Vin[i] - V_{ref} \cdot \sum_{i=1}^{M1} D_{s1}[i] \tag{3.10}$$

Even with the feedforward path, the output voltage range of integrator will still go as high as the power supply voltage if the reference voltage is equal to the voltage supply for calibration. Therefore, to make sure the integrator will not be saturated, the reference voltage was scaled down to 1.2V in the calibration mode. This will introduce an error, but it is only a gain error which is linear, so it will not degrade the entire calibration accuracy.

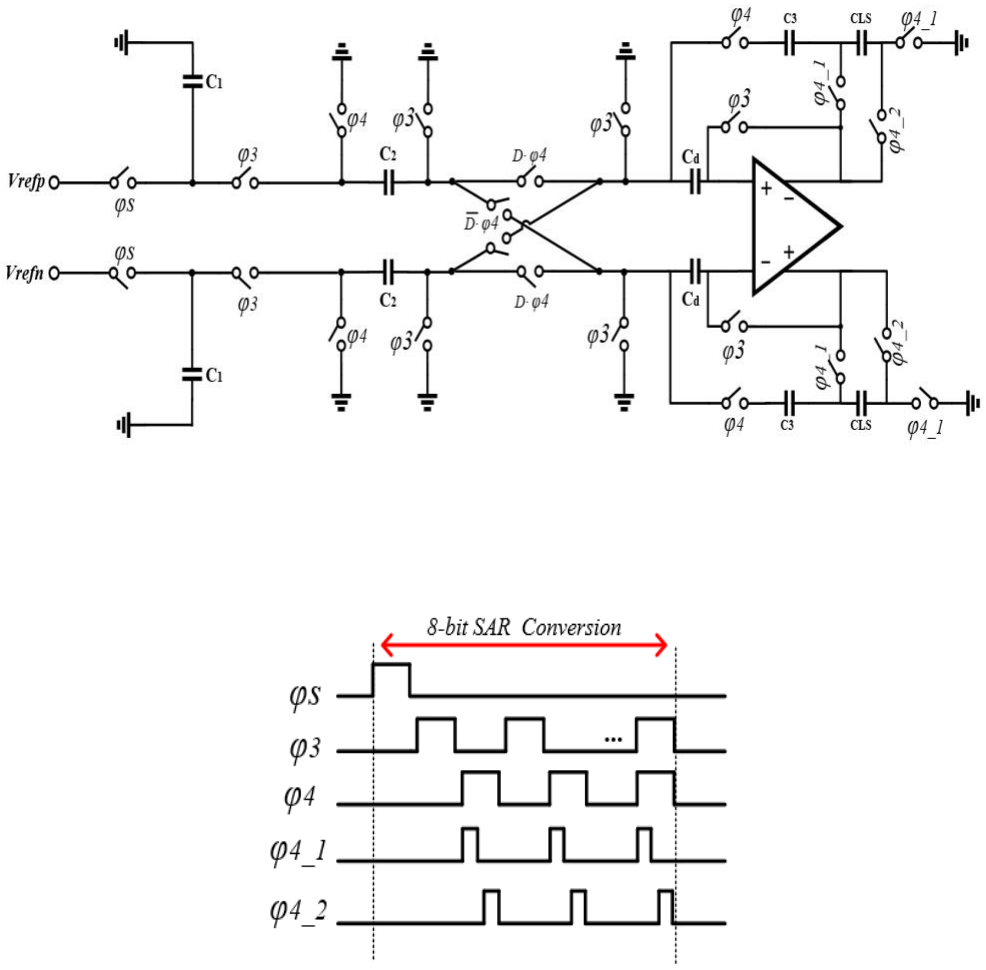


Fig. 3.22 Second step of calibration

In the second step of the calibration mode, the circuit will be reconfigured as a 8-bit SAR with a 2-C DAC. Because the residue of step 1 is already stored at the output of integrator, with this 8-bit conversion this residue will be scaled to a smaller value:

$$V_{res} = \sum_{i=1}^{M1} Vin[i] - \left\{\sum_{i=1}^{M1} D_{s1}[i] - \frac{1}{2^{M2}} \sum_{i=1}^{M2} 2^{M2-i} \cdot D_{s2}[i]\right\} \cdot Vref \qquad (3.11)$$

With the two-step operation, the final residue value left at the output of integrator will be

$$Vin = \frac{1}{M1} \cdot \left\{ \sum_{i=1}^{M1} D_{s1}[i] - \frac{1}{2^{M2}} \sum_{i=1}^{M2} 2^{M2-i} \cdot D_{s2}[i] \right\} \cdot Vref + \frac{Vref}{M1 \times 2^{M2}} \quad (3.12)$$

where the red part is converted value, and the blue part is residue. M1 is equal to 256 cycles and M2 is 8. The calibrated SQNR can be estimated as:

$$SQNR \approx 20 \cdot log_{10}(M1 \cdot 2^{M2}) \quad (3.13)$$

Equation (13) indicates a 96 dB SQNR after calibration corresponding to a 16-bit accuracy. Based on the requirement, we may increase the accuracy of calibration. This can be done by increasing conversion cycles in the first step or the conversion bits in the second step. However, the accuracy of the second step is limited by the 2-C DAC, therefore, if it needs a higher accuracy for the calibration. It is better to increase the number of the conversion cycles in the first step. Transient response of integrator is shown in Fig. 3.23.

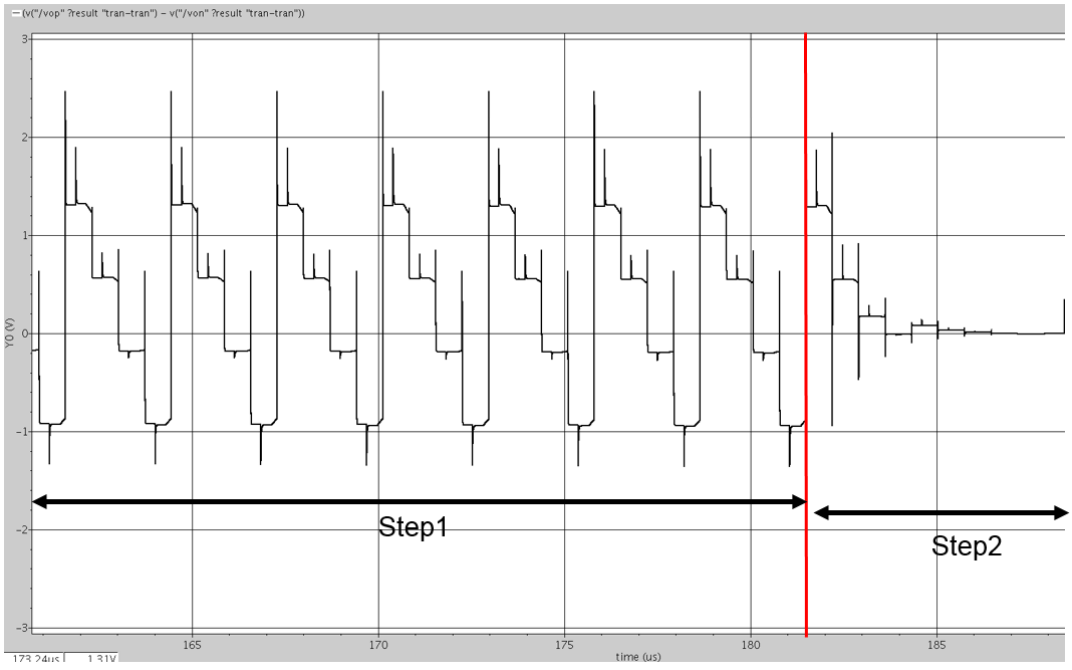


Fig. 3.23 Integrator output transient response in calibration mode

3.3.5 Integrator Op-amp

Correlated double sampling and correlated level shifting were implemented to this work, so we did not need a very high gain op-amp. A current mirror based single stage op-amp [21] [22] was designed as shown in Fig. 3.24.

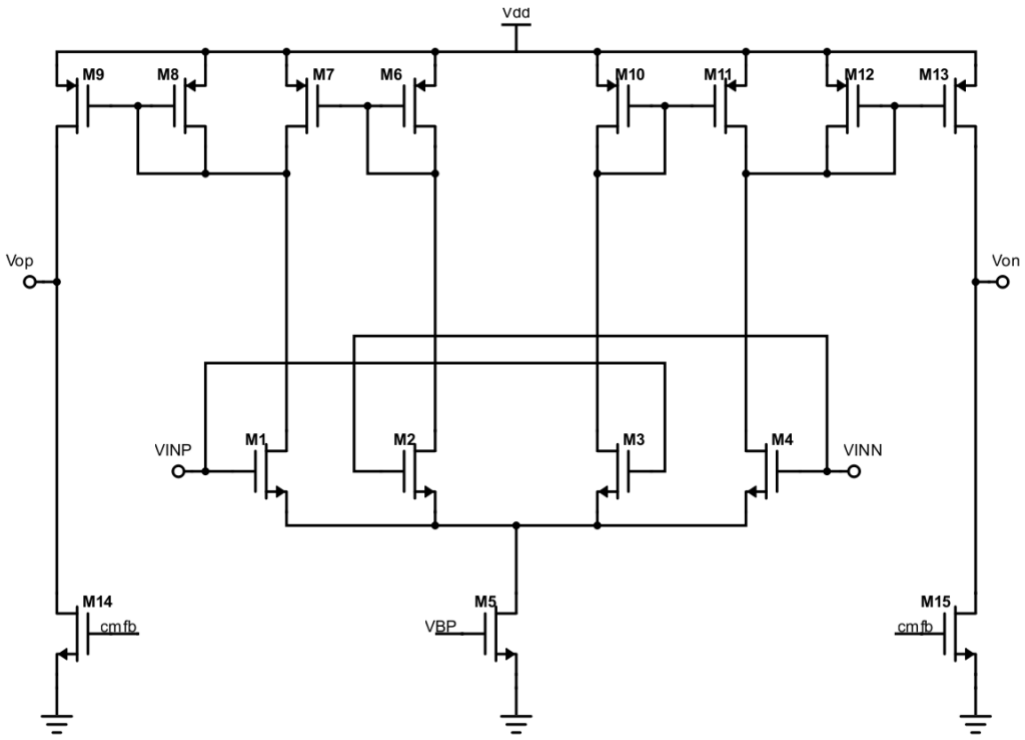


Fig. 3.24 Current mirror integrator op-amp

The effective Gm can be calculated as:

$$G_m = g_{m1} \cdot \frac{(W/L)_{M9,M13}}{(W/L)_{M8,M12}} \cdot (1 + \frac{(W/L)_{M7,M11}}{(W/L)_{M6,M10}} \cdot \frac{(W/L)_{M2,M3}}{(W/L)_{M1,M4}}) \quad (3.14)$$

The dominant pole is located at the drain of M8, we need to size this transistor carefully for stability consideration. The total current consumption was designed as 16uA with 1.6V supply voltage. Based on the simulation, it achieves a 54dB DC gain and 20MHz unity gain bandwidth with a 52-degree phase margin.

To save power, a switched-capacitor common mode feedback (SC-CMFB) circuit is needed to control the output common mode voltage. Since the integrator will work in both CDS and CLS clock cycles, a fully symmetric SC-CMFB [23] is needed.

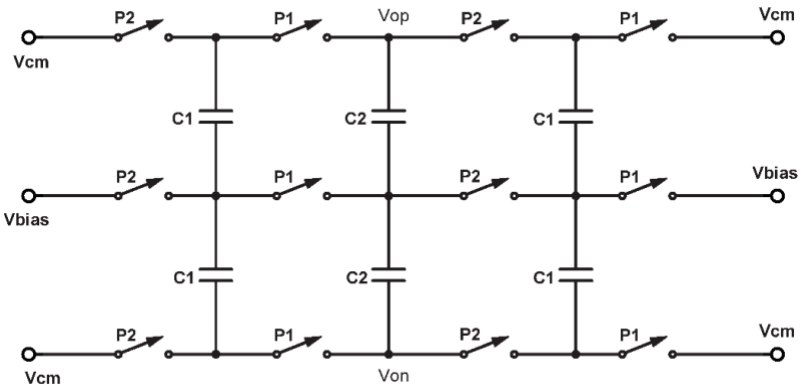


Fig. 3.25 Symmetric SC-CMFB

Compared to traditional SC-CMFB, this SC-CMFB can work for continuous time application [23] . It adds extra capacitance to load the op-amp, but in both phases, the load on the integrator is the same. In this work, C_1 was selected as 0.2pF and C_2 was designed as 1pF. With such small value of C_1, the CMFB circuit can have a faster settling.

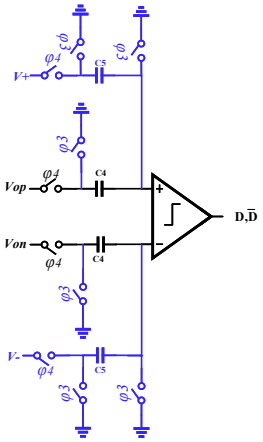


Fig. 3.26 Passive adder for calibration

3.3.6 Passive Adder and Comparator

A passive adder was implemented in this work for the calibration mode. Capacitor C_4 and C_5 are equal as 1pF. At the same time, C_4 also works as auto-zeroing for preamplifier of comparator. The comparator consists of one preamplifier and a dynamic latch.

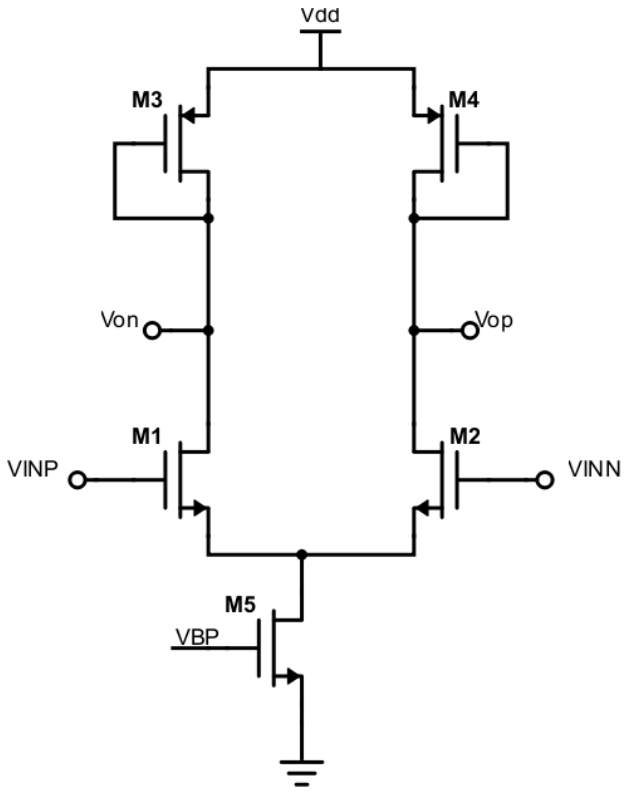


Fig. 3.27 Preamplifier in the comparator

The preamplifier consumes a 1uA current and achieved 8dB DC gain. To reduce the DC offset and flicker noise, auto-zeroing was used in it. The noise of this preamplifier is not critical because it is at the output of the integrator which has a large loop gain to suppress the noise from preamplifier.

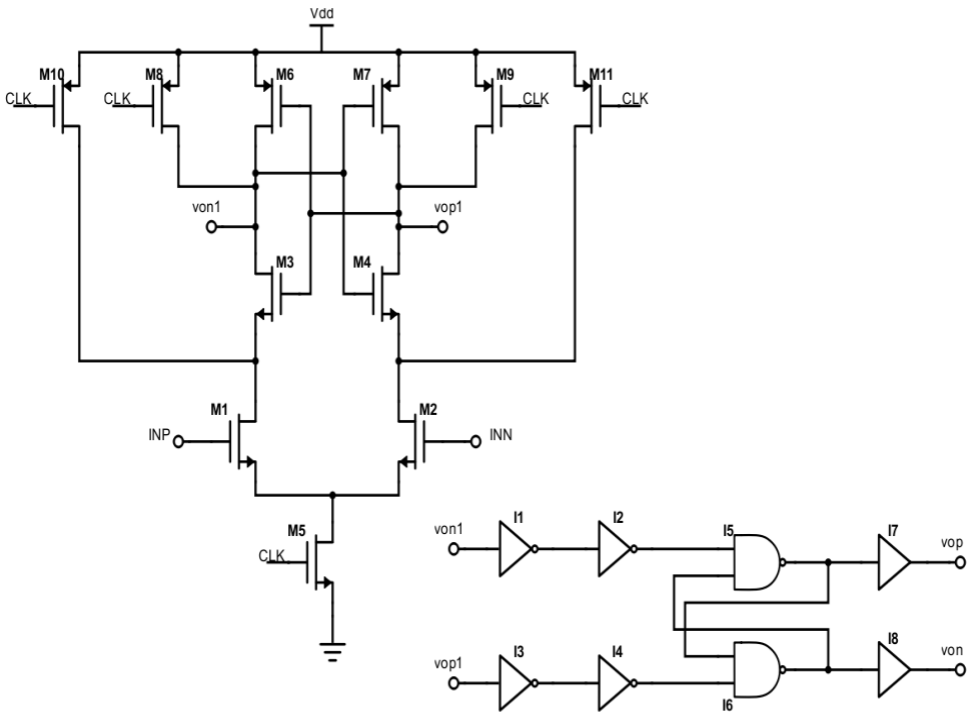


Fig. 3.28 Latch used in comparator

A StrongARM based dynamic latch [24] was used. Inverter buffers are added to prevent the RS latch from disturbing the output of latch, especially for small input. The comparator works with a 1.6V power supply.

3.4 Measurement Results

The prototype test chip was fabricated in a 0.13 um CMOS process. The die microphotograph of the prototype NS SAR ADC is shown in Fig. 3.29. The total active area is around 0.20 mm^2. A 3.84MHz external clock was used and all other clocks and digital control signals were generated by on-chip circuits. The Audio Precision 555 was used to generated fully differential input sinusoid signals for the chip. No extra input buffer and filter were used in the input path. Both analog and digital circuits used 1.6V

power supply. The measured PSD of CDS noise with shorted input is shown in Fig. 3.30. As expected, with CDS for each bit, the noise is getting smaller.

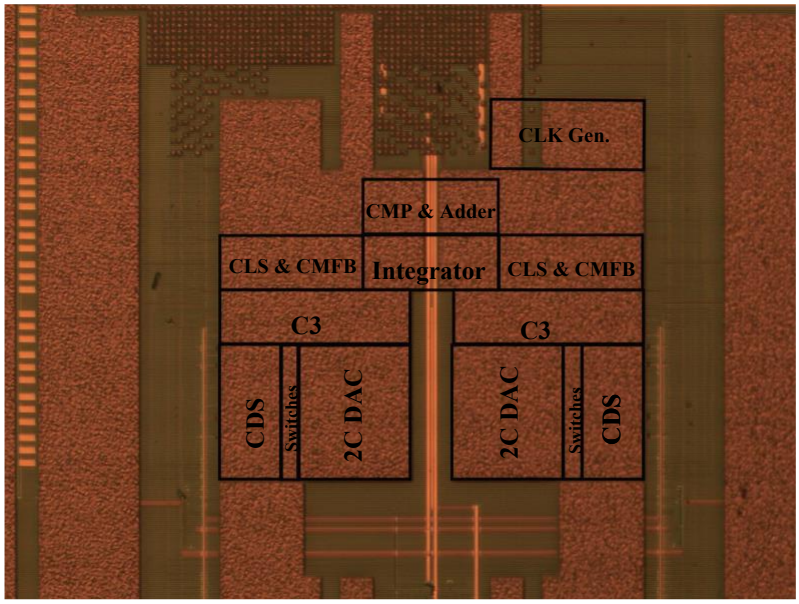


Fig. 3.29 Die photo of proposed NS SAR ADC

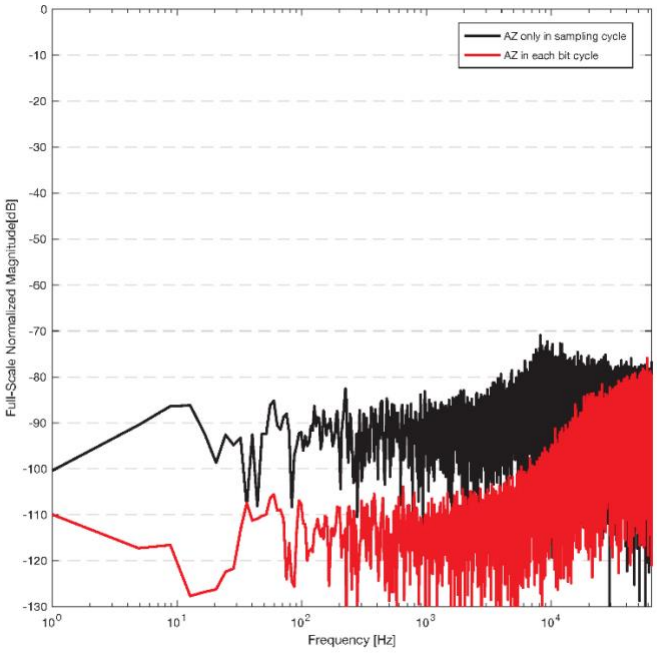


Fig. 3.30 Measured CDS noise

Figure 3.31 shows the measured power spectral densities (PSDs) for the ADC with -2.1 dBFS input sinusoid signal. It indicates that the proposed NS SAR ADC achieves an 82.6 dB SNDR and 90. 9dB SFDR over a 2 kHz signal bandwidth with calibration. The SNDR and SFDR were improved 13 dB and 16 dB, respectively, by calibration.

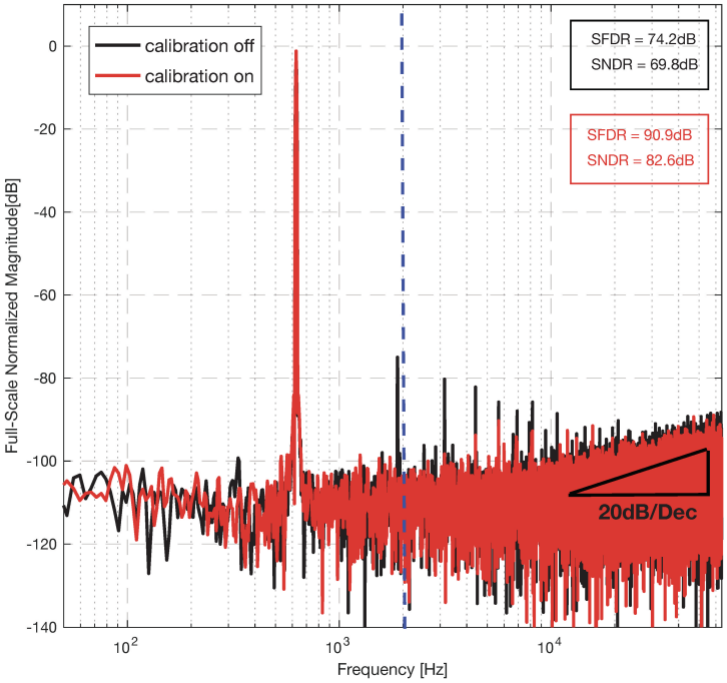


Fig. 3.31 Measured PSD of proposed ADC

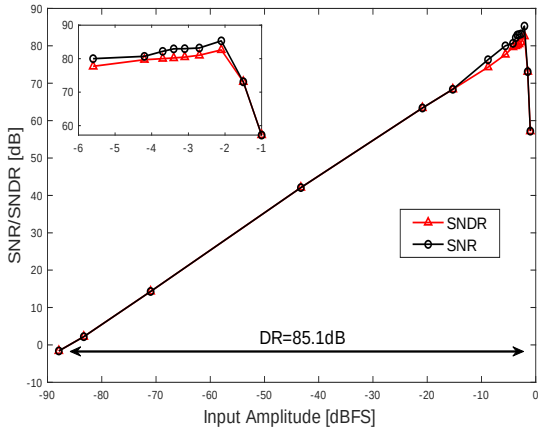


Fig. 3.32 SN(D)R versus input amplitude

It achieved an 85.1dB dynamic range (DR). It consumes a total power of 40.8uW from 1.6V supply. The power breakdown with each block is shown in Fig. 3.33. It has a 163 dB Schreier Figure of Merit. Table 3.1 summarizes the measured performance of the prototype NS SAR ADC and compares it with that of prior works.

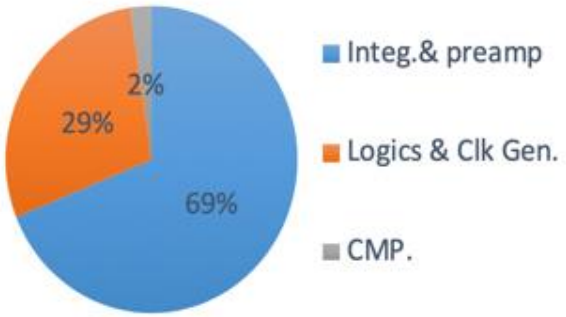


Fig. 3.33 Power consumption

Parameter	**This Work**	CICC 19, [25]	VLSI 15, [3]	ISSCC 13, [26]
Architecture	**NS-SAR**	NS-SAR	NS-SAR	IADC
Technology (nm)	**130**	65	65	160
Supply (V)	**1.6**	0.9/2.1	0.8	1
Area (mm)	**0.2**	0.081	0.0123	0.45
Fs (kHz)	**128**	80e3	50e3	750
Bandwidth (kHz)	**2**	2e3	625	0.667
Power (uW)	**40.8**	2.1e3 w/buffer	120.7	20
SNDR (dB)	**82.6**	73.8	58	81.9
SFDR (dB)	**90.9**	87.3	-	-
DR (dB)	**85.1**	77	-	81.9
FoMs1* (dB)	**163**	167	-	157
FoMs2 (dB)**	**160**	164	165	157

* FoM_{s1} = DR+10log(BW/Power); **FoM_{s2} = SNDR+10log(BW/Power);

Table 3.1 Performance comparison

3.5 Summary

A noise shaping SAR ADC with on-chip digital DAC calibration was proposed and implemented. Correlated double sampling (CDS) and correlated level shifting (CLS) are combined in the proposed architecture. With these two techniques, the design specifications for the op-amp used in integrator are relaxed. CDS minimized the effect of DC offset and flicker noise from the op-amp, and CLS boosted the effective DC gain of the op-amp. Therefore, the total power consumption of op-amp can be decreased by about 50%. Also, an incremental ADC (IADC) based on-chip DAC calibration scheme is proposed and implemented. The proposed calibration scheme shares all blocks in the proposed NS SAR ADC, so it will not increase the complexity of the circuitry. The calibration gives a more than 13dB improvement in the SNDR. The proposed ADC was fabricated in 130nm CMOS technology. It achieved 85.1 dB DR, 82.6dB SNDR and 90.9dB SFDR with 32 OSR. It consumes 40uW power from 1.6V power supply which gives a 163dB Schreier Figure of Merit (FoMs) which is as good as other similar architecture ADCs.

4 Conclusions

Many wearable devices are used in people's daily life now. There are more functions that can be done with these devices, such as monitoring health. In these devices, sensors play a key role to acquire and communicate data between the outside world and the inside of devices. These sensors need very power-efficient and high-performance ADCs to process data. Noise-shaping SAR ADCs are getting more popular because they combined the traditional SAR ADC operation with noise-shaping scheme is borrowed from Delta-sigma ADCs. Compared to Delta-sigma ADCs, active noise-shaping SAR ADC can achieve the same noise attenuation effects, but the NS SAR ADC has simpler operation algorithm. Moreover, an active NS SAR ADC has flexible noise transfer function selection compared with passive NS SAR ADC. The power consumption of the integrator op-amp is the major limitation for low power application, so special design considerations and techniques are proposed to address this issue.

In Chapter 2, a first-order active NS SAR ADC with a two-capacitor (2-C) DAC is presented. 2-C DAC reduces the capacitance spread and relaxes the reference buffer design. An ideal first order noise shaping NTF was achieved by using active integrator. The ADC was fabricated in a 180nm CMOS technology. The prototype occupies 0.25mm^2. For a 2kHz signal bandwidth, it achieved 78.9dB SNDR and 87.6dB SFDR with a 32-oversampling ratio (OSR). It consumes 74.2 uW power from 1.5V power supply.

Chapter 3 presents an improved NS SAR ADC with on-chip DAC calibration. The implemented calibration shared all circuit blocks used in normal operation, and hence does not increase the complexity and power of the proposed ADC. With the calibration,

it gives a more than 13dB improvement of the SNDR. The proposed ADC was fabricated in 130nm CMOS technology. It achieved 85.1 dB DR, 82.6dB SNDR and 90.9dB SFDR with 32 OSR. It consumes 40uW power from 1.6V power supply which gives a 163dB Schreier Figure of Merit (FoMs) which is as good as other similar architecture ADCs'.

References

[1] A. Agnes, E. Bonizzoni, P. Malcovati and F. Maloberti, "A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with Time- Domain Comparator," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2008, pp. 246-610.

[2] M. Saberi, R. Lotfi, K. Mafinezhad and W. A. Serdijn, "Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters Used in Successive Approximation ADCs," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1736-1748, Aug. 2011.

[3] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 9.35-ENOB 14.8 fJ/conv.step fully-passive noise-shaping SAR ADC," in *IEEE Symp. VLSI Circuits Dig.*, June 2015, pp. C64-C65.

[4] J. Fredenburg and M. Flynn, "A 90-MS/s I1-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2012, pp. 468-470.

[5] L. Shi, Y. Zhang, Y. Wang, M. Kareppagoudr, M. Sadollahi and G. C. Temes, "A 13b-ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 153-156.

[6] C. -. Chen, Y. Zhang, J. L. Ceballos and G. C. Temes, "Noise-shaping SAR ADC using three capacitors," in *Electronics Letters*, vol. 49, no. 3, pp. 182-184, 31 Jan. 2013.

[7] W. Guo, and N. Sun, in *ESSCIRC Conference*, 2016, pp. 249-252.

[8] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, "Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers," in *IEEE Transaction on Circuits and Systems I*, vol. 51, no. 2, pp. 275-285, 2004.

[9] R. Schreier and G. Temes, "Understanding Delta-Sigma Data Converters," in *1st ed. Hoboken, NJ: John Wiley and Sons, Inc*, 2005.

[10] H. Ghaedrahmati, J. Zhou and L. Shi, "Gain-boosted Complementary Dynamic Residue Amplifier for a 160 MS/s 61 dB SNDR Noise-Shaping SAR ADC," in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 141-144.

[11] H. Klar, "Integrierte digitale schaltungen MOS/BICMOS," in *Springer*, Berlin, 1996.

[12] V. Srinivas, S. Pavan, A. Lachhwani, N. Sasidhar, "A Distortion Compensating Flash Analog-toDigital Conversion Technique," in *IEEE. J. Solid-State Circuits* , 1959-1969.

[13] C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Auto-zeroing, correlated double sampling, chopper stabilization," in *Proc. IEEE,* vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[14] R.Gregorian, "Introduction to CMOS Op-Amps and Comparators," in *John Wiley & Sons*, 1999.

[15] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΣΔ modulator with 88-dB dynamic range using local switch bootstrapping," in *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, Mar. 2001.

[16] S. Saisundar, J. H. Cheong and M. Je, "A 1.8V 1MS/s rail-to-rail 10-bit SAR ADC in 0.18μm CMOS," in *2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Singapore, 2012, pp. 83-85.

[17] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel and R. Thewes, "A 0.7-V MOSFET-only switched-opamp /spl Sigma//spl Delta/ modulator in standard digital CMOS technology," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1662-1669, Dec. 2002..

[18] B. Gregoire and U. Moon, "An Over-60 dB True Railto-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain," in *IEEE Journal of Solid-State Circuits*, 2008, vol.43, no.12, pp.2620,2630.

[19] Y. Zhang, C.H. Chen, T. He, and G. C. Temes, "A 35μW 96.8dB SNDR 1 kHz BW multi-step incremental ADC using multi-slope extended counting with a single integrator," in *Proc. IEEE Symp. VLSI Circuits*, pp. 24-25, June 2016.

[20] C.-H. Chen, Y. Zhang, T. He, P. Chiang and G. C. Temes, "A micro-power two-step incremental analog-to-digital converter," in *IEEE J. Solid-State Circuits*, vol.50, no. 8, Aug. 2015.

[21] J. Zheng, W. Ki and C. Tsui, "A Fully Integrated Analog Front End for Biopotential Signal Sensing," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3800-3809, Nov. 2018.

[22] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "Nested-current-mirror rail-to-rail-output single-stage amplifier with enhancements of DC gain, GBW and slew rate," in *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2353–2366, Oct. 2015.

[23] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," in *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 12, pp. 906-917, Dec. 2003.

[24] Yun-Ti Wang and B. Razavi, "An 8-bit 150-MHz CMOS A/D converter," in *Proceedings of the IEEE 1999 Custom Integrated Circuits Conference (Cat. No.99CH36327)*, San Diego, CA, USA, 1999, pp. 117-120.

[25] T. Kim and Y. Chae, "A 2MHz BW Buffer-Embedded Noise-Shaping SAR ADC Achieving 73.8dB SNDR and 87.3dB SFDR," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, USA, 2019, pp. 1-4.

[26] C. Chen, Z. Tan and M. A. P. Pertijs, "A 1V 14b self-timed zero-crossing-based incremental ΔΣ ADC," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, 2013, pp. 274-275..

[27] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-V 140-μ/W 88-dB audio sigma-delta modulator in 90-nm CMOS," in *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.