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Siyuan Chen for the degree of Master of Science in Electrical and Computer Engineering presented on December 04, 2018.

Title: A 400Mb/s 850nm FSO Link based on CMOS Integrated Receiver for Hybrid WiFi and Optical Femtocells

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Arun Natarajan

The increasing demand for higher data-rates is challenging to satisfy with spectrum-deficient indoor WiFi networks. A novel hybrid WiFi Free-Space Optical (WIFO) system has been proposed to enhance the wireless capacity of indoor WiFi networks. In this thesis, an integrated optical wireless receiver is designed and integrated in 65-nm CMOS technology as a part of the hybrid WIFO network. Signal-to-noise (SNR) at trans-impedance amplifier(TIA) output is increased due to correlated signal addition while noise from different TIA is uncorrelated. A distributed TIA array structure with four Si-PIN photodiodes is introduced to improve SNR by 6dB, each with a capacitance of 1.6pF and sensitivity of 0.4A/W at 850nm wavelength. Simulations suggest an input-referred current noise of 12nA (with 200 MHz integration BW). The receiver and a low cost FSO transmitter using commercial off-the-shelf components, achieve 400 Mb/s data rates at distances beyond 1m. The receiver consumes 80 mW from a 1.2V supply.

A 400Mb/s 850nm FSO Link based on CMOS Integrated Receiver for Hybrid WiFi and Optical Femtocells

by

Siyuan Chen

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

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Siyuan Chen, Author

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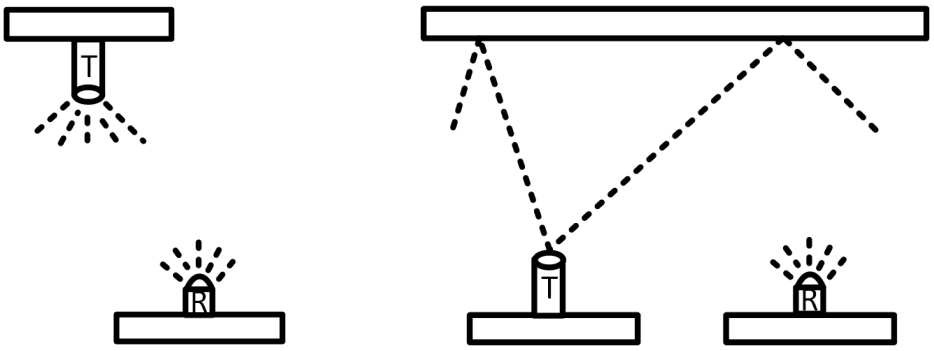
Chapter 1: Introduction

Nowadays, wireless communication devices such as cellphones, tablets and laptops fully occupy people's daily life. The growth of these devices and anywhere-anytime connectivity has led to increasing demand for a high speed and stable wireless local area network (WLAN), especially in crowded places, such as airport terminals, offices, and in homes where several people have multiple wireless devices sharing the same network. Due to the wireless capacity limitation, the speed can be very low in high volume occasions. As a result, there is a demand to provide a high bandwidth and easy accessibility WLAN. There are two major technologies to realize WLANs, radio frequency (RF) technology and millimeter-wave systems, such as Wireless high-speed Internet (Wi-Fi), which is now most commonly used, and optical wireless technology.

Wi-Fi is the currently the most mature indoor wireless communication system, which can provide a easy accessibility, high mobility wireless network and can be also used as an widely available RF energy sources at low cost [1], [2], [3]. The Wi-Fi network operation ranges are 2.412-2.483 GHz and 5.18-5.24 GHz frequencies, which are quite limited. The bandwidth for each channel is even lower with different Wi-Fi standards. Wi-Fi throughput is used to define the actual data per device can get. It depends on the the real transmission rates and local conditions, such as the average packet size, the distance to the access point and the number of users per access point. For example, assuming the typical data rate of IEEE 802.11.ac is 866.7 Mb/s and there are six devices using the same access point, each device can only get one sixth of the channel capacity when near the access point, about 145 Mb/s. This will be decreased by lower rates if more devices are sharing this access point. Additionally, the interferences between different networks on the same channel further degrade the channel capacity. That is, the performance of Wi-Fi is highly reduced in crowded public places, such as airports, libraries and so on.

Optical wireless (OW) communication system is another way to realize a wireless LAN. It has many advantages compared with Wi-Fi system, such as large bandwidth, unregulated spectrum, and immunity towards electromagnetic interference [4]. It also has an obvious disadvantage, poor mobility. OW communications can be categorized in



(a) Line of sight system (b) Diffuse system

Figure 1.1: Optical wireless communication system

two groups, the line of sight system (LOS) and the diffused system and [4], shown in Fig. 1.1 . The direct LOS system employs a narrow laser beam to establish a point-to-point transmission link between the transmitter and receiver [5]. The transmission data rate of LOS system can easily go up to several Gb/s without suffering from bandwidth limitation and it is high power efficiency. But, the mobility of LOS is quite poor because of its point to point transmission characteristic. Therefore, the transceivers can only achieve a small effective area even in a very strict alignment condition, which makes the range of LOS system quite limited. The latter one uses diffused beam generated by different reflecting surfaces to cover the entire service area and provides mobility functionality to subscribers [5]. However, it is very low power efficiency. The diffused system also suffers from multi-path distortion due to the different arriving time to the receiver and the transmission bit rate is limited.

To solve the wifi capacity limitation, a novel model hybrid WiFO system is proposed by taking advantage of both Wi-Fi and optical wireless system. The objective of such an approach is to provide a high data downlink connectivity through a FSO link when user is within deployed FSO cones, while lower data rate uplink is provided over WiFi [6]. In addition, seamless transition to WiFi is ensured when user moves outside the light cones. Such connectivity is particularly relevant for deployment in public spaces with large number of users sharing limited spectrum. The system uses inexpensive components to send data at 100 Megabits per second (Mb/s). In prior work[7], a 50 Mb/s data rate per user without sacrificing mobility through the use of FSO-based femtocells has been

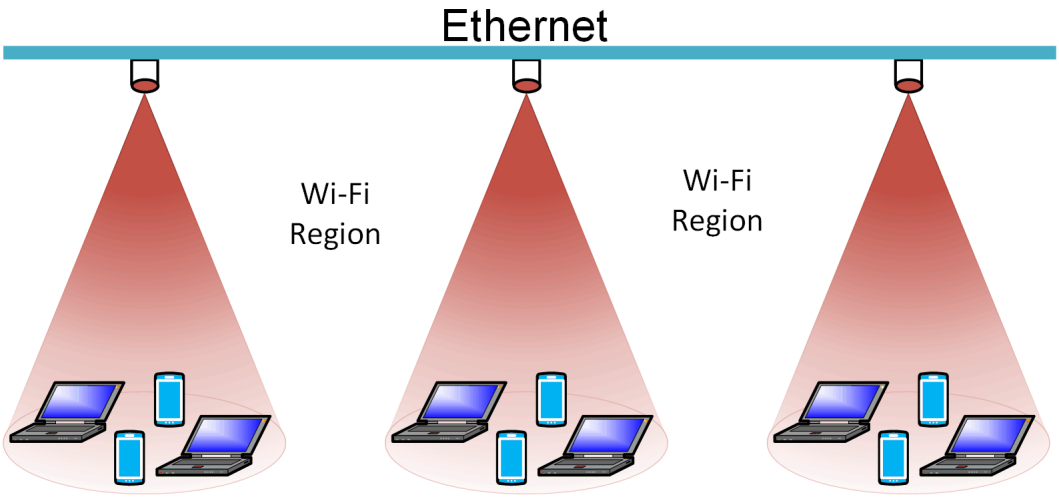


Figure 1.2: Proposed WiFO scheme that combines WiFi and Free-space Optical (FSO) links

demonstrated. Even though a similar data rate can be provide by the current WiFi systems, it has to be shared by several wireless devices, which reduces the data rate for each device. In a crowded place, as the number of the devices increase, the data rate per user decreases much lower. However, this hybrid system can evenly deliver 50 Mb/s to each user. This thesis focuses on the physical implementation of an integrated low-cost FSO receiver with higher data rate, which is critical for such applications as shown in Fig. 1.3. In this work, increasing the optical range and bandwidth is the key point for

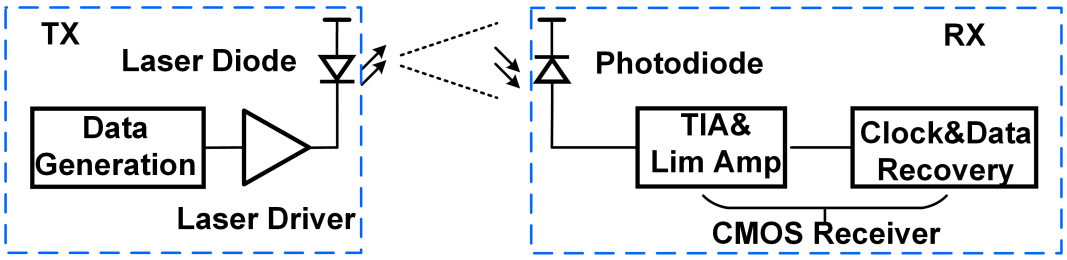


Figure 1.3: System level figure

optical link mobility consideration. There are two major ideas used in this design, First, propose a innovation design our-element TIA array to improve the noise performance

by 6dB with out sacrificing the bandwidth and.Second, design a high gain and very low noise TIA.

The thesis is organized as follows. Chapter 2 outlines existing free space optical communication system structures. Chapter 3 describes the transmitter design and analysis the receiver design in system level. Chapter 4 implements the low-noise front-end optical receiver design in 65 nm CMOS and presents the simulation and measurement results.

Chapter 2: Prior works

Free-space optical channels have attracted a lot of interests in indoor communication system design. Many works related to increasing the range and region of optical link has been published. The hybrid system in [8] employs orthogonal frequency division multiplexing (OFDM) in the visible light spectrum to achieve a data rate of 75 Mb/s over a range of 2 m. The structure in [9] uses post-equalization circuit to implement a VLC system to achieve 340 Mb/s with 43 m with BER $> 2 \times 10^{-3}$. The optical system described in [7] uses WiFi and FSO together to achieve seamless connectivity to get data rate up to 50Mb/s over a distance of 3 m with BER $> 1 \times 10^{-4}$, which is a previous version of our project. All these works do not provide any integrated chip solutions. Additionally, VLC systems must deal with interference when deployed in hard-to-control real-world environments such as airports and stadiums. Moreover, VLC systems always suffer from the slow response of the LED transmitter, which means a lower bandwidth. The bidirectional optical system in [10] also modulates visible light

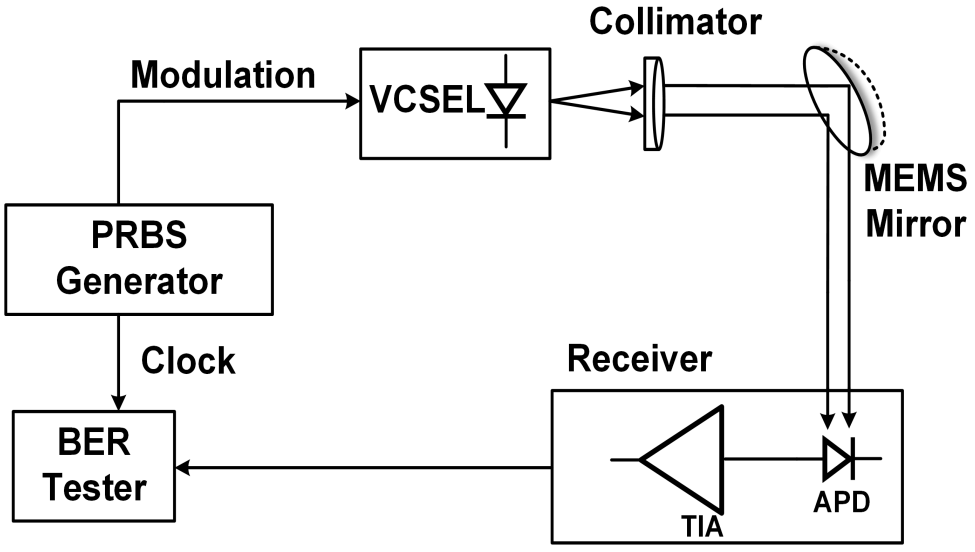


Figure 2.1: Block diagram for measurement setup of the optical wireless system in [12]

to get data rates of 250 Mb/s in uplink and downlink channels. Notably, this work uses avalanche photodiodes (APD), that require high bias voltages, and complex multi-tone modulation schemes to overcome limited analog bandwidth.

Another approach [12] is shown in Fig. 2.1. It achieves a 1 Gbit/s data rate with a sensitivity of -31.8 dBm at a $BER < 10^{-9}$. This paper focused on using high sensitivity APD and adaptive beam steering techniques with MEMS based mirrors to improve the sensitivity of the receiver. However, APD needs a high bias voltages to reach the ionization energy, which makes it difficult to integrate the APD in advanced CMOS technologies that can lower power consumption but have low breakdown voltages. In [13], a data rate of 10 Gb/s is achieved over a range of 2 m. In both of these papers, sophisticated MEMS based mirrors are used to steer the highly focused transmitter output, reducing loss in the optical power and thus, improving the range of the system without increasing the sensitivity of the receiver. Incorporating such approaches in low-cost portable electronics is challenging.

Chapter 3: System Level design

In this chapter, the system design of the optical wireless receiver with a data rate of 400 Mb/s is described in details. Section 3.1 outlines the basic optical receiver model. Section 3.2 describes the transmitter design and the optical photodiode used in the receiver. The transmitter is major designed by Spencer Liverman. Only a brief description and the measurements are provided. Section 3.3 analyses the noise of the system and allocates the design specifications to each stage. Section 3.4 proposes a four-element TIA array structure.

3.1 Basic Optical Receiver Model

An optical receiver is used to sensing the optical input signal and translate the data received. It typically consists of three parts, a photodiode, a trans-impedance amplifier (TIA) and a cascade of main amplifiers (MAs)[14]. The photodiode detects the light and converts the light signal into a current proportional to the power received. The TIA transfers the current signal to voltage signal and the MAs amplify the TIA output voltage to desired signal level and drive the following decision circuits. The receiver model is shown in Fig. 3.1. The decision feedback equalizer (DFE) block adopts feedback to reduce the intersymbol interference caused by the limited bandwidth of the optical channel. The receiver's performance is governed by the Photodiode and TIA.

3.2 Optical transmitter laser diode and receiver photodiode

The transmitter mainly comprises two parts, a laser diode and a laser driver, shown in Fig. 3.2 . The model of the laser diode is LCU85C051A [15] and the laser driver model is ATF-511P8. The transmitter is target to realize 1GHz modulation signal. But the data rate can only go up to 400 Mb/s in measurements. Data is transmitted in on-off keying modulation. To get the optimum bias point of the transmitter, the forward current was measured by sweeping the bias voltage. The measurements are shown in

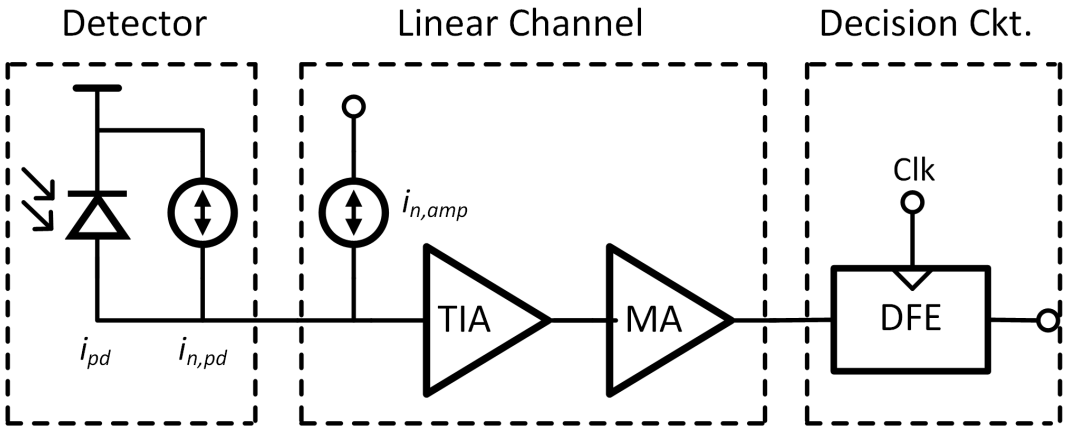


Figure 3.1: Basic optical receiver model

Fig. 3.3. The maximum bias voltage was set by checking the max current allowed with the corresponding maximum power. The minimum bias voltage was limited by the switching speed of the laser driver. As the consideration of maximum power amplitude, the transmitter is biased at 1.05V and the signal peak to peak voltage amplitude is 200 mV.

The transmitter power was biased with this setting, and the measurements are shown in Fig. 3.4. The power was calculated by measuring the current of the photo detector which will be described in next section, and then divided it by the photodiode responsivity. To be consistent with the following sensitivity calculation, the photo detector was used to sense the power because the detecting area of power meter is much larger than that of the photo detector. The power was decreased by more than 95% when the distance is over 1 meter.

Table 3.1: Photodiode S5973 specifications

Reverse voltage	3.3 V
Responsivity	0.32 A/W
Dark current	1pA
Bandwidth	1GHz

The optical photodiode used in the receiver is S5973 [16] . It's a high speed Si PIN photodiode. The specifications of the photodiode are listed in Table 3.1. The noise

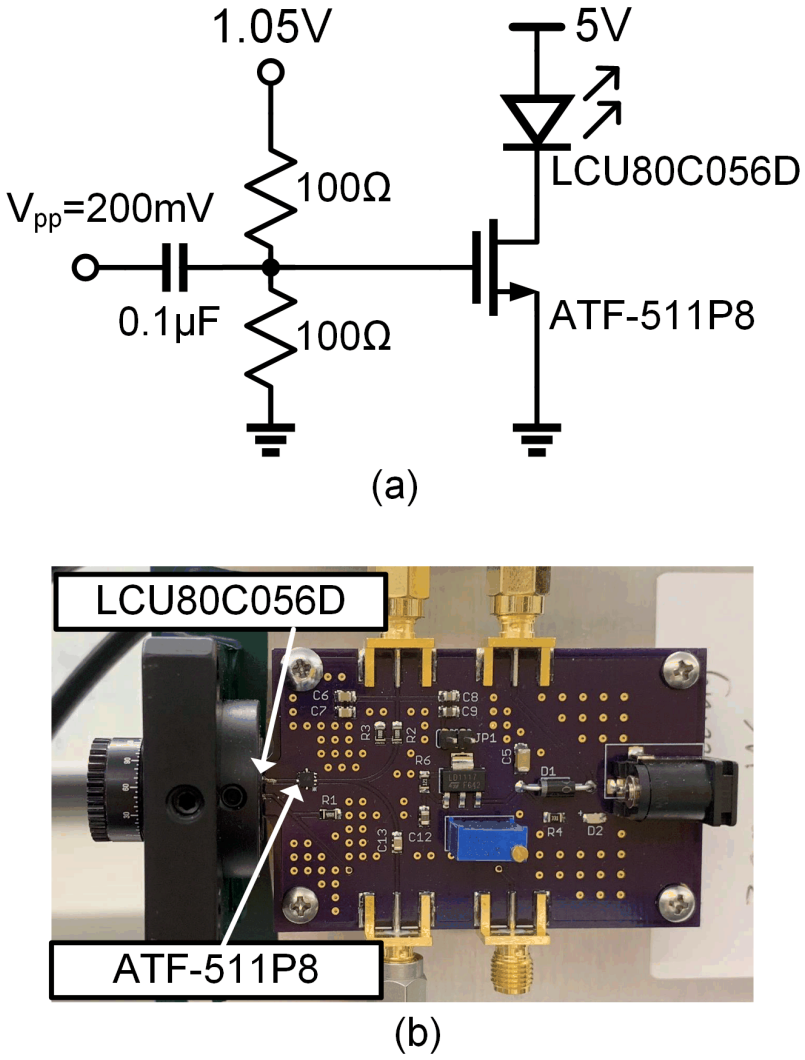


Figure 3.2: (a) Schematic and (b) implementation of 300mW 850nm IR transmitter.

current of the photodiode known as shot noise can be calculated:

$$\bar{i}^2_{n,PIN} = 2qI_{PIN}BW_n \tag{3.1}$$

where I_{PIN} is the signal current and BW_n is the noise bandwidth. The photodiode noise is input signal current dependent and proportional to square root of it, so the

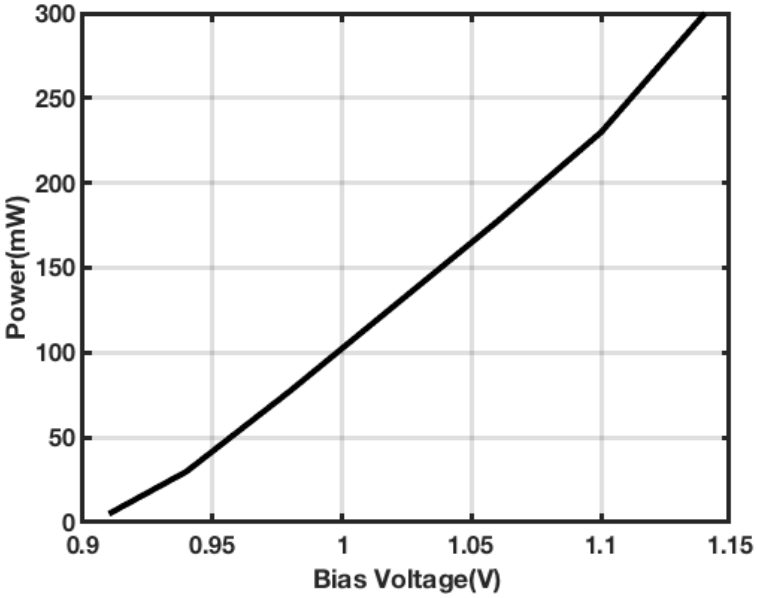


Figure 3.3: Optical transmitter current vs. voltage bias

minimum noise current set the limitation. Assume the average signal current is 2 uA, the photodiode generates a shot-current noise of 35.8 nA with 1 GHz bandwidth. The dark current noise 1 pA can be ignored compared with the shot noise. The values are reasonable based on the power measurements in transmitter section.

3.3 Receiver noise analysis

In this section, the input sensitivity is discussed, and then noise requirements are derived. The optical receiver sensitivity is the minimum signal power need to achieve a desired BER. The parameter used to evaluate BER is personic Q. It is the ratio between signal and noise current, defined as equation 3.3 [17]. For gaussian distribution,

$$BER = \int_{Q}^{\infty} Gaussiandx \tag{3.2}$$

$$Q = \frac{i_s^{pp}}{2i_{n,rms}} = \frac{P_s^{pp}}{2Ri_{n,rms}} \tag{3.3}$$

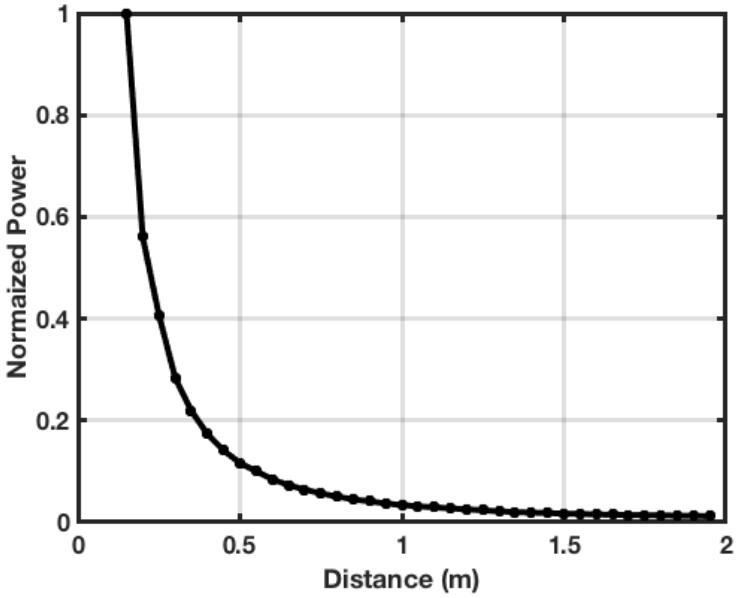


Figure 3.4: Transmitter power vs. distance

where i_s^{pp} is the input peak to peak signal current, $i_{n,rms}$ is the input referred rms nosie and R is the photodiode responsivity.

Table 3.2: Numerical relationship between BER and Q

BER	Q	BER	Q
10^{-3}	3.090	10^{-8}	5.612
10^{-4}	3.719	10^{-9}	5.998
10^{-5}	4.265	10^{-10}	6.361
10^{-6}	4.753	10^{-11}	6.706
10^{-7}	5.199	10^{-12}	7.035

This optical receiver is targeted to achieve 10^{-4} bit error ratio over a 2 meter distance with 2Gb/s data rate. The numerical relationship between BER and Q are listed in Table 3.2 [17]. To give some design margin, Q greater than 4.265 should be achieved for $BER > 10^{-5}$. Based on equation 3.3 and the power distribution of the transmitter, the input referred rms noise can be calculated. The signal current of '0' can be assumed to 0 uA because the power is very low in sensitivity derivation, so $i_{dc} = i_s^{pp}/2$.

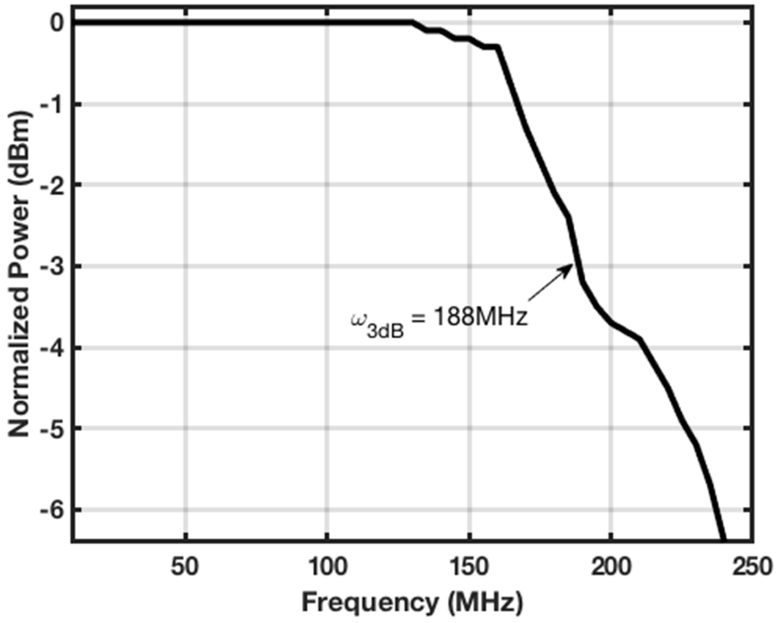


Figure 3.5: Measured transmitter bandwidth

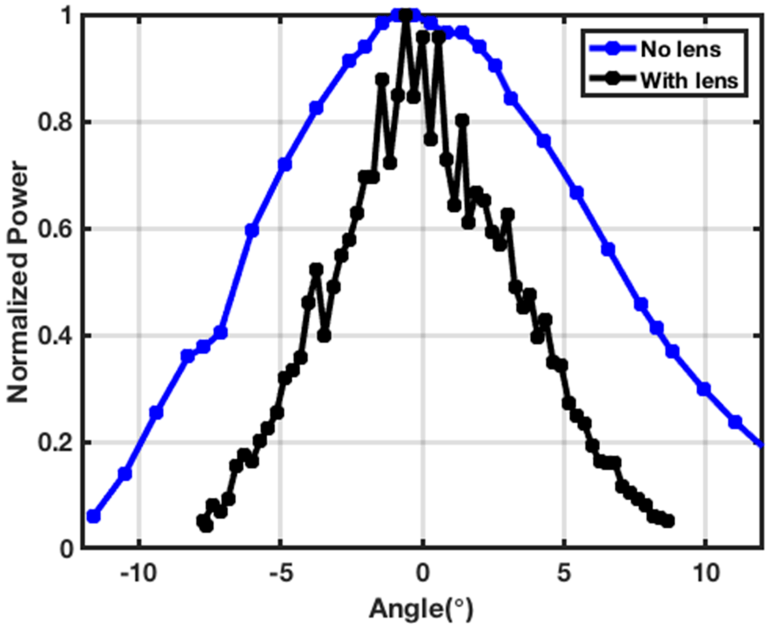


Figure 3.6: Measured transmitter power vs. angle

The receiver noise comes from two parts, the photodiode noise and the TIA noise. The photodiode noise is 36 nA when the incident current is 2 uA. The TIA noise in a 1 GHz bandwidth with large photodiode capacitance is usually much larger that, which means the receiver noise is mainly contributed by the TIA when roughly calculating the input sensitivity. Here, other non ideal effects such as the noise from the following stages are ignored because of the high gain of TIA block.

3.4 Four-element TIA array structure

While there are numerous TIA topologies, the shunt feedback TIA is mostly used because of its excellent gain and noise performance. The basic shunt feedback TIA with major noise contributors is shown in Fig. 3.7. $\overline{i_n^2}$ represents the input referred current noise of TIA, which includes the current noise of photodiode $i_{n,pd}^2$, feedback resistor i_{n,R_f}^2 and voltage noise of feed forward amplifier $v_{n,amp}^2$.

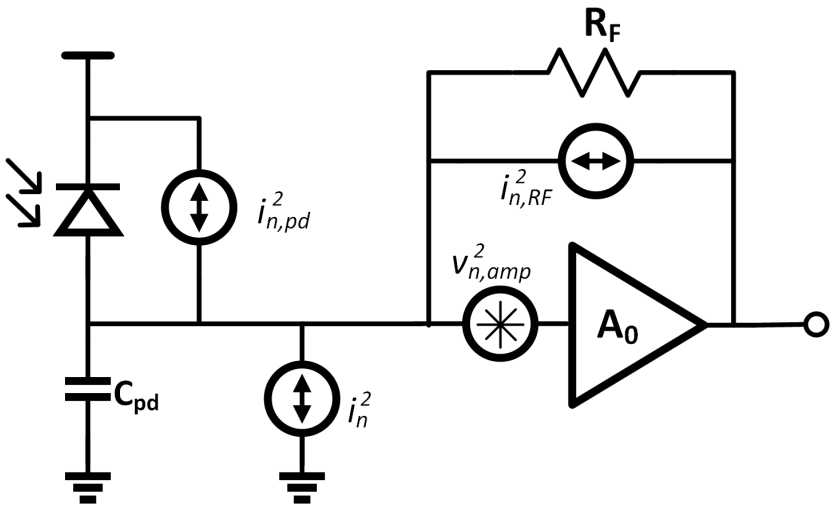
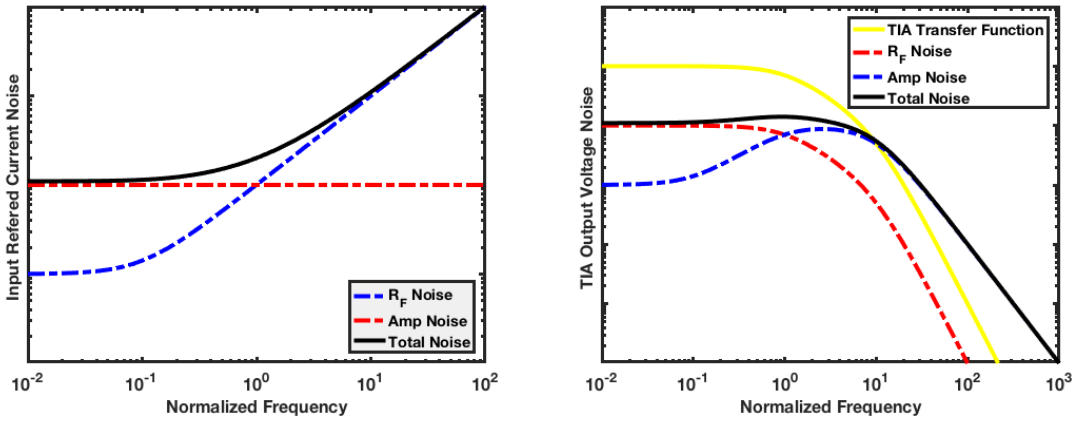


Figure 3.7: Simplified receiver model with noise contribution

In a simple analysis that the feedback amplifier is ideal with an infinite bandwidth, the trans-impedance transfer function can be calculated as

$$Z_T(s) = -R_T \frac{1}{1 + s/\omega_p} \tag{3.4}$$



(a) Input referred current noise (b) Output voltage noise

Figure 3.8: TIA noise power spectrum density

where the dc trans-impedance R_T is equal to $R_F A_0/(1+A_0)$, and the only pole frequency ω_p is $(1+A_0)/R_F C_T$. C_T includes the parasitic capacitor of the photodiode and input capacitor of the TIA. The bandwidth is increased $(1+A_0)$ times because the input resistance is $(1+A_0)$ times smaller than R_F.

The impact of finite TIA bandwidth must be accounted if the data rate is much higher and comparable with the bandwidth of the feedback amplifier. The ideal amplifier is modified as an amplifier with a single dominant pole ω_A. The amplifier transfer function is $A_0/(1+s/\omega_0)$. The trans-impedance transfer function is modified as

$$Z_T(s) = -R_T \frac{1}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \tag{3.5a}$$

$$w_0 = \sqrt{\frac{(1+A_0)\omega_A}{R_F C_T}} \tag{3.5b}$$

$$Q = \frac{\sqrt{(1+A_0)\omega_A R_F C_T}}{1 + R_F C_T \omega_A} \tag{3.5c}$$

For maximally fat frequency response, which is also called Butterworth response, $Q =$

$1/\sqrt{2}$, the TIA bandwidth BW_{3dB} is equal to $\omega_0/2\pi$ and can be calculated as

$$BW_{3dB}(s) = \frac{1}{2\pi} \times \frac{\sqrt{2A_0(A_0+1)}}{R_F C_T} \approx \frac{\sqrt{2}A_0}{2\pi R_F C_T} \tag{3.6}$$

Compared with infinite bandwidth amplifier case, the shunt feedback TIA bandwidth is increased by $\sqrt{2}$.

The input referred noise of the shunt feedback TIA is given by,

$$\overline{i_n^2}(f) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2}(1 + sR_F C_T)^2 \tag{3.7}$$

Where, gm is the transconductance of the input transistor of TIA. The first part is caused by the feedback resistor R_f. The second part is the noise contribution of the voltage amplifier, and exists a zero at $1/2\pi R_f C_T$, which is $\sqrt{2}A_0$ times smaller than the bandwidth of TIA. This expression plot versus frequency is shown in Fig. 3.8.

There are some inherent tradeoffs between the bandwidth, gain and sensitivity design of receiver. The receiver's sensitivity is mainly determined by the diode responsivity and the noise of the TIA. Increasing diode area to increase diode responsivity leads to larger diode capacitance, C_{PD}, which limits overall bandwidth. Increasing R_F can be also applied to reduce the noise of TIA, but this also reduces the low-frequency transconductance in the TIA and limits the bandwidth.

To further release the constraints between these design factors, a novel structure with four-element TIA array is proposed and shown in Fig. 3.9. Four photodiodes PD_1, PD_2, PD_3 and PD_4 drive four TIAs. Each TIA can be individually enabled/disabled. C_1, C_2, C_3 and C_4 are used to decoupling the dc current. A dummy TIA stage is added to generate the reference voltage used as the other input for all the differential trans-conductances G_m. Trans-conductances blocks and the programmable resistors R_{sum} consist of the summing up stage. The TIA outputs drive one input of the differential summing stage where the currents from each TIA are combined into the load resistors. Programmable-load resistors R_{sum} are used to adjustment of DC offsets and gain control. The output of the summing stage drives a limiting amplifier for subsequent digitization.

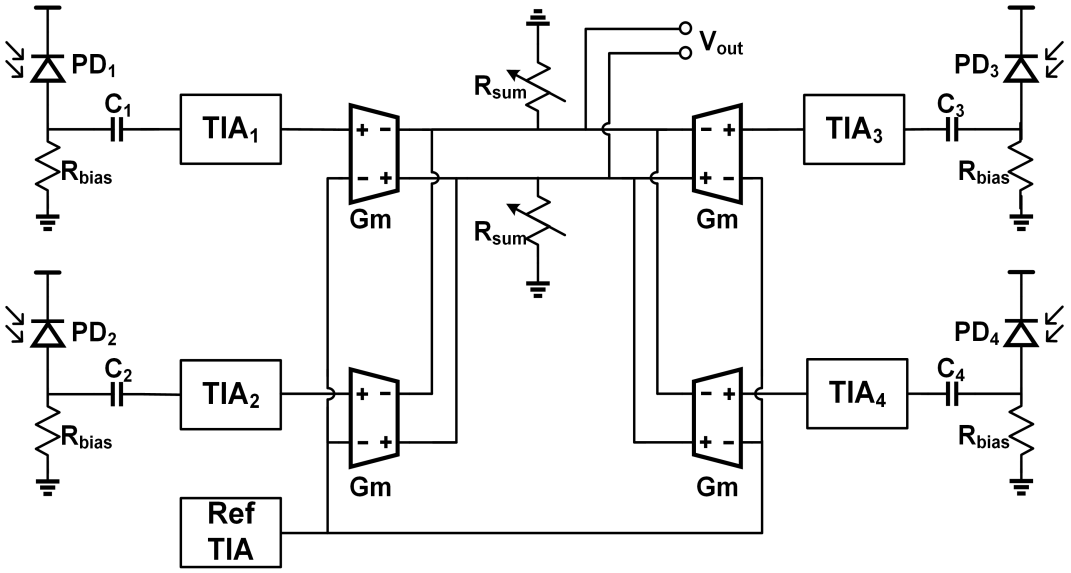


Figure 3.9: Receiver architecture with four-element TIA array

The signal-to-noise ratio(SNR) at the output of each TIA can be expressed as,

$$SNR_{TIA} = \frac{v_{sig}}{\sqrt{v_{n,out}^2 + v_{n,ref}^2}} \tag{3.8}$$

where, $v_{n,out}$ is the output noise of each TIA, $v_{n,out}$ is the output noise of reference TIA, and v_{sig} is the output signal of each TIA. The reference TIA is used to provide a reference voltage to convert single ended TIA signal to a differential output. Even though the dummy TIA contributes extra noise, it is necessary to create a differential output to immune the common noise. Moreover, the noise of it can be set as much lower than the four TIAs array by removing the feedback resistor and adding a filtering capacitor. Hence, it can be ignored.

The noise from each TIA is uncorrelated at the summing stage while the input signals are correlated, thereby improving the signal-to-noise ratio.The SNR with TIA array is given as,

$$SNR_{4TIA} = \frac{4v_{sig}}{\sqrt{4v_{n,out}^2 + 16v_{n,ref}^2}} = \frac{4v_{sig}}{\sqrt{4v_{n,out}^2}} = 2SNR_{TIA} \tag{3.9}$$

By comparing this two equations, we can get that the proposed four-element TIA array improves the SNR by 6dB and ensures wide bandwidth and high responsivity concurrently.

Chapter 4: Circuits Implementation and Results

In this chapter, the implementation and measurements of the receiver are presented. TIA block and GmR block are described. Some of the circuits was designed by Anindita Borah. The measurements are presented in the last section.

4.1 Trans-impedance Amplifier

Schematic of TIA with the photodiode is shown in Fig. 4.1. The voltage amplifier is implemented using a cascade of three CMOS inverter stages to achieve high gain and bandwidth with a 1.2 V voltage supply. The feedback resistance of the TIA is programmable from 15 kΩ to 90 kΩ. The amplifier simulated gain is around 500, and the low-frequency input resistance of the TIA can be varied from 30 Ω to 180 Ω.

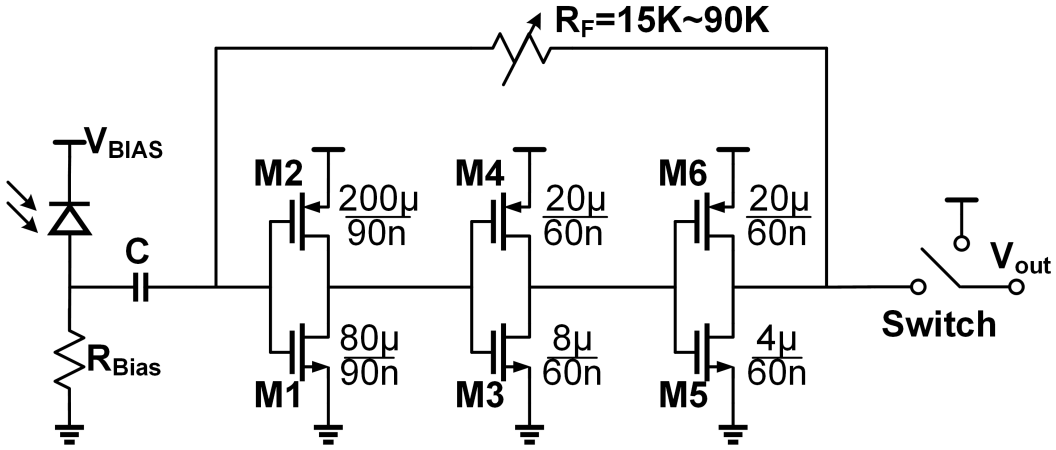


Figure 4.1: Schematic of TIA

The noise of the TIA in equation 3.7 can be rewritten as [13],

$$\overline{i_n^2}(f) = \frac{4kT}{R_F} + \frac{4kT\gamma(2\pi C_T)^2}{g_m} f^2 \tag{4.1}$$

and the integral input referred noise is given as,

$$\overline{i_n^2} = \frac{4kT}{R_F} \times I_1 \mathrm{BW}_{3\,\mathrm{dB}} + \frac{4kT\gamma(2\pi C_T)^2}{g_m} \times \frac{I_2^3}{3} \mathrm{BW}_{3\,\mathrm{dB}}^3 \tag{4.2}$$

where, personick integral numbers I_1 and I_2 equal 1.11 and 1.49 reletively for Butterworth response [14], and $g_m = 2\pi f_T C_{in}$. To minimize the voltage amplifier noise, we can get the optimal TIA input capacitance C_{in} is equal to C_{PD}. But the total noise is relatively flat with the ratio of C_{in}/C_{PD} variation from 0.5 to 1. To reduce the power consumption, the input capacitance of the TIA alone is designed about 900 fF, which only increases TIA noise by 8% compared with the optimal case.

TIA simulated dc gain with default setting feedback resistor 60 kΩ is 95.85 dB and bandwidth is about 584 MHz, shown in Fig. 4.2.

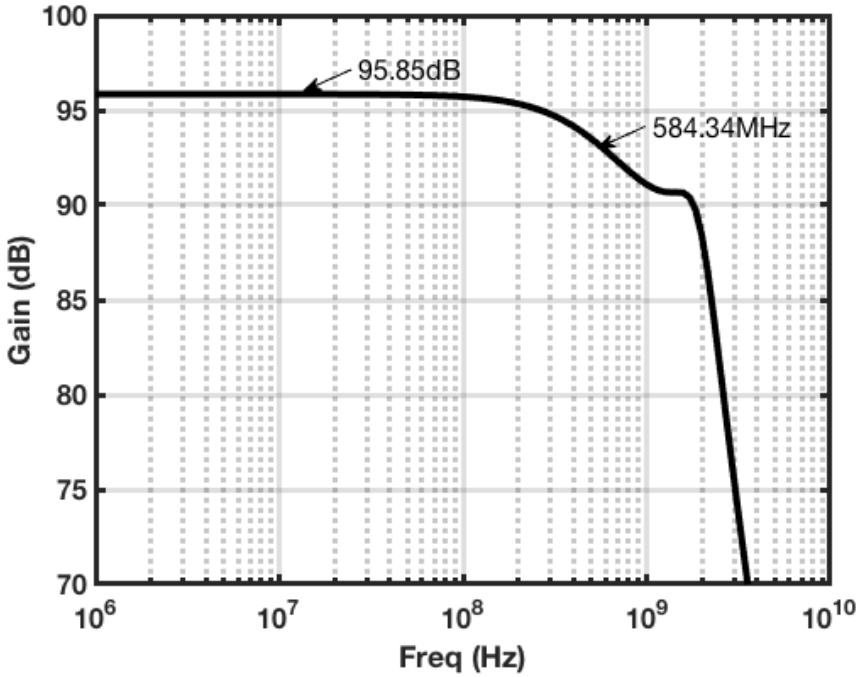


Figure 4.2: Simulated bandwidth of TIA with photodiode

4.2 Summing Stage

The summing stage schematic is shown in Fig. 4.3. The range of the programmable-load resistors R_1 and R_2 is 0.66 kΩ to 6 kΩ, which are used to set the output common voltage and cancel the output mismatch. The gain of this stage is, which is set by the required voltage level.

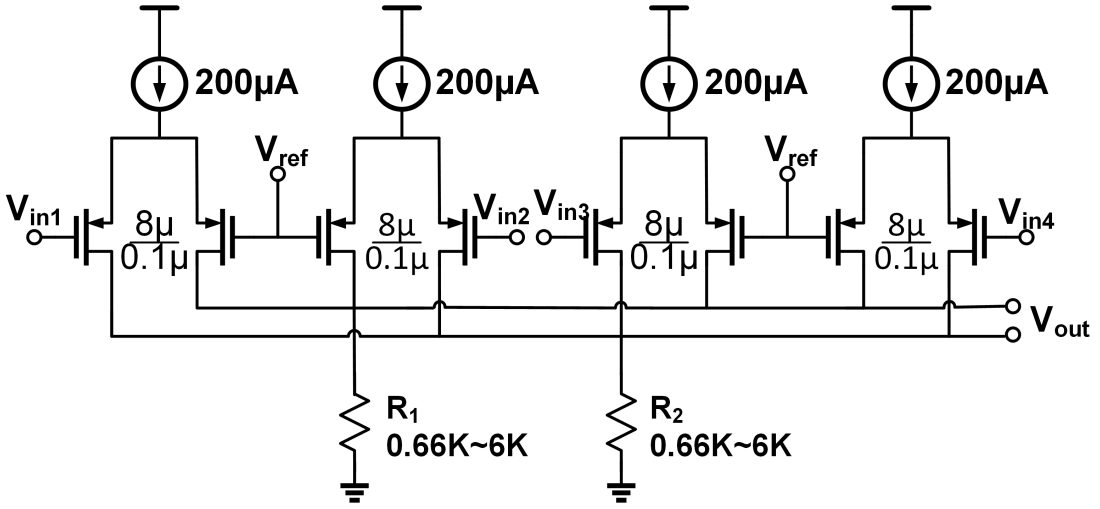


Figure 4.3: GmR sum up stage schematic.

The noise from each TIA is uncorrelated at the summing stage while the input signals are correlated, thereby improving the signal-to-noise ratio. Ideally, this would lead to a 6dB improvement in SNR with a 4 TIA array. However, in our implementation a shared reference path introduces correlated noise reducing improvement. Simulations that exclude this reference path provide expected 6dB higher SNR.

The simulated input-referred noise with 1 TIA, 2 TIA and 4 TIA active for the combined TIA and summing stage is shown in Fig. 4.4, demonstrating improvement without affecting bandwidth. The integrated input-referred noise current up to 200 MHz and 1 GHz RX bandwidth are 14.7 nA and 107 nA respectively.

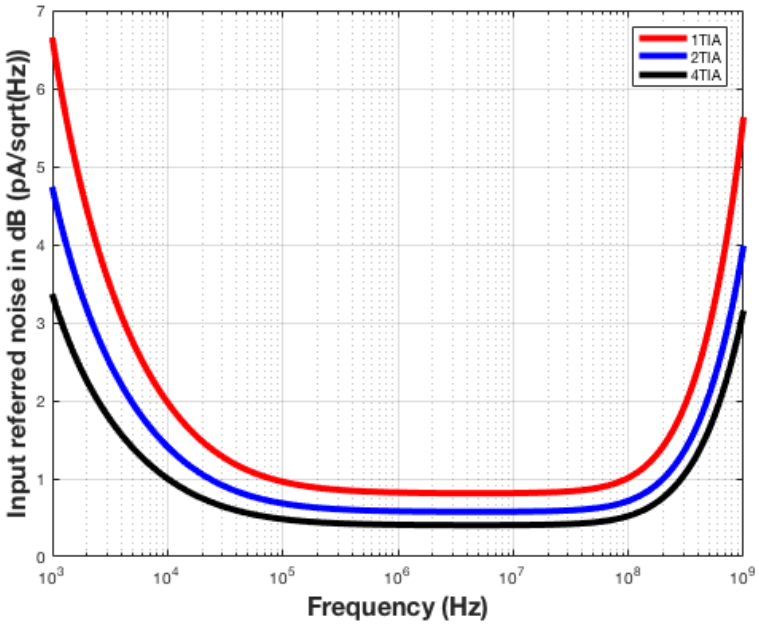


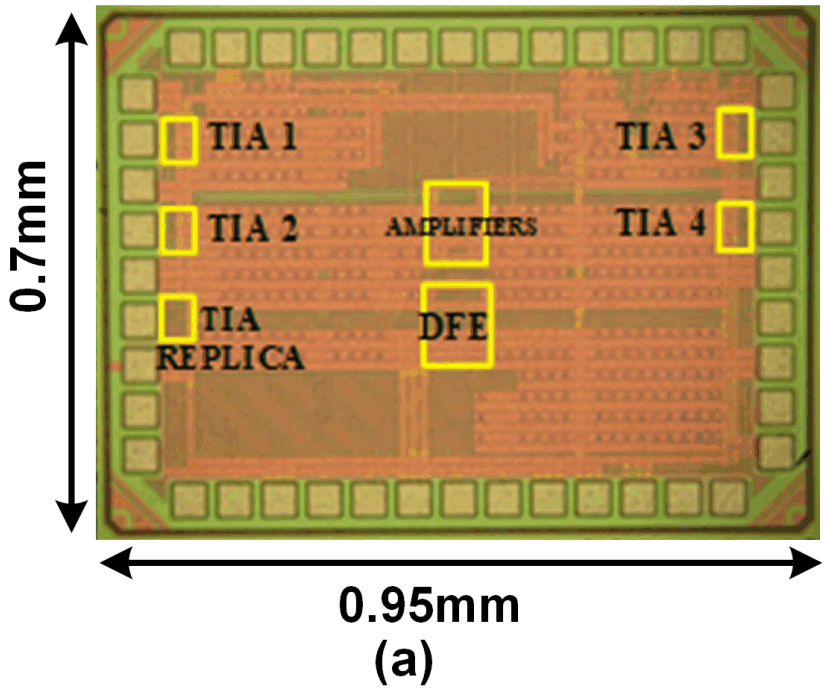
Figure 4.4: Simulated input refer noise

4.3 Measurement Results

The die photo of the implemented IC in 65-nm CMOS is shown in Fig. 4.5 and occupies 0.65 mm^2. The IC is packaged with four Si-PIN diodes corresponding to four TIAs. The measurement setup for the IC is shown in Fig. 4.6. The receiver is placed at a line-of-sight axis with the transmitter. There are two rails in the setup, rail 1 is for the distance test and rail 2 is for the test of viewing angle. The summing output of the receiver's four TIAs array is fed to an off-chip low noise amplifier (LNA) with a gain of 24 dB [20]. The output of the LNA is connected to a Bertscope.

Two receiver configurations were tested. Fig. 4.7 shows measured performance with one and two elements for the transmitter with lens across distance. The RX supports 100 Mb/s for range up to 1.9 m with 2-elements active. Additionally data rates of 400 Mb/s is demonstrated for range $>$ 1 m (Fig. 4.7). The 2-element array shows improvement over 1-element TIA array. The measured eye diagram with 1 TIA active and 2 TIA active for 400 Mb/s data rate are shown in Fig. 4.9 demonstrating improvement in sensitivity

in the array. Measurements without the lens incorporated in the TX at 50 cm distance are shown in Fig. 4.8. The viewing angle was also improved with the improve of the sensitivity. Further measurements with 4-element array is on-going. The analog part of the IC consumes 80 mW from 1.2 V, with 19 mW in each of the TIAs and 19 mW in the reference TIA as well.



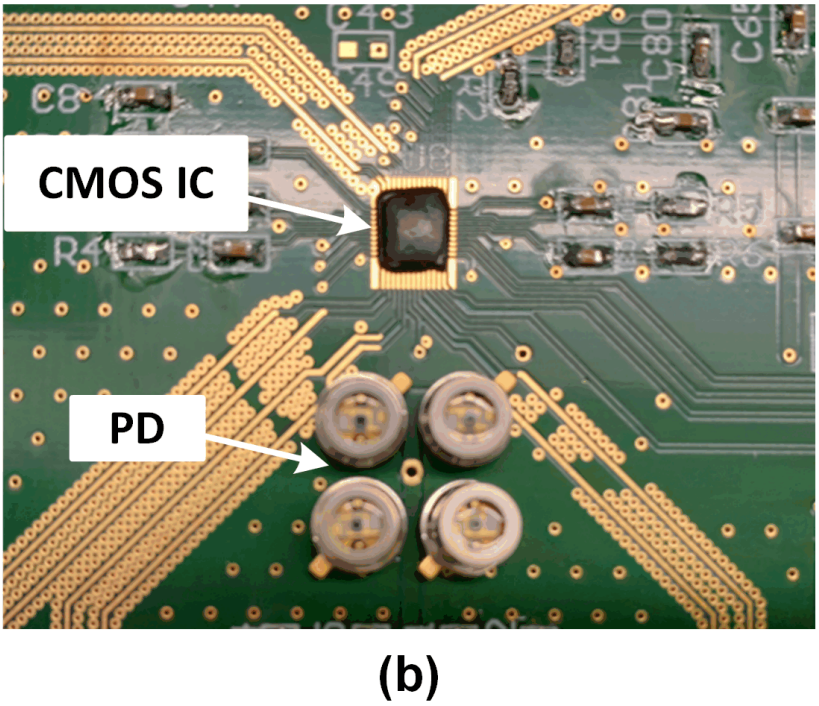
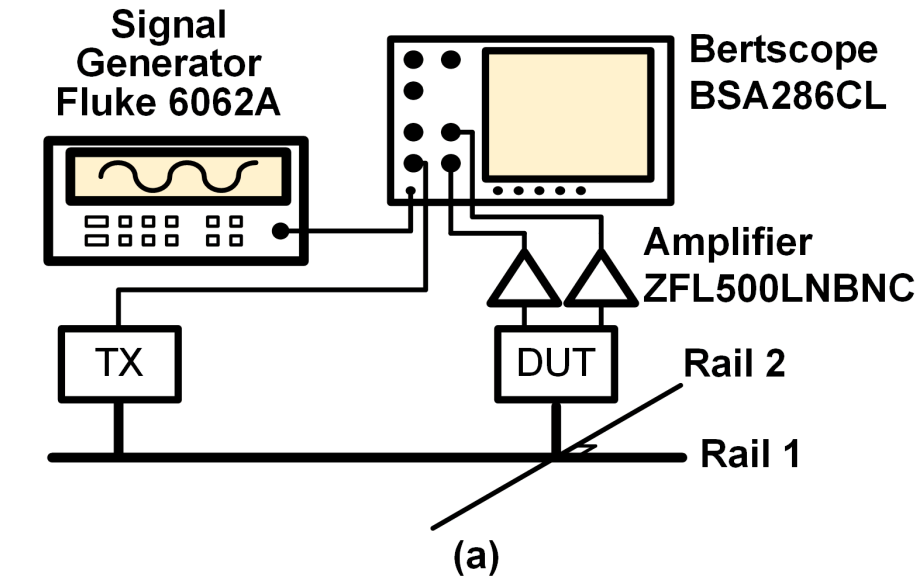


Figure 4.5: Die photo of the implemented TIA array in 65nm CMOS, (b) The IC packaged with diodes on a FR-4 PCB.



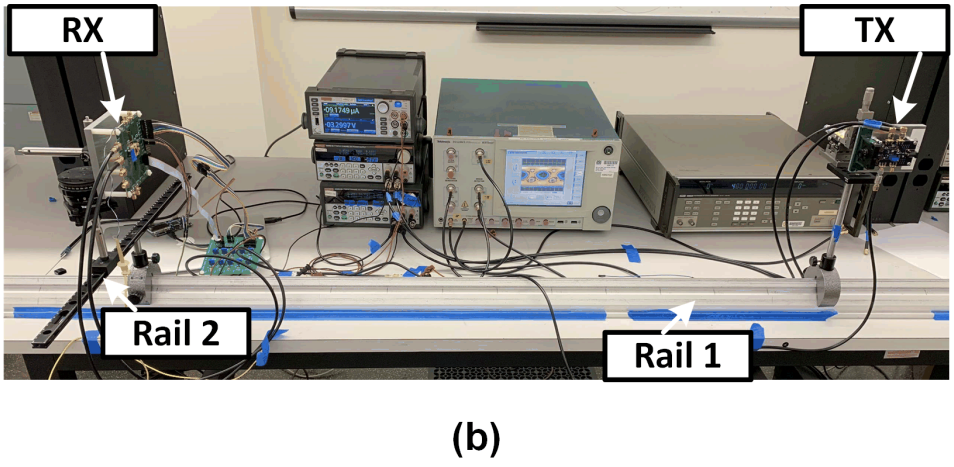


Figure 4.6: Measurement setup for FSO link bit-error rate testing of the packaged IC and diodes

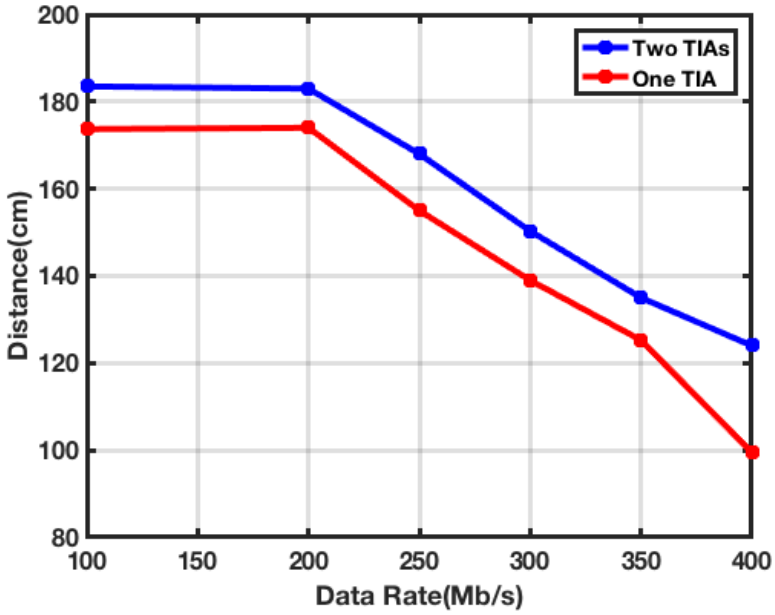


Figure 4.7: Measured distance vs. data rate using integrated RX for BER=10-4

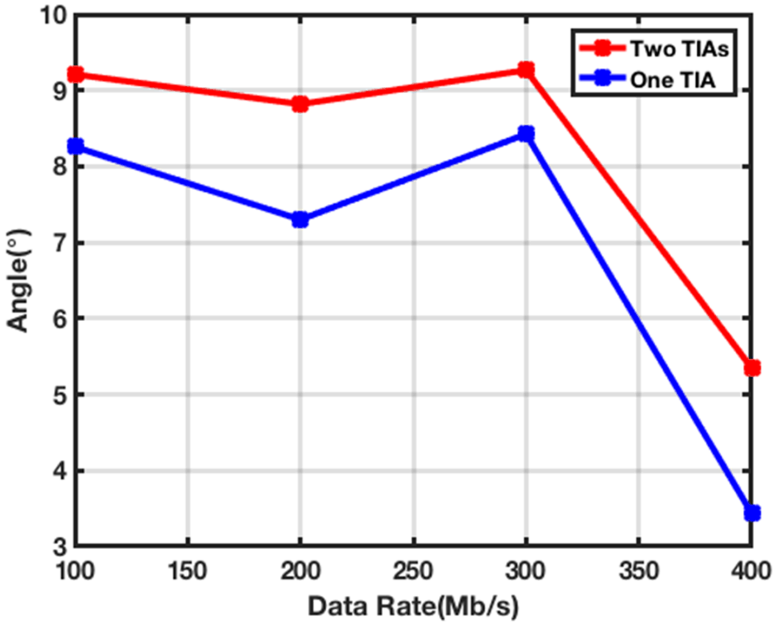
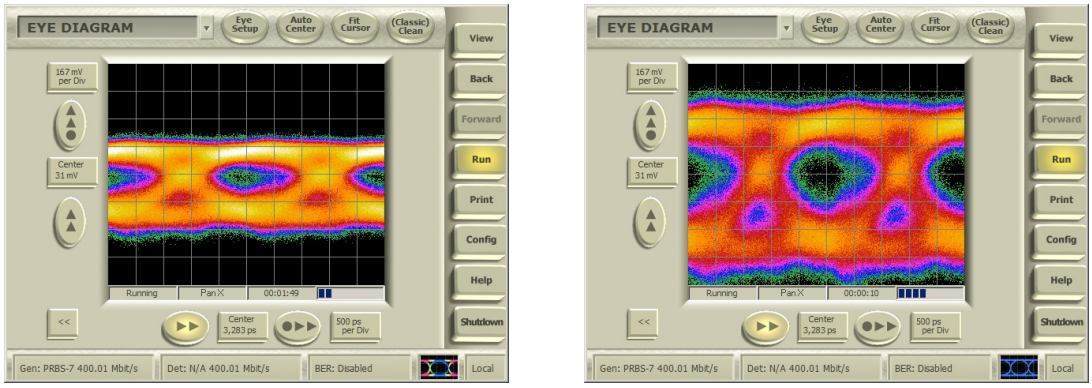


Figure 4.8: Measured angle vs. data rate using integrated RX for BER=10-4



(a) Single TIA eye diagram

(b) Proposed two TIA eye diagram

Figure 4.9: Measured eye diagram

Chapter 5: Conclusion

Translating FSO links from backhaul applications to portable devices requires receiver sensitivity and bandwidth challenges to be addressed while simultaneously ensuring low power consumption and compatibility with low-cost integrated CMOS technologies. In this work, we have demonstrated a distributed TIA approach in 65-nm CMOS to combine signals from multiple TIA and Si PIN photodiodes to achieve high bandwidth and low noise. With this approach, we achieve 400 Mb/s links up to 1 m using FSO, while ensuring compatibility with CMOS integration and low-cost off-the-shelf components. In this work, the data rata is limited by the bandwidth of the laser transmitter. In next step, we can design a higher bandwidth transmitter. On the other side, DFE circuits can be also implemented to get a higher bandwidth receiver. And this part is still on-going.

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