AN ABSTRACT OF THE DISSERTATION OF

Yanchao Wang for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on November 12, 2020.

Title: A 90.5dB DR 1MHz BW Hybrid Two Step ADC with CT Incremental and SAR ADCs

Abstract approved: _____

Gabor C. Temes

The sensors in real time data processing IoT devices require high resolution and sub-MHz data converters, usually implemented as Incremental ADCs due to the advantages of oversampling technique and low latency. In discrete time incremental (IDT) ADCs, the sampling switch non-linearity, charge injection degrade the resolution, and power hungry OPAMPs are demanded to provide fast and accurate settling for the switch-capacitor circuits. While the continuous time incremental (ICT) ADCs overcome these issues by removing the sampling switches and it also relax the OPAMPs settling accuracy to save power. A hybrid architecture of ICT ADC and SAR two step ADC is proposed to achieve high resolution at low oversampling ratio (OSR). The first ICT ADCs enable higher resolution, faster conversion speed with lower power consumption. The residual error of the ICT ADC is extracted at the last integrator output and transfers to the 2^{nd} SAR for further conversion. In this architecture, only the mismatch between the cascade of integrators (CoIs) and decimation filter transfer functions causes 1^{st} stage quantization noise leakage which can be solved by increasing opamp parameters instead of increasing the digital decimation filter complexity. In addition, the overall SQNR is independent of the first ICT ADC's NTF, which gives more freedom to trade-off between the loop stability and DAC errors. A 4bits DRZ DAC with data weighted averaging (DWA) technique is adopted to reduce the clock jitter of DAC, mitigate ISI error and static mismatch errors. Based on this architecture, a 16b resolution, 1MHz signal bandwidth hybrid two step ADC is designed and measurement results are demonstrated. Important sub circuits are introduced and analyzed in detail to get the target resolution. The ADC is fabricated in AKM 180nm CMOS process with 1.8V supply voltage, it achieves a DR of 90.5dB, and SNR/SFDR/SNDR of 82.5dB/85dB/80.5dB over 1MHz BW sampled at 64MHz.

A 90.5dB DR 1MHz BW Hybrid Two Step ADC with CT Incremental and SAR ADCs

By

Yanchao Wang

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Head of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Yanchao Wang, Author

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Chapter 1 : Introduction

1.1 Motivation

Delta sigma ADC can provide high resolution and low noise by using the oversampled techniques to do noise shaping. There are some applications, delta sigma ADCs are widely used and a lot of design challenges come out recently with the increasing data conversion rate. For example, in modern communication system, based on the long term evaluation advanced (LTE-A) standard, the RF bands requirements of the delta sigma ADCs have grown from 35-75MHz bandwidth [1],[2],[3],[4], in 2G/3G/4G standards to 300+MHz and more than 10bits resolution in 5G scenarios [5],[6] to support more users. Another applications are for the IoT devices [7]-[13], especially when large amount of data needs to be processed by sensor array, the sensors [9] demand MHz bandwidth and more than 16 bits resolution delta sigma ADCs. Since the transit frequency f_T of MOS transistor is limited, in 5G applications, targeting for more than 300MHz signal bandwidth, the possible oversampling ratio (OSR) is usually smaller than 16 [5],[6]. Meanwhile, in the MHz bandwidth and more than 16 bits resolution cases, the possible OSR is limited to around 40 [14]-[19]. Therefore, new delta sigma modulator architectures which provide high order noise shaping with low OSR needs to be explored.

To circumvent these challenges, high order single loop delta sigma modulator [2], [17],[18], [19] can be used, however, high order modulator loops are prone to be instability and the input dynamic range becomes smaller due to the overload issues. An alternative option is Multi-Stage-Noise-Shaping (MASH) ADCs, they combine multiple low order sub delta sigma loops [1], [3], [4], [5], [6] to provide high order noise shaping and still remain stable. In MASH architecture, all the sub-loops work at oversampling frequency and the quantization error transfer between different loops also happens at oversampling frequency. But the traditional MASH architectures suffer from quantization noise leakage [1], [5], [6], which requires complex digital filters and calibration techniques to replica the analog loop filter transfer functions. The Sturdy MASH (SMASH) [3], [4] feeds back all the sub-loops to the first loop input which eliminates the complex digital filters, But the speed of SMASH is limited for large BWs, since the main DAC can only feedback output after all the sub-loops finishing conversion. Therefore, the speed of the sturdy MASH is limited and difficult to achieve more than 300MHz signal bandwidth for 5G applications. Besides, the internal delay in the sub-loops cause stability issues. Another solution is the hybrid architectures that incorporate Incremental and Nyquist-rate ADCs to perform extended counting [10]-[13].

Comparing with MASH architecture, the quantization error transfer between each stages happens at Nyquist frequency in extended counting architectures which can relax the circuit design difficulties and save power consumption of following stages. The hybrid schemes have the advantages of both oversampled and Nyquist-rate ADCs, enabling them to achieve high resolution with superior energy efficiency. In hybrid schemes, the circuit non-idealities cause the quantization noise leakage between different conversion steps. However, the leakage issues are less serious and it can be solved by either designing better sub-circuits or doing some simple calibrations.

The implementation of delta sigma ADCs might be discrete-time (DT) converters or continuous time (CT) converters. The DT converters are based on switch capacitor (SC) techniques featuring robustness over process variations. However, the wide band thermal noise folding increases the in band thermal noise and the sample hold circuits need fast settling in each clock cycle by burning more the power. Recently, the high conversion rate and low power requirements make the CT converters more attractive. Comparing with DT converters, there is no sampling process with in CT loop filters and the constraint of maximum sampling frequency depends on the regeneration time of the quanitzer and the update rate of the DAC making the CT converters have large bandwidth. Another advantage is the anti-aliasing performance which helps filter out wide band noise, distortion and the CT converters are easier to drive eliminating the steep roll-off power hungry front end drivers demanded by Nyquist ADCs. The drawbacks are the process variation leading to stability issues and its sensitivity to clock jitters. When realizing high performance CT converters, these problems need to be carefully considered in both system level and circuit level designs. Similarly, the CT Incremental (ICT) ADCs inherit the advantages of CT converters in power consumption and speed. Meanwhile, the periodic reset convert the ICT to a Nyquist-rate converters by sacrificing some anti-aliasing performance.

In this dissertation, a robust MASH architecture and a hybrid two step scheme of ICT and SAR ADCs is proposed. Then the hybrid architecture is designed and implemented. It proves the concepts of the proposed data conversion schemes and motivates the ICT architectures.

1.1 Contribution of this Research

The major development and innovation of this research can be summarized as following:

1. Propose and simulate a Robust MASH (RMASH) architecture [20]. Its quantization leakage issue is better than tradition MASH [1], [5], [6], [14]-[16], [21] and complex digital filter and calibration can be saved. Also, its conversion speed are faster than the current MASH and SMASH [3],[4],[22] schemes, because the quantization error transfer is more straightforward and the second stage ADC is allowed to have arbitrary latency.

2. Based on the RMASH, a hybrid schemes of ICT and two capacitor SAR is proposed and designed.
3. A 16-bit ENOB with 2MS/s conversion rate hybrid ADC is implemented in AKM 180nm CMOS process. Measurement results are shown to demonstrate the proposed ideas.

1.2 Organization of this Dissertation

In this dissertation, chapter 2 reviews the existing MASH architectures and analyzes the proposed Robust-MASH architecture. Chapter 3 illustrates the system level design of hybrid ICT-SAR ADC. Chapter 4 describes the circuit implementation and analyzes dominating non-idealities. Layouts of the blocks are shown in Chapter 5. Chapter 6 offers measurement setup and results. Chapter 7 concludes this work.

Chapter 2 : Robust CT MASH

When targeting for high order noise shaping, single loop delta sigma modulators suffer from stability and input dynamic range degradation issues. One of the popular solution is the MASH delta sigma modulator [1], [3]-[6], [14]-[16],[22]. They achieves a higher order noise shaping by cascading lower stages, and thus benefiting from the stability of lower stages. Therefore, MASH architectures are suitable for high speed ADCs with low OSR.

2.1 Traditional MASH

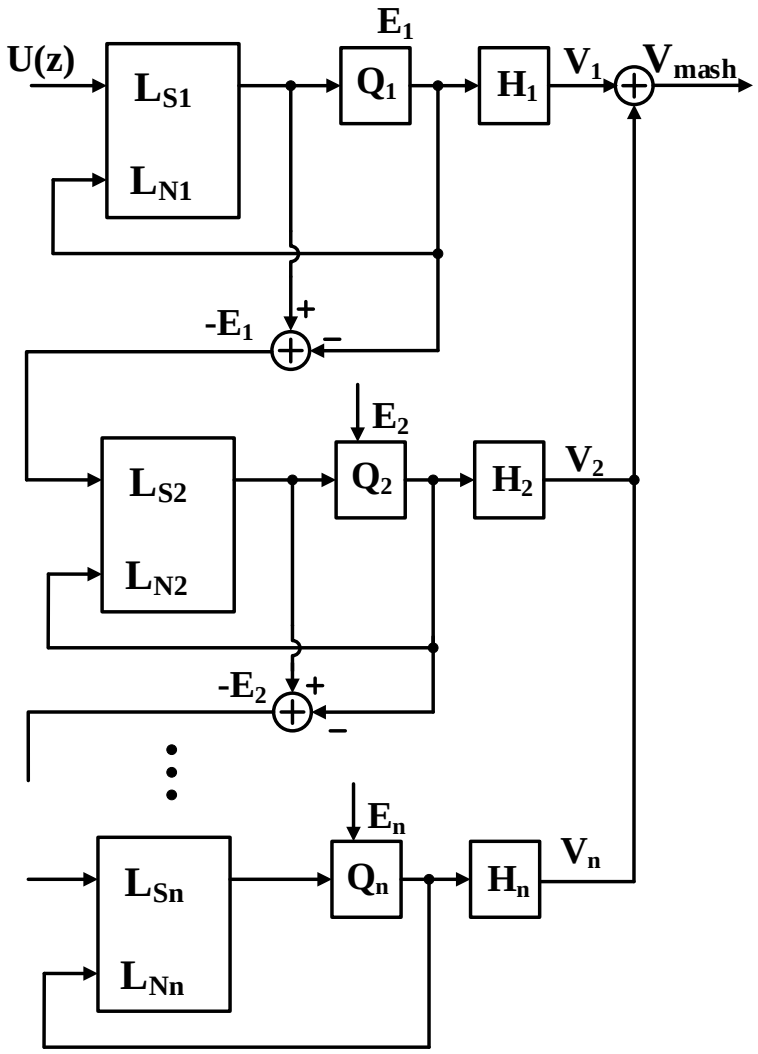


Figure 2.1: A general N^{th} order MASH architecture

Figure 2.1 shows the generalized block diagram of a n-loop MASH delta sigma modulator. The quantization error of preceding stage is extracted in analog domain and fed to the following stage.

Therefore, the following stage input includes the previous stage quantization error. By replicating the noise transfer function of the preceding stage analog NTF_{i-1} in the digital noise cancellation logic H_i, the quantization error can be cancelled using the digital representation. If the NTF_{i-1} matches H_i perfectly, the preceding stages' quantization errors can be eliminated at the final output V_{mash}, and only the quantization error E_n of the final stage shaped by all the previous stage noise shaping orders appears in the V_{mash} which is referred as the theoretical quantization noise (TQN). The overall output is described by

$$V_{mash} = (STF_1 \times U + NTF_1 \times E_1) \times H_1 - (STF_2 \times E_1 + NTF_2 \times E_2) \times H_2 + (-1)^{n+1}(STF_n \times E_{n-1} + NTF_n \times E_n) \times H_n = STF_1 \times STF_2 \times \cdots STF_n \times U + (-1)^{n+1} \times NTF_1 \times NTF_2 \times \cdots NTF_n \times E_n \quad (2.1)$$

where $H_i = \prod_{i+1}^{n} STF_i \prod_{i=1}^{i-1} NTF_i$, then all the terms are canceled except for U and E_n. In addition, the final stage quantization error E_n is suppressed by the cascade of n[th] order noise shaping function.

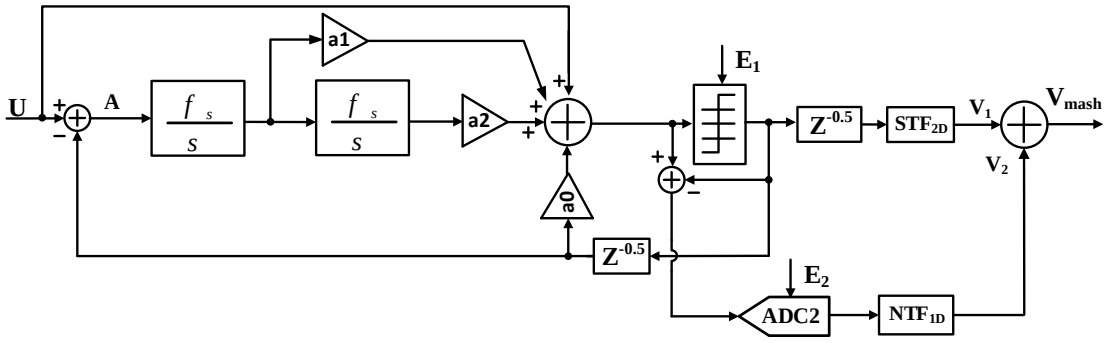


Figure 2.2: The CT 2-0 MASH delta sigma modulator

For the sub-loops in MASH, they can be zero or high order modulators. A 2-0 MASH is illustrated in Figure 2.2 to examine the MASH for more depth understanding. The input U is applied to the 1[st] loop, and the extracted quantization error E_1 is injected to the 2[nd] loop. The first stage is a low distortion CT feedforward CIFF modulator making STF_1=1 due to the feedforward path from input to the quantizer input. Since the 2[nd] step is a zero order Nyquist ADC, ideally, the STF_{2A}=1 and NTF_{2A}=1, simplifying H_1=STF_{2D}=STF_{2A}=1. To cancel E_1 at final output, H_2 needs to track the analog noise shaping function of the 1[st] delta sigma modulator requiring H_2=NTF_{1D}, where NTF_{1D} is the digital replica of NTF_{1A}. The final output of modulator can be figured out as

$$V_{mash} = STF_{1A} \times STF_{2D} \times U + NTF_{1A} \times STF_{2D} \times E_1 - STF_{2A} \times NTF_{1D} \times E_1 - NTF_{1D} \times NTF_{2A} \times E_2 = U - NTF_{1D} \times E_2 \quad (2.2)$$

From (2.2), if the digital STF_{2D}, NTF_{1A} match the STF_{2A}, NTF_{1D}, the E_1 will be removed from the final output V_{mash}. However, it is difficult to make sure the digital transfer functions NTF_{1D}, STF_{2D} perfectly match NTF_{1A}, STF_{2A}, the mismatch leads to the quantization noise E_1 leakage. The coefficients variations coming from process variation and non-idealities such as parasitic loading effects, finite DC gain and UGBW of opamps cause analog transfer function variations resulting in quantization noise leakage. This issue can be solved by designing high accuracy integrators, analog calibrations for coefficients variations or digital calibration for NTF_{1D}, STF_{2D} to make them track the analog transfer functions.

As shown in Figure 2.2, the preceding stage quantization noise E_1 extraction is implemented by using active opamps as an adder. After transferring E_1 to the second stage, the first stage is able to start another conversion, and the 2nd stage has maxim one cycle to do the 2nd step conversion. Therefore, the MASH is able to perform fast conversion.

2.2 Sturdy MASH

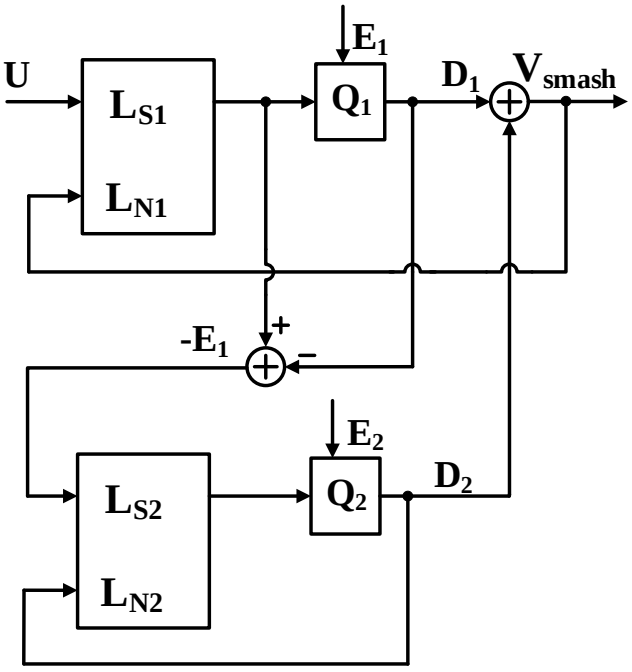


Figure 2.3: A two-loop SMASH architecture

The traditional MASH architectures provide aggressive noise suppression capability without suffering stability issues. In spite of these advantages, the quantization noise leakage in traditional MASH demands high accuracy analog components and power hungry digital filters to reduce the leakage. To circumvent this issues, the SMASH [3],[4],[22] eliminates all the digital filters and

relaxes the requirements of opamps DC gain and coefficients accuracy. At frequency range that SMASH can cover, the SMASH combines stability advantages of multi-loop structure with relaxed circuit requirement of the single loop modulator over traditional MASH.

Figure 2.3 shows the block diagram of SMASH, the second quantizer outputs add with the first loop outputs in digital domain and then feedback to the main DAC. As a result, the digital quantization noise cancellation loop is removed. The transfer function of this structure is derived as

$$V_{smash} = STF_1 \times U - NTF_1 \times NTF_2 \times E_2 + NTF_1 \times (1 - STF_2) \times E_1 \quad (2.3)$$

If the SMASH is implemented as a DT circuit [22], the sample hold circuits make the STF_2 have an unavoidable delay making STF_2 cannot equal to 1, and the E_1 is left at the final output. If choosing$NTF_2 = 1 - STF_2$, the DT SMASH output becomes

$$V_{smash} = STF_1 \times U - NTF_1 \times NTF_2 \times E_2 + NTF_1 \times NTF_2 \times E_1 \quad (2.4)$$

From (2.4), in DT SMASH output, both of the quantization error E_1 and E_2 are suppressed by the cascade of the two stage noise transfer functions. Comparing with traditional DT MASH, the digital filter is removed and thus the analog components requirements are much relaxed. Instead of cancel E_1 as in traditional MASH, E_1 is shaped by the cascade of two stage noise transfer functions.

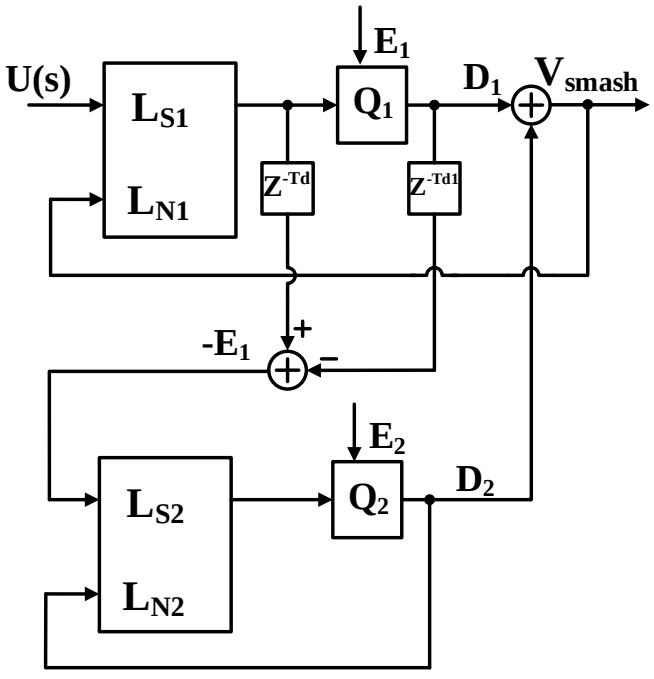


Figure 2.4: The CT SMASH architecture

For CT SMASH implementations, the delay of STF_2 is less than that in DT SMASH, if choosing feedforward architecture with a direct path from the 2nd stage input to its quantizer, then STF_2 becomes 1. Ideally, T_d equals T_{d1} as presented in Figure 2.4 [4], then the CT SMASH output becomes

$$V_{smash} = STF_1 \times U - NTF_1 \times NTF_2 \times E_2 \quad (2.5)$$

From (2.5), the first stage quantization noise can be canceled as in traditional MASH. The mismatch between T_d and T_{d1} results in E_1 leakage in the final output. If the mismatch is large, the residual signals of E_1 cause the second stage saturate and E_1 appears at both of the two stages resulting in increased quantization noise floor and performance degradation.

As a conclusion, the SMASH architecture enables multi-loop modulators to achieve high order noise shaping without stability issues. In addition, it removes the digital filters demanded in traditional MASH architectures and relax the analog components accuracy requirements. However, the latency of SMASH equals to the total operating time of all the sub-loops, therefore, its conversion speed is limited.

2.3 Robust MASH

2.3.1 RMASH

The recent applications of delta sigma ADCs demand large signal bandwidth and low power consumption. Therefore, new MASH architectures that are able to provide large signal bandwidth, without complex digital filter attracted more interests. [20] proposes a new low leakage Robust MASH (RMASH) scheme. Instead of extracting the analog E_1 at quantizer input, the previous stage's residual error relative to $NTF_1{*}E_1$ is extracted in the analog domain and transfers to the following loop. $NTF_1{*}E_1$ is recovered from the following stage digital output to cancel the same item in the first stage output. Then both the NTF_1 variation and E_1 of the preceding loop enter the following loop and its digital outputs include these information as well. This structure features that the E_1 can be canceled in the final RMASH output even with NTF_1 variation. As a result, the RMASH is able to perform fast conversion as traditional MASH architecture with relaxed analog components accuracy requirements and simplified digital filters.

Figure 2.5 illustrates the proposed two loop RMASH structure. Its 1st stage is a feedforward DSM [24] with the advantages of STF=1 to provide low distortion in the loop filter. Unlike in traditional MASH, the shaped quantization noise is extracted at last integrator output as shown in Figure 2.5. Assuming STF_1=1, V_A = $-NTF_1{*}E_1$ [25] which is small, thus V_A can be integrated first to get a

larger value V_B=NTF_1*E_1*I^N, which relaxes 2nd ADC resolution. So, the 2nd ADC output needs to be differentiated to recover -NTF_1*E_1. This way, the NTF_1*E_1 components in D_1 and D_2 can be canceled. The final output V_{rmash} is

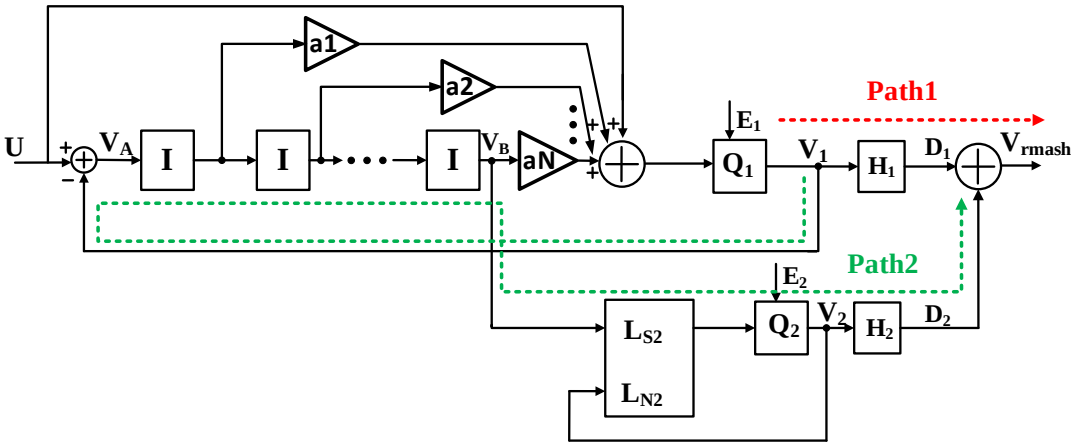


Figure 2.5: Proposed low quantization noise leakage structure

$$V_{rmash} = H_{1D} \times STF_{1A} \times U + NTF_{1A} \times E_1 \times H_{1D} - NTF_{1A} \times E_1 \times I^N \times STF_{2A} \times H_{2D} + H_{2D} \times NTF_{2A} \times E_2 = H_{1D} \times STF_{1A} \times U + NTF_{1A} \times E_1 \times (H_{1D} - STF_{2A} \times I^N \times H_{2D}) + H_{2D} \times NTF_{2A} \times E_2 \quad (2.6)$$

where N is the order of the 1st DSM, and I^N is the transfer function of the cascade of N integrators. Usually, we do not want to change the STF of the input signal U, therefore, H_{1D} can be chosen as

$$H_{1D} = STF_{2A} \quad (2.7)$$

To cancel the NTF_{1A}*E_1 in (2.6), H_{2D} becomes

$$H_{2D} = I^{-N} \quad (2.8)$$

Then the final output becomes

$$V_{rmash} = STF_{1A} \times STF_{2A} \times U + I^{-N} \times NTF_{2A} \times E_2 \quad (2.9)$$

Based on the previous analysis, to cancel E_1 at final output, the transfer functions of path 1 and path 2 in Figure 2.5 should be equivalent. If H_{1D} and H_{2D} deviate from their ideal values given in (2.7) and (2.8), the NTF_{1A}*E_1 term will appear at the RMASH outputs leading to quantization noise leakage. However, the leakage term is the shaped quantization noise which is much smaller than E_1 in traditional MASH. In addition, the H_{1D} matching requirement remains the same as tradition MASH. H_{2D} only needs to match all the cascade of integrators transfer function instead of the NTF_1 in traditional MASH. Therefore, the H_{2D} becomes simpler.

In brief, the RMASH architecture has the advantages of simplifying the H_{2D}, lower quantization noise leakage which relaxes the analog component accuracy requirements and thus reduces power consumption.

2.3.2 DT RMASH

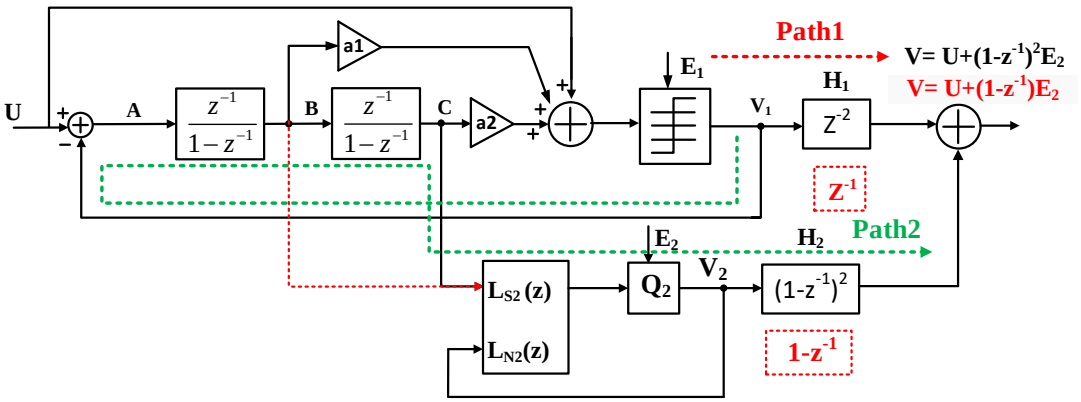


Figure 2.6: Low leakage DT 2-2 RMASH ADC

A DT 2-2 RMASH is shown in Figure 2.6. Its first stage is a 2nd order DSM, and the 2nd stage is the same as the first stage. If the shaped quantization error is extracted at the first integrator output *B*, H_2 becomes a differentiator and $H_1 = z^{-1}$ to match the integrator delay. E_2 is first-order shaped at the output. If the quantization noise is extracted at *C*, both H_1 and H_2 transfer function become 2nd order, and E_2 is 2nd-order shaped regardless of the NTF_1 of the modulator. Therefore, to achieve more aggressive noise shaping, the last integrator output is the better node for sampling the quantization noise. From (2.7) and (2.8), the transfer function of H_{1D} and H_{2D} can be figured out:

$$H_{1D}(z) = z^{-2} \tag{2.10}$$

$$H_{2D}(z) = (1 - z^{-1})^2 \tag{2.11}$$

If both the STF_1 and STF_2 are 1, the final output becomes

$$V_{rmash}(z) = z^{-2} \cdot U + (1 - z^{-})^2 \cdot NTF_2(z) \cdot E_2 \tag{2.12}$$

The H_{1D} matching can be ensured by choosing a feedforward low distortion DSM architecture to make STF=1. To figure out the quantization noise leakage, the transfer function of cascade of integrators including the non-idealities of the integrators needs to be modeled. The simplified DT integrator is shown in Figure 2.7. Considering the component non-idealities of integrators, its transfer function can be modeled as [26]

$$I(z) = \frac{C_1}{C_2} \times \frac{A_0}{A_0 + 1 + C_1/C_2} \times \frac{z^{-1}}{1 - \frac{(1+A_0)C_2}{C_1 + C_2 + A_0 C_2} z^{-1}} \tag{2.13}$$

From (2.13), the finite DC gain and capacitor ratio introduce a constant gain error and an extra pole for the DT integrator transfer function. The extra pole moves the NTF zero from z=1 to the inside the unit circle

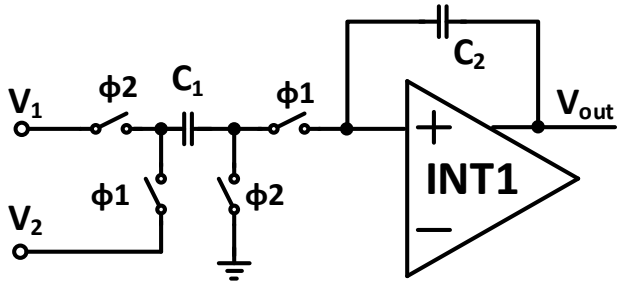


Figure 2.7: Simplified DT integrator model

making the integrator leaky and lossy. If GE and z_p represent the gain error and the extra pole, (2.13) becomes

$$I(z) = GE \times \frac{z^{-1}}{1-z_p z^{-1}} \tag{2.14}$$

Where

$$GE = \frac{C_1}{C_2} \times \frac{A_0}{A_0+1+C_1/C_2} \tag{2.15}$$

$$z_p = \frac{(1+A_0)C_2}{C_1+C_2+A_0C_2} \tag{2.16}$$

Combining (2.11)-(2.16), the H_{2D} becomes

$$H_{2Dr}(z) = \frac{1}{GE_1 \times GE_2} \times \left(1 - z_{p1}z^{-1}\right) \times \left(1 - z_{p2}z^{-1}\right) \tag{2.17}$$

Where the gain error and extra poles are relative to the ratio of C_1 and C_2, DC gain of the opamps which are all constant. The constant gain errors can be modeled in H_{2D} to make the E_1 cancellation better even including the non-idealities of the integrators and relax the analog components design requirements. However, (2.17) is difficult to implement in digital domain, and the mismatch between (2.11) and (2.17) might cause quantization noise leakage.

From (2.12), the DT 2-2 RMASH achieves the most aggressive 2nd order noise shaping from the first stage regardless the value of NTF_1. The limitation of NTF_1 comes from the first stage modulator's stability, jitter and ISI error considerations. Aggressive NTF_1 leads to more high frequency quantization noise and DAC transitions all of which increase the jitter and ISI error. While smaller NTF_1 leads to larger quantization noise leakage when transfer function mismatch exists.

Thus, it is important to model the jitter, ISI error and non-idealities of integrators in SIMULINK for the DSM modulator to pick up a reasonable NTF which provides the target resolution with good stability.

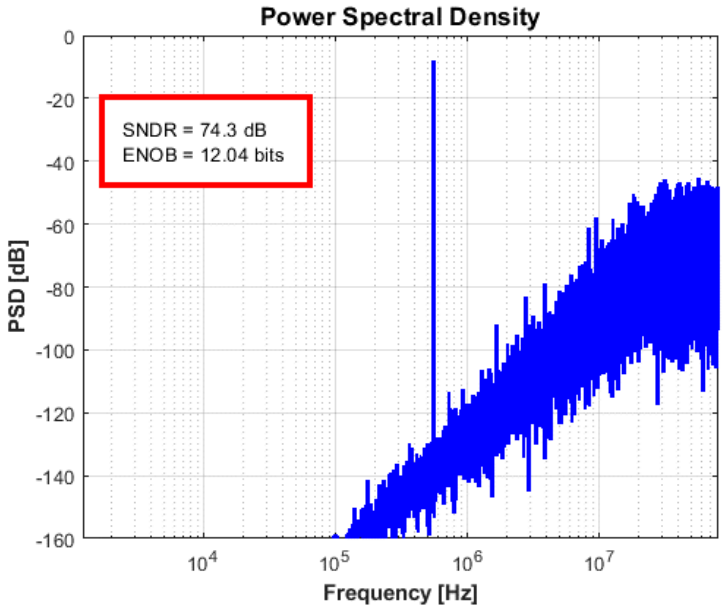


Figure 2.8: PSD of the 2nd order DSM

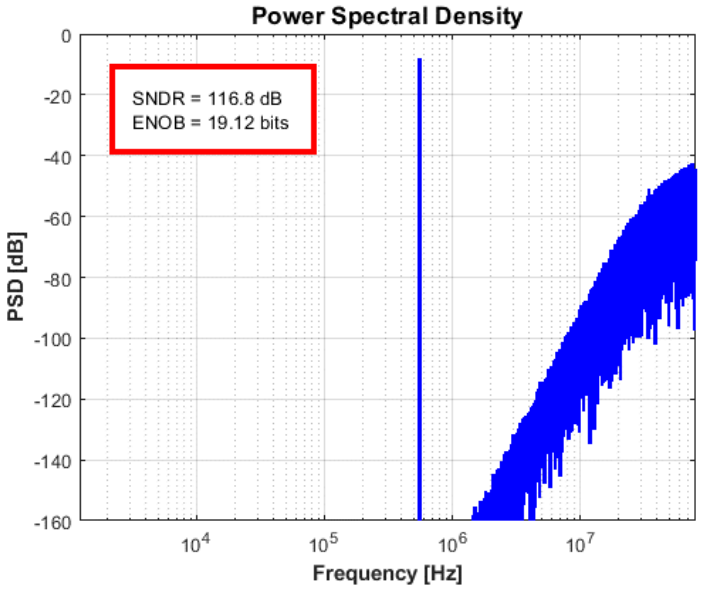


Figure 2.9: PSD of 2-2 Robust DT MASH

A design example of 2-2 DT Robust MASH with 3bits internal quantizer, fs= 80MHz, and OSR=32 are modeled and simulated in SIMULINK, and the first and second stages are two

equivalent 2nd order DSMs. The 2-2 MASH PSDs are shown in Figure 2.8 and Figure 2.9. Based on the simulation results, the 2-2 MASH increases the SNDR by 40dB.

In DT RMASH, the switch capacitor DAC is less sensitive to clock jitter. However, the DT integrators are based on sample hold circuits requiring power hungry OPAMPs to provide large unity-gain bandwidth, high DC gain and slew rate. In addition, the sample hold circuit leads to wide band thermal noise folding and thus large sampling capacitors are demanded to reduce the noise. As a result, the conversion rate of DT RMASH is limited by the speed of sample hold circuits due to the large sampling capacitors.

2.3.3 CT RMASH

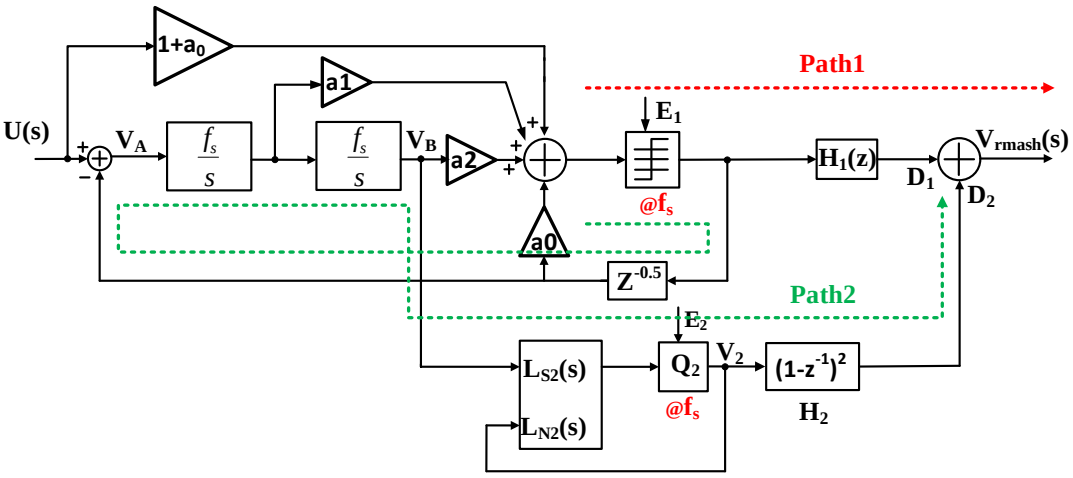


Figure 2.10: CT RMASH structure

A 2-2 CT RMASH architecture is shown in shown in Figure 2.10, it includes two equivalent 2nd order DSMs. To cancel E_1 at output, the transfer functions of path1 and path2 need to be equivalent with each other. Since H_1 and H_2 are implemented in digital domain, they can only be DT transfer functions. Therefore, the DT equivalent transfer function of the CT path needs to be figured out. If the two DSMs have STF=1, and f_s=1, then the 2nd path transfer function becomes

$$H_{2p}(s) = \left(\frac{1}{f_s}\right)^2 \tag{2.18}$$

The 2nd loop is an oversampled system, therefore, the IIR transformation can be used to find out its DT equivalent transfer functions [27] or ***c2d*** function of MATLAB.

$$H_{2p}(s)|_{s=j2\pi f_s} = \frac{z^{-1}}{(1-z^{-1})^2} \tag{2.19}$$

Similarly to the 2-2 Robust DT MASH, H_1 and H_2 are:

$$H_1(z) = z^{-1} \tag{2.20}$$

$$H_2(z) = (1 - z^{-1})^2 \tag{2.21}$$

A design example of 2-2 CT Robust MASH with 3 bits internal quantizer, fs=80MHz, and OSR=32 are modeled in Simulink and the PSD are shown in Figure 2.11. Comparing with Figure 2.9, the 2-2 CT RMASH ADC gets the same result as the DT 2-2 RMASH. So the 2-2 RMASH architecture is also valid for CT implementations.

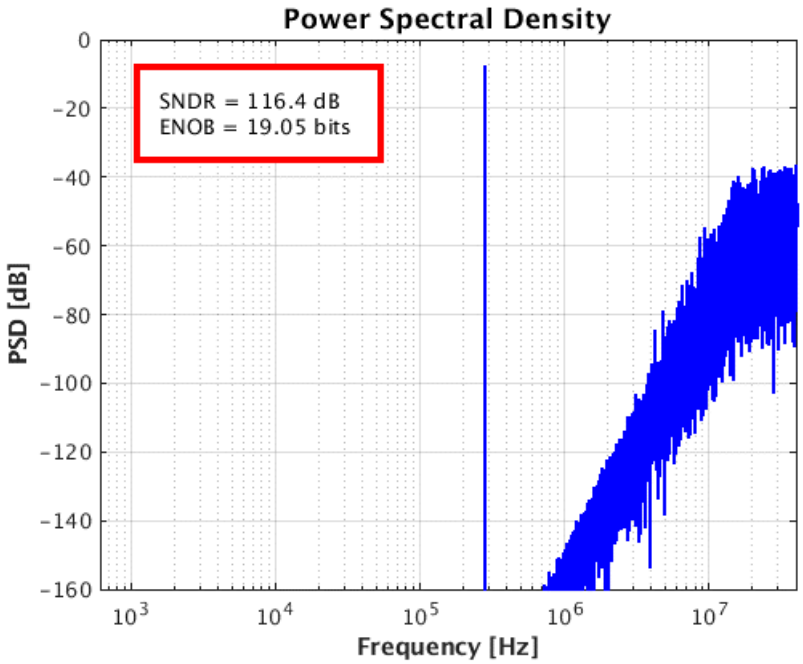


Figure 2.11: PSD of CT 2-2 RMASH

The CT RMASH does not include sampling switches, so there is no wide band thermal noise folding. Meanwhile, the DC gain, unit-gain bandwidth and slew rate requirements are much more relaxed than the DT implementations. The drawback of CT RMASH includes the STF and NTF transfer function variations coming from the RC variation. It leads to quantization noise leakage which requires digital calibration to process this issue. Besides, the main feedback DAC in CT DSM is more sensitive to clock jitter noise and dynamic ISI errors comparing with the DT implementations.

2.3.4 CT-DT hybrid RMASH

A CT-DT hybrid 2-2 RMASH architecture is shown in Figure 2.12. It includes a 2nd order CT DSM and a 2nd order DT DSM, both of them work at oversampling frequency.

The first delay is to match the delay of the sample hold circuit delay of the 2nd DT DSM, the $H_1(z)$ is the same as that in CT RMASH, since it still follows the IIR variation.

$$H_1(z) = z^{-1} \tag{2.22}$$

$$H_2(z) = (1 - z^{-1})^2 \tag{2.23}$$

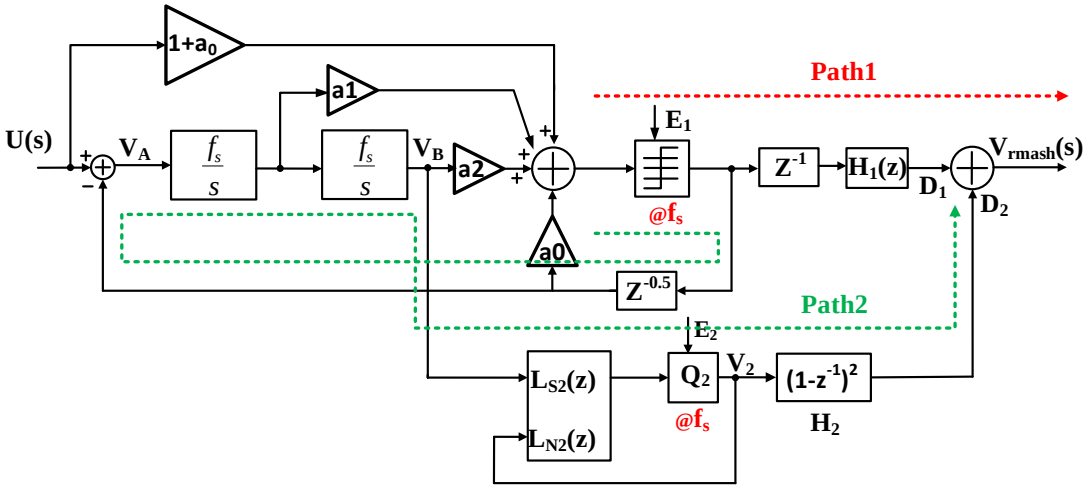


Figure 2.12: CT-DT hybrid MASH

A CT-DT 2-2 hybrid RMASH with 3 bits internal quantizer, fs=80MHz and OSR=32 are modeled in Simulink and the PSDs are shown in Figure 2.13 and 2.14. The hybrid 2-2 RMASH achieves the same resolution as the DT 2-2 MASH.

The hybrid 2-2 RMASH includes a continuous time first stage to avoid sampling switches and wide band thermal noise folding. Comparing with the 2-2 CT RMASH architecture, the 2nd stage DT DSM is more robust and less sensitive to process variation helping reduce the quantization noise leakage from the transfer function mismatches. The settling accuracy requirements of the sampled hold circuits in the DT DSM are also relax because the settling error impact becomes much less when referred into the first stage input.

2.3.5 Hybrid 2-0 RMASH

To solve the quantization noise leakage issue in the hybrid 2-2 MASH. The hybrid 2-0 RMASH is proposed as shown in Figure 2.15. It includes a 2nd order CT DSM as its 1st stage and a nyquist ADC as its 2nd stage. The first stage CT DSM can provide high conversion speed with less power consumption. The DT 2nd SAR features accurate transfer function in which both the STF and NTF are 1 to simplify the digital transfer functions H_{1D} and H_{2D} in the RMASH. In the hybrid structure, the output at node ***B*** is sampled and stored on the sampling capacitor of the 2nd ADC for one nyquist

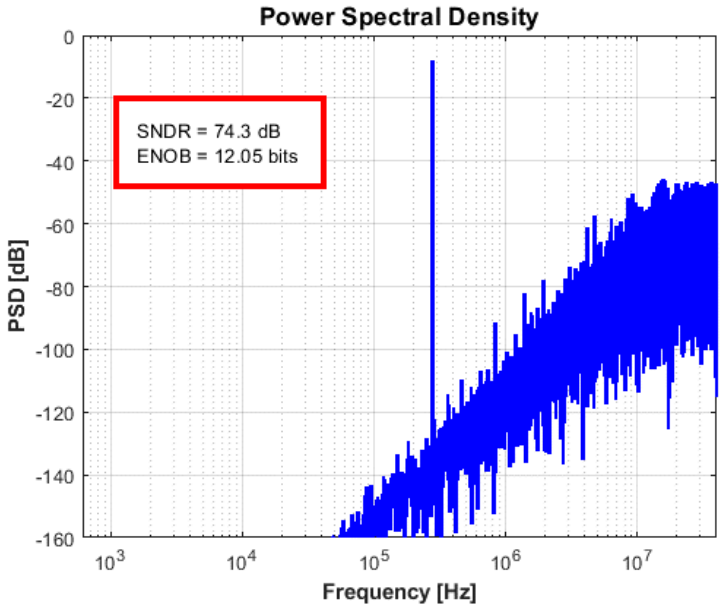


Figure 2.13: PSD of 1st CT DSM

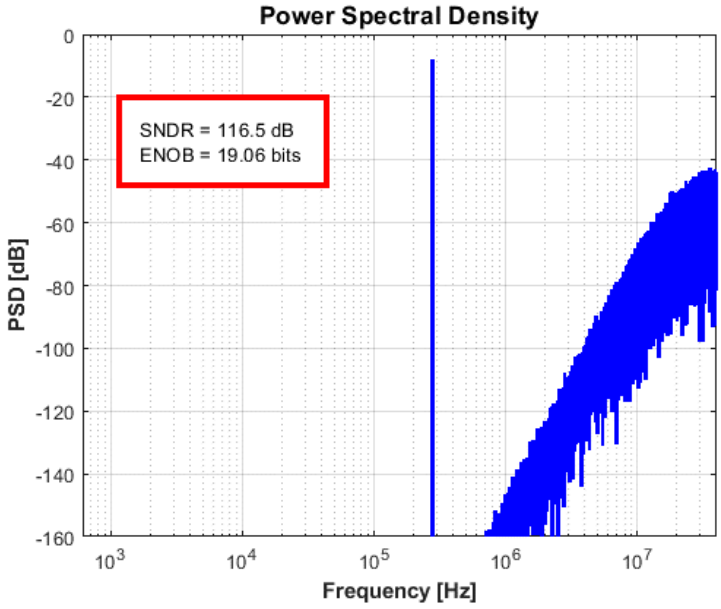


Figure 2.14: PSD of 2-2 CT-DT hybrid MASH

period. Therefore, Zero-Order-Hold (ZOH) transformation [28] can be used to figure out the equivalent DT transfer function of the cascade CT integrators as shown in Figure 2.16. To match the delay of the sample hold circuit in SAR, one period delay is introduced in the path1. Since half cycle delay is introduced in the feedback DAC, to sample the first stage quantization error completely, half cycle delay is added at the last integrator output.

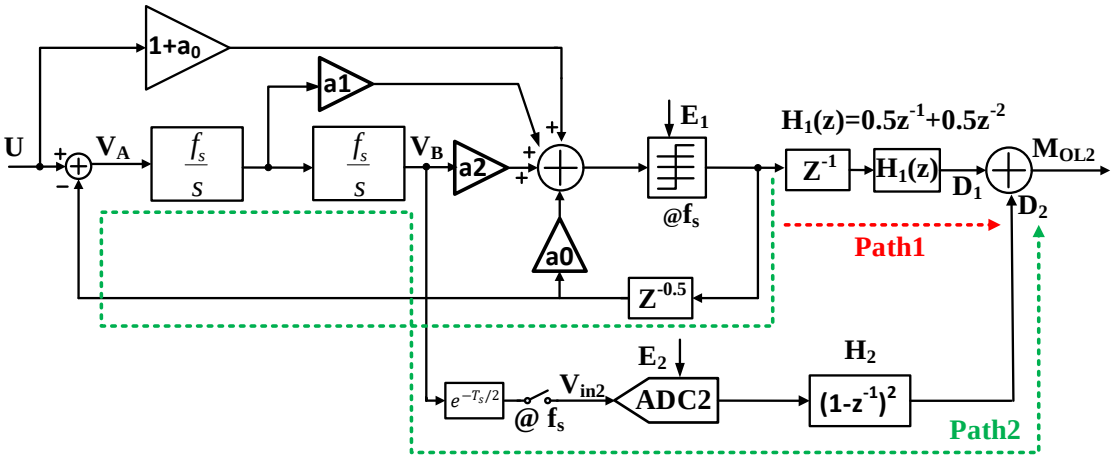


Figure 2.15: CT-DT hybrid 2-0 RMASH

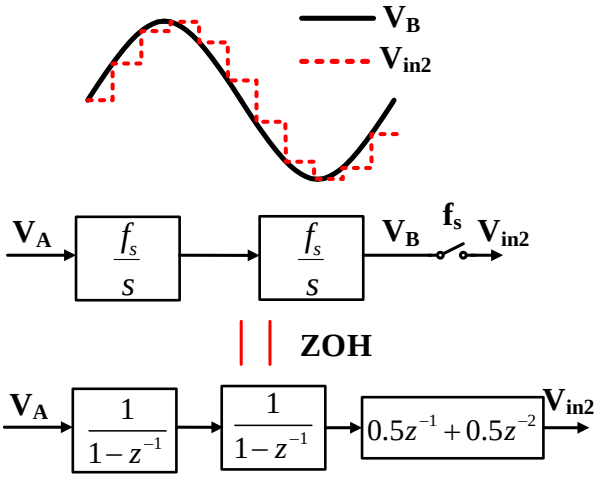


Figure 2.16: CT-DT ZOH transformation

As shown in Figure 2.16, with ZOH transformation, the cascade CT integrator transfer function is equivalent to two cascade non-delay DT integrators and one FIR term. Then, the transfer functions of H_1 and H_2 becomes

$$H_1(z) = 0.5z^{-1} + 0.5z^{-2} \tag{2.24}$$

$$H_2(z) = (1 - z^{-1})^2 \tag{2.25}$$

The final output is figured out as

$$M_{OL2} = (0.5 \cdot z^{-1} + 0.5 \cdot z^{-2}) \cdot U + (1 - z^{-1})^{-2} \cdot E_2 \tag{2.26}$$

From (2.26), the second SAR contribution to the SQNR is like the internal quantizer of the 1st DSM. The advantages are, it locates outside the loop and the latency of the SAR does not affect the stability of the 1st DSM loop which allows high resolution SAR to get high SQNR.

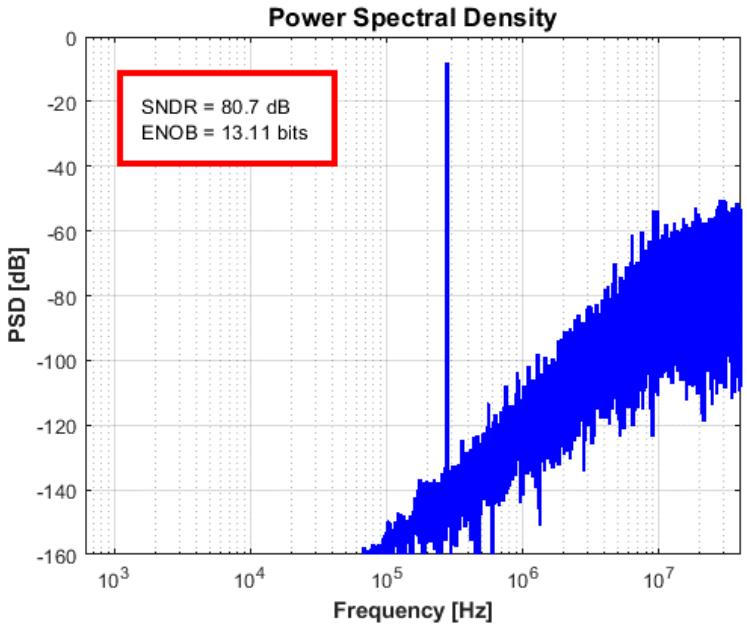


Figure 2.17: PSD of the 2nd order CT DSM

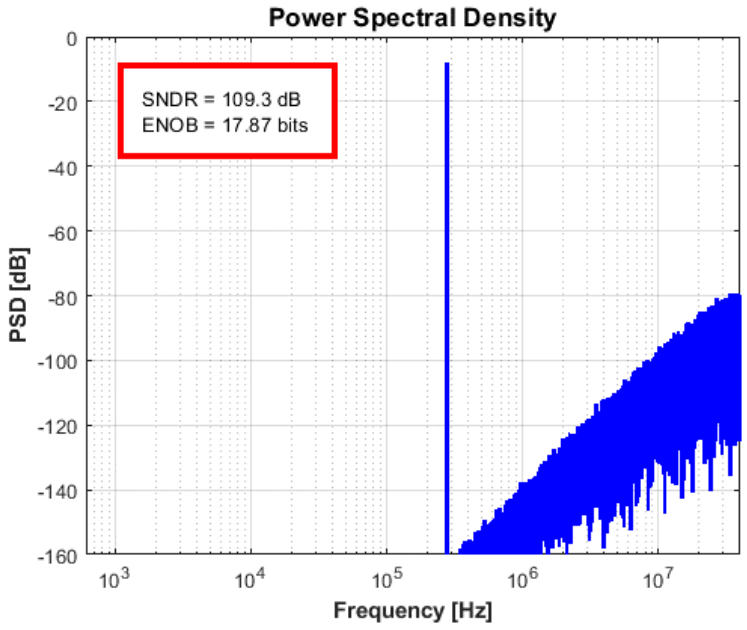


Figure 2.18: PSD of the 2-0 hybrid MASH

A design example of a hybrid 2-0 RMASH including a 2nd order CT DSM with a 4 bits internal quantizer, fs =80MHz and OSR=32, and an 8bits SAR working at 1.25MHz nyquist frequency. It

is modeled and simulated in SIMULINK, the PSDs of the first stage and the RMASH results are shown in Figure 2.17 and 2.18. The first stage provides 80dB SQNR, and the 2nd 8 bits quantizer improves SQNR to 109dB. If the E_1 is perfectly canceled at output, the remaining quantization noise will be the E_2 shaped by the 2nd order differentiator given in (2.26). Therefore, the SQNR can have 24dB (4 bits) improvement.

The PSD comparison with the ZOH and IIR transforamtions result is shown in Fig. 2.19. They achieve the same SQNR since the inband spectrums are the same. However, the IIR transformation has larger peak at high frequency and leads to more high frequency DAC transitions which worse the dynacmic DAC errors. Therefore, the ZOH transformation is choosen.

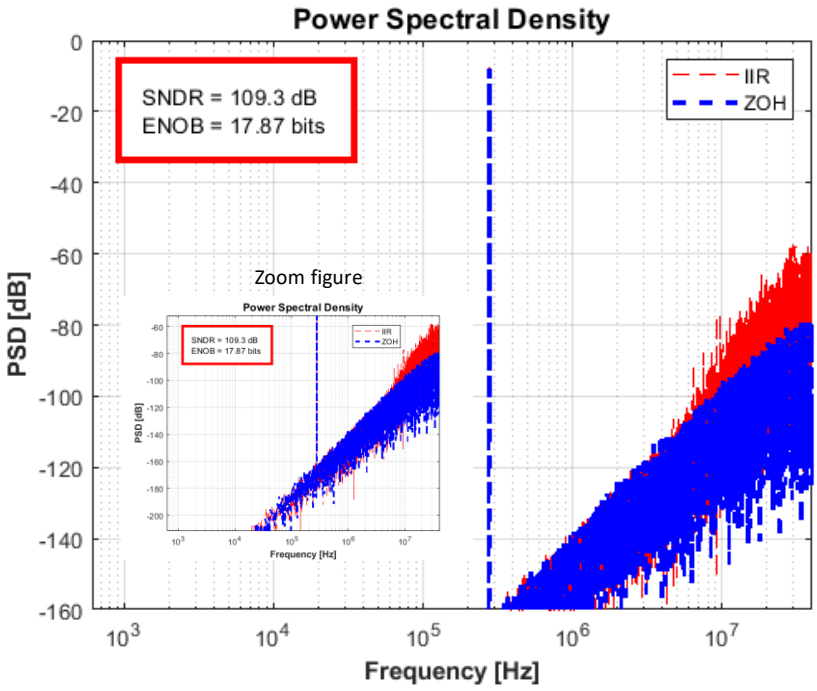


Figure 2.19: The PSD comparison of ZOH and IIR transformations

Chapter 3 : Extended Counting ADC

The MASH architectures are based on oversampled technique, and they cannot provide Nyquist-rate conversion. Recently, the IoT devices and sensor circuits require power efficient high resolution Nyquist rate ADCs to process the large amount of data. Incremental analog-to-digital converters (IADCs) are essentially delta sigma ADCs which are periodically reset, thus converting them into Nyquist-rate ADCs [11]-[13],[29]-[31] which inherit the advantages of over-sampling technique to give high resolution and Nyquist conversion rate to reduce input and output latency. However, the periodical reset for integrators in Incremental ADCs reduces the noise shaping ability and thus causes SQNR degradation.

3.1 DT extended counting ADC

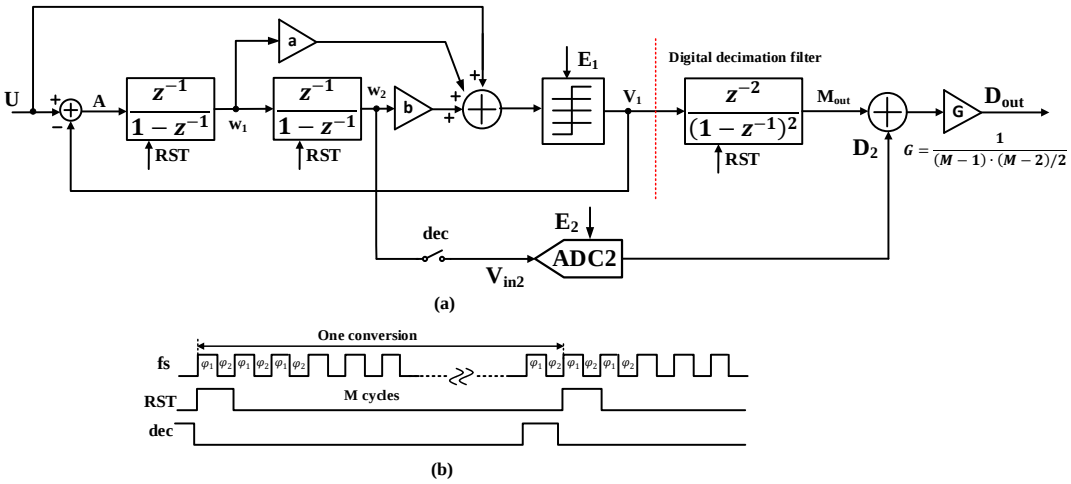


Figure 3.1: (a) The z-domain model of a single-loop IADC2 with a low-distortion feed-forward modulator. (b) The simplified timing diagram.

Fig. 3.1(a) depicts a two-step ADC constituting by a DT Incremental and Nyquist type ADC [11]-[13]. The first stage is a 2nd order feedforward low distortion the DT Incremental ADC, and the 2nd step is a N bits SAR. The simplified timing diagram is presented in Fig. 3.1(b), M is the oversampling ratio (OSR) of the IADC in every conversion. All the memory blocks including the integrators and decimation filters are reset every M clock cycles. Due to the reset, the consecutive two conversions are independent, and the IADC converts the analog data sample-by-sample making it function as a nyquist ADC.

The nyquist type IADC can be analyzed in time domain [31], the input U and output V_1 equation can be figured out at the last integrator output node. At the end of every conversion (M^{th} cycle), the last integrator output is

$$w_2[M] = \sum_{K=1}^{M-1} \sum_{i=1}^{K-1} (U[i] - V_1[i]) \tag{3.1}$$

The input singal can be regarded as constant in one conversion and all the U[i] is approximated to a constant value U:

$$U = \frac{\sum_{K=1}^{M-1} \sum_{i=1}^{K-1} V_1[i] + w_2[M]}{(M-1)\cdot(M-2)/2} \tag{3.2}$$

To recover the input, the digital decimation filter can be implemented as two delayed cascade-of-integrators (CoIs). Usually, the digital decimation filter has the same transfer function as the analog cascade of Integrators from node *A* to w_2 in the incremental modulator. The residual error of every conversion in the IADC is the last integrator output value $w_2[M]$ of M^{th} cycle

$$w_2[z] = -NTF_1(z) \cdot E_1(z) \cdot I^2(z) \tag{3.3}$$

When the modulator coefficients in Fig. 3.2 is a=2, b=1, then

$$NTF_1(z) = (1 - z^{-1})^2 \tag{3.4}$$

It is the most aggressive NTF of the 2^{nd} order modulator. Then

$$w_2[z] = -z^2 \cdot E_1(z) \tag{3.5}$$

In time domain, w_2 is

$$w_2[M] = E_1[M - 2] \tag{3.6}$$

When the NTF is less aggressive than the value in (3.4), the $w_2[M]$ is also smaller than $E_1[M-2]$, for L level internal quantizer, the ENOB of 2^{nd} order IADC can be derived as

$$ENOB = log_2 \left[\frac{(M+1)\cdot M \cdot L}{2} \right] \tag{3.7}$$

And the SQNR is approximated to be

$$SQNR_2 = 2 \cdot 20log_{10}(M) + 20log_{10}(L - 1) - 6 \tag{3.8}$$

So the SQNR of IADC is determined by the order and internal quantizer level of the first IADC. After $w_2[M]$ is sampled and converted by the 2^{nd} step ADC, it has

$$w_2[M] + E_2 = D_2 \tag{3.9}$$

Combing (3.2) and (3.9), the two step ADC output is

$$U = \frac{\sum_{K=1}^{M-1}\sum_{i=1}^{K-1} V_1[i] + D_2[M/OSR] + E_2[M/OSR]}{(M+1)\cdot M/2} \tag{3.10}$$

Then, the input signal is recovered by

$$U = \frac{\sum_{K=1}^{M-1}\sum_{i=1}^{K-1} V_1[i] + D_2[M/OSR]}{G} \tag{3.11}$$

$G = M \cdot \frac{(M-1)}{2}$, and the SQNR of the two step ADC given in (3.8) is modified as

$$SQNR_{2-step} = 2 \cdot 20log_{10}(M) + 6.02 \cdot N - 6 \tag{3.12}$$

Where M is the OSR of IADC and N is the ENOB of the 2nd SAR, the 2nd SAR contribution to the overall SQNR is like an internal quantizer. But it is outside the IADC and high resolution SAR can be implemented to improve the SQNR without introducing latency to the IADCs. Comparing with delta sigma modulator, the IADCs lose some SQNR due to the periodical reset.

3.2 Hybrid Extended Counting ADC

In the DT IADC and SAR hybrid two step ADC, the first DT IADC suffers from sampling switches non-idealities and charge injection problems, which leads to distortion and increases noise floor. In addition, the sample hold circuits demand power hungry OPAMP to respond fast and accurate, usually, the finite OPAMP speed also limits the conversion speed of IADCs. To overcome these limitations, this work proposes a hybrid two step ADC to provide large conversion speed with lower power consumption.

Figure 3.2(a) illustrates the proposed two step ADC, it includes a 2nd order feedforward ICT ADCs working at oversampling frequency and a SAR ADC at nyquist frequency. The residual error is extracted at the last integrator output of the last cycle in every conversion from ICT ADC and transfer to the 2nd SAR. Half period excess loop delay (ELD) is utilized to tolerate the delay of the internal quantizer and data-weighted averaging (DWA) logic in the ICT ADC. Therefore, the feedback DAC output has half cycle delay of the quantizer output, and the reset of the CT integrator is synchronized with DAC output as given in Figure 3.2(b),. Usually, the DAC also introduces delay causing the last cycle (Mth) DAC output in previous conversion leak to the 1st cycle of next conversion. Since the weight of the first modulator output is highest in its decimation filter of IADCs, the signal dependent errors from previous Mth cycle lead to large harmonics and increase noise floor. To solve this issue, the DAC output is reset to a fixed value 0 at Mth cycle to avoid signal dependent leakage which is implemented in the digital control logic of DAC. There are M-

1 effective DAC outputs enter the loop filter, and one cycle delay is introduced in path1 to match it.

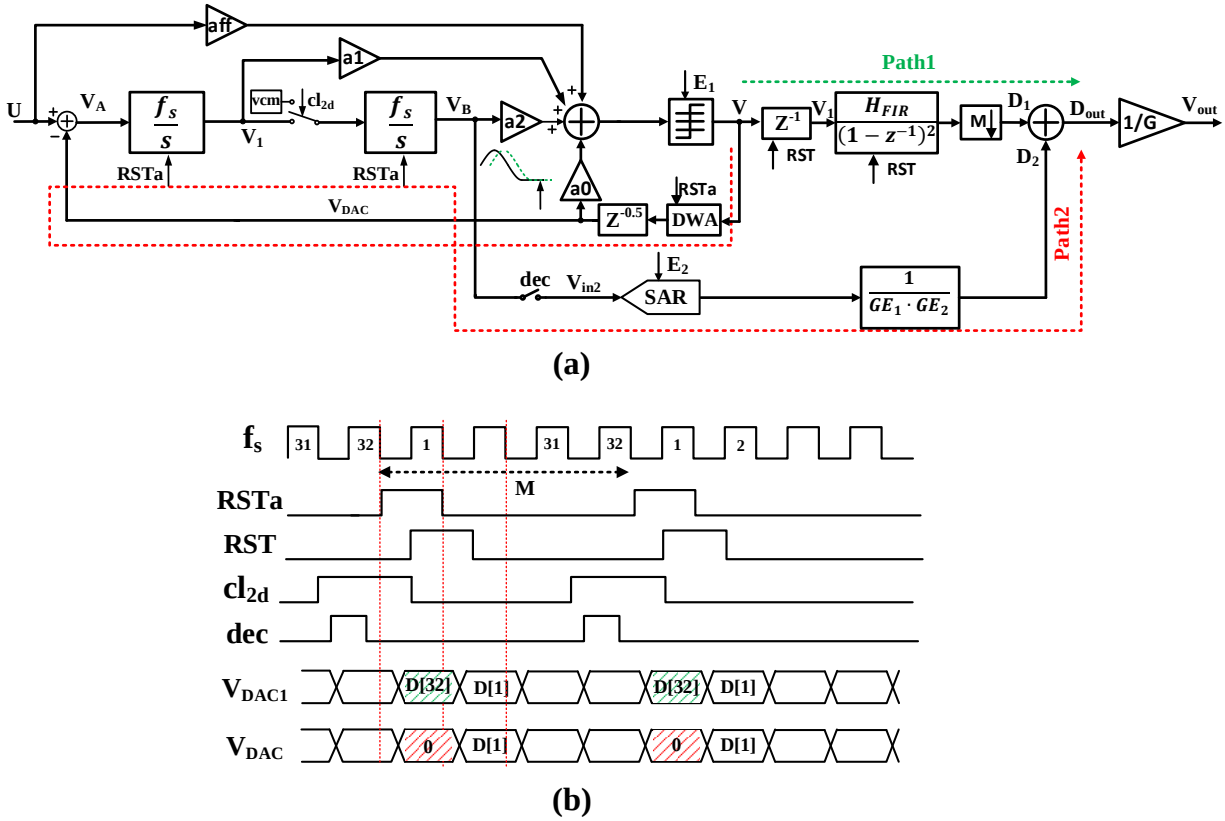


Figure 3.2: (a) The hybrid extended Counting ADC, (b) simplified timing of the hybrid ADC

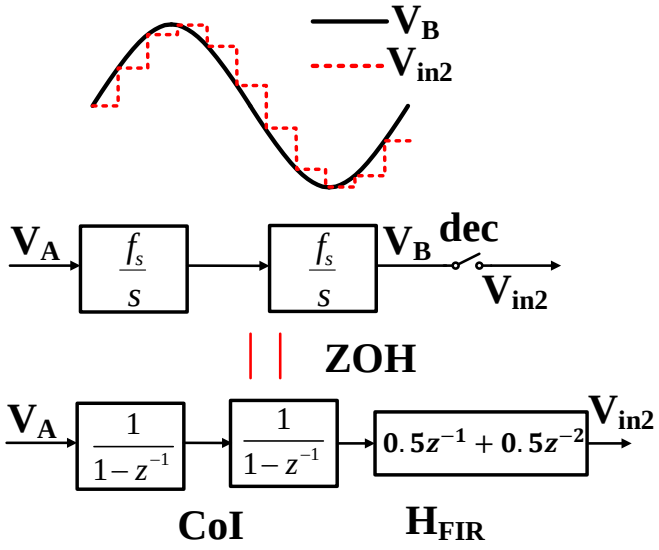


Figure 3.3: ZOH for the CT CoIs

The decimation filter of ICT ADC equals to the transfer function between V_A and V_B in Figure 3.2(a), and the gain error correction block is added at the 2nd SAR output to normalize the gain error comes from the CT blocks. The proposed ICT-SAR two step ADC is designed and analyzed in time domain. The residual error of ICT ADCs needs to be sampled correctly in time domain to do the extended counting operation. Also, the following stage is a SAR ADC based on switch capacitor circuit. Thus, zero-order-hold (ZOH) transformation is used to figure out the equivalent DT transfer function of the CT cascade of integrators (CoI), it becomes two cascade non-delay integrators and one finite-impulse response (FIR) term as presented in Figure 3.3. The decimation filter transfer function becomes

$$H(z) = \frac{0.5 \cdot z^{-1} + 0.5 \cdot z^{-2}}{(1 - z^{-1})^2} \tag{3.13}$$

Comparing with the decimation filter is Figure 3.1, the denominator becomes a FIR term. Figure 3.4 presents the bode plots of the two different decimation filters for ICT ADC with ZOH and IIR transformation. The filters have similar AC response within signal band, but high frequency responses are different. As discussed in Figure 2.19, the ZOH transformation has smaller peak in the spectrum which may fold back to in-band in the IADCs, therefore, the ZOH is chosen. It also helps reduce the DAC ISI errors due to less high frequency transitions.

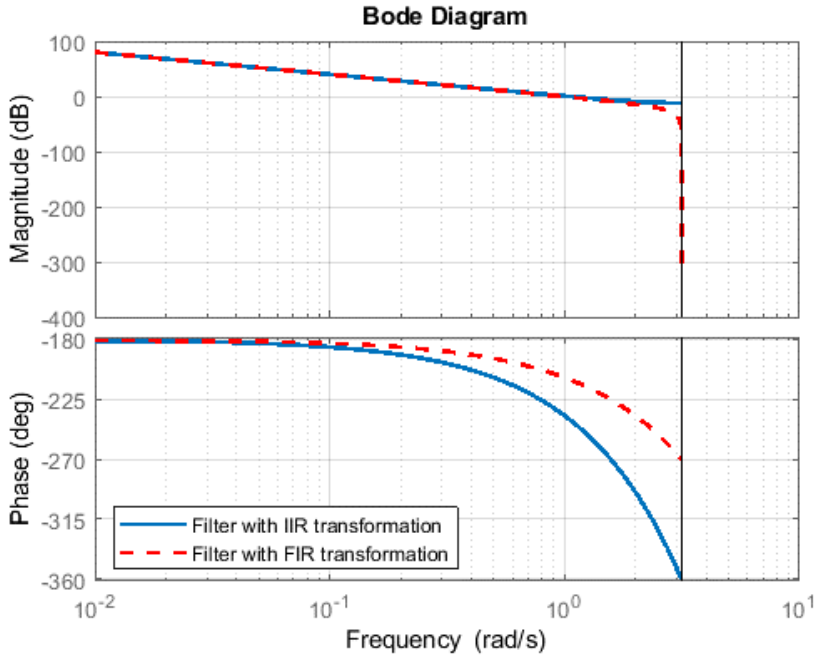


Figure 3.4: Bode plots of decimation filters with FIR and IIR transformation

With ZOH transformation for CT CoIs, GE_1=GE_2=1 for ideal CT integrators,

$$\frac{0.5\cdot z^{-1}+0.5\cdot z^{-2}}{(1-z^{-1})^2}\cdot[U(z)-V(z)]=V_B(z) \tag{3.14}$$

$$V_B(z)+E_2(z)=D_2(z) \tag{3.15}$$

Then the two step ADC input and output have the following relationship:

$$\frac{0.5\cdot z^{-1}+0.5\cdot z^{-2}}{(1-z^{-1})^2}\cdot U-\frac{0.5\cdot z^{-1}+0.5\cdot z^{-2}}{(1-z^{-1})^2}\cdot V(z)=D_2(z)-E_2(z) \tag{3.16}$$

Since the input signal can be simplified as a constant value for all the modulator outputs in one conversion, the time domain equation becomes

$$U=\frac{\sum_{K=1}^{M}\sum_{i=1}^{K}(0.5\cdot V[i-1]+0.5\cdot V[i-2])+D_2[M/OSR]-E_2[M/OSR]}{M\cdot(M+1)/2} \tag{3.17}$$

If the ENOB of the SAR is also N bits, the ICT-SAR hybrid two step ADC achieves the same SQNR as the IDT-SAR two step ADC

$$SQNR_{hybrid-step}=2\cdot 20log_{10}(M)+6.02\cdot N-6 \tag{3.18}$$

Where M is the oversampling ratio, N is the ENOB of 2nd SAR. Since the CT integrator output is changing during operation, the SAR needs to sample instantly to get the residual error correctly. To relax the speed requirements of SAR, the 2nd integrator inputs are shorted to VCM making the integrator hold the residual error to give longer time for SAR to sample.

The benefits of this architecture is the 2nd SAR SQNR contribution is the same as the internal quantizer of the IADC, but it locates outside the loop filter and the latency of SAR does not affect the DSM stability. Second, the transfer function mismatch of the CT CoIs and its equivalent DT decimation filter results in NTF_1*E_1 leakage which is smaller than extracting E_1 scheme. Finally, only the order of the 1st ICT ADC determines the SQNR instead of its NTF.

3.3 System level modeling

A design example of a 16b 1MHz BW ICT-SAR two step ADC is modeled and simulated in MATLAB. The first ICT works at fs=64MHz, with OSR=32 and the 2nd step is a 8 bits SAR. From (3.18), the NTF of the first ICT modulator does not affect SQNR, therefore, the NTF=2.2 is selected for the modulator. The NTF needs to ensure the stability of the modulator when including the RC variation and also it should not be too large to increase the DAC dynamic errors by causing more high frequency quantization noise. The non-idealities of the DAC limit the resolution of the ADC

and the finite OPAMPs parameters in the CT integrators degrade the SQNR as well. Therefore, these non-idealities need to be modeled properly to finalize the sub-blocks design parameters.

With all blocks ideal, the simulated FFT results of the first ICT and the two step ADC are illustrated in Figure 3.5 and Figure 3.6. The quantization noise is reduced by around 24dB corresponding to 4bits resolution. This results match the equation (3.18), since the 2nd step 8bits SAR makes the quantization noise 1/(2^4) smaller than the 4bits flash quantizer.

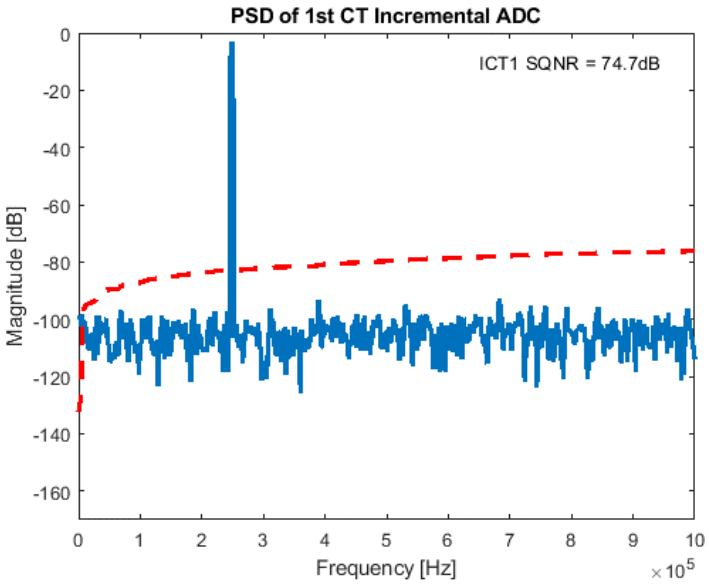


Figure 3.5: PSD of the ICT with ideal Simulink Model

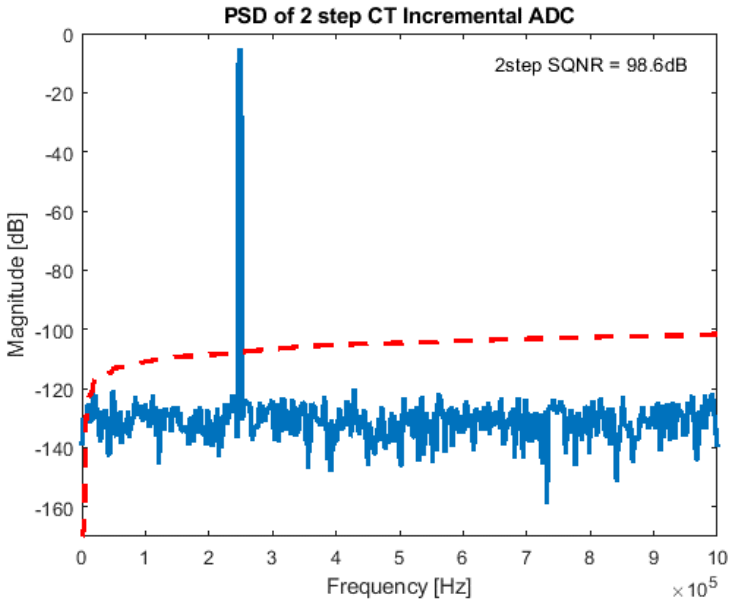


Figure 3.6: PSD of the two step ADC with ideal Simulink model

3.3.1 DAC non-idealities analysis

Current DACs are widely used in high resolution large bandwidth continuous time ADCs, since they feature high output impedance making the virtual ground movements and power supply noise have less impact on the DAC linearity. In the current DACs, both the dynamic errors and static errors degrade the DAC performances.

Current mirror DAC output waveforms mostly depend on the sensitivities to clock jitter and inter-symbol-interference (ISI) error. Similarly, both of these non-idealities appear when the DAC output experiences transitions. But, the clock jitter degrades performance by modulating a random phase noise to every transition and it is relative to the DAC output step amplitude. While ISI error is introduced by the constant charge difference between rising edge and falling edge of the current waveform.

The current DAC implementations include return-to-zero (RZ) DAC [32] and non-return-to zero (NRZ) DAC [33]. Figure 3.7 shows the jitter and ISI error model for these two types of DAC. As given in Figure 3.7, NRZ DAC has smaller jitter noise, but the ISI error is signal dependent. Especially, in multi-bit DAC, the ISI error dominants performance due to the increasing transition density caused by data-weighted-averaging (DWA). Meanwhile, in RZ DAC, the same ISI error happens at every clock period and the ISI error becomes a constant error instead of signal dependent error making RZ DAC ISI free. As shown in Figure 3.7, RZ DAC has more transitions and larger output current, both of which increase the jitter noise. Besides, in RZ DAC, a faster clock signal is necessary for generating control signal in DAC and the total power consumption of DAC drivers is increased. Also, the OPAMPS design budget is increased to process larger DAC output current.

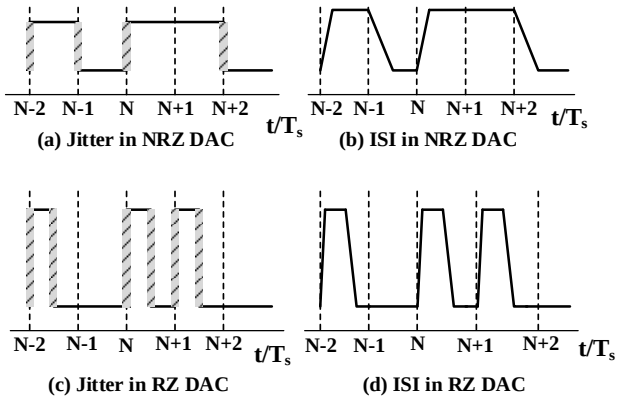


Figure 3.7: Jitter and ISI model in RZ and NRZ DAC

Based on previous discussions, the ISI error dominants performance in NRZ DAC while the jitter noise limits the SNDR in RZ DAC. And Dual-return-to-zero (DRZ) DAC presented in Figure

3.8, combines the benefits of both RZ and NRZ DAC [33]. DRZ DAC topology contains two identical RZ DAC. The summation current of their output behaves like a NRZ DAC making they have the same jitter tolerance as RZ DAC. However, extra power consumption in DAC driver circuitry is needed since the double clock frequency. To achieve low jitter and ISI error, the DRZ DAC is chosen for this design, and the DAC jitter, ISI error and static error coming from current mismatch are modeled in MATLAB SIMULINK.

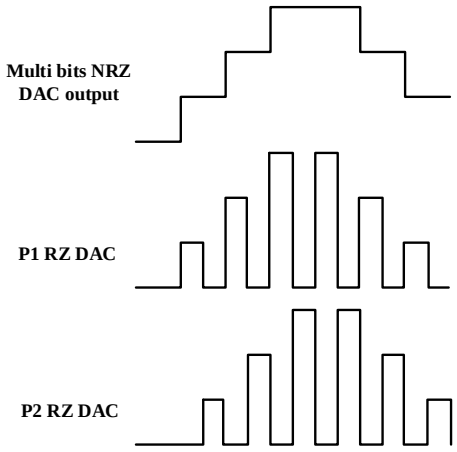


Figure 3.8: Multi-bit DRZ DAC

The jitter in Figure 3.5(a) can be expressed as

$$e_{j,NRZ}(n) = [y(n) - y(n-1)] * \frac{\Delta t(n)}{T_s} \tag{3.19}$$

Where v[n] is the DAC output, Δt is the clock jitter of every clock cycle. From (3.19), the jitter error is determined by the DAC output step and the clock source jitter.

The jitter model of NRZ and DRZ DAC are compared in Figure 3.9.

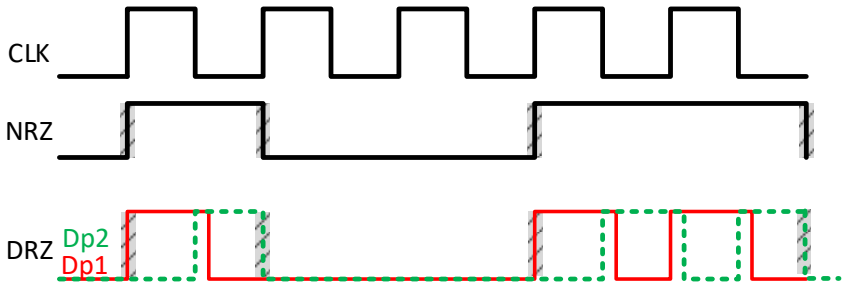


Figure 3.9: Jitter model comparison of NRZ and DRZ

As shown in Figure 3.9, the jitter error in NRZ DAC happens at the transition edges of the DAC output. In the DRZ DAC, the two sub-cells are controlled by the same clock with invert phases,

therefore, the clock jitter can be canceled when these two sub-cells have inverse transitions. As a result, the over-all jitter of the DRZ DAC happens only when one of the sub cell has transitions, making it have the same jitter noise as the NRZ DAC.

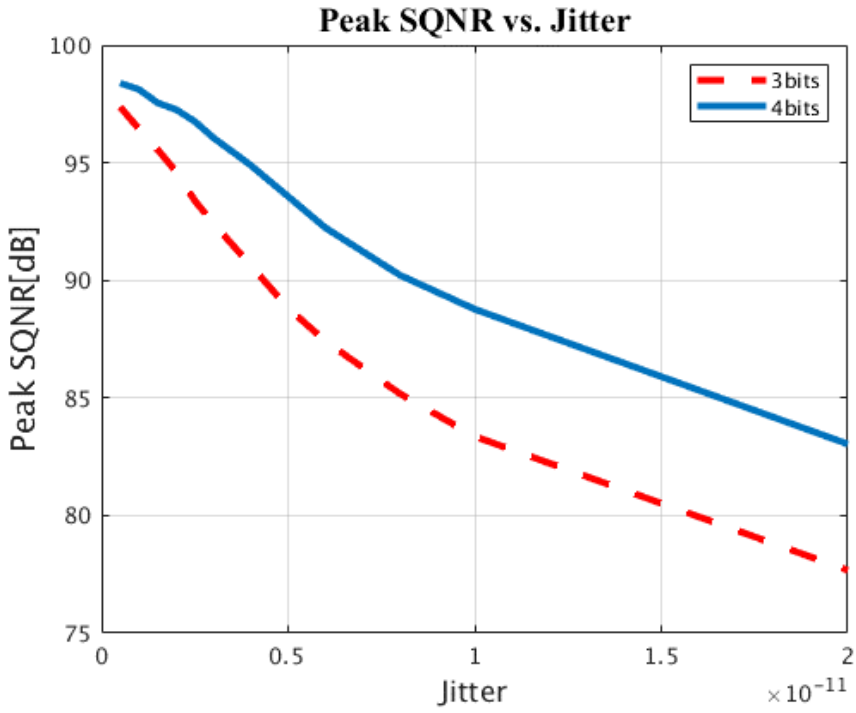


Figure 3.10: Peak SQNR vs. jitter values with 3bits and 4bits internal quantizer

Usually, the arbitrary waveform generator has 1-2ps rms jitter for clock at hundreds of MHz. The jitter noise is added when DAC output has transitions. The simulated SQNR vs RMS jitter values of the two-step ADC is shown in Figure 3.10. With 4bits quantizer for the 1st ICT ADC internal quantizer, the SNDR is still larger than 96dB at 2ps jitter value which is sufficient for this design. Therefore, 4bits internal quantizer is required to tolerant the jitter nosie in the ICT ADC.

Figure 3.11 (a) presents the NRZ DAC ISI model, when the DAC output rising and falling edges have mismatches, the ISI error happens, the rising and falling edge mismatch Δ_p represents the ISI error for the DAC out. The ISI error is modeled at 0 to 1 transition edge of DAC output. While in the DRZ DAC, the two sub-cells have transitions as long as the dac output is 1, and $\Delta_p$is added for every high level DAC output. Therefore, the error becomes a constant gain error instead of signal dependent dynamic errors as illustrated in Figure 3.11(b).

With 2ps RMS jitter, 0.4% static error and 0.1%T_s ISI error for DRZ DAC, the simulation results from MATLAB are given in Figure 3.12 and Figure 3.13. The SQNR of the two step ADC is higher

than 96dB. Therefore, the DRZ 4bits current DAC with DWA can provide 16bit linearity for the design.

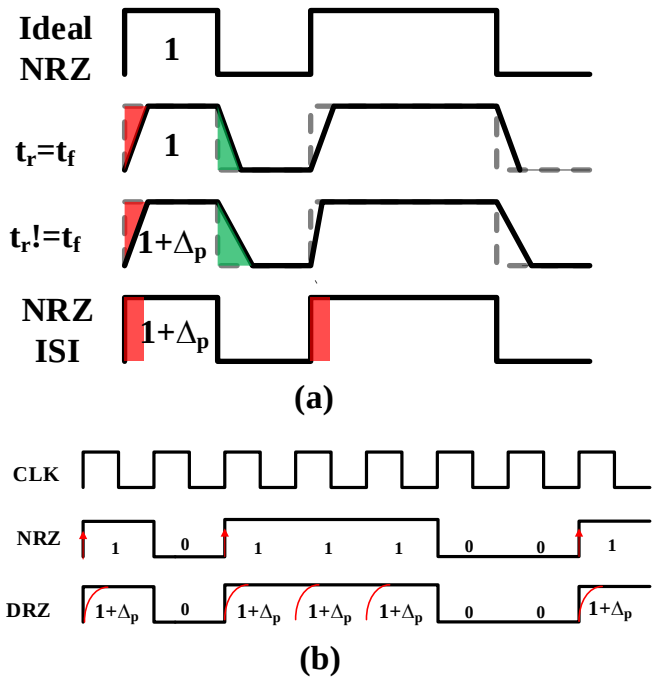


Figure 3.11: (a) NRZ DAC ISI model, (b) NRZ and DRZ ISI comparison

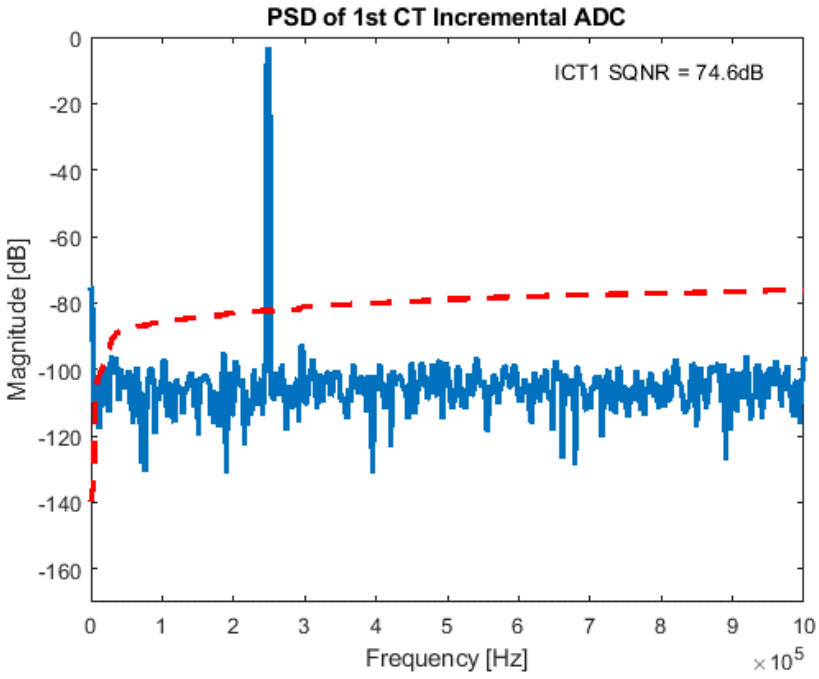


Figure 3.12: FFT of ICT with DAC non-idealities

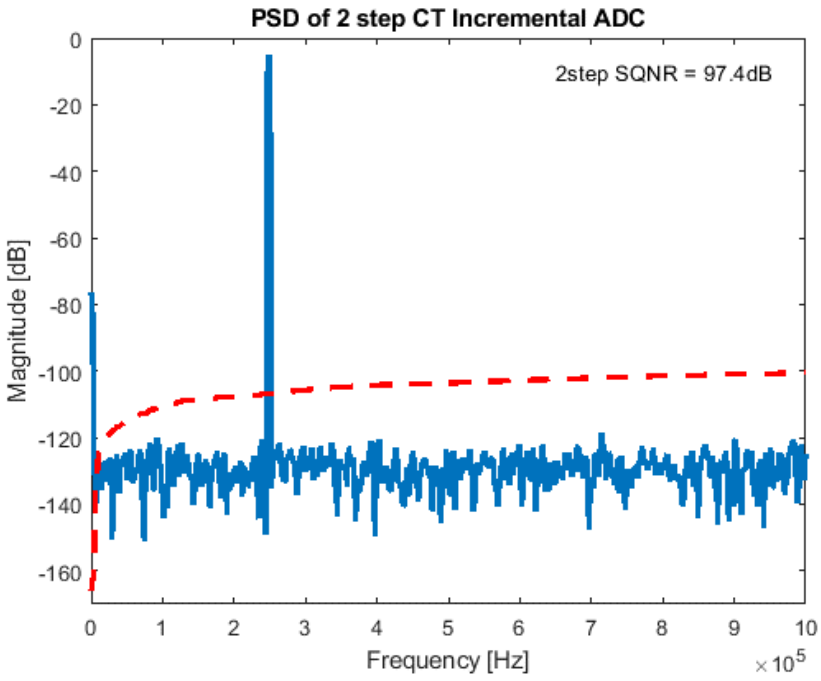


Figure 3.13: FFT of two-step ADC with DAC non-idealities

3.3.2 OPAMP Non-idealities

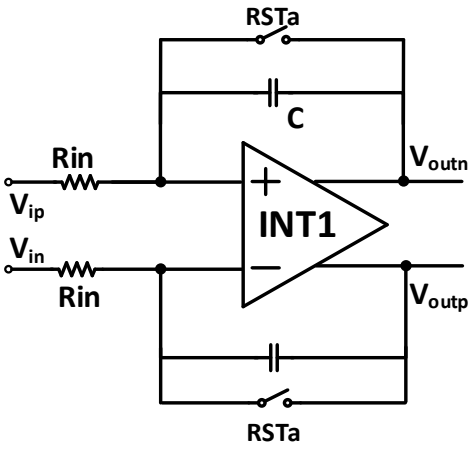


Figure 3.14: CT Incremental RC integrator

A CT Incremental RC integrator is shown in Figure 3.14. Considering the finite parameters of OPAMPs in the integrator, its transfer function can be expressed as[32]

$$I_s(s) = \frac{1}{\frac{s^2 CR}{\omega_u} + s\left[\frac{1}{\omega_u} + CR + \frac{CR}{A_0}\right] + \frac{1}{A_0}} \tag{3.20}$$

Here, A_o is the amplifier's DC gain in the OPAMP, ω_u is the unit gain bandwidth (UGB) of OPAMP. R and C are the input resistor and feedback capacitor of the integrator. The integrator gain k is defined by$1/RC = k*f_s$ and if $A_o>>1$, the integrator transfer function becomes

$$I_s(s) = \frac{kf_s}{s} \cdot \frac{\omega_u/(k \cdot f_s+\omega_u)}{1+s/(k \cdot f_s+\omega_u)} \tag{3.21}$$

As (3.21) shows, the finite ω_u of integrator and RC variations contribute a gain error GE and an additional pole f_p. The integrator gain can be normalized to k=1, defining the gain error GE and the extra pole f_p as

$$GE = \frac{\omega_u}{f_s+\omega_u} \tag{3.22}$$

$$f_p = f_s + \omega_u \tag{3.23}$$

Then the RC integrator transfer function is simplified as

$$I_s(s) = \frac{f_s}{s} \cdot \frac{GE}{1+s/f_p} \tag{3.24}$$

The finite integrator parameters cause mismatch between the CT CoIs and the digital decimation filters transfer functions as shown in Figure 3.2, and it leads to quantization noise E_1 leakage. To solve this problem, the constant gain errors GE can be calibrated at the SAR output as given in Figure 3.2(a), and the extra pole affection can be reduced by increasing the UGB of OPAMPs.

The finite OPAMP parameters are modeled in MATLAB based on equation (3.24), the SQNR versus UGB, and SQNR versus DC gain plots are shown in Figure 3.15 and Figure 3.16. In Figure 3.15, the integrator gain error comes from the finite UGB of OPMAPs are corrected at the 2nd SAR output. When the UGB is higher than $4f_s$, the SQNR of the two step ADC is stable, and the extra pole influence is negligible. In the CT integrators, the OPAMP settling accuracy is relaxed and more than 55dB DC gain is enough.

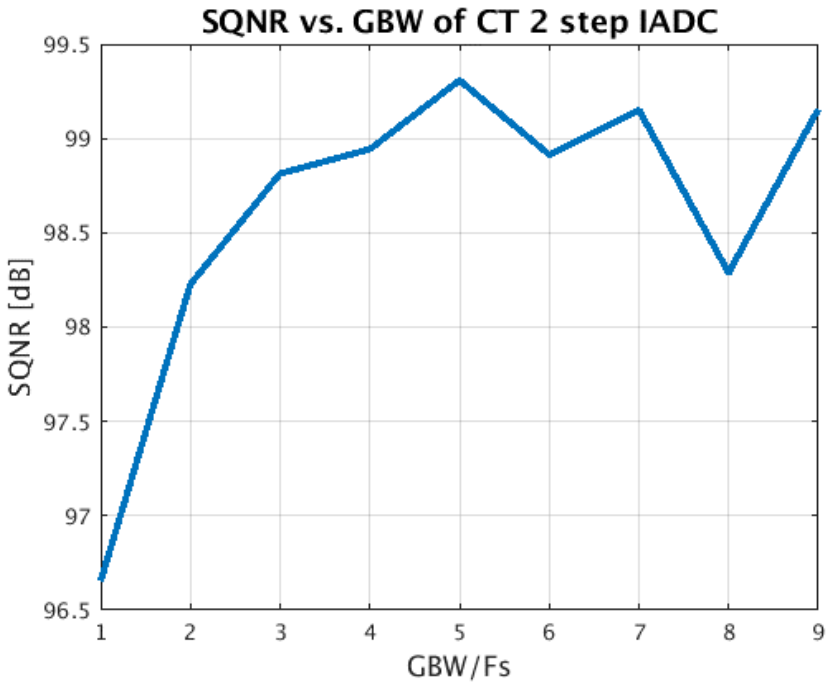


Figure 3.15: SNDR versus UGB of OPAMP in integrator

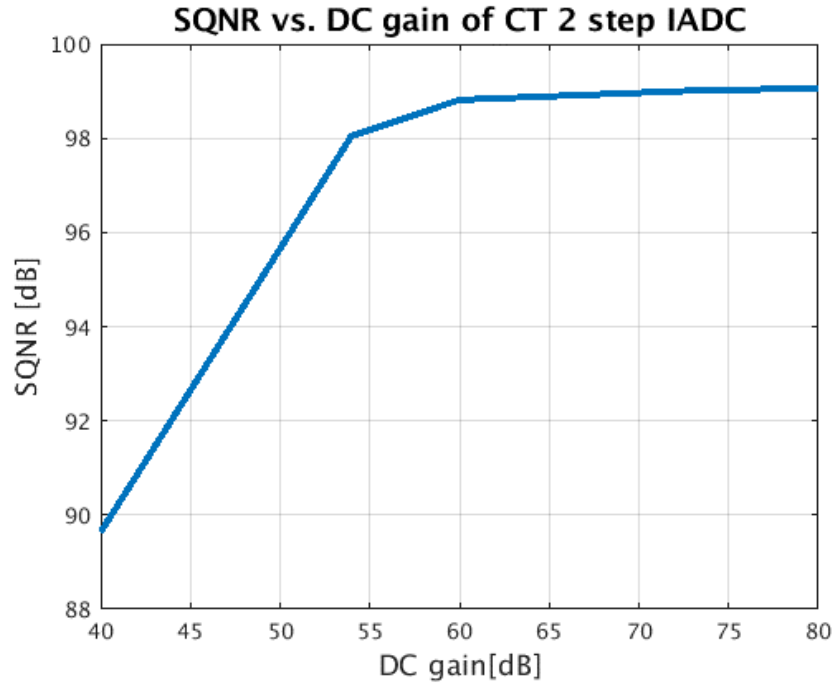


Figure 3.16: SQNR vs. DC gain of OPAMP in integrator

Chapter 4 : Circuit implementation and layout design of the ICT-SAR Two Step ADC

In this chapter, the circuit implementation is covered in detail. The design specs are summarized in the Table 4.1.

Table 4.1: Design specs of the circuits

Process	180nm
Supply	1.8V
SNDR	96dB
BW	1MHz
Fs	64MHz
OSR	32

4.1 Topology overview

Figure 4.1 illustrates the implementation of the proposed 2-step ADC architecture with 16b resolution and 1MHz BW. After reset of integrators, the integrator has a step response output illustrated in Figure 4(b) and the OPAMP needs to provide large current causing OPAMP to slew and obvious jump at the virtual ground. As a result, the DAC linearity becomes much worse at the first cycle and the performance of ICT ADC drops a lot since the first output has the highest weight in the decimation filter. The assistant gm and non-return-to-zero (DAC) are introduced at the first integrator output to track the input and DRZ output currents which relaxes the output current requirement of OPAMP [34]. With the assistance blocks, the 1^{st} opamps only need to handle the current difference of the input branch and the assistance blocks. As a result, the first opamps can always work in the normal region and the 1^{st} integrator can have fast response to after the reset. Also, the virtual ground becomes cleaner and help improve the DAC linearity. Since the assistant blocks locate at the 1^{st} integrator output, their linearity will not affect the ADC performance. The NRZ DAC is utilized to save the digital driver power. As discussed in Chapter 3, a 4 bits internal flash quantizer is implemented to enable the DAC to tolerate 2ps rms clock jitter noise. The 4 bits dual-return-to-zero (DRZ) DAC converts the dynamic ISI error of each DAC cell to signal independent static error which can be averaged out by the DWA. The excess loop delay DAC is implemented as a resistance-DAC to save current.

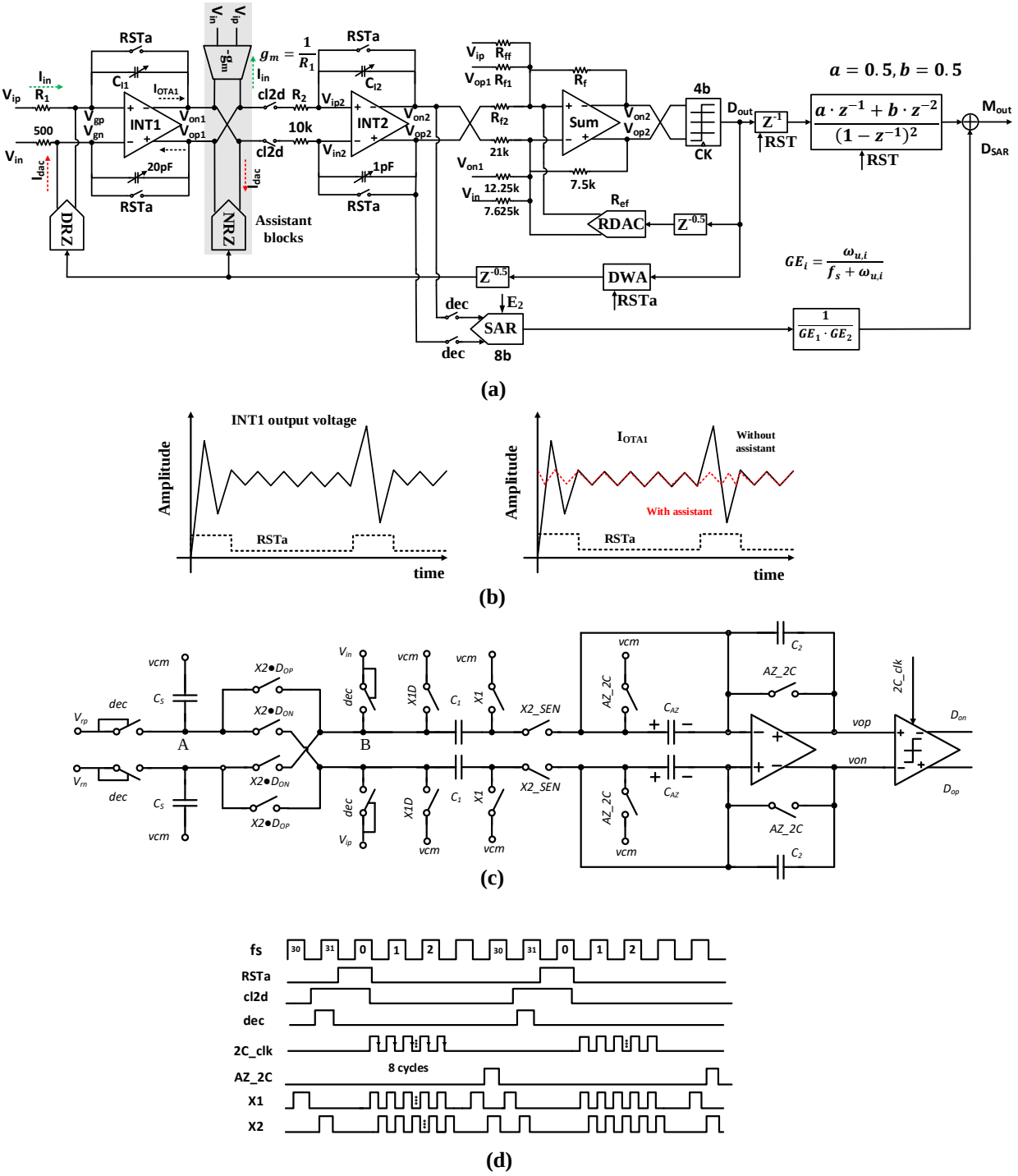


Figure 4.1: (a) circuits implementation of ICT1, (b) first integrator output response, (c) 2C-SAR circuit, (d) timing of the ICT-SAR ADC.

The second SAR is implemented as 2C SAR ADC [35]. The 2-C DAC is constituted by C_s and C_1, and the charge sharing between them every cycle forms the SAR operation. The parasitic capacitors mismatch at node A and B degrade the DAC linearity. To tolerate 20fF mismatch capacitor and get

8bits linearity, 1pF capacitor is chosen for C_s and C_1. And the auto-zero technique helps reduce the opamp low frequency noise. The advantage of the 2C SAR ADC is it requires less number of DAC reference voltages, and the 2C SAR operation is all passive during conversion which saves power.

4.2 Integrator design

In ADC, the quantization noise, thermal noise from input resistor, DAC, OPAMPs contribute most of the noise. To realize more than 96dB noise floor, the noise assignment of different blocks in the ADC is shown in Figure 4.2.

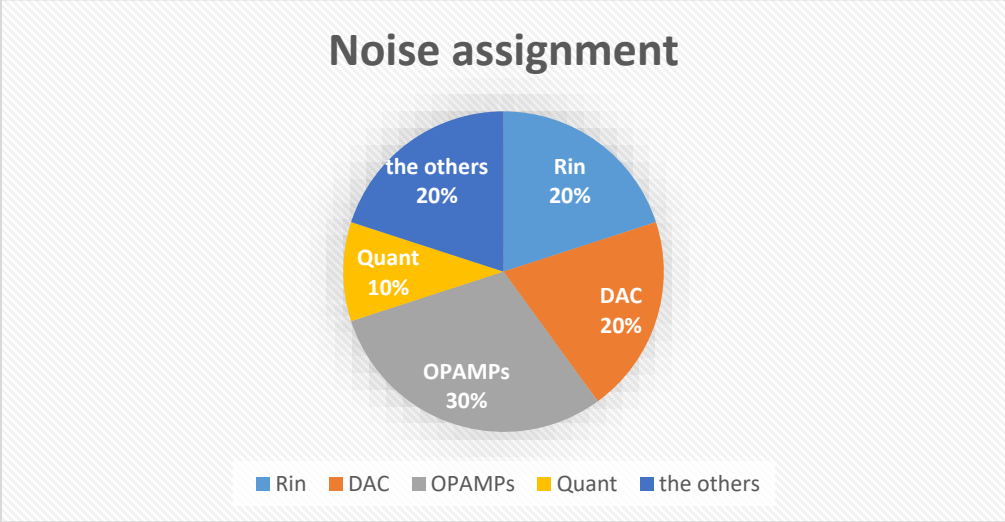


Figure 4.2: Noise assignment in ADC

4.1.1 Input resistor

In the first CT integrator in Figure 4.1(a), the thermal noise contribution from R_1 is

$$v_{n,R_1}^2 = 4kT \cdot R_{in} \cdot 2 \cdot f_B \cdot n_p \tag{4.1}$$

Where n_p is the noise penalty factor, for 2nd order Icremental ADC with OSR=32, n_p=1.31. The full input swing is V_{FS}=2*V_{dd}, then the input signal energy can be expressed as

$$P_{sig} = \frac{V_{FS}^2}{8} \tag{4.2}$$

The SNR dominated by R_1 becomes

$$SNR_{R_1} = 10 \cdot log_{10}\left(\frac{V_{dd}^2 \cdot \eta_{R_1}}{16kT \cdot f_B \cdot n_p \cdot R_{in}}\right) \tag{4.3}$$

Where the input resistor noise ratio $\eta_{R1} = 0.2$ is chosen as shown in Figure 4.2, the SNR versus the R_1 plot

is given in Figure 4.3. To achieve more than 96dB SNR within 1MHz signal bandwidth, the input R_1 needs

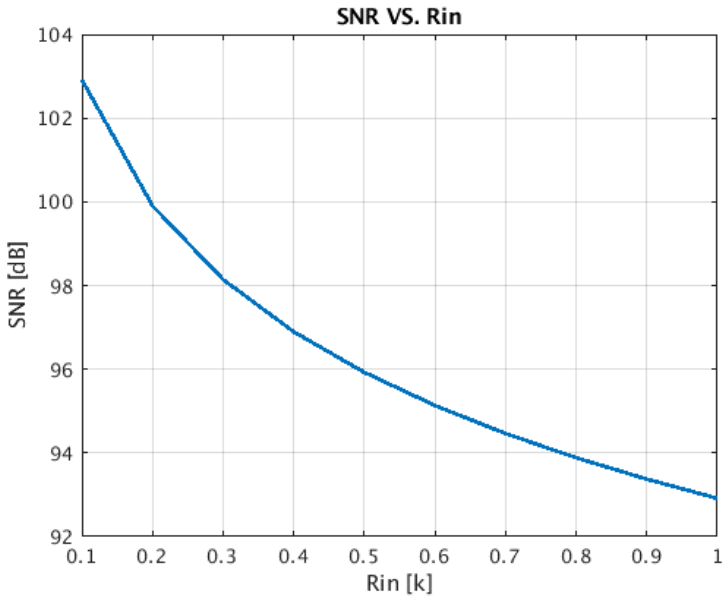


Figure 4.3: SNR versus R_1

to be smaller than 500 ohm.

4.1.2 Bootstrap switch

According to (3.21), to normalize the integrator gain requiring $1/R_1C_{i1}$=fs, 20pF integration capacitor is needed. To reset this large capacitor in one clock cycle, the turn on resistor of the reset switch should not be too large. The reset time constant is

$$\tau = R_{sw1}C_{i1} \tag{4.4}$$

It takes around 7τ to achieve 0.1% reset accuracy, and $7\tau \leq T_s$, so the R_{sw1} should be smaller than 110 ohm. Therefore, bootstrap switches are used to reset the first integration capacitors. If the first reset switch turn on resistance is too large and the capacitor cannot be reset to 0 completely, the previous conversion residual leaks to the next cycle which will increase both the noise floor and the distortions of the ADC. Considering the RC variation, the integration capacitors for C_{i1} and C_{i2} have 5b tuning range to cover +- 40% variation.

4.1.3 OPAMP

The OPAMP in the first integrator utilizes a power efficient two-stage feedforward compensation OPAs as shown in Figure 4.4(a). Their folded cascade first stage provides high gain, while the second stage provide large gm to drive the integration capacitor. Its simplified diagram is given in Figure 4.4(b), the feed-forward gm introduces a zero to cancel the non-dominant pole. Since the input of feedforward stage is the integrators virtual ground VCM, it limits the output stage output. Therefore, the input is capacitive coupled, and the output stage CMFB is implemented by a resistor. To increase the CMRR and block the noise from the ground, resistors are used at the source of feedforward transistors, which can increase their output impedance.

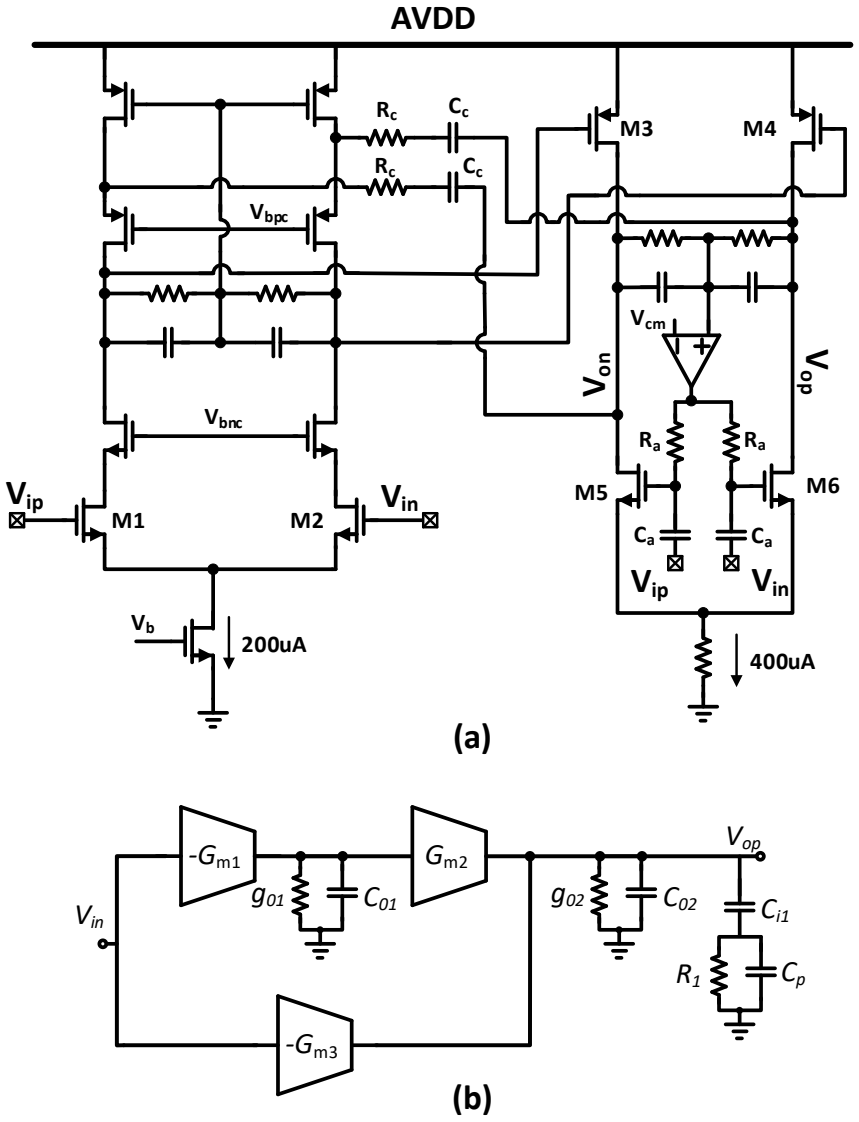


Figure 4.4: (a) Two-stage feedforward OPAMP, (b) simplified diagram of the OPAMP

The voltage drop on the resistor is only 50mV, which will not reduce the output swing too much. Its zeros and poles are given by the (4.5) and (4.6). In all the poles and zeros, w_{p2} and w_{z1} come from the R_a and C_a, and the zero is around half of the pole location. By choosing small R_a and C_a, this pole-zero doublet can be push to out of GBW of OTA_1. And the w_{p3} and w_{z2} come from the external load network, and they are close to the 1st dominant pole of the opamp. They will not change the GBW and PM at UGB, but it will degrade the input PM a lot. In time domain, there will be larger rings which decreases the ADC SNDR. So a compensation path including Rc and Cc are introduced to make the dominant pole far from load pole and thus increase the in band phase margin.

$$\begin{aligned}
\omega_{p1} &= \frac{g_{01}}{C_{01}} \\
\omega_{p2} &= \frac{1}{R_a C_a} \\
\omega_{p3} &= \frac{g_{o2}}{C_{o2} + C_I} \\
\omega_{p4} &= \frac{1}{R_{in}\left(C_{o2} + C_p\right)} \\
\omega_{z1} &= \frac{\omega_{p2}}{2} \\
\omega_{z2} &= \frac{1}{R_{in}\left(C_p + C_I\right)} \approx \frac{f_s}{2\pi} \\
\omega_{z3} &= \frac{g_{o1}}{C_{o1}} + \frac{g_{m2}}{g_{m3}}\frac{g_{m1}}{C_{o1}}
\end{aligned} \tag{4.5}$$

And the pole-zero cancellation relationships are

$$\begin{aligned}
\omega_{p2} &\approx \omega_{z1} \\
\omega_{p3} &= \omega_{z2} \\
\omega_{p4} &= \omega_{z3}
\end{aligned} \tag{4.6}$$

Except for the first integrator, the second integrator and the active adder utilize the same architectures.

4.2 DRZ DAC

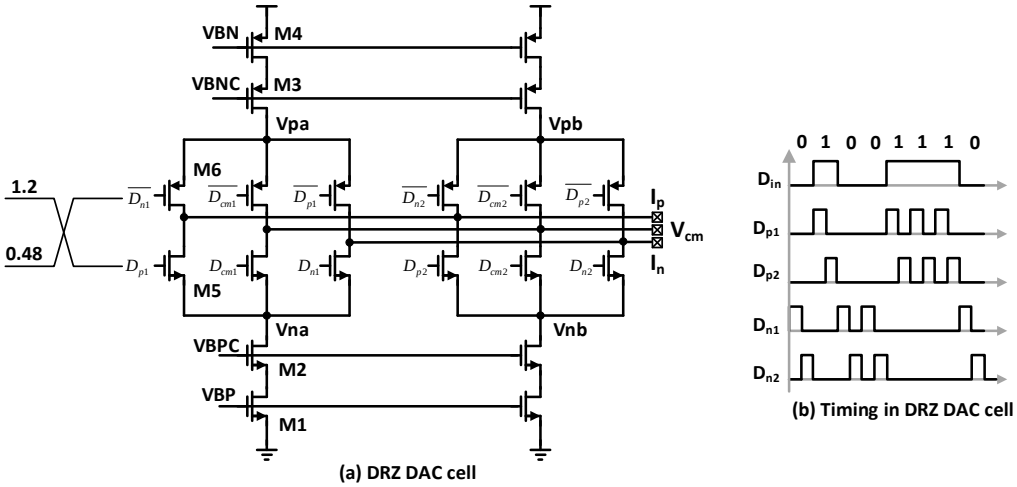


Figure 4.5: Schematic and timing of DRZ DAC

A commonly used DRZ is shown in Figure 4.5 [36], [37] and it includes a RZ DAC and a half delayed RZ DAC. The two sub-cells in the DRZ DAC output current alternatively, when one cell is active, the other one has current flowing between the power supply and ground in the middle branch to keep the top and tail current sources have constant currents. As a result the ISI error is reduced by avoiding the signal dependent error current coming from charging and discharging the parasitic capacitors in the current sources.

Since the I_p and I_n are connected to the first integrator virtual ground and they usually have a lot of movements. If the switches work in triode region providing small turn on impedance, the current source output nodes (Vpa, Vpb, Vna, Vnb) also sense the jumping at I_p and I_n which reduce the current mirrors accuracy and the output currents become signal dependent leading to the noise floor increment. To circumvent this drawbacks, the switches are biased in the saturation region by using smaller driven voltages of 0.48 and 1.2V. The large turn-on impedance of the saturate switches isolates the virtual ground from the current source and the supply noise can also has small influence to the virtual ground, both of which improve the DAC performances.

As shown in Figure 4.5, M1 and M4 contribute thermal noise to DAC output current while M2, M3, M5 and M6 do not output thermal noise. The thermal noise energy of one current DAC cell is

$$n_{DAC}^2 = 4kT \cdot \gamma \cdot (g_{m1} + g_{m4}) \cdot f_B \cdot R_{in}^2 \tag{4.7}$$

The SNR dominates by the DAC can be expressed as

$$SNR_{DAC} = 10 \cdot log_{10}\left(\frac{P_S \cdot \eta_{DAC}}{n_{DAC}^2}\right) \tag{4.8}$$

Where P_s is the input signal energy, and η_{DAC} is the DAC noise ratio in the overall noise of the ADC. As shown in Figure 4.1 (a), the input signal energy can written as

$$P_{sig} = \frac{(R_1 \cdot I_{DAC})^2}{2} \tag{4.9}$$

Then the SNR_{DAC} becomes

$$SNR_{DAC} = 10 \cdot log_{10}\left(\frac{V_{dd} \cdot V_{ov} \cdot \eta_{DAC}}{32kTf_B \cdot R_1}\right) \tag{4.10}$$

Where V_{ov} is the over dive voltage of current source transistors, η_{DAC} = 20% from Figure 4.2, R_1=500 ohm. To achieve more than 96dB noise floor within 1MHz signal bandwidth, the overdrive voltage of M1 and M4 should be larger than 400mV.

4.3 Assisted gm block

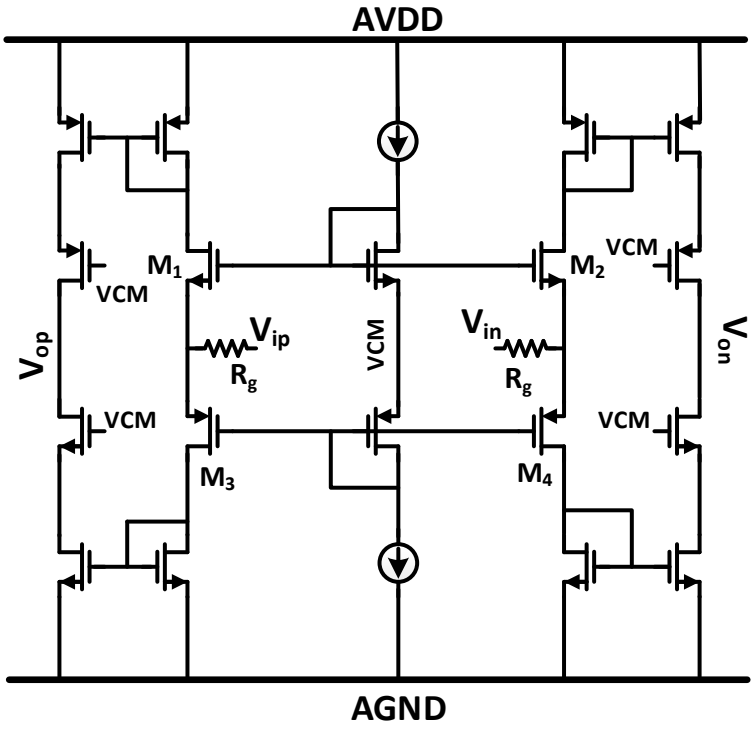


Figure 4.6: Assisted GM circuit

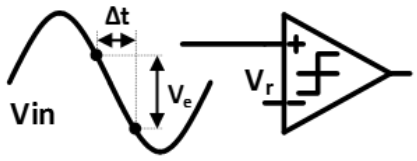
Since the assist gm block [39] input is the overall ADC input, its input range covers from gnd to vdd. To have the rail to rail input range, the input resistors are adopted to convert the input voltage to current. M1 and M3 are the class-AB control transistors. If the gm of M1 and M3 are too

large and the voltage at Vp and Vn will be very small. Then the current in M1 and M3 will not have big change and the class-AB operation is not insured. If the gm of M1 and M3 are too small, then most of input voltage will appear at Vp and Vn. M1 or M3 may go to triode region which will limit the linearity of the gm cell. To make it have class-AB operation and also have a good linearity. the gm values of M1 and M3 should be properly chosen. To have a trade of the linearity and gm matching with R_1, $Rg=2R_1=1k$ ohm is chosen in this design.

Any output offset current of this gm block need to be sink by the main OTA CMFB block. So it is necessary to increase the output current of the MAIN OTA to absorb the offset and non-linearity of GM.

4.4 Internal Flash quantizer

As illustrated in Figure 4.7, the input of quantizer keeps changing in a continuous time system, to have 4bits resolution and have one bit as margin, the input stage dominate pole fp needs to be 2^5 time larger than the input signal which is f_s here.



$$V_{emax} = \frac{dV_{in}}{dt}|_{max} = 2\pi f_{in} V_{ref} \times \Delta t_{max} < \frac{V_{ref}}{2^5}$$

$$\Delta t_{max} < \frac{1}{2\pi f_{in} 2^5}$$

$$\frac{\Delta Rad}{2\pi} = \frac{\Delta t_{max}}{T} = \frac{1}{2\pi f_{in} T_{in} 2^5}$$

$$\frac{f_{in}}{f_p} = \frac{\omega_{in}}{\omega_p} = \arctan\left(\frac{\omega_{in}}{\omega_p}\right) = \Delta Rad = \frac{1}{2^5}$$

$$f_p = 2^5 f_{in}$$

Figure 4.7: quantizer model in CT system

The internal 4b flash quantizer is shown in Figure 4.8 and it works at fs. To save power, the pre-amplifier is removed. A dummy MOS capacitor is added to the input differential pair to reduce the kick-back noise. clkd is a delayed signal of clk, and the delay needs to match the signal delay from M_{11} gate to drain to cancel the kick back noise perfectly.

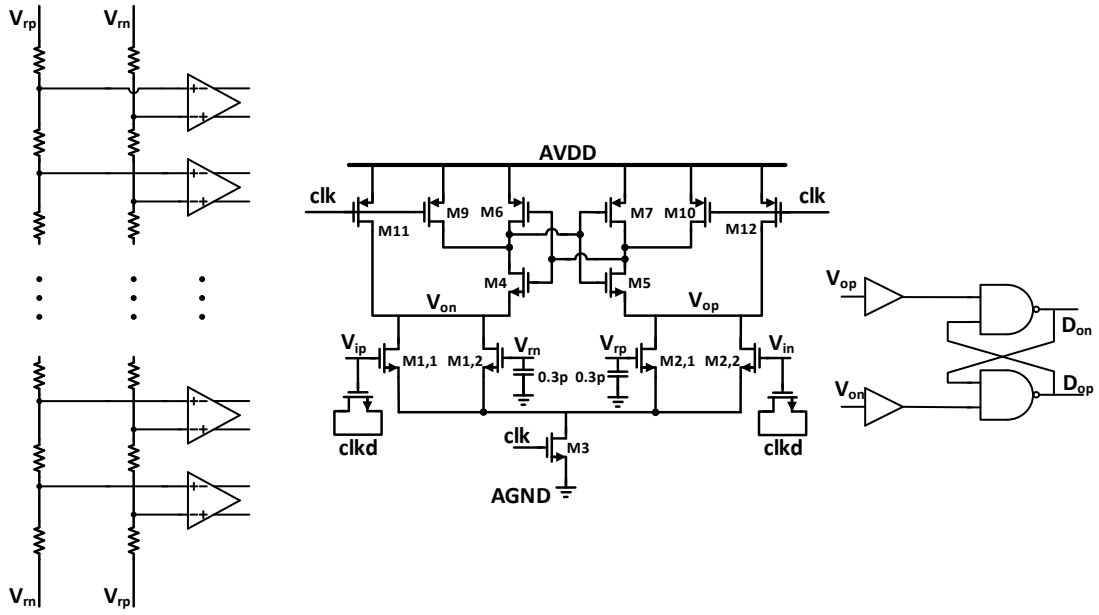


Figure 4.8: Flash quantizer and internal comparator

4.5 OTA in the 2C-SAR ADC

The 2C-SAR ADC needs an active OPAMP to do the charge transfer for the 2C DAC. A folded cascade opamp with switch-capacitor CMFB is illustrated in Figure 4.9.

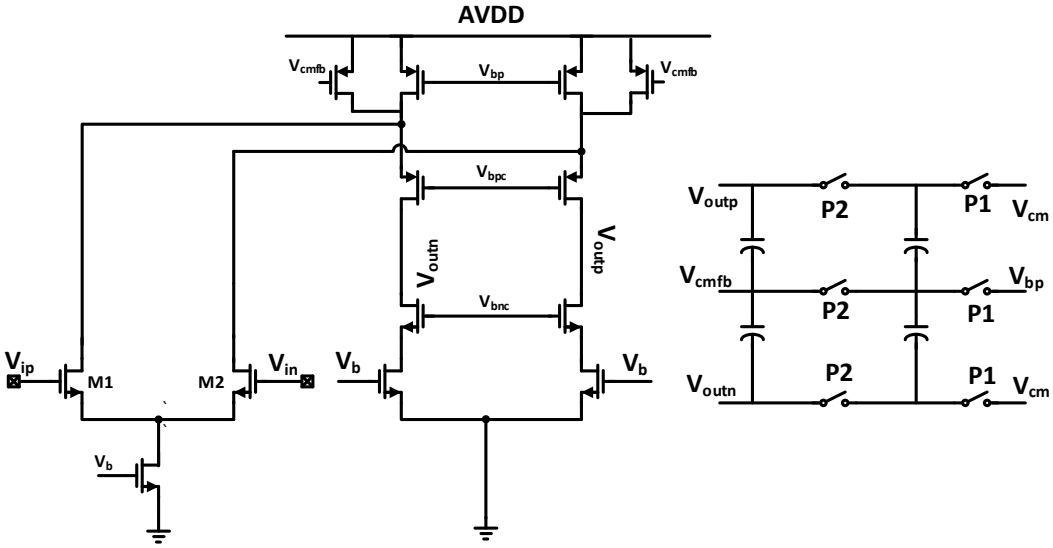


Figure 4.9: OTA in the 2C-SAR ADC

4.6 Circuit simulation results.

The sub-circuits simulated results are summarized in Table 4.2. With these values, the FFT results of the first stage and the two step ADC presented in Figure 4.1 are illustrated in Figure 4.10 and 4.11. The ICT provide 72.9dB SNDR and the two step ADC improve the SNDR to 91dB.

Table 4.2: Performance summary of OPAMPs in the loop filter (fs=64 MHz)

	DC gain (dB)	Closed loop UGB(Hz)	Closed loop phase margin(deg)	Power (mA)
INT1	59	520M	100	1.15
Gm	THD=-48dB			1
INT2(CT integrating)	70	470M	90	0.73
INT2(driving SAR)	70	300M	50	0.73
Adder	51	860M	87	1.13
OTA in SAR	54	340M	78	1.13

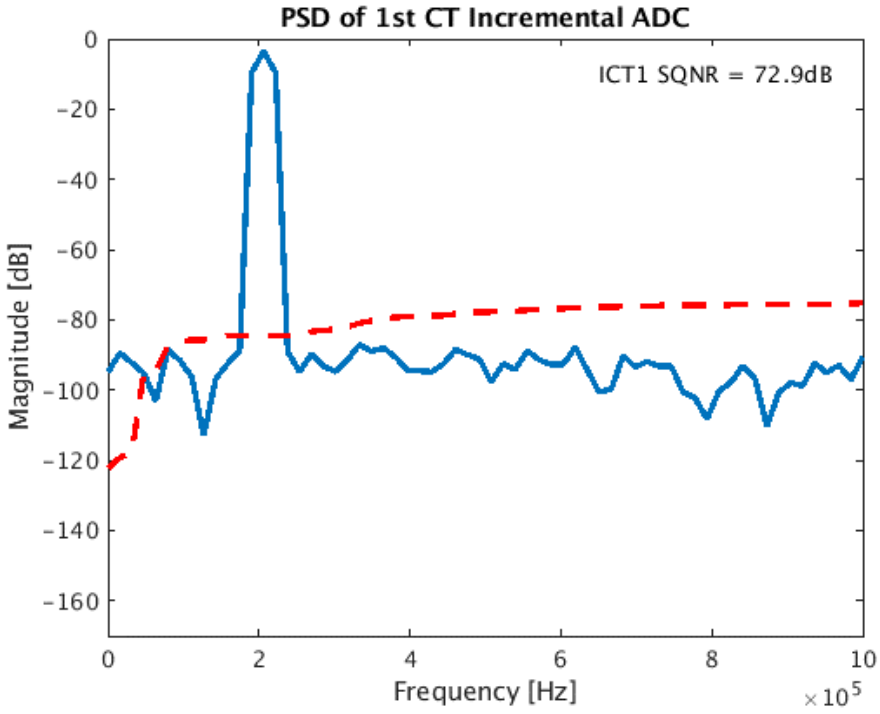


Figure 4.10: FFT results of ICT

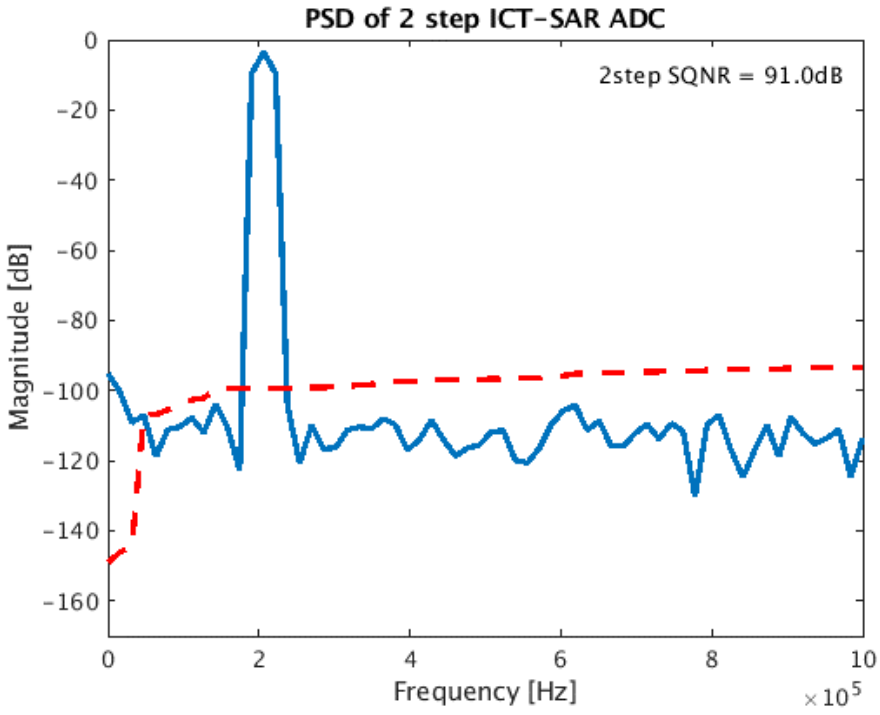


Figure 4.11: FFT of two-step ADC

Chapter 5 : Layout Design

The ADC is implemented in AKM 180nm CMOS process with 6 metal layers, 1.8V power supply devices are used and the chip occupies an area of 3.99mm^2. One important thing after the layout design is: the finite OPAMPs BWs of the integrators, output parasitic capacitor of the ELD DAC needs to be extracted for modeling their affects to NTF. Then using MATLAB SIMULINK to generate a new set of coefficients for the active adder to keep the same NTF and avoid stability issue of the ICT ADC.

The most important block with in the ADC is the DRZ DAC, it includes 16 NRZ DAC cells, its floor plan needs to be carefully designed to reduce the ISI and DAC mismatch errors. Figure 5.1 presents the layout of the DRZ DAC.

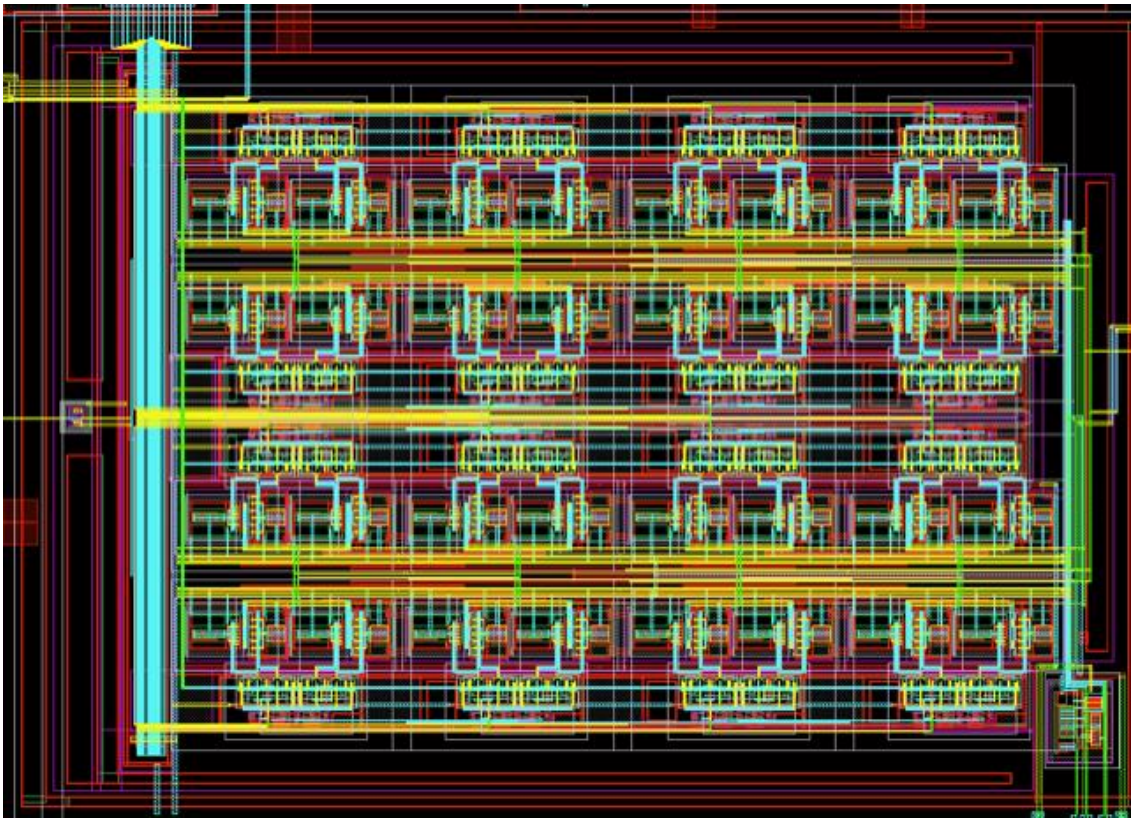


Figure 5.1: DRZ DAC layout

Its floorplan is shown in Table 5.1, every 4 cells are grouped together and placed common-centralized. And the 4 groups are also common central symmetric.

Figure 5.2 gives the overall layout of whole chip. The input two paths are fully symmetric and be shielded to avoid noise.

Table 5.1: DRZ DAC cells floorplan

0	7	5	3
9	15	13	11
10	12	14	8
2	4	6	1

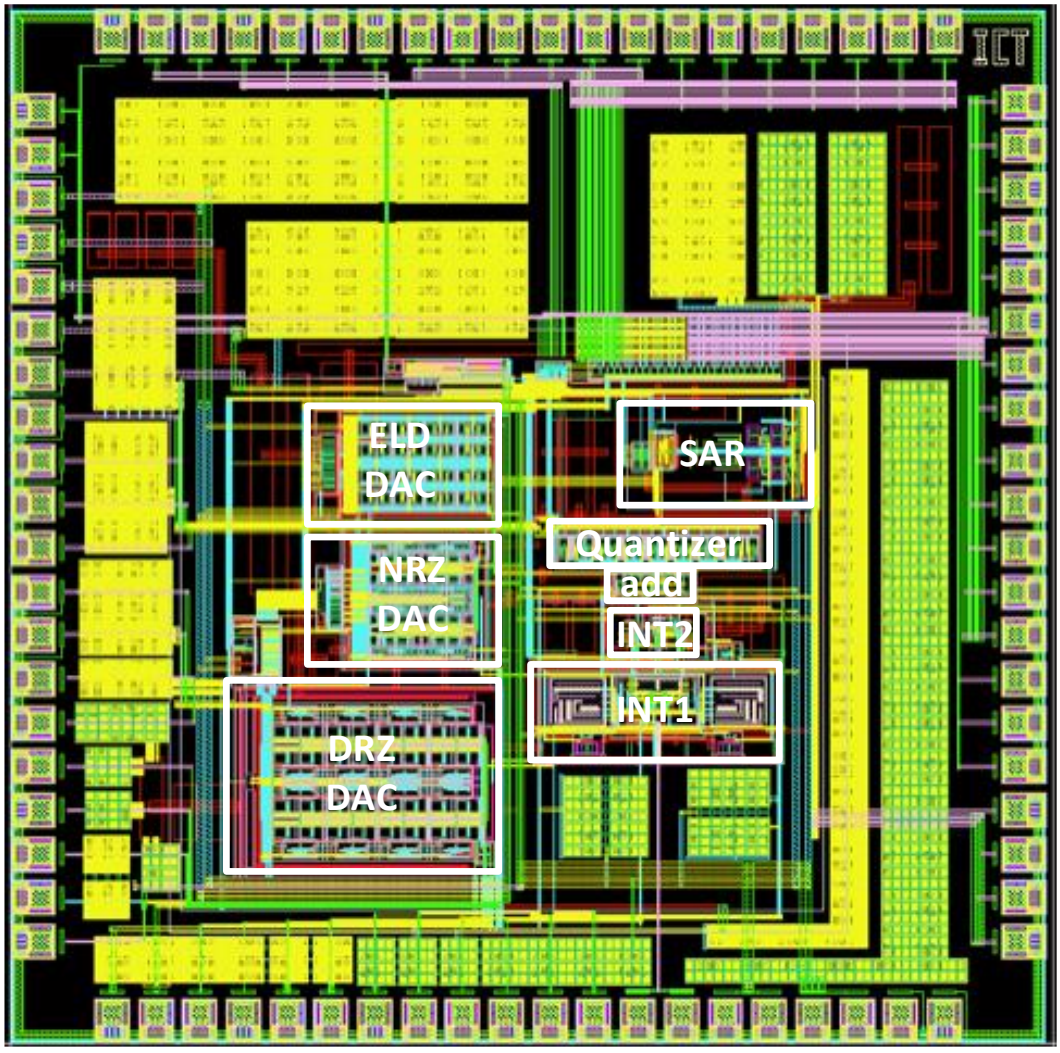


Figure 5.2: Layout design of the chip

The DRZ DAC needs to locate as close as possible to reduce the output signal delay and also the shorter routings reduce the INT1 virtual ground parasitic capacitors. In addition, the ELD DAC output routings introduce parasitic capacitors to the RDAC, the RC time constant slow the ELD

DAC and cause stability issues. Therefore, the unit-R in the ELD DAC cannot be too large and the output nodes also need to be close to the virtual ground of the active adder.

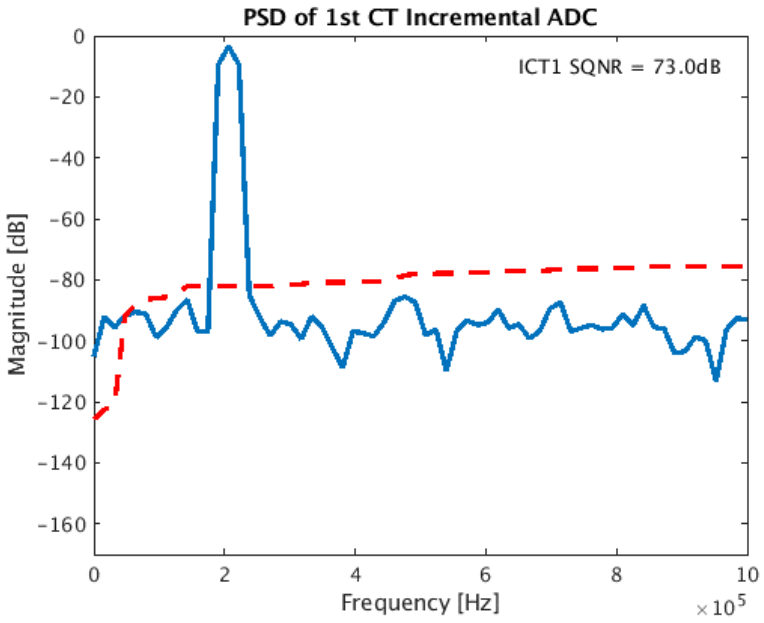


Figure 5.3: Post layout simulation results of the ICT ADC

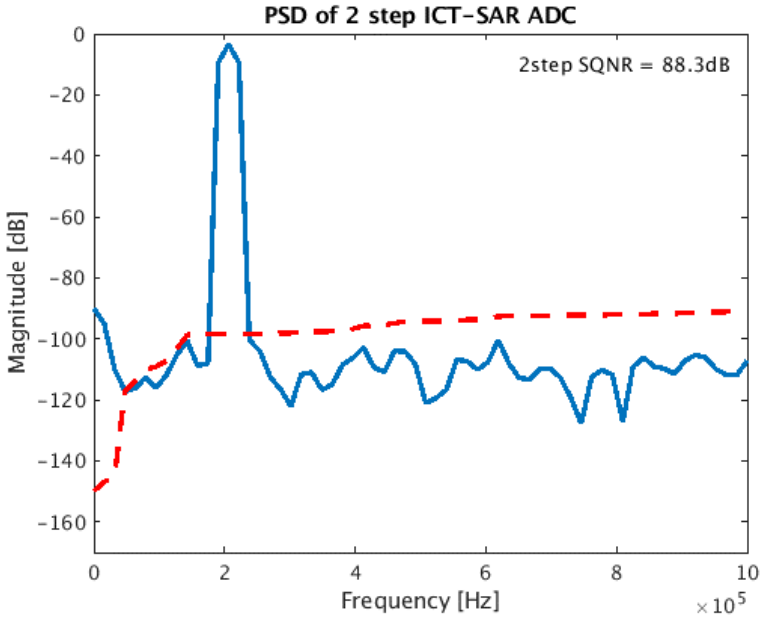


Figure 5.4: Post layout simulation results of two step ADC

To stable the reference voltages and currents when considering the inductor effect of the bonding wires, large decaps implemented by MOS caps are added inside the chip.

With CC extraction, the post layout simulation results are shown in Figure 5.3 and 5.4:

The die photo with floor plan indication is shown in Figure 5.5.

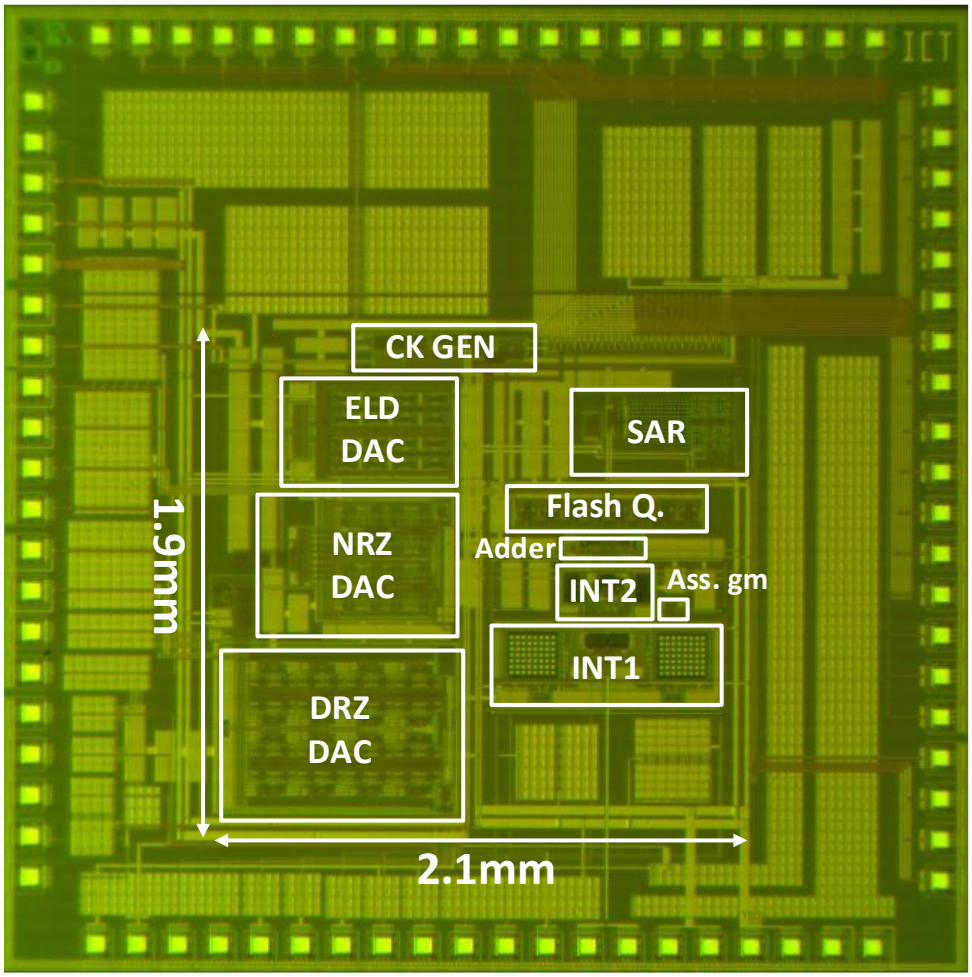


Figure 5.5: Die photo of the chip

Chapter 6 : Measurement Results

6.1 Test setup

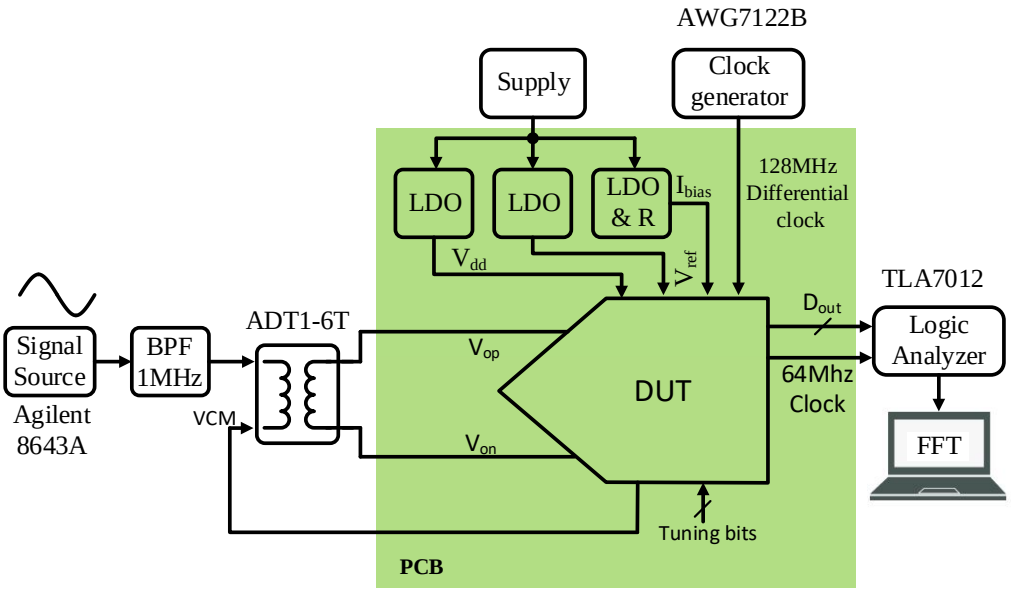


Figure 6.1: Test set up

The test setup is shown in Figure 6.1. The RF signal source Agilent 8643A output frequency covers from 260KHz to 1GHz. A passive BPF filter (Allen-Avionics F4526-1P0) helps reduce the noise floor of signal source output by around 20dB. Then a balun (Minicircuits-ADT1-6T) transform the single end signal to differential ones to drive the ADC. The clock generator (Tektronix AWG 7122B) can provide 128MHz clock with around 1.3ps rms jitter. The chip has divided by 2 digital logic circuits to generate 64MHz main clock from the external 128MHz clock, and this clock is also used to synchronize the logic analyzer (TLA7012). The power supply source gives +-5V voltages for the LDOs on board to generate the supply voltages, reference voltages and bias current for the chip.

The PCB design is presented in Figure 6.2. Four metal layers are chosen to fabricate the PCB board, with the ground and power supply locating between the top and bottom layers to isolates noise. The input, DRZ DAC references and clock signals are put close to the chip. To avoid power and ground plan noise coupling, the analog, digital, DAC and clock ground planes are split with an inductor to ensure they have the same DC voltages.

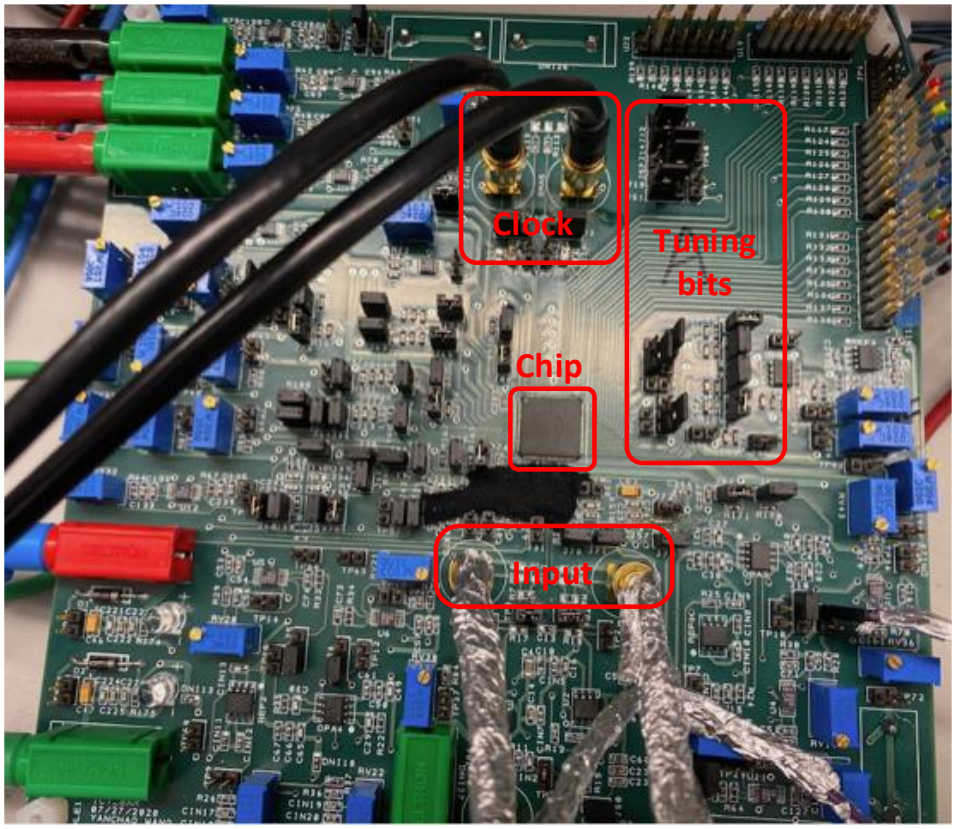


Figure 6.2: PCB design

6.2 Measurement results

6.2.1 Small signal test

When the input single amplitude is small, the dominate noise sources are the quantization noise and thermal noise. Figure 6.3 presents the PSDs of the ICT and the two step ADC with -80dBFS input signal at 990KHz. The two step ADC output noise floor moves down by around 23dB, and integration noise is also 23dB less which match the 4bits improvement of this architecture.

6.2.2 Dynamic range and PSD

When input signal is 990KHz, fs=64MHz, BW=1MHz, all the integrators are at the nominal values, the dynamic range (DR) plot is shown in Figure 6.4. The two step ADC achieves 90.5dB DR and the peak is at -4.5dBFS input. At SNDR peak, the FFT results of the first ICT and the two step ADC are given in Figure 6.5 and 6.6. The SNR/SFDR/SNDR are 74.1dB, 74.7dB, and 72.2dB for the ICT, and 82.4dB, 85dB, and 80.5dB for the two step ADC, respectively.

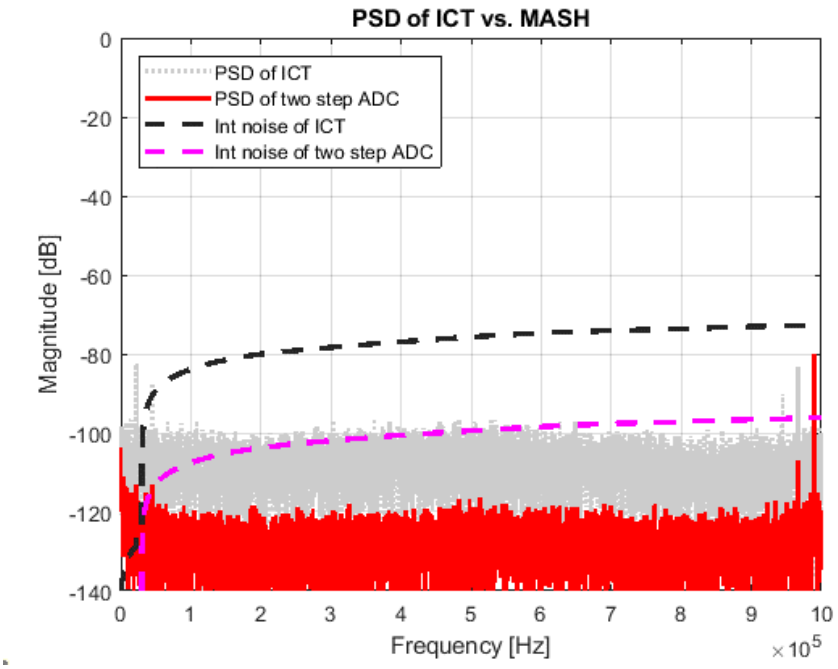


Figure 6.3: PSD and integration noise with -80dBFS and 990KHz input signal

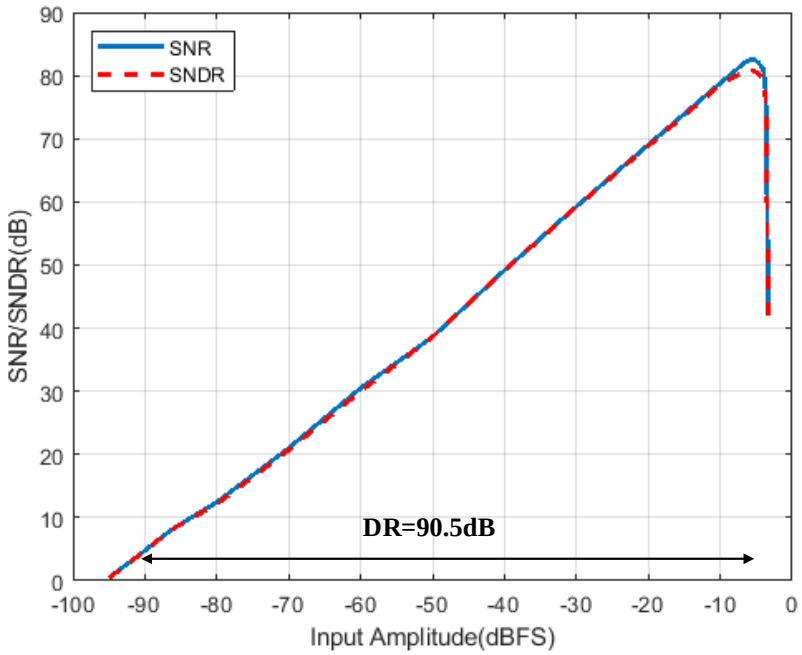


Figure 6.4: dynamic range plot of with 990KHz input signal input

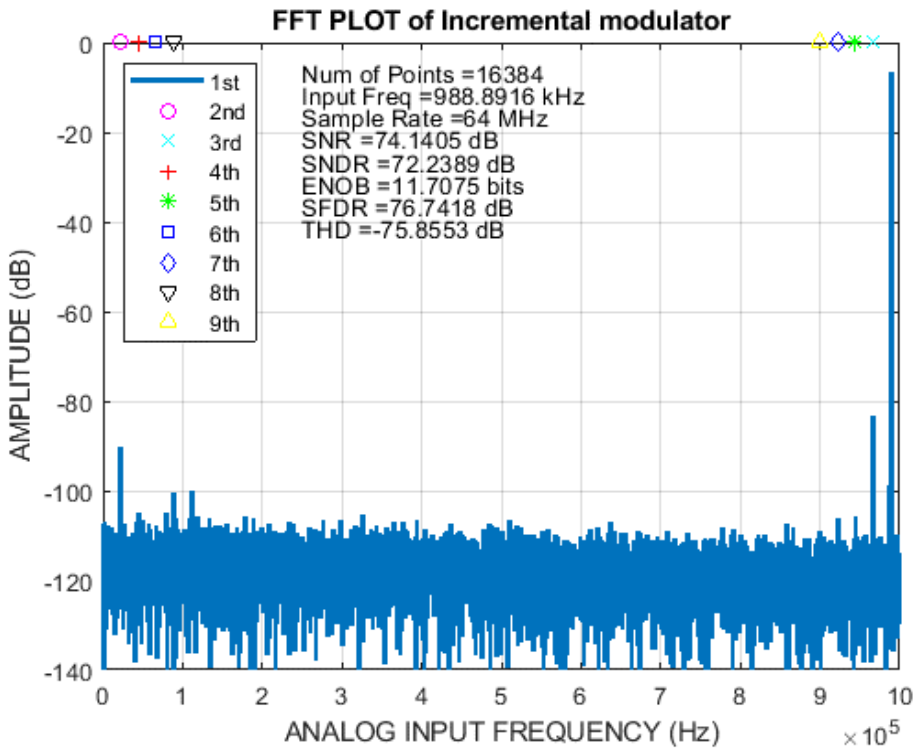


Figure 6.5: PSD of the ICT at -4dBFS 990KHz input signal

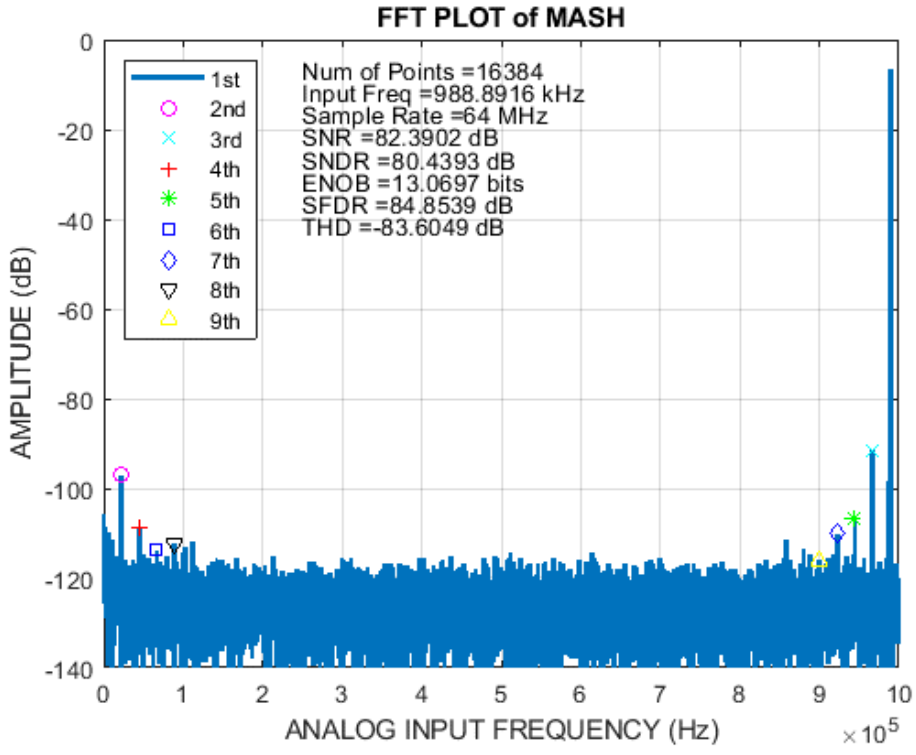


Figure 6.6: PSD of two step ADC at -4dBFS 990KHz input signal

When the input signal amplitude becomes larger, the non-linearity of the ADC may introduce distortions and increase the noise floor. The SNR versus input amplitude at large input signal is presented in Figure 6.7. The two step ADC achieves 8dB improvement in SNR comparing with the ICT ADC.

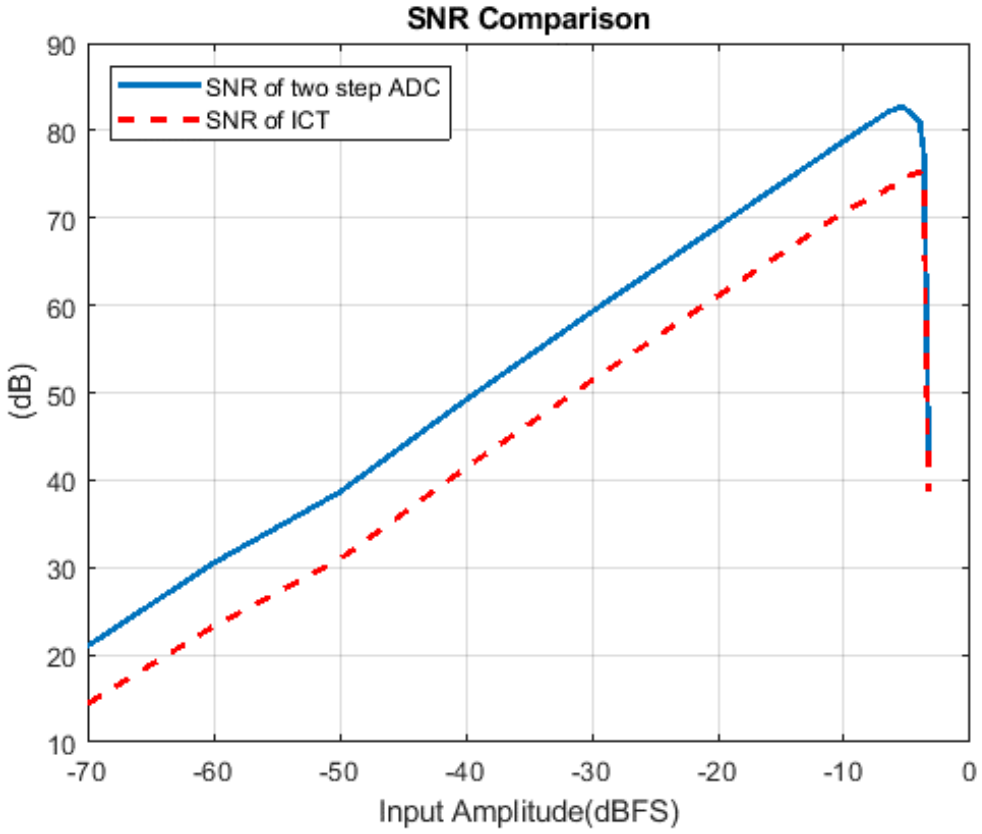


Figure 6.7: SNR comparison of ICT and two step ADC

6.2.3 Power consumption distribution

At 64MHz clock frequency, BW=1MHz, the ADC consumes 23.9mW from 1.8V power supply as illustrated in Figure 6.8.

6.2.4 Measurement Summary

Table 6.1 summarizes the measurement results discussed so far, it achieves the Schreier Figure-of-Merit (FoMs) in the range of 165.5dB at the highest input frequency among the state-of-the-arts ICT ADCs.

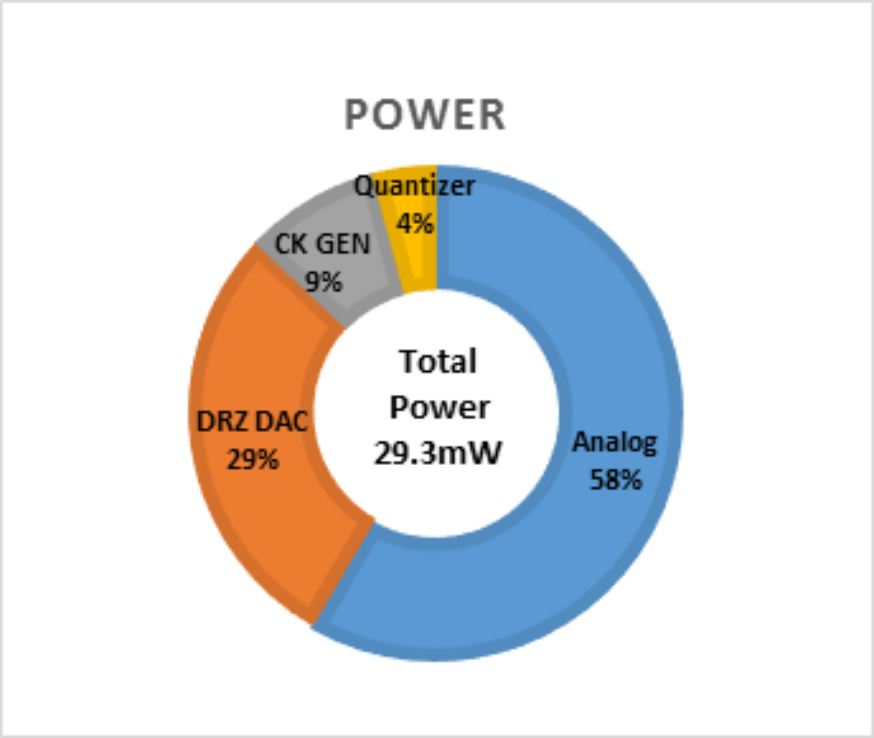


Figure 6.8: Power consumption and contribution of the major blocks at fs=64MHz

Table 6.1: Measurement summary and comparison to state-of-art ADCs

	This Work	[40]	[39]	[41]	[42]
Architecture	**ICT-SAR**	ICT	ICT	ICT	IDT
Technology [nm]	**180**	180	180	180	180
Area [mm^2]	**3.99**	0.175	0.35	0.337	0.363
Supply [V]	**1.8**	3	1.8	1.8/1.2	3
Power [mW]	**29.3**	1.27	0.055	0.0348	1.098
F_s [MHz]	**64**	32	3.048	0.32	30
F_{nyq} [Ks/s]	**2000**	200	12	8	200
SNDR [dB]	**80.5**	83	85.1	75.9	86.6
SFDR [dB]	**85**	94.3	97	88.1	101.3
DR [dB]	**90.5**	91.5	88**	85.5	91.5
$FoM_{s,DR}$* [dB] @ f_{in}	**165.5 @ 990KHz**	170.4 @ 11Khz	168.4 @ 6KHz	168.4 @175Hz	171.1 @13KHz

*$FoM_{s,DR} = DR + 10 \cdot log_{10}\left(\frac{BW}{Power}\right)$

** Estimated from given plots

Chapter 7 : Conclusions

In this work, firstly, a RMASH architecture is presented. The RMASH extracts the shaped quantization error at integrator output from the previous stage and transfer to the following stage. The mismatch between the digital filer and the analog blocks transfer function leads to shaped quantization noise leakage which is smaller than traditional MASH. Therefore, the digital filter can be simplified to save power and area. Besides, the overall SQNR is independent of the NTF of the delta sigma modulator, and the NTF optimization can be more flexible based on the DAC linearity and loop stabilities considerations. Simulations results from MATLAB proves the RMASH works for DT, CT and hybrid architecture implementations.

Secondly, a hybrid two step ADC with ICT and SAR ADCs is proposed. The ICT ADCs are realized by periodically reset the CT DSM, and they become nyquist rate ADCs having small input and output latency. In discrete time incremental (IDT) ADCs, the sampling switch non-linearity, charge injection degrade the resolution, and power hungry OPAMPs are demanded to provide fast and accurate settling for the switch-capacitor circuits. While the continuous time incremental (ICT) ADCs enable higher resolution, faster conversion speed with lower power consumption by removing the sampling switches and the CT integrators relax the OPAMPs settling accuracy requirements. Besides, the hybrid ICT-SAR two step ADC inherits the advantages of the RMASH architecture. It has smaller quantization noise leakage and the SQNR of the two step ADC is independent of NTF of the first ICT ADC, which gives more freedom to choose NTF targeting for better performances.

A design example of 16b, BW=1MHz, ICT-SAR two step ADC is implemented in AKM 180nm cmos process. At small input signal case, the two step operation reduces the ICT ADC noise floor by 23dB which verifies the effectiveness of the proposed architecture. The measured DR is 90.5dB at 990KHz input signal with FoMs=165.5dB. The ADC achieves SNR/SFDR/SNDR of 82.4dB/85dB/80.5dB respectively at the -4.5dBFS input amplitude. The measurement results indicate this architecture features high conversion speed and low noise.

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