AN ABSTRACT OF THE DISSERTATION OF

Jyotindra R. Shakya for the degree of Doctor of Philosophy in Electrical Engineering presented on November 5, 2021

Title: Plasmonic Color Filter array, high performance Analog to Digital Converter architectures and novel circuit techniques.

Abstract approved:

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Professor Alan X. Wang Professor Gabor C. Temes

Part I: Plasmonic color filters can be manufactured at lower cost since they can be fabricated in single lithographic process step as compared to Fabry-Perot based filters. In addition, they have narrow passband making resolving sharp features in sample spectrum possible. Due to these benefits, in this thesis, Plasmonic color filters are investigated as alternative to conventional color filters and their feasibility for spectroscopy demonstrated through reconstruction of 6 sample spectra by using a set of 20 color filters. The error in reconstructed sample spectra is less than 0.137 root mean squared error across all samples.

Part II: A novel 12-bit pipelined successive approximation analog to digital converter is investigated for high speed data conversion. The design was implemented in TSMC 65nm process to demonstrate the feasibility of the architecture. Furthermore, a high dynamic range audio delta sigma modulator using pseudo-pseudo differential topology was investigated and feasibility simulated using TSMC 65nm process. In addition, various novel systems and circuit techniques including efficient calibration of feedback digital to analog converters, new boosted switch and push-pull source follower circuits were investigated to improve upon existing circuit topologies.

Plasmonic Color Filter array, high performance Analog to Digital Converter architectures and novel circuit techniques

by
Jyotindra R. Shakya

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Head of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Jyotindra Shakya, Author

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1. Part I: Plasmonic Color Filter Array

1.1 Introduction and Motivation for Plasmonic Color Filters

The nature is abundant in rich spectral information, especially in visible range. There are many animals, who are able to take advantage of such spectral information using many color vision such bluebottle butterflies[1] and mantis shrimp[2]. However, humans are able to see only 3 colors and hence limits our capabilities to distinguish minor changes in spectra or detect sharp spectral features. Hence, when high spectral fidelity is needed hyperspectral cameras are often used. For example, hyperspectral cameras in medical applications for imaging cancerous tissue[3-5] and detecting level of bilirubin[6] in infants by taking picture of the skin etc. Furthermore, hyperspectral cameras can be used in remote sensing[7-9], mineralogy[10], food safety[11] and artwork authentication and preservation [12-15]. In the most advanced state-of-art hyperspectral cameras [16-18], Fabry-Perot based color filters are arranged in Bayer pattern such that at each pixel in the image plane, many color channels are detected. Figure 1 below illustrates the use of Fabry-Perot filters in state-of-art hyperspectral image sensor.

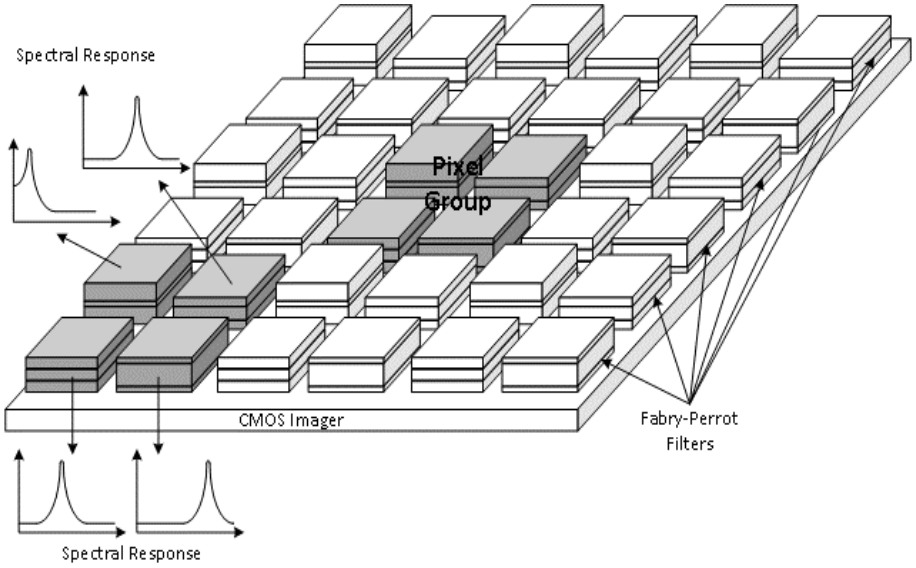

Figure 1 Illustrative Hyperspectral Imager based on FP filters (exaggerated for illustration). Each pixel with distinct spectral response requires different thickness of dielectric layers and hence the fabrication process requires number of process steps proportional to the number of color channels.

However, fabrication of such color filters is expensive due to many fabrication process steps needed to create as many different Fabry-Perot filters as number of color channels desired. In contrast, many different plasmonic color filters can be fabricated in a single lithographic process step as only the lateral dimensions determine the location of resonance peaks. As such plasmonic color filters can be a good alternative to Fabry-Perot filters often used in hyperspectral imagers and cameras. Figure 2 below

illustrates the use of Plasmonic color filters in conceptual image sensor. In this thesis, an end-to-end demonstration of use of plasmonic color filter array for detecting sample spectra is presented.

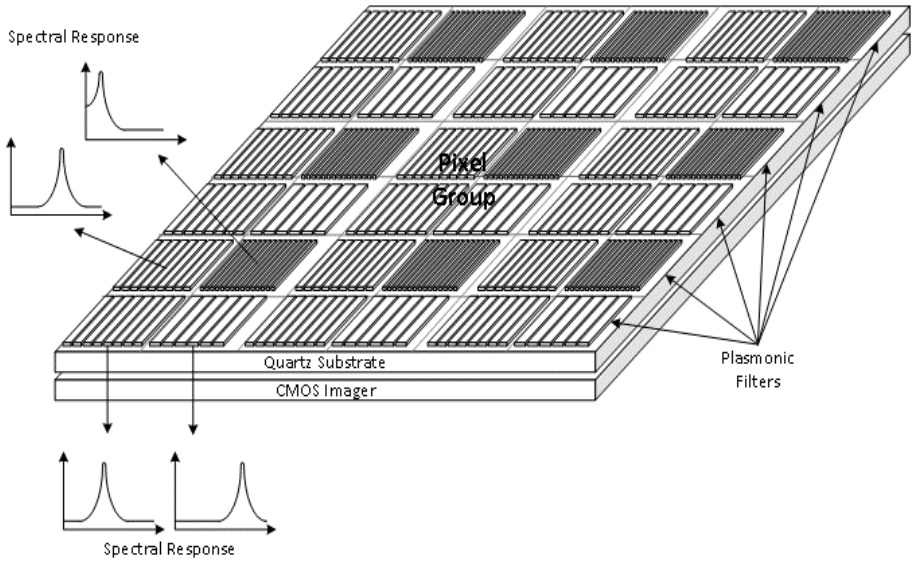

Figure 2 Illustrative Hyperspectral Imager based on Plasmonic color filters (exaggerated for illustration). Here only four spectral bands are illustrated, but the complexity of fabrication is independent of number of spectral bands.

1.2 Literature on plasmonic sub-wavelength grating filters

The theory of extraordinary optical transmission through sub-wavelength hole array was established nearly two decades ago [19]. When an array of periodic holes was made on metal coated on dielectric substrate, a set of transmission peaks through such structure were observed. The transmission efficiency at the peaks was orders of magnitude higher than that predicted by aperture theory (based on area of the holes) and hence such transmission was termed extraordinary optical transmission. The location of transmission peaks linearly depends on the period of the hole array or the grating and is independent of thickness or diameter of the holes. The width of peak depends on the aspect ratio (thickness/diameter) of the holes, wherein transmission width progressively decreases with increase in aspect ratio. Similar extraordinary optical transmissions have also been observed in 1-D structures such as grating [20]. There are at least two theories that has been proposed to explain such phenomenon [20]. The first one is strong coupling of surface plasmon polariton (SPP) modes on the air-metal interface with the metal-dielectric interface. The second is waveguiding of electromagnetic energy through the holes or slits. The first mechanism is more prevalent in thin grating structures, while the second mechanism is more prevalent in the thick grating structures. In both cases, more than ordinary amount of electromagnetic energy is transferred from one side to the other, hence lending to the phenomenon of extraordinary optical transmission. The detail analysis and phenomenology of extraordinary optical transmission is still an

ongoing research topic and many research papers have been published since the early observation [21-25].

Since early observation of extraordinary optical transmission, many research papers have been published in using such extraordinary optical transmission for spectral filtering [26-28]. It is well known in dielectric gratings that inclusion of waveguide structure under the grating improve the Q-factor of transmission peaks. These are called guided-mode resonance (GMR) filters [29]. Hence a similar idea was introduced for metallic grating [30-32] by placing a slab waveguide under or over the metallic grating. Although the transmission efficiency was improved the transmission width was wide due to losses in the SPP modes, except in infrared region [33] where the losses are low. The inclusion of slab waveguide directly underneath the lossy plasmonic grating causes slab waveguide to be lossy due to losses in the metal-dielectric interface and scattering at the holes or slits. This renders resonant coupling between grating and slab waveguide unable to replenish energy periodically since both have similar losses. A significant improvement was made by making the slab waveguide buried at a certain distance from the metal grating [34]. By including 55 nm buffer layer with lower refractive index between metal grating and slab waveguide, the transmission width was reduced from 70 nm to 30 nm. Since then, such structures have become very interesting as it allows designing color filters with high spectral selectivity.

Hence, in this thesis, design of such plasmonic color filters with buried slab waveguide is explored for the application in visible light spectroscopy. Although silver was used in [34] as plasmonic material, aluminum has been shown to have lower losses in shorter wavelengths [35]. Also, aluminum is compatible with complementary metal oxide semiconductor (CMOS) process and can lead to homogenous integration of plasmonic color filter directly on top of CMOS imagers. Hence aluminum was chosen as the metal for the sub-wavelength grating studied in this thesis. Figure 1 below shows a section of such plasmonic color filter with annotations.

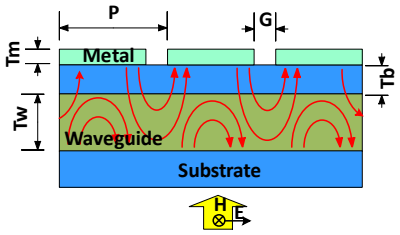

Figure 3 Schematic of a section of plasmonic color filter with annotated critical parameters and E-fields. P is period of the grating, G is gap of the slits, Tm is thickness of grating, Tw is thickness of slab waveguide and Tb is separation between metallic grating and slab waveguide.

There are several design parameters of the structure that determine the transmission spectra of such filter such as the period (P), the gap (G), the thickness of the metal (Tm), thickness of slab waveguide (Tw) and distance of the slab waveguide from the metallic grating (Tb). The period determines the location of transmission peak, the thickness of the metal together this the slit width determine the aspect

ratio and affects the transmission width, the thickness of the waveguide and its distance from the grating determine the quality factor (Q-factor) of the transmission peak. Although location of transmission peak can be calculated, the exact transmission spectra of each filter depend on many factors including loss in SPP modes, and evanescent coupling between SPP modes and waveguide modes and hence such structure can only be simulated in advanced electromagnetic simulators such Rigorous Coupled Wave Analysis (RCWA).

1.3 Surface Plasmon Polariton and coupling methods

The surface plasmon polaritons are surface wave propagating strictly at the metal-dielectric interface due to special properties of certain metals. The traveling SPP modes propagate at the surface via surface charge density fluctuations subject to excitation. Such SPP modes are strictly confined at the surface and do not leak into the bulk of the metal or the dielectric. Figure 4 below shows the SPP mode traveling at metal-dielectric interface.

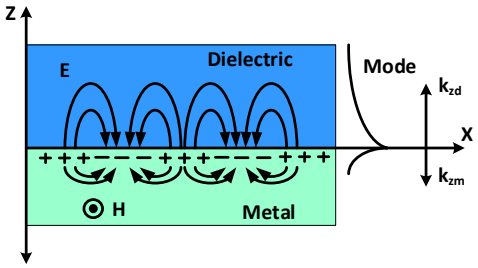

Figure 4 Illustration of SPP mode traveling at the metal dielectric interface and corresponding E and H fields

For such waves to exist, and to satisfy boundary conditions at the interface, following conditions must be met.

$$\frac{k_{zm}}{\varepsilon_m} = \frac{k_{zd}}{\varepsilon_d} \tag{1}$$

Here k_{zm} and k_{zd} are wave vectors in metal and dielectric in z-direction. As such these wave vectors are opposite in polarity for evanescent waves decaying away from the interface. Hence the above condition implies such wave can only exist if metal dielectric constant is negative. Furthermore, for any traveling electromagnetic wave, based on Maxwell's equations, following relation must be valid.

$$k^2 = k_x^2 + k_{zi}^2 = \varepsilon_i \left(\frac{\omega}{c}\right)^2 \tag{2}$$

Now the wave vector of SPP mode and hence k_x can be written as:

$$k_{spp} = k_x = \sqrt{\varepsilon_d \left(\frac{\omega}{c}\right)^2 - k_{zd}^2} = \sqrt{\varepsilon_m \left(\frac{\omega}{c}\right)^2 - k_{zm}^2} \tag{3}$$

Finally, eliminating k_{zd} and k_{zm} from equation (3) using relation (1), we find that wave vector of the SPP mode must be:

$$k_{spp} = k_x = \frac{\omega}{c}\sqrt{\frac{\varepsilon_m \varepsilon_d}{\varepsilon_m + \varepsilon_d}} \qquad (4)$$

Here, ε_m is dielectric function, which is function of wavelength. For certain wavelengths, it is negative quantity whose absolute value is close to ε_d . Under such conditions, when we plot the ω-k relation, we find that such mode lies below the light line. Therefore, such mode cannot be excited by directly coupling light at the interface. Due to this, often two coupling schemes are used, viz. Prism coupling or grating coupling. In the plasmonic color filters, the subwavelength gratings act as the coupling mechanism to couple incident light into SPP modes.

1.4 Principle of operation of plasmonic filter with slab waveguide

Although to support SPP modes using grating coupling, the metal-dielectric interface only needs to be corrugated, in plasmonic grating filters, the metal is fully etched to form slits. This causes SPP modes to be reflected at the terminations and many such reflections at fixed distance forms Bragg reflection in both directions. As such the SPP mode becomes superposition of two traveling waves in opposite direction, forming a standing wave as shown in Figure 5 below.

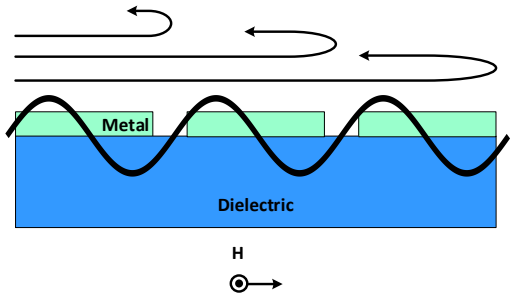

Figure 5 Plasmonic grating structure and formation of standing SPP modes

Such grating can itself act as color filters as they exhibit extraordinary optical transmission at certain wavelengths determined by the periodicity of the grating. However due to losses in the metal, such transmission peaks have broad spectra. The quality factor (Q-factor) of the transmission peaks can be improved by introducing buried slab waveguide. Similar to SPP modes, the slab waveguide cannot be excited by incident waves directly. The superposition of incident wave and SPP wave, however, can guide waves inside the slab waveguide. The effect of such superposition is shown illustrated in Figure 6 below. Therefore, the guided mode in slab waveguide exchanges energy from SPP mode through evanescent wave coupling and vice versa. Such coupling between two resonant modes allows for periodically replenishing energy into the SPP mode from a high Q-factor (low loss) guided mode. As in the case of plasmonic grating without slab waveguide, some energy from SPP modes leak due to

scattering at the terminations and hence leading to far-field transmission. Hence the plasmonic grating structure with slab waveguide can exhibit narrower transmission peaks.

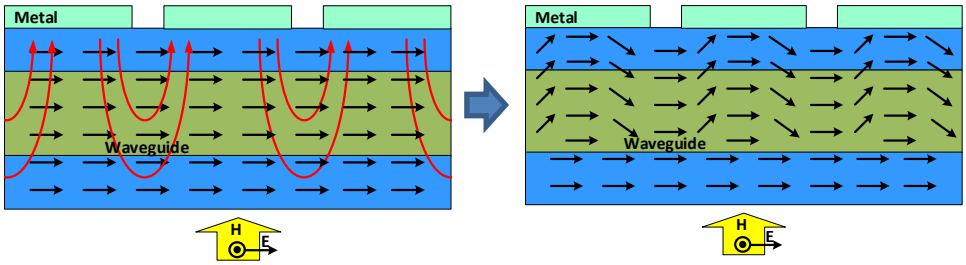

Figure 6 Superposition of incident wave and SPP mode results in guided mode. Since SPP mode is also excited by incident wave, it is coherent with the incident wave.

Due to complex wavelength dependent dielectric constant of the plasmonic material, the strong coupling between SPP mode and guided mode, the design of such structure requires electro-magnetic (EM) field solvers or Rigorous Coupled Wave Analysis (RCWA) solvers.

1.5 Design and simulation of plasmonic filter with slab waveguide

The design of plasmonic color filters were done in Rsoft DiffractMod simulator, which uses RCWA technique for simulating complex geometries. Several design parameters as shown in Figure 3 can be studied for its effect in spectral features. The period of grating has the most direct effect in location of peak in transmission spectra as shown in Figure 7 below.

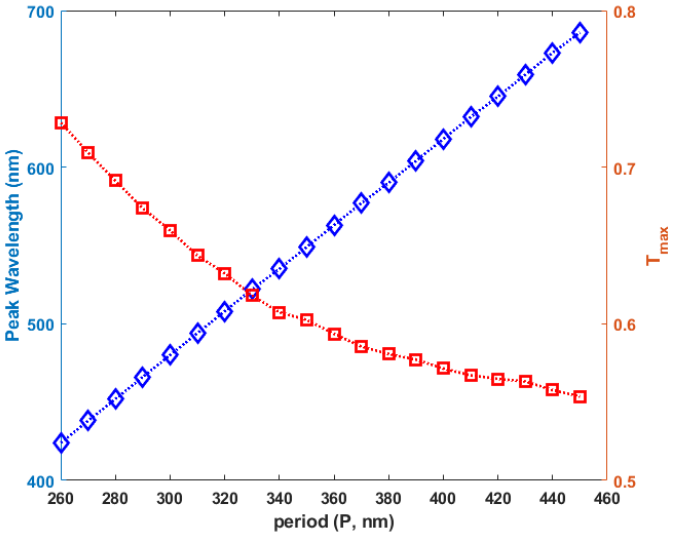

Figure 7 Peak wavelength and maximum transmission (T_{max}) as a function of Period

The location of the transmission peaks is roughly given by the effective wavelength in the substrate medium, which in this case is Silicon Dioxide. Hence for 450 nm period, the peak lies roughly around 675 nm. In addition to the main peak, there are two significant features of the transmission spectra are

of interest. The first one is one or more shallow, broad peaks at short wavelengths. These peaks are due to Rayleigh Anomaly. Second feature is the gradual increase in transmission at longer wavelengths. Such secondary peaks and long tails cause mixing of various parts of the spectrum and degrades spectral selectivity of a filter. However, such mixing can be undone to some extent using unmixing algorithm as long as the filter array characteristics are known accurately.

Similarly, the aspect ratio (Tm/G) has direct effect on the width of the transmission peak as shown in figure below.

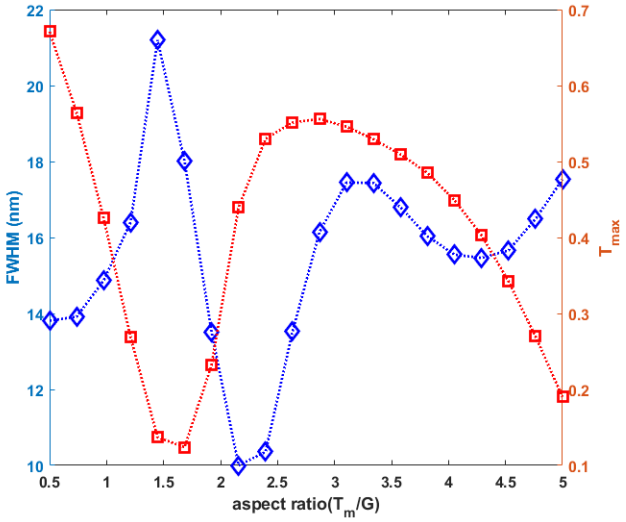

Figure 8 FWHM and peak transmission as a function of aspect ratio (T_m/G) for G = 60 nm

Similarly, the distance to the waveguide has direct effect on the width of the transmission peak as shown in figure below.

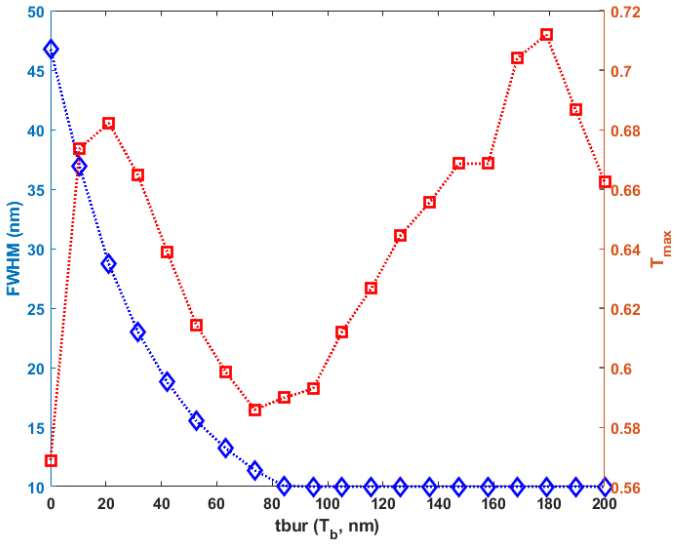

Figure 9 FWHM and peak transmission as a function of T_b

As the waveguide is placed close to the grating, the effect of guided mode replenishing the SPP mode is degraded as waveguide also becomes lossy due to presence of metal at the boundary. As the waveguide is placed further away, guided mode is less lossy and hence coupled resonance between the SPP mode and guided mode is able to enhance the Q-factor of the SPP resonance.

Based on target full width at half maximum (FWHM) of 10-20 nm, the design was optimized for maximum transmission and uniform transmission peaks across visible wavelengths. Using iterative simulations, the final design choice was made based on following parameters as shown in Figure 10 below.

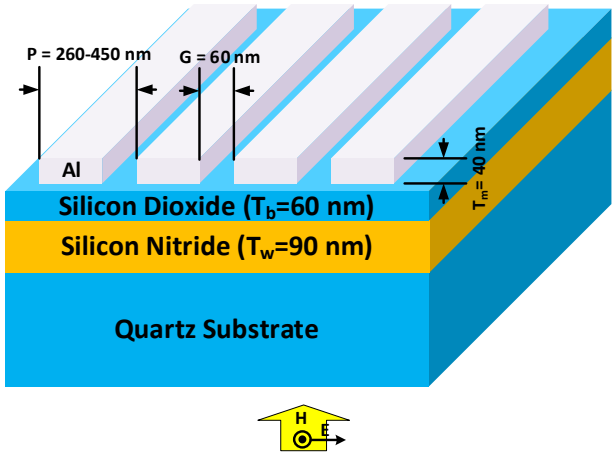

Figure 10 Final optimized design schematic with annotated design parameters

To further verify the understanding of the interactions between the SPP mode and guided mode, a set of field simulations were performed. Figure 11 below shows the E_x and E_z component of electric field in a unit cell at the transmission peak of one of the filters.

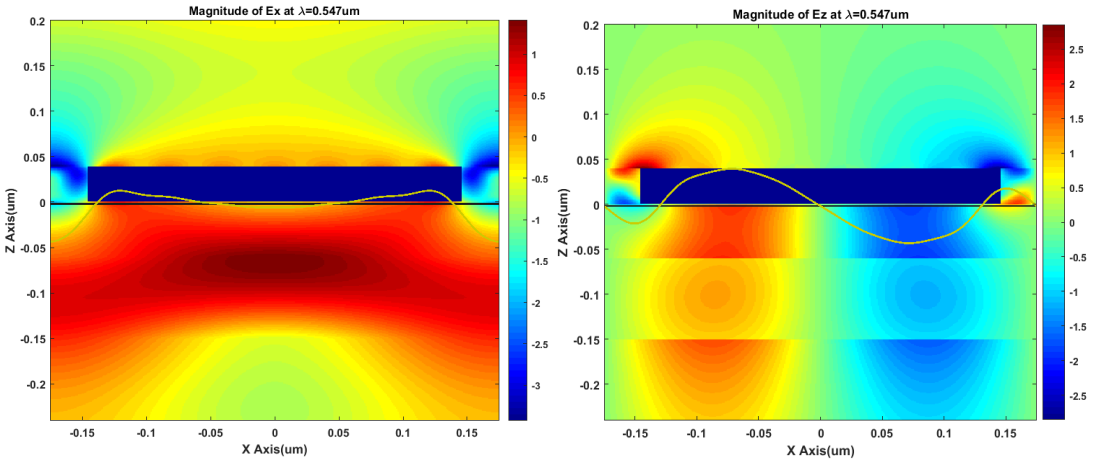

Figure 11 E_x and E_z component of electric field in a unit cell at peak transmission. Line plots show illustrative field profile at the metal-dielectric interface, where SPP mode exists.

It is noted here that E_x field is mostly featureless and represents the incident plane wave and serves only as means to excite SPP mode in the grating. However, E_z component of electric field clearly shows the standing SPP mode at the interface, which evanescently couples into the slab waveguide. The interpretation of the fields can be further clarified using magnetic field (H_y) and total electric field in the form of quiver plot as shown in figure 12 below and annotating the poynting vectors.

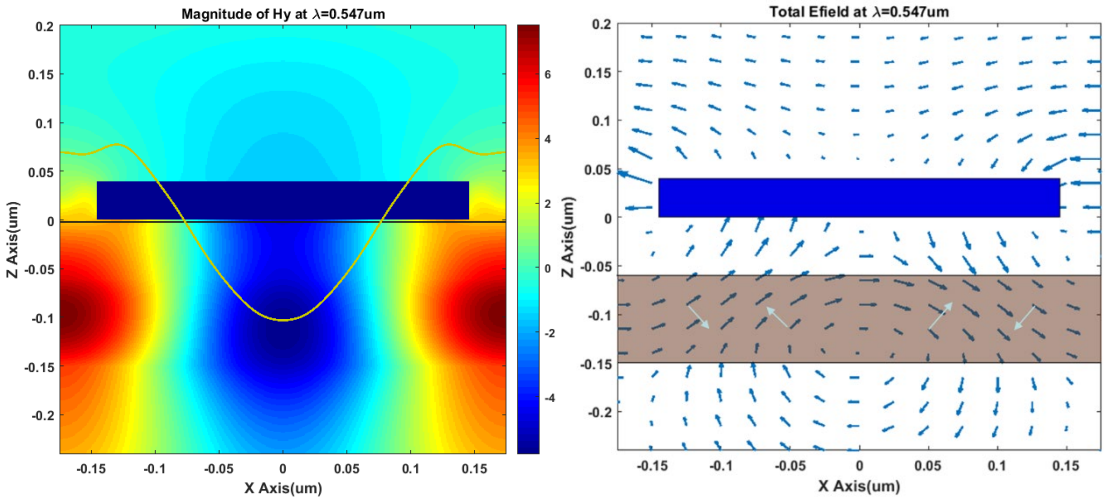

Figure 12 H_y component of magnetic field and total electric field showing magnitude and direction. Line plot in Hy field shows the field profile at the interface. The annotated white arrows show the direction of poynting vector at various points in the waveguide.

Based on total electrical field plot derived by E_x and E_z components from Figure 11, and magnetic field plot, we can deduce the direction of poynting vector at various points inside the waveguide. It is shown in Figure 12 that energy flow has forward and backward direction, indicating presence of standing wave with no net energy flow in x-direction. Hence the slab waveguide also has standing wave due to strong evanescent coupling from the SPP mode. This allows for strong coupling and exchange of energy between two modes. Furthermore, since waveguide is placed away from the grating, making it less lossy than the SPP mode, which allows for replenishing energy into the SPP mode by the guided mode.

1.6 Design and simulation of plasmonic color filter array

Furthermore, based on the characteristics and understanding of the operation, two set of 20 color filters were designed for demonstrating spectroscopy in visible range. The first set of filters (25 µm x 25 µm in 5 x 4 mosaic) contained 20 colors filters at a pitch of 50 µm [36]. The design parameters were as given in Figure 10, except the thickness of the metal was 30 nm. A second set of filter array was designed with parameters as given in Figure 10 with thickness of the metal equal to 40 nm [37]. In this array the filters were separated by 50 µm spacing to reduce amount of cross-talk between the filters during measurement. Due to presence of continuous slab waveguide across the mosaic, at wavelengths where the transmission in a particular filter is low, the rejected energy can flow through the slab waveguide and

into adjacent filters. Such cross-talk can only be measured if all the filters are illuminated, and response of each filter is characterized. Although separation is better in second set of filters, as can be seen in figure 13 below, the transmission peak of 30 nm filter array is slightly higher than that in 40nm filter.

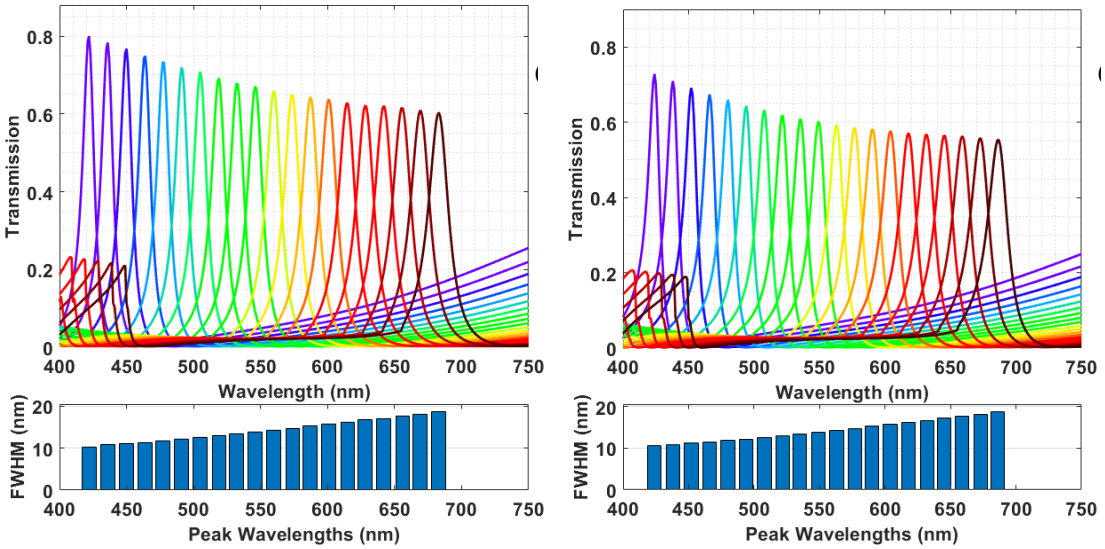

Figure 13 (a) Simulated spectra of first set of filter array with 30 nm thick metal layer (b) Simulated spectra of second set of filter array with 40 nm thick metal layer. Color of each spectra represents the human visual perception of color at each peak wavelengths.

1.7 Fabrication of plasmonic color filter array

The designs were fabricated on 500 µm thick Quartz substrate on which 90 nm of Silicon Nitride was deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) followed by 60 nm of Silicon Dioxide using same PECVD tool. Then 30 nm of Aluminum was deposited using evaporation for the first array and 40 nm of Aluminum was deposited for the second array. The filter array was then patterned using Focused Ion Beam (FIB) milling using Gallium ions with 30 keV energy. The writing was performed at 30 pA write current and with scan speed such that dose is 35 mC/cm^2. Figure 14 below shows the scanning electron microscope (SEM) image of a section of one of the filters.

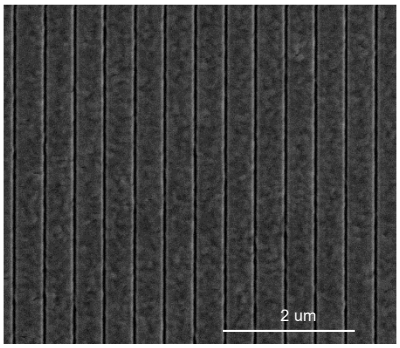

Figure 14 SEM image of a section of one of the filters

1.8 Testing of plasmonic color filter array

The first filter array was characterized using following test setup by replacing sample with a monochromator. Then monochromator was removed, and various samples were placed. The sample images were then used as signals for spectral unmixing and reconstruction.

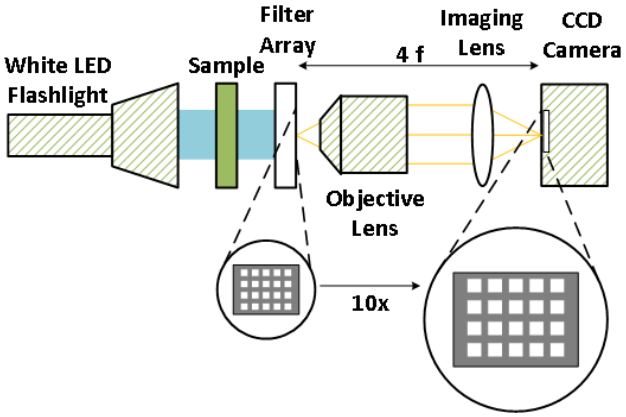

Figure 15 Test setup for characterization of first set of filter array and measuring sample spectra by taking snapshot images.

The filter array was characterized by scanning the monochromator and taking picture on the camera using the same setup to avoid additional errors. A flashlight with white light emitting diode (LED) was used as illumination. The camera was algorithmically set to adjust exposure time such that analog to digital converter (ADC) values were at the middle of the dynamic range. The images were processed through an image processing algorithm for segmentation and background subtraction. The same process was repeated for samples. Figure 16 below shows the measured filter array spectra and RGB image of the filter array taken in a microscope with polarized light bright-field illumination.

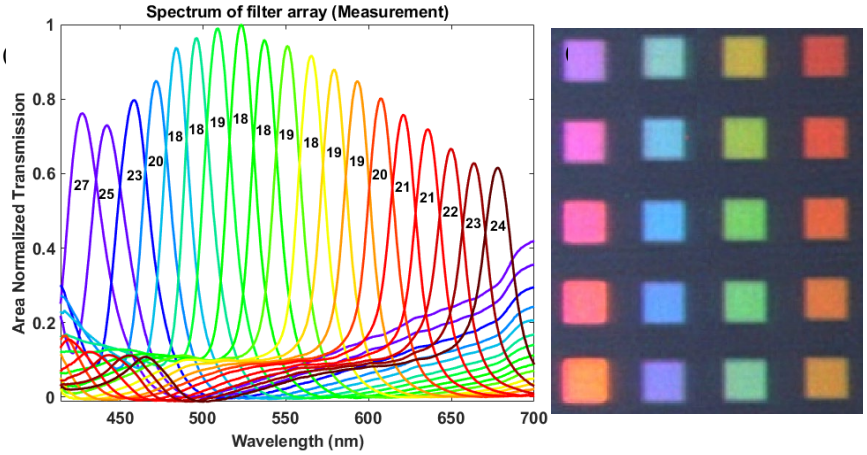

Figure 16 (a) Measured spectra of filter array with FWHM annotated in each spectrum. (b) RGB image of the filter array taken under microscope with polarized bright-field illumination.

The second filter array was characterized using spectrometer instead of using monochromator as in previous filter array. The use of monochromator introduced an unknown error in absolute transmission due to its wavelength dependent diffraction efficiency across wide visible range. In addition, the monochromator slit needed to be large in order to detect signal at the camera due to low sensitivity of the camera. To avoid these issues, a spectrometer was used for characterizing the second filter array. Figure 17 below shows the test setup used for characterizing second filter array.

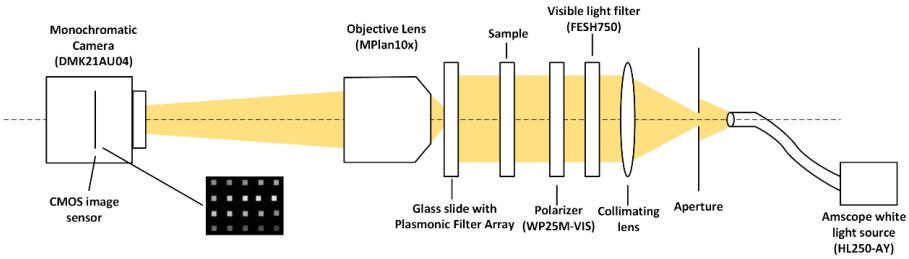

Figure 17 Test setup used for characterizing second filter array and measuring samples using second filter array.

In this case, a 150W halogen white light source was used as illumination. This allowed for higher signal at the camera as well as spectrometer. The white light source was passed through aperture to generate point source. This was required as the filter array is sensitive to incident angles and hence needed to be illuminated by collimated light. Then light from aperture was collimated, passed through visible light filter, a polarizer and color filter array. The sample was removed during filter characterization. After passing through color filter array, the light collected using 10x objective lens and was imaged directly onto the fiber tip of USB2000+ spectrometer. For taking sample images a monochromatic camera was placed at the image plane as shown in Figure 17 above. Figure 18 below shows the measured filter array spectra and RGB image of the filter array taken with a microscope.

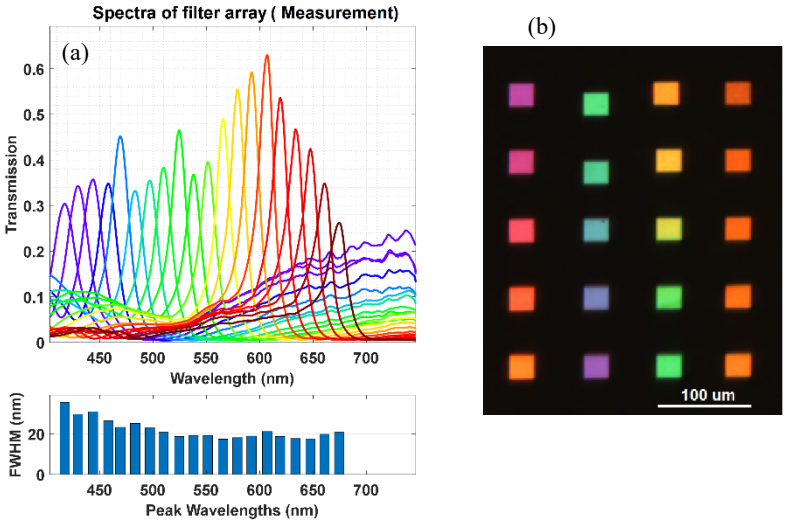

Figure 18 (a) Measured spectra of filter array with FWHM (b) RGB image of the filter array taken under microscope with polarized bright-field illumination.

Since the filter array was characterized by directly coupling the filter images onto the tip of a fiber connected to the spectrometer, there was additional error to changes in coupling efficiency. Hence peak filter transmission is non-uniform. Also filters with peak at shorter wavelengths are broader than simulation due to losses in the deposited aluminum. The evaporative deposition of aluminum is grainy and hence losses will be higher compared to solid aluminum as used in simulation. However, when we look at the general trend of the total area under each curve, they match with simulation.

1.9 Sample measurement and spectral reconstruction

The samples (6 colored glass filter from Newportglass [38]) were measured by passing white light through the samples and the Plasmonic Filter Array and capturing snapshot images of the Filter Array using an objective lens. The Amscope HL250-AY was used as white light source. The gooseneck of the lamp was held on a mounting fixture and the light was used to illuminate a variable aperture. The light from the aperture was then collected using an aspherical achromatic collimating lens (APAC15) with effective focal length of 30 mm from Newport Optics. The light was then passed through visible light filter (FESH750) with cutoff at 750 nm. Then a wire grid polarizer (WP25M-VIS) was used to polarize the illumination. Then the samples were placed in the light path with a mounting fixture. Then the glass slide with plasmonic filter array was mounted on X-Y stage and placed in the optical axis. Then a MPlan 10x objective was used to image the filter array from the other side onto DMK21AU04 monochromatic camera. The background illumination was reduced by conducting the experiment in a dark room and by properly shielding stay light. The camera was connected to a computer in which automatic exposure time adjustment algorithm was run to keep the signals in images around 50% of the camera's dynamic range. The detected signals were then extracted by postprocessing the sample images for background subtraction and image segmentation.

The use of the color filter array to detect energy in each spectral band and reconstruction of original spectra poses several challenges. Firstly, the spectrum of each filter has prolonged tail at the longer wavelengths and Rayleigh anomaly peaks at the short wavelengths, which causes spectral mixing. For example, in Figure 18(a) the first filter can transmit light in the range of 425nm to 450nm as well as that beyond 600nm. Hence any reading on this color channel could be due either of these spectral bands. Due to such mixing, as can be seen in Figure 19, the detected signal is quite different from the original sample spectra. Hence an unmixing algorithm was developed to band-wise unmix detected signals. Secondly, the reconstruction of original spectra (at 1 nm steps) from under-sampled data (only 20 filters in entire visible range) can be framed in the linear algebraic terms as solving under-determined least square problem, which has infinite many solutions. Hence a unique regularization method using second order difference operator was used for reconstructing smooth spectra from unmixed signals. The details of the algorithms used will be described in following section. Figure 19 below shows the spectra of 6 different samples with as detected signals, unmixed signals, and reconstructed spectra. Each spectra also contains the original snapshot image of the sample take by a monochromatic camera.

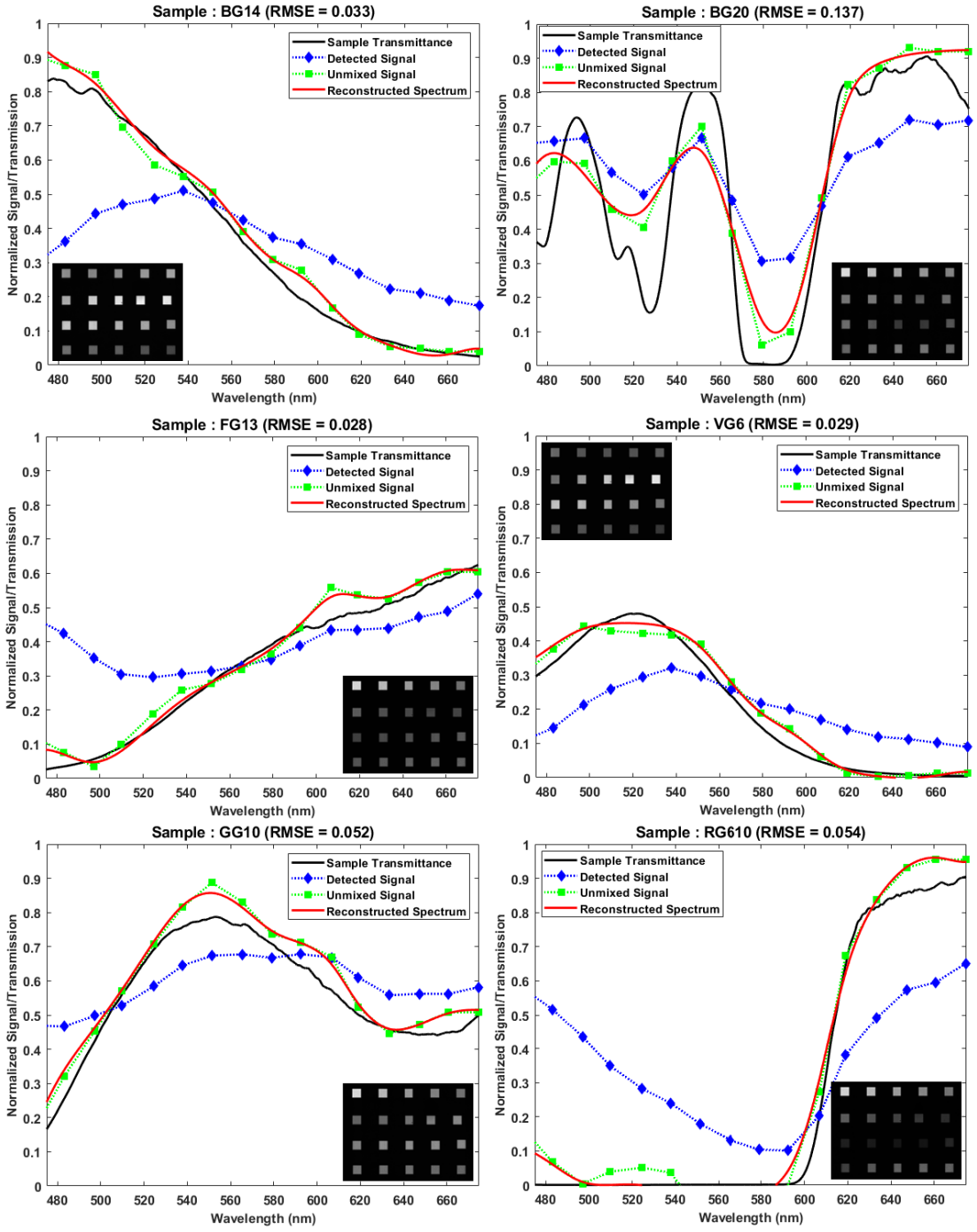

Figure 19 Results of spectral reconstruction of 6 samples using snapshot images (shown in insets) through the color filter array. Black curves show sample transmission (ground truth), blue curves show the signal extracted from images, green curves show the signals after unmixing algorithm and red curves show the reconstructed spectra.

As can be seen in Figure 19 above, the detected signal is quite different from original sample spectra and unmixing algorithm is able to correct for spectral mixing such that unmixed signal is very similar to the sample spectra. The maximum root mean squared error (RMSE) across all the samples tested is less

than 0.137 with worst case in sample BG20, which has many sharp features. The sample BG20 was included in the sample set to test the limits of the system and the reconstruction algorithm. For the rest of the samples without such sharp features, the RMSE is less than 0.054.

Although sample spectra could be recovered there are several sources of error that limits the performance, some of which are:

1. There is inherent assumption in proposed algorithm that spectrum is constant within each band. This introduces some error.
2. Some of the spectra, especially sample two BG20, contains very sharp features which has frequency components higher than that Nyquist frequency and hence some of the information is aliased, which degrades reconstruction accuracy in this filter.
3. The reconstruction is based on filter characterization and measurement errors in filter characterization can result in reconstruction error. The filters were characterized by coupling imaged filter patterns onto an optical probe of the spectrometer and hence variations in coupling efficiency could results in errors in filter characterization, which leads errors in reconstruction.
4. Lastly, there is inherent cross-talk between filters due to proximity and due to presence of contiguous slab waveguide. The slab waveguide provides means for some of the rejected energy from one filter to appear in the other filters. However, this effect is partly captured during filter characterization and as long as filters are characterized in-situ including such cross-talk, it doesn't affect the reconstruction. However due to cross-talk, the characterized filter array spectra are expected to be different from simulation.

1.10 Unmixing algorithm

For unmixing algorithm, we consider the signal acquisition in two steps. Firstly, the illumination passes through an idealized set of filters (without much overlaps) and then secondly these signals are mixed at various proportions to produce detected signals. Such operation can be represented by:

$$\mathrm{D_N} = \mathrm{M_{N\times N}} \times \mathrm{G_{N\times}}_n \times (S_n \bullet I_n) \qquad (5)$$

Here $\mathrm{S_n}$is sample transmittance, I_n is illumination, $\mathrm{G_{N\times}}_n$ is idealized filter transmission matrix, $M_{N\times N}$ is the mixing matrix and D_N is the detected signal. Here × signifies matrix multiplication and • signifies element-wise product. The mixing matrix $M_{M\times N}$ is then computed using following algorithm.

Algorithm 1. Algorithm for computing mixing matrix

Input: F (N×n matrix : actual filter transmission)
Initialize: W= 1 (N×n matrix : Hadamard identity matrix)
for i $= 1 \rightarrow$ n do
  for $j = 1 \rightarrow$ n do
    if $j \neq$ i then
      $W_i = W_i \bullet (F_i > F_j)$
    end if
  end for
end for
$M = W \times F^T$

Then M is a N×N matrix representing mixing proportions from each filter to every other filter. This is an invertible square matrix. This assumes that spectrum is constant across each band, which for a set of narrow filters is a good approximation. Also, this implies the product $M^{-1} \times F$ results in idealized filter transmission matrix. Now unmixing can be performed using following operation.

$$D_U = M^S_{N\times N} \times D_N \tag{6}$$

Where D_U is unmixed detected signals per color channel and s operation is smoothing regularized pseudo-inverse. A regularized pseudo-inverse is used instead of matrix inversion to find a smooth low frequency signal and to discard oscillatory and unrealistic solutions.

1.11 Pseudo-inverse with smoothing regularization

Solving underdetermined least square error problem requires inverting rectangular design matrix and hence proper matrix inverse is not possible. There are infinite many solutions which satisfy the minimum least squares error criteria. Hence often pseudo-inverse is used, which allows us to choose the minimum norm solution among many possibilities [39]. A pseudo-inverse of a rectangular (n × N) matrix A is a (N × n) matrix A^+, which satisfies these four criteria, often called Penrose conditions.

$$\left.\begin{array}{ll} i) & AA^+A = A \\ ii) & A^+AA^+ = A^+ \\ iii) & (AA^+)^T = AA^+ \\ iv) & (A^+A)^T = A^+A \end{array}\right\} \tag{7}$$

Such matrix can be explicitly computed as:

$$A^+ = (A^TA)^{-1}A^T \tag{8}$$

Note here that $AA^+ \neq I$ and hence A^+ is not really a multiplicative inverse of A. However, it is well known that such pseudo inverse provides least square solution when the system is overdetermined and minimum norm solution when the system is underdetermined. Given a least square problem Ax = b, the pseudoinverse of A and hence solution $z = A^+b$ is the minimum norm solution. However, when applied to the case of time dependent signal or in this case wavelength dependent spectral reconstruction, we often desire to seek for smooth (low frequency) solution, which is not the same as minimum norm solution. For example, L2-norm of vector [1 0 1 0] is same as vector [1 1 0 0]. Hence, smoothing regularization is required. The smoothing regularization can be applied by including Tikhonov regularization matrix in computation of solution to least square problem. Then the smooth pseudoinverse can be computed as:

$$A^S = \left(A^TA + \Gamma^T\Gamma\right)^{-1}A^T \tag{9}$$

Where Γ is first order difference operator and hence $\Gamma^T\Gamma$ is second order difference operator. It is well established[40] that such smooth pseudoinverse minimizes $\|Az - b\|_2^2 + \|\Gamma z\|_2^2$. As such the solution found using such regularization minimizes the residuals as well as first order derivative.

1.12 Spectral reconstruction using smoothing regularization

Now after the signals are unmixed, the reconstruction can be performed by solving least square problem using smoothing regularized pseudo-inverse. Firstly $G_{N\times n}$ is computed as factor of the characterized filter transmission matrix $F_{N\times n}$ using following equation.

$$G_{N\times n} = M^{S}_{N\times N} \times F_{N\times n} \tag{10}$$

Now such idealized filter spectra can be used to reconstruct spectra from the unmixed signals as below.

$$R_n = \frac{G^{S}_{N\times n}\times D_U}{R_{n1}} \tag{11}$$

Here again the inverse is regularized pseudo-inverse and $R_{n1}(= G_{N\times n} \times D_{U1})$ is the first reconstructed spectrum without any samples. The regularized pseudo-inverse of a matrix A is computed using following equation:

$$A^S = \left(A^T A + k\Gamma^T \Gamma\right)^{-1} A^T \tag{12}$$

Where k is the regularization parameter and $\Gamma^T\Gamma$ is second order difference operator given by:

$$\Gamma^T\Gamma = \begin{bmatrix} 1 & -2 & 1 & \cdots & 0 & 0 & 0 \\ & \vdots & & \ddots & & \vdots & \\ 0 & 0 & 0 & \cdots & 1 & -2 & 1 \end{bmatrix} \tag{13}$$

The regularization parameter k determines the strength of smoothing by penalizing highly oscillatory solutions. Choosing a k value equal to zero leads to the case of non-regularized pseudo-inverse or least square error minimum norm solution, while choosing higher k value leads to smoother solution. The value of k was optimized with many iterations to seek for optimum solution. In inversion operation in equation (6), the k value was 100 and that in equation (11) it was 1.

1.13 Suppressing Rayleigh Anomaly

As seen in Figure 13 (a) and (b), when the filter array spans wide spectral range, the Rayleigh Anomaly peak at short wavelength starts to occur within the spectral range. This causes undesired mixing of colors and hence degrades spectral selectivity of the filters in the array. To remedy such effects and hence to extent spectral range without sacrificing spectral selectivity, a Metal-Insulator-Metal (MIM) structure can be used. The proposed MIM structure includes and additional metal layer on top of the primary grating separated by a layer of dielectric. The width of the second metal is made nearly half of the period. For example, in the last filter shown in Figure 13 (a) and (b), the period was 450 nm and that's where the Rayleigh Anomaly peak appears. This is due to the SPP resonance at the top interface (metal-air), where the effective length is simply the period. By adding another metal layer with half the width, the SPP mode is partly copied on the second metal layer, with 180° phase shift. For example, at locations where bottom SPP mode has positive charge, there will be negative charge on the top metal layer and so forth the oscillations have 180° phase shift. Furthermore, the scattering at the ends of metal layer is not hindered by the top level layer. Therefore, the whole structure acts as if there are two gratings

resonating at 180° phase shift, which results in cancellation of transmission at far field. The proposed structure has been thoroughly investigated and results published [41]. The proposed structure is shown in Figure 20 below, with design parameters annotated.

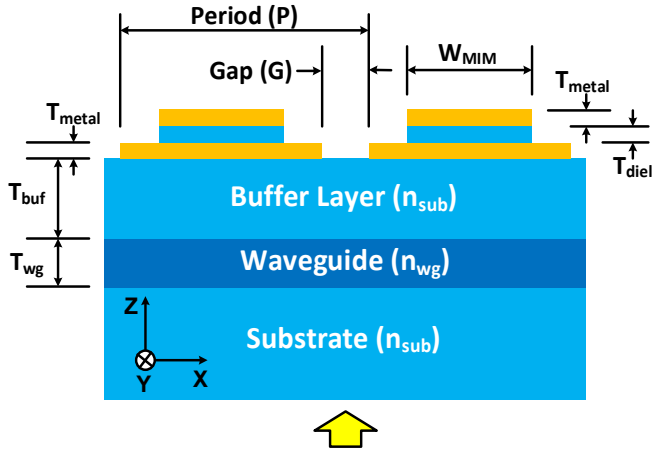

Figure 20 Cross section of the proposed plasmonic filter with MIM structure (not to scale). Period (P) = 425 nm, Gap (G) = 60 nm, W_{MIM} = 0.5×P, T_{wg} = 100nm, T_{buf} = 50nm, T_{metal} = 20nm, T_{diel} = 20nm, n_{wg} = 2.0, n_{sub} = 1.46.

Figure 21 below shows the E-field with and without the MIM structure at Rayleigh Anomaly point.

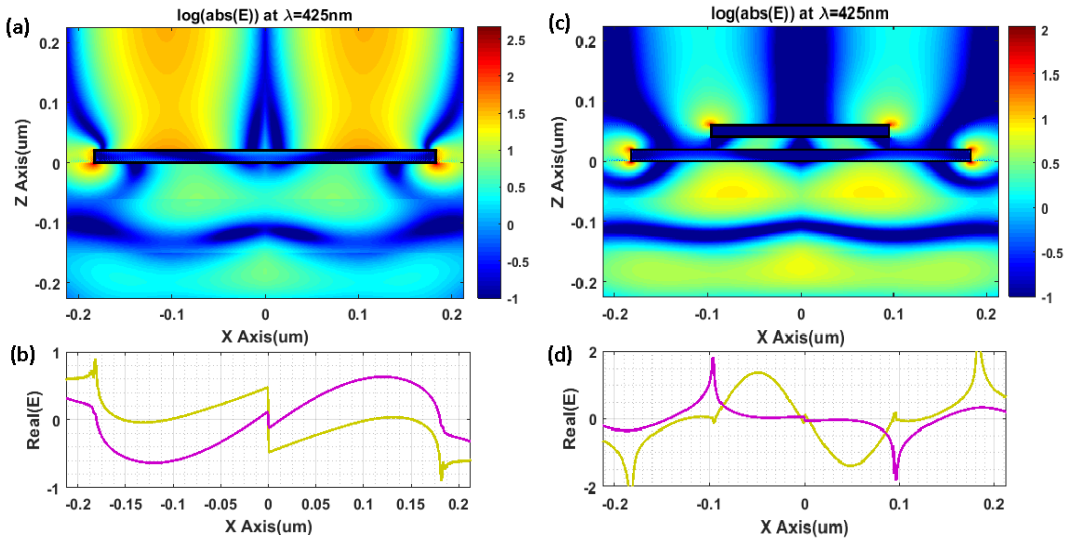

Figure 21 (a) Magnitude of E-field at λ=425nm in log-scale for conventional plasmonic grating filter (b) Corresponding cross section of real part of E-field at Metal-Air interface and Metal-dielectric interface (c) Magnitude of E-field at λ=425nm in log scale for plasmonic grating filter with proposed MIM structure (d) Corresponding cross section of real part of E-field at two Metal-Air interfaces on top and bottom metal layers. Real part is plotted to indicate the polarity and hence phase relationship.

Based on field plots, it can be seen that at Rayleigh Anomaly peak, the structure resonates such that two SPP modes on top and bottom interface of the metal grating at in phase and hence the scattering

field is also in phase. After adding the additional metal layer (of width equal to half the period), the added structure resonates at 180° phase shift, as shown in Figure 21 (d). Hence the scattering field are in opposite phase as well, which in turn cancels far field transmission. Figure 22 below shows the transmission spectra of two plasmonic filter with and without MIM structure designed for transmission at two different wavelengths.

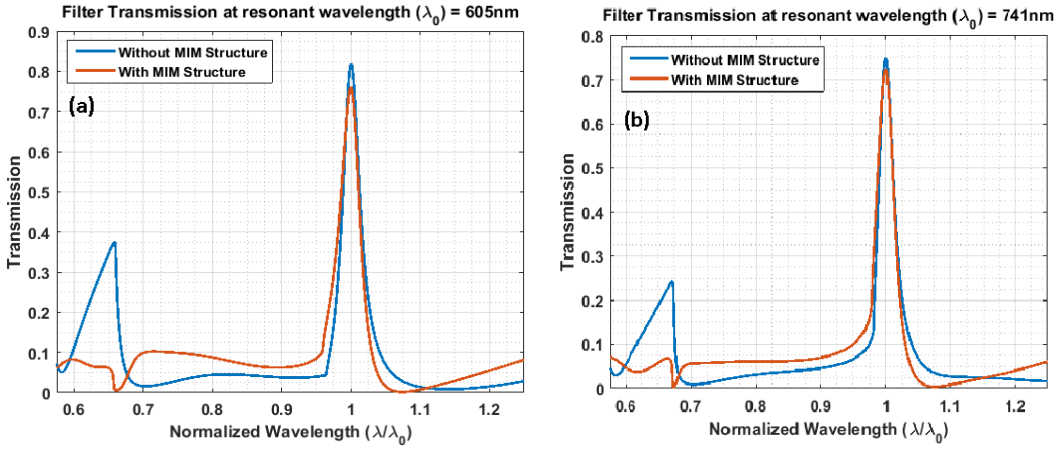

Figure 22 Transmission Spectra of Plasmonic Grating Filter with (red) and without (blue) proposed MIM structure at various grating period. (a) 400nm and (b) 500nm. The proposed filter improves desired to undesired peak ratio (extinction ratio) from 2.2 to 7.6 and 3.0 to 9.7 respectively.

Now since such structure requires two step lithographic process, the alignment of these two process steps can be a practical concern. Hence the sensitivity of peak ratio (desired vs undesired peak) was simulated with variation in width of the top metal layer and its placement with respect to bottom metal layer. Figure 23 below shows the design space in which the proposed design still has peak ratio of 7.

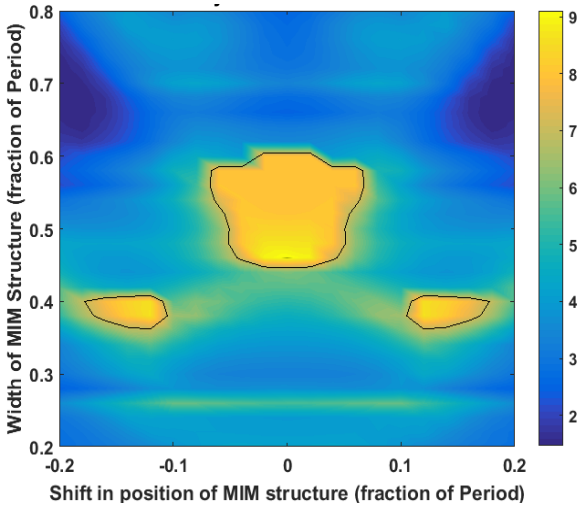

Figure 23 Sensitivity to process variations. The width of MIM structure was varied from 0.2 to 0.8×Period and shift in location of MIM structure was varied within ±0.2×Period. It can be seen that design has large tolerance around center point. Contour shows the design space where peak ratio is greater than 7.

2. Part IIA: High speed pipelined SAR ADC

2.1 Considerations for high speed pipelined ADCs

The conventional pipelined ADC requires analogue subtraction and multiplication at each stage, which is usually done in a single circuit called MDAC. The MDAC calculates residue in each stage by subtracting the equivalent analogue voltage of the ADC stage from the input voltage. The residue is then multiplied by gain G, which in simplest case is 2, such that it is full scale for the next stage. A typical pipelined ADC is shown in figure below:

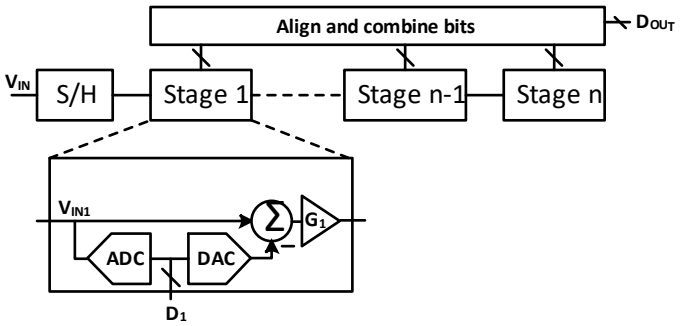

Figure 24 Conventional pipelined ADC

In the conventional pipelined ADC, the gain in each attenuates the input referred noise of the following stage, hence relaxing design constraint for following stages. However, it comes at the cost of design complexity and speed limitations. The MDAC, which is often used for calculating the residue and amplifying it, achieves such amplification using capacitance ratio and it is subject to mismatch. This gain error is detrimental to the ADC performance and various calibration schemes have been proposed to correct for it, which increases ADC complexity, power, and area. Secondly the MDAC is a closed loop circuit, which requires certain settling time based on its unity gain bandwidth and hence imposes speed limitation. In this paper we propose an architecture that obviates need for MDAC and hence reduces the complexity and increases conversion speed.

2.1.1 Effect of Gain Error in pipelined ADCs

In the simplest case, if the analogue gain G is not exactly equal to 2, it will cause local gain error around the codes determined by that stage. If the gain is higher than 2, it will overload the next stage and information is clipped. The sources of gain error are due to finite gain of Op-Amp and capacitor mismatch in the MDAC. The effect of gain error in the first stage has the worst impact in SQNR. Fig. 25 below shows degradation in SQNR and hence effective resolution as a function of standard deviation of gain error in first stage of a 10-bit, 12-bit and 14-bit pipelined ADC.

As it is evident from the plot below, to maintain 12-bit accuracy, we need better than 0.01% gain mismatch across 12 stages of conventional pipelined ADC. Various calibration and compensation techniques have been proposed to correct for the gain error [42-44].

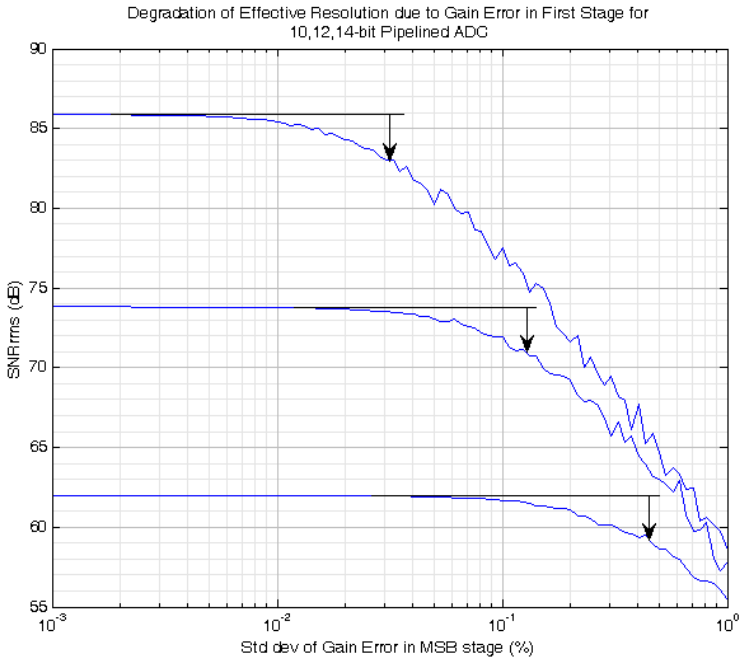

Figure 25 Degradation of pipelined ADC performance as a function of error in MSB block gain stage

The calibration schemes can be broadly categorized into foreground and background calibration scheme. In foreground calibration scheme, the ADC converter operation is interrupted for calibration, whereas in background calibration, the normal ADC operation continues while calibration happens in the background. Considering interruption in normal operation and possibility of drift in gain error originating from finite Op Amp gain, background calibration is preferred to foreground calibration. The skip and fill background calibration scheme proposed in [42] requires skipping some of the input samples in order to perform calibration and filling in the digital code for missing sample using non-linear interpolation. The interpolation of missing sample in this scheme only works if the input signal at that time was within 2/3 the nyquist bandwidth or else the interpolation error is much higher. Also, digital interpolation with 44 taps will at least require 22 sample latency in the output. Another technique proposed in [43] utilizes an additional stage that can be calibrated offline, while rest of the stages are working for normal ADC operation. At each clock cycle, the calibrated stage is swapped into the main ADC and another stage is taken out for calibration. While this scheme avoids skip and fill, it requires an additional stage, a comparator and calibration DAC with higher resolution than the ADC. Yet another technique often proposed for pipelined ADC gain error calibration uses injection pseudo-random noise into the ADC and derive effective radix in digital domain using correlation to digitally correct for gain errors [44]. All of these calibration schemes are complex and require extra power and area.

2.1.2 Speed limitation in pipelined ADCs

In addition to gain error and its effect in achieved resolution, the major speed limitation in conventional pipelined ADC is imposed by operational amplifier used in implementing gain stage.

Considering only linear settling, the maximum achievable switching frequency of a switched cap MDAC is given by:

$$f_s \leq \frac{\pi f_u}{\ln(2^N)} \tag{14}$$

Where f_u is the unity gain frequency of the operational amplifier and N is the settling resolution or ADC resolution. For 72° phase margin, we need non-dominant pole to be 3x higher than f_u and hence:

$$f_s \leq \frac{\pi f_{p2}}{3 \bullet \ln(2^N)} \tag{15}$$

Where f_{p2} is the location of non-dominant pole. For a given process the non-dominant pole is set by device parasitics and hence strongly depends on process node and device f_T. Hence it is seen that sampling frequency in pipelined ADCs show strong correlation with process node. Fig. 26 below shows speed trend for pipelined ADC published in ISSCC and VLSI from 1997 to 2021 (based on data from [45]).

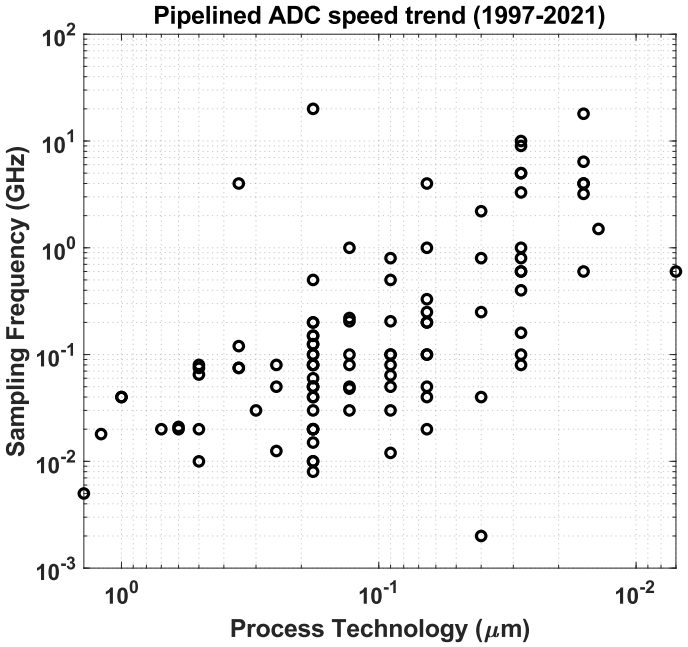

Figure 26 Pipelined ADC speed trend

However, in the case of open loop architectures such as flash ADC, there is no phase margin requirement that must be met and hence can operate faster than architectures with closed loop settling such as pipelined ADC. Hence, when noise is not a concern, it is favorable to forego the gain stage and make all the blocks equally important from noise point of view. This leads to a pipelined SAR architecture originally published in [46], in which the gain stage is removed, and each stage compares sampled input voltage with digital to analog converter (DAC) voltages based on conversion in previous stages. Such ADC was also published in US patent 7265704 [47].

2.1.3 Time Interleaving

In order to improve the speed, it is possible to time-interleave many slower ADCs such that overall conversion is faster. In doing so each sample and hold has M times longer settling time, where M is the number of time interleaving. However, the speed benefit comes at the cost of other issues such as timing accuracy and mismatch in nonlinearity and gain across various ADCs [47]. The design considerations and effect of gain mismatch and timing mismatch are detailed in reference 6. The effect of gain error across channels can be studied using spectral domain analysis. Even though each ADC samples are reduced speed, considering full BW of input signal, the input signal is under-sampled by each ADC individually. This results in heavy aliasing of input signal spectrum when we consider a single channel. However, when multiple channels are de-multiplexed after conversion, the aliasing is undone. For this to work perfectly, the aliased component of each channel needs to cancel each other. This results in strict requirement for gain matching across all channels. For a two-channel time interleaved system, when SNR is strictly limited by such gain mismatch, the limiting SNR is given by [47]:

$$SNR \leq \frac{4}{\alpha^2} \tag{16}$$

where α is the mismatch in gain across two channels.

For SNR of 72dB roughly lower than 3% mismatch between channels is required. The major source of gain error across channels is due to the fact that various samples are processed by different ADCs and hence the gain error is different for each sample. In addition to gain error, the nonlinearity in different ADCs also result in time varying non-linearity which requires calibration of each ADC to compensate for such error.

2.2 Advantages of pipelined SAR ADC architecture

The proposed architecture obviates need for analogue subtraction and multiplication and hence MDAC by changing reference voltage of i^{th} stage based on digital values of all bits higher than i^{th} bit. In this architecture, the analogue multiplication is eliminated since it is introduced only so that error voltage from previous stage is full scale to the next stage and doesn't affect the ADC conversion even if it is removed. The gain by factor of 2 helps in reducing the accuracy requirement progressively for lower resolution stages by enhancing the residue voltage at each stage. Then the analogue subtraction is eliminated by performing addition in the quantized (digital) domain. By eliminating analogue multiplication and subtraction, the proposed architecture relieves following two constraints of conventional pipelined architecture:

i. There is no need for gain error calibration since all the inter-stage gains are 1 by design and this reduces complexity due to calibration requirements.
ii. Each stage now only contains open-loop regenerative comparators, which can operate at much faster speed than operational amplifiers.

In addition, the proposed architecture employs time-interleaving, where each bit of each sample is processed by the same set of DAC and comparator and hence sample to sample error is more uniform than in conventional time-interleaved ADCs. Hence proposed architecture is favorable in terms of following additional constraint:

i. The sample to sample gain and offset error is uniform and hence doesn't degrade SNR performance even when time-interleaving is applied.

2.3 Design of 1GHz pipelined SAR ADC

The proposed architecture can be derived by simple transformations and reductions to the conventional pipelined ADC. The conventional pipelined ADC can be represented by following signal flow diagram.

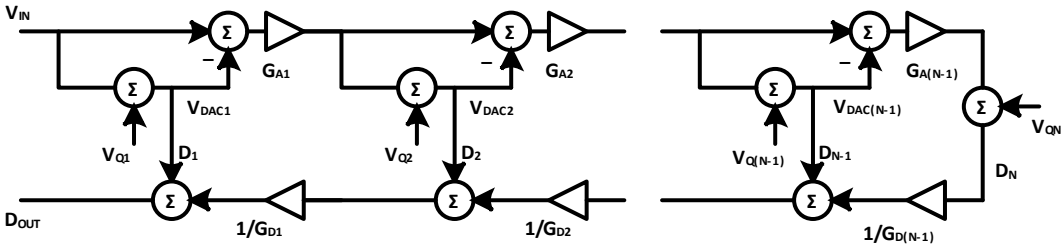

Figure 27 Pipelined ADC signal flow diagram

Where V_{Qi} are quantization noise, G_{Ai} are analog gains, D_i are digital outputs and G_{Di} are digital gains in i^{th} stage. The digital gains represent the fact that later stages have less significance in the final digital word D_{OUT}. For example, in a simple case of interstage gain of 2, the second stage digital output is MSB-1 and hence G_{D1} is 2, meaning second stage digital output is weighted by ½ that to the first stage.

In order to derive at the proposed architecture, we can eliminate the analog gain and subtraction in following manner. First to eliminate the gain from first stage, which is also the gain at the input of rest of the stages, we can transfer the first stage gain the output of the rest of the stages and scale all the inputs inside the remaining stage. Similarly, we can repeat this process for each gain resulting in following signal flow diagram.

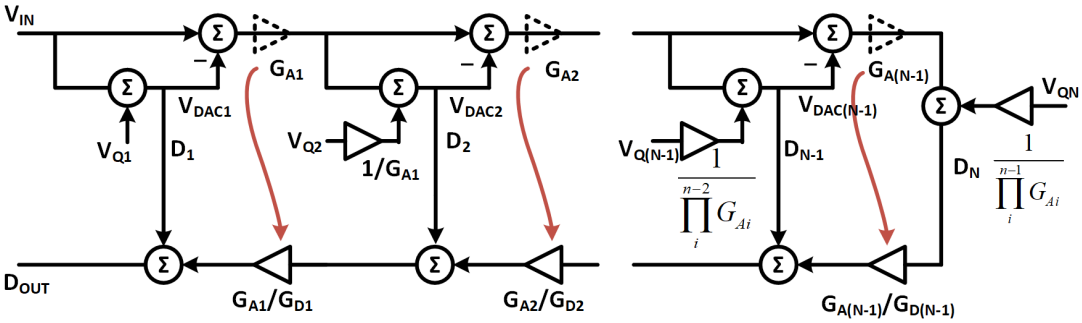

Figure 28 Pipelined ADC signal flow diagram after reduction 1

Now in the quantizer in stage, we choose to work with raw (unscaled) residue voltage instead of scaled residue. The effect of this is that we will need half the reference voltage of previous stage and corresponding quantization error will also be halved. Here all the analog gains have been transferred to digital domain at the cost of scaling the references. The ratios of analog to digital gains appearing in digital domain, can hence been chosen to be unity for simplicity.

Now the analog subtraction nodes can also be eliminated by choosing to work directly with the sampled voltages, instead of residues. Since the DAC voltages are subtracted to produce the residue, we can equivalently subtract such voltage in the later stages, such that there is only one summing node, which is the DAC of the next stage. Then the resulting signal flow diagram is as follows:

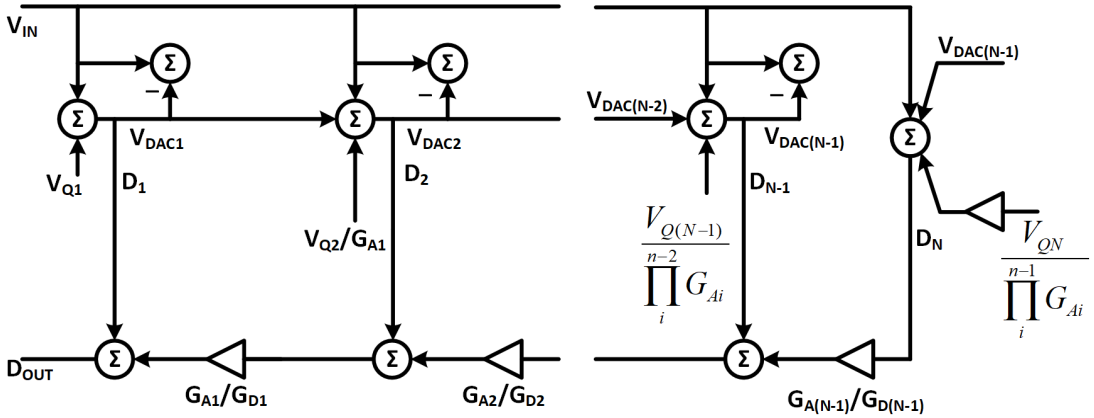

Figure 29 Pipelined ADC signal flow diagram after reduction 2

Here as we can see, the analog subtraction has become redundant and hence can be removed. Furthermore, as mentioned before, the analog to digital gain ratio can be conveniently chosen to be unity and hence the simplified signal flow diagram will result in:

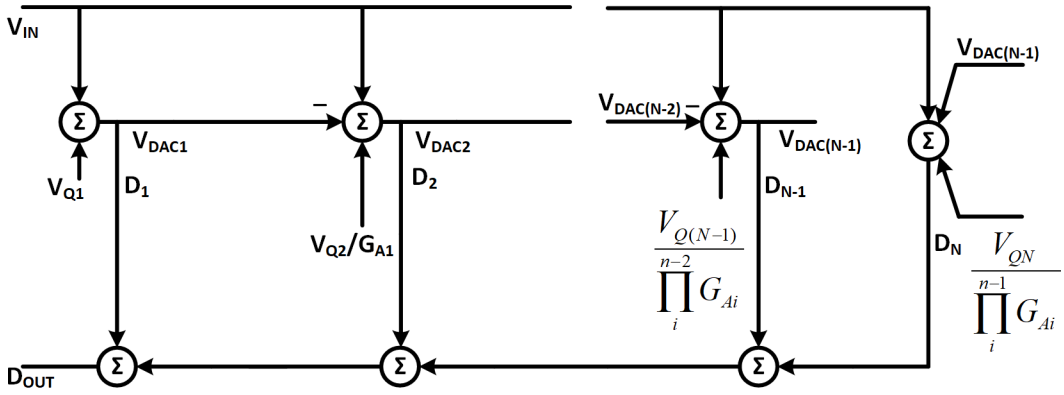

Figure 30 Pipelined ADC signal flow diagram after reduction 3

In this scheme, since second quantizer cannot be triggered until the first quantizer result is available and the resulting DAC voltages will need to be held for at least one additional clock cycle. Hence time interleaving needs to be implemented such that first stage converts next sample as soon as it is done with

comparison. The result from first stage then needs to be held in digital domain using chain of flip flops and hence DAC voltage doesn't need to be held. In each stage, then a separate DAC generates a voltage to compare the input voltage against. This results in following proposed architecture, hereafter called pipelined SAR ADC as shown in Figure below.

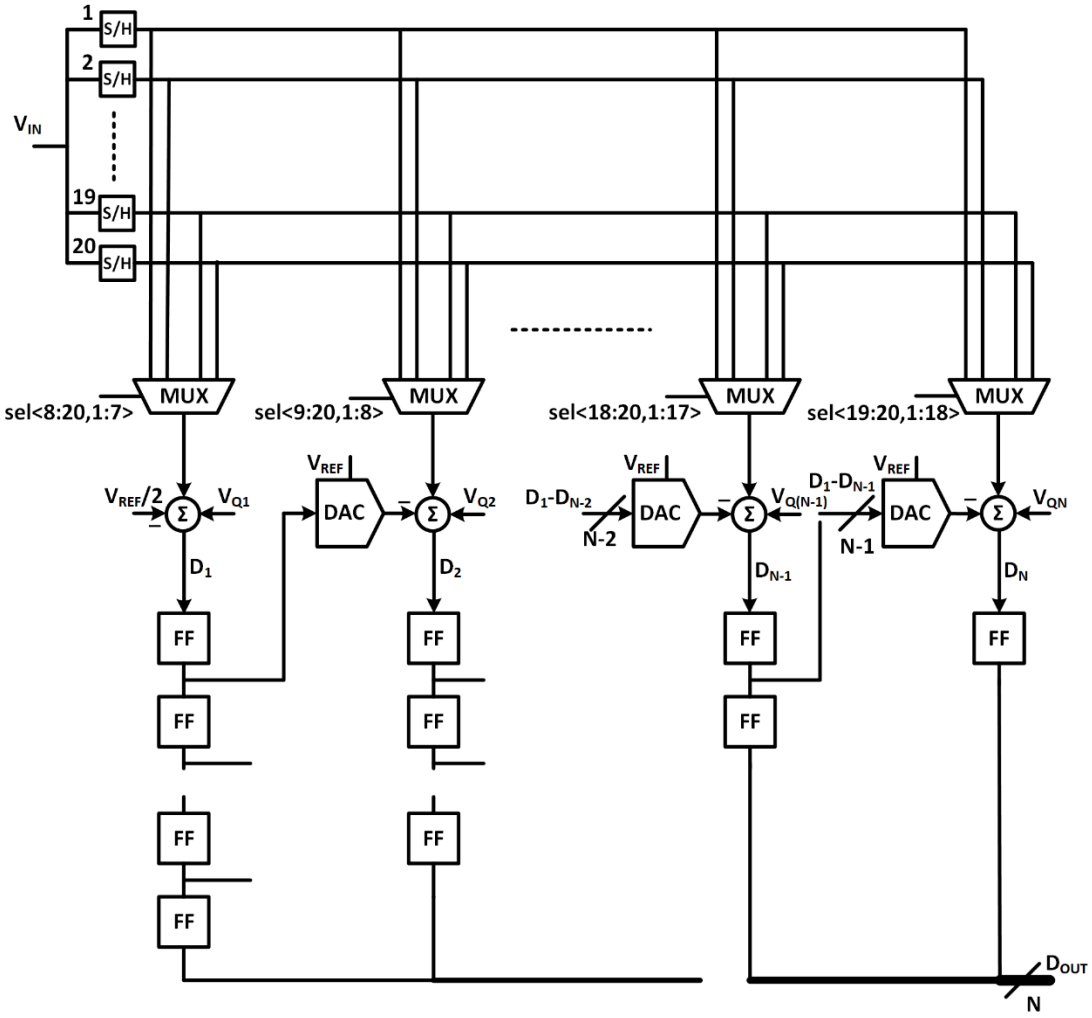

Figure 31 Pipelined SAR ADC block diagram

In above architecture the analogue subtraction and multiplication is eliminated at the cost of requiring progressively higher bit DAC in each stage. This trade-off however is compelling if speed and accuracy is of higher priority than area. Such pipelining and time-interleaving results in full speed converter, where speed of conversion is that of each stage and latency is N times the conversion time of each stage.

A 12-bit pipelined SAR ADC was implemented with 20 samplers and 12 comparators and DACs. This allowed for longer sample time for each sampler. Each sampler had 8 clock cycle sample time and

12 clock cycle conversion time, in which each clock cycle was used for converting each bit of the digital output. Figure 32 shows the timing diagram for the implemented pipelined SAR.

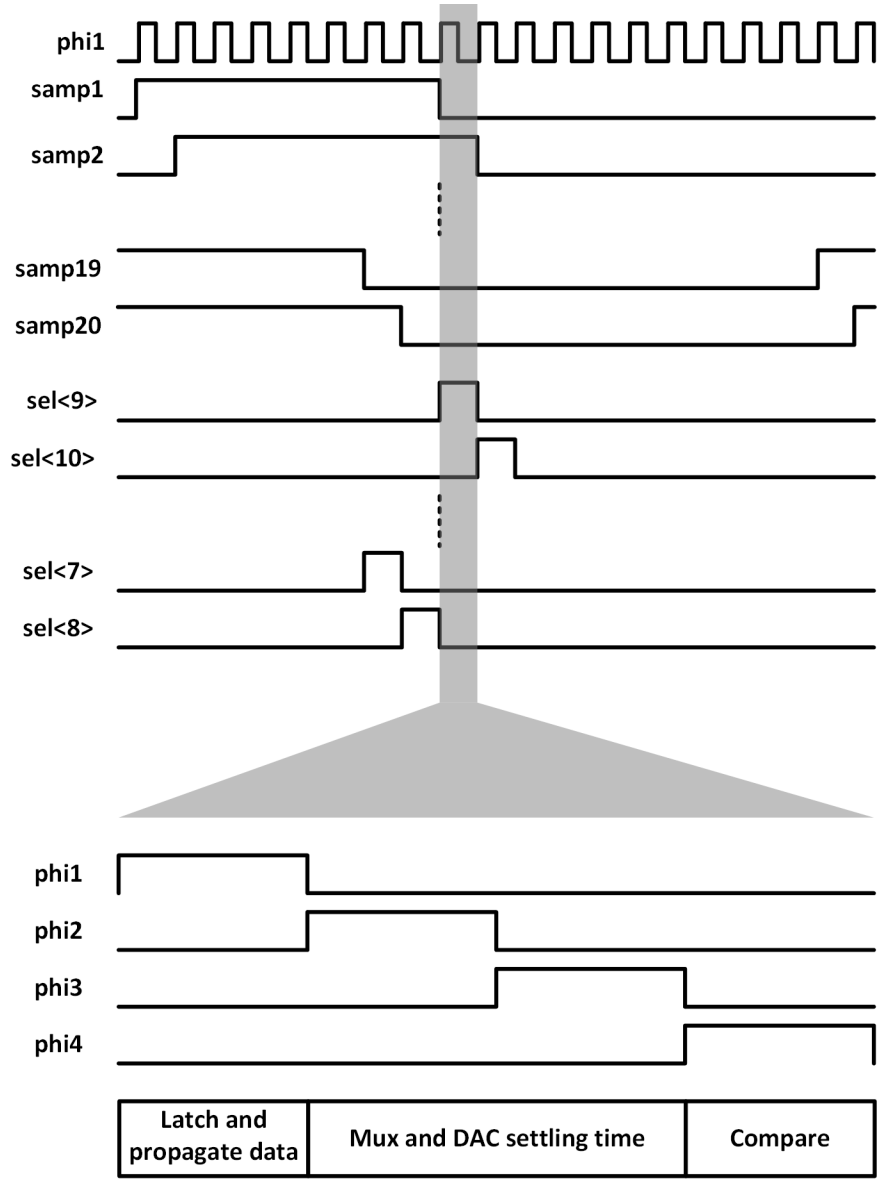

Figure 32 Timing Diagram

During each conversion time, one of the 20 samples is selected for each DAC/Comparator slice. The timing is configured such that out of 20 samplers, the outputs from 12 samplers are fed into each slice and rest is not selected are in sampling phase. In each conversion, there is latch and flip-flop propagation time, mux/DAC settling time and comparison time. The 20 samplers and mux selection lines are derived from internal state machine, which propagates a sequence of 1s in a cyclic fashion and loops around. The mux/DAC settling time is made twice as long compared to comparison time and flip-flop propagation time due to need to drive routing parasitics and device parasitics.

2.3.1 Sampler design

The sampler was designed using boosted switch [48] and bottom plate early switch followed by a source follower buffer. Figure 33 below shows the schematic of the differential sampling circuit.

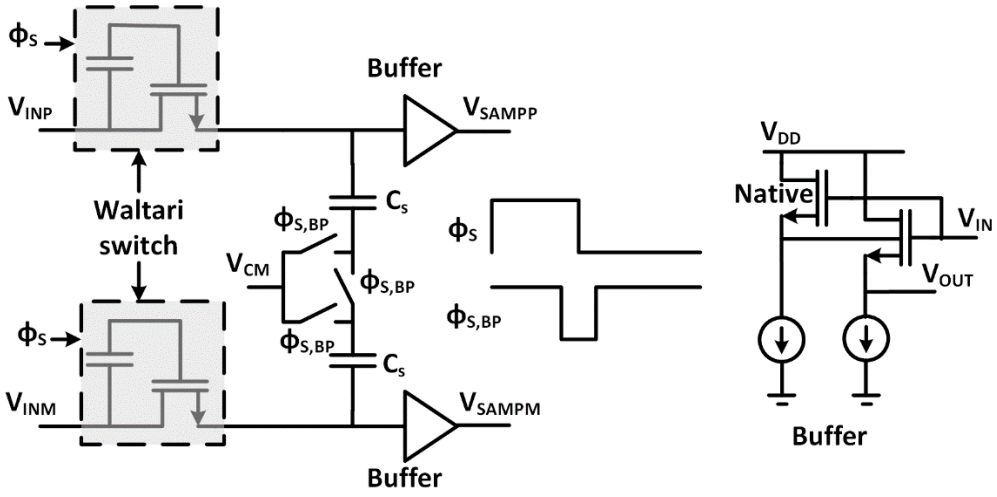

Figure 33 Sampling Circuit

By including bottom plate sampling switches which opened earlier than the main sampling switch, the residual signal dependent charge injection from the main sampling switch is suppressed since the capacitors are open when the switch opens. The bottom plate is then connected back to V_{CM} once the sampling process is complete. The boosted sampling switch had on resistance R_{ON} of 20 Ω and sampling capacitor was 2.5 pF. The sampling capacitor was sized such that kT/C noise was 57 μV_{rms}, which would make the design limited by quantization noise rather than thermal noise. The sampled voltages are then buffered using source follower buffers. The source follower buffer transistor was bulk biased using another source follower with a native device. This allowed for reducing non-linearity due to signal dependent bulk voltage as it would occur in the case of normal source follower.

2.3.2 Preamplifier and comparator design

The comparators were preceded by preamplifiers, which allowed to isolate the comparator kick-back noise as well as functioned as block for performing differential subtraction of the sampled voltage and DAC voltage. The preamplifier was designed using PMOS input differential pair with current output, which was fed into the comparator as input. The preamplifier output current mirror was 1:2 and that in the comparator input was 1:8 and hence there was 16x current gain. The preamplifier was not clocked such that it is always tracking the inputs. Based on simulation, keeping preamplifier online allowed for faster settling than when preamplifier is enabled only during comparison time. However, this meant there is no auto-zeroing and hence preamplifier offset would not be compensated for. Hence a pair of differential tunable current sources were used such that each preamplifier could be calibrated for offset errors. During such calibration, the variable current can be varied until the bit output corresponding to a

particular preamplifier/comparator slice produces equal number of ones and zeros (due to noise) when the input is set to zero. Figure 34 below shows the schematic of the preamplifier and the comparator circuits.

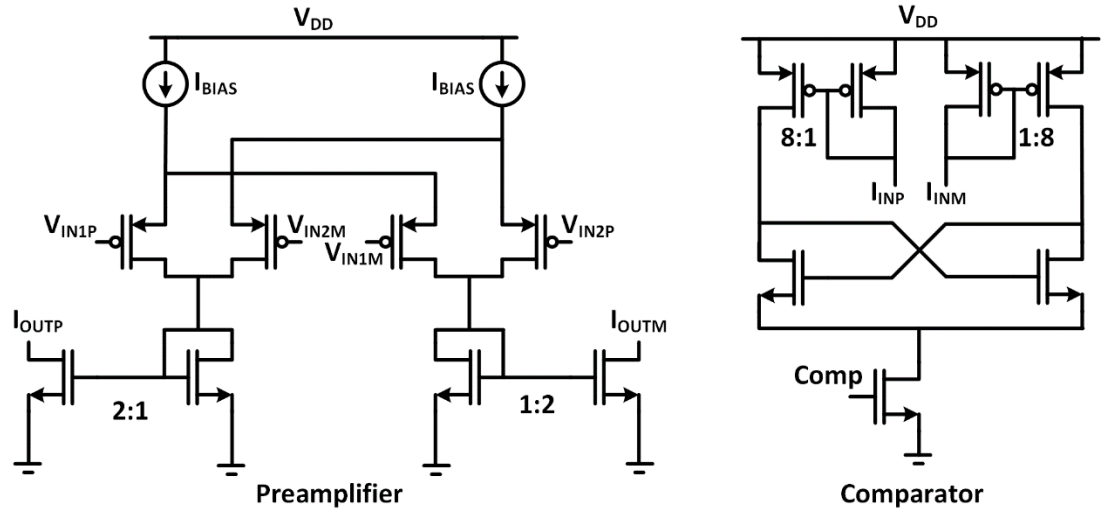

Figure 34 Preamplifier and comparator schematic

2.3.3 Current steering DAC design

Due to high speed considerations current steering DAC was considered for this project. The DAC was segmented into thermometric DAC and a binary DAC. Such segmentation allowed for reducing number of unit current elements from 4096 to 128. The DAC schematic is shown below.

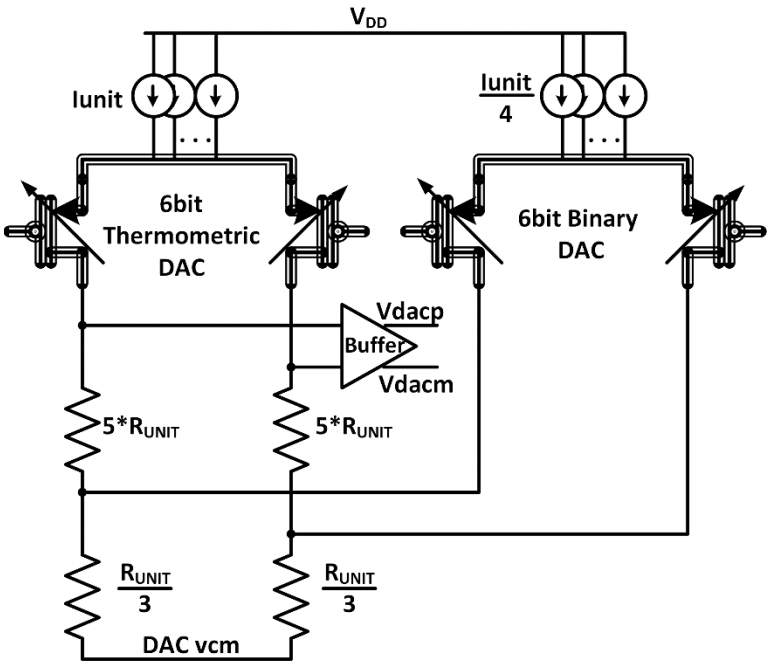

Figure 35 12-bit Segmented DAC schematic

The DAC was implemented using distributed current sources with current steering transistors acting as second level cascode devices. The current sources were terminated into resistive branch as indicated. The DAC output voltage is then given by:

$$V_{DAC} = I_{UNIT} D_{THM} \left(5 + \frac{1}{3}\right) R_{UNIT} + \frac{I_{UNIT}}{4} D_{BIN} \frac{R_{UNIT}}{3} \quad (17)$$

Which can be simplified as:

$$V_{DAC} = (64 D_{THM} + D_{BIN}) \frac{I_{UNIT} R_{UNIT}}{12} \quad (18)$$

The unit resistor elements were chosen to be 25 Ω based on speed considerations. Then the require unit current to generate 1.1V peak to peak signal is about 128 µA. The bias current can be set externally, however reducing bias current would reduce the full scale and hence kT/C noise starts to dominate.

2.4 Simulation Results

The design was implemented in TSMC 65 nm process and simulated. The following plot shows the spectrum of the sampled voltages.

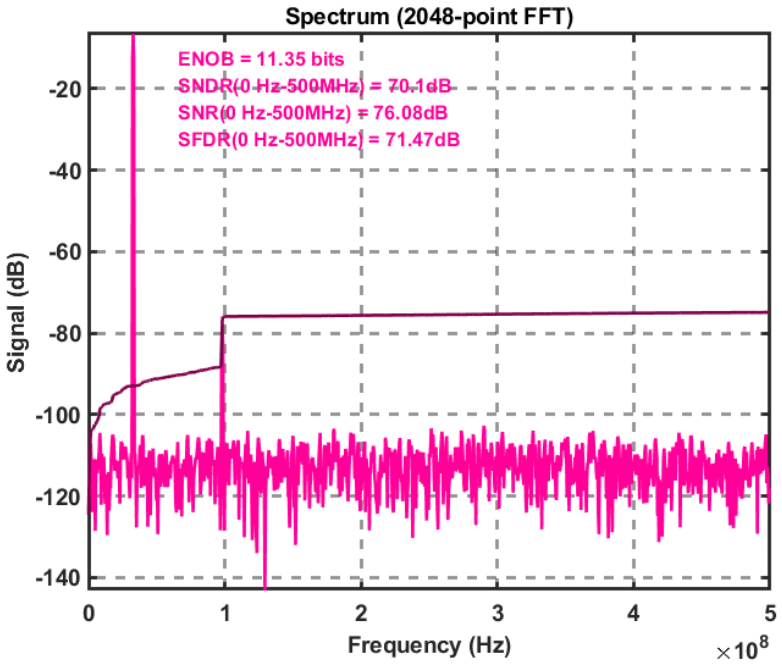

Figure 36 FFT Spectrum of sampled voltage

The sampled voltage is linear up to 71 dB and performance is limited by non-linearity of the source follower buffer. The buffer was biased at 100 µA current and schematic was as shown in Fig. 33. The buffer had third order harmonic of 72.8 dB, when input signal was 1V differential amplitude. Some of the additional distortion was contributed by sampling process, which included residual signal dependent charge injection. Additionally, the settling error while operating at 1GHz rate also contributed to

additional non-linearity. However, as will be discussed later, some of the non-linearity will be cancelled due to similar non-linearity in the DAC source follower buffer.

The DAC was simulated for systematic DNL/INL and mismatch. Due to finite R_{OUT} or current sources, the DAC linearity will be affected. Therefore, double cascode were used in unit current elements. This allowed for non-linearity be improved however for high current the limitation is still due to finite R_{OUT} of the current sources. The second level cascode devices also acted as current steering devices whose gate voltage switched from dac_lo to dac_hi voltages while turning on and off. Figure below shows the DNL/INL of the DAC due to systematic error contributed by finite R_{OUT}.

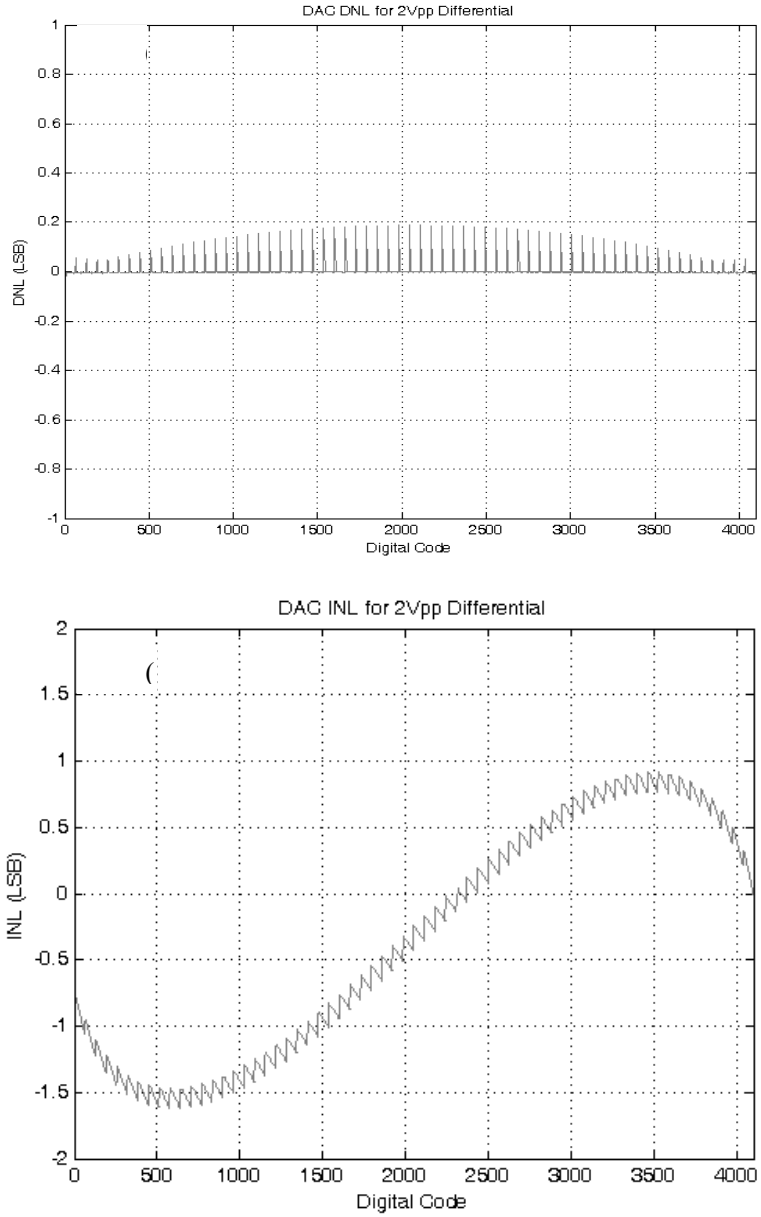

Figure 37 (a) DAC DNL plot (b) DAC INL plot

As shown in figure 37 (a), there are huge DNL spikes at the major code transitions. Since the DAC was segmented, at the major code transitions when all of the binary DAC elements need to be turned off and a single DAC element in thermometric segment needs to be turned on, there are glitches which takes longer to settle. Hence there are these spikes in DNL plot. The INL across the code space is mainly due to finite R_{OUT} of the unit current elements and it is about ±1.5 LSB.

The DAC is expected to have additional DNL/INL due to mismatch in current elements which are spread over large distances. Hence a monte carlo simulation (N=200) was run to estimate the error due to mismatches. Figure below shows the results of the monte carlo simulation.

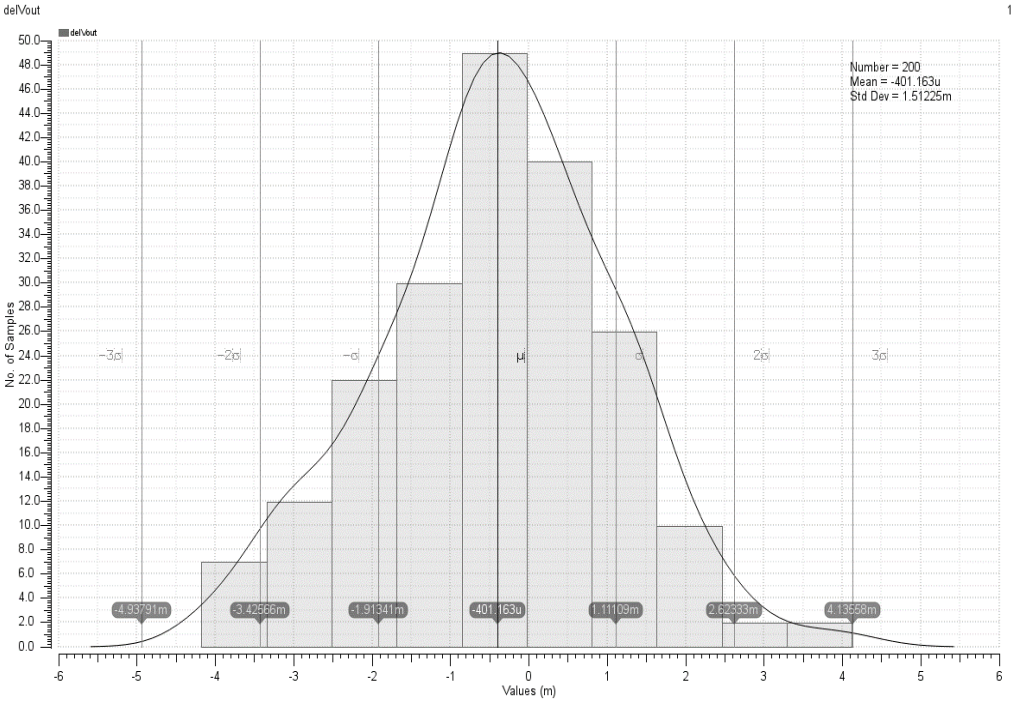

Figure 38 Monte carlo simulation result

Based on the simulation, the standard deviation of DAC voltage across various perturbations in current elements is 1.5mV. This means it is expected to have 3 LSB of error in 63% of the chips. However, such simulation included extreme process variation across multiple chips and hence on a single chip, the mismatch itself is expected to be less.

The DAC buffer was designed using PMOS input devices with body tied to the source. The DAC buffer was more linear than the sampler buffer. It was simulated to have third order distortion of -76 dB at 1V differential amplitude and 100 µA bias current. Since the feedback and the input had similar distortion levels as it connected to the comparators, a portion of the distortion is cancelled as can be seen in the final overall simulation. Also, since some of these non-linearities are systematic and hence it can be calibrated out as it is consistent for a particular chip.

Figure below shows the output spectrum of the ADC at 1GHz and 1V input amplitude.

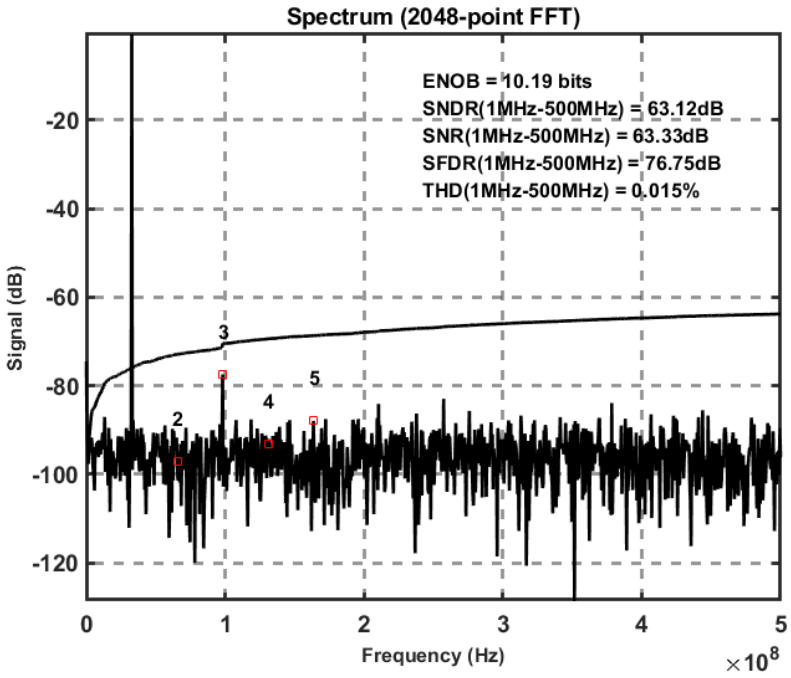

Figure 39 Output spectrum at 1GHz and 1V input amplitude

The final simulation was run at various amplitudes and input frequencies. The figure below shows the simulation results for various input amplitudes.

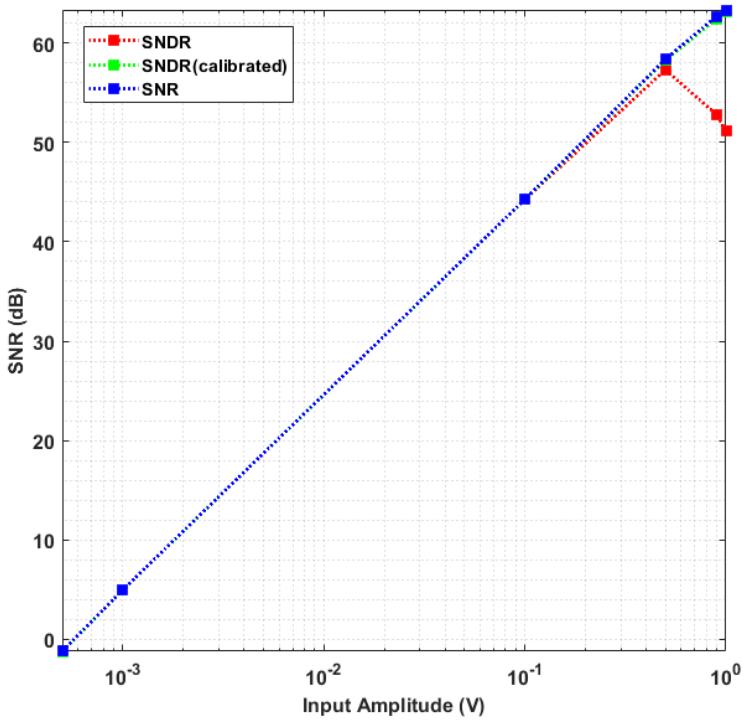

Figure 40 Input amplitude sweep

Based on simulation results, the peak SNDR is 63 dB and is limited by kT/C noise if the differential amplitude is limited to 1V and it is limited by distortion if the differential amplitude is changed to 2V. Figure below shows the simulation results of changing input frequency.

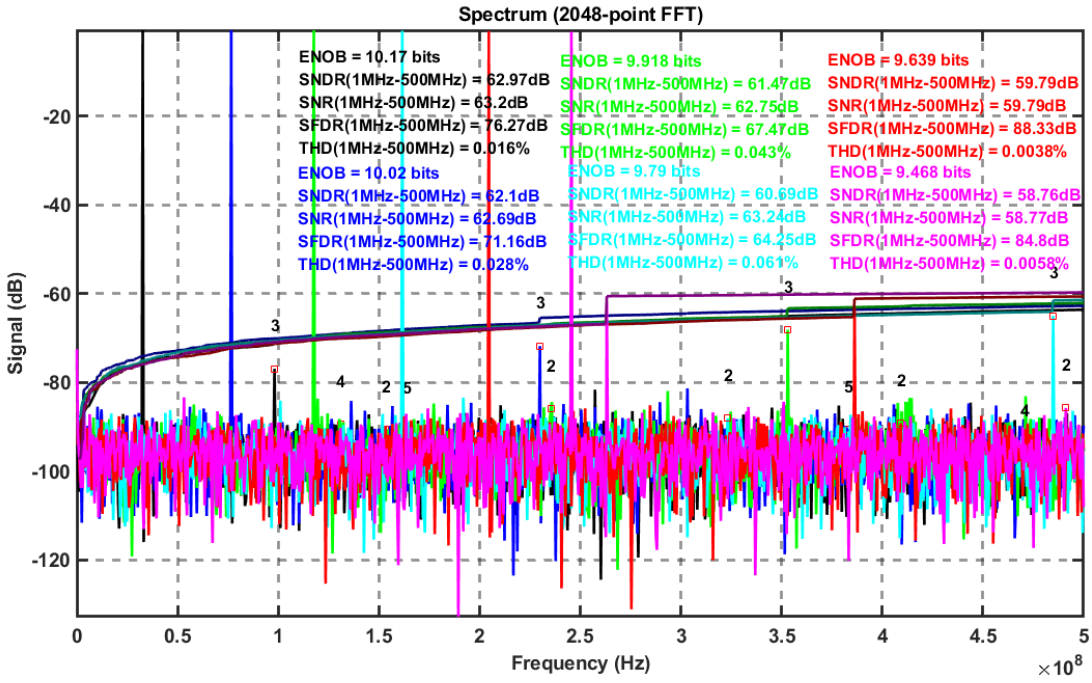

Figure 41 Input frequency sweep

Based on above simulation, the design works up to 1Gsps at 1V reference and 1V signal amplitude. Figure below shows the layout of the chip.

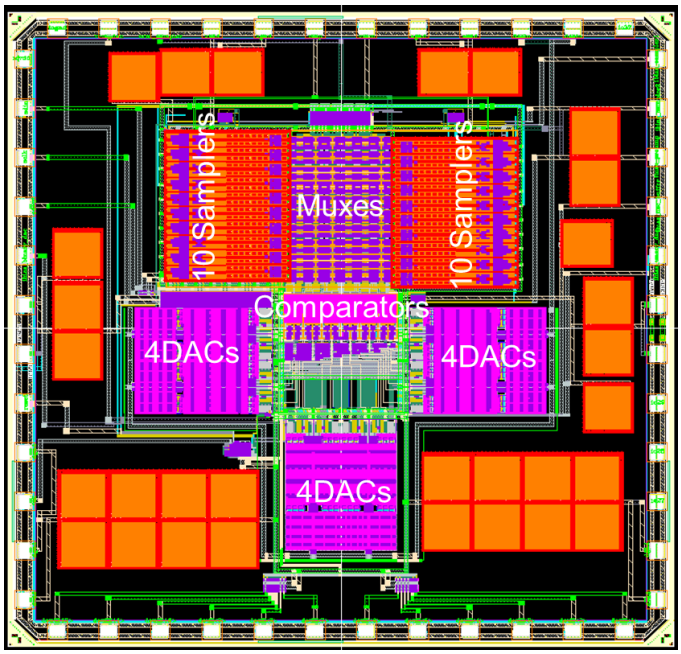

Figure 42 Chip layout

3. Part IIB: High dynamic range ΣΔ ADC architecture

3.1 Considerations for high dynamic range audio ADCs

The audio analog to digital converters are often very high dynamic range due to the extent of the human hearing, which extends from 0 dB SPL to 120-140 dB SPL. The 0 dB SPL is equal to 20 µPa and is considered the threshold of human hearing, while 120-140 dB SPL is the pain threshold for humans. Based on these the microphone system should have dynamic range greater than 100 dB, in order to not lose information that could be perceived by human ear, when played back. Hence the state-of-art ADCs in audio range typically have dynamic range greater than 100 dB. When specifying the ADCs for audio range normally the distortion and SNR specification is specified at 94 dB SPL, which corresponds to 1 Pa. For considerations for ADCs, the microphone sensitivity and distortion also need to be considered. For example, if the microphone sensitivity is low, the input referred noise of the ADC has to be very low. In addition, the distortion in the microphone directly impacts the overall system performance. In past the Condenser Microphone and Electret microphones have been used. Recently piezoelectric microphones in small packages have also been popular. However due to lower sensitivity and higher noise, the capacitive microphones (C-MEMS) chosen for this project. The change in capacitance due to acoustic pressure is non-linear as the distance between the capacitor is proportional to the applied pressure. Hence sensing capacitance will yield large non-linearity. Therefore, often constant charge sensing scheme is often employed in which the charge across the C-MEMS microphone is kept more or less constant by using large resistors as biased to a fixed voltage as shown in figure below:

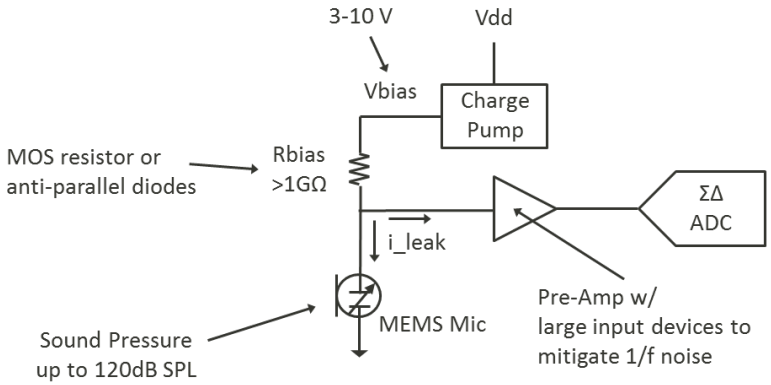

Figure 43 Typical biasing scheme for C-MEMS microphone

The C-MEMS microphone can be further implemented using dual back plane structure such that some of the displacement causes differential change in voltage and some of the common mode noise in the system is cancelled. Following figure represents the typical dual back plane C-MEMS microphone structure.

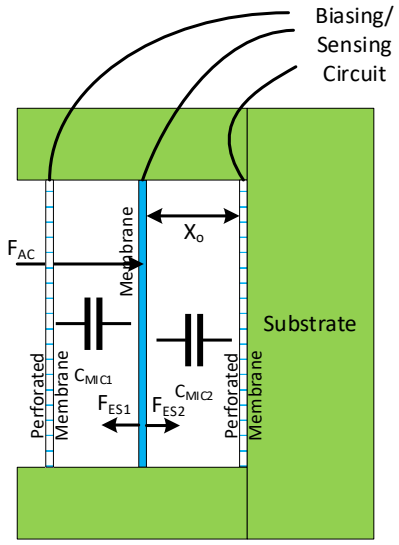

Figure 44 Dual back plane C-MEMS microphone

Here we have two electrostatic forces and hence the force balance equation results in following governing equation:

$$m\ddot{x}+\beta\dot{x}+kx=F_{ES2}-F_{ES1}+F_{AC}=\frac{1}{2}\frac{\varepsilon_O A}{(x_O-x)^2}V_2^2-\frac{1}{2}\frac{\varepsilon_O A}{(x_O+x)^2}V_1^2+F_{AC} \qquad (19)$$

The above equation can be solved for circuit parameters resulting in following equation:

$$C_1^2V_1^2-C_2^2V_2^2+2\varepsilon_O Akx=2\varepsilon_O AF_{AC} \qquad (20)$$

In dual back plane C-MEMS microphone, the central terminal is biased to a bias voltage through a large resistor and the voltage across two backplanes in sensed. In above equation, then total charge $C_1V_1+C_2V_2$ is kept constant. Due to non-linear nature of the solution, it can be solved numerically and following plot can be generated to shows the benefit of constant charge sensing scheme vs constant voltage sensing scheme.

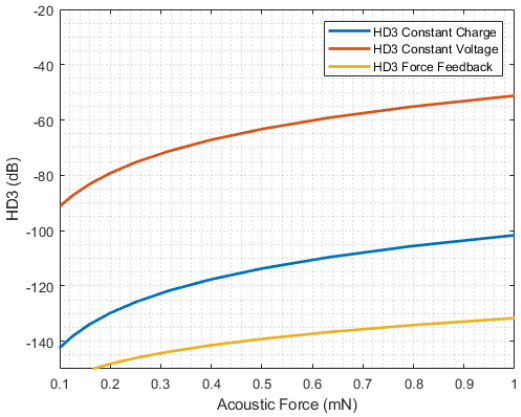

Figure 45 C-MEMS microphone non-linearity

As can be seen, for most applications, constant charge sensing scheme is sufficient and hence force feedback approach is not considered. The force feedback scheme however can yield better linearity at the cost of circuit complexity and higher power. At the same time, the constant voltage sensing scheme yields higher non-linearity than constant charge sensing scheme to the point where non-linearity is becomes an issue.

Furthermore, circuit noise is another major concern for high dynamic range audio processing and hence needs to be addressed very carefully. One of the issues concerning noise if the flicker noise inherent in any MOS devices. Whereas thermal noise issue can be partly mitigated by simply increasing the current and hence increasing gm and reducing input referred noise, such is not the case for flicker noise. The flicker noise power spectral density (PSD) depends on the bias current. As there are more carriers in the channel, the probability of trapping and un-trapping of carriers in trap states also increases and hence flicker noise depends on the bias current. Therefore, bias current cannot be used to deal with flicker noise. Often chopping and correlated double sampling (CDS) techniques are used for mitigating flicker noise. The chopping technique requires that input is upconverted as it passes through the circuit block and is down-converted at the output. In doing so, the flicker noise is added when the signal is at chopping frequency and hence is separated from the noise. By down-converting the signal is brought back to baseband and noise is upconverted. Hence the flicker noise is cancelled. In CDS technique, the flicker noise is double sampled, once without the signal and hence with the signal. In doing so, the sampled flicker noise in first phase is subtracted from the input in the second phase, hence subtracting the noise that would be added. In this scheme, the correlation of noise from phase1 to phase2 is assumed to be high such that the cancellation works almost perfectly at low frequencies. However, at higher frequencies the correlation between two noise sampled at two instances are not correlated and hence noise is not perfectly cancelled. In that sense, the noise shaped rather than cancelled. Since flicker noise has 1/f PSD, it is often sufficient to shape the flicker noise.

Although chopping and CDS can be employed to reduce the effect of flicker noise, these techniques have certain disadvantages:

i. Chopping introduces chopping artifacts such as glitches in the waveform, which adds to the settling time required for the circuit block.
ii. Chopping technique also requires that the circuit block can process signal at the chopping frequency with enough settling time constants.
iii. Due to chopping at the input, there is switches capacitor resistor formed due to input parasitic capacitance of the circuit block, which leads to leakage path and can be problem when interfacing with high impedance sensors such as C-MEMS microphones.
iv. CDS technique requires additional phase for sampling noise.
v. Additional kT/C noise from the CDS capacitor is added to the noise budget.
vi. The CDS technique requires that at least half of the time the circuit block is sampling noise and not actually processing the signal.

3.2 Advantages of pseudo-pseudo differential architecture

To remedy issues inherent in chopping and CDS techniques, a pseudo-pseudo differential architecture can be used. In this scheme, a single ended circuit block is used twice to process positive and negative signal. When processing differential signal in such fashion, the inversion is already implied. For example, positive signal will be $V_{CM}+V_{IN}/2$ and negative signal will be $V_{CM}-V_{IN}/2$. Hence chopping switches are not needed anymore. Also, a single ended circuit block, with half the power and area can be used to process fully differential signal. The noise is added similarly in two phases of operation, while the signal is on opposite polarity. Hence when taking a subtraction of the output, the noise (low frequency) is cancelled. Therefore, while getting the benefits of differential topology and noise shaping, the pseudo-pseudo differential architecture allows for reduced power consumption. In addition, the aforementioned issues with chopping and CDS are eliminated.

3.3 Design of pseudo-pseudo differential ΣΔ ADC

Due to benefits outlined above, a pseudo-pseudo differential architecture is investigated for use in sigma-delta ADC for audio application. Following block diagram represents the proposed architecture.

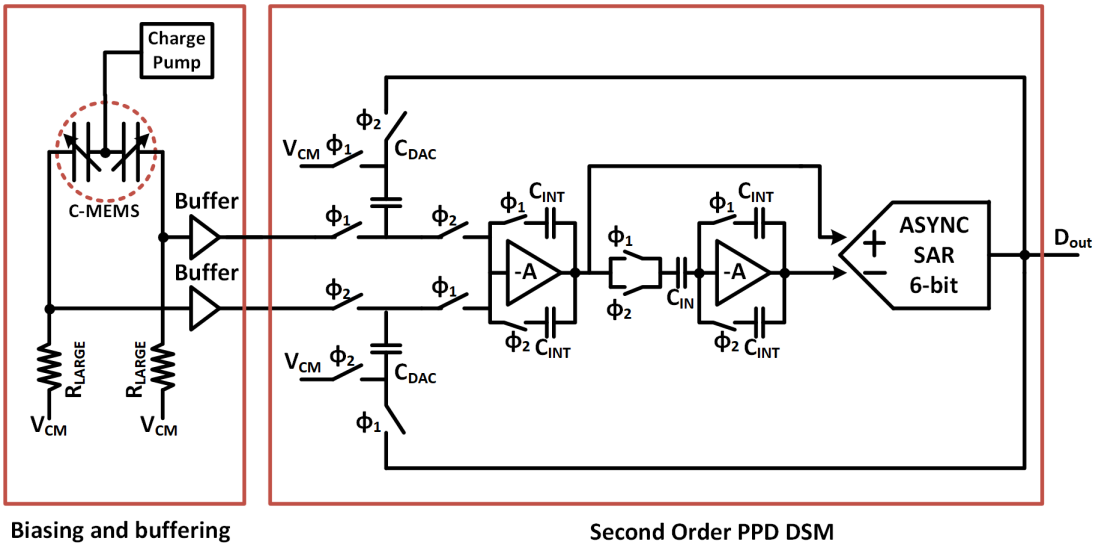

Figure 46 Pseudo-pseudo differential Sigma Delta ADC architecture

As shown in the figure above, the C-MEMS microphone is biased to boosted voltage of 10V, and together with biasing resistors (R_{LARGE}) provide constant charge biasing scheme. Due to large time constant of the biasing network, the change in capacitance changes the voltage across differential capacitors instead of drawing charge from the biasing network. This differential voltage is buffered and then applied to the sigma delta ADC. The ADC samples the differential voltage one at a time on phase 1 (ϕ_1) and phase 2 (ϕ_2) using a 4pF sampling capacitors (C_{DAC}) which is formed of the feedback DACs. The DAC is then fed with the feedback digital word (6-bits), which applied $C_{DAC}(V_{IN}-V_{DAC})$ amount of charge to the integrator virtual ground. Which is then integrated on each of the integrating capacitors

(C_{INT}) successively in phase 1 and phase 2. Unlike conventional integrator circuit the pseudo-pseudo differential integrator has two capacitors, which are active in each phase processing either positive or negative signal. The second integrator is formed using similar approach; however, input capacitor is reduced to 100 fF and integrating capacitor is reduced to 200 fF. Due to the gain of first integrator, the kT/C noise from second stage when referred to the input of the sigma delta ADC is highly attenuated and hence smaller capacitors could be used. Therefore, the second operational amplifier is also designed to operate at lower power due to reduced load. The output of first integrator is then given by:

$$V_{INT1} = z^{-1}V_{INT1} - \frac{C_{DAC}}{C_{INT1}}(V_{IN} + z^{-1}V_{DAC}) \tag{21}$$

Here, $C_{INT1} = C_{DAC} = 4$ pF. Now the second integrator output is given by:

$$V_{INT2} = z^{-1}V_{INT2} - \frac{C_{IN}}{C_{INT2}}(2V_{INT1}) \tag{22}$$

Here $C_{INT2} = 2C_{IN} = 200$ fF. The factor of 2 is due to the fact that voltage across C_{IN} will be changing from $-V_{INT1}$ to V_{INT1} in each phase and hence twice V_{INT1} amount of charge is disposed at the virtual ground of second integrator. Therefore,

$$V_{INT1} = -\frac{V_{IN}+z^{-1}V_{DAC}}{1-z^{-1}} \tag{23}$$

and

$$V_{INT2} = -\frac{V_{INT1}}{1-z^{-1}} = \frac{V_{IN}+z^{-1}V_{DAC}}{(1-z^{-1})^2} \tag{24}$$

Then the input to the quantizer $V_{INT1} - V_{INT2}$ is given by:

$$V_{INT1} - V_{INT2} = -\left(\frac{1}{1-z^{-1}} + \frac{1}{(1-z^{-1})^2}\right)(V_{IN} + z^{-1}V_{DAC}) \tag{25}$$

Now the quantization noise E_Q is introduced at the asynchronous SAR ADC. Hence,

$$V_{DAC} = V_{INT1} - V_{INT2} + E_Q = -\frac{2-z^{-1}}{(1-z^{-1})^2}(V_{IN} + z^{-1}V_{DAC}) + E_Q \tag{26}$$

Hence,

$$V_{DAC}\left(1 + \frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2}\right) = -\frac{2-z^{-1}}{(1-z^{-1})^2}V_{IN} + E_Q \tag{27}$$

$$D_{OUT} = V_{DAC} = -(2 - z^{-1})V_{IN} + (1 - z^{-1})^2 E_Q \tag{28}$$

Hence as shown in equation (28), the quantization noise will be shaped by second order. The STF is not unity and has peaking at higher frequencies, which doesn't affect the performance as there will be no signal applied at those frequencies. The STF can be modified to become unity across all frequencies by including feed-in path directly from input to the input of the quantizer, however doing so will require additional summation block, which consumes power and hence such option was not included in this architecture. The subtraction of two integrator output by directly applying them as differential signal to the quantizer eliminates need for any summation block and hence simplifies the implementation as well as saves power.

3.3.1 Design of first operational amplifier

The first operational amplifier is designed as a single ended inverter based push-pull amplifier with gain boosting as shown in Figure below:

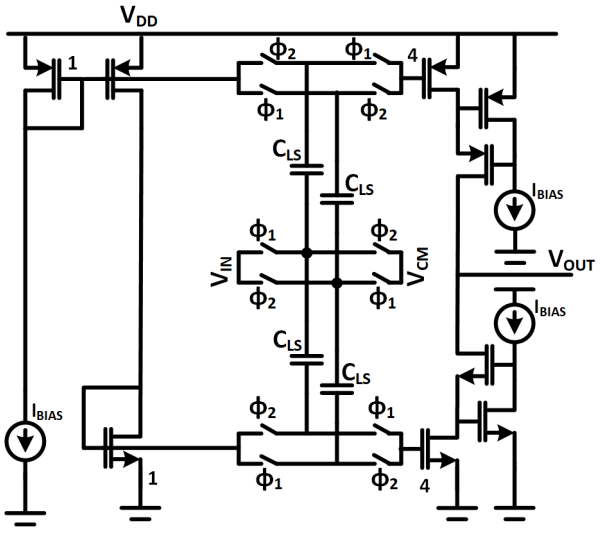

Figure 47 Schematic of first operational amplifier

A set of four C_{LS} capacitors are used to level shift the input to PMOS bias voltage as well NMOS bias voltages. In order to mitigate the effect of kT/C noise due to level shifting capacitors, they are sized equal to the input capacitor (C_{DAC} in Figure 45). A novel and simple gain boosting technique is applied where only one branch current is used per gain boosters. The amplifier has loop gain of 54 dB and unity gain bandwidth of 110MHz at 1pF output load. The phase margin was 78 deg. Figure below shows the stability analysis of the first operational amplifier design.

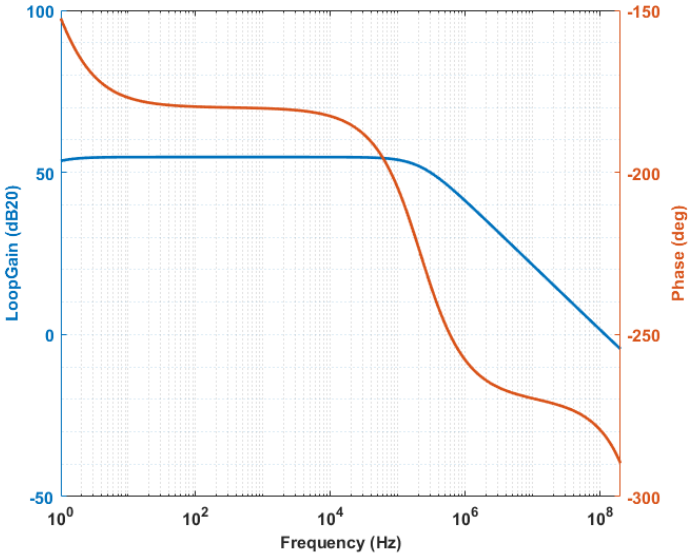

Figure 48 Stability analysis of first operational amplifier

3.3.2 Design of second operational amplifier

The second operational amplifier is designed as a single push-pull amplifier push-pull amplifier as shown in Figure below:

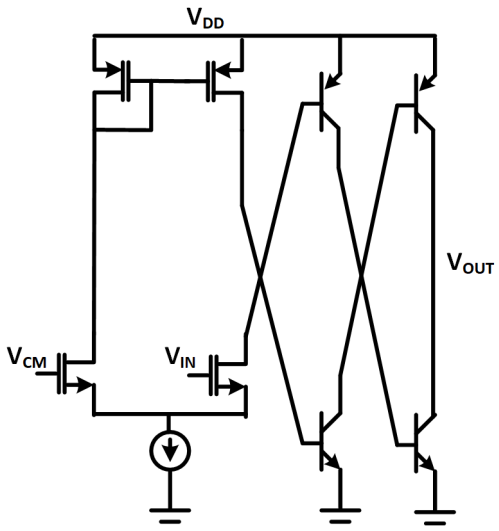

Figure 49 Schematic of second operational amplifier

Due to large voltage swing at the output of the second integrator, the second operational amplifier needed to support such large swing and hence cascodes were avoided to maintain maximum swing with reasonable gain. In first stage was biased at 500nA and the total static current for the amplifier was 9uA. The amplifier has loop gain of 63 dB and unity gain bandwidth of 10MHz at 1pF output load. The phase margin was 45 deg. Figure below shows the stability analysis of the first operational amplifier design.

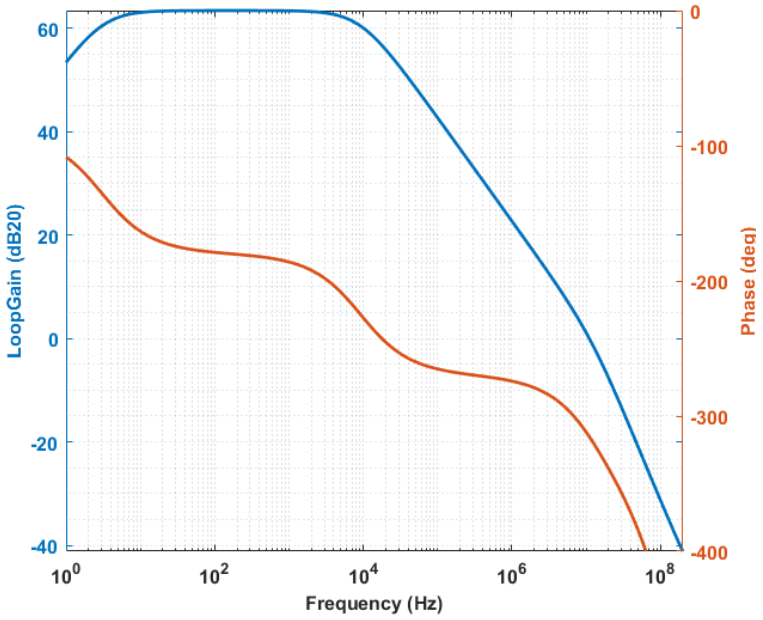

Figure 50 Stability analysis of second operational amplifier

3.4 Simulation results

The design was implemented in TSMC 65nm process using core devices operating at 1.2V supply. The asynchronous SAR was also implemented at circuit level. The capacitors were chosen to be metal-insulator-metal (MIM) capacitors. The design overall consumed 52uW of power. Figure below shows a typical output spectrum of the implemented sigma delta ADC.

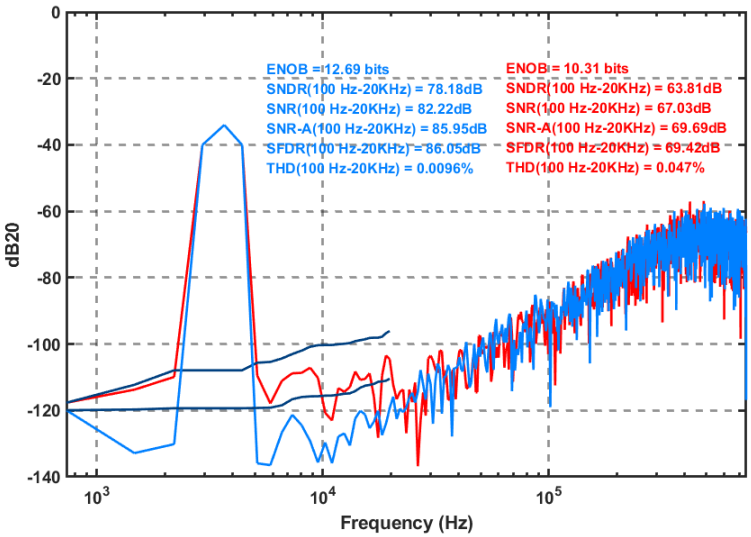

Figure 51 Output spectrum of PPD DSM operating at 1.5MHz at 1 Pa input. Blue line shows transient spectrum and red line shows transient noise spectrum.

Figure below shows the input vs SNDR for various input levels.

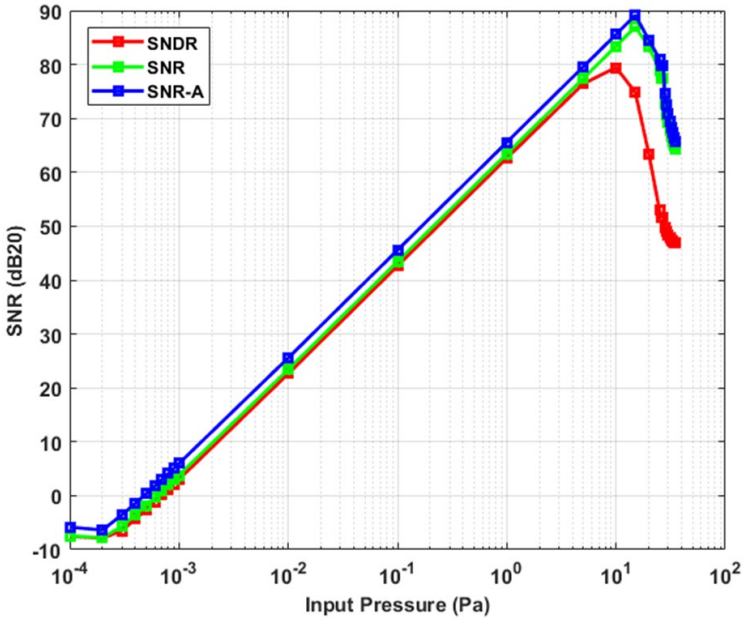

Figure 52 Input vs SNDR, SNR and SNR-A performance.

Figure below shows the power breakdown of the overall ADC.

1st Integrator	26uW
2nd Integrator	11uW
ASAR	14uW
Total	~51uW

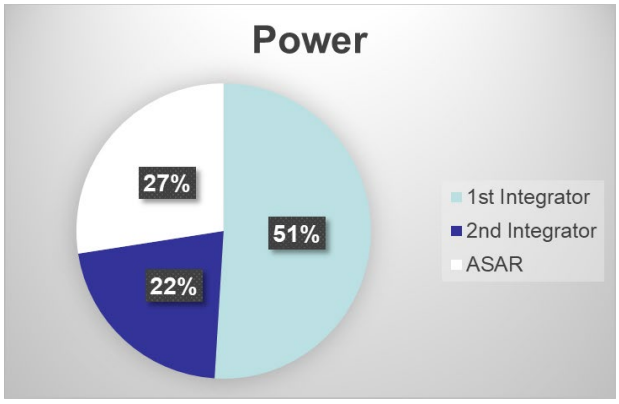

Figure 53 Power breakdown

Based on above simulation, given that peak SNDR is 90 dB, the Schreier Figure of Merit FoM_S is equal to 176 dB and considering dynamic range of 95 dB, the Figure of Merit based on dynamic range, FoM_{DR} is equal to 181 dB.

4. Part IIC: Novel system and circuit techniques

4.1 Predictive noise shaping SAR ADC

Since the early publication of a noise-shaping (NS) SAR ADC [50], there has been continued effort to optimize the noise transfer function (NTF) for achieving higher order noise shaping with lower power consumption. Many passive NS SAR ADCs have been proposed which doesn't require active amplifier and hence promises to reduce power consumption [51-53]. Techniques such as noise shaping using FIR filters have also been proposed [54]. Besides improving power efficiency by coming up with novel circuit techniques to implement noise shaping, there is a fundamental aspect of any oversampled converter that is not fully exploited yet. The oversampling feature of the NS SAR ADC requires that input signal bandwidth be limited to fs/(2×OSR). This may be achieved using an input anti-aliasing filter, or it may be guaranteed by the nature of the signal source. This means whenever there is over-sampling, the input signal doesn't change by more than certain amount sample to sample. This means there is no need to do full SAR conversion every cycle. In most noise shaping SAR ADCs, this trivial yet very powerful feature is not yet fully exploited. Allowing for local search within a certain range allows for segmenting the analog to digital conversion problem into two different problems, which can be solved differently. First problem is to come up with a range for each conversion using intelligent prediction algorithms, which can be done in digital domain more efficiently. Second is to perform finer analog to digital conversion within this range which still requires analog circuitry. In this era of rapidly advancing digital signal processing and machine learning, this segmentation can open up new possibilities for digitally assisted ADCs which can make better use of process scaling.

Therefore, it is proposed to use extrapolation (prediction) in the digital domain to determine a range for NS SAR operation such that it guarantees convergence. Since digital technology is now fast and inexpensive, even complex prediction algorithms can be easily implemented using digital logic. Once the range is determined, the SAR operation can limit its binary search within this range. To accommodate for thermal noise and other circuit non-idealities, the search range can be extended slightly, but it is never necessary to perform a full-scale SAR operation on each sample. Through theoretical analysis an equation for minimum number of bits that needs to be tested for guaranteed convergence is derived. Then the theoretical calculation is verified through extensive simulation[54]. Figure below shows the basic block diagram of the predictive noise shaping SAR ADC.

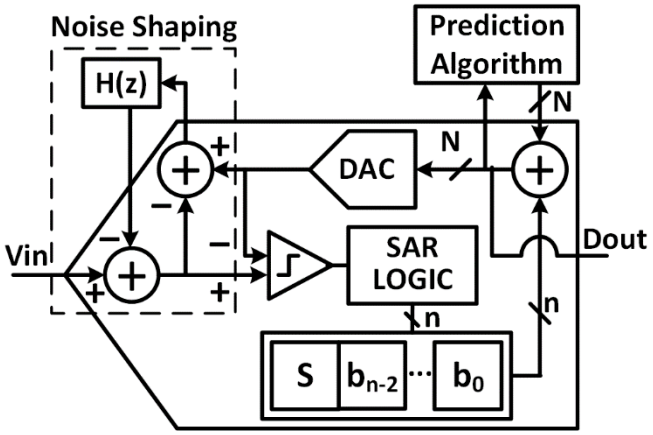

Figure 54 Simplified block diagram of predictive noise shaping SAR ADC

When such prediction is applied, the number of bits that need to tested can vary depending on activity and signal content. If the signal however is bandlimited due to input anti-aliasing filter or due to inherent bandwidth of input source, the number of bits that must be tested can be calculated. The worst case situation is when there is a first-order band-limiting filter preceding an ADC with a slow roll-off. Let the transfer function of such filter be:

$$H(s) = \frac{\omega_B}{s + \omega_B} \tag{29}$$

where $\omega_B = 2\pi f_B$ is the 3-dB bandwidth of the system. Then for a full-scale output of 1, the step response of the system will be given by:

$$v(t) = 1 - e^{-\omega_B t} \tag{30}$$

Since the step response has its largest rate of change at t=0, taking one sample at t = 0 and other at $t = 1/f_s$ gives the maximum possible change in signal from one sample to next sample. This maximum change in signal is given by:

$$\Delta v\big|_{\max} = 1 - e^{-2\pi \frac{f_B}{f_S}} \tag{31}$$

where f_s is the sampling frequency of the ADC. For an oversampled SAR ADC with an over-sampling ratio equal to OSR (= $f_s/2f_B$), this reduces eq (3) to:

$$\Delta v\big|_{\max} = 1 - e^{-\frac{\pi}{OSR}} \tag{32}$$

Therefore, the maximum number of bits that may change from sample to sample is given by:

$$N_{test} = \log_2\left(\Delta v\big|_{\max} \cdot 2^N\right) = N + \log_2\left(1 - e^{-\frac{\pi}{OSR}}\right) \tag{33}$$

where N is the resolution of the ADC. Using power series expansion of e^x, we can write

$$N_{test} = N + \log_2\left(\frac{\pi}{OSR} - \frac{1}{2}\left(\frac{\pi}{OSR}\right)^2 + \cdots\right) \tag{34}$$

Now in the case of moderate to large OSR (>32), including only first order term, the number of bits that must be tested is:

$$N_{test} = N + \log_2(\pi) - \log_2(OSR) \tag{35}$$

Hence for a band-limited signal in an oversampled SAR ADC there is no need for testing all bits every sample. For example, for N=12 and OSR=256, we only need to test the lower 6 bits. This is the case for zeroth order prediction, where the predicted value is simply the previous conversion result.

The prediction can be further improved using higher-order prediction algorithms. For example, first-order prediction can be easily implemented in the digital domain to estimate the slope of v(t), and account only for the rate of change of the slope (or second order derivative). Taking the first derivative of (30) gives:

$$\dot{v}(t) = \omega_B e^{-\omega_B t} \tag{36}$$

Finding how much slope can change from t = 0 to t = t_s and multiplying by $\Delta t = t_s$ gives the voltage range or possible error of the first-order prediction:

$$\Delta v(t)\big|_{\max} = \omega_B t_s\left(1 - e^{-\omega_B t_s}\right) \tag{37}$$

Using similar argument and approximations as in the zero-order case this results in:

$$N_{test} = N + 2 \cdot \log_2(\pi) - 2 \cdot \log_2(OSR) \tag{38}$$

In general, the number of bits that needs to be tested for M^{th}-order prediction is given by:

$$N_{test} = N + (M+1) \cdot \log_2\left(\frac{\pi}{OSR}\right) \tag{39}$$

Figure below shows the number of LSBs that need to be tested to obtain maximum SNDR (as that in the case without prediction) as a function of the OSR for various prediction order.

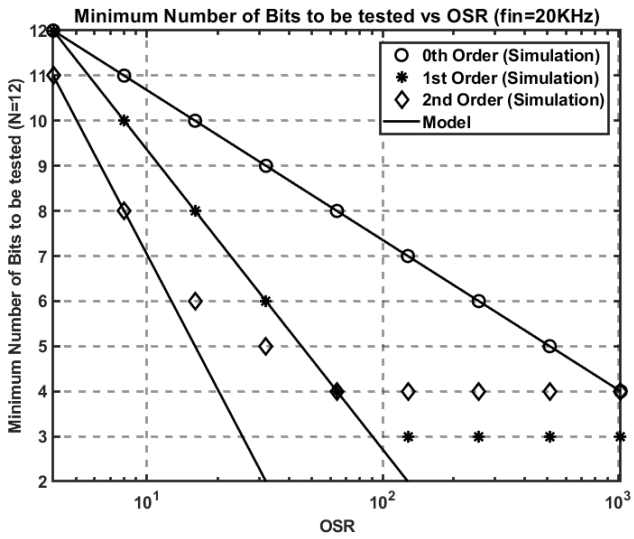

Figure 55 Model vs simulation for first order NS SAR

The markers indicate simulation results, and the lines represent the mathematical model (eqn. 39). It is shown that the model can accurately estimate the number of bits that must be tested when using zeroth-order and first-order predictor. For higher-order prediction algorithms, the number of bits required asymptotically reaches a certain minimum. As shown, using higher-order prediction algorithms, it is possible to reduce the number of bits needed to be tested significantly especially for smaller OSR. For example, for a second-order predictor, only 4 LSBs out of 12 bits is needed at an OSR of 32, which can save lot of power.

Using such approach, first order noise shaped SAR was designed and simulated, in particular, for DAC switching energy. Figure below shows the results of applying prediction to NS SAR and reduction in DAC switching energy by 70%.

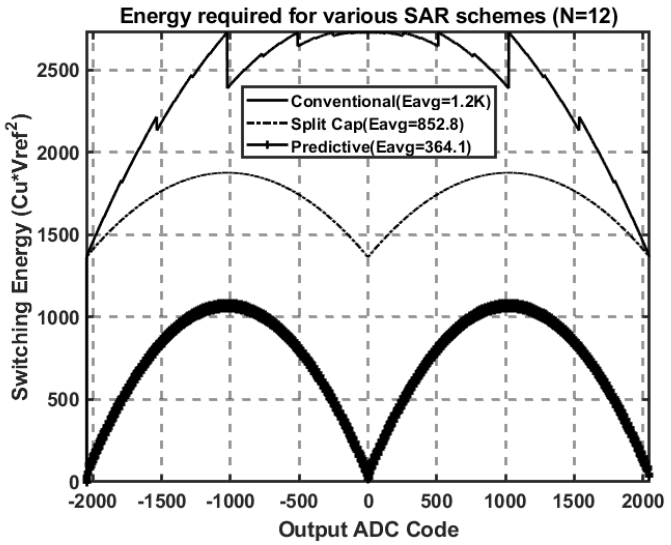

Figure 56 DAC switching energy plot for conventional SAR, split capacitor SAR and Predictive NS SAR

4.2 Efficient calibration of feedback DAC in ΣΔ ADC

In high dynamic range sigma delta ADCs, often multi-bit digital to analog converter (DAC) is used as feedback due to improved stability, lack of idle tones and inherent reduction in magnitude of quantization noise, which in turn results in reduction of non-linearity caused by non-linearity of operational amplifiers in the loop filters. However, due to mismatch in unit elements of the DAC, the overall DSM performance can be significantly reduced. Since DSM output and hence input to the DAC has both signal component as well as shaped quantization noise, harmonics of the signal component appear as well as noise floor increases. One of the most popular schemes to mitigate these effects due to DAC mismatch is Data Weighted Averaging (DWA) [56], which shapes the mismatch induced error by first or second order based on implementation. However, DWA requires keeping track of a pointer and additional element shuffling analog multiplexers and switches. Also delay in DWA hardware can increase excess loop delay causing stability issues. In addition, for higher resolution DACs, due to increasing complexity, implementation of DWA becomes challenging and dynamic power used by DWA starts to become significant. Another method often used is foreground calibration scheme, where sine wave input is applied [57], and filtered and decimated digital output is fitted to the applied sine wave to estimated DAC weights required to reproduce the input signal. Such calibration scheme however requires highly linear sine wave input with low enough noise floor. Laboratory equipment with such high linearity might not be readily available or can be corrupted by system noise when feeding in such input signal, which eventually reduces the accuracy of calibration and hence post calibration performance. An improvement was proposed in [58] where out of band non-sinusoidal excitation is used and system of linear equations is solved to reduce sum of in-band Fourier coefficients or total in-band quantization noise. However, it requires taking FFT of a very large data stream (220 point FFT as mentioned in the paper) to achieve required accuracy. This results in significantly longer calibration time. Also, if the DAC nonlinearity produces harmonics, these will be out-of-band and will not be considered in computing weights. Hence harmonic components of the non-linearity will not be corrected for when actual signal is applied. Alternatively, the calibration of DAC weights can be performed using digital calibration techniques such as proposed in [59] where the multi-bit DSM is reconfigured as single bit DSM to calibrate the weight of each DAC code. By adding a pair of switches and an adder, most significant bit (MSB) of the quantizer is directly used as feedback, while the feedback DAC is used as input to the DSM. The DAC is excited with each possible code (2B codes for B bit DAC) using a counter and then 2B×N bit lookup table is filled in using the filtered digital output. This requires additional analog hardware such as counter, adder and switches. Besides it also requires 2B+N clock cycles where N is the bit precision of look-up table and also calibration accuracy. An improvement was proposed in [60], where only the deviation from ideal value of the DAC code is stored and hence storage memory requirement could be reduced for the same calibration accuracy. However, the lookup table still stores correction values for each possible DAC code, which is unnecessary and significantly increases

calibration time and memory requirement. Yet another method was proposed in [61], where each DAC element is sequentially removed, and the average of the digital output is used to solve for contribution of each element using system of linear equations. However, this requires complicated digital hardware, including dividers and requires storing calibrated weights for each DAC element, which will require significant memory for higher resolution DACs.

Therefore, a new efficient calibration scheme was invented [62], which neither requires additional analog hardware, nor precise input signal or reconfiguration of the DSM for calibration. It only requires B×N bit storage for B bit DAC (and N bit calibration accuracy) and corrects for mismatch induced increase in noise floor as well as harmonics. The principle of the proposed scheme is simple. We assume that the DSM uses a binary-weighted DAC, whose output (X) is given by:

$$X = \mathbf{W_I} \bullet \mathbf{V} = \sum_{i=0}^{B-1} w_i b_i \qquad (40)$$

Here $\mathbf{W_I}$ is the ideal weights vector whose elements are w_i, $\mathbf{V}$ is the output of DSM whose elements are b_i. Let us also define the actual weights vector $\mathbf{W_A}$ whose elements are $w_{A,i}$ and calibrated weights vector $\mathbf{W_C}$ whose elements are $w_{C,i}$ where $i = 0..B-1$. Consider normalizing all the weights by MSB weight such that the weights are:

$$\begin{aligned} \mathbf{W_I} &= \left[\frac{1}{2} \quad \frac{1}{4} \quad \ldots. \quad \frac{1}{2^{-B}}\right] \\ \mathbf{W_A} &= \left[\frac{1}{2} \quad w_{A,B-2} \quad \ldots. \quad w_{A,0}\right] \\ \mathbf{W_C} &= \left[\frac{1}{2} \quad w_{C,B-2} \quad \ldots. \quad w_{C,0}\right] \end{aligned} \qquad (41)$$

The weights are ideally $\mathbf{W_I}$, but mismatches change their values to $\mathbf{W_A}$. This introduces nonlinear distortion and heightened noise floor in the output spectrum. The problem can be solved by introducing a digital look-up table (LUT) at the output of the DSM with calibrated weights $\mathbf{W_C}$ as shown in Figure below:

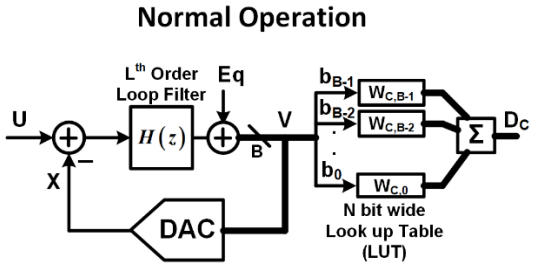

Figure 57 Normal operation after calibration using LUT

The LUT now will have the same (limited only by calibration accuracy) input-output characteristics as the DAC. Since it also has the same input word $\mathbf{V}$ as the DAC, it must have the output $D_C = \mathbf{W_c} \bullet \mathbf{V}$. Since the DAC output is forced by the feedback loop to track the ADC input U in the signal band, the output of the LUT will be an undistorted digital equivalent of the analog input U.

The problem is thus reduced to finding the digital replicas of the DAC weights w_i. The proposed calibration scheme to determine the weights of the DAC is as shown in Figure below.

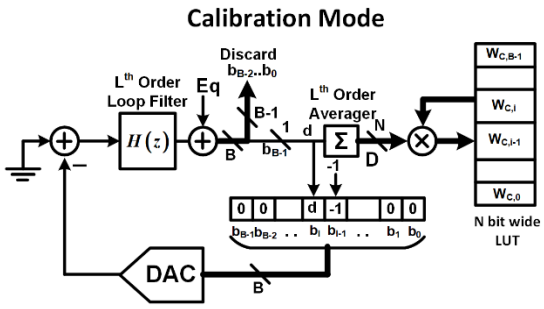

Figure 58 Efficient calibration of feedback DAC

The proposed calibration scheme can be briefly summarized as below.

1. Accept the MSB weight $w_{C,B-1}$ as ½; set U = 0; disable all DAC input except $(B-1)^{th}$ input and $(B-2)^{th}$ input and reset all integrators and accumulators.
2. Calibrate $w_{A,B-2}$ by feeding back in every clock period $d \times w_{A,B-1} - w_{A,B-2}$, where d is MSB of the ADC output. Repeat for $M = 2^N$ cycles where $M >> 1$.
3. The DC value of $d \times w_{A,B-1} - w_{A,B-2}$ will be forced to 0 by the DSM loop, so $w_{C,B-2} = ½ \sum d(n)/M$.

Next, the process is repeated with $(B-2)^{th}$ input (whose weight is now known) playing the role of feedback and $(B-3)^{th}$ bit as input. This gives an estimate of $w_{A,B-3}$. After B-1 such cycles, all $w_{C,i}$ will have been found, and deposited in the LUT. And during normal operation these values in the LUT can be used for mismatch correction. A detailed mathematical derivation can be found in [62].

To illustrate the efficacy of the proposed scheme, Figure below is plotted with comparison to DWA technique.

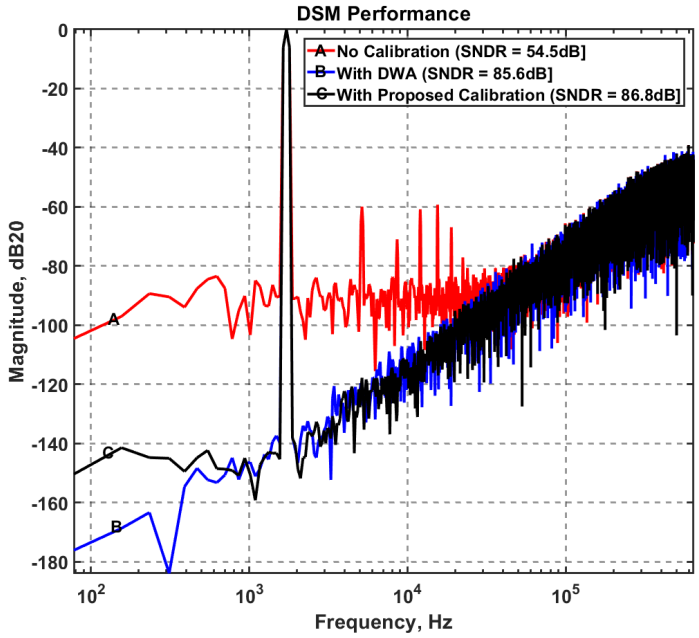

Figure 59 FFT Spectrum of DSM output. Spectrum A is without calibration or correction. Spectrum B is with DWA applied. Spectrum C is with proposed Calibration technique applied (500 cycles per bit)

Based on above results, it can be seen that the proposed calibration scheme corrects for mismatch related increase in noise floor as well as harmonics to the same degree as that can be done with DWA without requiring additional analog hardware.

4.3 Highly linear boosted sampling switch

The input sampling switch is a crucial circuit element in analog to digital converters (ADC) and switched capacitor circuits. It limits the overall system linearity. The major sources of non-linearity (in the order of significance) are signal dependent charge injection, signal dependent charge draw, and signal dependent clock feed-through. The signal dependent charge draw is identified as a key source of error in this research.

The signal dependent charge injection is mainly attributed to the carriers injected from the main transistor's channel when it is turned off. In previously published boosted switches, this problem was mostly resolved using clock boosting technique [63], which ensured that channel charge is independent of signal level by boosting the clock voltage referenced to the input signal itself. Several such boosted switches have been published which solve the problem of signal dependent charge injection [64-67]. These switches perform well in reducing the nonlinearity due to signal dependent charge injection. However, if the source has non-zero resistance, the performance is degraded due to charge drawn from the sampling capacitor during cut-off. To provide a low-impedance source for the input v_{in}, analog to digital converters (ADC) are often preceded by input drivers, which consume significant power. Also, when interfacing with a high impedance sensor, often a buffer is used in order to attain low source impedance. These additional circuit blocks add noise and consume additional power. This research proposes a sampling switch for which linearity does not depend on the input source impedance and hence eliminates need for high power and highly linear buffers in the signal path [68]. Figure below shows the schematic of the proposed boosted switch and the buffer.

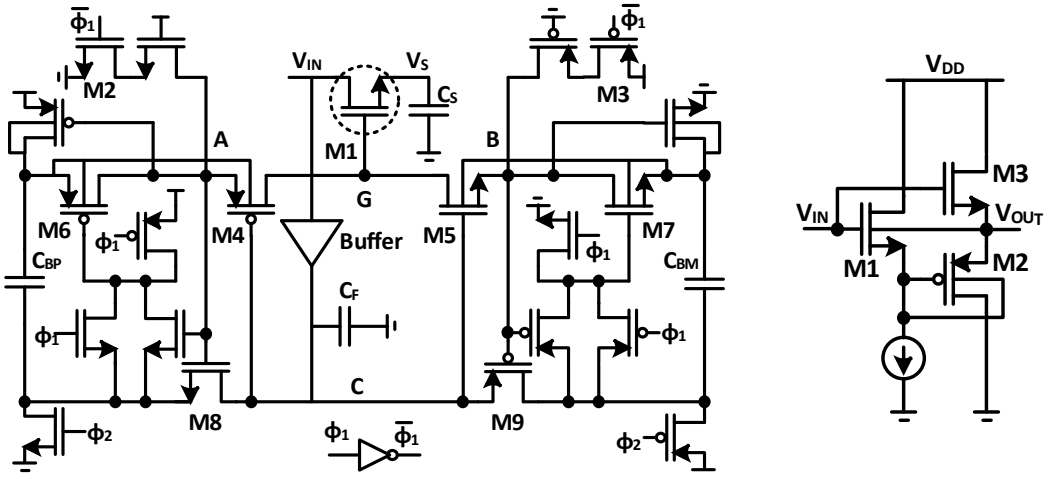

Figure 60 Schematic of the proposed boosted switch and the buffer

In order address the nonlinear errors mentioned in the previous paragraph, a complementary boosting technique is introduced, and a buffer is added to drive the boosted switch so that the glitching due to charge draw doesn't affect the sampled voltage. The switch circuit consists of two complementary half circuits. The left half is used to set the voltage at the gate (G) of the main transistor M1 to $V_{IN}+V_{DD,}$ and the right half of the circuit is used to drive it to $V_{IN}-V_{DD}$. Since the gate is driven below ground GND, a low-threshold transistor can now be used as main switch, which further improves its on-resistance. In contrast to conventional boosted sampling switches, there is no explicit pull-down transistors to drive the gate (G) to ground. Instead, the negative terminal of a complementary half circuit's capacitor C_{BM} is connected to the gate, and the positive terminal is connected to the input. This drives the gate voltage low without needing explicit pull-down transistors. Since the buffer is only used to drive the boosted switch and since it is not in the signal path, it is not required to be highly linear or low noise. Adding such buffer in the sampling switch allows for reducing power of the input buffer or completely eliminating it without degrading linearity. The buffer can be low power, such as the buffer in the presented implementation only consumes 560 nA of static current. The buffer was only 63 dB linear at 2V amplitude whereas the sampling switch is more than 100 dB linear. Furthermore, the buffer may be replaced by a resistor in cases where rail to rail operation is desired. The addition of the buffer obviates need for highly linear and possibly high power (due to noise considerations) input driver in the signal path.

The proposed boosted sampling switch was designed in a TSMC 65 nm CMOS process for validation. The sampling capacitor was chosen to be 1 pF, the sampling frequency was 10 MHz and input signal was 100 kHz. The boosting capacitors C_{BP} and C_{BM} were 500 fF each. The filtering capacitor C_F was 25 fF. The buffer was sized so that total static current was 560nA. All transistors were chosen as 2.5V IO devices. All of them (except M1, M5, M7 and M9) were minimum size devices with W/L = 400nm/280nm. W/L for M1 was 2um/280nm, for M5 and M7 it was 1um/280nm and for M9 it was 2um/280nm.

Figure below shows the 3rd order non-linearity of the sampled voltages for when input source resistance is varied.

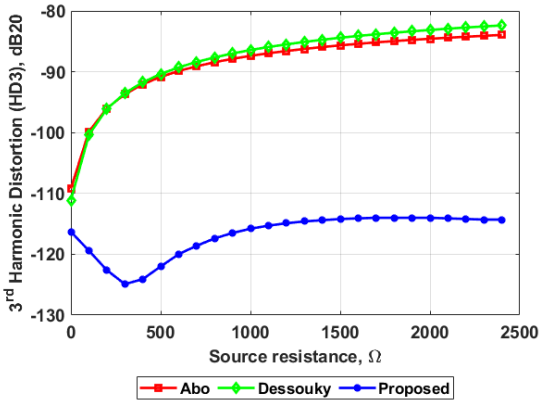

Figure 61 HD3 for Rs for proposed switch in comparison with Ref [63] and Ref [64]

As can be seen in the simulation result, the boosted switches from [63] and [64] suffers from signal dependent charge draw and hence performance is highly reduced for even small input resistances. Whereas the proposed boosted switch more than 100dB linear across various input resistances and is independent of input source resistance. A similar simulation was performed by varying the sampling frequency and hence oversampling ratio (OSR). Figure below shows the results of such simulation.

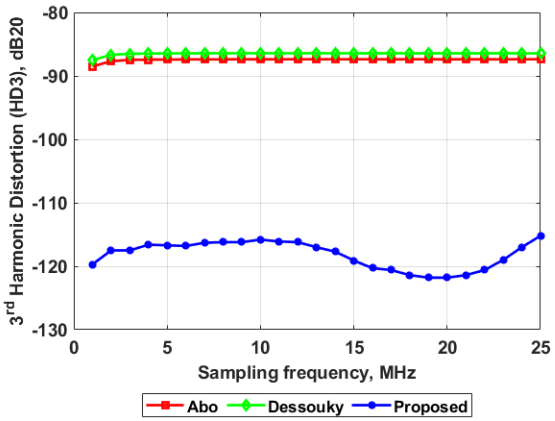

Figure 62 HD3 vs fs for proposed switch in comparison with prior switches

The simulation was performed with input source resistance of 1 kΩ and it is shown here that the problem of input dependent charge draw is independent of sampling frequency and is a consistent problem for which the proposed boosted switch always works, even up to high sampling rate. Furthermore, the proposed switch was simulated for various input amplitude and figure below is plotted to show the results of such simulation.

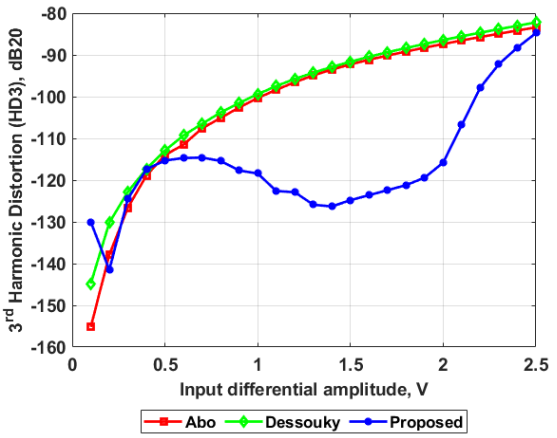

Figure 63 HD3 vs input amplitude in comparison with prior switches

As is shown in the figure above, the proposed boosted switch works well up to input amplitude of 2V differential, when the supply voltage is 2.5V. Beyond 2V, the non-linearity of the buffer starts to dominate the performance as the buffer can only swing between $V_{DSAT}+V_{TH,LVT}$ to $V_{DD}-V_{DSAT}$ and hence the signal starts to clip. When such rail to rail operation is desired, a resistor in place of buffer may be

used to partially remedy the problem with signal dependent charge draw. But since there is always going to be some charge drawn from the input, the performance improvement is lowered. Figure below shows the input amplitude vs HD3 for such configuration.

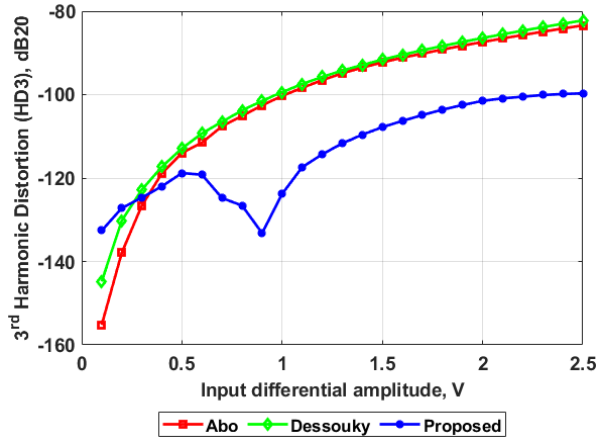

Figure 64 HD3 vs input amplitude for proposed switch with buffer replaced by 1 kΩ resistor

In above simulation a 1 kΩ resistor was used in place of the buffer and the filtering capacitor C_F was changed from 25 fF to 1pF. As can be seen, the proposed switch is 100 dB linear up to 2.5 V input amplitude and is at least 15 dB better than switches proposed in [63] and [64].

4.4 Push-pull source follower circuit

A source follower buffer is an important circuit element in many analog designs. The basic source follower however is limited in its performance (in terms of linearity) due to asymmetric sourcing and sinking current. For example, an NMOS source follower can have large sourcing current hence being able to follow the input on rising edge, while it has constant sinking current due to constant current bias and hence not being able to follow the input on falling edge. Such asymmetric rise time and fall time causes harmonic distortion similar to that in slew rate limited operational amplifiers. Some of this effect is mitigated in the super source follower topology since during falling edge, the PMOS device (M2 in Figure below) will be turned off, allowing for full bias current to discharge the output node. A better alternative was proposed in [69], where a NMOS device is diode connected to the drain of the main transistor such that it allows for complete push-pull operation. However, this significantly limits the allowed voltage swing at the output since output cannot go beyond V_{GS} of the NMOS device and hence clips the signal. To remedy such limitations, a push-pull source follower topology is proposed, in which the voltage swing at the output can be from V_{DSAT} to V_{DD}-I_BR_S, where R_S is chosen such that I_BR_S is close to 100-200 mV. This allows for almost rail to rail operation and push-pull driving capability. Figure below shows the typical source follower, super source follower, flipped source follower and proposed push-pull source follower.

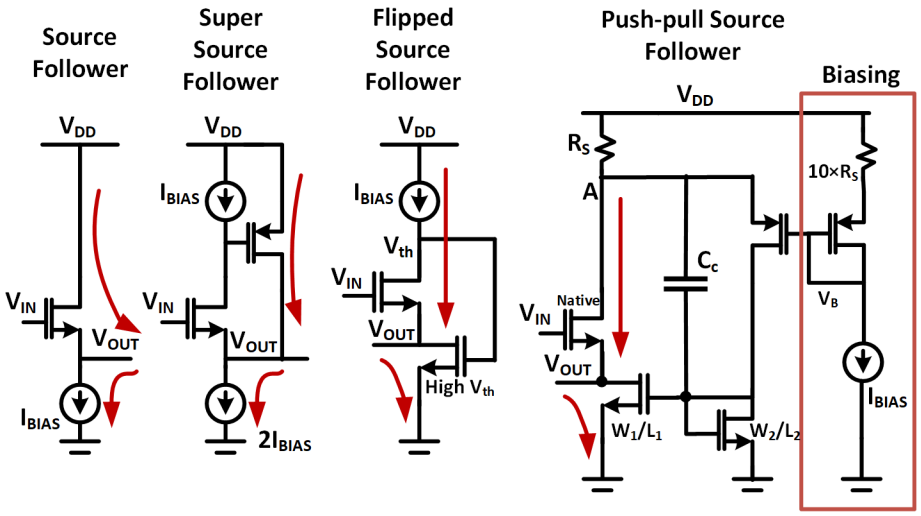

Figure 65 Schematic of source follower, super source follower, flipped source follower and push-pull source follower. Red arrows indicate charging and discharging currents.

The push-pull source follower was implemented in TSMC 65 nm process for operating at 2.5V supply. The W_1/L_1 was 2.4um/100nm, W_2/L_2 was 120nm/1um, R_S was 100 kΩ and current in the main branch for all designs were roughly equal to 1 µA. The feedforward capacitor C_C was 500 fF. The designs were compared with 1 MHz input signal driving 1 pF load capacitor, while varying input amplitude. Figure below shows the results of the simulation.

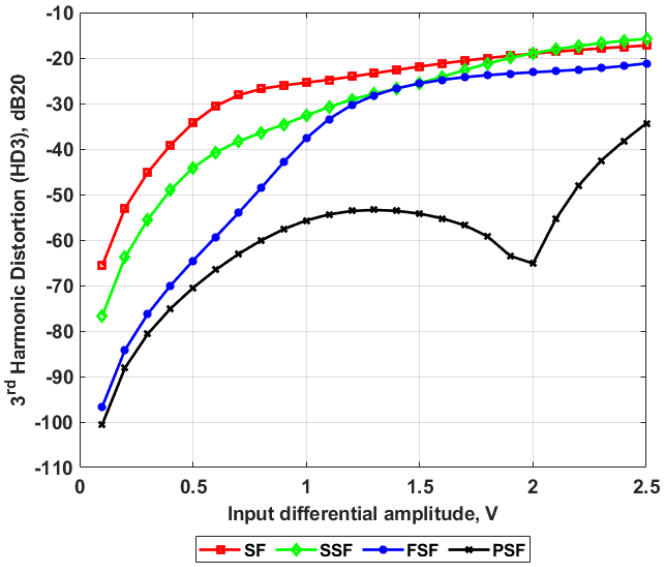

Figure 66 HD3 vs input amplitude for various buffer topologies. SF = source follower, SSF = super source follower, FSF = flipped source follower and PSF = push-pull source follower

As expected to due to large voltage swing capability and large charging and discharging currents, the push-pull source follower is more linear than other conventional source follower, especially at higher amplitude.

4.5 Novel flicker noise cancellation scheme

The flicker noise is one of the concern for low frequency and high dynamic range circuits. It is often mitigated by either using chopping or auto-zeroing. While using chopping technique, the input is upconverted before adding device noise and hence input and device noise are separated in frequency domain. Now by down-converting by chopping again at the output of a circuit block, the input signal is brought back to baseband and flicker noise is upconverted. However, the circuit block now needs to be drive by low impedance source since the chopping introduces switched capacitor leakage path at the input. In addition, due to chopping artifacts such as glitches, when chopping is applied to continuous time signals, the output starts to show higher distortion components. Similarly, auto-zeroing also requires that input be driven by low impedance source, and it further requires additional auto-zeroing phase in which input is not processed. Furthermore, applying auto-zeroing automatically requires signal to be discrete time and hence is not applicable for continuous time signal processing. An interesting technique was proposed and validated in [70], where the input devices were periodically switched from depletion to accumulation to reset the trap states. However, doing so requires switches at the input, which has similar disadvantages as described before when high impedance input is desired.

In order to address these issues, especially the fact that input needs to be driven, a novel flicker noise cancellation technique was devised in which input impedance into the block is very high lending to direct connection with high impedance sensors. This obviates need for buffers often used between sensors and a signal processing circuit block. In order to suppress the flicker noise, the circuit block is biased such that in one phase the transconductance is positive, while in other phase the transconductance is negative. For example, if the circuit block is a transconductance amplifier, the effective G_m is switched from $+G_m$ to $-G_m$ periodically. The proposed technique when applied to transconductance amplifier is shown in figure below.

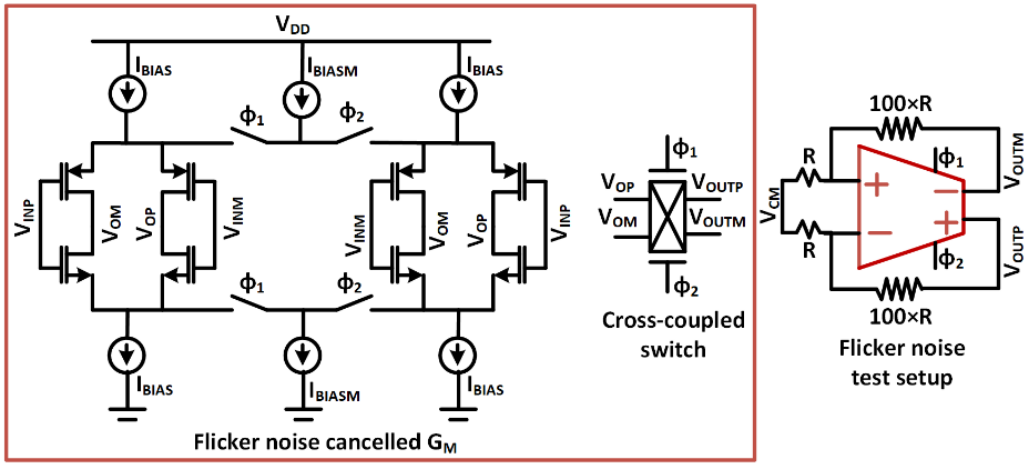

Figure 67 Proposed flicker noise cancellation scheme applied to a transconductance amplifier and test setup

In doing so the output current is upconverted as it passes through the circuit block. In terms of flicker noise, however, since flicker noise is a slow process, it is expected that it only responds to the low frequency or average value of the current. This hypothesis cannot be verified in simulation, as in circuit models, flicker noise PSD is modeled in a way that it instantaneously changes based on bias current. Such static flicker noise model is unable to simulate the dynamic nature of the flicker noise process. Hence this scheme is being planned for verifying in Silicon by tapeout a test chip in future projects.

The scheme was simulated in transient noise analysis by implementing the flicker noise cancelled Gm in TSMC 65 nm process. Figure below shows the simulation results without any cancellation, with chopping and with proposed scheme.

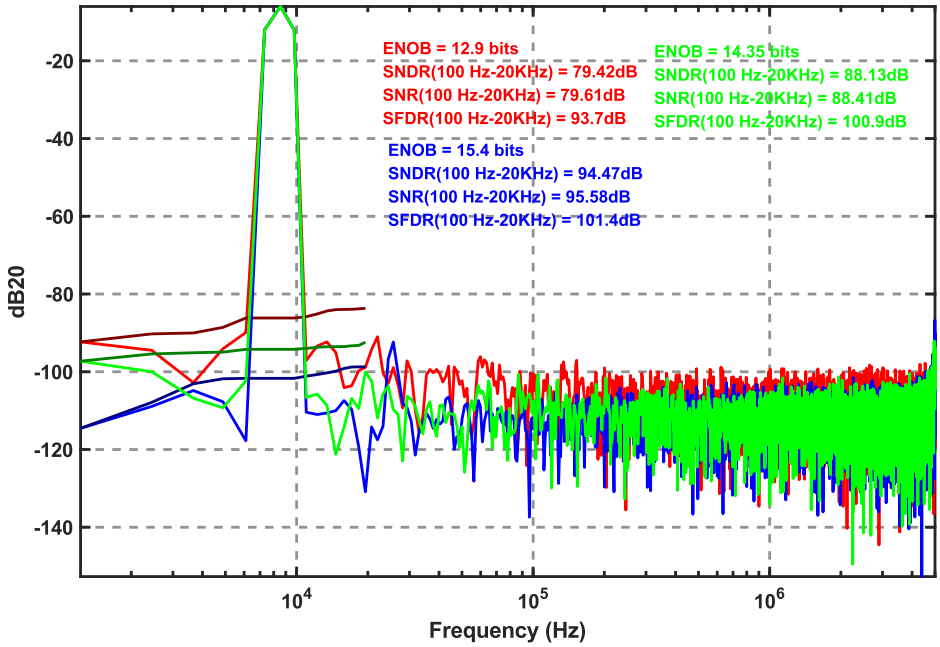

Figure 68 Simulation results for flicker noise cancellation scheme. Red spectrum without any cancellation, blue spectrum with chopping and green spectrum with proposed scheme.

Based on the simulation, the flicker is reduced completely when chopping is applied. However as seen in the figure (blue curve), third harmonic appears a consequence of chopping artifacts. The performance for proposed scheme shows intermediate results. It shows some fraction of flicker is cancelled however some of it is still present. It is hypothesized that this partial cancellation is simulation is due to the way flicker is modeled as described before. Albeit even partial cancellation can reduce the flicker noise by a significant factor and might be an interesting chopper-less flicker noise cancellation scheme useful when directly interfacing with higher impedance sensors.

5. Conclusion

In this dissertation, various research projects were investigated and implemented to demonstrate novel ideas and innovations and their advantages. In Part I, Plasmonic color filter array based visible light spectroscopy was demonstrated. The research included theoretical analysis, device simulation, fabrication, testing and algorithm development. This research for the first time to my knowledge demonstrates end-to-end design and use of plasmonic grating filter with slab waveguide for the purpose of spectroscopy in visible range. A novel unmixing algorithm was presented and a smoothing regularization was used to reconstruct sample spectrum from sub-sampled data. Furthermore, a novel technique for suppressing Rayleigh Anomaly was also presented with extensive simulation results.

In Part IIA, a high speed data converter using pipelined SAR architecture was investigated and a thorough design was presented with extensive simulation results. The proposed design is expected to perform better when design specification is such that it is not limited by thermal noise. In such cases, the switching for conventional pipelined ADC to pipelined SAR ADC has benefits of being opamp-less and hence able to run faster in the same process node. The design was implemented and simulated at chip level in 65 nm process.

In Part IIB, a pseudo-pseudo differential sigma delta ADC was investigated for use in audio application. Based on such architecture, the design showed no effect of flicker noise, albeit there was no chopping or correlated double sampling applied. The design was power efficient and achieves dynamic range of 95 dB with FoM of 181 dB.

In Part IIC, various system and circuit techniques were invented to mitigate issues and challenges in analog to digital converter design. One of the novel ideas included predictive noise shaping ADC, which allows for predicting some of the output bits, when the ADC is oversampling ADC. Such technique has promise to reduce power and was demonstrated through simulation that at least 70% power reduction in DAC switching energy is possible using such predictive SAR approach. Secondly an efficient calibration scheme for the feedback DAC used in sigma delta ADCs was invented and the design was thoroughly verified to perform as good as DWA technique, without requiring additional analog hardware. Furthermore, a novel high-linearity complementary boosted switch was conceptualized, and the design was simulated and was verified to perform at least 20 dB better than prior publications in terms of linearity. Yet another novel circuit technique of using push-pull structure for source follower was presented and design verified through simulation to overperform conventional source follower structures. Lastly, another novel circuit technique was presented for mitigating effects of flicker noise. Using such technique, flicker noise cancellation was simulated and shown that partial cancellation of flicker noise was feasible. This work allows for direct connection of any high impedance sensors to circuit front-end without need for high power buffers and other interface circuits.

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