AN ABSTRACT OF THE THESIS OF

Bohui Xiao for the degree of Master of Science in Electrical and Computer Engineering presented on November 26, 2018.

Title: A 1V 40mA Fast Transient Capless LDO with 7uA Quiescent Current in 180nm CMOS using Ring Amplifier with Adaptive Damping

Abstract approved:

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Un-Ku Moon

Ring amplification has emerged as an efficient technique to drive large capacitive loads in switched capacitor circuits. We propose circuit techniques to demonstrate the first application of a ring amplifier in a non-capacitive feedback system of a LDO. These techniques enable a simple cap-less LDO structure in 180nm CMOS that can achieve less than 700ns settling time for load transitions between 100uA-40mA with a quiescent current of 6.5uA while regulating a 1V output with a 80mV drop out voltage.

A 1V 40mA Fast Transient Capless LDO with 7uA Quiescent Current in 180nm CMOS using Ring Amplifier with Adaptive Damping

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Bohui Xiao

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Head of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

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Bohui Xiao, Author

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CHAPTER 1. INTRODUCTION

Modern day SOCs require multiple power domains within a system which demands for area and power efficient on-chip Low-Dropout (LDO) regulator. There are two types of LDOs which are Analog LDOs and Digital LDOs. Analog LDOs using an error amplifier to control a large power transistor in the feedback loop. They require large quiescent current for fast transient response [1, 2] and large area for compensation capacitor. Also, the Power Supply Rejection Ratio is better in Analog LDOs comparing to Digital LDOs. Digital LDOs is using some digital cell and a simple ADC (usually just simple comparators) to control how many unit power transistor is on or off. They offer low power consumption but control circuits increase circuit complexity [3, 4]. Also due to the ADC accuracy, Digital LDOs suffer from poor output accuracy. In this work a ring amplifier (ring amp) based capacitor-less analog LDO is proposed to achieve fast transient response with low quiescent current while offering an area efficient and scalable LDO structure.

In the Analog LDOs, there are also 2 types: Output Capacitor loaded or Output Capacitor-less LDO. In the Capacitor loaded LDO, the dominant pole is located at output with a large capacitor loaded. This capacitor is taking a lot of area if it is on chip. In conventional capless LDOs, the dominant pole is usually provide either in error amplifier or directly at gate of the power transistor. Large changes in load currents require opamps to have large gain-bandwidths to achieve faster settling time. This results in very high static power consumption. Due to the large pass transistor size, the non-dominant pole is also a problem. Alternate solutions exist which include additional dynamic biasing and compensation circuits to speed up the

opamp. However, the additional circuitry significantly adds to the complexity of the amplifier design.

Over the recent years, Ring amplification has emerged as a scalable and power efficient amplifier technique to drive large capacitive loads in switched capacitor systems such as ADCs [5-7]. The slew based charging and dynamic operation of ring amps result in a fast transient response with very low power consumption compared to conventional opamps. Because of the inherent dynamic operation and inverter based topology of the ring amplifier, the Ring amplifier based LDO can achieve faster settling time with low power consumption and a simple structure.

This work aims to utilize the properties of ring amp to drive the large gate capacitance of the pass transistor in an analog LDO. However, ring amp techniques pose challenges when used in a non-capacitive feedback system of an LDO due to the limited stable operating region of the amplifier. In this work, a capacitor less compensation technique for ring amps is proposed which adapts the ring amp output stage for an LDO's feedback system. Using this technique, a ring amp based capacitor less LDO is demonstrated in 180nm CMOS that achieves <700ns settling time for load transitions between 100uA-40mA with a quiescent current of only 6.5uA, while regulating at 1V output with 80mV dropout voltage.

CHAPTER 2. RING AMPLIFIER

Ring amplifier has been implemented with variety architectures since it introduced. The high slew capability and dynamic behavior of ring amplifier is good candidate for the lower power analog design. However, all of the ring amplifiers implemented so far are only used in Analog to Digital Converter (ADC) designs, especially in Multiplying Digital to Analog Converter (MDAC). Those are discrete time systems. LDO is a continuous behavior circuit. In order to design ring amplifier in the LDO circuit, first thing is deciding the best topology. In this Chapter, Ring amplifier will be discussed. And different structure will be explained. Then, in order to illustrate the operation of the Ring amplifier, a switch capacitor circuit with ring amplifier will be discussed. After that, the operation of the ring amplifier in the LDO circuit will be explained.

2.1 Ring Amplifier Structure and Analysis

Ring amplifier is usually implemented with three inverter stages. The Figure 2.1 shows the basic structure of the ring amplifier. First couple stages are usually just a gain stage and the third stage is a “class AB” structures. While ring amplifier can have different forms, the last stage is a consistent feature. The output stage is always implemented with class AB architecture. The PMOS and NMOS transistors are biased into a sub-threshold condition which is defined as the "deadzone".

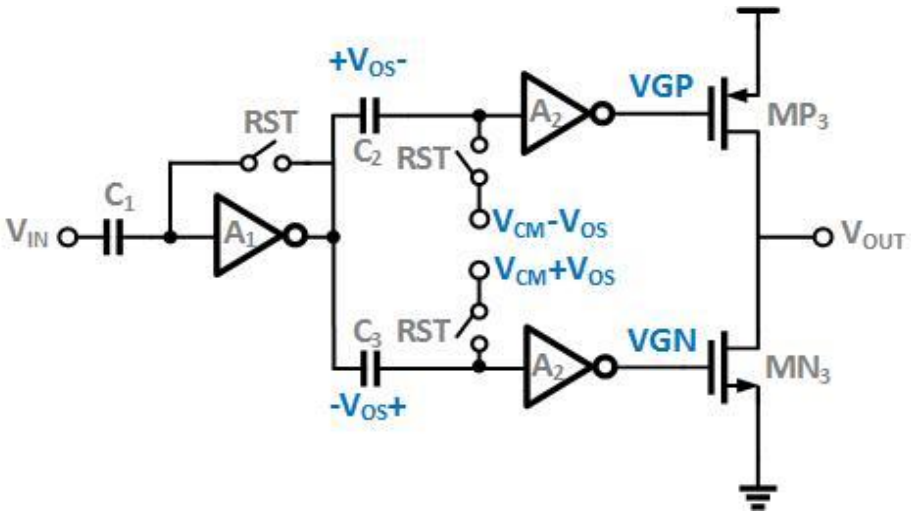

Figure 2.1. Basic Ring Amplifier Structure

Furthermore, the signal and bias are shared at same node at gate of output transistor (MP_3 and MN_3). Ring amplifiers are able to achieve high gain with the multistage structure. The dynamic behavior of the class AB structure makes settling much faster. From small signal perspective, ring amplifier place the dominant pole at the output node because the output stage transistors are biased at low transconductance state.

Just evaluating the small signal of the ring amplifier is not enough to determine the stability of the amplifier. The small-signal approximations are only accurate when each node is close to its steady state value. Since the gate voltage VGP and VGN contain both signal and bias voltage, during the initial parts of the amplification, the bandwidth of the ring amplifier increases due to large current in the output stage. The large signal delay from each stage and output load makes the output stage never get into stable region.

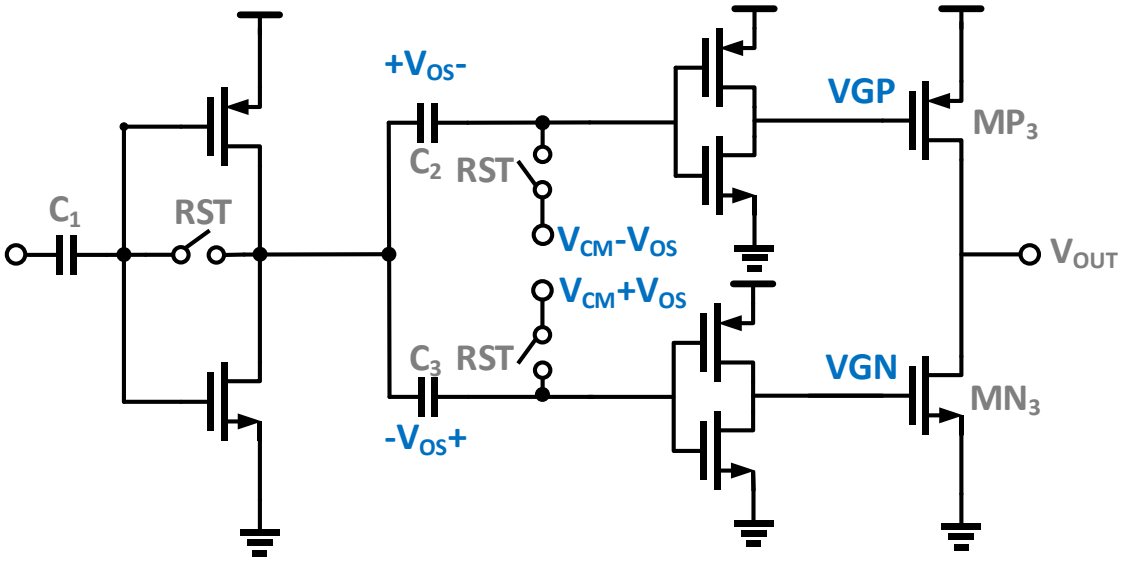

Figure 2.2. Ring Amplifier with Capacitor Level Shifter Architecture [5]

In order to bias the output stage into sub-threshold region, many approaches were implemented before. In Figure 2.2. Ring amplifier uses capacitor for level shifting for biasing output transistor. As seen in Figure 2.2, this architecture sets the voltages VGP and VGN such that the output stage transistors are biased in sub-threshold region. The first 2 stages are just gain stages. By resetting switch, a given voltage is stored in the C_2 and C_3. This Vos biases the gate of the output stage into sub-threshold region.

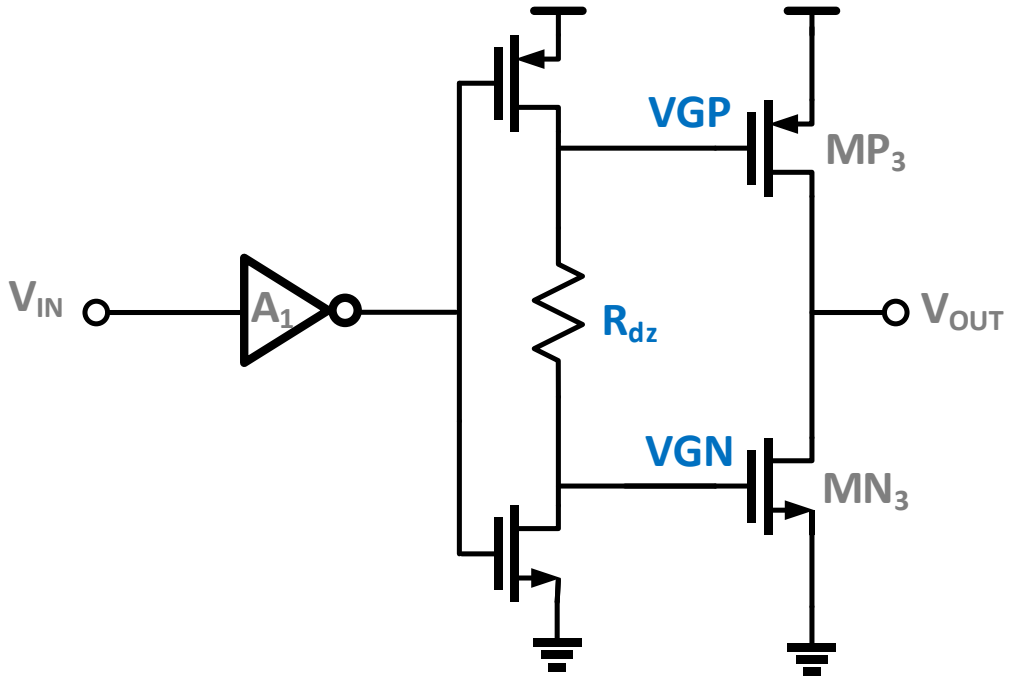

Figure 2.3. Ring Amplifier with Resistor Biased Architecture

Another type of the biasing technique is proposed. In [6], as shown in Figure 2.3, a resistor is added in between PMOS and NMOS of the second stage. By adjusting the resistor value, voltages VGP and VGN can be set to a desire value. This structure does not require a clock. However, it reduces the slew capability of the ring amplifier. The gate voltage of the output stage is not be able to fully turn off or on. A voltage boundary is created by the resistor.

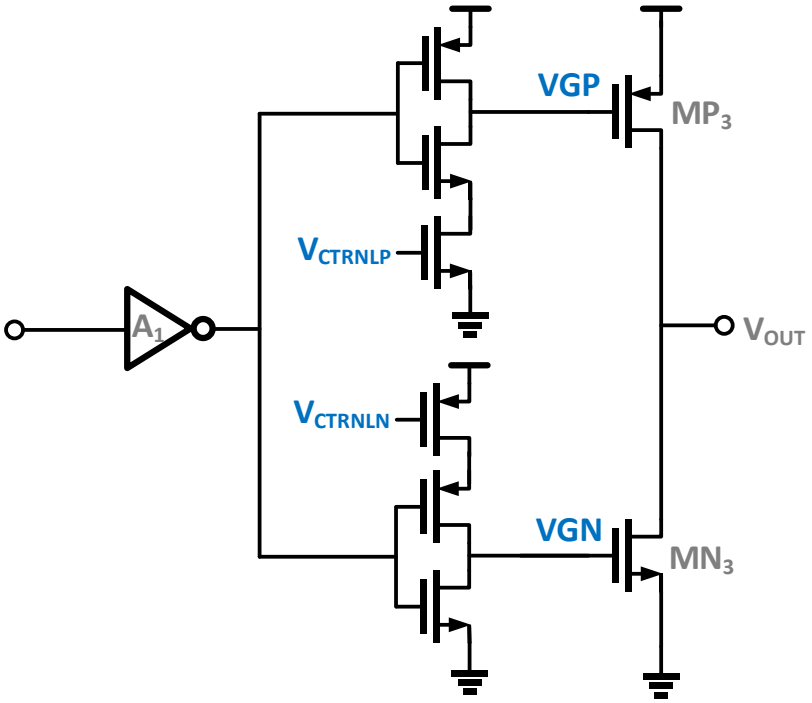

Figure 2.4. Ring Amplifier with Current-Starved Inverter (CSI) Architecture

In [7], a current-starved inverter (CSI) ring amplifier is proposed. As shown in Figure 2.4, the second stage is implemented with current-starved inverters. By adjusting V_{CTRLN} and V_{CTRLP}, in the steady state, voltages VGP and VGN are set to desired voltage. This structure does not require any clock and it keeps the advantage of the slewing of the inverter structures.

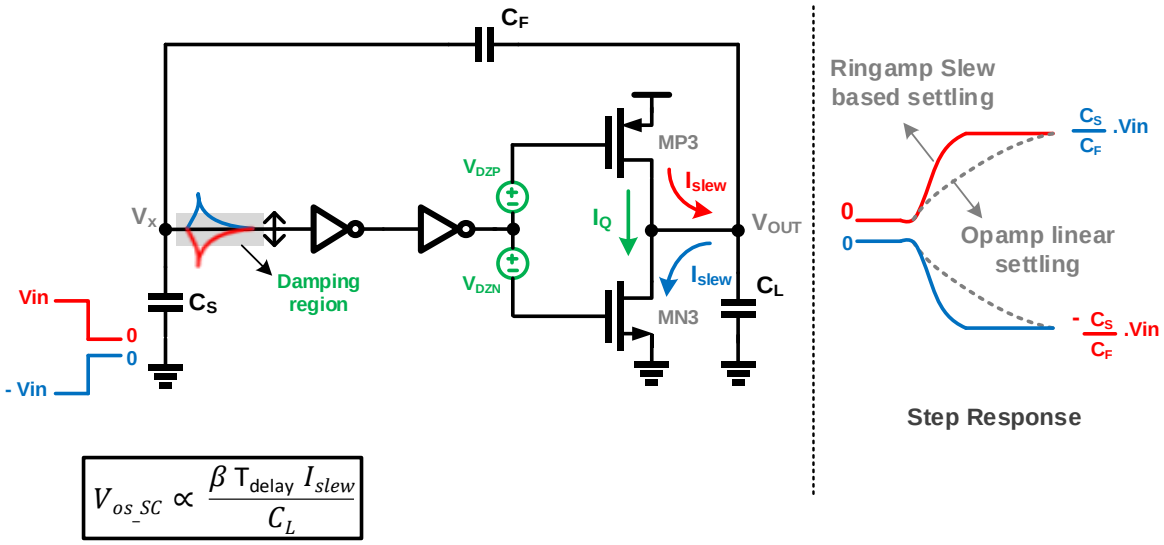

Figure 2.5. Ring Amplifier Operation in Switched Capacitor Feedback Circuits

2.2 Ring Amplifier operation in Switch Capacitor circuit

As mentioned before, small signal is not enough to analysis ring amplifier. It is therefore necessary to understand the transient response of the ring amplifier. In Figure 2.5, Ring Amplifier Operation in Switched Capacitor Feedback Circuits is presented. During the steady state operation, the dominant pole at the output of the ring amp is set by the deadzone voltage, that results in a low output stage quiescent current I_Q. During the event of a step input in a switched capacitor network, the disturbance at the input of the amplifier is amplified by the first two stages, resulting in a large slewing current I_{slew} that facilitates faster charging of the load capacitor. As the capacitor voltage approaches the steady state value, the amplifier returns to its quiescent current mode resulting in a very low power consumption. The deadzone voltage of the ring amp creates a range of input voltage (damping range) for which

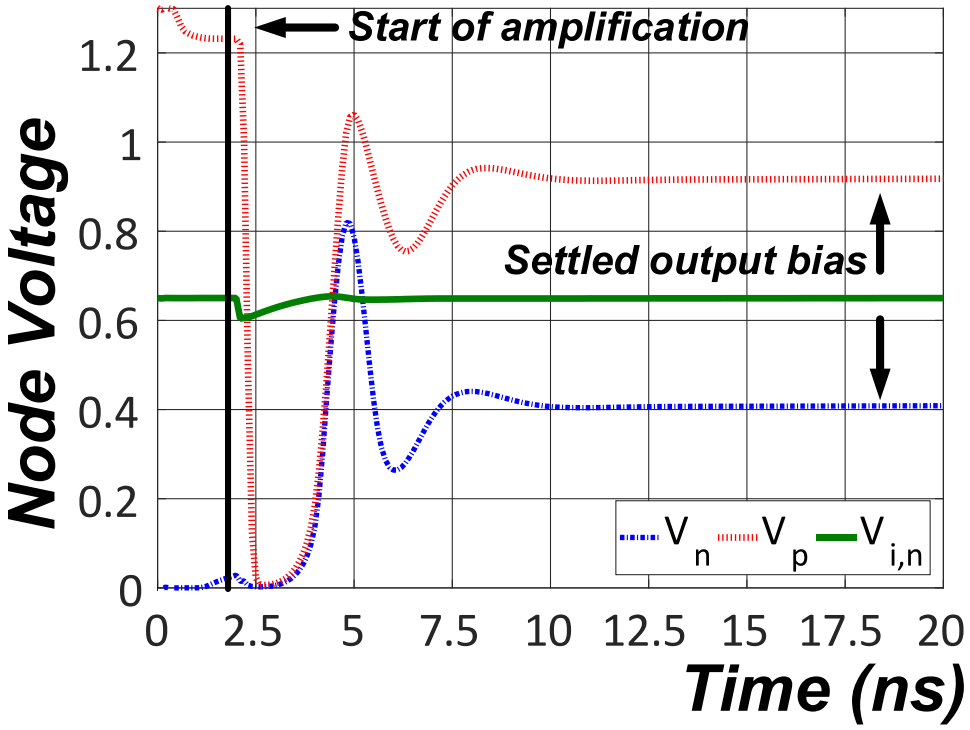

Figure 2.6 Gate voltage of a CSI Ring Amplifier output stage during amplification

amplifier is in its stable state. Overshoot in the transient voltage beyond the damping range results in large signal ringing. The maximum value of overshoot voltage V_{OS} is a function of the maximum I_{slew} the feedback factor and the delay through the loop, T_{delay}.

A transient simulation of the ring amplifier's output stage gate voltages are shown in a switched capacitor circuit, for a positive slewing of the output voltage. As shown in the figure 2.6, red line is VGP and blue line is VGN. At the initial state of the amplification, the gate voltage is going to zero which turns the PMOS fully on and causes the output to slew towards the desired voltage. When the output voltage approaches close to desired value, the amplifier enters small signal settling which brings back all the bias to the steady state voltage.

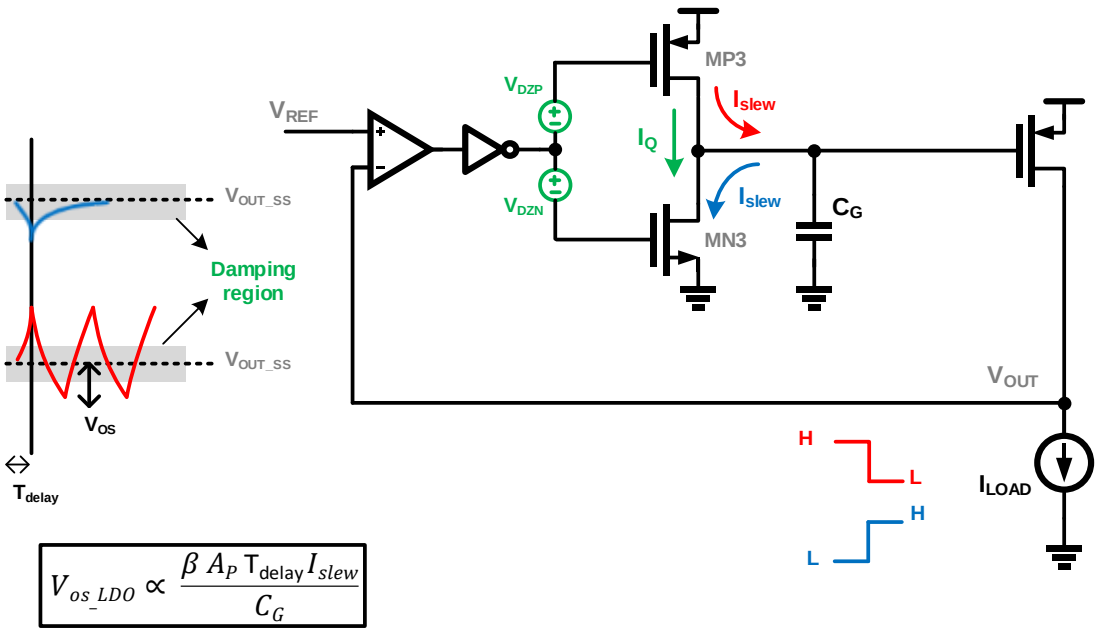

Figure 2.7. Ring Amplifier Operation in LDO Circuits

2.3 Ring Amplifier Operation in Low-Dropout Regulator circuit

When a ring amp is used in an LDO as shown in Figure. 2.7, the disturbance in the output voltage of the LDO during the load transients is directly seen at the input of the ring amp. In addition to the direct feedback, the high gain and the large delay through the pass transistor during the load transition from high to low load current (H-L), results in a large V_{OS} causing instability. Increasing the damping region using conventional ring amp techniques can provide solution to the stability issues for the H-L load transitions but at the cost of slower response during the light to heavy load current (L-H) transitions. In this work circuit techniques to adopt the ring amp for an LDO are proposed, while retaining the low I_Q and fast transient response of its dynamic operation.

CHAPTER 3. RING AMPLIFIER IN LDO

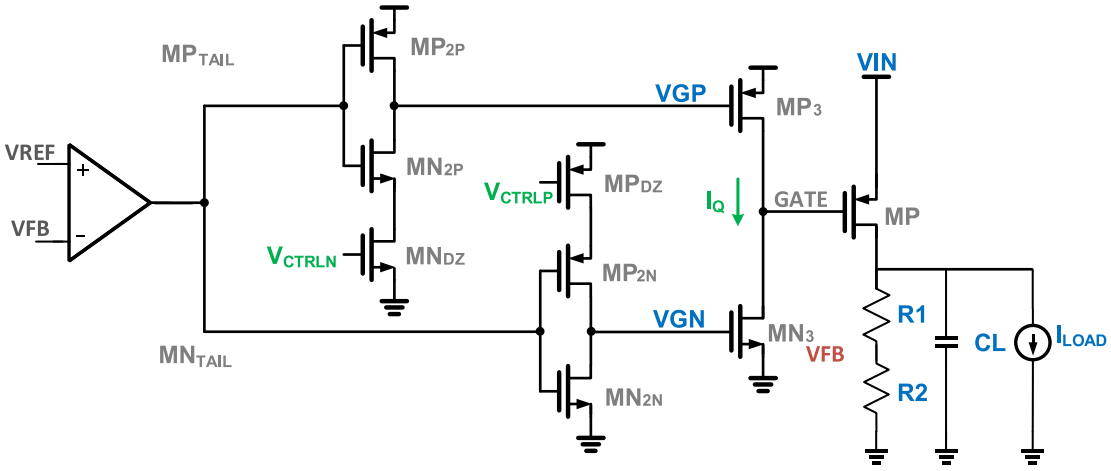

Figure 3.1 Ring Amplifier based LDO with CSI Architecture

3.1 Design Procedure

As discussed in Chapter 2, there are different architectures for the ring amplifier. In order to design a ring amplifier based LDO, the first step is choosing the appropriate architecture. In the analog LDO, clock is not required. Adding a clock needs an extra timing generator. So the capacitor level shifting architecture is not good idea since it requires an additional clock. The Rest of two architecture does not need a clock. However, the resistor biased ring amplifier is also has some inefficient property. The resistor reduced the third stage slew capability which will reduced the LDO settling speed. Also in order to design a low power LDO, each stage required to push the current into very low level. To biasing the output stage into the appropriate stage, the resistor takes a lots of area. So in this work, CSI based ring amplifier is chosen for clock free biasing and faster slewing capabilities.

Figure 3.1 shows the structure of the proposed Ring amplifier based LDO. The first stage is just a differential input single ended opamp because LDO is not

differential circuit. The initial design procedure is same as designing a traditional analog capless LDO. After deciding the size of the power transistor, the intrinsic gate capacitance is important for the starting point of the ring amplifier design. Since the dominant pole of the ring amplifier is at the output stage, the huge power transistor helps the small signal stabilization of the amplifier. To decide the size of the output NMOS and PMO for slewing current, equation (3.1) is used

$$C \times dv = I \times dt \tag{3.1}$$

Where *C* is the intrinsic gate capacitance of the power transistor and *I* is the ON current of the NMOS and PMOS. Based on the initial design specification, voltage range at gate of the power transistor and the slewing time are known. From this the size of the NMOS and PMOS at output stage can be decided. Due to the dynamic operation of the ring amplifier, the bandwidth in the ring amplifier can be much smaller than the traditional opamp for the same settling time. Since the gain bandwidth (GBW) is already smaller than traditional opamp, all the non-dominant poles can be placed at lower frequencies resulting in power savings.

To design the second stage. Given a steady state input voltage, while sweeping the control voltage V_{CTRLN} and V_{CTRLP}, the output voltage should cover a large range which includes the appropriate biasing voltage range of the output stage. The steady state input voltage is depends on the load changed range. The first stage is just a simple differential input singled ended output amplifier.

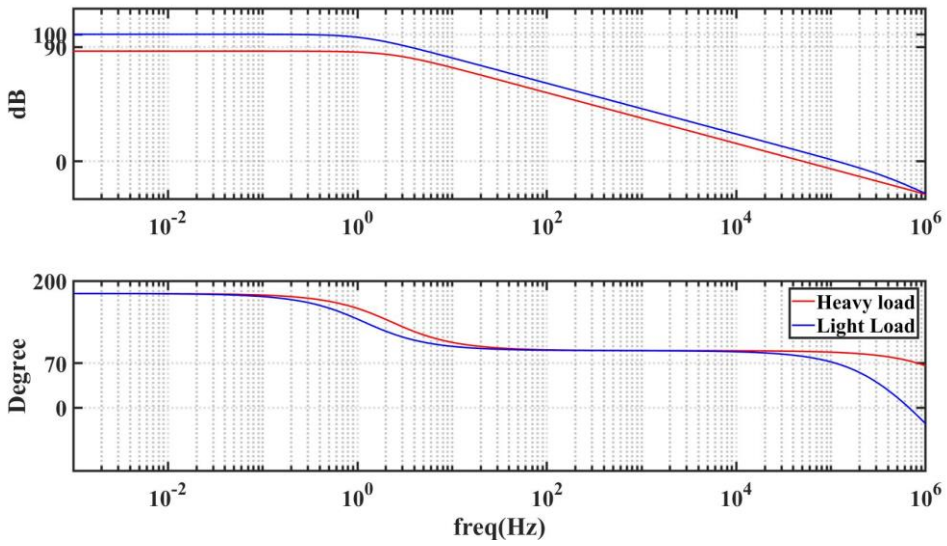

Figure 3.2 AC simulation of the LDO Loop

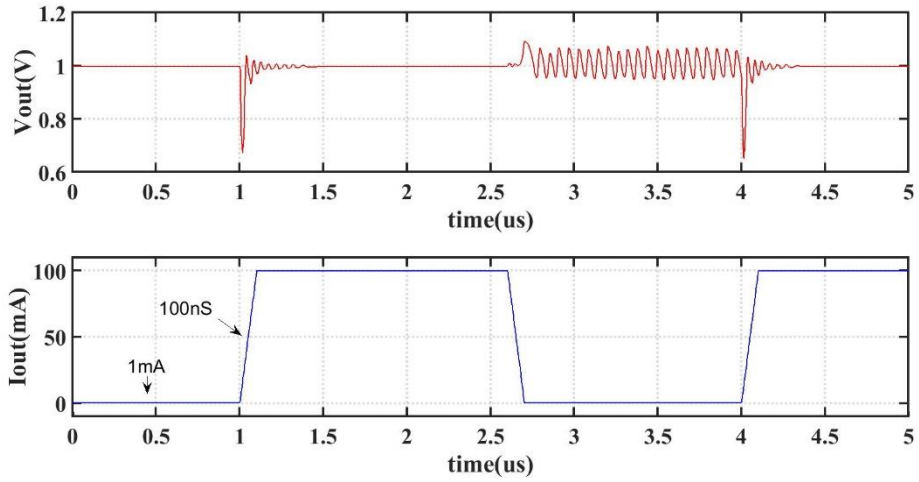

Figure 3.3 Load transient Simulation with “good” phase margin

3.2 Stability Analysis

After initial design the ring amplifier based LDO, an AC simulation is shown in the Figure 3.2. From the AC plot, the loop has phase margin greater than 70 degrees

which means the loop should be in stable condition. However, shown in the Figure 3.3 is the transient simulation for the heavy to light load change condition. As seen from the figure there is a significant ringing in the transient showing a large signal stability issue.

As mentioned before, initial transition of the ring amplifier is a dynamic behavior. Small signal response is only valid when amplifier is close to the steady state. Ring amplifier based LDO has 4 gain stages. The large signal delay especially, the delay at power transistor, makes the system unstable for large transients. Due to the class AB type of the output stage, NMOS and PMOS will easily overcharge or discharge the gate of the power transistor. The ring amplifier will never get into damping region.

CHAPTER 4. PURPOSED AND IMPORVING TECHNIQUE

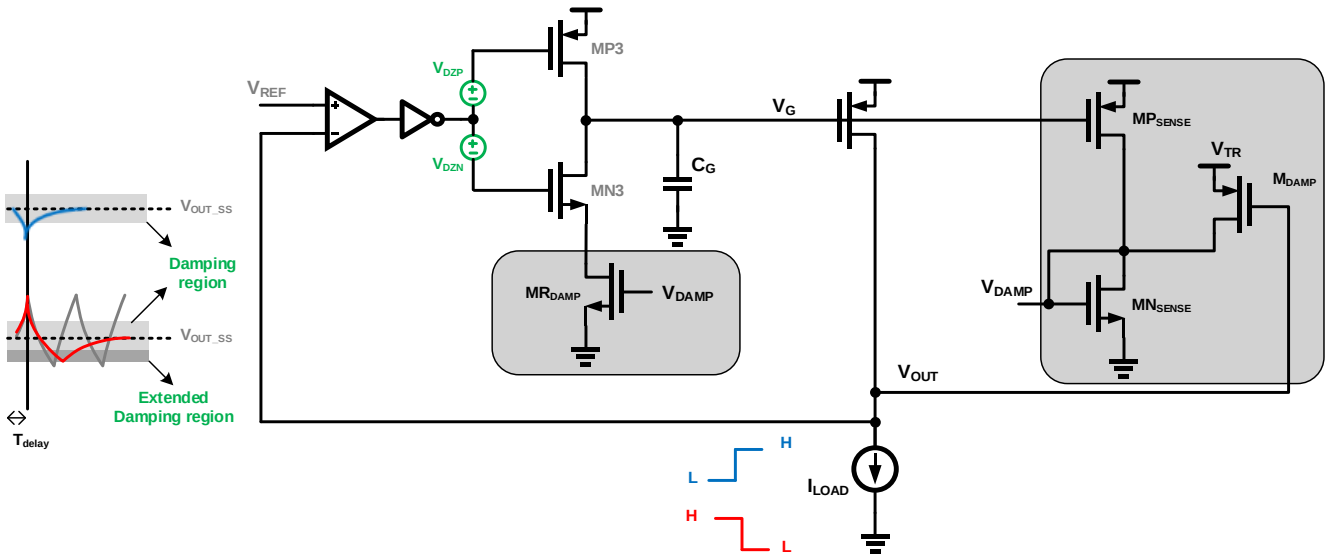

Figure 4.1 Purposed Compensation Technique

In order to solve the stability issue, a damping region extended was purposed and implemented in this works. Furthermore, a replica biasing circuit is implemented [8]. In this Chapter, both technique will be discussed in detail.

4.1 Damping Region Extended Technique

Fig. 4.1 shows the proposed compensation technique for ring amp based LDO that introduces an extended damping region for H-L load transition. This is implemented by using transistor (acting as a voltage controlled resistor R_{DAMP}) in series with the NMOS transistor MN3 at the output stage of the ring amp. The small signal ac parameters of the ring amp remain unaltered by ensuring that the R_{DAMP} is much smaller than the steady state output resistance of MN3,. During the H-L load

transient, R_{DAMP} dominants the resistance of MN3, thereby weakening MN3 from pulling down the output of the ring amp and creating an effective damping to reduce any large signal ringing. The control voltage MR_{DAMP} is generated by a load current sensing circuit to ensure that the nominal value of V_{DAMP} tracks all load conditions and also to ensure that V_{DAMP} does not affect the fast settling time during the L-H load transitions. Equivalently this technique increases the damping range of the ring amp while retaining the fast transient response. Additional transistor MR_{DAMP} defines the width of the extended damping range during the H-L load transient. Choosing a wide damping region results in overdamped response, while choosing a very narrow damping region results in ringing. Trimming of compensation supply voltage V_{TR} is enabled to allow the option of defining the damping region for a wide range of regulated output voltages.

Figure. 4 shows the complete schematic of the proposed ring amp based LDO. The first stage is a differential input single ended output common source amplifier. The second stage of the ring amp is composed of current starved inverters. V_{DZP} and V_{DZN} set the deadzone voltage and hence IQ at the third stage of the amplifier.

4.2 Replica biasing Technique

In the CSI based Ring amplifier, the second stage use control voltage to control the deadzone, which required 2 different voltage for biasing. Once chip are

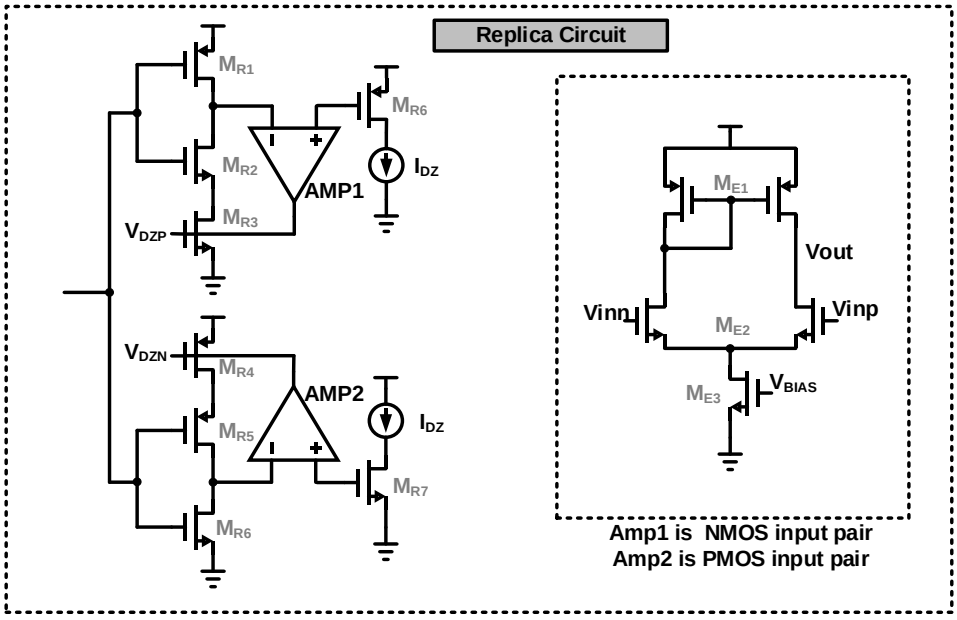

Figure 4.2 Replica biasing Technique

fabricated due to the PVT variation, it always become a problem for find correct or optimizing control voltage.

In [8], a replica biasing technique is purposed for finding the correct voltage. As shown in Figure 4.2, there is a feedback loop. On the negative side, a current starved inverter is connected. The size is same as the second stage ring amplifier. On the positive side, the diode connection transistor is connected. The size is same as third stage. A current source is tied to the drain. So in this way, the third stage in the ring amplifier can be easily balanced. Furthermore, Power supply rejection is always a problem in the inverter. Those replica biasing circuit can also sensing the noise from power supply and cancel the noise from the second stage of ring amplifier.

CHAPTER 5. SIMULATION AND MEASUREMENTS RESULTS

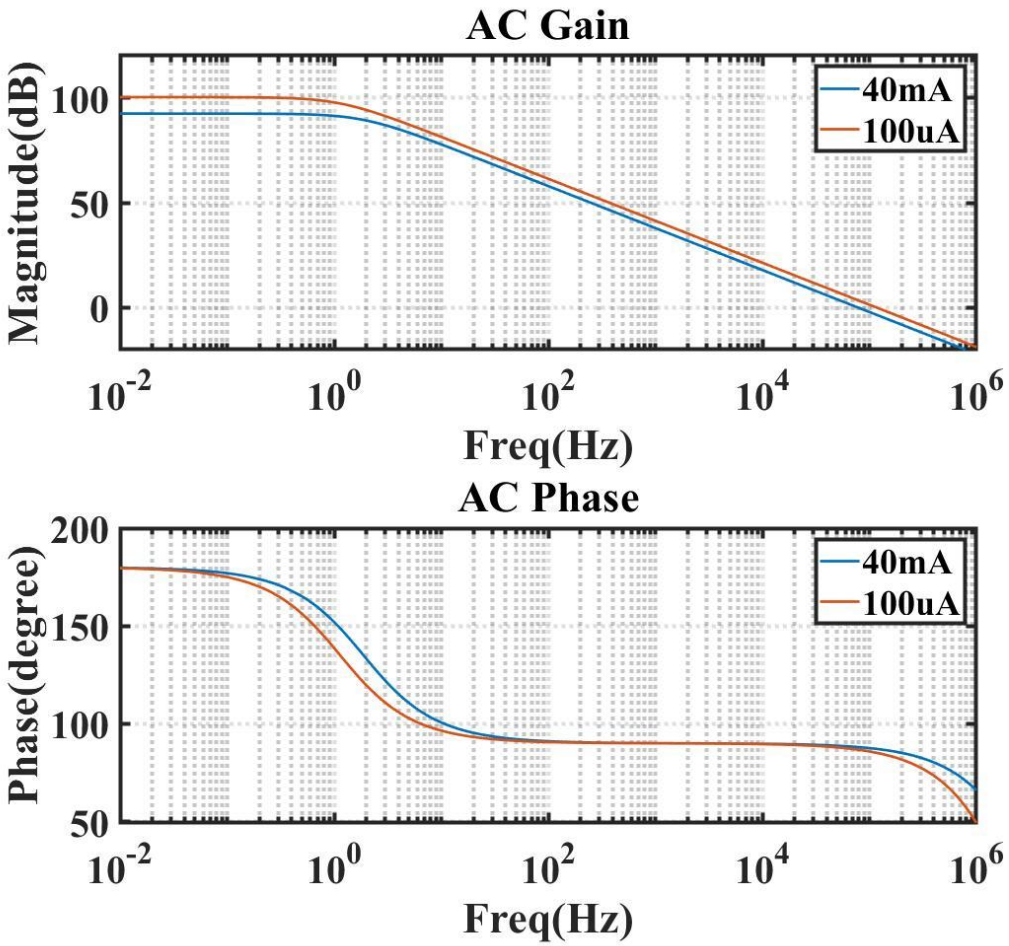

Figure 5.1 AC simulation Result with Purposed Technique

Figure. 5.1 shows the simulated ac response with 2 load conditions. A dc gain higher than 80dB is achieved across 100uA to 40mA load conditions with Gain bandwidth of 100 KHz and a phase margin higher than 80 degrees.

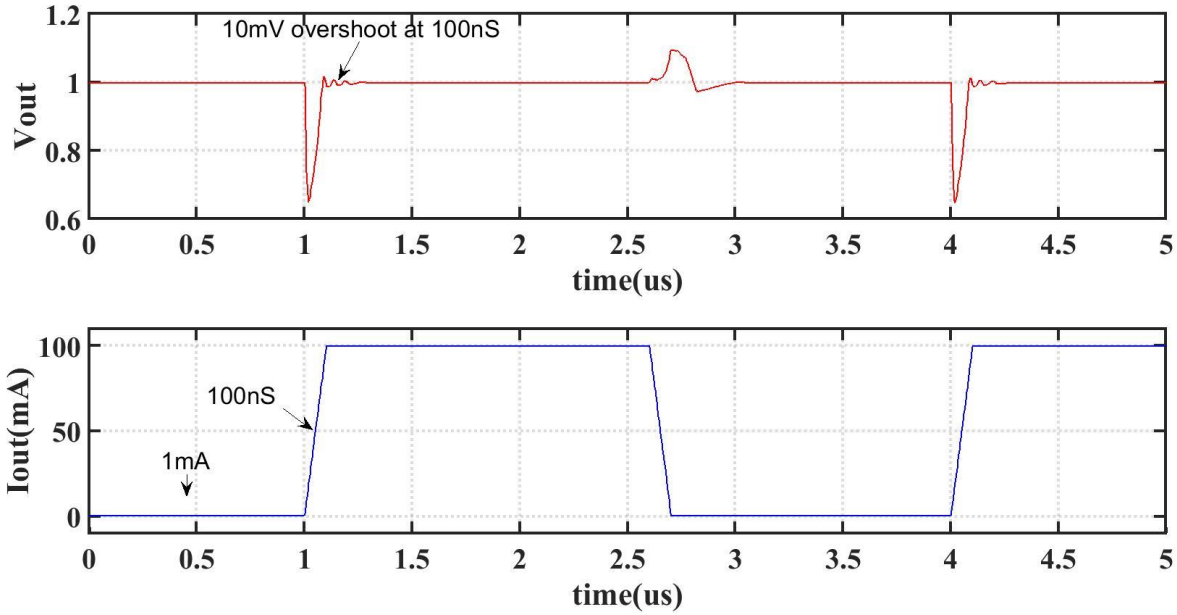

Figure 5.2 Transient Simulation Result with Purposed Technique

Figure 5.2 shows the transient simulation result with purposed technique. Here, the simulated load transient step is from 1mA to 100mA. As we can see, the system is in a pretty stable condition. There are small ripple at low to high condition, but those ripple is in 10mV range and quickly disappear.

This chip is implemented and fabricated in (ASAHI KASEI MICRO-DEVICES) AKM 180nm Technology. After measurements, the performance is not good as the simulation results but still compatible. Next couple figure shows the measurements result and comparison table.

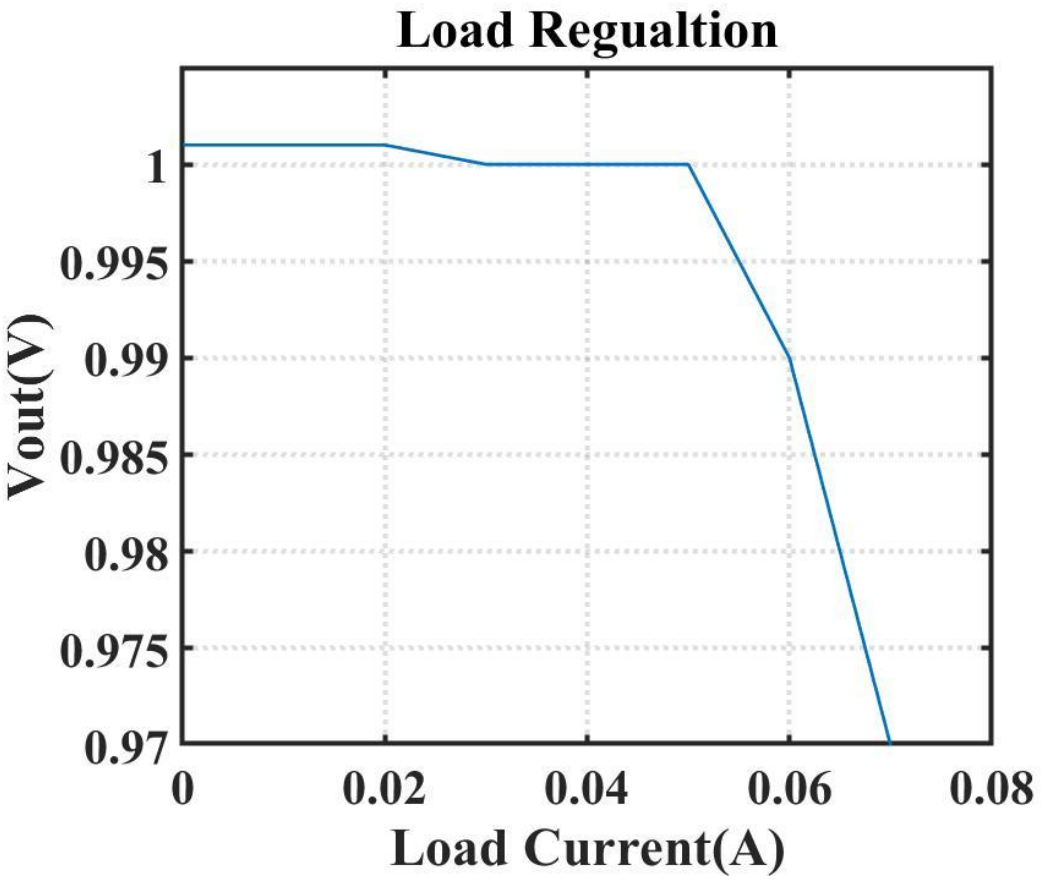

Figure 5.3 Load Regulation Measurements

Figure 5.3 shows the load Regulation. By sweeping the output load, we can find when the Vout start drop. This chip is design for contact 100mA current. However, as we can see from figure 5.3, the output voltage start decreased about 50mA. This is because at high current, the voltage caused by the parasitic resistor from the power transistor and pad dominant. If the Vout keep at 1V, the Vds of the power transistor is not enough to conduct above 50 mA current, so that the Vout has to drop in order to conduct that much currents.

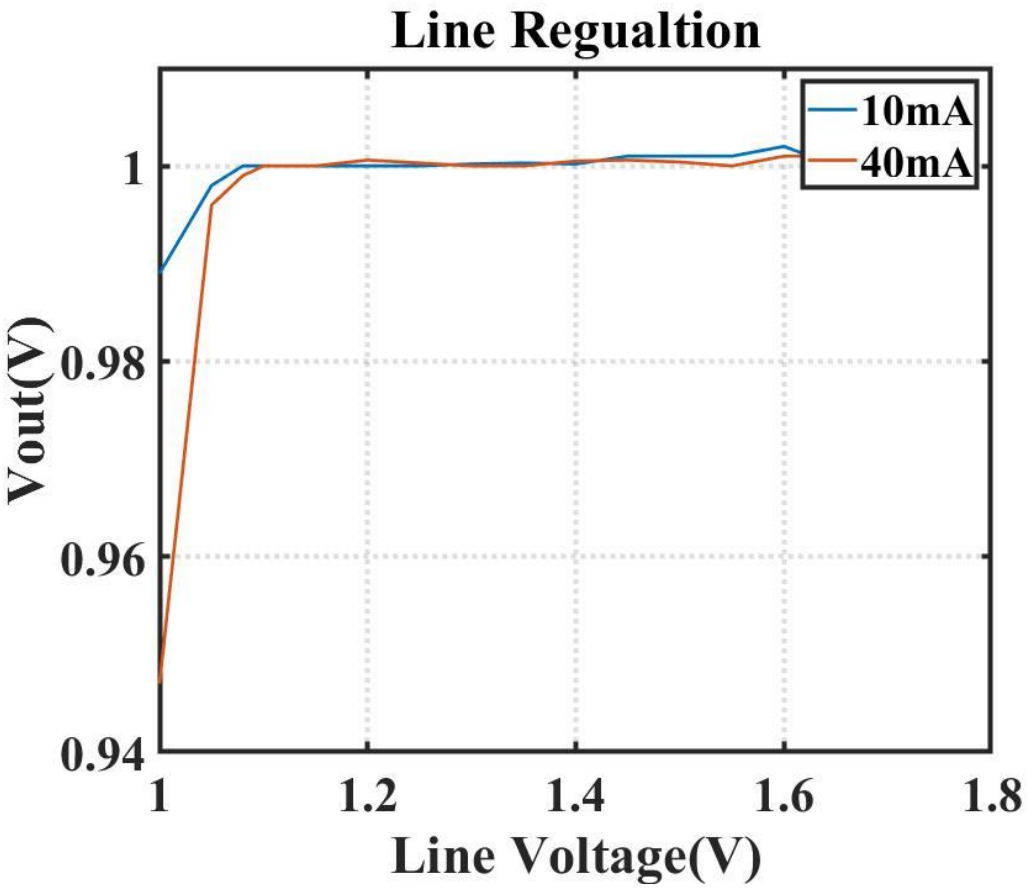

Figure 5.4 Line Regulation Measurements

Figure 5.4 shows the line Regulation Measurements. At given current load condition, by sweeping the Vdd which is line voltage, a Output voltage can be measured. If we want to output 40mA current, the vdd has to be higher than 1.08 V. Again, this is due to the parasite resistance.

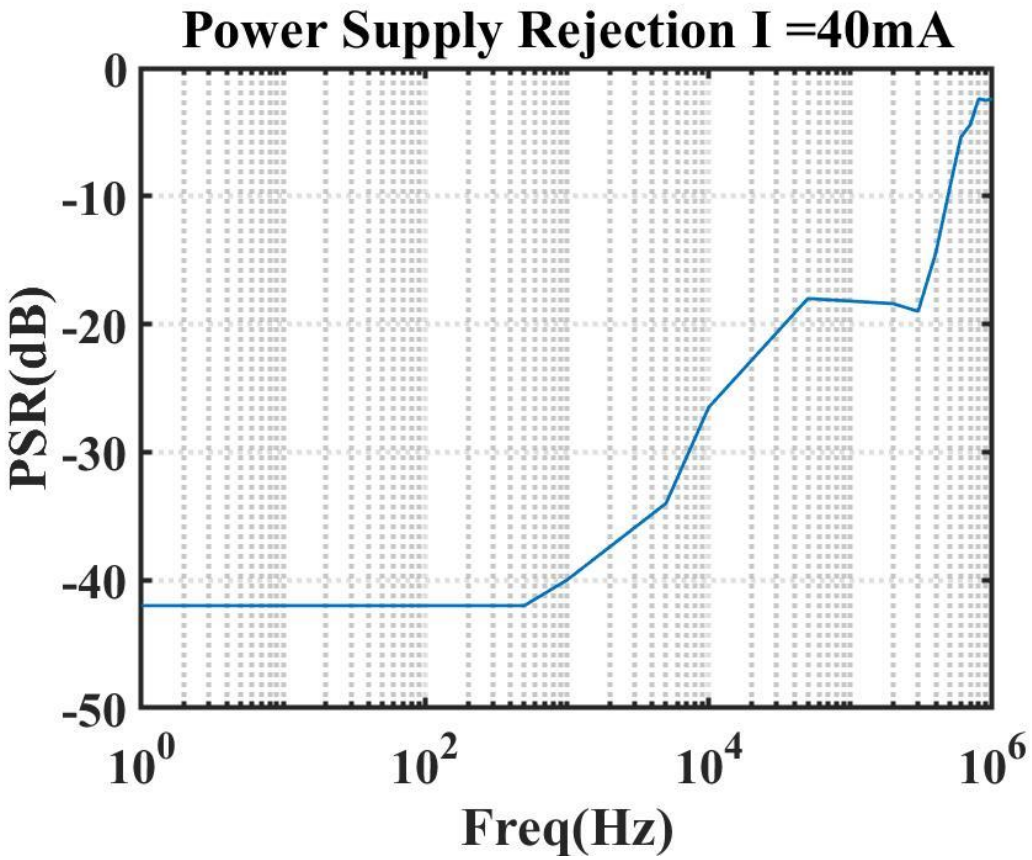

Figure 5.5 Power Supply Rejection Ratio

Figure. 5.5 shows the measured Power Supply rejection Ratio(PSRR) of the LDO for 40mA load current. The DC PSRR of 42dB is mainly caused by the supply noise from first stage of the ring amp.

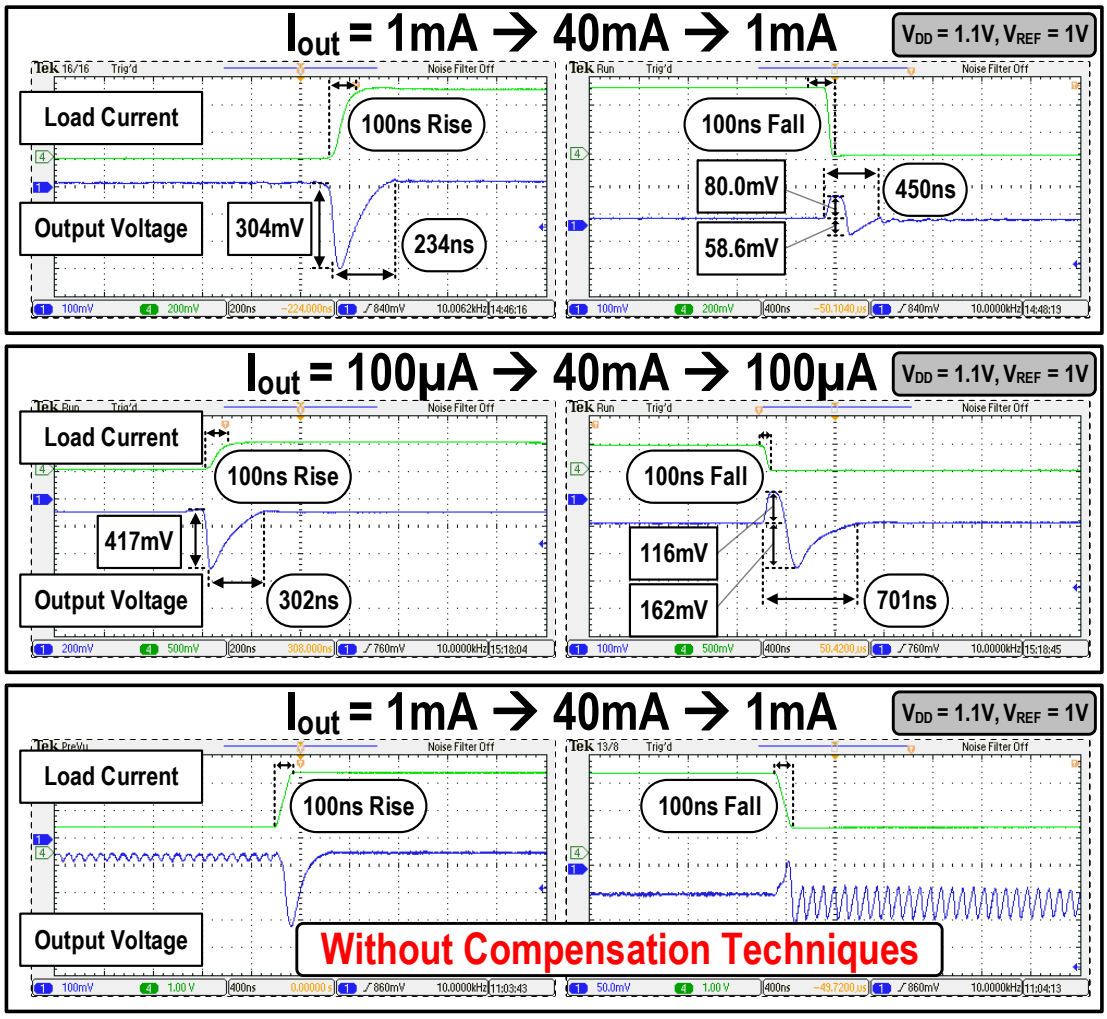

Figure. 5.6 Load Transient Measurements

Fig. 5.6 shows the measured transient response for load current steps with 100ns rise/fall time with and without the proposed compensation technique. The effectiveness of the proposed compensation technique can be observed by visible ringing in the output without compensation. With the proposed compensation, the settling time for load current transients are 234ns and 450ns for 1mA to 40mA and 40mA to 1mA respectively; 302ns and 701ns for 100uA to 40mA and 40mA to 100uA respectively. A maximum droop of 400mV is observed during the low to high

Publication	This work	[1]	[2]	[3]	[4]
Technology	180nm	130nm	65nm	65nm	65nm
Control Method	Ring Amplifier	Analog	Inverter Based	SR+AA	Event Driven
VDD(V)	1.08-1.65	1.05-2.0	0.6	0.5-1	0.45-1
VOUT(V)	1	1	0.3-0.55	0.45-0.95	0.4-0.95
IOUT(mA)	40	300	50	12	0.014-3.356
Tsettle(ns)	234-700	8000	2500	3000	11200
COUT(nF)	0.01	1000	0.04	0.1	0.1
Edge time Δt(ns)	100	1000	150	1	1000
Edge Time Ratio K	100	1000	150	1	1000
Current Step ΔI_{OUT}(mA)	40	300	10	10	1.4
Undershoot ΔV_{OUT}(mV)	304	80	133.9	105	34
Iq(uA)	6.5	14-120	32	3.2	8.1-258
FOMt(ps)	0.011	12.4	1.71	0.333	14.1
FOMv(V)	0.00525	0.00261	0.0643	0.0000336	0.197

*FOMt = (COUT *VOUT *Iq)/ $IOUT^2$

*FOMv = K(ΔV_{OUT} * Iq)/ΔI_{OUT} (K is the Δt ratio w.r.t smallest t among all compared)

Table 1. Comparison Table

current transition. The large droop is a result of the initial delay through the first two stages of the ring amp before the output stage of the amplifier begins its slewing operation. The LDO consumes a quiescent current of 6.5uA under no load condition. An output capacitor of 10pF is used during the measurements.

The Comparison table(Table 1) compares recent year outstanding LDOs. From table, this work has best settling time and good quiescent current consumption. Furthermore, the figure of merit is also in a good situation. There are still some

problem need to be fixed such as the large undershoot voltage. Also the maximum current this LDO can conduct need to be also improved. In the simulation, it supposed to conduct 100mA current or even higher. So the layout is thing need to be improved. Also the rising edge testing can be also improved. Due to the equipment and testing method limit, the fast edge it can be tested with is 100ns. In the simulation, 1 ns is also can be achieved .

Conclusion

A capless LDO with scalable ring amp is demonstrated to achieve faster transient response and low quiescent current. Ring amp offers area efficient architecture compared to state-of-the-art Analog and Digital LDOs [1-4]. Circuit techniques are introduced to adopt the ring amp operation for a non-capacitive feedback system of the LDO. Proposed capacitor less compensation technique improves the damping region of a ring amp across various load conditions without any large area overhead. A current starved inverter based ring amp with replica biasing ensures tracking of steady state parameters across PVT. The ring amp occupies an area of 70um x 60um while the power transistor occupies an area of 350um x 250mThe LDO can handle an output capacitor range of 0 to 300pF.

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