AN ABSTRACT OF THE DISSERTATION OF

Carly Fengel for the degree of Doctor of Philosophy in Physics presented on December 16, 2021.

Title: Bioelectronic Systems for Neurosensing Enabled by Graphene.

Abstract approved:

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Ethan Minot

Taking long-term electrical measurements of a large number of neurons simultaneously is required for many modern neuroscience experiments. However, such experiments are currently limited by the shortcomings of traditional neurosensing technology. For example, there is a significant mechanical mismatch between rigid silicon probes and soft biological tissues. This mismatch can lead to tissue damage upon probe insertion and formation of scar tissue around the recording sites. The scarring, as well as the migration of salts from biological fluids into silicon electronics, diminishes the recording ability of the sensors over time. Additionally, traditional passive electrodes require one wire for every recording site. To reach the range of thousands of simultaneous measurements, the number of wires necessary to connect the implanted sensors to the external electronics is not feasible. Recently, nanomaterials have been explored for next-generation neural probes. Nanomaterials have unique properties that can be utilized in novel neurosensor designs that can address the previously mentioned limitations.

Graphene is a nanomaterial that is well-suited for building neurosensors due to its biocompatibility, mechanical flexibility, and good electrical properties. Furthermore, prior research has shown graphene field-effect transistors can measure action potentials of *in-vivo* and *in-vitro* neurons. We investigate unique uses for graphene field-effect transistors (FETs) in neurosensing applications.

We first show that the noise in our devices is low enough to detect neuronal signals. The effective gate voltage noise for our best device is ~170 μV_{RMS} for a 20 μm x 40 μm

device, which is about a factor of 5 larger than the noise for state-of-the-art graphene FETs when normalized for area. Improvements in noise were achieved with anti-aliasing filters and, to a lesser extent, fabrication techniques like sandwich contacts and annealing.

Next, we developed an array of graphene FETs with multiplexing (wire sharing) for taking simultaneous measurements of many neurons. A twin-liquid-gate wafer with 1x2 test arrays of graphene FETs was fabricated, and 1 kHz signals were successfully reconstructed after multiplexing. A spacing of 10 kHz between carrier frequencies was used. The reconstructed signals from the multiplexed current were compared to signals from DC measurements; the multiplexing and reconstruction processes did not reduce signal size or increase noise. The crosstalk between channels was tested and found to be negligible. Based on the performance of our prototype devices, we argue that this is a scalable technology that be used to operate arrays of more than 2000 sensors with fewer than 100 input/output wires. We interfaced our graphene FET array with a custom integrated circuit chip that amplifies and digitizes the multiplexed signals.

Then we show that our graphene FETs are capable of measuring action potentials from single cells *in-vitro*. A signal-to-noise ratio of up to 20 was achieved when cells were cultured on top of the graphene FET. We developed a procedure to release graphene FETs from the substrate and then place the released graphene devices on individual cells for targeted single-neuron measurements. No electrical signals were observed, and we speculate that this was due either to cell injury upon contact, migration of ion channels away from the sensor channel, or too much distance between the cell membrane and the sensor channel. The distance between the cell membrane and the graphene channel of a lowered device was estimated using fluorescence techniques and in conjunction with the electrical data, we estimate that the distance was > 30 nm.

Bioelectronic Systems for Neurosensing Enabled by Graphene.

by
Carly Fengel

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APPROVED:

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Carly Fengel, Author

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CONTRIBUTION OF AUTHORS

Morgan Brown taught me many of the fabrication and testing techniques used in this dissertation. Siyuan (Richard) Yu and Jinyong Kim from Matt Johnston's group designed the IC chip and assisted in testing the joint graphene FET-IC chip system for the data in Chapter 4. Samantha Norris and Michael Reynolds from Paul McEuen's lab contributed to the fabrication of graphene devices in Chapter 5. The neuronal cell line used in Chapter 5 was obtained from Patrick Chappell. Amani Alobaidi provided training on cell culture and Chris Eddy provided training on the fluorescence microscope in the lab of Bo Sun. Ethan Minot provided guidance for all work presented in this dissertation.

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CHAPTER 1: INTRODUCTION

1.1 Future of Neurosensing Technologies

The complex problems at the forefront of neurosensing require larger number of longer, higher resolution measurements than ever before. While silicon has been used as the infrastructure for neurosensing probes since 1970[2] due to the wide array of silicon microfabrication techniques, tools for recording neural activity are moving beyond silicon due to its mechanical incompatibility with soft tissue and limitations in long-term use. Silicon by nature is a sharp, crystalline material and while silicon shank probes can make high density, high sensor count recordings with excellent temporal resolution[3], when in contact with soft tissue these shanks can cause damage and become encapsulated in scar forming tissue, impeding the sensor performance over time[4,5]. *In-vitro* studies of cells, for example culturing cells onto an electrode array, don't require as stringent of mechanical compatibility with soft tissue; however, silicon is susceptible to degradation from the salty biological fluids that living cells inhabit[6]. The limitations in silicon-based electrodes have inspired the exploration of novel materials for neurosensor development.

Mechanical compatibility can be addressed with small and minimally invasive or soft and flexible sensors. Nanowires are minimally intrusive as they're on the size scale of cells. They have been shown to support cell adhesion[7], and can be fabricated into a variety of shapes, such as 3D arrays[8,9], nanowire mesh networks[10,11], and microstructures to guide axon growth[12]. Flexible arrays use thin, plastic substrates with flexible active materials to conform to the surface of soft brain tissue[13–16]. Other unique nanosensing tools include injectable mesh electronics[17], 3D hydrogels[18], and deep fluorescence microscopy with photon collection via small optical fibers[19]. A transparent flexible nanowire array that allows simultaneous fluorescence and electrical measurements was published in 2021[15].

While the aforementioned technologies address the issues with mechanical compatibility, meeting the requirements of high temporal resolution, high density sensor counts with a high signal-to-noise ratio (SNR) are additional challenges.

The temporal resolution required for recording individual action potentials (APs) from cells requires millisecond resolution (~1 kHz)[20]. For example, fluorescence imaging can achieve high signal count and spatial resolution, but not the temporal resolution required for single action potentials[21]. Organic semiconductors are flexible but are better suited for low frequency-band (<200 Hz) measurements of the local field potential (LFP) than of APs[22] due to their limited mobility.

High-sensor-count technologies need to be scalable. Passive electrode designs are difficult to scale up because each sensor requires one wire, and the area required by wiring quickly becomes a limiting factor in the total number of sensors that can be monitored simultaneously. Innovative active electrodes have recently made multiplexing possible so that large arrays can operate with significantly fewer wires[23] (as discussed in Chapter 3).

The SNR achievable depends on the device configuration and the intrinsic properties of the sensor material. The currents created by neurons are ionic, while those in the sensor are electron (or hole) currents, and understanding the interface using established models[24,25,26] can help inform sensor design to maximize the signal measured. For example, reducing the impedance between the electrolyte and the sensor improves the signal size[26]. The impedance of this interface increases as the electrode surface area decreases, which must be considered when making sensors on the size order of cells (~10 μm). Using nanomaterials to modify the sensor surface can improve the impedance of small electrodes by increasing the surface area without losing the single-cell selectivity; for example, a study that coated electrodes with carbon nanotubes, which have a high surface area, was able to increase the impedance at 1 kHz by a factor of 25, and improve the amplitude of recorded signals, as well as improve the biocompatibility[27]. Another study made sensors that recorded APs with a high SNR (>100) by using vertical nanowires to improve the coupling between the neurons and the sensors[28]. The vertical nanowires penetrated the cell membrane, which prohibits long-term study of the same cell. Flicker, or 1/*f*, noise is intrinsic to many electronic devices and is prominent in the sensing band relevant to LFPs and APs. The salty and sometimes dirty environment that neuron measurements take place in can contribute to that overall noise, making it even more important to maximize signal strength.

Graphene is a 2D material that has shown promise as a tool for neurosensing. It is chemically stable, soft, and promotes cell growth and adhesion[29,30]. Graphene is flexible and compatible with fabrication techniques for making devices on flexible substrates[16,31,32], or even free-floating sensors when etched from the substrate[33]. Wafer-scale fabrication is achievable with CVD-grown graphene, enabling large arrays of sensors. Graphene's high mobility also enables measurements in the frequency band of individual action potentials. The noise in graphene is well described and there are several fabrication techniques developed for improving the SNR.

In this thesis, I will discuss my work developing neurosensing tools based on graphene field-effect transistors (FETs). First, I measure the noise in my graphene FETs and compare it to existing noise models. I show that the device noise is well described by the augmented charge noise model, and is low enough to detect action potentials. Then I create a 1x2 array of graphene FETs that uses signal

multiplexing to reduce wire count; this is proof-of-concept for a large array capable of large numbers of simultaneous measurements. Next, I show that individual action potentials from neuronal cells cultured onto the graphene FET devices can be measured. Then, I develop a method to release graphene sensors from the substrate for targeted measurements of single cells. Released graphene sensors are put directly onto cells and measurements are attempted.

1.2 Graphene Field-Effect Transistor Operation and Sensing Mechanism

Graphene FETs sense changes in the electric potential local to the graphene channel. Neurons generate changes in voltages during APs, and a graphene FET near the cell can detect this change. This will be modeled in Chapter 5. Figure 1.1a shows a cross-section of a liquid-gated graphene FET. Devices are fabricated on an SiO2 substrate, and consist of a graphene channel, with a gold source and drain electrode on each end. Devices are operated in an electrolyte which acts as the gate. The electrolyte doubles as a cell medium when working with *in-vitro* cells. A layer of SU-8 polymer is deposited on regions of gold in contact with the electrolyte to prevent Faradaic currents.

The measurement setup of a graphene FET is shown in Figure 1.1b. When used as a sensor, the source-drain bias V_{sd} and gate voltage V_g are set at fixed values, and the current I is monitored. The device is operated where a change in the gate voltage creates a proportional change in the source-drain current. To determine an operating point of a graphene FET, a source-drain bias V_{sd} is applied across the gold contacts on the graphene, an Ag/AgCl electrode applies the voltage gate voltage V_g to the electrolyte gate, and the source-drain current I is measured as V_g is swept. The current as a function of gate voltage for a device is shown in Figure 1.1c, while the resistance ($R = V_{sd}/I$) is shown in Figure 1.1d. The operating point is set where the transconductance dI/dV_g is constant, so changes in I are proportional to changes in V_g. When a neuron generates an AP near the graphene channel, the changes in the local electric potential result in changes in the current through the graphene FET. The voltage signal can then be determined from the measured changes in current using the transconductance (found from Figure 1.1c). Operating the device in the region with the largest transconductance will give the largest change in current per change in gate voltage signal.

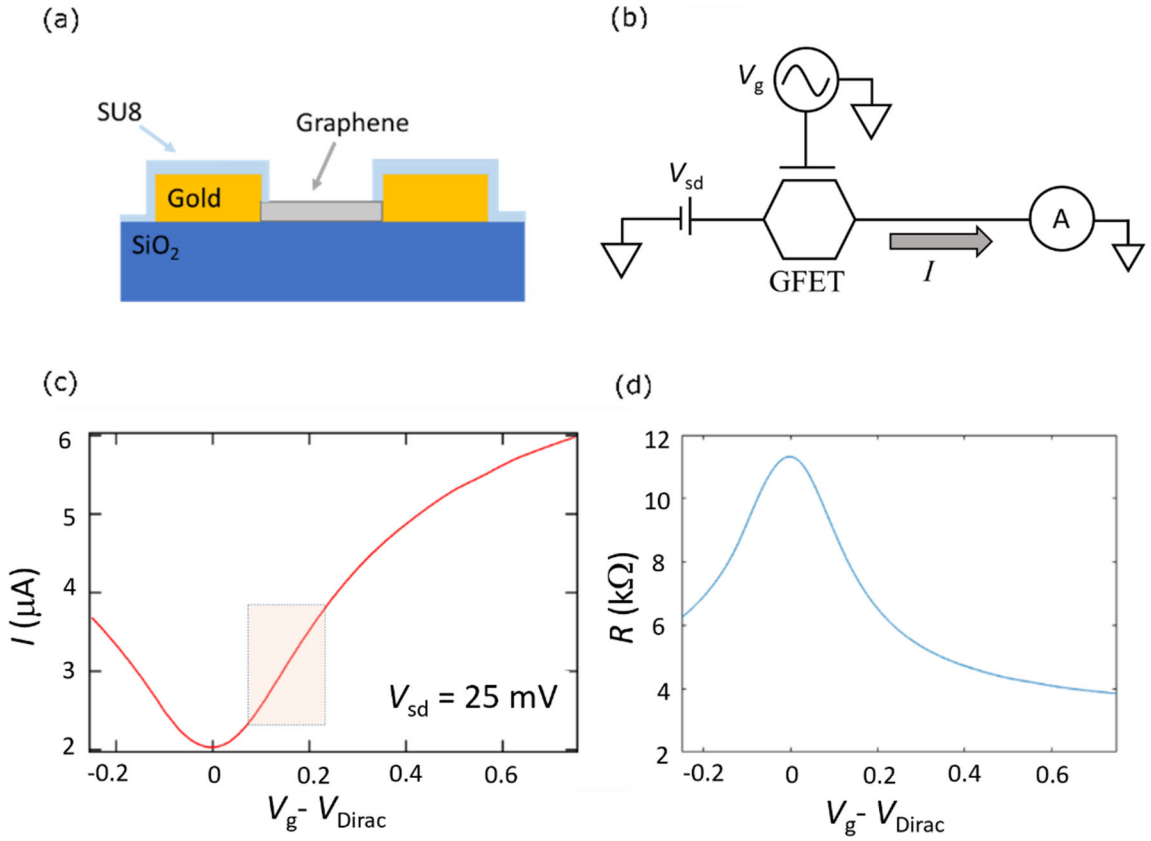

Figure 1.1: Device geometry and electrical characterization. (a) The cross-section of a graphene FET is shown (not to scale). (b) A constant source-drain bias V_{sd} is applied to the graphene channel and a gate voltage V_g is applied to the electrolyte gate. The source-drain current I is measured. (c) The transfer characteristics (IV_g curve) of a graphene FET with V_{sd} = 25 mV. The box highlights a possible operating regime, where dI/dV_g is constant. (d) The resistance of the system $R = V_{sd}/I$ as a function of gate voltage.

The change in current (or resistance) of the graphene channel in response to applied gate voltages is related to the band structure of graphene. Graphene is a zero bandgap material with a linear dispersion, as shown in Figure 1.2. The Dirac point is where the valence and conduction band meet, and it is the minimum conductance of the material. Typically the Dirac point does not occur at $V_g = 0$ due to electrostatic doping from nearby charges in the substrate or residual chemicals from fabrication. As the voltage of the gate electrolyte changes, the Fermi level within the graphene shifts, changing the number of free carriers in the graphene channel. Graphene is ambipolar; it conducts electrons when $V_g > V_{Dirac}$, and holes when $V_g < V_{Dirac}$.

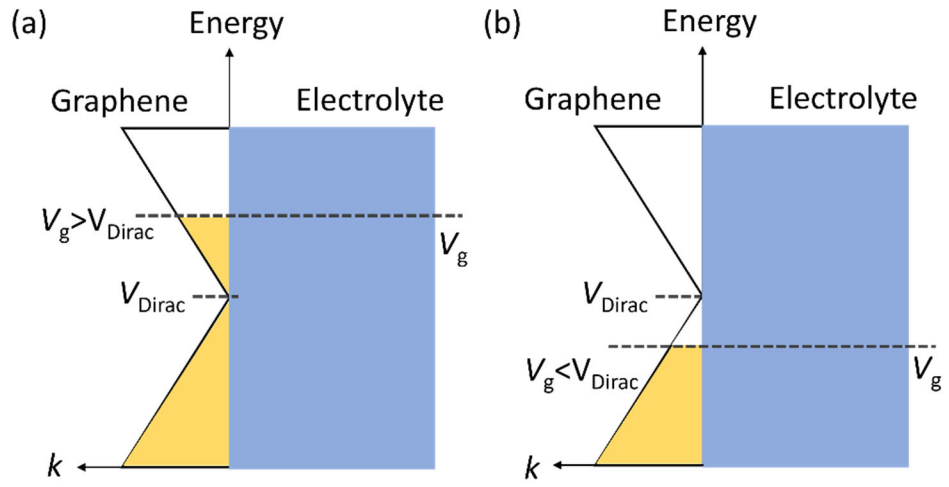

Figure 1.2: Band structure of graphene around the Dirac point. (a) When a gate voltage $V_g > V_{Dirac}$ is applied to the electrolyte, the Fermi level of the graphene shifts into the conduction band and electrons conduct through the graphene channel. (b) When $V_g < V_{Dirac}$, the Fermi level of the graphene is in the valence band and holes are the conductors in the graphene channel.

CHAPTER 2: METHODS

2.1 Fabrication Procedures

2.1.1 Graphene FET Fabrication

Graphene FETs are formed with graphene channels and metal electrodes and leads. The devices are liquid-gated. The cross-section of a device is shown in Figure 2.1a. The devices used in Chapter 2 and Chapter 4 for noise analysis and frequency-division multiplexing have leads coated in SU-8 connecting the graphene channel source and drain electrodes to contact pads, as shown in Figure 2.1b. The devices used in Chapter 5 for *in-vitro* cell work have no leads, and are not passivated (pictured in Figure 2.1c); high impedance probes are lowered directly onto the exposed metal of the source and drain electrodes through the electrolyte to connect to the graphene channel.

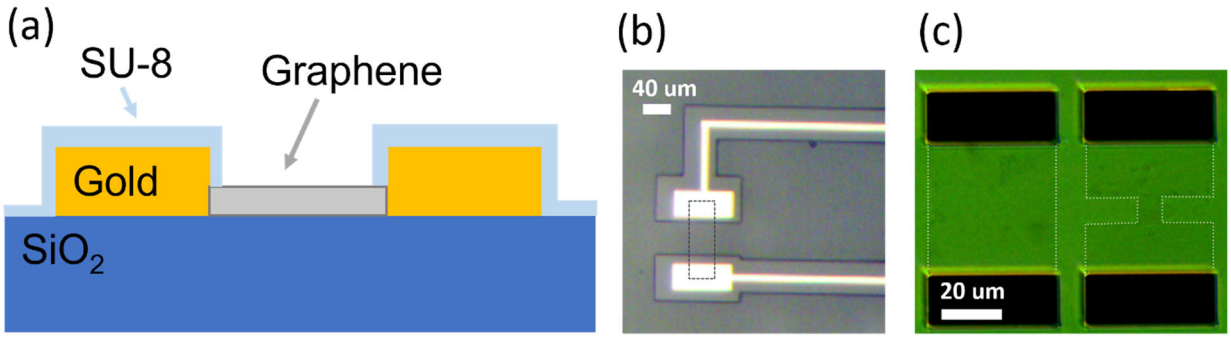

Figure 2.1: Liquid-gated graphene FET structure. (a) Cross-section of a graphene FET. (b) Optical image of a graphene FET with leads. The graphene channel is outlined in a dotted line. (c) Optical image of two graphene FETs used for *in-vitro* cell measurements. The graphene channels are outlined in dotted lines.

To fabricate a graphene FET device, first the metal electrodes and leads were photopatterned with AZ1512 photoresist (Microchem). A fused silica wafer or a coverslip that had been triple-rinsed (with acetone, isopropanol, and DI water) was baked on a hotplate at 115° C for 3 minutes. Primer (20/80) was spun on at 4k RPM (ramp rate 1k RPM/s) for 45 s. Then LOR3A (lift-off resist) was spun on at 4k RPM for 45 s. The wafer was hard baked at 190° C for 4 minutes. The photoresist AZ1512 was spun on at 4k RPM for 30 s, then the wafer was hard baked at 110° C for 90 s. The wafer was exposed under a contact aligner with an exposure dose of 40-60 mJ/cm^2 (2-3 s under a lamp with power~20 mW/cm^2). The wafer was then developed in a dish of AZ300 MIF developer (Integrated Micro Materials) with ample agitation for ~30 s, then put into a dish of DI water for 60 s and agitated. Then the wafer was triple-rinsed and dried with nitrogen (N_2).

Next the metal for the leads was deposited with electron beam deposition. The wafer was placed into the vacuum chamber, and the chamber was pumped down to about 3 μTorr. A layer of Cr was deposited (to adhere to the SiO2 substrate), then a 40 nm layer of Au was deposited. After deposition, the wafer was placed into a bath of Remover PG at 60° C for 15 minutes. After 15 minutes, a disposable pipette was used to spray the wafer with warm PG and remove some of the lifted-off metal, then the wafer was moved to a fresh bath of Remover PG at 60° C overnight. After the wafer was triple-rinsed and dried with N_2.

The next step was adding the graphene to the wafer via a wet transfer process. The graphene used was CVD grown on copper foil (ACS Materials). A square of graphene on foil ~1 cm x 1 cm was cut out, and the polymer PMMA (MicroChem, 4 % 495PMMA in anisole) was spun onto the foil at 3k RPM for 60 s. Then the foil was baked at 90° for 60 s. On later samples the foil was treated PMMA-side facing down with oxygen plasma (50 W, for 60 s) to remove the layer of graphene on the backside of the foil. Then the PMMA-graphene-copper foil stack was placed PMMA-side up in copper etchant (CE200, Transene). The foil should float on the surface of the etchant, rather than being submerged. The stack is left until the copper foil is completely etched, leaving PMMA and graphene only; at room temperature, it is left overnight, or if the etchant is placed on a hotplate at 40° C, it is left for about one hour. The unpolished side of a Si wafer was used to transfer the PMMA-graphene stack. The stack was first transferred to a DI water bath. The wafer was rinsed, and the stack was immediately transferred to a fresh DI water bath and left for 15 minutes. The PMMA-graphene stack was transferred to another fresh DI water bath and left for two hours. The stack was transferred to fresh baths more times and left for a few hours each. Then the PMMA-graphene stack was scooped from the bath onto the wafer with the electrodes. The wafer was set underneath a crystallization dish to dry overnight. Next the PMMA is removed from the graphene by putting the wafer into a covered dish of acetone overnight.

Next the graphene is patterned into individual channels. AZ1512 is spun onto the wafer at 4k RPM for 30 s, then the wafer is hard baked at 110° C for 90 s. The photoresist was exposed under a contact aligner with an exposure dose of 40-60 mJ/cm^2 (2-3 s under a lamp with power~20 mW/cm^2). The wafer was then developed in a dish of AZ300 MIF developer (Integrated Micro Materials) with ample agitation for ~30 s, then put into a dish of DI water for 60 s and agitated. Then the wafer was triple-rinsed and dried with nitrogen (N_2).

For sandwich contacts, an additional round of photolithography was done to pattern the top layer of electrodes. The same photolithography procedure and photomask was used as for the first layer of electrodes. The metals deposited for the top layer were nickel (20 nm), followed by gold (40 nm).

For devices that were annealed, the annealing step was performed after the metal and graphene steps were completed. Devices were annealed in vacuum or in argon/hydrogen (1 SLM Ar/0.45 SLM H_2) for 60 minutes. Annealing temperatures of 300° C and 400° C were tested, and 300° yielded good results. The results of a 400° C anneal in Ar/H_2 are shown in Figure 2.2. The gold electrodes showed marks after annealing that may have been due to gases or other debris trapped underneath the gold erupting to the surface. Annealing at 300° C still gave the desired results of lowering the contact resistance, and the metal features did not get the marks. Electrical data for annealed vs non-annealed devices is shown in Section 3.5. Photopatterning the leads with SU-8 for wafers that require passivation is the final fabrication step. Details for SU-8 patterning are discussed in Section 4.3.1.

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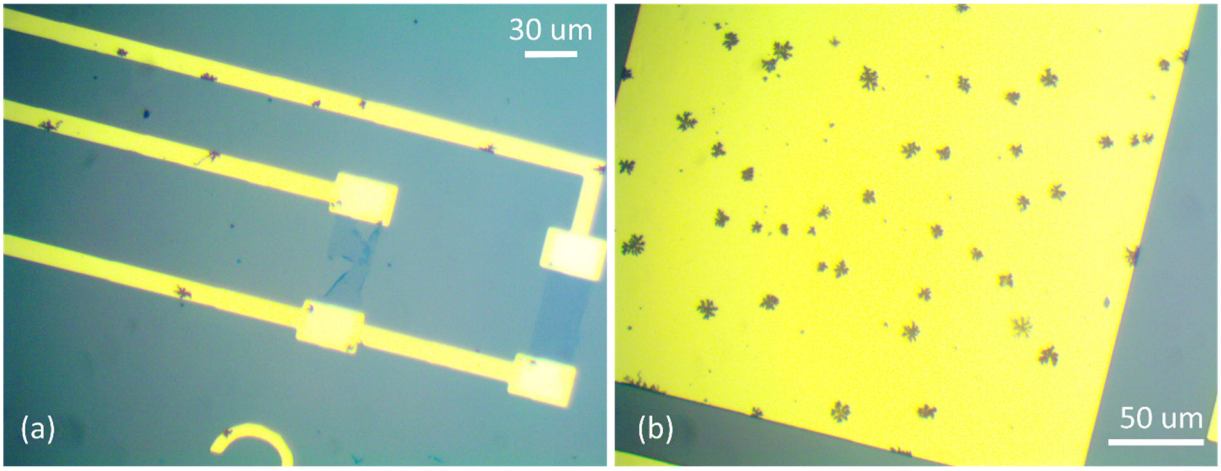

Figure 2.2: Devices annealed at 400° C. Optical images of (a) metal leads and (b) contact pads after annealing at 400° C. Imperfections introduced by the anneal can be seen on the metal.

2.1.2 Platinum Black Electrodes on Flexible Substrates

As a project independent from my graphene FET work, I fabricated platinum black electrodes on flexible polyimide substrates for a collaborator, Tal Sharf (UCSB). A photo of a completed device is shown in Figure 2.3a. The total device length is around 3". The sensing region contains 32 passive platinum black electrodes with a diameter of 30 μm each (shown in Figure 2.3b). The electrodes are attached by long leads along the flexible substrate to an Omnetics connector. The layers of the device are the polyimide base, the platinum leads and electrodes, then a top passivation layer of photopatternable polyimide.

The base layer of polyimide was formed by first adding VM650 primer (HD Microsystems) to a Si/SiO_2 wafer and letting it spread for about 30 s, then spinning at 4k RPM for 45 s. Then PI2611

polyimide precursor (HD Microsystems) was poured onto the wafer and spread around by tilting the wafer. Then the wafer was spun at 600 RPM for 30 s, then 1k RPM for 0 s, then 2k RPM for 30 s. The wafer was then baked on a hotplate at 170° C for 3 minutes. The process of adding, spinning, and baking PI2611 was repeated twice more to form a thicker total layer (about 27 μm). Then the wafer was baked in a tube furnace under nitrogen gas for 60 minutes at 350° C.

Next the platinum leads and electrodes were photopatterned. The same recipe was used as described for forming the metal leads on an SiO2 substrate. Electron beam deposition was used to deposit Cr (2 nm) and Pt (100 nm). Remover PG was used to remove the excess metal as detailed in the previous section.

Then the passivation layer of photopatternable polyimide was formed. The passivation layer had openings over the Pt electrodes, and at the other end at the pins for the Omnetics connector. The precursor HD4100 (HD Microsystems) was poured onto the wafer and spread across the entire surface with a plastic paddle. Then the wafer was spun at 1k RPM for 30s, followed by 2k RPM at 30 s, then 4k RPM for 30 s. The wafer was then baked at 90° C for 2 minutes, then baked at 110° C for 2 minutes. N2 was then blown over the wafer to cool it. Then the wafer was exposed on a contact aligner with an exposure dose of about 400 mJ/cm^2 (20 s under a 20 mW/cm^2 lamp) and let rest for 5 minutes. Next the wafer was baked on a hotplate at 80° C for 1 minute. Then the wafer was placed onto the spinner. Developer (PA401D, HD Microsystems) was puddled onto the surface and let sit for 60 s. Then the wafer was spun at 1k RPM, during which developer was sprayed at the wafer, then water was sprayed. The wafer was hard baked in the tube furnace under an inert nitrogen atmosphere at 350° C for 60 minutes.

Electroplating was performed to change the Pt electrodes into platinum black electrodes. Measurements performed at UCSB showed that the conversion from Pt electrodes to Pt black electrodes lowered the impedance from ~10 MΩ to ~20 kΩ.

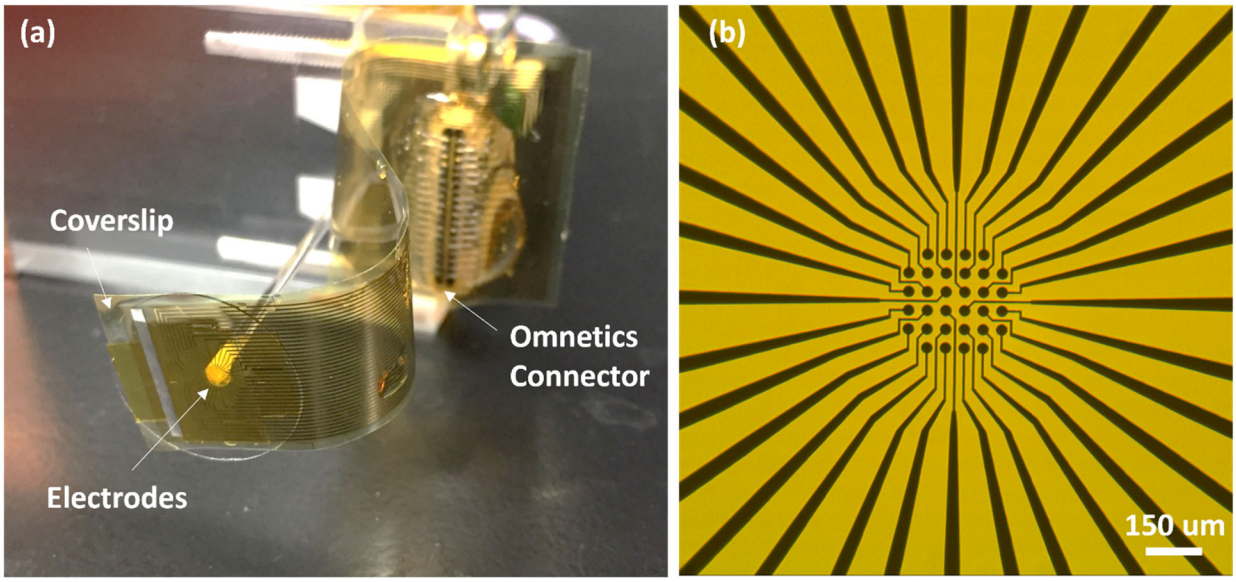

Figure 2.3: Flexible array of platinum black electrodes. (a) A completed device, connected to an Omnetics connector. The total length of the device is around 3". (b) An optical image of the platinum electrodes. The smallest feature is the 5 μm wide leads that connect to the circular electrodes.

2.2 Electrical Measurements with Graphene FETs

2.2.1 Characterization of Graphene FETs

The transfer curve, or IV_g curve, was collected for each tested device. The IV_g curve gives the transconductance dI/dV_g, which is needed to convert from change in current data to change in gate voltage data. The experimental setup is shown in Figure 2.4a. Before testing, ~200 μL of the gate electrolyte solution (either cell growth medium (DMEM) or a mixed salt solution with the same components as DMEM (81 mM NaCl, 44 mM $NaHCO_3$, and 5.3 mM KCl)) was added to the chip. A constant source drain bias in the range V_{sd} = 15 – 25 mV was applied across the graphene channel by the current amplifier or a signal generator (Rigol). The gate voltage V_g was applied to a Ag/AgCl electrode in the gate fluid by the DAQ and swept in 2 mV steps at a rate of 100 steps/s. A ~1 V wide range of V_g values was tested, centered around the Dirac point. The current was collected by a current amplifier (FEMTO DLPCA-200) with a variable gain (set to 10^6 V/A for most measurements). The voltage output from the current amplifier was read into a DAQ (National Instruments USB-6343) that interfaces with a Labview program (modified from the open-source Labview program called meaSureit) and was saved to a text file. An example of the raw IV_g data is shown in Figure 2.4b. The IV_g data was smoothed using a MATLAB script I wrote. First the current over multiple sweeps was averaged together. Then robust 2nd degree loess smoothing was applied; the smoothed IVg curve is shown in Figure 2.4c.

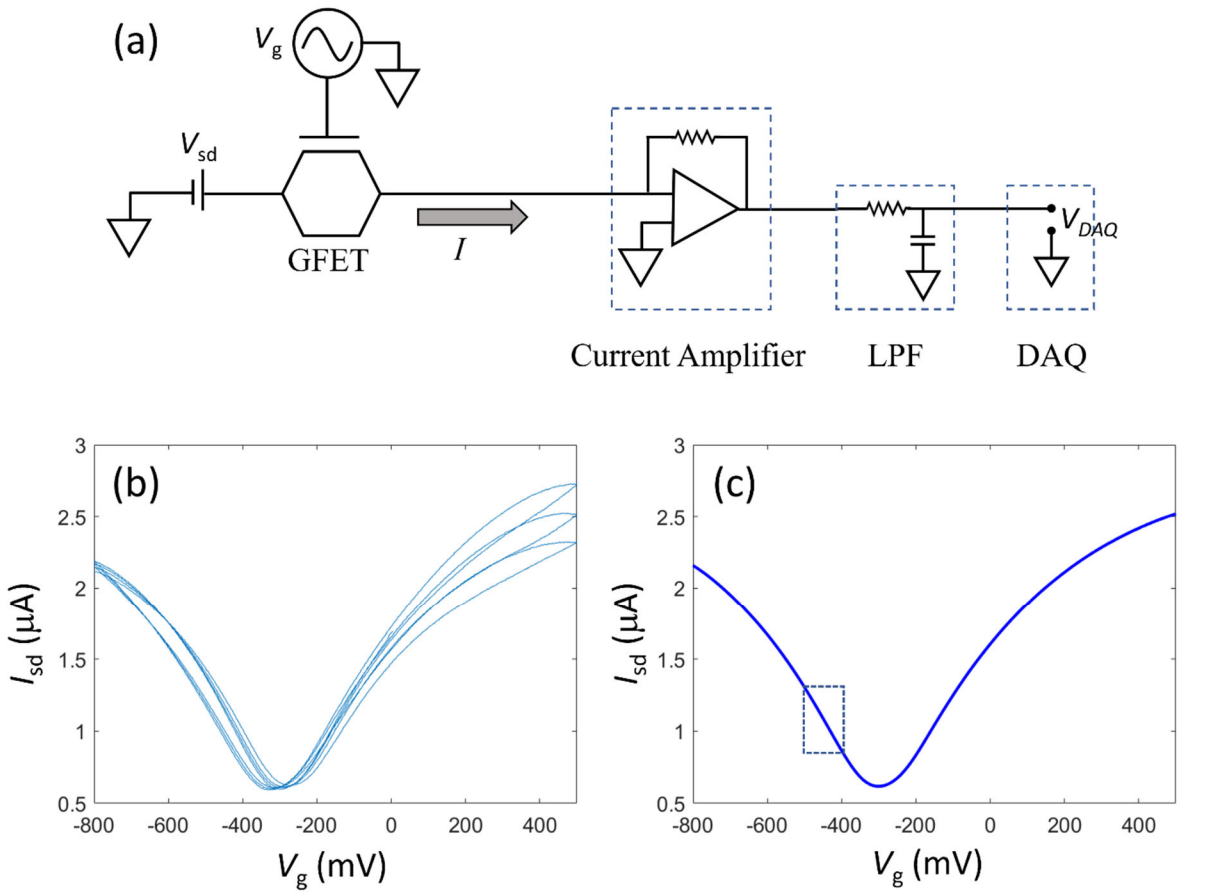

Figure 2.4: Electrical characterization of a graphene FET. (a) The measurement setup. (b) Raw data of the current I as a function of gate voltage V_g. Some hysteresis is present at high gate voltages. (c) Averaged and smoothed IV_g curve. A possible operating window is outlined with a dashed box.

The operating point chosen is where the transconductance g is constant for a window of at least 100 mV, and is large, such that a change in gate voltage from the signal source results in the largest change in channel current possible. For Figure 2.4c, an example of a good operating window is outlined in the dashed box. Therefore, the gate voltage of the gate electrode for this device would be set to -450 mV for a sensing experiment.

When studying the noise in the graphene FET or using it to sense changes in local gate voltages, the current as a function of time was collected at a fixed gate voltage. A sampling rate for the DAQ, $f_{sampling,}$ in the range 20kHz to 500kHz was chosen. For *in-vitro* work, long durations of time were typically recorded so a lower sampling frequency $f_{sampling}$ = 20 kHz – 35 kHz was selected to make manageable file sizes. For multiplexing work, $f_{sampling}$ must be at least two times the carrier frequencies used, as will be discussed in Chapter 4. Discussion on selecting $f_{sampling}$ for studying graphene FET noise is in the next section.

2.2.2 Measuring and Minimizing Measurement Noise in Graphene FETs

The noise in graphene FETs has a $1/f$ dependence (where f is the frequency). Power spectral densities (PSDs) show the frequency content of the signal in dimensions of power per frequency. PSDs are similar to Fourier transforms because both transform the time domain data to the frequency domain; however PSDs are preferred for systems with a degree of random noise, because they utilize smoothing and averaging that can minimize the random fluctuations[34]. In this thesis I use PSDs to look at the frequency domain information of current and voltage signals. The units of a PSD analyzing current data are A^2/Hz, while the units when analyzing a voltage are V^2/Hz. The integral underneath a PSD is the square of the RMS value. For example, the integral of the current noise PSD is I_{RMS}^2 for the integrated bandwidth.

To create a PSD, the current through the graphene FET was measured with a source-drain bias V_{sd} = 15-25 mV applied across the graphene channel, and the gate voltage V_g was set to a fixed value in the range -500 mV to 500 mV. The current from the graphene FET was amplified by a current amplifier, passed through an anti-aliasing filter (a passive RC low pass filter), and read into a DAQ (NI USB-6343). The current at a single V_g value was collected twice; once at a sampling frequency of $f_{sampling}$ = 20 kHz with a 4.8 kHz anti-aliasing filter, and once at $f_{sampling}$ = 200 kHz with a 48 kHz anti-aliasing filter. The current vs time data was then processed by a Welch PSD algorithm in Igor Pro graphing software or MATLAB to create a PSD plot, which shows the power in current fluctuations as a function of frequency.

The maximum frequency component that we can detect is half of the sampling frequency. In practice, the cutoff frequency of the anti-aliasing limits our measurement bandwidth further. The minimum frequency on the PSD is limited by the collection time and the segment size used by the Welch PSD algorithm. The segment size is inversely proportional to the frequency step size.

To measure fluctuations at low frequencies (1-100 Hz), data was collected at $f_{sampling}$ = 20 kHz for approximately 100 s. The window size for the Welsh PSD algorithm was 132,000 data points which gives a step size in the frequency domain of 1.5 Hz. To detect fluctuations at higher frequencies (100 Hz-10 kHz), 4 s of data is collected at $f_{sampling}$ = 200 kHz and processed with smaller window size (around 8,000 data points, with a resultant step size of 250 Hz). Combining the resulting PSD plots from the two data sets form a PSD that covers 4 orders of magnitude, 1 Hz - 10 kHz, which is the relevant frequency band for neurosensing.

Optimizing the measurement system and minimizing outside sources of noise makes it easier to analyze the frequency content of the graphene FET noise directly, and also lowers the overall RMS noise

of the device. Figure 2.5a shows two non-optimized measurements, and Figure 2.5b shows two optimized measurements. In Figure 2.5a, the 1/*f* noise of the graphene FET is visible at low frequencies. However, a multitude of spikes and a noise floor obscure the 1/*f* noise, especially at higher frequencies. The spikes can also contribute significantly to the total RMS noise. In Figure 2.5b, the 1/f noise is clear up to 10 kHz, and the noise spikes are minimal. Next, I'll discuss what is occurring in Figure 2.5a, and how it relates to the data collection methods used.

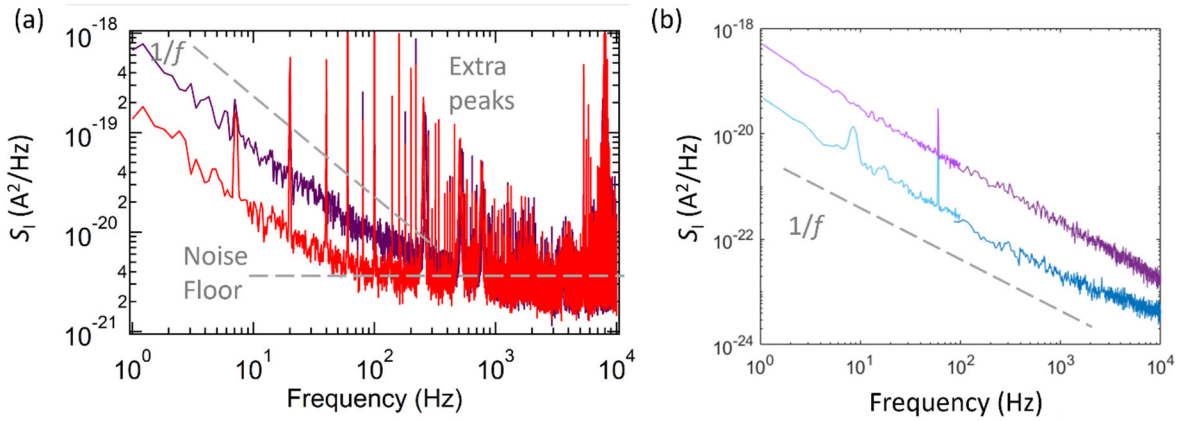

Figure 2.5: Current noise PSD of graphene FET in unoptimized and optimized system. (a) In an unoptimized system, aliasing from high frequency noise, as well as 60 Hz interference, obscures the 1/*f* device noise in the spectrum. (b) With proper filtering and shielding, the 1/*f* graphene FET noise is clear.

If the noise floor in Figure 2.5a was from the graphene FET itself, should shift as the current (or gate voltage) changes (as discussed in Section 3.2). Figure 2.5a shows the spectrum for two different gate voltages, and the noise floor stays constant regardless of V_g, which implies there is another cause. The current amplifier has a fixed noise floor; however, testing the current amplifier with a resistor equal in resistance to a graphene FET shows that the noise floor of the amplifier at the gain setting used to collect this data (=10^6) is 10^{-24} A^2/Hz, well below the floor observed in the measured data.

The floor in Figure 2.5a is created by aliasing. Aliasing is the folding of data from higher frequency bands onto lower frequency bands, and it occurs when an analog signal is sampled, and the analog signal contains significant frequency content larger than half the sampling frequency. Aliasing can result in skewed spectra and introduces noise from outside the band of interest into the sampled band. For a signal with a 1/*f* shape, aliasing causes an artificial noise floor as seen in Figure 2.5a. This effect can be recreated with simulated data. I wrote a MATLAB script (see Appendix B) to create data with a 1/*f* spectrum (4 s of data with T = 10 ns between data points, 1/T = 100 MHz). The spectrum of this data is shown in Figure 2.6a. Then I sampled that data at 100 kHz, with the resulting spectrum shown in Figure

2.6b. The data in the region greater than half the sampling frequency (i.e. all the data from 50 kHz up to 100 MHz) from the original signal was folded into the 0-5 kHz band of the sampled signal, so the shape of the spectrum is altered, and an artificial noise floor is created. Now instead of directly sampling the 100 MHz band data, first I applied a low pass filter with f_{LPF}= 40 kHz. Then I sampled the data at 100 kHz. The spectrum of the sampled filtered data is shown in Figure 2.6c.

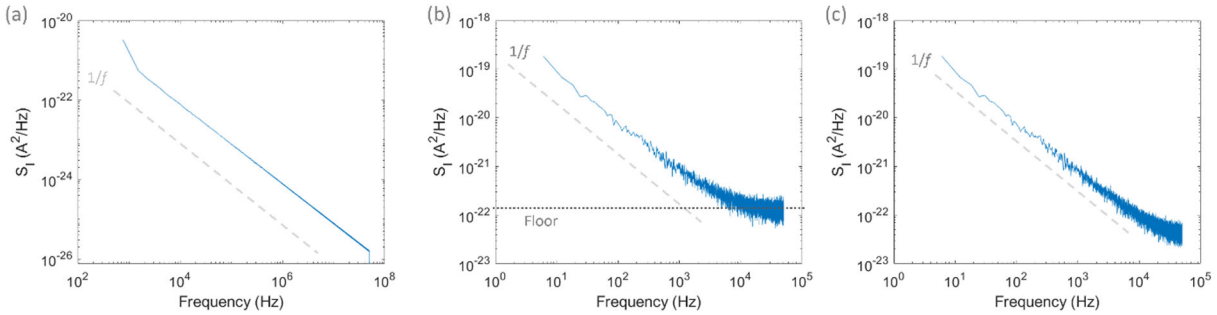

Figure 2.6: Simulated 1/f data and aliasing. (a) PSD of 1/*f* noise (the raw signal) generated with MATLAB. (b) The sampled signal with no filtering applied to the raw signal. (c) The sampled signal with a 40 kHz LPF applied to the raw signal prior to sampling.

This shows that the signal should be filtered with a LPF (i.e. anti aliasing filter) before sampling, and the cutoff frequency of the filter f_{LPF} should be greater than the signal band, but smaller than half the sampling frequency in order to prevent aliasing. Therefore $f_{signal}<f_{LPF}<f_{sampling}/2$. Adding an anti-aliasing LPF (home-built from a resistor and a capacitor) to our measurement setup before the data was sampled by the DAQ largely eliminated the artificial noise floor, as simulated in Figure 2.6c, and demonstrated experimentally in Figure 2.5b. There is a small flattening of the data at around 30 kHz in Figure 2.6c. This can be moved outside the window of interest by increasing both $f_{sampling}$ and f_{LPF}.

Another source of noise in the system was 60 Hz noise from the wall power and overhead fluorescent lights in the lab. To minimize interference, the wafer and the current amplifier were placed inside a shielded probe station. A low-ripple power supply was used for the current amplifier. All AC voltages inside the probe station (e.g. power strip) were unplugged during testing. The overhead fluorescent lights were turned off during testing, to prevent noise in the components outside the probe station (such as BNC cables and the DAQ). The 60 Hz peak in the noise spectrum is still present after these measures (in Figure 2.5b) but it is small and can be removed when digitally processing the signal.

2.3 Optical and AFM Images

Patterned graphene channels can be inspected with an optical microscope. Figure 2.7 shows the graphene channels of two completed devices on an Si/SiO2 substrate with 300 nm of oxide. Figure 2.7a has a channel that is mostly intact, while the channel in Figure 2.7b is significantly torn. The resistance of the device is relate to the channel condition; the intact channel has R = 6 kΩ, while the torn channel has R = 11 kΩ.

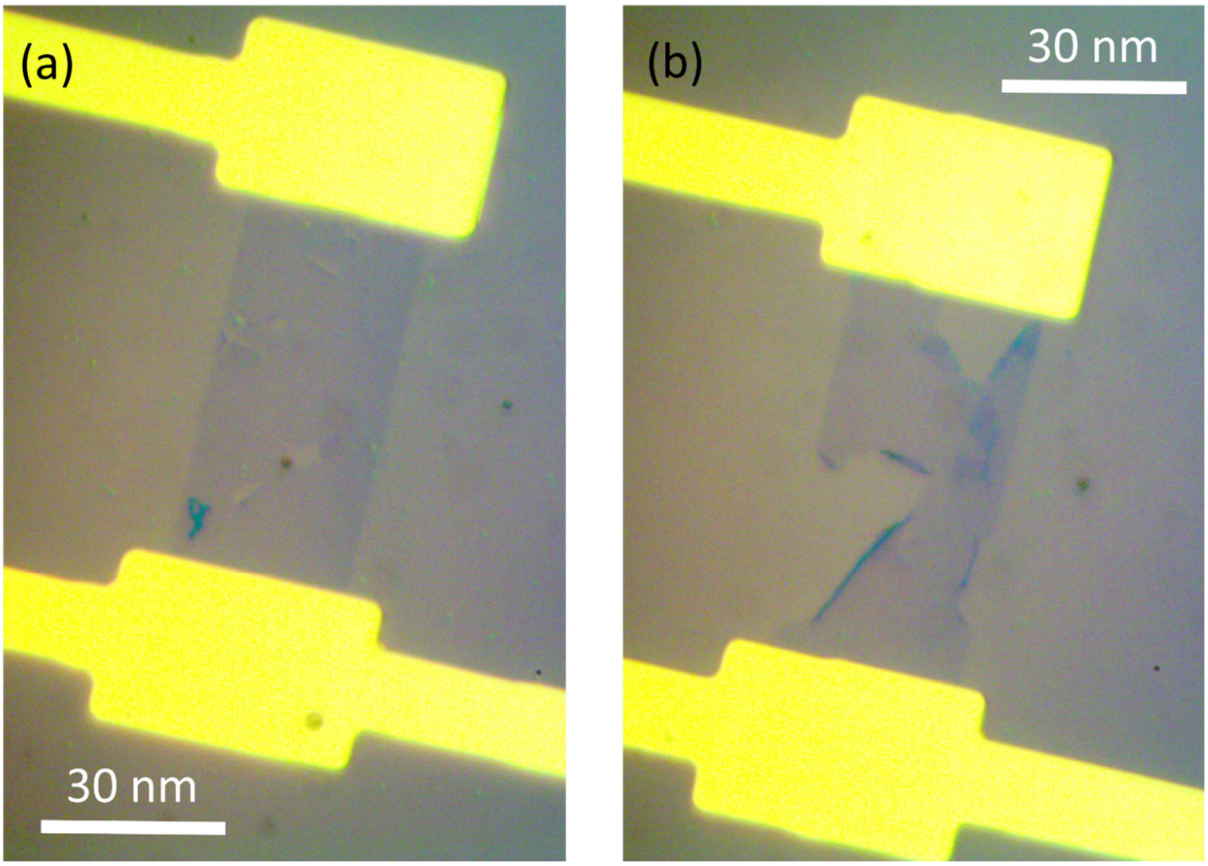

Figure 2.7: Optical images of graphene FETs. (a) A relatively intact channel. The source-drain resistance is about 6 kΩ. (b) A channel with significant tears. The resistance is about 11 kΩ.

Atomic force microscopy (AFM) is also a valuable tool for looking at the quality of the graphene surface. For example, Figure 2.8 shows a device before (a) and after (b) annealing. The profile data (taken along the red line) shows the thickness of the graphene channel region decreased to about 20% the original value after the anneal process. Furthermore, the surface roughness was decreases by 40% by the anneal.

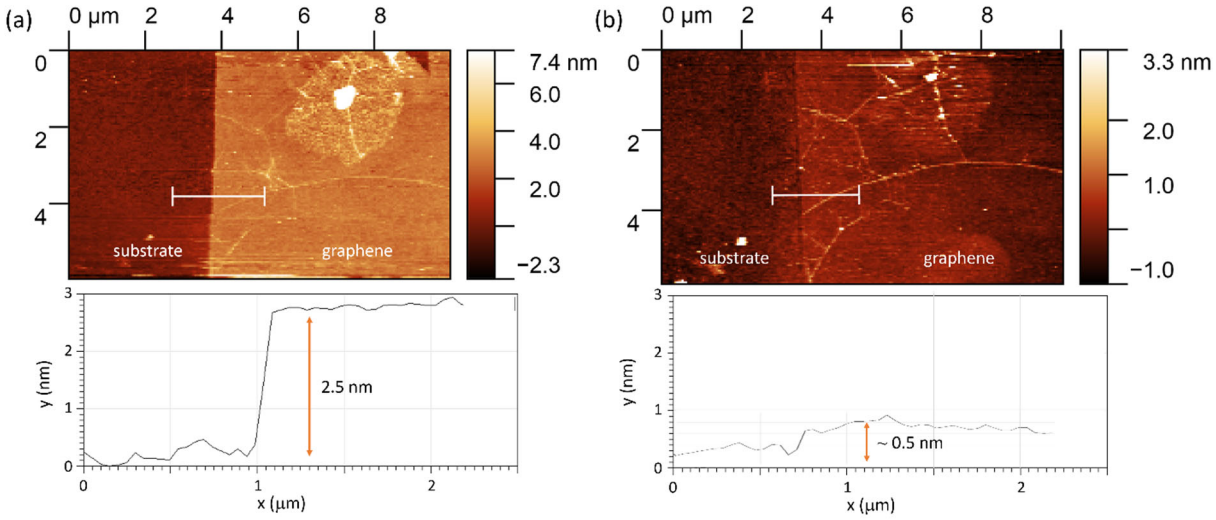

Figure 2.8: AFM of graphene channels. (a) Graphene channel before annealing. The thickness of the graphene was around 2.5 nm. (b) Graphene channel after annealing. The thickness was around 0.5 nm. The annealing process may have removed residues left over from the photopatterning process. The white line on each image indicates where the profile data (bottom) was collected from.

CHAPTER 3: ONE OVER F NOISE IN GRAPHENE FETS

3.1 Introduction

The signal-to-noise ratio (SNR) is an important metric when evaluating the performance of a sensor. This ratio consists of two parts: the signal size measured by the device, and the noise level of the device/measurement system. Ideally, the device will be operated in a regime where the noise of the instrumentation is negligible, and device noise behaves in a predictable manner. Let us examine the sources of noise in a graphene field-effect transistor (FET), and how they can be minimized.

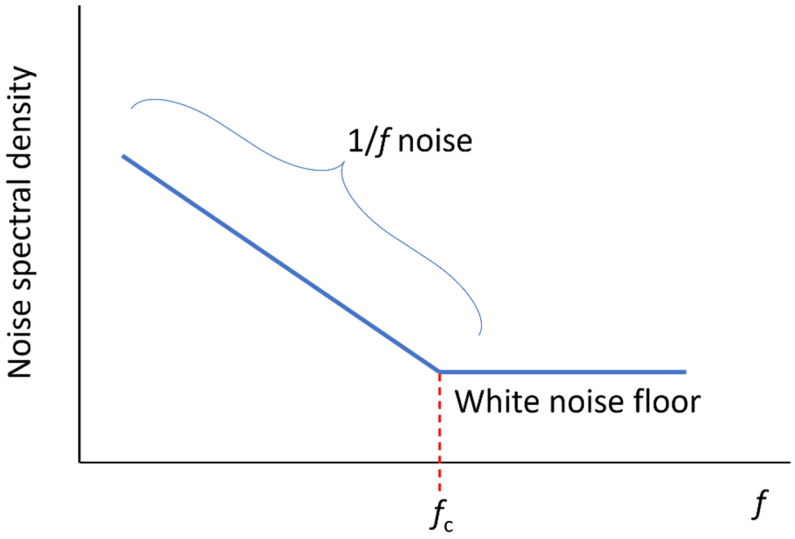

Figure 3.1: Log-log plot of noise spectral density as a function of frequency. The noise spectrum of graphene is made up of contributions from white noise sources (thermal and shot noise) and 1/*f* noise sources (such as generation-recombination noise). The 1/*f* noise dominates at low frequencies. The frequency at which these two types of noise are equal is called the corner frequency, f_c.

In general, the noise sources in a solution-gated graphene FET produce either a frequency-independent noise power spectrum (white noise), or a noise power spectrum with an inverse frequency dependence (1/*f* noise). The noise power spectrum observed in graphene FETs is a combination of both types of noise, as illustrated in the power spectral density (PSD) plot shown in Figure 3.1. Due to its inverse relationship with frequency, this type of noise will dominate at low frequencies, while white noise will dominate at high frequencies. The frequency at which the 1/*f* noise is equal to the white noise is the corner frequency, f_c. Typical sources of white noise are thermal (aka Johnson) noise and shot noise[35]. The 1/*f*-type noise sources include charge traps and fluctuations at the liquid gate-graphene interface[1]. The testing regime of graphene FETs is typically in the range of 1 Hz – 10 kHz, where 1/*f* noise is prevalent.

We will discuss sources of white noise in Section 3.2, and 1/*f* noise in Section 3.3. Experimental data from my devices is examined, and the corner frequency f_c is determined to be greater than 10 kHz. Therefore only 1/*f* noise is relevant in the frequency band of interest. Then, in Section 3.4, the device noise as a function of gate voltage is examined and compared to existing models. The models considered are McWhorter's model, the Hooge model, and the augmented charge noise (ACN) model. Our graphene FETs are best described by the augmented charge model, which indicates that the major sources of noise in our devices are from fluctuating charges coupling to the channel via the field effect and scattering in the graphene channel. The contact resistance is not considered in the ACN, and we estimate the functional form of the noise from the contact resistance to be ~I^2. The contact noise is relevant because it may increase the total magnitude of 1/*f* noise and cause a deviation from the ACN at high gate voltages. Early results from using annealing to reduce contact noise is shown.

3.2 White Noise

Several sources of white noise exist in a solution-gated graphene system. We can estimate the magnitude of the noise from each source using well-established models and compare to experimental data from my graphene FETs.

3.2.1 Shot Noise

Shot noise is caused by the fluctuations in the number of charge carriers passing between the source and the drain in the FET. At frequencies and temperatures relevant to biosensing it is typically only a small contribution to the total device noise. To estimate the magnitude of the shot noise in a graphene FET, we can use the equation

$$S_I = 2e\langle I\rangle F, \tag{3.1}$$

where e is the electron charge, $\langle I\rangle$ is the average current, F is the Fano factor, and S_I is the current noise power. The Fano factor was found to be $F \approx 0.36$ for single layer graphene at $T = 0.3$ K[36]. The average current can be written in terms of the resistance R (which includes the channel resistance and the contact resistance) and the source drain bias V_{sd} as $\langle I\rangle = V_{sd}/R$ so

$$S_I = \frac{2eFV_{sd}}{R}. \tag{3.2}$$

S_I can be estimated with representative values for our graphene FET (R = 6 kΩ and V_{sd} = 25 mV) to be

$$S_{\mathrm{I}} = \frac{2(1.6 \text{ x } 10^{-19}\mathrm{C})(0.36)(25\mathrm{mV})}{6 \text{ x } 10^{3}\Omega},$$

$$S_{\mathrm{I}} = 5 \times 10^{-25}\mathrm{A}^2/\mathrm{Hz}\,.$$

This is constant across all frequencies.

Shot noise has been measured in graphene FETs at high frequencies (> 1 MHz) and low temperatures (< 5 K), where thermal and 1/*f* noise is low and transport is near-ballistic[36,37]. The shot noise was measured to be ~10^{-24} A^2/Hz, similar to our prediction[37]. In systems at room temperature, scattering processes suppress the shot noise. Graphene FETs for biosensing applications are operated at biological temperatures and the relevant frequency band is 1 Hz – 10 kHz, so shot noise is negligible.

3.2.2 Thermal Noise

Thermal noise is noise due to the random motion of charges within the materials. The noise power in the voltage across an element, S_{V}, is given by

$$S_{\mathrm{V}} = 4k_{\mathrm{b}}TR, \tag{3.3}$$

where k_{b} is Boltzmann's constant, T is the temperature and R is the resistance of the system. In our work we measure current as opposed to voltage. To convert from voltage noise S_{V} to current noise S_{I} one must use the relationship between changes in the current in the channel and changes across the element that is the source of the voltage noise. For thermal noise in the graphene channel, the noise power in the current S_{I} is given by

$$S_{\mathrm{I}} = S_{\mathrm{V}}\left(\frac{dI}{dV_{\mathrm{sd}}}\right)^2 = S_{\mathrm{V}}\left(\frac{1}{R}\right)^2, \tag{3.4}$$

$$S_{\mathrm{I}} = \frac{4k_{\mathrm{b}}T}{R}. \tag{3.5}$$

Here the resistance R is a function of the gate voltage V_{g}. Note the similarity between Equation 3.2 and 3.5 when $eV_{\mathrm{sd}} \sim k_{\mathrm{b}}T$. Setting R = 6 kΩ, the noise power due to thermal noise is

$$S_{\mathrm{I}} = \frac{4(25 \text{ meV})(1.6 \text{ x } 10^{-22}\,\frac{\mathrm{J}}{\mathrm{meV}})}{6 \text{ x } 10^{3}\Omega},$$

$$S_{\mathrm{I}} = 3 \times 10^{-24}\mathrm{A}^2/\mathrm{Hz}.$$

This noise is constant across all frequencies. Operating at a higher resistance point (further from the Dirac point) can decrease thermal noise in the channel. Operating at lower temperatures also reduces this noise but when used in biosensing applications the temperature range is limited to biological temperatures.

3.2.3 Comparison to our Graphene FETs

The equations in the previous subsections let us predict the white noise floor for the power spectral density (PSD) plots for our graphene FETs. A generalized PSD for a graphene FET is shown in Figure 3.1.

The PSDs of the current in two of my graphene FETs are shown in Figure 3.2. The device in figure 3.2a has a graphene area of 30 μm x 30 μm, has sandwich contacts, and was annealed in vacuum (see Section 2.1.1 for fabrication details). The device in Figure 3.2b has single layer contacts and was not annealed. The procedure for collecting the relevant data and making a PSD plot are discussed in Section 2.2.2. Briefly, a DC V_{sd} was applied across the graphene and the current through the graphene at a fixed V_{g} was measured as a function of time. The current as a function of time was collected for several different values of V_g for each device to give insight into how the noise changes with gate voltage (as will be discussed in section 3.4). The current vs time data was then processed by a Welch PSD algorithm in Igor Pro graphing software or MATLAB to create a PSD plot, which shows the power in current fluctuations as a function of frequency.

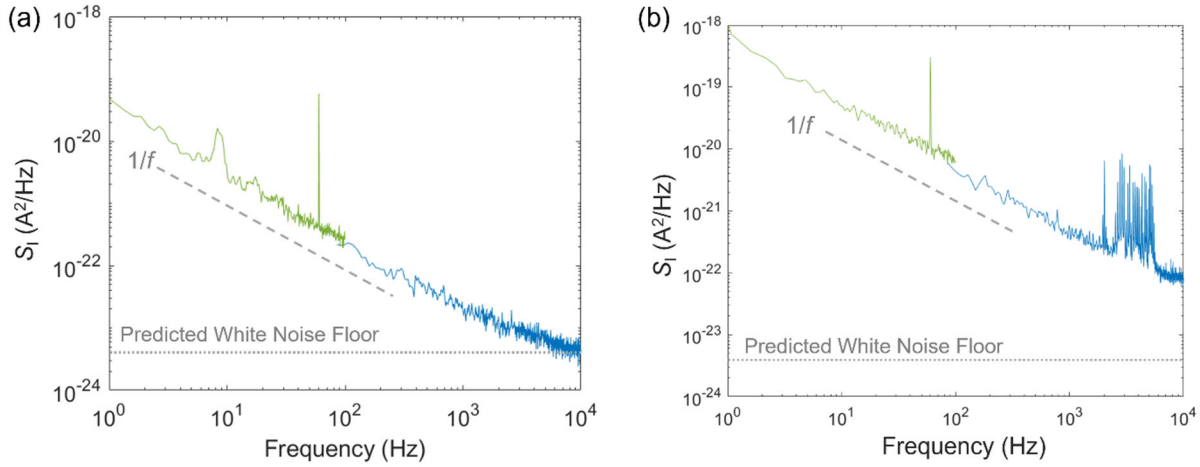

Figure 3.2: Current noise spectrum of two graphene FETs. A 1/*f* dependence is observed at low frequencies. The predicted white noise floor for each is labeled with a dotted line. A tall 60 Hz peak is present on both spectra due to electrical interference. (a) The resistance of the device is R = 12.5 kΩ, and the source-drain bias is V_{sd} = 16.5 mV. (b) A different device with R = 5.2 kΩ, and V_{sd} = 19.4 mV.

In Figure 3.2a and b, the slopes of S_I are consistent with a 1/*f* dependance, and the 1/*f* region extends to at least 10 kHz, thus f_c > 10 kHz. The spectra both have a peak at 60 Hz, due to electrical interference from wall power. There are also peaks starting around 2 kHz from an undetermined source in Figure 3.2b.

The sum of the shot noise power (Equation 3.2) and the thermal noise power (Equation 3.5) predicts the total of the white noise power as a function of R and V_{sd}. For the device in Figure 3.2a, R = 12.5 kΩ and V_{sd} = 16.5 mV, resulting in a predicted noise power of $S_I = 4.4 \times 10^{-24}$ A^2/Hz (labeled on the figure with a horizontal dashed line). For the device in Figure 3.2b, R = 5.2 kΩ and V_{sd} = 19.4 mV, so the equations predict $S_I = 4.2 \times 10^{-24}$ A^2/Hz. The predicted noise floor for both devices is below the minimum value of 1/*f* noise observed in the data, so in the bandwidth of interest (1 Hz – 10 kHz) 1/*f* noise is relevant while white noise is not.

The RMS current noise can be calculated from the integral of the PSD for the bandwidth f_1 to f_2 as

$$I_{\mathrm{RMS}}{}^2 = \int_{f_1}^{f_2} S_I \, df. \tag{3.6}$$

If the bandwidth is completely within the 1/*f* noise region of the frequency spectrum (as in Figure 3.2) the integral can be written as

$$I_{\mathrm{RMS}}{}^2 = \int_{f_1}^{f_2} \frac{A{I_\mathrm{o}}^2}{f}\,df, \tag{3.7}$$

where A is a unitless constant and I_o is the DC current. Completing the integral,

$$I_{\mathrm{RMS}}{}^2 = A \ln\left(\frac{f_2}{f_1}\right) {I_\mathrm{o}}^2. \tag{3.8}$$

The noise I_{RMS} is related to the bandwidth and the constant A, called the noise parameter. Looking ahead to Chapters 4 and 5, the resolution of the gate voltage signal will be relevant, and the RMS gate voltage noise is related to the RMS current noise by the transconductance dI/dV_g such that

$$V_{\mathrm{G,RMS}}{}^2 = A \ln\left(\frac{f_2}{f_1}\right) \frac{{I_\mathrm{o}}^2}{\left(dI/dV_\mathrm{g}\right)^2}. \tag{3.9}$$

The noise parameter A is relevant when characterizing the noise level of a graphene FET. Measuring and modeling A will be discussed in the next sections.

3.3 Introduction to 1/*f* Noise

Flicker noise, or 1/*f* noise, is important to biosensing experiments with graphene FETs because it is the dominant form of noise in the frequency band relevant to biosensing (1 Hz – 10 kHz). The 1/*f* dependence appears whether looking at current noise power S_I, resistance noise power S_R, or conductance noise power S_G. The normalized noise spectra are equivalent in that[38]

$$\frac{S_I}{I^2} = \frac{S_R}{R^2} = \frac{S_G}{G^2} = \frac{A}{f}. \tag{3.10}$$

Here, I is the current, R is the resistance, and G is the conductance. The noise parameter A measures the relative noise of the system[38], as

$$A \propto \frac{\delta I^2}{I^2}, A \propto \frac{\delta R^2}{R^2}, A \propto \frac{\delta G^2}{G^2}. \tag{3.11}$$

A is independent of the source-drain bias and allows for easy comparison of the noise amplitude of many different systems.

Models for 1/f noise will be discussed in Section 3.4. Some predict the value of A, such as the Hooge model and McWhorter's model. Other models, like the augmented charge noise model make predictions for the current noise power S_I as a function of frequency. Note that these different views are reconcilable because the noise parameter A is related to the current noise power at 1 Hz, S_I(1 Hz), by

$$A = \frac{S_I(1\text{ Hz})}{I^2}. \tag{3.12}$$

The noise parameter for a single device is a function of the gate voltage V_g because both S_I and I change with V_g. For practical use, the most important value of A is at the operating V_g, though looking at A as a function of V_g can reveal information about the source of the 1/f noise, which will be discussed in Section 3.4. The Garrido group recently published their work[39] with solution-gated flexible graphene transistors with a noise parameter A on the order of 0.8 – 1.2x10^{-9} for devices of area of 80 μm x 30 μm.

I can determine A in my own devices by calculating the current noise PSD and fitting the 1/f region with a line. Then S_I(1 Hz) is found from the fitted line, as shown in Figure 3.3. The current I is the average of the current vs time data collected to calculate the PSD. Then the noise parameter A is then found using Equation 3.12. For my devices, $A \sim 10^{-8}$ at the operating point, with $A = 5 \times 10^{-9}$ for the best device. The device area is 20 μm x 50 μm, or 20 μm x 30 μm. When comparing A between different devices, it is important to account for device size because 1/f noise is expected to scale inversely with device area. A model to demonstrate why 1/f noise scales with device size is discussed in the next section.

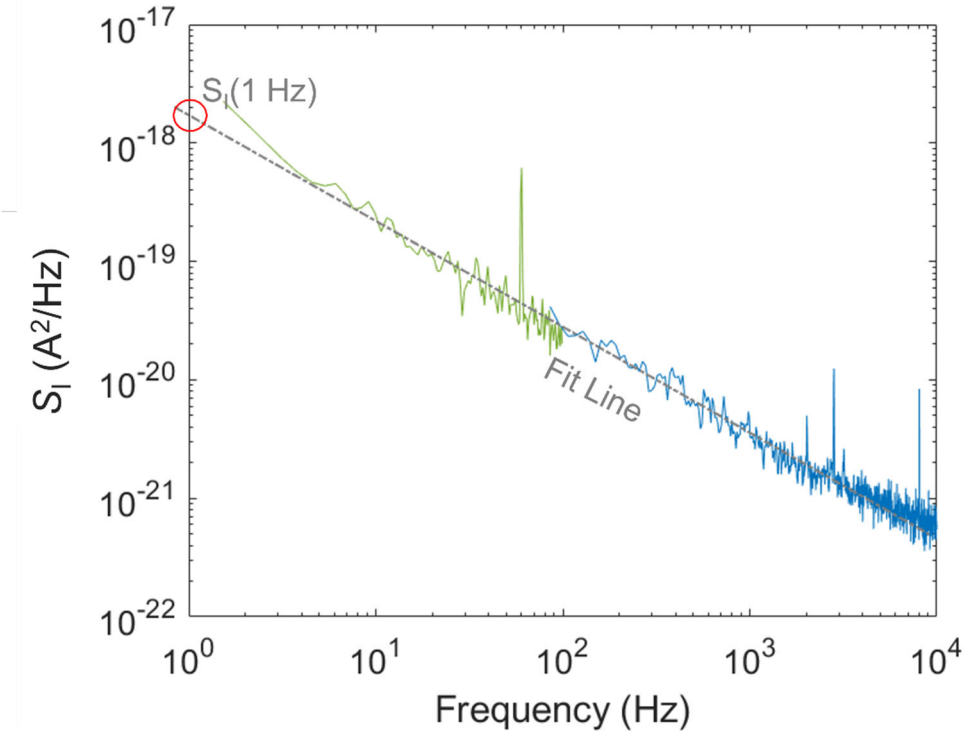

Figure 3.3: Determining S_I(1 Hz) from a PSD. The loglog plot of a PSD is fit by hand with a straight line. The noise power at 1 Hz can be estimated from where the line intersects $f = 1$ Hz. In this case, S_I(1 Hz) $\approx 1.8\text{x}10^{-18}$ A^2/Hz.

3.3.1 Scaling of Noise Parameter with Device Area

A simple way to explain the relationship between the noise parameter A and device area is that the larger the graphene is, the more likely it is that resistance fluctuations in one area of the graphene are canceled out by resistance fluctuations in another area. To quantify this intuition, consider a distributed element model of a piece of graphene as N resistors in series, each with average resistance R. The resistance of each resistor can fluctuate; say the smallest unit of fluctuation is δR, and a resistor can add or remove δR from its total resistance at each time step. The sum of the N resistors can be treated like a random walks with N steps. The RMS fluctuation of the sum is $\sqrt{N}\delta R$. Then the proportional change in the resistance due to these fluctuations is

$$\frac{R_{RMS}}{R_{total}} = \frac{\sqrt{N} \times \delta R}{NR}, \tag{3.13}$$

$$= \frac{1}{\sqrt{N}} \frac{\delta R}{R}. \tag{3.14}$$

The relative RMS resistance fluctuation is inversely proportional to $\sqrt{N}$, where N is proportional to the length of the graphene sheet.

A similar argument can be applied when treating the graphene as a network of N resistors in parallel. The analysis is more straightforward when looking at the conductance G of each resistor. The total conductance of the network is NG. The conductance of each resistor can fluctuate, with the smallest unit of fluctuation being δG. Treating each resistor as a random walk, the RMS conductance fluctuation is $G_{RMS} = \sqrt{N}\delta G$. The relative RMS conductance fluctuation is then

$$\frac{G_{RMS}}{G_{total}} = \frac{\sqrt{N} \times \delta G}{NG}, \tag{3.15}$$

$$= \frac{1}{\sqrt{N}} \frac{\delta G}{G}, \tag{3.16}$$

where N is proportional to the width of the graphene sheet. The noise parameter A is proportional to the square of a relative fluctuation as stated Equation 3.11, so Equations (3.14)3.14 and 3.16 show that A is inversely proportional to the area of the graphene sheet.

We can account for the effects of device area by multiplying the noise parameter A by device area. The noise parameter multiplied by device area for graphene FETs from several research groups (about 50 total data points) was calculated in a review paper by Balandin[35]. Despite the different fabrication techniques and device sizes featured, all fell within one order of magnitude (A × Device Area = 10^{-7} – 10^{-6} μm^2). I estimated Garrido's devices[39], which are 80 μm x 30 μm, to have A x Device Area = 2 x 10^{-6} to 3 x 10^{-6} μm^2. In my 20 μm x 50 μm devices, most had A × Device Area ~ 10^{-5} μm^2, with the best device at 5 x 10^{-6} μm^2. In my annealed devices with Ni sandwich contacts that were 20 μm x 30 μm in area, a slight improvement was observed with A × Device Area = 2.5 x 10^{-6} μm^2. My best devices have a normalized noise parameter that is less than an order of magnitude larger than those in Balandin's paper, and about the same as Garrido's devices. The difference in noise between my non-annealed and annealed/sandwich contact devices is likely related to contact resistance, as discussed in Section 3.5. First, we'll discuss the lower bound of 1/f noise specific to liquid gated graphene FETs, which is thermal noise at the interface between the gate liquid and the graphene.

3.3.2 Thermal Noise in Graphene-Gate Interface

Thermal fluctuations of charges at the liquid-graphene interface couple to the graphene channel through the field effect, and are a fundamental limit to graphene FET noise[1]. To estimate the noise due to these thermal fluctuations, we use the change in current through the graphene channel per change in gate voltage, dI/dV_g, to convert S_V to S_I

$$S_I = S_V \left(\frac{dI_{sd}}{dV_g}\right)^2, \tag{3.17}$$

$$S_I = 4k_b T Z_{Re} \left(\frac{dI_{sd}}{dV_g}\right)^2. \tag{3.18}$$

To estimate this, we need to know the resistance across the interface Z_{Re}. A paper from our group published in 2015[1] examined the impedance across this interface in a solution-gated graphene FET and found that the real component of the impedance (i.e. the resistance) of the interface had a frequency dependence $1/(f)^p$, where $p \approx 1$. This gives the current noise power a $1/f$ dependence.

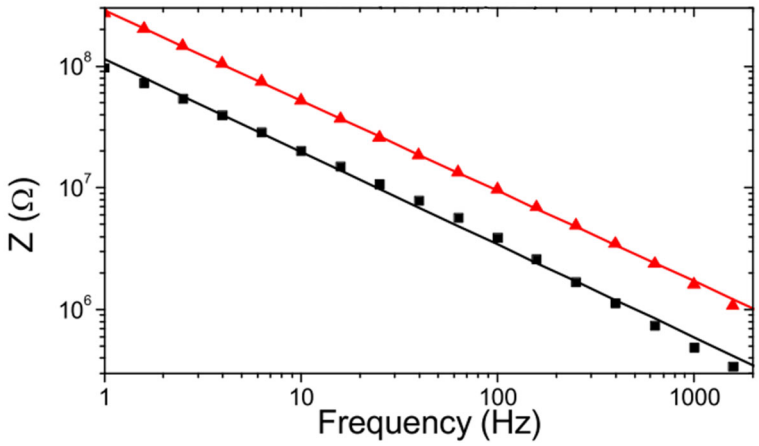

Figure 3.4: Real and imaginary components of the impedance Z across graphene-electrolyte interface. The red triangles and the black squares represent the measured imaginary and real components of impedance, respectively, for a device with an area of 5000 μm^2. The solid lines are fits to the raw data. Adapted from Ref. [[1]] with permission.

The impedance measurement is a function of the size of the devices. Z_{Re} (and thus S_V) are inversely proportional to device area[1]. Figure 3.4 shows the impedance components for a device with area 5000 um^2. Our devices have an exposed area of 1000 μm^2, so by scaling the values on the above plot by we can get an estimate for Z_{Re} for our devices. At 1 Hz, we estimate $Z_{Re} \approx 500$ MΩ. We can use this value

to estimate the thermal noise boundaries due to the gate-graphene interface. The voltage noise power at 1 Hz is found using Equation 3.4

$$S_{\mathrm{V}} = 4(25\mathrm{meV})\left(1.66 \times 10^{-22}\frac{\mathrm{J}}{\mathrm{meV}}\right)(5.0 \times 10^{8}\ \Omega),$$

$$S_{\mathrm{V}} = 8.0 \times 10^{-12}\, V^2/Hz.$$

From Equation 3.17, the current noise power at 1 Hz is then

$$S_{\mathrm{I}}(1\ \mathrm{Hz}) = S_{\mathrm{V}}\left(\frac{dI}{dV_{\mathrm{g}}}\right)^2,$$

$$S_{\mathrm{I}}(1\ \mathrm{Hz}) = \ (8.0 \times 10^{-12}\ \mathrm{V}^2/\mathrm{Hz})(1 \times 10^{-5}\ \mathrm{A/V})^2,$$

$$S_{\mathrm{I}}(1\ \mathrm{Hz}) = 8.0 \times 10^{-22}\mathrm{A}^2/\mathrm{Hz}.$$

In my devices under similar testing conditions, I found that $S_{\mathrm{I}}(1\ \mathrm{Hz}) \sim 10^{-20}$-$10^{-19}\ \mathrm{A}^2/\mathrm{Hz}$. The noise in my devices is greater than the thermal limit; the additional noise is likely due to fluctuations in the number of charge carriers or carrier mobility.

3.3.3 Charge-trap 1/*f* Noise

The generation/recombination of charges due to charge traps creates noise in the current in the graphene FET. When a charge is captured or released by a trap, both the number of charge carriers N_c and the mobility μ can change. The current I is proportional to $qN_c\mu$, and fluctuations in N_c and μ can cause noise in the current.

Fluctuations in the number of charge carriers N_c are caused by charges from the graphene channel entering or leaving trap states. Fluctuations in N_c can also be caused by capacitive coupling between charge in the graphene and a fluctuating trapped charge. Fluctuations in μ can be caused by changes in the scattering cross-section of traps in the graphene channel[40]. The scattering cross-section of a trap can be affected by charges entering and leaving the trap.

Fabrication and materials quality play a role in the value of the 1/*f* noise and noise parameter A, due to their relation to charge trap density and lattice defects. A 2010 paper showed an order of magnitude difference in current noise between suspended graphene devices and non-suspended devices[41], which could indicate interactions with charge traps in the substrate as a cause of noise.

3.4 Models for 1/*f* Noise in Graphene FETs

Flicker noise is prevalent in many types of electronic systems[42], and several models have been developed to explain its origin and to relate it to know quantities. Some models consider fluctuations in N_c as the dominant noise source, such as the augmented charge noise model and McWhorter's model, while other models consider primarily fluctuations in μ, such as the Hooge model. In both cases, a 1/*f* noise spectrum is predicted. We find that the augmented charge noise model best describes the noise in my graphene FETs.

3.4.1 McWhorter's Model

McWhorter's model[43] predicts that the noise parameter A is inversely proportional to the square of the charge carrier density n

$$A \propto \frac{1}{n_c^2}. \tag{3.19}$$

While this model is not a good fit for graphene FETs (as will be discussed in the next section, see Figure 3.4), it does experimentally fit many conventional semiconductor devices[35,40]. McWhorter's model attributes 1/*f* noise to fluctuations in the number of charge carriers due to charge trapping in surface states[43], and thus sees it as a surface phenomenon.

3.4.2 Hooge's Model

In the Hooge model, the source of flicker noise is attributed to fluctuations in mobility, and is thought to be a bulk phenomenon, with the noise parameter A given by

$$A = \frac{\alpha_H}{N_c}, \tag{3.20}$$

where α_H is Hooge's noise parameter. Hooge's noise parameter is relatively constant for a fixed device geometry, though variations in the quality of fabrication and/or materials can cause variations in α_H[44]. While some carbon nanotube and graphene FETs show noise patterns in good agreement with the Hooge model[44–46], other seemingly similar systems do not[47,48]. For 2D materials, a reassuring feature of the Hooge model is the scaling of A with the device area. Larger area devices have more charge carriers and therefore lower A. This trend is consistent with experiments on 2D materials.

I fit my data with the Hooge model. To determine the relationship between the noise amplitude A and the number of charge carriers in the graphene, I measured A at various values of V_g as discussed in section 3.3. To relate V_g to N_c, I used the results from a paper I coauthored in 2019 where the charge carrier density n in electrolyte-gated graphene FETs as a function of gate voltage was determined using the Hall effect[49]. Briefly, the system was modeled as two capacitors in series, with quantum capacitance C_Q and electric double-layer capacitance C_{DL}, respectively. The voltage drop across these capacitors equals the gate voltage V_g minus the Dirac voltage V_o,

$$|V_g - V_o| = |V_Q| + |V_{DL}|. \tag{3.21}$$

The voltage drop across the electric double layer is given by

$$|V_{DL}| = \frac{Q}{C_{DL}} = \frac{en}{C_{DL}}, \tag{3.22}$$

where n is the carrier density. In the single carrier regime, the quantum capacitance is shown to be

$$C_Q = e^2 \hbar v_f \sqrt{\pi(n - n^*)}, \tag{3.23}$$

where n^* is related to the spatial inhomogeneity of the charge density in the graphene[49]. This results in

$$|V_Q| = \frac{\hbar v_f}{e} \sqrt{\pi(n - n^*)}. \tag{3.24}$$

Therefore, the gate voltage is related to the charge carrier density as follows

$$|V_g - V_o| = \frac{\hbar v_f}{e} \sqrt{\pi(n - n^*)} + \frac{en}{C_{DL}}. \tag{3.25}$$

In the paper this model was fit to experimental data. It was found that $v_f = 1.2 \times 10^6$ m/s, and the value of the double layer capacitance C_{DL} depends on the anion in the electrolyte used for gating (but not the concentration). The electrolyte I used to gate my devices is a mixture of salts in concentrations similar to cell growth medium, with the major component being sodium chloride. Therefore, I used the C_{DL} value for NaCl found in the paper, which is $C_{DL} = 0.094$ F/m^2. Lastly the paper was able to determine n^* from Hall voltage curves, finding $n^* = 4.4 \times 10^{15}$ m^{-2}. We now have all the parameters to estimate the

concentration of charge carriers from the gate voltage. The charge carrier concentration is then related to the number of charge carriers N_c by device area.

I fit my experimental data to find the noise amplitude A as a function of gate voltage (see Figure 3.5). I then converted the axis from gate voltage to number of charge carriers N_c to see if the Hooge model fits my data, i.e. if A is inversely proportional to N_c.

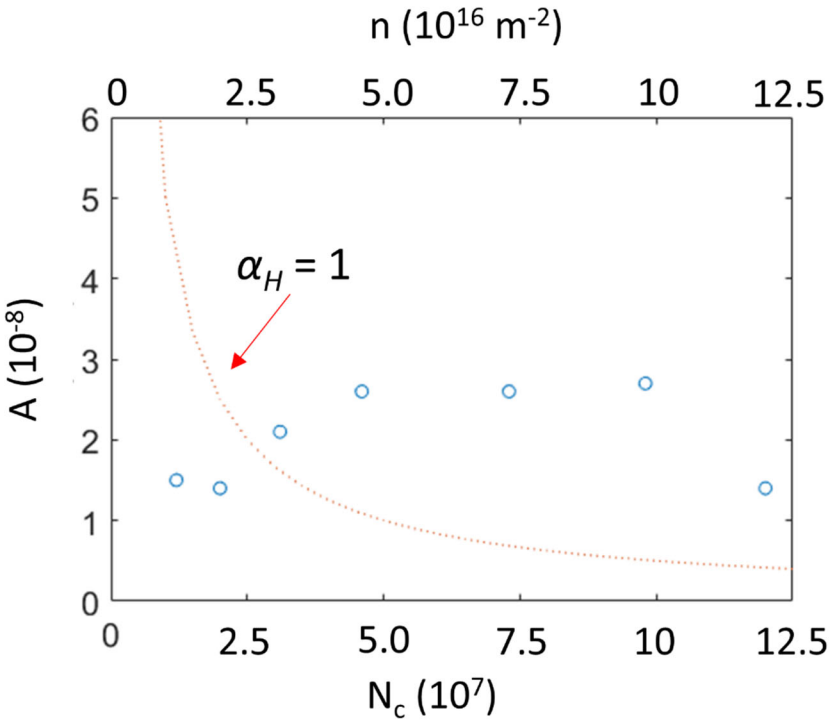

Figure 3.5: Noise amplitude *A* as a function of carrier number N_c. The Hooge model predicts the noise amplitude to be inversely proportional to the number of charge carriers. My experimental data is shown with open blue circles, while the Hooge model is the red dashed line. Hooge's noise parameter α_H was set to 1.

The Hooge model does not describe the noise seen in my graphene devices, particularly around the Dirac point. A study of liquid-gated graphene FETs by Heller et al[47]. found an alternative model, called the augmented charge noise model[48], to be a better fit for this system.

3.4.3 Augmented Charge Noise Model

Heller et al. studied the current noise in liquid-gated graphene FETs with surface area < 10 μm^2. Their work found that S_I closely follows a $1/f$ trend in the frequency band of 1 - 100 kHz[47]. They

determined that the device area and gate voltage play an important role in the total noise in the system, and found that the augmented charge noise (ACN) model[48] can be used to describe this noise. According to the ACN model, the current noise power S_I at 1 Hz is given by

$$S_I(1\text{ Hz}) = S_{\text{input}}\left(\frac{dI}{dV_g}\right)^2 + \alpha_s I^4. \tag{3.26}$$

Tersoff first developed the ACN model to describe the current noise in ballistic carbon nanotube (CNT) FETs[48]. The main source of noise in his CNT FETs was the Schottky barriers formed at the high-resistance contact/nanotube interface, and so the channel resistance was initially treated as negligible. The height of the Schottky barriers is controlled by the electric field at the contact. The major source of electric field at the contact is the applied gate voltage V_g. The field due to the gate is approximately $E_g = V_g/S_g$, where S_g is a parameter related to the gate oxide thickness and is proportional to the subthreshold slope of the device. Fluctuations of charges in the gate oxide create an additional electric field at the contact. This field is modeled $\delta E = \gamma F(t)$, where $F(t)$ is a unitless function that has a $1/f$ power spectral density and an average value of zero, and γ is a parameter that is related to the oxide quality and reflects charge trap density and the proximity of traps to the contact. The total electric field at the contact then is $E_{\text{contact}} = E_g + \delta E = V_g/S_g + \gamma F(t)$.

Tersoff realized that this system could be modeled as a device where the current fluctuations were caused by noise in the gate voltage. The noisy gate voltage V_g' could then be written as $V_g' = V_g + \delta V_g$, with $\delta V_g = S_g \gamma F(t)$. The current through the FET would be given by

$$I = I_o(V_g) + \delta V_g \frac{dI}{dV_g}, \tag{3.27}$$

$$I = I_o(V_g) + S_g \gamma F(t) \frac{dI}{dV_g}. \tag{3.28}$$

The noise spectrum due to this current would have a $1/f$ shape due to the characteristics of $F(t)$, and the noise amplitude is related to the amplitude of $F(t)$, namely $S_g\gamma(I/dV_g)$. The power spectral density for this current is given by

$$S_{\mathrm{I}}(f) = \frac{1}{f} {S_{\mathrm{g}}}^2 \gamma^2 \left(\frac{dI}{dV_{\mathrm{g}}}\right)^2. \tag{3.29}$$

The noise parameter A_{SB} is then

$$A_{\mathrm{SB}} = \frac{{S_{\mathrm{g}}}^2 \gamma^2}{I^2} \left(\frac{dI}{dV_{\mathrm{g}}}\right)^2. \tag{3.30}$$

Note that the noise parameter A_{SB} can be related back to the resistance fluctuations in and the total resistance of the Schottky barrier similarly to Equation 3.11

$$A_{\mathrm{SB}} = \frac{{\delta R_{\mathrm{SB}}}^2}{{R_{\mathrm{SB}}}^2} \cong \frac{{\delta R_{\mathrm{SB}}}^2}{{R_{\mathrm{Total}}}^2}. \tag{3.31}$$

Here $R_{\mathrm{Total}} \cong R_{\mathrm{SB}}$ since it is assumed the channel resistance $R_c << R_{SB}$. Tersoff found that this noise model agreed well with experimental data from a CNT ballistic FET[48]. Note that the current noise power here has the same dependence on the square of the transconductance as the thermal gate noise developed by Crosser et al.[1] due to the fact that it is caused by charge fluctuations coupling to the channel via the field effect. In the ACN model the source of these fluctuations is unspecified, though it may be from the gate oxide, while Crosser studied thermal fluctuations of charges at the liquid gate-graphene interface.

Tersoff further developed the model to include the non-ballistic case, i.e. where the channel resistance is not negligible compared to the Schottky barriers, by adding an additional noise term to describe channel noise. The channel is represented by a constant series resistance R_c with noise parameter A_c, such that

$$\frac{S_{\mathrm{R}}}{{R_{\mathrm{c}}}^2} = \frac{A_{\mathrm{c}}}{f}, \tag{3.32}$$

where S_R is the resistance noise power of the channel resistance. It was assumed the channel was short enough and the V_g testing window small enough that the dependence of the channel resistance on the gate voltage was negligible compared to the Schottky barrier gate dependence. This assumption is questionable for the graphene FETs I use because the channel resistance changes approximately 3-fold in the V_g testing window. Moreover, the contact resistance is a similar order of magnitude as the channel resistance.

The total noise parameter A for the device is

$$A = \frac{\delta R_{\mathrm{SB}}{}^2 + \delta R_{\mathrm{c}}{}^2}{(R_{\mathrm{SB}} + R_{\mathrm{c}})^2}, \tag{3.33}$$

where R_{SB} and δR_{SB} are the Schottky barrier resistance and Schottky barrier resistance fluctuation, respectively, and R_{c} and δR_{c} are the channel resistance and channel resistance fluctuation, respectively. This can be rewritten as the sum of the noise parameters from the individual sources (the Schottky barrier and the channel) as

$$A = A_{\mathrm{SB}} + A_{\mathrm{c}} \left(\frac{R_{\mathrm{c}}}{R_{\mathrm{c}} + R_{\mathrm{SB}}} \right)^2, \tag{3.34}$$

where we earlier showed $A_{\mathrm{SB}} = \delta R_{\mathrm{SB}}{}^2/(R_{\mathrm{SB}} + R_{\mathrm{c}})^2$ as the noise parameter of the Schottky barrier by itself and A_{c} is the noise parameter of the channel resistance by itself as shown in Equation 3.32 and, equivalently,

$$A_{\mathrm{c}} = \left(\frac{\delta R_{\mathrm{c}}}{R_{\mathrm{c}}} \right)^2. \tag{3.35}$$

The second term of Equation 3.34 can be written in terms of the current through the device, $I = V_{\mathrm{sd}}/(R_{\mathrm{c}}+R_{\mathrm{SB}})$. Then we have

$$A = A_{\mathrm{SB}} + A_{\mathrm{c}} \left(\frac{R_{\mathrm{c}}}{V_{\mathrm{sd}}} \right)^2 I^2. \tag{3.36}$$

Tersoff assumed that $A_{\mathrm{c}}(R_{\mathrm{c}}/V_{\mathrm{sd}})^2$ would stay approximately constant, therefore, he defined

$$\alpha_{\mathrm{c}} = A_{\mathrm{c}} \left(\frac{R_{\mathrm{c}}}{V_{\mathrm{sd}}} \right)^2, \tag{3.37}$$

such that the total noise parameter can be written as

$$A = A_{\mathrm{SB}} + \alpha_{\mathrm{c}} I^2, \tag{3.38}$$

$$A = \frac{{S_g}^2 \gamma^2}{I^2}\left(\frac{dI}{dV_g}\right)^2 + \alpha_c I^2. \tag{3.39}$$

Note that the constant α_c is a function of V_{sd} (Equation 3.37) and the noise parameter (Equation 3.35) cannot be improved by using V_{sd} to lower I. From Equation 6 we can find the current noise power of this system.

$$S_I = \frac{1}{f}\left({S_g}^2 \gamma^2 \left(\frac{dI}{dV_g}\right)^2 + \alpha_c I^4\right). \tag{3.40}$$

The first term of the Equation 3.40 is the charge noise term, while the second term is referred to as the series resistance or channel resistance term. The charge noise term in the model is the noise due to random fluctuations in the environment coupling to the device via the field effect, which is why the transconductance dI/dV_g is a factor in this term. These fluctuations can be associated with the liquid gate-graphene interface, and/or the oxide substrate beneath the graphene. The channel noise term is due to scattering in the graphene channel.

Heller et al. used this model to describe the noise in their solution-gated graphene FETs, with $S_{input} = {S_g}^2\gamma^2$. Interestingly, they did not comment on the assumptions made by Tersoff in the development of the model, particularly how the terms map from the context of CNT FETs with Schottky barriers to the context of graphene FETs, which have no Schottky barriers. Tersoff created the first term to describe the noise at the contact (Schottky barrier), while the second term described the noise in the channel. In contrast, when applied to a graphene FET the dependence of the first term on the transconductance dI/dV_g indicates that this term is related to coupling of fluctuating charges to the graphene channel, while the second term is likely related to the contact resistance of the device. Further support for this view is given by the 1/(device area) dependence of the first term as discussed later in this section. These ideas are still under development.

The charge noise term is largest in the regions to the left and right of the Dirac point, where the transconductance dI/dV_g is largest and it goes to zero at the Dirac point. From Equation 3.33, the charge noise term will dominate for devices with high contact resistance and when the gate voltage V_g far from the Dirac point ($R_{contact} >> R_c$) while the channel resistance term will dominate for devices with high channel resistance. Our devices have $R_{SB} \approx R_c$ so we must consider both terms.

Other physical factors also play an important role in the size of the two terms. For example γ reflects the density of charge traps in the gate, and an ultra-clean or suspended device could result in a lower charge noise term[41]. Device dimensions in terms of the charge noise term were discussed earlier but are worth revisiting here. To analyze the role of device dimensions it is helpful to rewrite the ACN model as Heller et al did for the case of a liquid-gated graphene FET. Recall the ACN can be expressed as:

$$S_I = S_{input}\left(\frac{dI}{dV_g}\right)^2 + \alpha_c I^4. \tag{3.41}$$

We can use Heller's results to estimate values for S_{input} and α_c and then use Equation 3.41 to fit data from our devices. The coefficient on the first term, S_{input}, represents the power of the voltage noise due to nearby fluctuating charges that couple to the channel via the field effect. In terms of the gate capacitance C_g, we can write

$$S_{\text{input}} = S_q\left(\frac{1}{C_{\text{gate}}}\right)^2, \tag{3.42}$$

where S_q is the power of charge fluctuations (with units of C^2/Hz). If we assume that the fluctuating charges are uniformly distributed, then S_q is proportional to the area of the graphene channel. The gate capacitance C_g is also proportional to area. This determines that S_{input} is inversely proportional to area. Heller et al[47] established area-normalized constants for single layer and bilayer graphene FETs. Defining $S_{\text{input}} = \xi/Area$, they found $\xi = 0.11$ +/- 0.01 $\mu m^2 mV^2/Hz$ for single layer graphene FETs. This allows us to estimate $S_{\text{input}} = 2.8 \times 10^{-10}$ V^2/Hz for our devices with an area of 1000 μm^2. The charge noise term for our devices is predicted to be:

$$S_{\text{input}}\left(\frac{dI}{dV_g}\right)^2 = 2.8 \times 10^{-10}\,\frac{V^2}{Hz}.$$

The constant on the second term in Heller's ACN model, α_c, is related to the channel noise parameter A_c $(= (\delta R_c/R_c)^2)$ and the channel resistance R_c by:

$$\alpha_c {V_{sd}}^2 = A_c {R_c}^2. \tag{3.43}$$

As A_c is proportional to 1/(device area) and R_c is proportional to (device length)/(device width), the quantity $\alpha_s V_{sd}^2$ is proportional to (device length)/(device width)^3. Heller et al. experimentally verified this

proportionality between $\alpha_s V_{sd}^2$ and (device length)/(device width)^3 over three orders of magnitude of the latter.

For the channel resistance term in the ACN model, we can use Heller's results to find $\alpha_c V_{sd}^2$ for our device dimensions, which are W = 20 μm and L = 50 μm. This gives L/W^3 = 6.25 x 10^{-3} μm^{-2}. Note that this value of L/W^3 is about 2 orders of magnitude smaller than any single layer graphene FETs measured by Heller. If we assume the trend on the plot continues to smaller values of L/W^3 we can estimate $\alpha_c V_{sd}^2 \approx 6 \times 10^{-3}\ \Omega^2/\text{Hz}$. We use $V_{sd} \approx 25$ mV, so $\alpha_c \approx 10\ A^{-2}\ Hz^{-1}$. Therefore, the channel noise at 1 Hz for our devices is predicted to be

$$\alpha_c I^4 = \left(10\ \frac{1}{A^2 Hz}\right) I^4. \tag{3.44}$$

I fit my data with the augmented charge noise model. I calculated the current noise power at 1 Hz as discussed in section 3.2.3 at 9 different gate voltages. I chose only V_g values greater than V_{Dirac}, as Heller saw different fit parameters were needed to describe the n-doped region and the p-doped region. This same analysis can also be applied to the region $V_g < V_{Dirac}$.

To utilize the augmented charge noise model, I needed to know the current I and the transconductance dI/dV_g at various gate voltage values. I took a transfer characteristics curve to obtain this information. Figure 3.6a shows the transfer curve for the tested device (gate voltage step = 2 mV). The x-axis has been shifted such that the Dirac point lies at x = 0. Loess smoothing was used to remove noise in the curve and enable a reasonably smooth derivative to be calculated. Loess is a smoothing process that locally fits second-order polynomials. Figure 3.6a shows the raw data (in blue) and the loess data (red). The overall shape of the IVg curve was maintained in the post-smoothing curve. The inset of Figure 3.6a is zoomed in to a small region to show the local results of the loess function. Figure 3.6b shows the numerical derivative of the smoothed transfer curve, calculated using the centered differencing formula.

I wrote a MATLAB script to calculate S_I based on the augmented charge noise model. The current and transconductance were taken from the data set in figures 3.6a and 3.6b at each gate voltage, and the parameters S_{input} and α_c were hand-adjusted to get a close fit to the measured values. The measured data and the model are plotted together in Figure 3.6c.

The best-fit value of S_{input} was very similar to that predicted by Heller's data (same order of magnitude). The value of α_c was different by two orders of magnitude than predicted. The values used to estimate α_c assumed the trend Heller experimentally confirmed between α_c and (length)/(width)^3

continued outside the range they tested by two orders of magnitude. The assumption could be incorrect leading to an incorrectly predicted α_c.

For gate voltages close to the Dirac point, the model fits the data well. The parameter S_{input} is approximately zero, which implies the charge noise contribution is relatively low compared to the noise from scattering in the graphene channel. This result is in contrast with Heller's work, which showed a strong dependence on the charge noise term[47]. This is in part due to the large area of the graphene device I used (area = 1000 μm^2) when compared to those used by Heller (area < 10 μm^2), since charge noise is inversely related to device area. At high gate voltages the experimental data deviates from the ACN model. Other devices (N = 9) were tested, and the general shape of S_I vs V_g was the same, with good agreement to the charge noise model at low gate voltages and deviations at higher gate voltages. At high gate voltages, the graphene resistance becomes small relative to the contact resistance in our devices, which may explain the deviation from the ACN. In the next section I will model the graphene FET system as the contact resistance and the channel resistance in series to explore how the contact resistance affects the predictions for A.

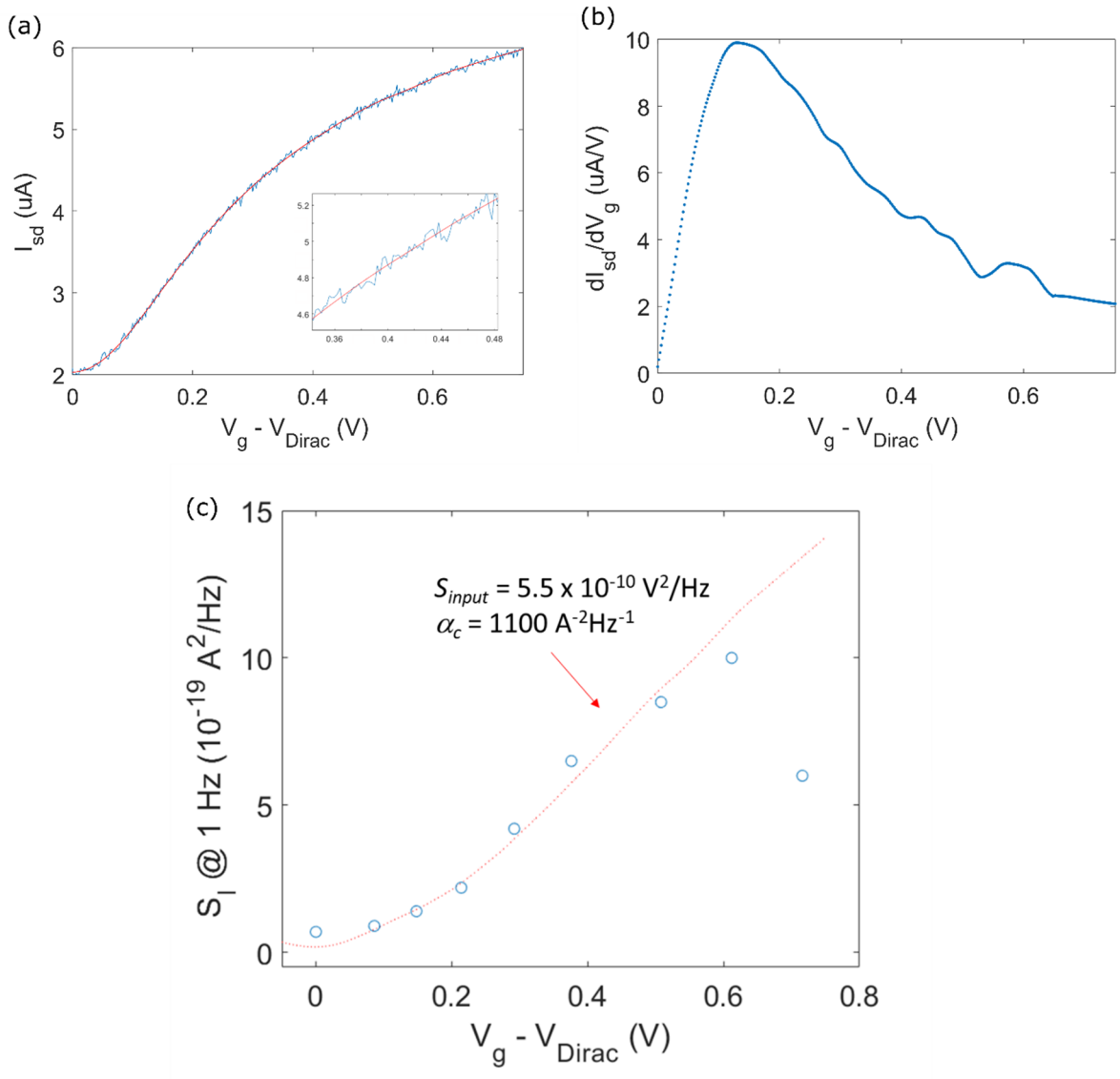

Figure 3.6: Applying the augmented charge noise model to my data. (a) The raw transfer characteristics curve in blue, with the smoothed curve in red. The overall shape was maintained in the smoothed data. The inset is a close-up of the curves. V_{sd} = 20 mV. (b) The numerical derivative of the smoothed IV_g plot. (c) The model is the red dashed line, and the experimental data is open circles. The parameters chosen for the fit are included. There is good agreement between the data and the model in the region near V_g-V_{Dirac} = 0.

3.4.4 Deriving the Noise Parameter with Contact Resistance

The contact resistance was not considered in the ACN. To see what effect it has on the noise parameter, a simple model of the graphene channel and the gold-graphene contacts as two resistors in series can be used. The total noise of the system (channel plus contacts) can then be determined by considering the noise in the two resistors. The noise parameter for a classical resistor is given by[48]

$$A = \frac{\delta R^2}{R^2}, \tag{3.45}$$

where R and δR are the resistance and the RMS resistance fluctuation, respectively. The noise parameter due to the gold-graphene contacts A_{con} is

$$A_{\mathrm{con}} = \frac{\delta {R_{\mathrm{con}}}^2}{{R_{\mathrm{con}}}^2}. \tag{3.46}$$

We expect this noise parameter to be independent of the applied gate voltage. The noise parameter for to the graphene channel is

$$A_{\mathrm{gr}} = \frac{\delta {R_{\mathrm{gr}}}^2}{{R_{\mathrm{gr}}}^2}. \tag{3.47}$$

The graphene resistance R_{gr} is a function of the applied gate voltage V_{g}. The resistance fluctuations δR_{gr} are due to voltage fluctuations in the gate δV_{g}. These voltage fluctuations couple to the graphene channel via the field effect. This relationship is

$$\delta R_{\mathrm{gr}} = \delta V_{\mathrm{g}} \frac{dR_{\mathrm{gr}}}{dV_{\mathrm{g}}}. \tag{3.48}$$

I would like to rewrite $dR_{\mathrm{gr}}/dV_{\mathrm{g}}$ in terms of the transconductance dI/dV_{g}. The relationship between these quantities is

$$\frac{dI}{dV_{\mathrm{g}}} = \frac{d}{dV_{\mathrm{g}}}\left(\frac{V_{\mathrm{sd}}}{R_{\mathrm{gr}} + R_{\mathrm{con}}}\right) \tag{3.49}$$

w*here* V_{sd} is constant. The derivative can be found using the chain rule

$$\frac{dI}{dV_{\mathrm{g}}} = V_{\mathrm{sd}}\left(\frac{-1}{\left(R_{\mathrm{gr}} + R_{\mathrm{con}}\right)^2}\right)\frac{dR_{\mathrm{gr}}}{dV_{\mathrm{g}}}, \tag{3.50}$$

$$= I^2 \left(\frac{-1}{V_{\mathrm{sd}}}\right) \frac{dR_{\mathrm{gr}}}{dV_{\mathrm{g}}} \tag{3.51}$$

where $R_{\mathrm{total}} = R_{\mathrm{gr}} + R_{\mathrm{con}}$. Therefore Equation 3.48 in terms of dI/dV_{g} is

$$\delta R_{\mathrm{gr}} = \delta V_{\mathrm{g}} \left(\frac{-V_{\mathrm{sd}}}{I^2}\right) \frac{dI}{dV_{\mathrm{g}}} \tag{3.52}$$

The noise parameter for the graphene channel can then be rewritten as

$$A_{\mathrm{gr}} = \frac{\delta {V_{\mathrm{g}}}^2}{{R_{\mathrm{gr}}}^2} \frac{{V_{\mathrm{sd}}}^2}{I^4} \left(\frac{dI}{dV_{\mathrm{g}}}\right)^2 \tag{3.53}$$

The noise parameter for the system is equal to the sum of the noise parameters of the individual resistors weighted by the square of the proportion of the individual resistance to the total resistance

$$A = A_{\mathrm{con}} \frac{{R_{\mathrm{con}}}^2}{{R_{\mathrm{total}}}^2} + A_{\mathrm{gr}} \frac{{R_{\mathrm{gr}}}^2}{{R_{\mathrm{total}}}^2} \tag{3.54}$$

with $R_{\mathrm{total}} = R_{\mathrm{con}} + R_{\mathrm{gr}}$.

Substituting Equations 3.46 and 3.53 into 3.54 we get

$$A = \frac{\delta {R_{\mathrm{con}}}^2}{{V_{\mathrm{sd}}}^2} I^2 + \frac{\delta {V_{\mathrm{g}}}^2}{{I_{\mathrm{sd}}}^2} \left(\frac{dI}{dV_{\mathrm{g}}}\right)^2 \tag{3.55}$$

This has a very similar form to Tersoff's augmented charge noise (ACN) model in Equation 3.48; one term is proportional to the square of the current, while the other is proportional to the square of the transconductance. However, there are differences in the interpretation. Specifically, in the augmented charge noise the I^2 term was due to the scattering in the graphene channel, while in Equation 3.55 this term is due to the contact noise. The dI/dV_{g} term in Tersoff's ACN model of CNT FETs refers to noise at the contact, while in Equation 3.55 this term is noise due to charge fluctuations coupling to the graphene channel, which matches Heller's interpretation of the ACN for graphene FETs. These differences in interpretation may be because the ACN model was developed for CNT FETs with large contact resistances and the assumption that in the range of gate voltages tested the channel resistance was not a function of V_{g}.

In the V_{g} regime far from the Dirac point the total resistance R_{total} approaches the contact resistance, and the transconductance dI/dV_{g} to approach zero, so we'd expect the first term in Equation 3.55 to dominate such that

$$A \cong A_{\mathrm{con}} \frac{{R_{\mathrm{con}}}^2}{{R_{\mathrm{total}}}^2} \cong A_{\mathrm{con}} \tag{3.56}$$

The parameter A_{con} is constant as defined by Equation 3.51. Therefore, at gate voltages where $R_{gr} << R_{contact}$ (i.e. far from the Dirac point), the total noise parameter A may approach a constant. This more closely matches the behavior observed in my graphene FETs at high gate voltages compared to the ACN, which predicts that A continues to increase as shown in Figure 3.6.

3.5 Methods for Reducing Noise

Because the contact resistance contributes to device noise, particularly at high carrier concentrations, lowering the contact resistance can reduce $1/f$ noise[40,50]. Studies have shown the current transfers through the edge of the graphene, not the full area[51]. Bonds formed between the metal and dangling bonds on the graphene edge decrease the contact resistance[52]. To determine that bonds were formed, a Raman spectrum was collected at the interface between a graphene edge and nickel, before and after annealing. The peak corresponding to defects (like dangling bonds) in the graphene decreased after annealing, implying bond formation. The contact resistance decreased by approximately 50% after annealing. Nickel and cobalt readily form bonds with the graphene edges upon annealing[52], as does palladium[53], so these are ideal metals to use for the contacts. Increasing the perimeter of graphene in contact with the metal[50,54], treating the graphene contact region with O_2 plasma[55] or ultra-violet ozone (UVO)[56], and using sandwich contacts, and all have shown to decrease the contact resistance. In the UVO-treated devices, the contact resistance decreased about 50% for devices 5 μm in length, but little improvement was observed in devices 40 μm long. Similarly, the RMS gate noise improvement was significant for 5 μm channels and not significant for 40 μm channels.

I investigated how the noise changed with annealing and using sandwich contacts with Ni. The fabrication procedure was detailed in Chapter 2. Briefly, metal electrodes and leads were photopatterned on an Si/SiO_2 wafer. The metals (Cr, 4 nm, and Au, 40 nm) were deposited with electron beam deposition. Graphene was transferred to the wafer and patterned using photolithography and oxygen plasma. The graphene area exposed to electrolyte was 20 μm x 30 μm, and the overlap area between the graphene and the source/drain contacts was 20 μm wide x 15 μm long. A second layer of electrodes was patterned and deposited on top of the first layer, sandwiching graphene between the two layers. For the top layer, Ni (20 nm) and Au (4 nm) was used. The nickel was deposited first so it contacts the graphene directly. Some devices were annealed in vacuum at 300° C, some were annealed in Ar/H_2 at 300° C, and

some were not annealed. Lastly SU-8 was added to passivate the leads and form a hydrophobic ring to hold the electrolyte.

The results for non-annealed, vacuum annealed, and Ar/H_2 annealed devices are shown in Figure 3.7. Two devices of each type were tested. This result shows that A of the annealed devices is lower by up to two orders of magnitude than those of the non-annealed devices. However, compared to devices from previous fabrication runs with a single layer contact (i.e. not sandwich contacts) and no annealing, the noise improvement with annealing is marginal (about a factor of 2 improvement) when device area is accounted for. A larger sample size is necessary to better quantify this effect.

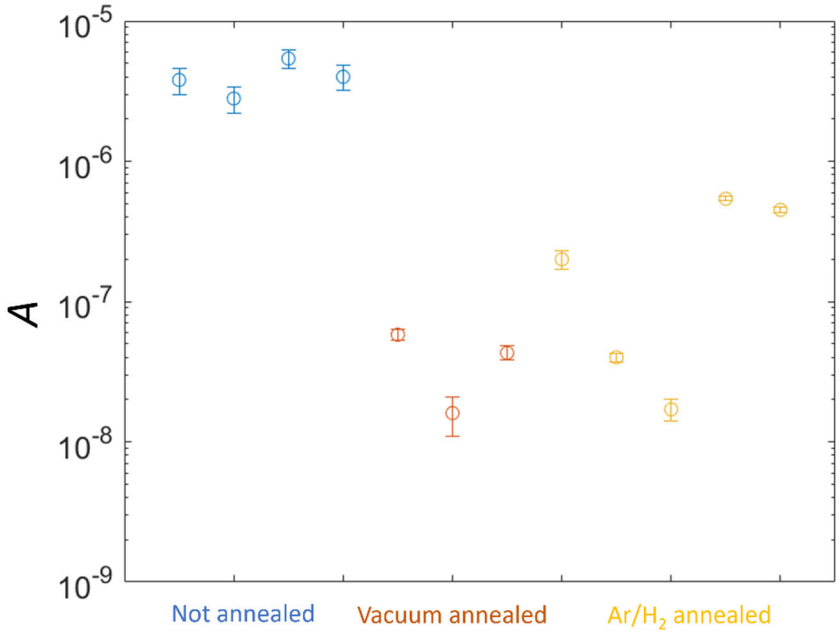

Figure 3.7: Noise parameter for annealed vs non-annealed graphene FETs. The devices that were not annealed (blue) have a higher noise parameter than the vacuum annealed (orange) and Ar/H_2 annealed (gold) devices.

3.6 Gate Voltage Noise

The noise parameter is a useful value to relate device noise to a model, and to compare the noise in dissimilar devices. It's important to consider that the end goal for these sensors is measurement of action potentials from cells. An estimate for the detectable size of action potentials is 100 µV for cells that are far away, and 1 mV for cells close to the sensor channel (this is explained in Chapter 5). Therefore it is useful to calculate the gate voltage noise $V_{g,RMS}$ for the devices to confirm it is small enough to detect an action potential. The gate voltage noise can be calculated by integrating the current noise PSD data over

the desired bandwidth to find I_{RMS}, taking the square root and dividing by the transconductance to get $V_{g,RMS}$. The results for one of my graphene FETs is below. The minimum noise for the bandwidth 1 Hz – 10 kHz was 170 μV at V_g = -50 mV. Note that the noise level at this operating point is low enough to measure action potentials from cells in close proximity, but not from cells far away. State-of-the-art graphene FET devices can reach $V_{g,RMS}$ ~ 10 μV for the bandwidth 1 Hz – 10 Hz[23]. We can estimate the noise for the 1 Hz – 10 kHz bandwidth if we assume the noise is perfectly 1/f throughout the bandwidth, and, normalizing with the device size (this is for a 50 μm x 50 μm device), we find that $V_{g,RMS}$(1 Hz – 10 kHz) x Device Area = 5 x 10^4 μV μm^2. For our device, which is $V_{g,RMS}$(1 Hz – 10 kHz) x Device Area = 10.2 x 10^4 μV μm^2. Therefore, our device noise is only about a factor of 2 larger than the state-of-the-art device when device area and bandwidth are accounted for.

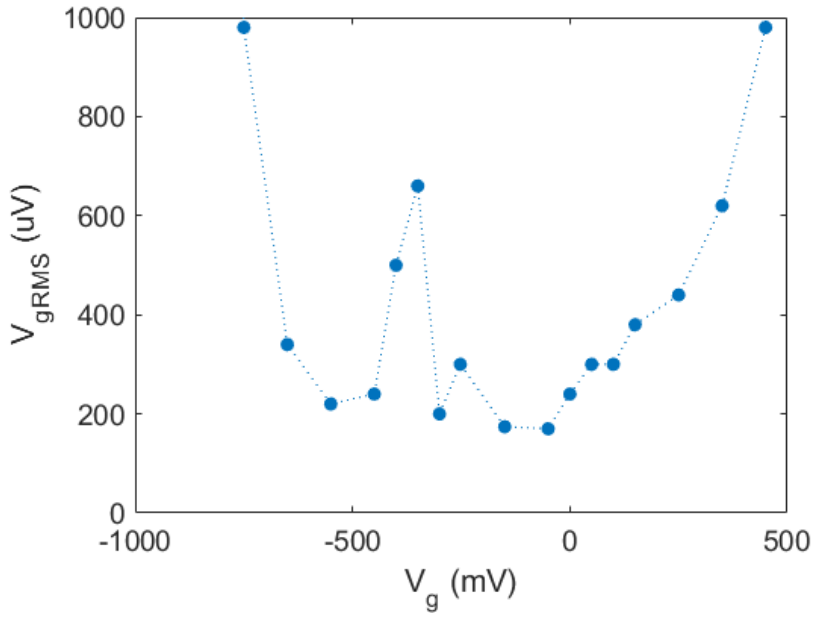

Figure 3.8: Gate voltage noise $V_{g,RMS}$ as a function of gate voltage V_g. The minimum noise occurs at V_g = -50 mV, with a value of 170 μV. The Dirac point is at -300 mV.

3.7 Conclusion

I measured the noise in my graphene FETs and found the biosensing regime of 1 Hz – 10 kHz was dominated by 1/*f* noise. I determined the noise parameter *A*, and, when normalized for device area, *A* for my devices was the same order of magnitude as published devices. The noise parameter for my devices as a function of gate voltage was measured and compared to existing models. The ACN model showed good agreement with my devices at low gate voltages. An argument was presented that predicted that contact resistance could be the cause of the deviation from the ACN at high gate voltages. The

contact resistance was also expected to increase the overall 1/*f* noise. Early results for using annealing and sandwich contacts to reduce contact resistance were shown as a possible method for reducing 1/*f* noise. The gate voltage noise for our device for the 1 Hz – 10 kHz bandwidth was found to be 170 μV, which is about a factor of 2 larger than state-of-the-art graphene FETs. This level of noise is expected to be sufficient for measuring action potentials from cells close to the graphene channel.

CHAPTER 4: AMPLITUDE MODULATION AND MULTIPLEXING WITH GRAPHENE FETS

4.1 Introduction

Electrical measurements of large populations of neurons can elucidate how information is processed in the brain. This type of measurement requires thousands of sensors densely packed into a small area of the brain. If electrical signals are recorded with passive electrodes, each sensor requires one wire output. The wires themselves take up a large amount of space on the sensor surface (or inside a sensor needle), which limits the sensor density. Furthermore, the output wires need to interface with an integrated circuit (IC) outside the brain. There are typically only a few hundred wired inputs to an IC. The challenge of wiring sensor systems is now a serious bottleneck to the advancement of neurosensory technology.

A technique to get around the wiring bottleneck is multiplexing. Multiplexing allows us to send multiple signals through a common medium. It is a familiar technique for telephone landlines, fiberoptic communication and radio broadcasting. However, multiplexing is still in early development in the field of neuroscience. A multiplexed silicon CMOS probe capable of monitoring around 1300 channels simultaneously was developed in 2017[57]. Unfortunately the density at which these probes can be inserted is limited due to the damage the shank-type probes do upon insertion[4,5]. A flexible array for measurements from the surface of the brain was developed that uses wire sharing, but it relied on switching between channels on the shared wire rather than reading all channel simultaneously[58]. Garcia-Cortadella et al. recently demonstrated multiplexing with an array of 32 graphene FETs operated with 12 wires[23]. The authors suggest a path forward to operate 1024 graphene-based sensors with 64 wires.

We independently developed a scheme similar to Garcia-Cortadella et al. (Ref. [23]). In this chapter I describe our scheme and my experiments to test the feasibility of the scheme.

I first show how graphene field effect transistors (GFETs) can amplitude modulate a carrier wave and explain how amplitude modulation (AM) facilitates multiplexing. Then, I show experimental results demonstrating multiplexing signal from 2 GFET sensors. I operate the sensors with a detection bandwidth of 1 kHz (suitable for measuring the action potentials from single neurons[20]). I show that the minimum resolvable signal is set by the intrinsic noise of the sensor (~ 100 μV) and is not degraded by modulation/demodulation process. Finally, I discuss the prospects for scaling the GFET array to a grid of approximately 45 x 45 sensors operated with 90 wires.

My work included development of testing and measurement techniques for graphene-based multiplexing sensors arrays. Our collaborators in electrical engineering designed and built an IC for operating the sensor array. We successfully interfaced this IC with one of my GFET arrays. I also developed hardware for a "model sensor array" which simulates the behavior of a GFET array for the purpose of testing IC designs.

4.2 Amplitude Modulation

Graphene field-effect transistors are well suited to amplitude modulation (AM). Amplitude modulation encodes signals into the amplitude of a high frequency carrier sine wave. Many AM waves, each with a unique carrier frequency, can be transmitted on a common wire. The encoded signals can then be recovered by a demodulation process.

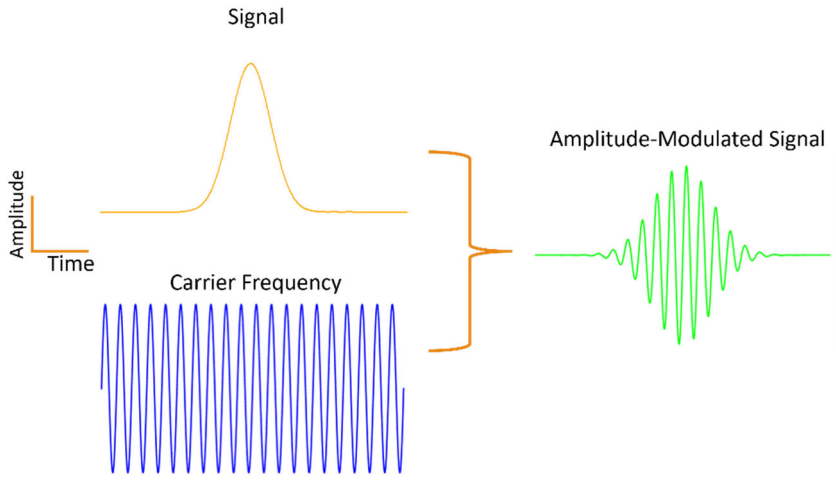

Figure 4.1: AM signal. A signal (yellow) is multiplied by a carrier (blue) to create an AM signal (green). When multiple AM signals are transmitted through a single medium, they can be separated out again if different frequency carriers were used. This is how multiplexing is done with AM signals.

Mathematically, AM is equivalent to the multiplication of the signal with the carrier sinusoid. A representation of an AM signal is shown in Figure 4.1. It is important that the frequency of the carrier is large enough that multiple oscillations of the carrier occur in the duration of the signal, so that the amplitude is captured with high resolution. I explored two signal types in my work: sinusoids and Gaussian pulses. The sinusoids are useful because they are spectrally simple, and I will discuss shortly how frequency domain analysis is useful for designing a frequency-division multiplexing system. The Gaussian pulses are used because they are good approximations for neuron action potentials, and successful transmission of these signals can demonstrate the utility of graphene FETs for sensing individual action potentials.

A simple example illustrating the relationships between the raw signal and the AM signal is shown in Figure 4.2. Figure 4.2a shows a 1 kHz signal tone in the time and the frequency domains. Figure 4.2b shows the signal after being multiplied by a 7 kHz carrier sine wave to form an AM signal. The shape of the raw signal is visible in the upper and lower envelopes of the time domain plot of the AM signal (Figure 4.2b). The frequency representations of the AM signal shows three prominent peaks. One is at the carrier frequency f_c. The other two are at $f_c + f_{signal}$, and $f_c - f_{signal}$, where f_{signal} = 1 kHz. These peaks are known as sidebands, and they carry the information of the signal. For example, the 1 kHz signal in Fig. 4.2 is carried by the sidebands at 6 and 8 kHz. The relevancy of this to multiplexing will be discussed shortly.

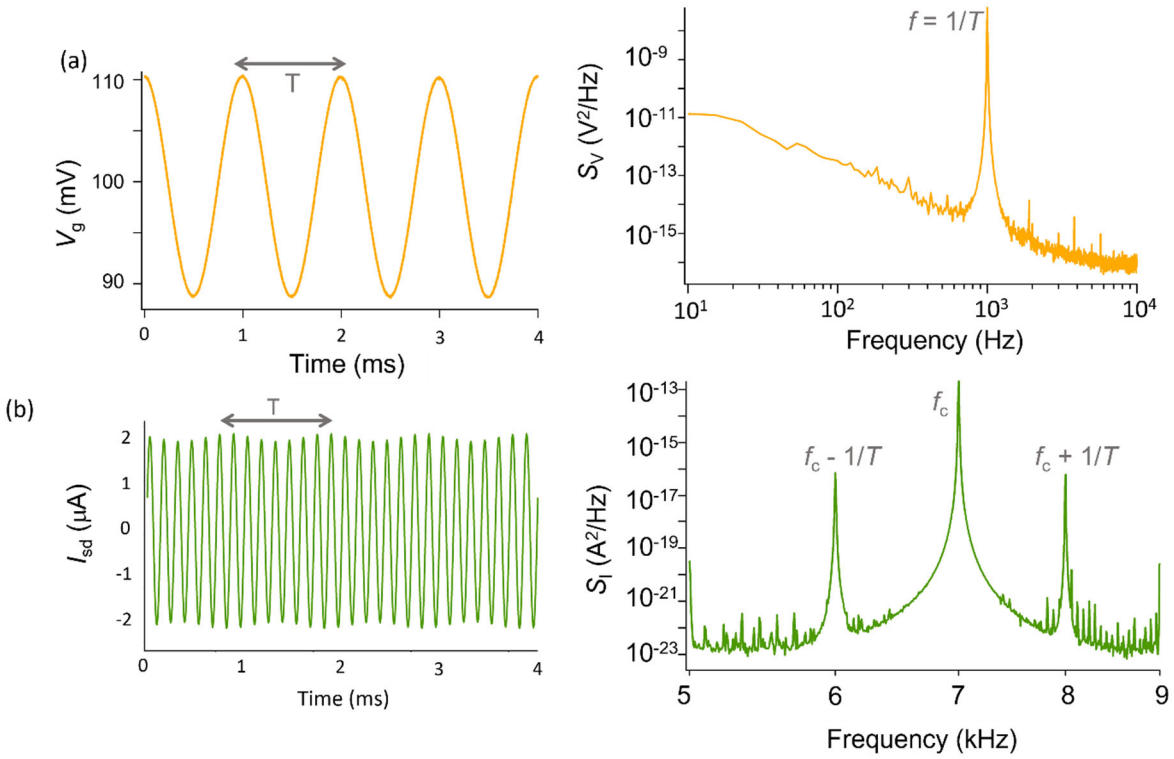

Figure 4.2: Amplitude modulation with sinusoidal signal. (a) The time and frequency domain representations of a sine signal with frequency = 1 kHz. The frequency spectrum shows a large peak at 1 kHz. (b) The time and frequency domain representations of the AM signal. The three prominent peaks appear in the frequency spectrum, one is the carrier frequency f_c and two are the sidebands $f_c + f_{signal}$, and $f_c - f_{signal}$. The sidebands are where the signal information (i.e. the 1 kHz sine signal) is stored in the AM signal.

The sidebands in Figure 4.2 can be explained mathematically as follows. Represent the carrier wave as cos(a), and the signal as 1+cos(b). Starting from the trig identity

$$\cos(a)\cos(b) = \frac{1}{2}\cos(a+b) + \frac{1}{2}\cos(a-b), \tag{4.1}$$

add *cos*(a) to both sides to yield

$$(1+\cos(b))\cos(a) = \frac{1}{2}\cos(a-b) + \cos(a) + \frac{1}{2}\cos(a+b). \tag{4.2}$$

The left side of the equation is the AM signal; it's the product of the carrier cos(a) and the modulating signal (1+cos(b)). The right side has three terms, which represent the left side band, the carrier frequency, and the right side band, respectively. Equation 4.2 shows that the AM signal can be written as the sum of the carrier with the two sidebands.

Amplitude modulation effectively copies the information from the original signal into a higher frequency band. This is why amplitude modulation is useful for multiplexing. By multiplying each signal by a unique carrier frequency, each signal is encoded in a unique part of the frequency spectrum. Then when the AM signals are added together, although they are superimposed in time, they occupy unique spaces in the frequency domain. The original signals can be extracted by applying a demodulation process (demodulation is described in Section 4.2.1).

Figure 4.3 shows a signal relevant to biosensing; a train of Gaussian pulses spaced 20 ms apart is a good approximation of the spike train from a neuronal cell. Figure 4.3a shows the raw signal in the time and frequency domains. Note that the periodic behavior of the pulses (T = 20 ms) is reflected in the frequency spectrum as peaks spaced 1/T = 50 Hz apart. Figure 4.3b shows the AM signal, from multiplying the raw signal by a 27 kHz carrier sine wave. Again, the shape of the raw signal is visible in the upper and lower envelopes of the time domain plot of the AM signal. The frequency spectrum of the amplitude modulated signal in Figure 4.3b shows the largest peak is at the carrier frequency of 27 kHz, and the sidebands consist of multiple peaks spaced 50 Hz apart, as seen in the raw signal spectrum.

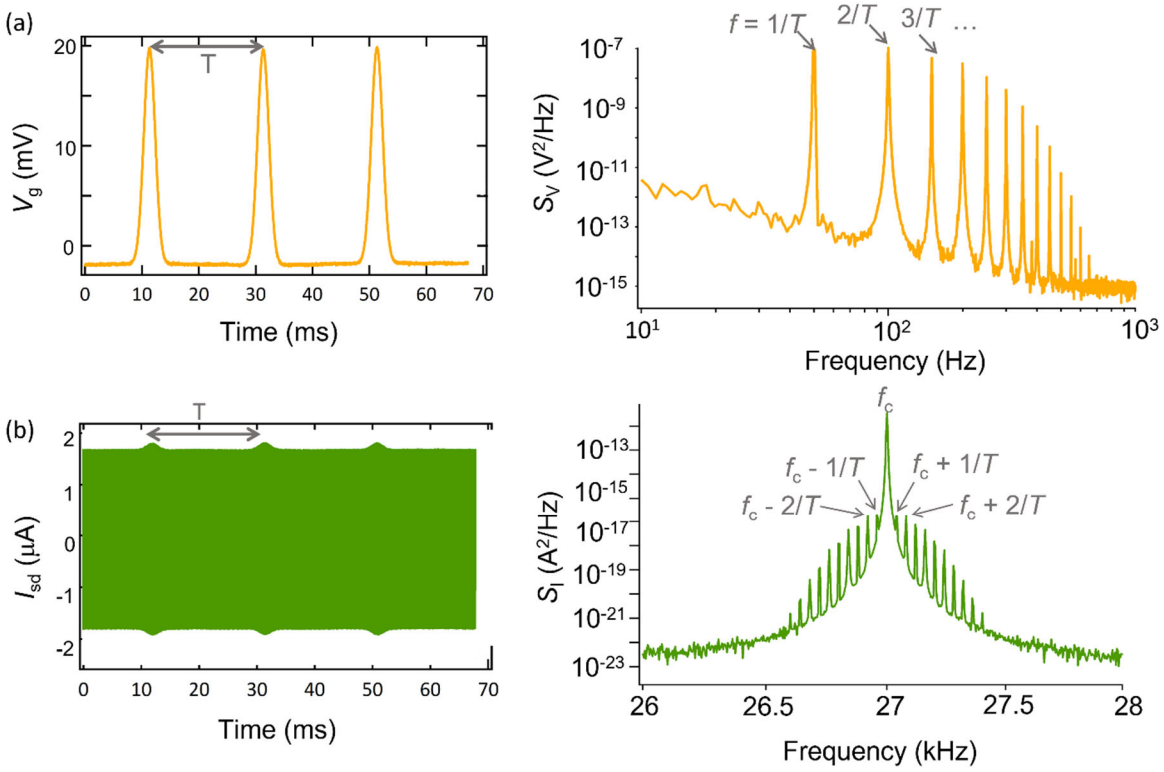

Figure 4.3: Amplitude modulation with Gaussian pulses. (a) The time and frequency domain representations of a series of Gaussian pulses. The spacing between the pulses is $T = 20$ ms, while the spacing between the peaks in the frequency domain is $1/T = 50$ Hz. The frequency of each peak is labeled as $1/T$, $2/T$, etc. The Gaussians pulses are the sum of multiple tones, as shown in the frequency spectrum. (b) The time and frequency domain representations of an AM signal with Gaussian pulses as the original signal. The Gaussian pulses are visible in the time domain as the envelope of the AM signal. In the frequency domain, the Nth peak from the original signal spectrum shows up at $f_{carrier} + N/T$ and $f_{carrier} - N/T$.

4.2.1 Amplitude Modulation in Graphene FETs

To create an AM signal with a graphene FET, an AC voltage V_{sd} is applied across the channel. This acts as the carrier, with frequency f_c. The signal waveform (a sine function or a Gaussian) is input to the graphene gate. Our devices are liquid gated, so the gate is an electrolyte. An Ag/AgCl electrode is used to apply voltages to the electrolyte. The transconductance of the graphene FET is non-zero for typical operating conditions, therefore, a change in gate voltage (the signal) changes the conductance of the graphene channel. The change in amplitude of the AC current is proportional to the change in gate voltage, resulting in an AM current.

The experimental setup to create and record AM currents in graphene FETs is shown in Figure 4.4. The AM current is amplified with a low-noise current amplifier (Femto DLPCA-200) using the gain

setting of 10^6 V/A and filtered through a home-built anti-aliasing low pass filter (LPF). The analog current data is then converted to a digital signal by a DAQ (National Instruments USB-6343), which interfaces with a Labview program (modified from the open-source Labview program called meaSureit) and is saved to a text file. The data sampling rate, f_{sample}, is 500 kHz for most of the experiments described here. The anti-aliasing LPF has a cutoff frequency f_{LPF}, which is chosen such that that $f_c < f_{LPF} < f_{sample}/2$. The LPF cutoff frequency is above the carrier frequency to ensure the AM signal is not attenuated. The LPF cutoff frequency is below $f_{sample}/2$ to prevent aliasing (see Chapter 2 for more information on aliasing).

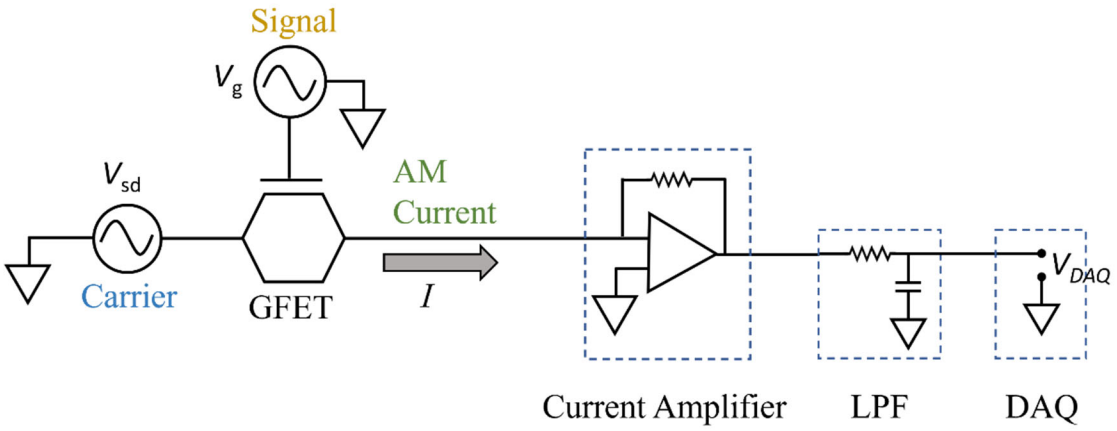

Figure 4.4: Measurement circuit for creating and recording AM signals in graphene FETs. The circuit shown represents a graphene FET generating an AM signal. The source-drain bias V_{sd} acts as the carrier with frequency f_c, while the signal is applied to the gate voltage V_g. The resulting current is the AM current, with a frequency of the carrier f_c, and an amplitude controlled by V_g. The AM current is amplified by a current amplifier and the high frequency components greater than f_c are filtered out to prevent aliasing. Lastly the signal is digitized by the DAQ and sent to the computer to be recorded.

Figure 4.5 shows amplitude modulation performed by one of my graphene FETs. A 20-mV_{pp} AC voltage with f_c = 11 kHz was applied as V_{sd} to a graphene FET, as shown in Figure 4.5a. The signal applied to the gate electrode was a 1-kHz sine, shown in Figure 4.5b. Figure 4.5c shows the resulting AM current measured from the graphene FET. The envelope of the AM current is the signal, while the frequency is f_c. The current was collected with a sampling frequency of 200 kHz, with a 48 kHz anti-aliasing filter applied before the DAQ.

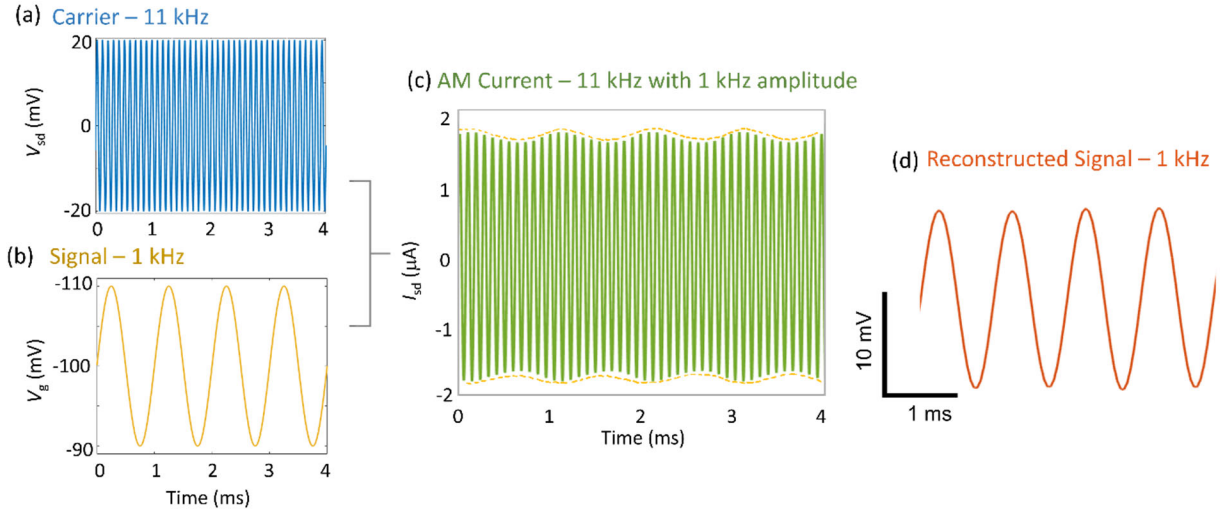

Figure 4.5: Amplitude modulation in a graphene FET. (a) The 11 kHz voltage carrier V_{sd} applied across the graphene channel, (b) the 1 kHz voltage signal V_g applied to the gate, and (c) the resulting AM current. The AM current has the 1 kHz signal stored in the amplitude (highlighted in yellow), and the high frequency oscillations occur at 11 kHz. (d) The reconstructed signal after DSP. The amplitude is about 18 mV (90% of the applied signal).

To recover the original signal from the AM current, I wrote a MATLAB script (see Appendix B) that utilizes digital signal processing (DSP) techniques. First, the $I(t)$ data is filtered with a bandpass centered on the carrier frequency of interest. This removes AM signals at other carrier frequencies while preserving the sidebands that encode the signal of interest. For the example illustrated in Figure 4.5a, I chose a 4 kHz bandpass centered at 11 kHz. This bandpass filter (BPF) was chosen to include all of the signal power in the sidebands. Next, the filtered data is squared so that all data points are positive and the 11 kHz carrier frequency is doubled (22 kHz). Then, a filter smooths the data, removing the unwanted component at 22 kHz and preserving the 1 kHz signal. For the data in Figure 4.5c, the data was smoothed with a BPF that admits frequencies 10 Hz to 2 kHz. Each data point is then multiplied by 2 (correcting for the smoothing step), and square rooted (reversing the squaring step). Finally, each data point is divided by the transconductance, dI/dV_g, to recover the original changes in gate voltage that were applied to the gate. The transconductance can vary at a given gate voltage due to hysteresis, so the average dI/dV_g of several cycles is used. The reconstructed voltage signal is shown in Figure 4.5d. The amplitude of the reconstructed signal is about 18 mV, slightly smaller than the applied signal (20 mV). Prior work has shown that the transconductance decreases as the frequency of gate signals increases[23]. The dI/dV_g value used to calculate the reconstructed signal was taken at a low frequency (f = 0.1 Hz), therefore the signal size in the reconstructed data may be underestimated.

The signal-to-noise ratio (SNR) is defined by

$$SNR = \frac{V_{\text{Signal}}}{\delta V_{\text{Noise}}}, \tag{4.3}$$

where V_{Signal} is the amplitude of the signal, and δV_{Noise} is the voltage noise. The voltage noise is the standard deviation of the voltage signal with constant V_g.

The long-term goal for these devices is measuring neuronal cell activity, and the signals generated by cells are on the order of 0.1-10 mV (as shown in Chapter 5). Using a 2 mV signal explores the middle of this range. Figure 4.6a shows reconstructed data from 2 mV Gaussian peaks with T = 20 ms, which resulted in a reconstructed amplitude of 1.8 mV and a SNR of 36. Closer-spaced peaks with T = 2 ms had reconstructed amplitudes of 1.2-1.5 mV and a SNR of 11. (Figure 4.6b).

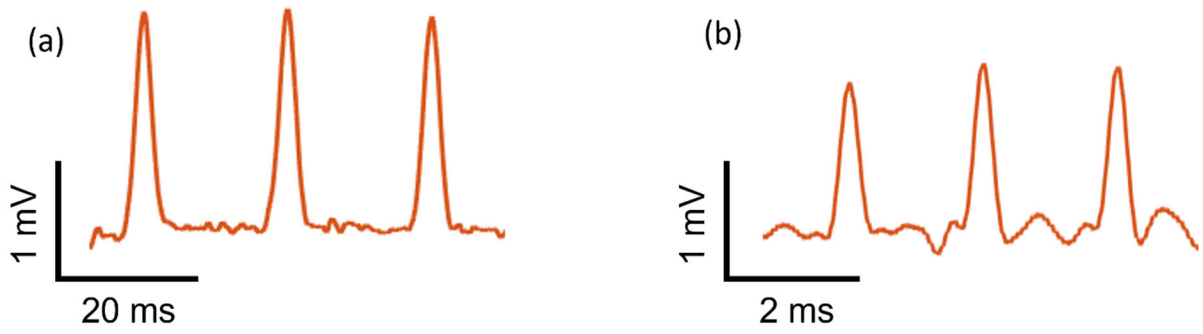

Figure 4.6: Reconstructed signals from Gaussian pulse signals. Gaussian pulses were applied to V_g and modulated with a 7 kHz carrier. The amplitudes of the applied signals were 2 mV, and the periods were (a) 20 ms and (b) 2 ms, respectively.

The SNR of a reconstructed signal from an AM current can be compared to a standard DC current. A reconstructed signal is shown in Figure 4.7a, while a signal probed with a DC current is shown in Figure 4.7b. The DC measurement setup is the same as in Figure 4.4, with a DC V_{sd} being applied rather than an AC V_{sd}. In the DC case, no carrier is used and the changes in current caused by the gate signal are measured directly. A single digital BPF is applied to the data to filter out noise outside the signal band. In Figure 4.6, the signal applied to each gate was a train of Gaussian pulses with T = 20 ms and amplitude of 20 mV. The SNR of the reconstructed signal is 120, while the SNR of the DC measurement signal is about 70. The amplitude of both resulting signals is about 19 mV. The signal transferred via AM results in the same amplitude after DSP and has lower noise than the DC measured signal. AM also has the advantage that multiplexing is possible, where it is not possible with DC signals.

There are some limitations to what carrier frequencies can be used for AM in graphene FETs, and we will discuss these limitations in the next section.

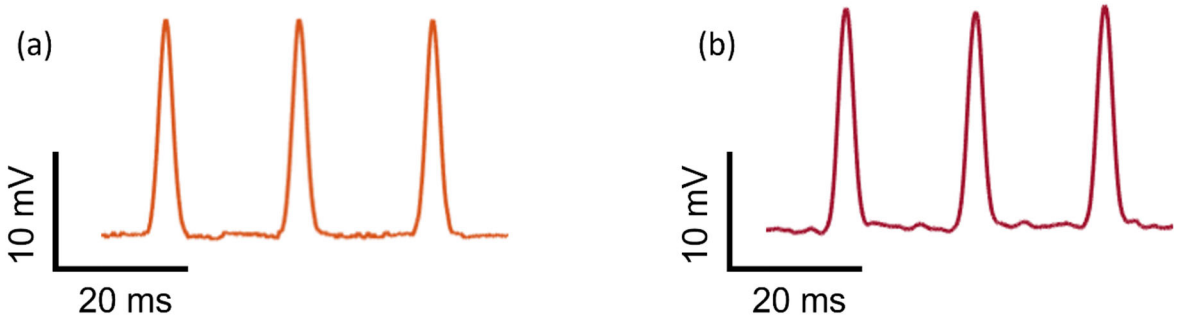

Figure 4.7: Comparison of AM signal with DC measured signal. A series of 20 mV Gaussian pulses with T= 20 ms was applied as the gate signal. The resulting signals are shown from (a) an AM measurement, and (b) a DC measurement. The amplitude of the resulting signals is very similar, and the AM signal has lower noise.

4.2.2 Device Performance at High Frequency

The smallest possible carrier frequency f_c is set by the frequency of the signal; many oscillations of the carrier should occur during the signal to encode enough information in the amplitude of the AM signal that it can be recovered again. As a rule of thumb, $f_c \gtrsim 10 f_{signal}$. In Fig. 4.5 I show that $11 f_{signal}$ was sufficient for recovering a simple sinusoidal signal. The highest possible frequency is related to the physical properties of the sensor.

A key factor limiting high-frequency operation of a graphene FET biosensor is the graphene-electrolyte interface. Prior work has examined how the interface impedance of a graphene FET with a liquid electrolyte behaves at high frequencies, and found that a distributed element model fits the experimental data well[59]. The current that reaches the drain decreases at large f_c. This can be explained qualitatively by considering capacitance between the graphene and the electrolyte gate. At high frequencies, current leaks from the graphene channel into the electrolyte, rather than going to the drain electrode. To quantify this effect, we modeled the graphene channel as a distributed set of resistors and capacitors (Figure 4.8).

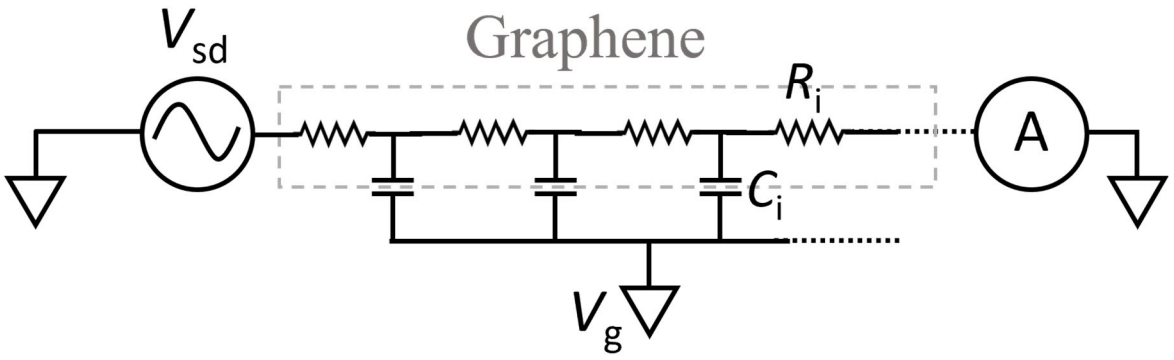

Figure 4.8: The distributed-element model of the graphene channel. The graphene channel is treated as a series of resistors, and the graphene-electrolyte interface is treated as a set of capacitors, coupled to the grounded gate. The resistance per unit length of the channel is R_i, and the capacitance per unit length is C_i.

I examined the circuit in Figure 4.8 circuit using a circuit simulator (Falstad Online Circuit Simulator) using 10 resistors and 9 capacitors. The value of the total resistance (sum of 10 resistors) was chosen to match the measured resistance of the graphene channel (R = 7.2 kΩ). The total capacitance (sum of 9 capacitors) was estimated using previous measurements of the graphene-electrolyte interfacial capacitance (≈ 1 – 3 μF/cm^2)[39,60]. For our graphene devices with a 50 μm x 50 μm channel, we expect a total capacitance of 25 – 125 pF. The simulated current through the channel (normalized to the DC current I_{DC}) as a function of the frequency of the applied voltage with R = 7.2 kΩ and C = 30 pF is shown in Figure 4.9 in orange. If we define the cutoff frequency f_{cutoff} as the point when the current to the drain reaches 50% of the value of the DC current I_{DC}, then f_{cutoff} = 5.2 MHz. Using the upper limit of the capacitance C = 125 pF in the simulation, then we find f_{cutoff} = 125 kHz.

By testing several values of R and C in the simulator, the relationship between the cutoff frequency and R and C can be determined. This is useful to know because increasing the cutoff frequency increases the range of possible carrier frequencies, and R and C can be tuned by adjusting the properties of the graphene channel. Figure 4.9 shows the normalized current as a function of frequency for several different values of R (while keeping C constant). The current I = 0.5I_{DC} is marked with a dotted line. As the total channel resistance increases, f_{cutoff} decreases such that $f_{cutoff} \sim 1/R$. Adjusting C while keeping R constant shows the same scaling. Therefore, the relationship between R, C, and f_{cutoff} is of the form

$$f_{\text{cutoff}} = \frac{\alpha}{RC}, \tag{4.4}$$

where α is a constant. Using a more complex model that accounts for the resistance of the electrolyte, other researchers found f_{cutoff} has the same dependance on R and C[59]. Furthermore, they were able to compare their findings with experimental results for solution gated graphene FETs and found $\alpha = (2\pi)^{-1}$. This differs from the value predicted by our simple model by about a factor of 10 ($\alpha = 1.14$). The published model predicts a cutoff frequency of 175 – 885 kHz for the values of R and C for our graphene FETs, while our model predicts 1.3– 6.3 MHz.

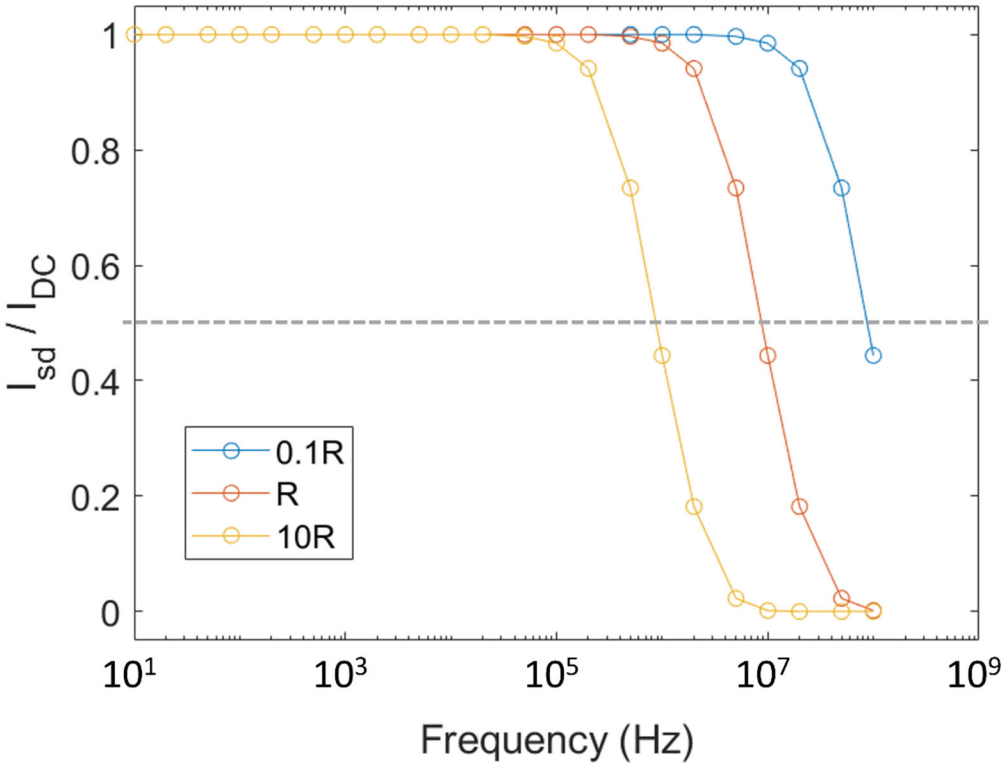

Figure 4.9: Normalized current through the graphene channel as a function of frequency with varying *R*. Increasing R by a factor of 10 decreases the cutoff frequency by a factor of 10, and vis versa. The current as a function of f_c was normalized to the DC current I_{DC}.

The cutoff frequency is a function of the resistance and capacitance, both of which can be modified by changing the graphene channel dimensions. The channel resistance is

$$R = \frac{\rho L}{W}, \tag{4.5}$$

where is the sheet resistivity of the graphene, W is the width of the graphene channel, and L is the length of the channel. The capacitance is given by

$$C = C_o WL, \tag{4.6}$$

where C_o is the specific capacitance of the graphene-electrolyte channel, due to the quantum capacitance and the capacitance of the electric double layer (C_o = 1-3 μF/cm^2)[39,60]. Substituting Equations 4.5 and 4.6 into Equation 4.4 gives

$$f_{\text{cutoff}} = \frac{\alpha}{\rho C_o L^2}. \tag{4.7}$$

Therefore, by shortening the graphene channel we can increase the cutoff frequency. This is relevant because it expands the range of usable carrier frequencies for amplitude modulation, and when multiplexing with unique carrier frequencies for each channel, more channels can be fit within the allowed range of carrier frequencies. In the next section I will discuss multiplexing with multiple AM signals in graphene FETs.

I tested the high-frequency response of a GFET sensor using the setup shown in Figure 4.10a. An AC voltage was applied to the channel, $V_{\text{sd,RMS}}$ = 8.5 mV, and the frequency f_c was varied from 1 Hz to 500 kHz. The amplitude and the phase of the current I was measured using an oscilloscope. The bandwidth of the current amplifier was 500 kHz, which limited the maximum frequency I could test. Figure 4.10b shows the experimental results of the current as a function of f_c; the experimental results are represented by the open circles. A control experiment with a 10 kΩ resistor in place of the graphene FET was performed and is represented by the grey circles on Figure 4.10b to test the roll-off of the current amplifier.

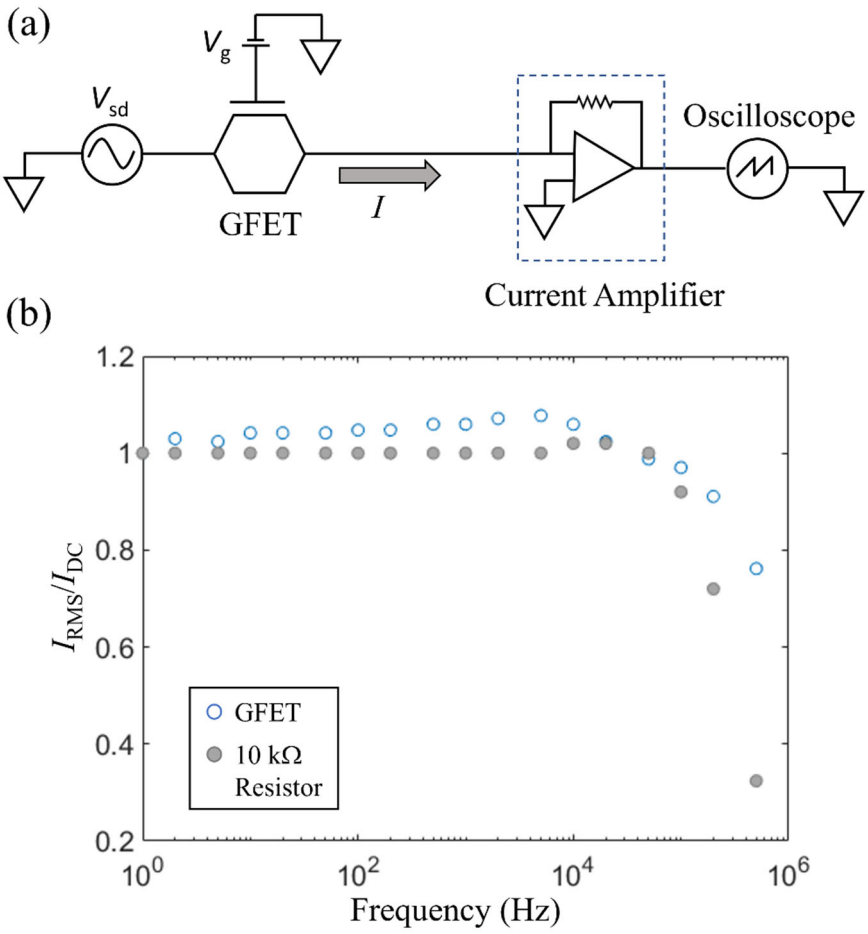

Figure 4.10: Graphene FET current as a function of frequency. The testing setup for graphene FETs at different carrier frequencies. The bandwidth of the current amplifier is reported to be 500 kHz. (b) The experimentally measured data of the graphene FET is the blue open circles. The experimental data measured with a 10 kΩ resistor is the gray filled circles. The resistor data shows that the roll-off of the system begins around 20 kHz.

The experiment shows that the current through the graphene FET stays constant up to at least 10 kHz, after which point the roll-off from the current amplifier begins to obscure the data. So far this agrees with the estimated values of f_{cutoff} = 175 kHz – 885 kHz. Further testing with a higher bandwidth measurement setup and/or graphene FETs of different channel lengths can be done to verify Equation 4.9.

4.3 Frequency-Division Multiplexing with AM Signals in Graphene FETs

To send multiple signals through a single medium (multiplexing), each signal must utilize a different frequency band (frequency-division multiplexing), or different time windows (time-division multiplexing). As shown above, graphene FETs are well suited to perform AM at the sensor site. The AM

signals from multiple graphene FETs can be multiplexed and share a single output wire. The multiplexing of AM signals each with a unique carrier frequency is called frequency-division multiplexing (FDM). Frequency-division multiplexing can address the wiring bottleneck present in high density, large number neurosensing experiments by allowing many sensors to share the same wire. Frequency-division multiplexing was pioneered in graphene FETs by Garcia-Cortadella et al in 2020[23]. In that work, they fabricated a 4x8 array of graphene FETs and multiplexed four graphene FET signals down a single wire. They demonstrated multiplexing using signals in the 50 -200 Hz range. I expand on this work by showing that signals up to 1 kHz can be multiplexed in graphene FETs, which is the frequency range of individual action potentials. I also interfaced our 1x2 graphene FET array with a custom integrated circuit (IC) chip to replace some of the large electronic components (the current amplifier, the LPF, and the DAQ). I also developed a junction FET (JFET) model cell to act as a stand-in for graphene FETs and demonstrated multiplexing with two JFETs.

4.3.1 Fabrication of Graphene FETs for Multiplexing Experiments

Multiplexing can drastically reduce the number of wires needed to record from an array of sensor sites. First let's start with discussing the simplest case of a 1x2 array. To multiplex with a 1x2 array of graphene FETs, each graphene FET needs to create an AM current with a unique carrier frequency. This is accomplished by applying V_{sd} to each channel using different carrier frequencies (for example, applying V_{sd} with f_{c1} = 28 kHz to device 1, and V_{sd} with f_{c2} = 39 kHz to device 2). Then the AM currents from both devices are sent down a shared drain wire (one output wire for two devices) to the current amplifier. The experimental setup is shown in Figure 4.11.

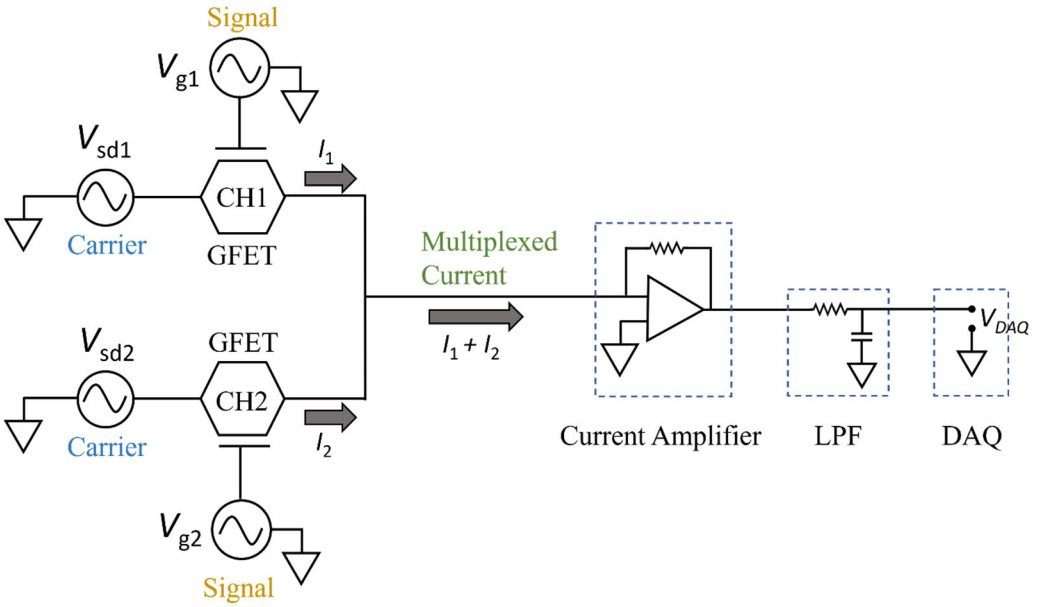

Figure 4.11: Circuit diagram for 1x2 array of graphene FETs. The two graphene FETs are shown on the left. The carrier frequency of V_{sd1} is f_{c1}, and the carrier frequency of V_{sd2} is f_{c2}. The output from each graphene FET is an AM current. The drains of the two devices are connected so the two AM currents are summed (i.e., multiplexed) and sent down a single shared wire to the current amplifier.

I designed and fabricated wafers with 1x2 arrays of graphene FETs to show that we can multiplex with our devices. When measuring *in-vitro* cells, local voltages produced by individual cells would gate each sensor individually (see Chapter 5 for more discussion on graphene FETs and *in-vitro* cells). For testing the devices without cells, I designed a novel wafer that has two separate liquid gates, as shown in Figure 4.12a. Device 1 and 2 are in different pools of liquid, but they share a common drain as illustrated in Figure 4.12b. This design enables us to apply a unique gate signal to each liquid-gated device. The two pools are formed using the photopatternable polymer SU-8 to form hydrophobic rings. A labeled photo of the measurement setup for a 1x2 array of graphene FETs is shown in Figure 4.12c.

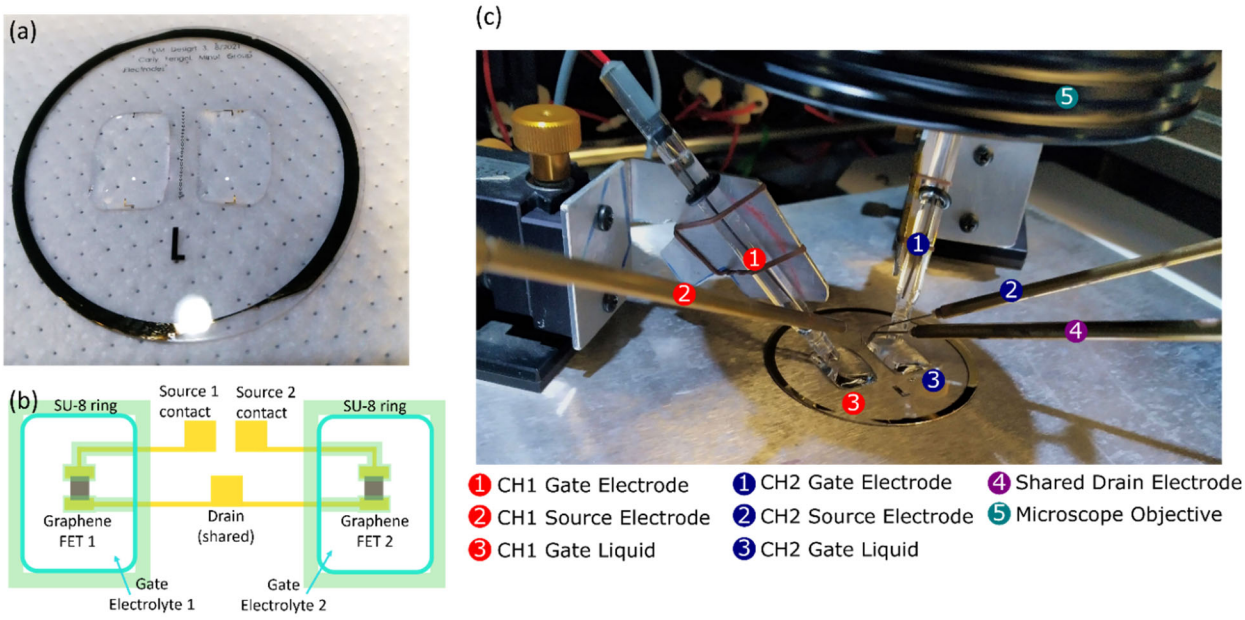

Figure 4.12: Wafer design for multiplexing with 1x2 arrays of graphene FETs. (a) Photograph of the 2-inch fused silica wafer. The two pools of liquid are the two liquid gates. The contact electrodes are in between the two liquid pools. (b) Illustration of one 1x2 array of graphene FETs. Each device has a source electrode and share a drain electrode. Device 1 is in the left liquid gate, while device 2 is in the right liquid gate. (c) A labeled photo of the measurement setup. The wafer is viewed through a microscope during testing.

The devices were fabricated on a 2-inch fused silica wafer. Formation of the electrodes and graphene channels is fully described in Chapter 2. Briefly, electrodes and leads were photopatterned and metal (5 nm Cr, 40 nm Au) was deposited using electron beam deposition. After metal lift-off, graphene was added to the wafer via a wet transfer process. Graphene was patterned using photolithography and oxygen plasma etch. After the graphene and electrodes were formed, the metal electrodes were encapsulated with a layer of SU-8 polymer. The SU-8 was spun to a thickness of 1.4 μm and then photopatterned with a contact aligner. The SU-8 serves two functions. It protects the source and drain leads from contacting the electrolyte and forms a hydrophobic ring to hold the two pools of electrolyte, as shown in Figure 4.12b.

Trial and error were needed to develop a recipe that both gave clean, sharp SU-8 edges and good adherence to the substrate. When the SU-8 had residual material around the edges of the design, the graphene channel adjacent to the SU-8 edges would have a layer of residue on it that could decrease the device response to gating and introduce noise. An optical image of the residue is shown in Figure 4.13a. The residue may have been caused by insufficient agitation during SU-8 development, overexposure, or poor contact between the photomask and the substrate during exposure.

When the SU-8 was not well adhered to the substrate, electrolyte liquid could get underneath the SU-8 layer and contact the metal leads, leading to large leakages between the exposed metal and the electrolyte. The SU-8 coating on the top lead in Figure 4.13b lifted completely from the substrate during a rinsing step and re-adhered to a different position. Corrosion of the metal can be seen. Metal leads in direct contact with the electrolyte create large oxidation and reduction peaks in the IV_g curve of the graphene FET. Furthermore, after long times (over an hour) in electrolyte, the SU-8 would visibly peel away from the wafer. Adhesion issues could have been caused by underexposure of the SU-8 or by microcracks forming in the material due to temperature changes that were too rapid when putting the wafer onto hotplates during the fabrication steps.

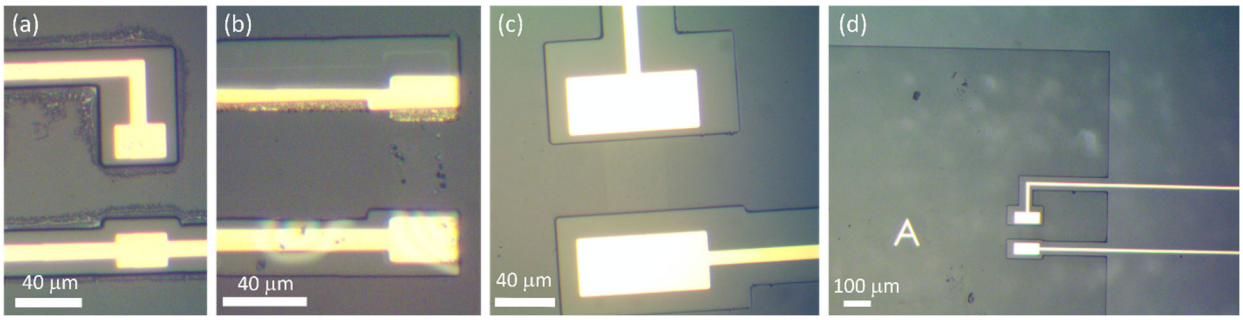

Figure 4.13: Optical images of SU-8 coating on gold leads. (a) Residue around edges of SU-8. (b) Delamination of SU-8. The SU-8 coating the top lead lifted and moved when the wafer was rinsed. During use, the exposed gold was corroded when a voltage was applied to the lead. The SU-8 coating on the bottom lead shows interference rings indicating poor adhesion to the substrate and lead. (c) and (d) Successfully patterned SU-8 coating. There is no residue, and the edges are sharp for both small and large features.

The final recipe developed used 2-inch wafers; the wafer size was closer to the design size and was easier to agitate by hand during the development step than a 3-inch wafer. Multi-stage baking steps were also utilized to prevent cracking from rapid temperature changes. These changes resulted in SU-8 with clean edges and that adhered well to the substrate, even after many hours in electrolyte, as shown in Figures 4.13c and d. The successful SU-8 recipe started with baking the wafer at 100° C for 10 minutes. SU-8 2002 (MicroChem) was droppered onto the wafer and spun at 3000 RPM (with 5000 RPM/s acceleration) for 30 s. The wafer was then placed on a 45° C hotplate for 30 s, then directly onto a 95° C hotplate for 90 s. The wafer was exposed in a contact aligner with the appropriate mask inserted (note SU-8 is a negative photoresist) with an exposure dose of about 128 mJ/cm^2 (14 s under a lamp with power 9.1 mW/cm^2). Note that this same exposure dose applied with an 18 mW/cm^2 bulb consistently resulted in the undesired edge effects mentioned earlier; this could be related to the bulb power or could be due to poorer contact between the mask and the wafer due to the mechanics of the contact aligner. After the wafer was exposed, a ramped post-exposure bake was performed. The wafer was placed on a hotplate at

30° C. After 2 minutes, the hotplate was turned up to 60° C. After 3 more minutes the hotplate was turned up to 95° C. Then after 3 minutes the hotplate was turned down to 30° C. After 3 more minutes, the wafer was moved off of the hot plate to a cooling rack. After the wafer cooled for several minutes, it was developed in a dish of SU-8 Developer (MicroChem) for 90 s with ample agitation. When removed from the developer the wafer was sprayed well with IPA, then DI water. A final ramped hardbake was then performed. The wafer was put onto a cold hotplate, and the hotplate was turned up to 50° C. After 7 minutes, the hotplate was turned up to 100° C and left for 7 more minutes. Then the hotplate was turned up to 150° C and left for 7 minutes. Next the hotplate was turned down to 100° C and left for 7 minutes. Then the hotplate was turned down to 50° C and left for 7 minutes. Lastly the hotplate was turned off and the wafers were left on for 7 minutes, then removed from the hotplate. The thickness of the SU-8 measured with a profilometer was 1.4 μm.

4.3.2 Multiplexing Measurements with Graphene FET arrays

I performed multiplexing experiments using the 1x2 arrays of graphene FETs. The first graphene FET is referred to as channel 1 (CH1), and the second is referred to as channel 2 (CH2). Carrier frequencies of f_{c1} = 79 kHz and f_{c2} = 89 kHz respectively were used for the two devices. Signals (either sinusoids or Gaussian pulses) were applied to each gate electrolyte. The multiplexed current was sent out on a single line and, after amplification and digitization, was recorded as a function of time.

Once the multiplexed current has been collected, the process for reconstructing the original signals from a multiplexed current is similar as described in Section 4.2.1. In the case of two channels with carrier frequencies f_{c1} and f_{c2}, two parallel processes are performed, one for each channel. The frequency spectrum of the multiplexed current from a 1x2 graphene FET array is shown in Figure 4.14a. In the case of Figure 4.14a, Gaussian pulses were applied to each gate with T = 25 ms. The two largest peaks are at the carrier frequencies. The space between the two channel bands is the guard band, which needs to be large enough to prevent the sidebands from the two channels from overlapping. Figure 4.14b shows a closer look around f_{c1}. The characteristic spikes of the Gaussian pulses are observable for about a 400 Hz wide band, which indicates that the most effective pass band when processing the signal is f_{c1} +/- 200 Hz. After appropriate bandwidths are identified for each channel, a bandpass filter is applied to the raw data; reconstructing the channel 1 data uses a BPF centered on f_{c1} while reconstructing the channel 2 data uses a BPF centered on f_{c2}. The highlighted region in Figure 4.14b shows the pass band for each of the two filters. Next both data sets are demodulated (squared), and a BPF is applied to both channels with f_{cutoff} equal to the bandwidth of the applied gate signal to filter out the carriers. Each data point is multiplied by two (to correct for the smoothing step) and the square-root of each channel is taken (to

correct the amplitude from squaring). Lastly each channel is multiplied by its transconductance to yield the gate voltage detected by each channel as a function of time. This reproduces the change in gate voltages detected by each channel.

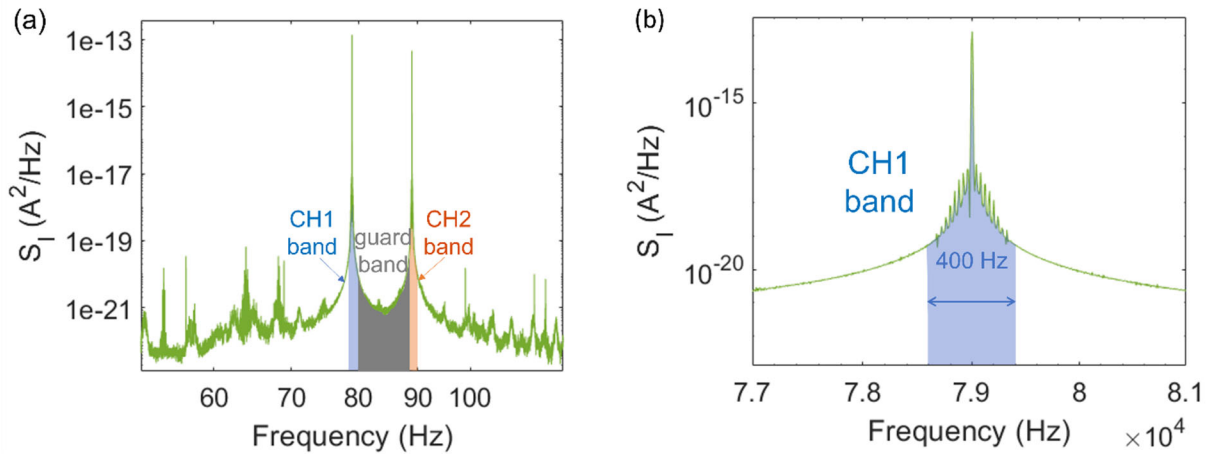

Figure 4.14: Frequency spectrum of multiplexed current from 1x2 graphene FET array. (a) The multiplexed current has two large peaks, one at each carrier frequency. The region in between the bands for both channels is called the guard band (highlighted in grey). (b) Around the CH1 carrier frequency, the Gaussian pulse spectrum is observable as the peaks with $1/T = 40$ Hz spacing. This is useful to examine before DSP to identify the best pass band to use when processing the data. In this case, $f_{c,1}$ +/- 200 Hz is the ideal passband, which is highlighted in blue.

Gaussian gate signals separated by 180° were applied to each channel as shown in Figure 4.15a. The multiplexed current was collected, and DSP was performed. The reconstructed signals are shown in Figure 4.15b and c. The SNR for the 20 mV Gaussian signal (Figure 4.16b) is 110 for CH1 and 50 for CH2. For the 2 mV applied signal, the SNR is 13 for CH1, and 5.1 for CH2. The SNR for both signal sizes is larger than the SNR of equivalent DC measurements.

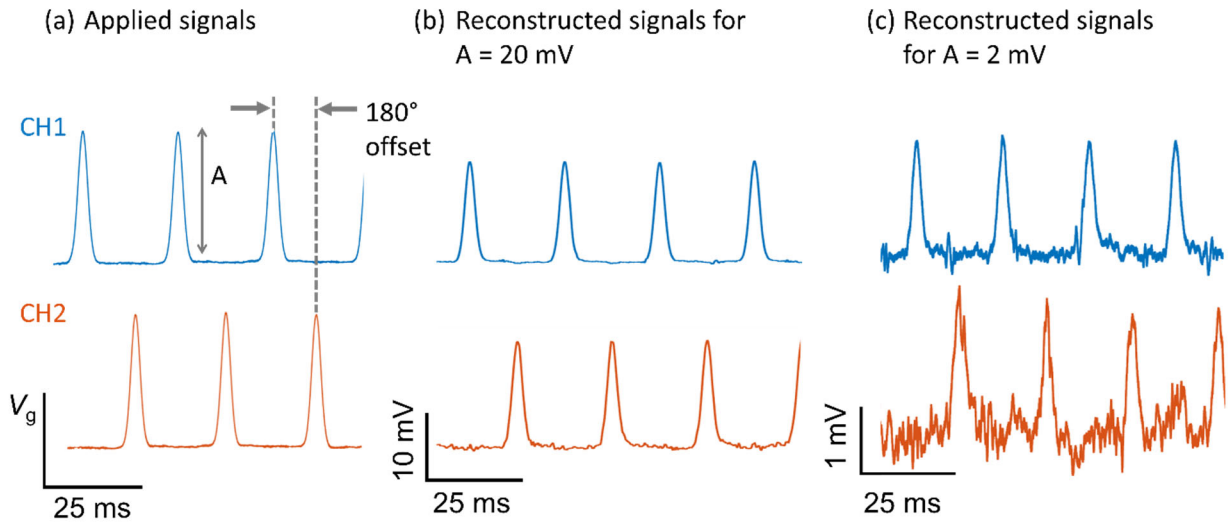

Figure 4.15: Multiplexed current from 1x2 array of graphene FETs. (a) The applied gate signals for each channel are Gaussian pulses, with period $T = 25$ ms, and are offset by 180°. (b) The reconstructed signals from the multiplexed current. Here the applied signals were 20 mV in amplitude. The filter width was 1 kHz. (c) The reconstructed signals from applied signals 2 mV in amplitude. The filter width was 1 kHz.

Figure 4.16 compares a reconstructed signal (top) and a signal measured with a DC bias (bottom). The applied signal was a 20 mV Gaussian, with $T = 25$ ms for the multiplexed (AC) data and $T = 20$ ms for the DC data. The multiplexed data had a SNR of 110, while the DC measured signal has a SNR of 70. The signal sizes in the AM and DC data are the same, and the noise is slightly lower in the multiplexed data. In the next section I will address crosstalk between channels and how our wafer design was improved to prevent it.

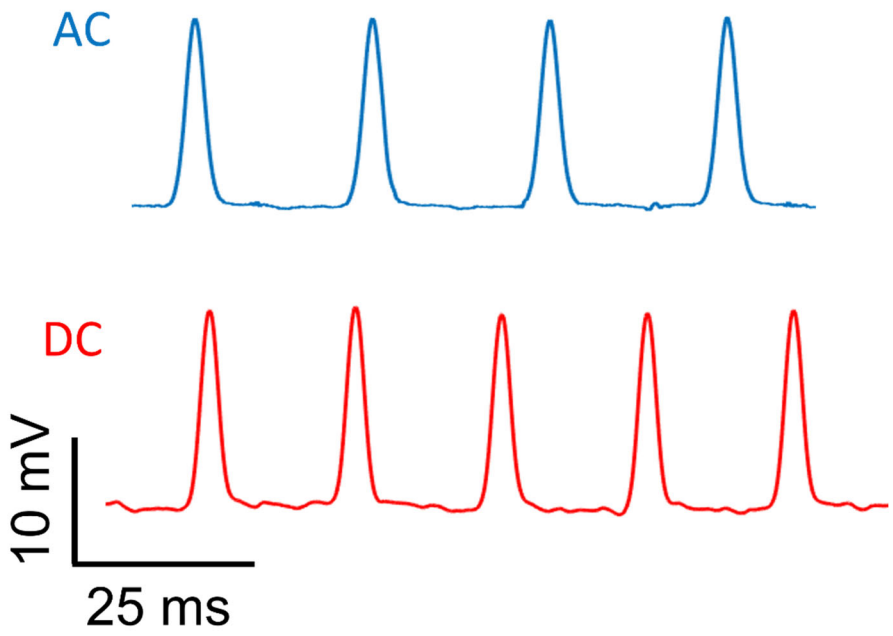

Figure 4.16: Reconstructed signal compared to DC signal. The reconstructed signal (top) has a similar SNR as the DC signal (bottom), indicating that multiplexing does not introduce noise or significantly reduce signal size.

4.3.3 Crosstalk between Channels

Ideally, there should be no crosstalk between channel 1 and channel 2. I tested for crosstalk by applying a signal to gate 1, while gate 2 is held at constant voltage. If there is crosstalk, the reconstructed signal associated with channel 1 will appear in the reconstructed signal associated with channel 2 (see Figure 4.17b).

An early design of the 1x2 GFET array showed significant crosstalk from channel 2 into channel 1 (Fig. 4.17b). The gate voltage waveforms applied to channel 1 and channel 2 are shown in Figure 4.17a. The resulting reconstructed signals are shown in Figure 4.17b. The inset of Figure 4.17b shows the design of the wafer. Note that the source lead for device 2 goes underneath the liquid gate of channel 1. We suspect that gate 1 was unintentionally coupled to the source of device 2. This explanation is consistent with the absence of crosstalk from channel 2 into channel 1. In later designs of the wafer, the electrodes for each device do not pass underneath the gate liquid corresponding to the opposite channel (see Figure 4.12b). No crosstalk occurred in the new design, as shown in the data in Figure 4.17c.

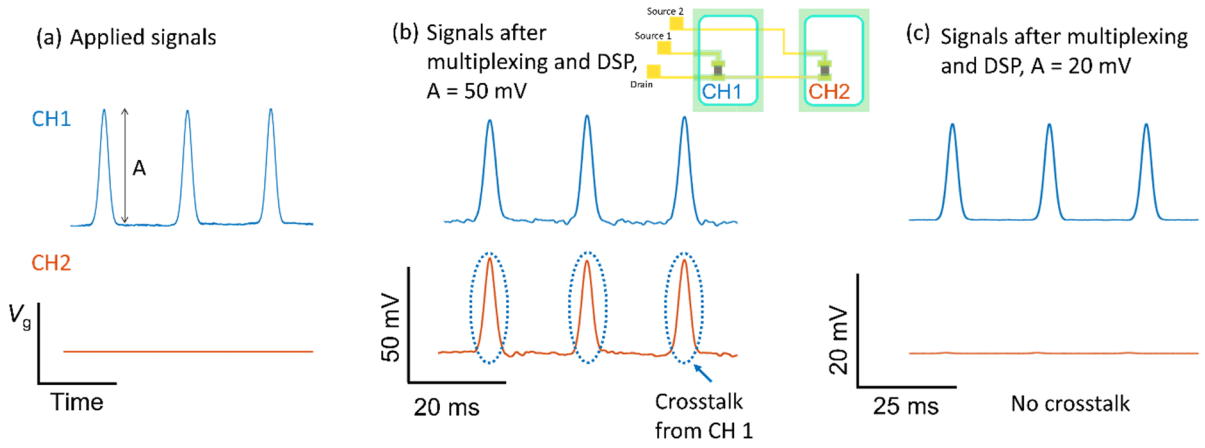

Figure 4.17: Comparison of crosstalk with different wafer designs. (a) The signals applied to each graphene FET gate. The results after multiplexing and DSP with (b) an earlier wafer design where crosstalk between the channels was present (design in inset), and (c) an improved wafer design where crosstalk was not present.

4.3.4 Extending to a Larger Array

Our scheme can be extended to larger arrays of graphene FETs. An array can be formed with rows and columns of sensors, as illustrated in Figure 4.18. Each column of graphene FETs can share a V_{sd} with a carrier frequency f_c, while each row can share an output wire. For a square array of N sensors, the number of input wires providing V_{sd} would be $\sqrt{N}$. The number of output wires from all the rows is $\sqrt{N}$. Therefore, the total number of wires needed to monitor an array of N sensors is $2\sqrt{N}$. This is much smaller than the "N wires for N sensors" limit for sensors that don't use multiplexing. For example, 180 wires could be used to build a sensor array with 8100 channels (compared to a passive array with 180 channels).

The number of channels is restricted by number of frequency bands available for multiplexing. For a graphene FET with channel dimensions W = 50 μm and L = 50 μm, we earlier estimated the maximum carrier frequency as about 880 kHz. The minimum carrier frequency must be greater than the second harmonic of the highest carrier frequency, which is 440 kHz. A possible set of 44 unique carrier frequencies is {450 kHz, 460 kHz, 470 kHz… 880 MHz}. This set of carrier frequencies allows for sensing signals up to 1 kHz with a guard band of 8 kHz separating each frequency band. If 44 wires are used as output wires, and 44 wires are used to supply the carrier frequencies, the system could handle 1936 sensors.

There is a fabrication challenge associated with insulating crossed wires. As shown in Figure 4.18, the output leads must be insulated from the V_{sd} wires. Garcia-Cortadella et al. recently solved this

fabrication challenge.[23] A first layer of metal is covered by a polymer layer. Then through-hole vias are made in the polymer layer and filled with metal. Then a top layer of metal is fabricated, and finally, graphene is transferred.

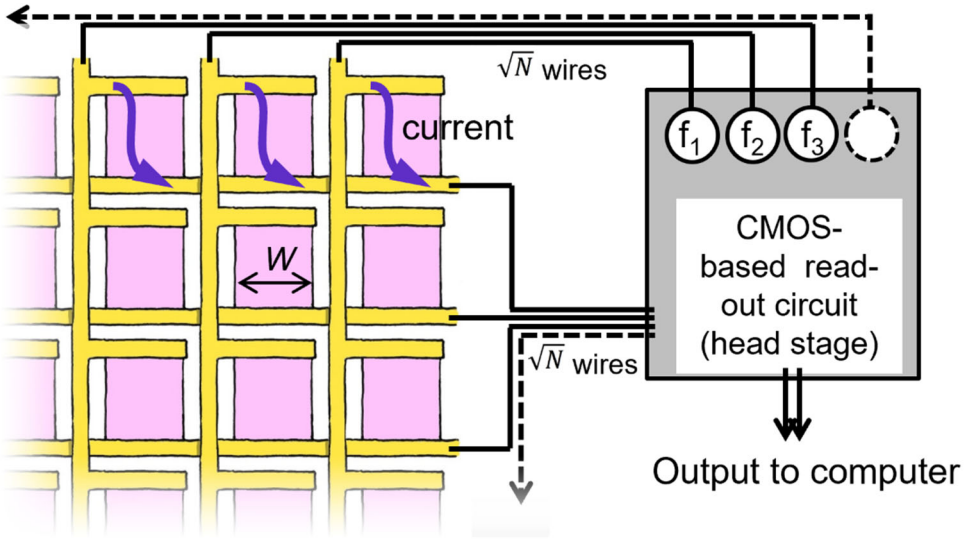

Figure 4.18: Array of graphene FETs. The pink rectangles represent graphene channels, and the gold are source and drain leads. The first column of devices is driven at carrier frequency f_1, the second column is driven at carrier frequency f_2, etc. Each row of devices shares a drain. For an array of N total sensors, $\sqrt{N}$ input wires are needed to provide V_{sd} to each column, and $\sqrt{N}$ output wires are needed to carry the multiplexed signal from each row out to the IC chip. The total number of wires needed to read all the channels in an N sensor array is $2\sqrt{N}$.

A 45 x 45 array of 50 μm x 25 μm channels with a 50 μm pitch would around 5 mm x 5 mm. This is within the possible size of a wet transferred piece of CVD grown graphene. The 50 μm pitch would allow flexibility of the lead width, which is important to consider as decreasing the lead resistance may help reduce crosstalk when using a large array of devices[23].

4.4 Integration of Graphene FET Array with Integrated Circuit Chip

Large arrays of graphene FETs will require many signal generators, many current amplifiers and many digital-to-analog converters. To provide the large number of carrier frequencies necessary for an array of graphene FETs, as well as the possibility of signal demodulation in real-time, we collaborated with Dr. Matt Johnston (ECE department, Oregon State) and his graduate students, who designed an IC chip to replace the large electronic components (the current amplifier, the anti-aliasing filter, and the DAQ) in our system. In this configuration, the multiplexed current from the graphene FETs is sent directly into the IC chip. The output from the IC chip is a voltage proportional to the multiplexed signal

that is sent into a logic analyzer, which interfaces with a computer to record the data. Our early results from interfacing the IC chip with our 1x2 graphene array (channels shared a gate voltage) were published in IEEE Transactions on Circuits and Systems II[61].

4.4.1 Description of IC Circuit

The first stage of the IC chip is a transimpedance amplifier with adjustable gain that amplifies the multiplexed current and converts it into a voltage signal. The next stage is an analog-to-digital converter (ADC) that converts the analog voltage signal into a digital signal. The digital voltage signal is sent into a logic analyzer, and the output of the logic analyzer is then sent to the computer to be saved and analyzed. A diagram of the graphene FET-IC chip system is shown in Figure 4.19.

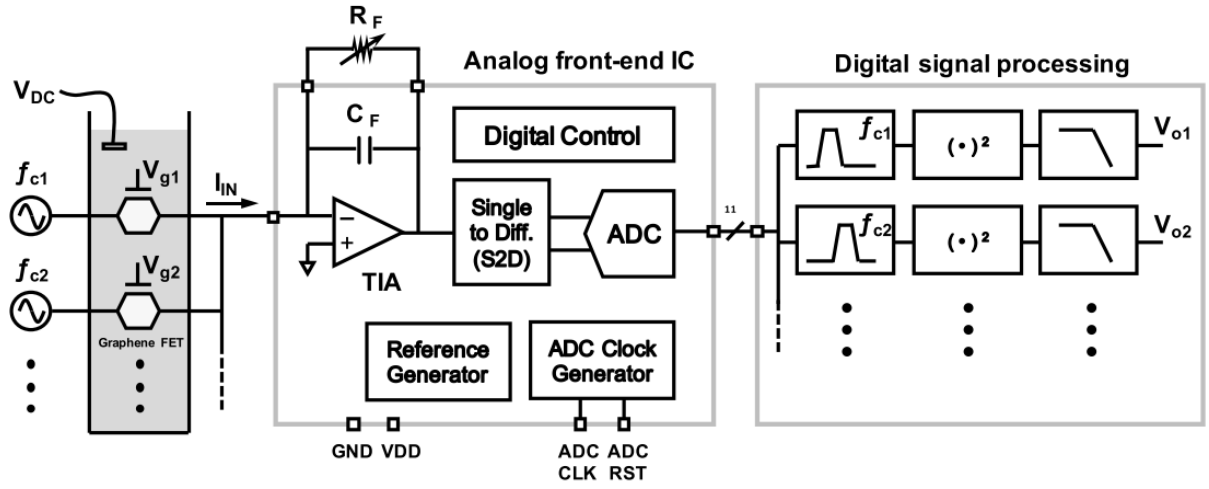

Figure 4.19: Graphene FET-IC chip diagram. The graphene FET array is on the left. The current output from the array goes to the IC chip (center). The IC chip contains a transimpedance amplifier (TIA), a single to differential, and an ADC. The output from the ADC is then processed using MATLAB.

A capacitor is used between the IC chip and the graphene FET because there is a mismatch in the voltage level offset between the two components. The data collected is thus AC coupled rather than DC coupled. Changes in the gate voltage are the desired information read from the graphene FETs, so AC coupling is acceptable. The first iterations of the IC chip design do not provide the source-drain carriers for the graphene FET channels, though that is a goal for future designs. Another goal for future designs is adding an FPGA that provides real-time demodulation of the multiplexed signals.

4.4.2 Graphene FET to IC Chip Data

We published our first iteration of interfacing the graphene FETs with the IC chip in 2021[61]. The graphene FET wafer was an earlier design with a 1x2 array with a shared gate, so the same gate signal was applied to each device (though each had a different source electrode and carrier frequency), as shown in Figure 4.20a. The general structure of the IC chip used to collect the data in Figure 4.20 was the same as Figure 4.19, but the core amplifiers were different. The reconstructed signal from multiplexed current measured with the graphene FET + IC chip system is shown in figure 4.20b. Gaussian pulses with 50 mV amplitudes were applied to the shared gate.

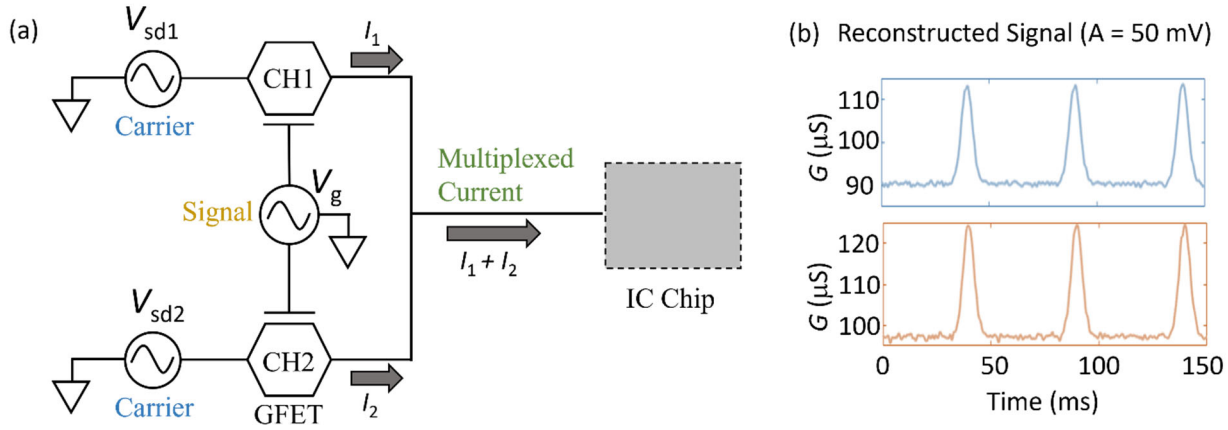

Figure 4.20: First data collected from graphene FET-IC chip interface measurements. (a) The testing circuit. Note that the two graphene FETs share a liquid gate but have individual source electrodes. (b) The reconstructed signals from both channels. In this case the change in conductance is plotted, which is proportional to the change in gate voltage.

The most recent iteration of graphene FETs (with individual gates) was interfaced with the most recent IC chip iteration. Figure 4.21a shows the signals applied to the gates of each graphene FET channel. Figure 4.21b shows the reconstructed signals for a 20 mV amplitude Gaussian signal, with a SNR of 5-10 (compared to a SNR = 50-100 for the same signal applied to a graphene FET interfaced with standard instrumentation). Figure 4.21c shows the reconstructed signals when a 10 mV signal is applied to the gate, at which point the noise level is almost equivalent to the signal size.

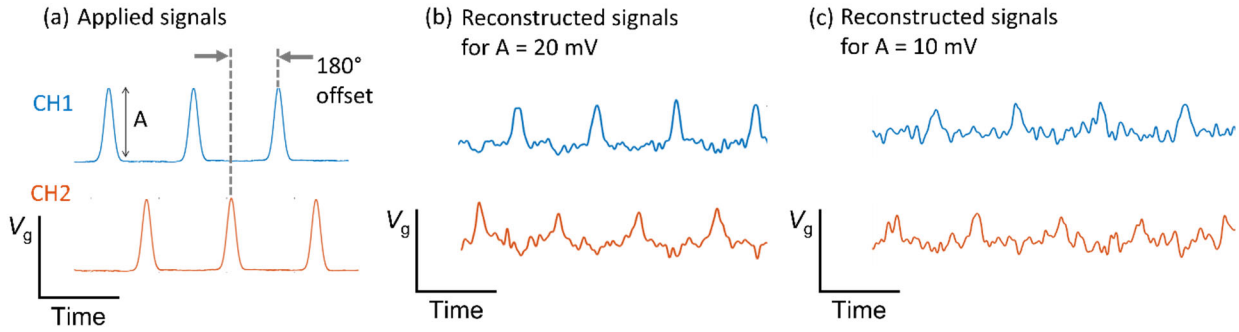

Figure 4.21: Multiplexed and reconstructed data from the graphene FET-IC chip system. (a) The V_g signals applied to each graphene FET channel. (b) The reconstructed signals from each channel with a 20 mV signal applied. (c) The reconstructed signals from each channel with a 10 mV signal applied. The signal is barely distinguishable from the noise.

More work is needed to reduce the noise level of the joint system to reach the desired operating point. However, this is a promising step towards interfacing our graphene FETs with custom IC circuits, which can enable many-channel recordings from a large graphene FET array.

4.5 JFET Model Cell

When working with the IC chip, we found that a junction field-effect transistor (JFET) could act as a stand-in (or "model cell") for a graphene FET. When using a graphene FET it is operated in a region where I is linear with respect to V_g, i.e. dI/dV_g is constant, as discussed in Chapter 2. This region needs to span about 100 mV in V_g. To mimic the behavior of a graphene FET in the testing regime, we needed to find a JFET with a linear I vs V_g curve with a similar current and transconductance dI/dV_g to a graphene FET. We found a JFET (InterFET 2N4339) that matched the parameters of a graphene FET when operated around Vg = -1.1 V. The JFET curve shifted along the x-axis to line up with a graphene FET curve is shown in Figure 4.22. The current and the transconductance of the JFET are very well aligned with those of the graphene FET, showing the JFET can approximate the graphene FET behavior accurately.

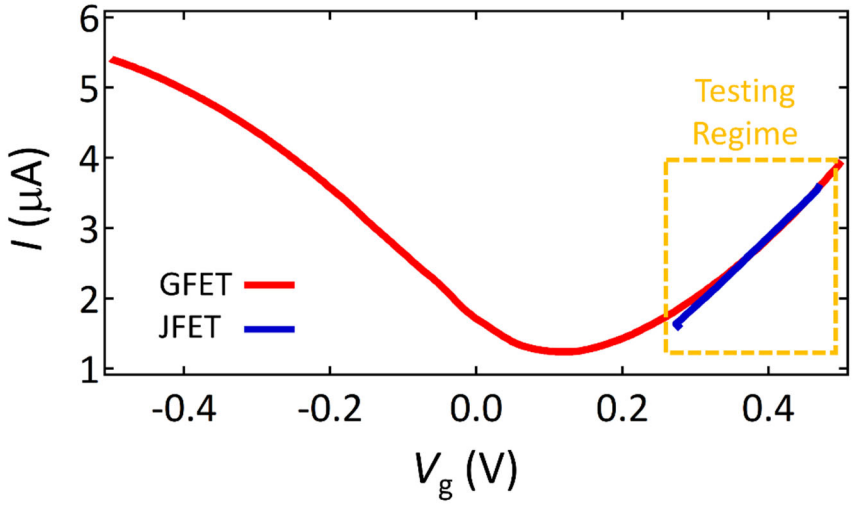

Figure 4.22: Current vs gate voltage of a graphene FET and a JFET. The operating region is enclosed in the yellow box. Note that the magnitude of the current and the slope dI/dV_g are very similar for the two devices. The JFET curve has been shifted by $V_g = 1.5$ V to align with the graphene FET curve.

Multiplexing was performed with a 1x2 array of JFETs. The experimental setup is shown in Figure 4.4, with JFETs in place of graphene FETs. The results for 2-mV Gaussian signals (with $T = 25$ ms and $T = 5$ ms, respectively) are shown in Figure 4.23.

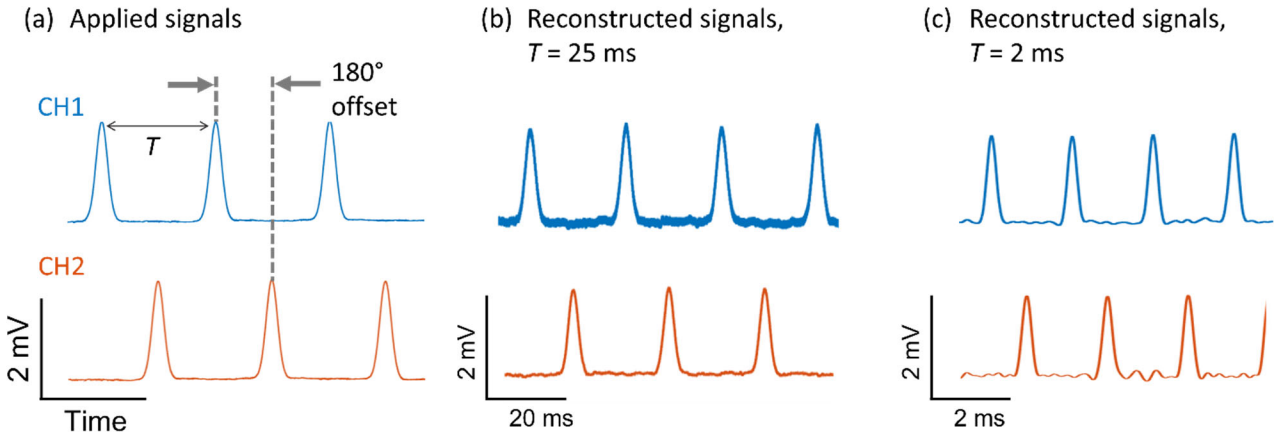

Figure 4.23: Amplitude modulated signals from a JFET. (a) The signals applied to each individual gate. The amplitude is 2 mV, the period is T, and the offset is 180°. The reconstructed signals from each channel for (b) $T = 25$ ms, and (c) $T = 2$ ms.

The reconstructed signals in Figure 4.23b and c have an SNR between 30 and 60. This is similar to the multiplexed reconstructed graphene FET signals when the applied gate signal is 20 mV. On the other hand, when the 2 mV signal is applied to the gate, the JFET has a much larger SNR than the graphene FET (50 compared to 5-10). The small voltage signals multiplexed by the JFETs verify the low

noise level of our measurement system (amplifier, filters, DAQ, and wired connections). and indicates that the noise in the multiplexed graphene FET data with 2 mV signals (4.15c) is due to the graphene FET itself and not electronic noise due to the instruments. No crosstalk is present between the JFET channels.

The model cell is useful when trouble-shooting a system that adjoins a graphene FET, like an IC chip. It allows testing of the read-out circuitry without access to an expensive, custom-made protype of graphene FETs.

4.6 Conclusion

In this chapter, I started by showing that graphene FETs can generate AM signals at the sensor site. Then I applied the distributed-element model to the graphene-electrolyte system and used it to relate the dimensions of the graphene channel to the maximum usable carrier frequency. Then I demonstrated multiplexing using two channel of graphene FETs with a novel wafer design with two liquid gates. I showed multiplexing of higher frequency signals than had been demonstrated previously in graphene FETs (200 Hz in previous work vs 1 kHz in my work), and that crosstalk between the channels could be mitigated using wafer design. I predicted that this scheme could be extended to an array of 2000 graphene FETs contacted by fewer than 100 wires. Lastly, I showed preliminary data from interfacing our graphene FET array with a custom IC chip .

CHAPTER 5: GRAPHENE FIELD-EFFECT TRANSISTORS AND IN-VITRO CELLS

5.1 Introduction

Looking at the functioning of individual neurons is an important step for understanding large-scale processes of the brain, like thoughts, behaviors, and degenerative diseases. Silicon shanks, microelectrode arrays (MEAs), and patch-clamps are well-established tools for electrically measuring neurons in the brain; however, each tool has its limitations. While silicon shanks can take measurements with high temporal resolution and resolve individual action potentials[62], the rigid, crystalline structure has limited compatibility with soft tissue due and can cause damage to the tissue upon insertion[4]. MEAs can have the same issue when fabricated on rigid substrates. Some MEAs are made on flexible substrates that can conform to soft tissue but many suffer from a poor signal-to-noise ratio (SNR) at frequencies > 1 kHz where individual action potentials are found[62]. Whole cell patch-clamps are capable of high resolution, high SNR measurements, but break the cell membrane to take the recording, which means the cell dies when the probe is removed. There exists a need for a tool that can conform to soft tissue and measure individual action potentials without damaging the cells.

Graphene is a soft, flexible material with a low bending stiffness[33], so it can be fabricated onto flexible substrates to be mechanically compatible with soft tissue. Furthermore research from the last decade shows the high SNR of graphene FETs used for measuring the electrical activity of cells. The first in-vitro experiment demonstrating graphene FETs measuring cell activity was published in 2010 by the Lieber group, monitoring the conductance of a graphene channel to measure the spontaneous electrical activity of cardiomyocyte (heart muscle) cells[63]. They achieved a SNR of about 4. The first in-vivo measurement was published by Garrido et al in 2017[14], taken by placing an array of graphene FETs on a flexible substrate onto the surface of a rat's brain. They monitored the current through the graphene channel and used the transconductance dI/dV_g to calculate the change in voltage local to the graphene channel. The average SNR of spontaneous brain activity was around 9. The study measured low-frequency averages of neuronal activity called local field potentials (LFPs) in the 20 - 200 Hz band as opposed to individual cell signals but did demonstrate the utility of graphene FETs in-vivo. My work in chapter 3 and in this chapter shows that graphene FETs can achieve noise levels on the order of 100's of μV for the band 1 Hz – 10 kHz, which is the relevant frequency band for biosensing[35].

We have adopted a model developed by prior researchers to explain the coupling of the electrical activity of cells with the sensor channel[25,64]. This model will be refined and discussed in section 5.2, and it predicts that the strength of the signal measured by the graphene FET will depend on the distance

between the graphene channel and the cell membrane. In this chapter, we investigate this relationship, and whether the flexibility of graphene can be leveraged to increase the SNR by decreasing the channel-cell distance.

First, I will explain the circuit model used to describe the graphene-cell interface. Next, I measure action potentials of cells grown on top of graphene FETs on a substrate. This demonstrates that my graphene FETs are capable of measuring action potentials, as well as allows us to calculate the SNR for the configuration of a cell resting on top of a graphene channel. Then I will discuss our free-floating graphene FETs that use the full flexibility of graphene to conform to single cells and how I put them on top of cells to attempt to decrease the channel-cell distance and boost the measured signal.

5.2 Model of the Bioelectronic Interface

Prior researchers have developed a circuit model of the sensor-cell interface[24,25,64] and a quantitative analysis will be explored in this section shortly. First to understand qualitatively how graphene senses individual action potentials consider what occurs when a neuron fires. The electric potential difference between the interior and exterior of the cell is called the membrane potential. For neurons at rest, the membrane potential is approximately -70 mV[20]. When a neuron fires, there is a rapid change in the membrane potential that lasts a few milliseconds and reaches approximately 40 mV. An example of the membrane potential as a function of time during firing is shown in Figure 5.1a. The potential changes are facilitated by the transport of ions into and out of the cell via proteins in the cell membrane called ion channels. The main charge carriers in a neuron are sodium ions and potassium ions[20]. When a graphene channel is located near ion channels, as shown in Figure 5.1b, the movement of the ions and the subsequent change in the local voltage gates the graphene channel and is detected as a change in the graphene channel current (or alternatively, change in the channel conductance).

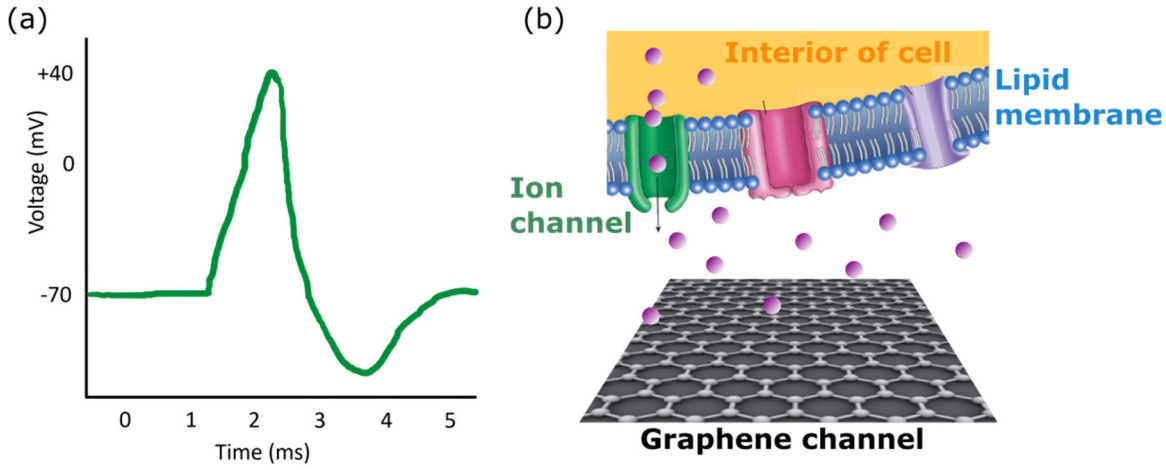

Figure 5.1: Action potential generated by a cell. (a) A representation of the membrane voltage during an action potential from a neuron. (b) An illustration of the interface between a cell and graphene. The ion channels in the cell membrane are near to the graphene surface, resulting in local changes in the electric potential gating the graphene as ions are ejected from the channels.

Now that we have a qualitative picture of how a graphene channel senses the action potential of a neuron, we can use established models that been developed to explain the coupling of a sensor channel of a FET with the membrane potential of a neuron in a fluid[24,25,64] to look at the interface quantitatively. The circuit model representing a cell and a sensor is shown in Figure 5.2a.

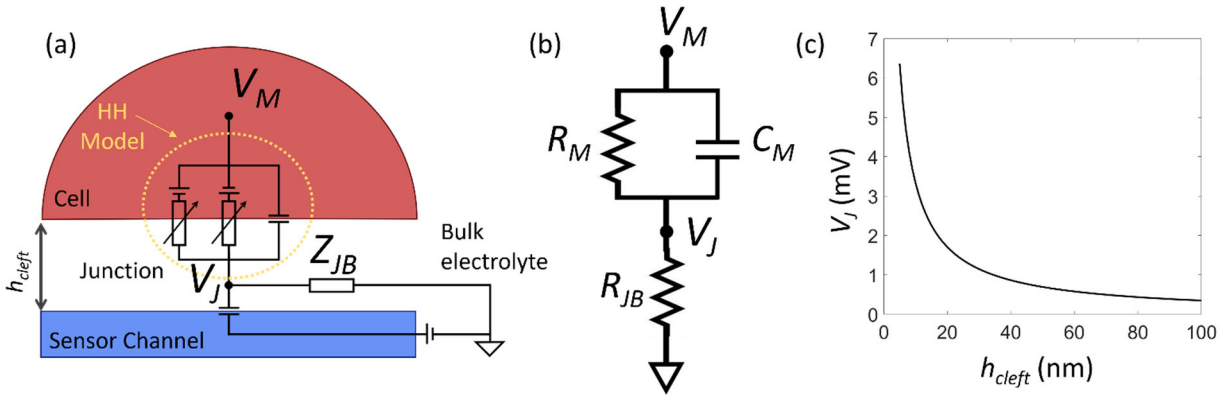

Figure 5.2: Circuit model of the cell and sensor. (a) A circuit model of a sensor (blue) and a cell (red). The Hodgkin-Huxley portion of the circuit is circled and labeled "HH Model". In a simple model, the impedance between the junction and the bulk fluid Z_{JB} is modeled as a resistor R_{JB}. (b) A simplified version of the circuit in (a). The membrane resistance R_M and the junction-bulk fluid resistance R_{JB} form a voltage divider. The membrane potential V_M and the junction potential V_J can be related using this circuit. (c) The magnitude of the junction potential V_J as a function of the distance of the cell from the sensor, h_{cleft}, for $V_M = 70$ mV and $R_M = 1$ GΩ. V_J is about 10% of V_M at $h_{cleft} = 5$ nm.

The sensor channel is shown in blue, with the cell shown in red. The membrane potential of the cell is V_M and it is what we want to measure. The distance between the sensor channel and the cell is h_{cleft}. The region of fluid between the cell and the sensor is called the junction. The junction potential V_J is what gates the channel and is measured by the sensor. Ideally we could directly probe the membrane potential such that $V_J = V_M$; however, V_J depends on both the membrane potential V_M and the impedance between the junction and the bulk electrolyte Z_{JB}. We will establish a relationship between the voltage measured by the sensor V_J and the membrane potential V_M as a function of the distance between the sensor and the cell h_{cleft} by the end of this section, but first we'll discuss the circuit in Figure 5.2a.

The large circuit in Figure 5.2a can be thought of as three relatively simple circuits, each describing one of the interfaces in the system; these interfaces are the cell with the junction, the junction with the sensor channel, and the junction with the bulk electrolyte.

The interface between the cell and the junction is described by the well-established Hodgkin-Huxley model[65], which represents the ion channels as variable conductors and the electrochemical gradients across the membrane as voltage sources. The part of the circuit represented by the Hodgkin-Huxley model is circled in Figure 5.2a. Each ion species has its own associated conductance and voltage, i.e. each branch on the Hodgkin Huxley model is for one ion type. Figure 5.2a shows the circuit when two ion species are included in the model. The ions important to our experiment are those most heavily correlated with the cells firing, which are sodium, Na^+, and potassium, K^+. The concentration of potassium is higher inside the cell than outside the cell at equilibrium[20], so the electrochemical gradient creates a force on the ions to out of the cell, and hence the voltage source on the potassium branch of the circuit has the negative terminal towards inside the cell. The concentration of sodium is higher outside the cell than inside the cell at equilibrium, and so the voltage source associated with the electrochemical gradient of sodium is faced the opposite direction. The lipid membrane is represented as a capacitor with voltage V_M (for membrane in contact with the bulk electrolyte) or V_M - V_J (for membrane in contact with the junction) across the plates.

The interface between the cleft and the sensor channel is represented by a single capacitor; this representation is referred to as the point-contact model[25]. The voltage of the junction V_J is what gates the graphene channel, and so changes in the current measured through the graphene channel (or, alternatively, the channel conductance) are proportional to changes in V_J.

The interface between the cleft and the bulk fluid is represented by a current pathway with an impedance. This pathway is important because it affects the junction voltage V_J, which in turn affects the reading made by the sensor. When the sensor forms a tight seal with the cell, the physical pathway from

the junction to the bulk electrolyte can be small, resulting in ion accumulation in the junction; in this case the pathway impedance Z_{JB} must account for ion concentration differences for each ion type and charge imbalances between the bulk fluid and cleft[25]. For sensors that form a weak seal with the cell, the pathway from the junction to the bulk fluid is large enough that the ions can diffuse freely between the junction and bulk fluid and the pathway can be represented by a simple resistor[64].

By treating the pathway as a simple resistor, and the cell membrane-electrolyte interface as a single resistor R_M and a capacitor C_M, as shown in Figure 5.2b, a relationship between the membrane potential V_M and the junction voltage V_J as a function of the cleft height h_{cleft} can be established. To do so, first note that the circuit in Figure 5.2b can be treated as a voltage divider with $V_{in} = V_M$ and $V_{out} = V_J$. The two resistors in the divider are the membrane resistance R_M and the resistance between the junction and the bulk fluid, R_{JB}. These quantities are related by the equation for a simple voltage divider

$$V_J = V_M \left(\frac{R_M R_{JB}}{R_M + R_{JB}} \right). \tag{5.1}$$

The membrane resistance R_M is approximately 1 GΩ. The magnitude of the membrane potential V_M reaches a maximum of 70 mV. The junction-bulk fluid resistance R_{JB} can be estimated as a function of h_{cleft} and substituted into Equation 5.1 to find V_J as a function of h_{cleft}.

For a biological electrolyte, the bulk resistivity is $\rho \approx 0.5$ Ωm. The resistance between the junction and the bulk fluid R_{JB} can be estimated by the equation

$$R_{JB} = \rho \frac{L}{A}, \tag{5.2}$$

where A is the cross-sectional area of the escape pathway and L is the length of the escape pathway. The area A is the width of the junction W times the cleft height h_{cleft}. If we approximate $W = L$, then Equation 5.1 becomes

$$R_{JB} = \frac{\rho}{h_{cleft}} = \frac{500\ \Omega\ \text{nm}}{h_{cleft}}. \tag{5.3}$$

As the cleft height decreases, the junction resistance increases. By substituting Equation 5.3 into equation 5.1 the relationship between the cleft height and the junction voltage is found to be

$$V_J = V_M \left(1 + \frac{R_M h_{cleft}}{500\ \Omega\ \text{nm}} \right)^{-1}. \tag{5.4}$$

For V_M = 70 mV and R_M = 1 GΩ, we can estimate the voltage measured by the sensor channel, V_J, as function of the distance between the cell and the sensor, h_{cleft}. The results are plotted in Figure 5.2c. As expected, as the sensor gets closer to the cell, the voltage measured by the sensor increases. When h_{cleft} is 5 nm, V_J is about 10% of V_M. This model is limited in use to sensors in close proximity to the cell. For measurements where the cell is far away (5 – 30 μm) from the sensor, detectable signals are on the order of 100 μV[26].

Minimizing h_{cleft} is a potential strategy for increasing the signal (and hence the SNR) measured by a graphene FET. This idea will be further explored in the chapter. First, we will establish a baseline SNR for cells grown on graphene FETs in section 5.4. Then in section 5.5 we will revisit the idea of putting graphene FETs closer to the cell membrane to increase signal size by working with released graphene FETs that are not attached to any substrate, which allows the graphene channels to be placed on top of live cells. Before that, in the following section, we will discuss the methods for taking measurements of live cells with graphene FETs.

5.3 Methods

5.3.1 Device Fabrication

The complete description for fabrication of graphene FETs was described in Chapter 2. Briefly, graphene was transferred to a glass coverslip, which acts as the substrate. Photolithography and plasma etching was used to create the graphene channels. Then source and drain electrodes for each channel were photopatterned and metal was deposited via electron beam deposition. Completed devices are shown in Figure 5.3. This image was taken on an inverted microscope, which is possible due to the transparency of the substrate that the graphene FETs were fabricated on. The dimensions and shapes of the channel were varied, as shown in Figure 5.3. Some of the graphene channels were patterned into simple rectangles (Figure 5.3a and b) while others were made into shapes that decreased the sensor area (“bow ties”, as seen in Figure 5.3c-e).

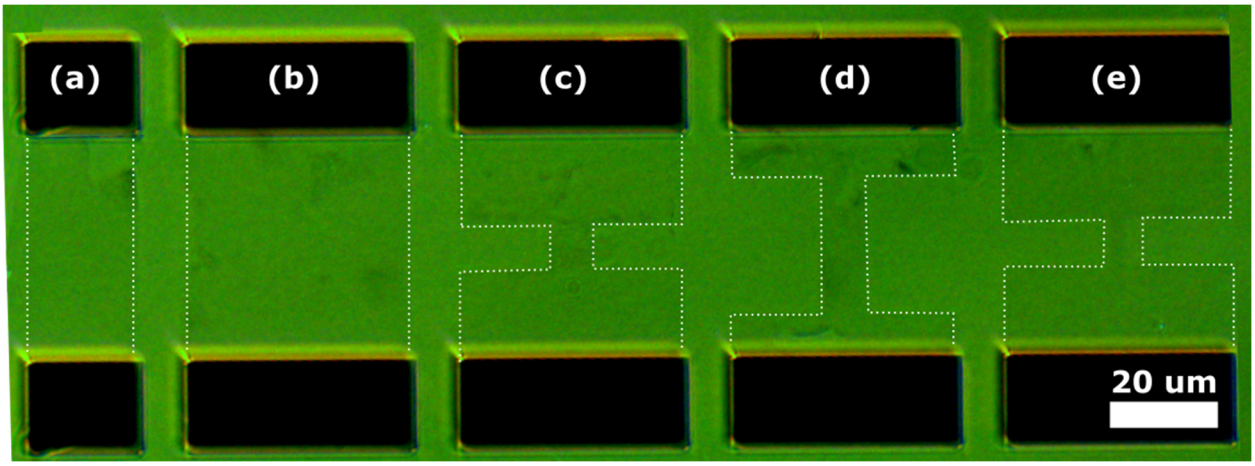

Figure 5.3: Optical image showing graphene FET channel types. Five graphene FETs are shown. The source and drain electrodes for each device are the dark rectangles at the top and bottom of the image, respectively. The graphene channels that connect each source and drain pair are outlined in white dotted lines (the graphene itself is difficult to see on a clear substrate). (a) and (b) are rectangle channel devices, while (c)-(e) are bowtie-type devices. The bowtie devices are designed to have a higher resistance, which may help increase the detected signal size.

The bow-tie shaped channels have a higher resistance in the center of the device compared to the rectangle channels, and so when the centers of the channels are gated with the same size gate signal, the change in channel resistance is greater in the bow-tie channel compared to the rectangle channel. To see why, model a rectangle graphene channel and a bow tie graphene channel as networks of resistors as shown in Figure 5.4. Each resistor piece that makes up the network has resistance R, so the rectangle device in Figure 5.4a has a total resistance of R, while the bow-tie device in Figure 5.4b has a total resistance of $(5/3)R = 1.67R$. Ideally the cell would gate the entire graphene channel. In practice, however, the cell typically gates only a part of the channel because of lack of control of the position of the cell relative to the sensor, and since the potassium and sodium ion channels are localized only above certain areas of the channel. A small sample cell is drawn on each resistor network in Figure 5.5 as an example. Say the cell gates one portion of the graphene channel such that the portion changes resistance by 10% (from R to $1.1R$). Then the new resistance of device (a) will be $1.01R$, which means the total change measured in the graphene channel would be $0.01R$, or 1%. If device (b) is gated by the same cell, resulting in a 10% change in the resistance of the center portion of the channel, the new total resistance of the channel will be $1.57R$, which means the total change measured in the graphene channel would be $0.1R$, or 6%. The bowtie device would measure a larger change in resistance compared to the rectangle device for the same small change in potential. Both rectangle and bowtie type devices are included as testing options on the chip. In the next section I will discuss how the cells are prepared for use with the graphene FETs for in vitro testing.

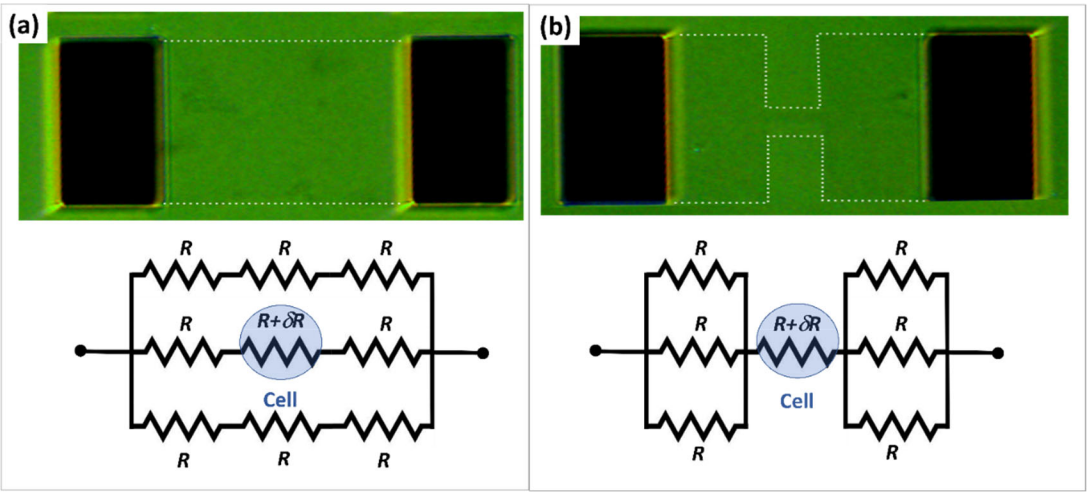

Figure 5.4: Resistor model of the graphene channel. Optical image (top) and circuit equivalent (bottom) of (a) a rectangle device and (b) a bowtie device. The region of each device that is gated by a cell is highlighted with a blue circle.

5.3.2 Cell Culture

For my in vitro experiments, I used KTaR-1 neuronal cells. This cell line was isolated by Dr. Patrick Chappell (College of Veterinary Medicine, OSU). The cell line was derived from primary neurons that were harvested from the hypothalamus of an adult mouse and immortalized (i.e. genetically altered to allow proliferation of the neuron cells that otherwise cannot undergo mitosis nor proliferate)[66]. I maintained my own population of KTaR-1 cells in the Sun lab (OSU Physics) under aseptic conditions. The cells were passaged every 3 days, when reaching about 70% confluency. To passage the cells, first TrypLE Select 1x (Gibco) was added to the vessel containing the cells (5 mL for a 25 cm^2 flask, 9 mL for a 75 cm^2 flask), then returned to the 37° C incubator. TrypLE Select contains the enzyme trypsin that facilitates detachment of the cells from the substrate. After 5 minutes the vessel was gently tapped on, then examined under a microscope to ensure most of the cells had released and were floating in solution. The vessel was returned to the incubator for 1-2 minutes if needed. The floating cells in trypsin were transferred to a 15 mL centrifuge tube and centrifuged for 5 minutes at 1000 RPM. Centrifuging causes a cell pellet, or conglomeration of cells, to form in the bottom of the tube. The liquid was emptied from the centrifuge tube with a pipette while keeping the cell pellet at the bottom. One mL of growth medium heated to 37° C was added to the tube and the cell pellet was gently sucked into and out of a pipette several times to break it up. The growth medium was mixed in-lab and contains 88% Dulbecco's Modified Eagle Medium (Gibco), 10% fetal bovine serum, and 2% penicillin streptomycin (Gibco). Then an amount of the cell pellet solution was added to a clean vessel; for a 60 mm petri dish, 30 µL of cell pellet solution plus 3 mL of warmed growth medium was added, and for a 25 cm^2 flask, 50 µL of cell

pellet solution plus 6 mL of warmed growth medium was added. The passaged cells reattach to the bottom of the vessel and continue to proliferate. Cells were discarded after around 15 cycles and restarted from earlier generations that had been cryo-frozen.

To get the cells onto a substrate containing graphene FETs or onto a plain coverslip, the substrate was added to the petri dish for cells to be passaged onto. The cells adhere without issue to the glass, graphene, and gold. After transferring the passaged cells to the petri dish containing the chip, the dish was put in the incubator for 24-48 hours to allow the cells re-adhere to the substrate and to reach a proper density for testing. The ideal testing density was approximately 20-40% confluency, which was high enough that many devices had cells growing on the graphene channel to allow for many potential testing sites, but low enough that most of the testable sites had one, rather than many, cells growing on the graphene channel in order to study the signals from a single cell rather than multiple cells at once. At the time of testing, several drops of 40 mM KCl solution was added to the cell medium to stimulate cell firing. In the next section, the setup used to take data from the KTaR-1 cells using the graphene FETs is described.

5.3.3 Electrical Measurement Setup

The setup for measuring graphene FETs with cells grown on them is shown in Figure 5.5. The graphene FETs coverslip was placed onto the stage over the inverted microscope objective. Approximately 150 μL of Dulbecco's Modified Eagle Medium (DMEM) (Gibco) was added to the chip, which acted as the liquid gate for the graphene FETs and kept the cells alive during the data acquisition. The surface tension of the DMEM was strong enough that the fluid stayed on the chip without additional measures. Contact was made to the source and drain electrodes using high impedance (0.1 MΩ) monopolar probes (Microprobes for Life Sciences). Each probe consists of either a tungsten or a platinum-iridium (Pt/Ir) wire coated with a 3 um parylene-C insulation layer and a small area of metal exposed at the tip. The insulation layer minimizes faradaic current between the probe and the electrolyte. Electrical contact was made to the probe via a gold-plated pin connector. The Pt/Ir probes offer higher electrochemical stability, while the W probes are mechanically stronger and less likely to bend upon contact with the electrodes or substrate. Little to no differences were observed in the electrical data I took, but lift attempts were marginally more successful using the Pt/Ir probes. When taking a measurement two probes of the same type and impedance were connected to piezoelectric micropositioners (see Figure 5.6b). and lowered from above down onto the chip. This lowering process was done while observing the probe positions through the inverted microscope. The probes were lowered until contact was made with the source and drain electrodes. A voltage was applied across the probes and the current through the

device was measured. The voltage was supplied, and the current was measured by a low-noise current amplifier (Stanford Research Systems SR570), which also applies a LPF of 30 kHz applied. The voltage output of the current amplifier was sent into a DAQ (National Instruments USB-6259), which sampled the current at 20 kHz and read the data into a LabView program, which generated a data file containing the current as a function of time. The electric potential of the liquid was controlled using a silver wire that had been treated with bleach (sodium hypochlorite) to form a Ag/AgCl electrode, with the gate voltage supplied by the DAQ. In the next section, the results from using these techniques to electrically measure KTaR-1 cells grown on top of graphene FETs are discussed.

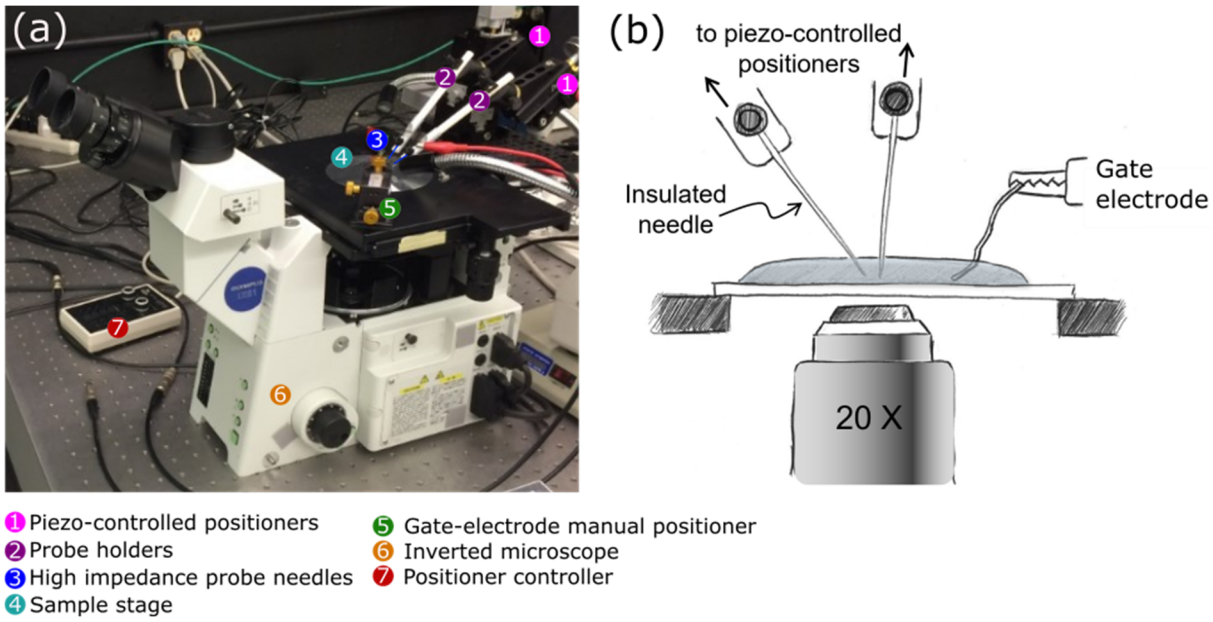

Figure 5.5: The experimental setup used for working with released graphene devices. (a) The inverted microscope with the micropositioners and probes. The source and drain electrodes are contacted with the high-impedance probe needles, which are controlled by piezo-controlled positioners. The (b) An illustrated close-up view of the sample stage, showing the source and drain probes, the gate electrode and gate fluid, and the microscope objective.

5.4 Graphene Devices on Surface

In this section, I show that the graphene FETs I made can measure individual action potentials from neuronal cells. KTar-1 cells were grown onto graphene devices on a coverslip substrate as described in the previous section. The substrate was placed onto the inverted microscope and inspected, looking for devices that have a single healthy cell grown over the graphene (sensor) region. A healthy cell is visually distinguishable from a dead or dying cell; optical images demonstrating the difference are shown in Figure 5.6. Healthy cells (shown in Figure 5.6a) are attached to the substrate and spread out while dead and dying cells (shown in Figure 5.6b) are poorly or not at all attached and float, appearing spherical.

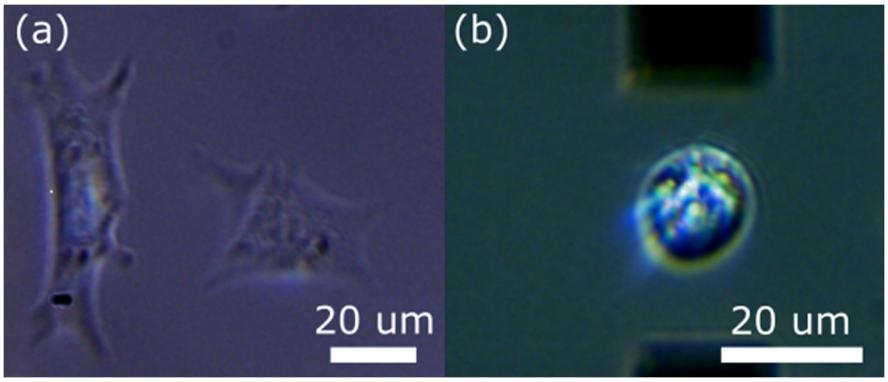

Figure 5.6: Optical images of KTaR-1 cells. (a) Two healthy KTaR-1 neuronal cells are shown. The cells are splayed out with dendrites (the small limbs) extending outward on the substrate from the cell body. (b) This cell is dead or dying. Its dendrites are no longer attached to the substrate, and it is floating in solution. This cell is not a good candidate for electrical study.

The ideal placement of a healthy neuronal cell grown across a GFET sensor is illustrated in Figure 5.7a. As much of the cell membrane as possible should be in contact with the graphene channel, and only a single cell is touching the channel. However, we cannot control where the cells grow on the chip, so using a large number of devices and cells statistically improves the chances of finding an ideally placed cell. Figure 5.7b shows an optical image of a cell grown on a graphene FET channel.

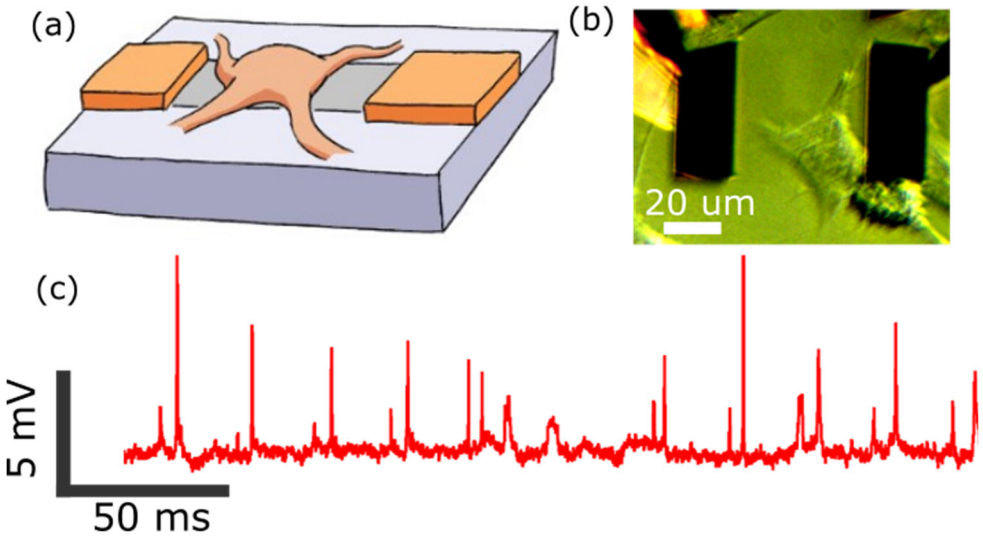

Figure 5.7: Cells grown onto graphene FETs. (a) The illustration shows the ideal placement of a neuronal cell on a graphene FET. A large portion of the cell membrane is overlapping the graphene channel (drawing by Ethan Minot). (b) The optical image of a KTaR-1 cell grown on a graphene FET is shown. (c) This is the change in gate voltage as a function of time for a graphene FET with a cell grown on it. The signals are from ion movement into and out of the cell, which in turn gates the graphene.

When a device with a well-placed cell was located, contact to the source and drain electrodes of the device was made with the high impedance probes. The transfer characteristics curve was taken by sweeping the voltage on the Ag/AgCl gate electrode and collecting the source-drain current. Examples of the transfer characteristics curve were presented in Chapter 2. The global gate voltage was set to a value where the transconductance dI/dV_g was large in order to provide the largest signal gain. Then the current as a function of time was recorded at a high sampling frequency (20 kHz). The collected current data was converted to the change in gate voltage detected by the graphene by dividing by the transconductance value.

Figure 5.7c shows the gate voltage measured by a GFET underneath a KTar-1 cell as a function of time. The action potentials created by the cell are the tall peaks visible in the data. This data demonstrates a high SNR of up to 30 of the graphene FET in realistic operating conditions (in cell medium, with cells plated on the chip). The RMS noise in the devices was 0.5 +/ 0.2 mV for the band 100 Hz - 10 kHz. The largest action potential measured reached a maximum of 15 mV, with most peaks above 2 mV. Recall the voltage measured by the graphene FET is equal to the junction voltage V_J established in section 5.2. In this data V_J was a relatively large portion of the membrane potential V_M = 70 mV. If we refer back to the voltage divider model relating the voltage measured by the graphene V_J and the cleft height h_{cleft} (Figure 5.2b and 5.2c) V_J = 10 mV corresponds to a cleft height < 5 nm. The action potential spikes are approximately 21 ms apart, which is characteristic of this cell line. The width of each spike is around 1 ms. These characteristics can help identify measurements as belonging to cells, rather than a source of external noise. Overall these measurements demonstrate the viability of our graphene FETs as sensors for neuronal cells, and show low noise. In the next section, we'll explore enhancing the signal further by attempting to decrease the distance between the graphene channel and the cell membrane further by placing free-floating graphene FETs on top of cells.

5.5 Released Graphene FETs

Decreasing the distance between the cell membrane and the sensor channel should increase the magnitude of the signal measured, as illustrated in Figure 5.2c. One way to accomplish this is to use a flexible sensor that, when placed on top of a cell, conforms to its shape as illustrated in Figure 5.8a. Some work has been done with graphene on flexible polymer substrates to allow the devices to conform to soft tissue[14,31,62]. Graphene on plastic works well for conforming to large soft tissue like the surface of a brain; however even a very thin plastic substrate has a bending stiffness orders of magnitude larger than that of graphene by itself (10^{-9} Nm for a 4 um thick parylene-c substrate, and 10^{-16} Nm for graphene[33]). The plastic limits the bending stiffness such that it cannot conform to an object the size of a single cell (around

10 um in diameter). By using a graphene device not on a substrate, the full flexibility of the graphene could be utilized, and would allow for closer contact between the graphene channel and the cell, resulting in a smaller junction height and a larger detected signal. Using a free-floating, movable graphene device would also provide the option to select individual cells specifically for study. An illustration of this is shown in Figure 5.8b, and an optical image of a graphene FET put over a selected cell is shown in Figure 5.8c. The patch clamp method also allows the user to select the cell to measure but has the downside of rupturing the cell membrane during the measurement, which precludes measuring the same cell multiple times. In the next section I will discuss the procedures I helped develop for make free-floating graphene FETs.

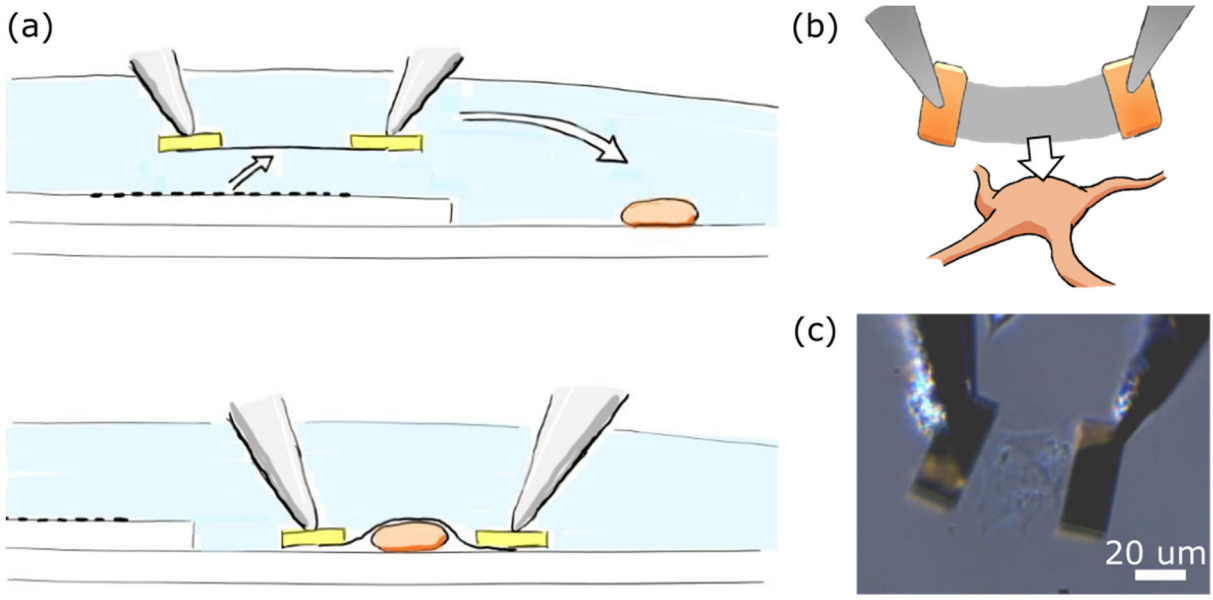

Figure 5.8: Released graphene FETs. (a) and (b) Illustrations of the process of lifting a graphene FET off the surface and placing it directly over (drawings by Ethan Minot). (c) Optical image showing a released graphene FET on top of a living KTaR-1 cell.

5.5.1 Method Development

To release graphene devices from the silicon oxide surface, I used a combination of hydrofluoric acid (HF) etching, surfactants, and micromanipulator probes. This is a delicate procedure that required significant trial and error to fine tune. To create free floating graphene FETs, the same fabrication steps were followed as described in section 5.3.1. Figure 5.4 is an optical image of the types of devices made for these experiments. After the graphene and electrodes were fabricated on a glass coverslip, the coverslip was placed into 1% aqueous hydrofluoric acid (HF) bath for approximately 30 seconds. After 30

seconds the HF was diluted with water gradually to reduce the acidity. After several dilutions, the coverslip was carefully transferred to a petri dish containing 1 mM NaDBS (a surfactant). Most devices were no longer attached to the substrate and were instead resting loosely on the substrate, so care had to be taken when transferring the chip through the meniscus of any liquids to prevent the devices from being washed away into solution.

For testing, the coverslip with the released graphene FETs was removed from the dish of surfactant and placed onto a large (55 mm x 24 mm) coverslip. The surfactant solution left on the device coverslip was wicked away with a KimWipe (Kimberly Clark) and DMEM was slowly pipetted onto the chip. This was done several times to significantly dilute the surfactant because high concentrations of surfactant results in the death of many cells. To get the graphene FETs near cells, cells were grown onto a coverslip that was broken into several smaller pieces. A piece of the coverslip with cells grown was placed directly on top of the graphene chip containing devices. While this method did cause some of the graphene FETs to be trapped underneath the cell chip and hence unusable, the cell chip piece was small enough that there was still an abundance of other graphene FETs available for testing left on the chip. The device chip and cell chip were covered in a single pool of warmed DMEM, to keep the cells alive and to provide the liquid for the graphene gate. An Ag/AgCl electrode was put into the DMEM pool to provide the global gate voltage for the graphene FETs.

The inverted microscope was used to look at the devices on the chip and identify a candidate for lifting. Devices that appeared to be sitting flat on the substrate (not partially floating or twisted) that were isolated (not touching other graphene FETs) were chosen. The high impedance probes on the piezoelectric controllers were then used to make contact to the chosen device by lowering them until they touched the source and drain electrodes. A transfer curve for the device was taken while it was sitting on the substrate; the gate voltage V_g was scanned in 2 mV steps from -500 mV to +700 mV at a rate of 200 mV/s. Then the probes were slowly lifted away from the surface, bringing the graphene FET device along. The probes stay connected to the electrodes by the Van der Waals force. Finally a candidate cell was chosen for measurement, and the graphene FET was slowly lowered down over the cell as shown in Figure 5.8a and b. When over a cell, the current as a function of time was monitored with a sampling rate of 20 kHz. The sampling rate is high enough to resolve the 1 ms wide peaks seen in the cell-over-graphene measurements in section 5.2.

5.5.2 Electrical Measurements

When working with a released device, first a transfer characteristics curve was taken when the device was sitting on the substrate. Then the probes on micromanipulators were used to lift the device off

the substrate and another transfer characteristics curve was taken. Comparison of the curves before and after the lift can help determine whether the graphene was damaged during the lifting process. Figure 5.9a shows a device that had electrical characteristics remain intact during the lift. Conversely, the device in Figure 5.9b was damaged during the lift as seen by the dramatic decrease in channel current; most likely the graphene was torn, decreasing the channel width which increased the channel resistance. There was a small but noticeable shift in the Dirac point of the curve towards Vg = 0 upon lifting. This is likely due to charged impurities in the substrate which create local gating effects; when the substrate is far away, the effect of the charged impurities is diminished. Furthermore, the slope dI/dV_g is almost the same between the lifted and on-substrate states. This implies that the coupling of the graphene to the fluid is retained upon lifting.

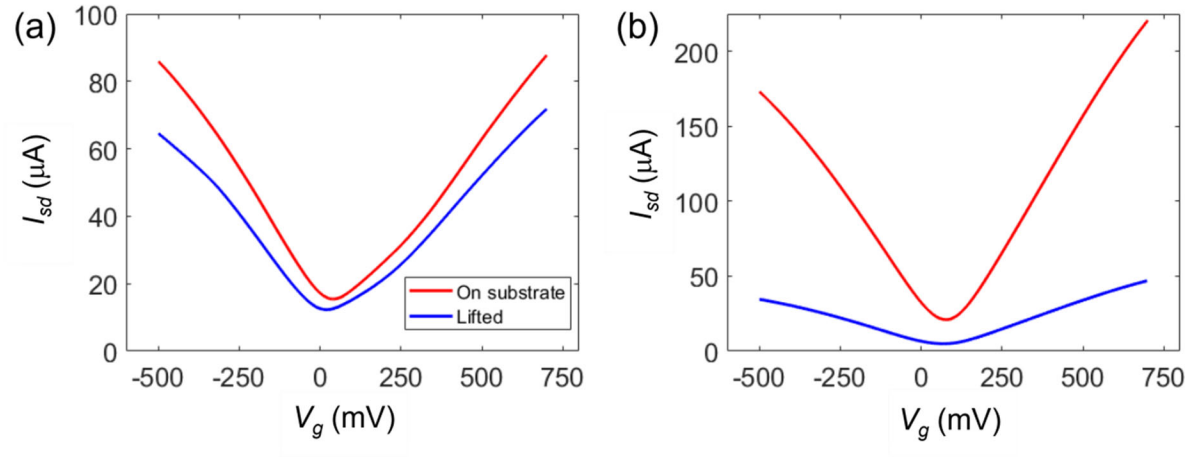

Figure 5.9: Transfer Characteristics Curves for Lifted and On Substrate Graphene FETs. (a) The current through the graphene channel as a function of gate voltage applied for a device before (red) and after (blue) the device was picked up from the surface. The electrical characteristics largely stayed the same after lifting. A small change in the location of the Dirac point is observed. (b) The current as a function of gate voltage for a device before (red) and after (blue) lifting, where the device was damaged after lifting.

I had 17 successful trials of putting graphene FETs over cells. However, no cell signals in the channel current were detected. We tentatively conclude that the noise level in the devices was greater than the signal level. The RMS noise level in the released graphene devices was 0.4 +/- 0.2 mV for the frequency band 100 Hz - 10 kHz, meaning the change in gate voltage for the channel created by the action potentials would have to be less than about 0.5 mV to go undetected. Using the voltage divider model established in Figure 5.2b to analyze the released graphene FET, it may be necessary to account for the fact that when the graphene FET is lifted from the surface, there are two sides that are being gated; the

bottom surface of the graphene channel is at the junction voltage V_J between the channel and the cell membrane, while the top surface of the graphene channel is at the voltage of the electrolyte bath V_{bath}. In this case the total voltage gating the graphene is not just the junction voltage V_J, but instead is the average $(V_J + V_{bath})/2$. For a fixed V_{bath}, changes in the junction voltage V_J would be diminished by a factor of 2. Therefore, a signal of 1 mV in the junction voltage V_J would be undetected for GFETs with noise about 0.4 mV. This would correspond to a cleft height of about 30 nm according to Figure 5.2c.

There are other possibilities for why no signals were detected. The membrane area in contact with the graphene channel may have been smaller compared to the work with cells grown on graphene FETs, resulting in a smaller number of ion channels ejecting ions into the junction and a smaller V_J created by the cell during firing. Similarly if the ion channel distribution is not uniform across the cell membrane, there may have been fewer ion channels in the area where the released graphene device makes contact (the top of the cell) compared to an on-substrate device (which contacts the bottom of the cell). The ion channels are membrane proteins free to move laterally within the lipid membrane. It is possible the ion channels move away from the area of the membrane contacted with the graphene channel when the device is lowered (due to the pressure from the device, or an electrostatic interaction). This could be tested by fluorescently labeling the ion channels, lowering the graphene FET onto the cell, and observing the channel position. It is also possible that during each measurement attempt the cells were not generating action potentials.

To further investigate the distance between the cell membrane and the graphene channel, and to determine if it is contributing to a low junction potential, an additional experiment was devised.

5.5.3 Cell Fluorescence to Examine Graphene-Cell Proximity

Another experiment was attempted to estimate the distance between the cell membrane and the graphene channel. This experiment relies on an interesting property of graphene. When a graphene lattice is in close proximity to a fluorescing molecule, when the molecule is excited, it may give the energy to the graphene lattice via a non-radiative energy transfer which allows the molecule to relax while preventing a fluorescent photon from being produced[67]. This phenomenon is called fluorescence quenching. The energy from the fluorescent molecule creates an electron-hole pair in the graphene lattice; this may be more likely to occur than in other materials due to the zero band gap of graphene near the Dirac point. A study found a reduction in photon emission greater than 85% occurs in rhodamine molecules less than 10 nm from the graphene flake[67].

Theoretically the fluorescence quenching property of graphene could be used to determine the distance of graphene from a cell membrane by using a membrane dye. Membrane dyes attach fluorescing molecules to a cell membrane for the purpose of imaging the cell. Placing graphene close enough to a cell membrane dyed with fluorescing molecules could reduce the lifetime of the photons to a noticeable point, which could be observed as a change in the photon flux coming from the cell, as illustrated in Figure 5.12. This would confirm that the graphene is in close contact to the cell. The goal of our next experiment was to use a membrane dye on the KTaR-1 cells and place a graphene FET over the top, comparing the brightness before and after to look for a dark spot that could be used to verify that the graphene was getting in close contact to the cell.

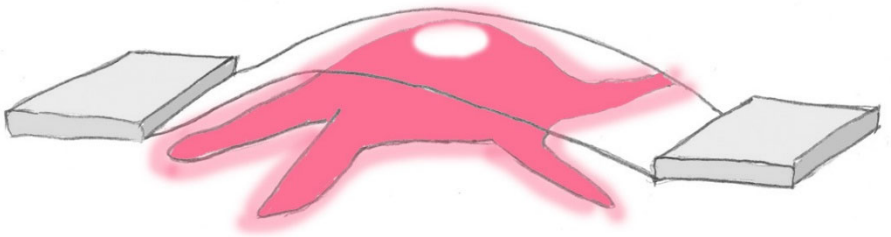

Figure 5.10: Graphene quenching the fluorescence of a cell membrane. An illustration of a cell fluorescing due to a fluorescent membrane dye is shown. The white spot on the top of the cell is where the graphene channel is in close contact with the fluorescing membrane and the fluorescence is quenched, resulting in an area that releases fewer photons than the nearby membrane that is not in close contact with the graphene channel.

To explore this, KTaR-1 were dyed using a fluorescent membrane dye (Cell Navigator Plasma Membrane Staining Kit, Orange). The fluorochrome in this dye is tetramethylrhodamine (TRITC) which was chosen because the excitation and emission spectra of TRITC (peaks at 557 nm and 576 nm, respectively) are well aligned with the filter cube available in the fluorescent microscope (excitation peak at 540 nm, emission peak at 590 nm). To dye the cells, a 2x solution was mixed according to the manufacturer's instructions. Then the growth medium was removed and 2.5 mL of dye solution was added to a petri dish containing KTaR-1 cells grown on a coverslip at about 70% confluency. The cells were put back into the incubator for 10 minutes. Then the dye was pipetted out of the dish and the cells were rinsed three times with phosphate buffered saline. Several mL of warmed cell medium was added back to the dish. At this point the cell membranes are dyed and ready for testing.

To take images of released graphene devices over fluorescing cell, the micromanipulators and probes were moved to sit above the fluorescent micrscope stage. A chip of released graphene devices was put on the stage in cell medium, and a piece of coverslip containing the dyed cells was put on top of the device chip, leaving some devices exposed. The probes were then used to pick up a released graphene

device and carry it over to the location of the cells. A cell was chosen that fluoresced brightly and an image was collected (500 ms exposure time, 1x1 binning), as shown in 5.12a. Then the graphene device was lowered down over the cell until the probe tips slid on the coverslip surface, and another fluorescence image was collected, as in Figure 5.12b. The intensity as a function of position was compared between the two images to see if any changes in photon emission were observed. A plot of the intensity along the yellow lines in Figures 5.12a and 5.12b are shown in Figure 5.12c.

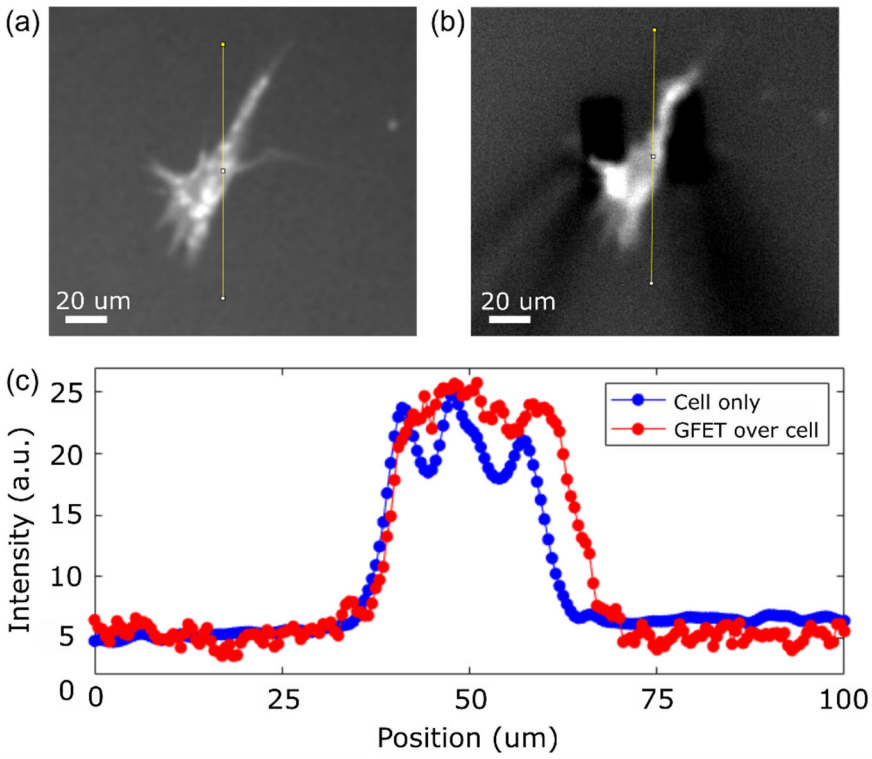

Figure 5.12: Fluorescence imaging of membrane-dyed cells and released graphene FETs. (a) A fluorescence image of a membrane-dyed cell. (b) A fluorescence image of the same dyed cell with a graphene FET lowered down on top of it. (c) Plots of the intensity as a function of position along the yellow lines in each fluorescence image. Note the slight broadening in the peak when the graphene device is on the cell; this is likely caused by pressure from the graphene on the cell.

The integral of the curve should be proportional to the number of photons collected. The integral of the data with the graphene over the cell is 16% larger than the data of just the cell. If fluorescence quenching was occurring, the data with the graphene over the cell should show fewer photons than the data of the cell alone. The change in the curve shape from the plain cell to the cell with the graphene on top may be due to pressure from the graphene pushing the cell down, changing the focal plane slightly. The lack of fluorescence quenching could mean the distance between the graphene and the cell was greater than 10 nm, which is consistent with the failure to see cell action potentials electrically.

5.6 Conclusion

I showed that our graphene FETs could readily measure action potentials from neuronal cells when on the substrate with a SNR of up to 30. This is competitive with previous work done with graphene FETs. Then I took free floating graphene sensors and successfully placed the graphene channel over the top of cells. Despite multiple trials (N=17) no electrical signals from the cells were detected. We postulate that the graphene placed on top of the cell did not form a tight seal. From our course-grained model of the cell-graphene interface, we estimate the distance between the graphene channel and the cell membrane exceeded 30 nm. To confirm the large separation between the graphene and cell, we labeled the cell membrane with fluorescent dye and showed that fluorescence was not quenched by placing graphene on the cell.

CHAPTER 6: CONCLUSION

The landscape of neurosensing tool development has been expanded in the last two decades with the addition of nanomaterials. A major goal of this new generation of sensors is to overcome the limitations of traditional silicon-based neurosensors to allow for high number, high density, long-term measurements of individual neurons with minimal damage to the tissue. Graphene is playing a role in the development of these new technologies. This thesis describes several geometries of graphene FET-based neurosensors that show promise for high signal-count and/or mechanical compatibility with soft tissue and cells.

When devices are scaled to small dimensions, noise becomes increasingly significant. For neurosensing applications, it is critical to keep noise levels lower than the signal size. There is already a significant body of literature describing noise in graphene FETs. In Chapter 3, I reviewed this literature and applied the existing models to describe measurements of our graphene FETs. The noise in our graphene FETs follows the expected $1/f$ dependance across the frequency range relevant to biosensing (1 Hz - 10 kHz). Current fluctuations are a function of gate voltage and we confirmed that this gate voltage dependence is consistent with the augmented charge noise model. The charge noise model suggests noise in the graphene FET current is due to charge fluctuations in the electrolyte and/or the substrate coupling to the graphene channel via the field effect, and scattering in the graphene channel. Missing from the augmented charge noise (ACN) model is noise due to the contact resistance between the graphene and the metal. We modeled the graphene channel and the metal-graphene contact as resistors in series found that the current noise power from contact resistance has the same dependence on current ($\sim I^2$) as the channel scattering term in the ACN. Our early results suggest that reducing the contact resistance may decrease the current noise. At the optimal gate voltage where the effective gate noise is minimized, our best devices had effective gate noise ~170 μV_{RMS} for the bandwidth 1 Hz – 10 kHz, which is about a factor of 2 larger that state-of-the-art graphene FETs when bandwidth and device size are considered.

In Chapter 4, we explored multiplexing with graphene FETs. I designed a twin-liquid-gate wafer that enables application of unique signals to two graphene devices with a shared drain. This wafer was used to perform multiplexing with a 1x2 array of graphene FETs, and a SNR of up to 15 was achieved from multiplexed signals when biologically relevant gate signals with a 2 mV amplitude were used. No degradation of the SNR was observed in signals reconstructed from multiplexed data compared to equivalent DC measurements. Taking into account frequency limitations of the graphene-electrolyte system and the fabrication challenges needed to achieve crisscrossing wires, our work suggests that multiplexed graphene FETs can be extended to an array of around 2000 sensors which can be

simultaneously monitored using only 90 wires. The array in combination with the integrated circuit chip in development offers a route to measure individual action potentials from large numbers of neurons with a workable number of wires.

In Chapter 5, we showed that our graphene FETs can measure action potentials from individual neuronal cells *in-vitro* when neurons are cultured onto the graphene FET devices. The strong signal magnitude was consistent with the formation of a tight cleft between the graphene and the sensor. We observed signal-to-noise ratios as large as 30. We also developed a releasing individual graphene FETs from the surface, and placing these sensors on top of cells. The method uses micromanipulation needles to place the electrically-contacted graphene FET on top of a chosen cell. Measurements from 17 different cells failed to show any electrical activity when the graphene sensor was on the cell. We speculate that the graphene did not form a tight cleft with the cell. Alternatively, the manipulation of the graphene onto the cell may have damaged the cell, or the ion channels may have migrated away from the region in contact with the channel as the device was lowered.

6.1 Outlook

Graphene FET neurosensors can be used for *in-vitro* or *in-vivo* studies. State-of-the-art graphene FETs can reach similar noise levels as traditional sensors on silicon (~10 μV_{RMS}), with the added benefits of biocompatibility, flexibility, and switchless multiplexing. Our work shows that large arrays of graphene FETs utilizing multiplexing and integrated with ICs could simultaneously monitor over 2000 neurons with individual action potential resolution.

Multiplexing local field potential signals (less than 200 Hz) with an array of graphene FETs was published by Garcia-Cortadella et al in 2020[23]. Our work with the dual-liquid-gate wafer showed multiplexing of signals at even higher frequency, with simulated action potential signals up to 1 kHz. Further work can be done with this project, including building a larger array, testing at higher carrier frequencies to confirm the predicted threshold frequency, and further developing the IC chip to provide the carrier voltages and collect the multiplexed output without adding significant noise.

For *in-vivo* studies, a mechanically soft device causes less damage on insertion and is better for long-term use than a hard shank. Graphene FETs are flexible and can be fabricated onto polymer substrates for surface measurements. Organic semiconductors are also biocompatible, flexible, and used for neurosensing. An advantage of graphene relative to organic semiconductors is the measurement bandwidth. In graphene FETs, signals at 1 kHz and above can be measured with a good signal-to-noise

ratio (as demonstrated in Chapters 4 and 5), where organic semiconductors are better suited for measuring low frequency brain oscillations < 200 Hz due to their limited mobility.

For *in-vitro* studies of action potentials, cultured neuronal cell lines, primary neurons, or brain slices are plated onto a planar electrode. An example of a high count state-of-the-art array utilizes time-division multiplexing (TDM) and is able to record from tens of thousands of sensors at a noise level of about ~10 μV (SNR of 55)[68]. The outputs from 4056 sensors share a single wire, which surpasses our estimate for the number of graphene FET channels that could share a single wire (45) using frequency-division multiplexing. Since the limitations of silicon-based electronics (rigidity and degradation over time in biological fluids) are compatible with most *in-vitro* experiments, which tend to be short-term and plated onto a flat substrate, we conclude that graphene FET arrays are not competitive with CMOS technologies for high signal count *in-vitro* measurements.

For targeted measurements of individual neurons *in-vitro*, we placed released graphene FETs on top of cells as a less-invasive alternative to whole cell patch clamp. Further work can be done to look into why the action potentials were not detected by the graphene FET as discussed at the end of Chapter 5. For example, observing the changes in positions of ion channels when a graphene device is lowered onto the cell using fluorescence labeling, or using fabrication techniques to form a tighter seal between the graphene and the cell.

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APPENDICES

Appendix A: MATLAB Code for Simulating 1/*f* Noise

```
%%creates random flicker (1/f) noise
%inputs:    fsampling -> sampling rate in Hz
%           timeTotal-> total time of trace in seconds
%           S1Hz -> desired noise power at 1 Hz
%outputs:   time -> vector of time (in seconds), with total time
timeTotal
%           flickerNoise -> random noise at rate fsampling with 1/f
spectrum

function [time, flickerNoise] = createFlickerNoise(fsampling,
timeTotal)

S1Hz = 1e-18; %defines Si at 1 Hz
f=0:1/fsampling:timeTotal-1/fsampling; %normalized frequency vector
(normalized to fsampling, as f = 0, 1/fsampling, 2/fsampling, ....,1)
S=1./sqrt(f); %S unitless (though would be in Hz^-1/2 if f wasn't
normalized)
%note S = fs * Si
S(end/2+2:end)=fliplr(S(2:end/2)); %flips for f > fs/2

S = S.*exp(1i*2*pi*rand(size(f))); %adds random phase to each term
S(1)=0; %changes S(1) from Inf to zero
%plot(S)

flickerNoise = real(ifft(S));
[p1,f1] = pwelch(flickerNoise,[],[],[],fsampling);
loglog(f1,p1)
factor = sqrt(S1Hz/p1(2));
flickerNoise = factor*flickerNoise;
time = 0:1/fsampling:timeTotal-1/fsampling;

end
```

Appendix B: MATLAB Code for Demodulating AM Signal

```
%define carrier frequencies
fcarrier1 = 27000; %in Hz
fcarrier2 = 38000; %in Hz
%define transconductance of each channel
g1 = 10.4e-6; %in A/V
g2 = 7.2e-6; %in A/V

timeWindow = [200 300]; %time window on plots, in ms

%open file
dataFileID = fopen('C:\Users\carly\Documents\Minot
Research\ProbeStation\GFET_Test_1127\real13_edit','r');

%%%%%%%read in multiplexed current file%%%%%%%
%define size of array to read data into
sizeA = [3 Inf];
%read txt file into array A
A = fscanf(dataFileID, '%f', sizeA);
fclose(dataFileID);

%create individual vectors for each column of data from array A
timeVec = A(:,1); %time in s
timeVec = timeVec'; %convert to column vector
fSamp = 1/timeVec(1); %sampling frequency in Hz

Iraw = A(:,2); %current in A
Iraw = Iraw'; %convert to column vector

%plot multiplexed I(uA) vs t(ms)
figure(1)
plot(timeVec*1e3, Iraw*1e6)
xlabel('Time (ms)')
ylabel('I_s_d (uA)')
xlim(timeWindow)

%calculate PSD of multiplexed I vs t data
windowsize = 16384;
[psd,fpsd] = pwelch(Iraw,windowsize*8,[],[],fSamp);


%plot PSD of multiplexed I vs t data
figure(2)
loglog(fpsd,psd)
xlabel('Frequency (Hz)')
ylabel('S_I (A^2/Hz)')
xlim([1 fSamp/2])
set(gca,'FontSize',18)
```

```
%% Digital Signal Processing (BP filter, demodulate via squaring, LP
filter)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%band-pass filter - filter around carrier frequency
%define fdelta such that pass band is fcarrier +/- fdelta
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
fdelta = 500; %in Hz
%limits for CH1 BPF (around frequency fcarrier1)
flow1 = fcarrier1-fdelta;
flow2 = fcarrier2-fdelta;
%limits for CH1 BPF (around frequency fcarrier1)
fhigh1 = fcarrier1+fdelta;
fhigh2 = fcarrier2+fdelta;
%filter order (for both BPFs)
filterOrder=256;

%create impulse for each filter, convolve with Iraw
bpImpulse1 = fir1(filterOrder, [2*flow1/fSamp 2*fhigh1/fSamp]);
filtered1 = conv(bpImpulse1, Iraw);
filtered1 = filtered1(1:end-filterOrder);

bpImpulse2 = fir1(filterOrder, [2*flow2/fSamp 2*fhigh2/fSamp]);
filtered2 = conv(bpImpulse2, Iraw);
filtered2 = filtered2(1:end-filterOrder);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%squaring, multiply by 2
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%demod = [filtered(:,1).*filtered(:,1) filtered(:,2).*filtered(:,2)];
demod1 = 2*filtered1.*filtered1;
demod2 = 2*filtered2.*filtered2;

figure(4)
plot(timeVec*1e3, demod1)
xlim(timeWindow)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%low-pass filter FIR
%second element is between 0 and 1, with 1 = nyquist frequency
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
flow = 500; %low of bpf, in Hz
%fhigh = 100; %high of bpf, in Hz
filterOrder=256;
%lowpassImpulse = fir1(filterOrder, [2*flow/fSamp 2*fhigh/fSamp]);
lowpassImpulse = fir1(filterOrder, 2*flow/fSamp, 'low');
%channel 1 filtering
filteredDemod1 = conv(lowpassImpulse, demod1);
filteredDemod1 = abs(filteredDemod1(filterOrder:end-1));
%channel 2 filtering
```

```
filteredDemod2 = conv(lowpassImpulse, demod2);
filteredDemod2 = abs(filteredDemod2(filterOrder:end-1));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
figure(5)
plot(timeVec*1e3, filteredDemod1)
xlim(timeWindow)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%rescale back down
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
filteredDemod1 = filteredDemod1.^0.5;
filteredDemod2 = filteredDemod2.^0.5;

%combine filtered data back into a single array
filteredDemod = [filteredDemod1, filteredDemod2];

%plot filtered, demod'd data
figure(6)
plot(timeVec'*1000, filteredDemod*1e6, 'LineWidth',2)
xlabel('Time (ms)')
ylabel('I_s_d (uA)')
xlim(timeWindow)
legend('CH1','CH2')

%taking PSD of demod'd filtered data
[psdPost,fPost] = pwelch(filteredDemod, windowsize*8,[],[],fSamp);
%[psdDemod,fDemod] = pwelch(demod, windowsize,[],[],fSamp);

%plot PSD of filtered, demodulated I channels with raw data PSD
figure(7)
loglog(fPost, psdPost, fpsd, psd)
xlabel('Frequency (Hz)')
ylabel('S_I (A^2/Hz)')
xlim([1 fSamp/2])
legend('CH1','CH2', 'I_r_a_w')

%calculate Vg from I, plot Vg vs time
vFilteredDemod = [filteredDemod(:, 1)/g1 filteredDemod(:,2)/g2];
figure(8)
plot(timeVec'*1000, vFilteredDemod*1e3, 'LineWidth',2)
xlabel('Time (ms)')
ylabel('V_g (mV)')
xlim(timeWindow)
legend('CH1','CH2')
```