# AN ABSTRACT OF THE DISSERTATION OF

Manjunath Kareppagoudr for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on June 14, 2021

Title: Switched Capacitor Circuit Techniques for High Performance CMOS Analog Circuits

Abstract approved:

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Gabor C Temes

Switched capacitor (SC) circuits are the main building blocks in many structures such as filters, data converters, sampling circuits and sampled-data amplifiers. The key challenge is to design such circuits which are the prime components of any IoT system with low power consumption without compromising on the performance. In this dissertation, power efficient novel switched capacitor techniques have been explored to suppress noise and mitigate the slewing in switched capacitor-based analog to digital converters (ADCs).

First, a two-step incremental ADC(IADC) with pseudo-pseudo differential (PPD) structure is presented. PPD integrators are implemented with added correlated level shifting (CLS) technique to relax the output swing and gain requirements of the operational transconductance amplifier (OTA). The two-step IADC is implemented with the first step configured as a single-bit first-order IADC and the second step, using a two-capacitor SAR-assisted extended counting to further enhances the accuracy. The design is demonstrated by implementing the prototype in 65nm CMOS technology.

Second, new passive charge compensation techniques are described. The proposed techniques mitigate the slewing in the OTA by providing a controlled amount of charge to the output of the OTA. The effectiveness of the proposed charge compensation technique in a switched-capacitor integrator is demonstrated in a second-order DSM.

Circuit-level simulations including the effects of process, voltage and temperature variations are also presented. The extracted simulation results show a 12 dB improvement in SNDR using the proposed technique compared to conventional DSM without charge compensation.

# Switched Capacitor Circuit Techniques for High Performance CMOS Analog Circuits

by
Manjunath Kareppagoudr

A DISSERTATION

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APPROVED:

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Manjunath Kareppagoudr, Author

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# LIST OF APPENDED PUBLICATIONS

The material presented in chapter 2 to 4 have been published in several IEEE journals and Conferences. Here are the details of publications.

1. Some part of the text in chapter 2 and chapter 3 are published in “Noise filtering and linearization of single-ended sampled-data circuits,” IEEE Transactions on Circuits and Systems-I, vol. 66, April 2019 and "System-level noise filtering and linearization," 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018.
2. Text in chapter 2 and chapter 4 is a reprint of two papers, first is "Slewing Mitigation Techniques for Switched- Capacitor Circuits", IEEE Trans. on Circuits and Systems-I, vol. 67, no. 10, pp. 3251-3261, Oct. 2020. Second paper will be published in a conference in August 2021, named, “Switched-Capacitor Integrator with Slew-Rate Enhancement and Low Distortion,” IEEE International Midwest Symposium on Circuits and Systems, August 7-9, 2021.

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*Dedicated to My Parents*

# CHAPTER 1. Introduction

## 1.1 Motivation

Data converters, filters and sampled data amplifiers are the key building blocks of many communications and Internet of thing (IoT) systems. Most of the IoT systems are battery operated, and the number of devices connected to such a system is increasing every year, which makes power consumption a major concern. The interface usually requires high accuracy, low power analog to digital converters with a few kHz of bandwidth. Continuous-time delta-sigma modulators (CTDSMs) have gained attention in recent literature [1]-[2] because of advantages over discrete time delta-sigma ADCs, such as implicit anti-aliasing filtering and power efficiency. Discrete-time modulators (DTDSMs) consume much more power, since the operational amplifiers used in the integrators must have higher bandwidth and gain requirements. However, CTDSMs are more sensitive to component mismatch, clock jitter, excess loop delay, and PVT variations than discrete-time ones.

Switched capacitor-based designs are more tolerant to process variations as critical specifications of such circuits depend on capacitance ratios, which are better controlled than transconductances and resistors. In fact, since most of the critical specifications such as gain, Q-factor and corner frequency can be made to depend only on capacitance ratios, even better process tolerance can be achieved. Also, due to the fact that in SC circuits only the final settled voltage in each clock phase is important and not how the circuit arrives at such voltage, many circuit techniques can be used to improve circuit imperfections. In operational amplifier (opamp) based switched-capacitor circuits, the imperfections of the opamp are the major sources of performance limitation. These imperfections include noise, input-referred offset, finite gain, finite bandwidth, and linearity. Due to shrinking supply voltages, it has become more important to reduce the noise to maintain high SNR. In this dissertation, novel switched capacitor techniques have been explored to supress noise and mitigate the slewing in switched capacitor based analog to digital converters (ADCs).

## 1.2 Organization of this dissertation

In this dissertation, Chapter 2 describes non-idealities in switched capacitor circuits and review some existing techniques to mitigate such non-idealities. Chapter 3 presents an implementation of pseudo-pseudo differential (PPD) two-step Incremental ADC in detail. In Chapter 4, charge compensation techniques are described and are demonstrated using a single-bit second order delta-sigma ADC. Chapters 5 concludes this dissertation.

# CHAPTER 2. Non-Idealities in Switched Capacitor Circuits

This chapter discusses the non-idealities associated with switched capacitor circuits and some popular circuit techniques to suppress the effect of switched capacitor circuit non-idealities. Non-idealities associated with switched capacitor circuits can be broadly classified into two categories, first, the noise generated in the circuits which include thermal noise, opamp's flicker (1/f) noise and DC offset. Second, non-idealities associated with the finite gain, finite slew-rate, and finite bandwidth of an opamp.

## 2.1 Noise

The major sources of electronic noise include thermal noise, 1/f noise and shot noise. The thermal noise is inherent in all electronic circuits due to the kinetic energy and interaction of electrons with the lattice of the medium it is flowing through. Random scattering and coulomb interaction with host atoms causes electrons to generate thermal noise. Similarly, due to random trapping and releasing of electrons from interface imperfections, 1/f noise is generated. The spectrum of noise in CMOS circuits is shown in Fig.2.1. The thermal noise is uniformly distributed in the frequency spectrum up to very high frequencies. The power of 1/f noise has, as the name suggests, impacts circuits mostly at low frequencies. Besides noise, the input referred opamp offset is another imperfection, which causes error in the output. In some circuits like integrators, depending on circuit topology, the offset will behave as an input, and when integrated over long time can saturate the integrator even without actual input signal.

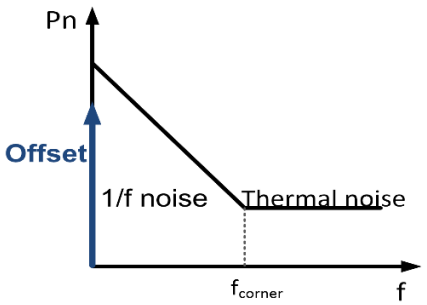



Fig.2.1 Noise spectrum

In order to overcome these inherent noise limitations of operational amplifiers, many techniques have been proposed. The most popular and widely accepted techniques are auto-zeroing (AZ), correlated double sampling (CDS) and chopping.

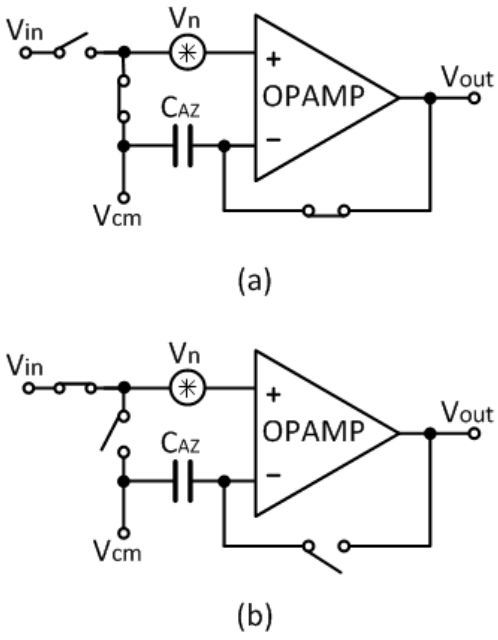





Fig. 2.2. Open-loop amplifier using auto-zeroing technique. (a) Offset sampling phase. (b) Amplification phase [3].

### 2.1.1. Auto-Zeroing (AZ) technique

Auto-zeroing is one of the widely used technique in switched capacitor circuits to filter out the DC offset and low frequency noise. The basic working principle of auto-zeroing technique [4] is depicted in Fig. 2.2. This technique needs two clock phases, In the offset sampling phase (Fig. 2.2a), the opamp is configured as a unity-gain amplifier. The noise voltage, $V_n$, is sampled and held in a capacitor $C_{AZ}$. In the amplification phase (Fig. 2.2b), the capacitor is connected to the inverting input of the opamp. As a result, performs high pass filtering operation eliminating DC offset and low frequency noise. Such technique is suitable for high-precision applications, particularly in oversampling systems, where the signal bandwidth is much smaller than sampling frequency.

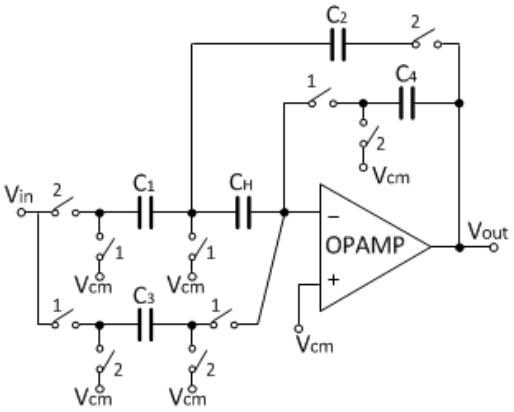





Fig. 2.3. Switched Capacitor integrator with correlated double sampling technique [3].

### 2.1.2. Correlated Double Sampling (CDS)

The basic principle of CDS [4] is shown in Fig.2.3. The CDS operation is performed in 2 phases. In phase 1, the low frequency input error of the opamp is sampled into the capacitor $C_H$. Assuming the ratio of $C_3$ and $C_4$ are equal to $C_1$ and $C_2$, and the input signal frequency is small compared to the switching frequency, the input-referred settling error will be same in both the phases. The input referred settling error is inversely proportional the gain A. Similarly, while considering offset and low frequency noise, the input-referred noise sampled on $C_H$ will be the same. Hence, in phase 2, when $C_H$ is in series with input capacitor $C_1$ , the equivalent input-referred settling error and low frequency noise sampled on the capacitor $C_H$ is subtracted from the inverting terminal of the opamp. Thus, the new virtual ground between $C_1$ and $C_H$ becomes closer to the ideal virtual ground. Since the gain error has be subtracted and input signal hasn't changed significantly, the new input referred settling error will be proportional to $1/A^2$. This has the same effect as having an opamp with $A^2$ gain. The input-referred noise has also been cancelled, as in AZ.

Even though CDS and autozeroing effectively attenuate the low-frequency imperfections in an opamp, they will cause increased noise at higher frequencies, due to folding of wide-band noise.

### 2.1.3 Chopping

The basic working principle of Chopping is shown in fig 2.4. Chopping is a modulation technique where input signal is modulated to chopping frequency($f_{chop}$) at the input, while the noise is in baseband. The input signal and noise are amplified by the opamp, and at the output the signal is demodulated from $f_{chop}$ to baseband while the baseband noise is modulated to $f_{chop}$. The low pass filter at the output eliminates the noise and restores the signal. Hence the DC offset and low frequency noise gets eliminated from the system.

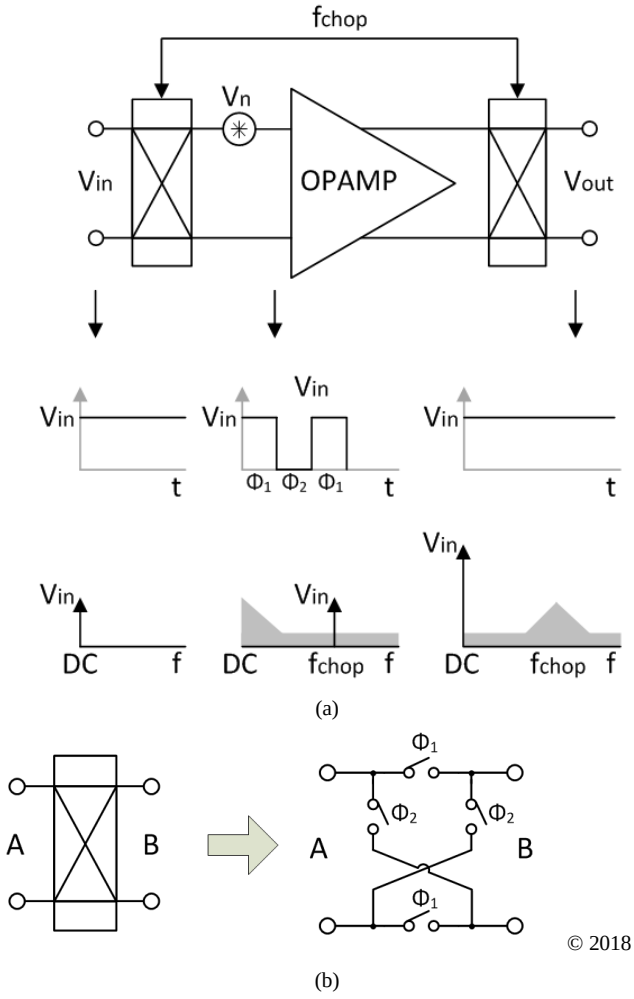





Fig. 2.4. Working principle of chopping technique. (a) time/frequency domain waveforms. (b) chopper implementation [3].

## 2.2. Harmonic Distortion due to Opamp in Switched Capacitor Integrator

Consider a conventional switched capacitor integrator [7] as shown in Fig 2.5, during phase $S_1$ the input is sampled into $C_1$, and during phase $S_2$ the charge in $C_1$ is transferred into $C_2$ by the OTA. The OTA output must settle to its final value within half clock cycle. This value depends upon the OTA gain, bandwidth, and slew-rate. The total settling time(charge transfer phase) can be divided into a non-linear slewing time and linear settling time. During slewing which is a large-signal phenomenon, large amount of current is drawn to charge the integration capacitor and load capacitor rapidly so as to track the input step. After slewing, during linear settling time, the charge transfer behaves linearly, and a small-signal model can be used in the analysis., For accurate settling, a sufficient linear settling time is required. So, slewing takes away some of the time left for linear settling, which often means the gain bandwidth (GBW) of the OTA needs to be increased to allow time for slewing. Hence, the power consumption of the OTA, as well as its linearity, is significantly impacted by slewing.

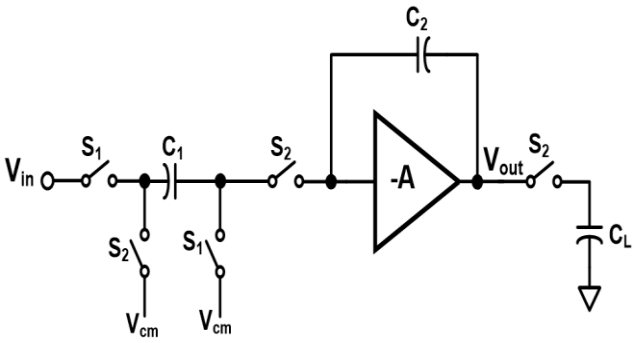



Fig. 2.5. Conventional integrator

In order to emphasize the importance of reducing slewing, its effect on settling error is calculated. The analysis assumes the non-inverting delaying SC integrator of Fig.2.5, with DC gain of 100 dB and an output current limited to $I_{BIAS}$. In a SC circuit with capacitive feedback, such as an integrator, there will be a feedthrough of the input voltage step through the feedback capacitor affecting the output voltage. The integrator needs to settle this feedthrough as well as provide charge to the total load capacitance at the output to bring it to the final voltage. Usually, the feedthrough's polarity is the same as the input step polarity, whereas the signal processed by the OTA has to

decrease for a positive input step, since the integrator is in a negative feedback configuration.

The slew rate for a single-stage OTA is given by

$$SR = \frac{I_{BIAS}}{C_{LTOT}} \tag{1}$$

Here, $C_{LTOT} = C_L + \beta \cdot C_1$ is the total load seen by the OTA. $C_1$ is the input capacitor, $C_L$ is the load connected to the output, $\beta \left(= \frac{C_2}{C_2 + C_1}\right)$ is the feedback factor, and $C_2$ is the integrating capacitor or feedback capacitor. Whether the OTA slews or not may be determined based on the voltage at the input of the OTA

($V_x$). Normally, when the $V_x$ is higher than the overdrive voltage by a factor $\sim\sqrt{2}$, the OTA is assumed to be slewing. So, the condition for slewing is

$$V_x > \sqrt{2} V_{OV} \tag{2}$$

Based on the input $V_i$, we can calculate the step at the input of the OTA, assuming the OTA does not instantly respond at time $t = 0$. From capacitive charge balance

$$V_x = V_i \frac{C_1}{C_1 + C_2 \,||C_L} \tag{3}$$

The total slewing time is the time required for the virtual ground voltage to return to a value less than $\sqrt{2} V_{OV}$. Since (1) gives the slew rate at the output, the slew rate at the input of the OTA is simply $\beta \cdot SR$. The time it takes to achieve this value is

$$t_{slew} = \frac{V_x - \sqrt{2} V_{OV}}{\beta \cdot SR} \tag{4}$$

Substituting (1) and (3) into (4), we get:

$$t_{slew} = \frac{V_i \frac{C_1}{C_1 + C_2 || C_L} - \sqrt{2} V_{OV}}{\beta \frac{I_{BIAS}}{C_L + \beta C_1}} \quad (5)$$

During this time, the OTA is providing constant current at the slew rate SR. So, if the final output voltage needs to change by $\Delta V_O$, at the end of slewing the remaining change left for linear settling is.

$$V_{lin} = \Delta V_o - t_{slew} \cdot SR \quad (6)$$

Here $\Delta V_o$ is the change in output voltage due to input $V_i$ given by

$$\Delta V_o = \frac{C_1}{C_2} V_i = \left(\frac{1}{\beta} - 1\right) V_i \quad (7)$$

Now the remaining error voltage ($V_{lin}$) must exponentially decay to the static error ($\epsilon_s$) during linear settling. The total error at the end of a charge transfer phase is then given by

$$\epsilon_t = V_{lin} e^{\frac{-t_{lin}}{\tau}} + \epsilon_s \quad (8)$$

Here, $t_{lin} = 0.5 t_{clk} - t_{slew}$ and $\epsilon_s$ is the static error. Then the total error is given by:

$$\epsilon_t = \left((1/\beta - 1) V_i - t_{slew} \cdot SR\right) e^{-t_{lin}/\tau} + \epsilon_s \quad (9)$$

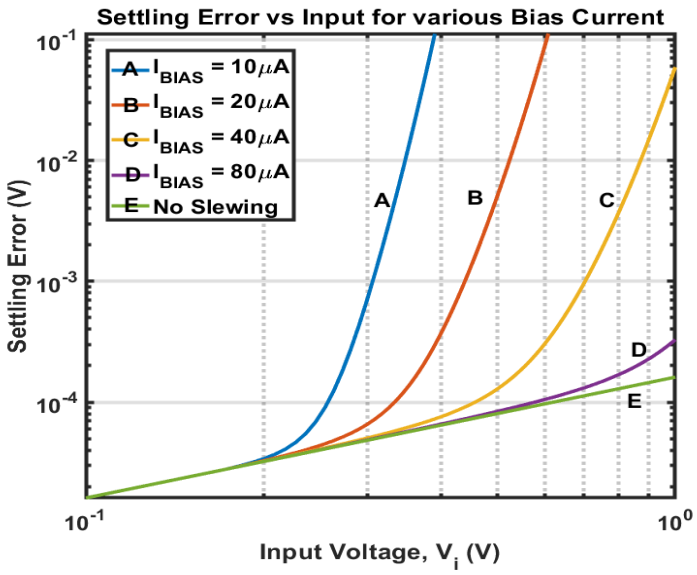



Fig. 2.6 Total error vs input voltage for various bias current © 2020 IEEE

In Fig.2.6 equation (9) has been plotted assuming $A_0$ = 70 dB, $f_{UGBW}$ = 40 MHz, $f_{clk}$ = 10 MHz, $C_L$ = 0.5 pF, $C_2$ = 4 pF, $C_1$ = 2 pF. From Fig. 2.6, it is clear that the settling error is a linear function of input if there is no slewing. However, when there is slewing, in addition to having a larger error, the error also depends non-linearly on the input voltage. Therefore, slewing mitigation is critical for improving linearity.

### 2.2.1 Correlated Level Shifting(CLS)

CLS technique can greatly relax linearity and gain requirements of the opamp. Furthermore, the CLS scheme significantly extends the allowable output swing of the opamp, allowing even larger than rail-to-rail output [8]. The basic operation of the CLS technique in a single-ended switched-capacitor amplifier is illustrated in Fig 2.7.

In the *sampling phase* (Fig. 2.7a), the input signal is sampled on $C_1$ and $C_2$, and $C_{cls}$ is reset. The *amplification phase* is divided into two sub-phases: estimating and level shifting phases. In the *estimating phase* (Fig. 2.7b), the circuit is a conventional amplifier with a nominal gain of $1+C_1/C_2$. Capacitor $C_{CLS}$ samples the output of the amplifier. This can have a significant error if a low-gain opamp is used. The input-referred settling error is proportional to 1/A. Next, in the *level shifting phase* (Fig. 2.7c), $C_{CLS}$ is connected in series with the opamp output. This will shift $V_{out}$ towards zero

voltage. Since the charge on negative terminal of opamp is fixed during the estimate phase, it also shifts the virtual ground voltage toward $V_{cm}$.. As a result, the equivalent gain A of the opamp is boosted almost to $A^2$ and the linear output swing is improved significantly. Hence, simpler and more power-efficient opamp topologies can be utilized. This allows a relaxation of the circuit noise requirements. Thus, smaller sampling capacitors can be used, which further improves the power efficiency. Also, unlike in CDS, as the CLS sampling operation happens at the output of the opamp, all sampling imperfections are attenuated by the gain of the opamp. But Unlike CDS scheme, CLS cannot cancel low-frequency imperfections in opamp.

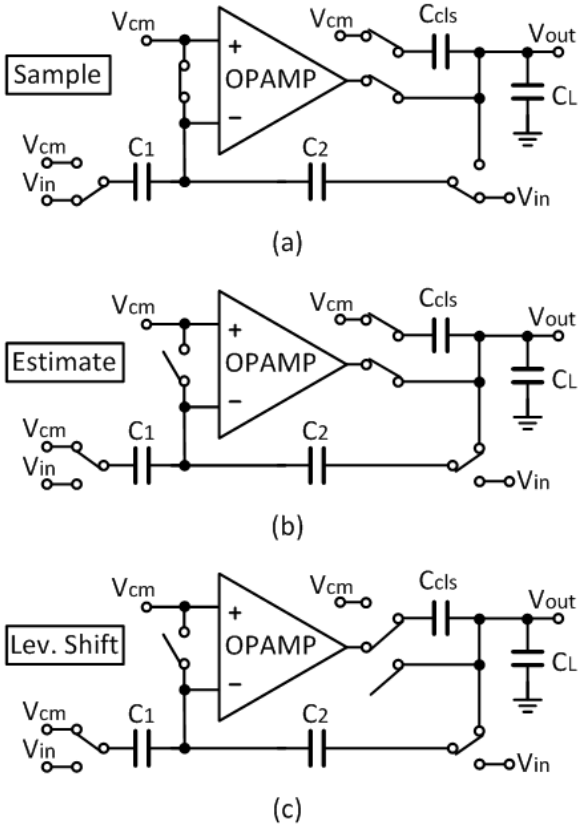





Fig. 2.7. Three-phase operation of correlated level shifting (CLS). (a) sampling phase. (b) estimate phase. (c) level shift phase [3].

# Chapter 3. Pseudo-pseudo-Differential (PPD) Structure for Switched Capacitor Circuits

This chapter introduces a pseudo-pseudo differential (PPD) structure which cancels low frequency noise, DC offset and suppresses even-order harmonics with a single ended implementation. The first section of the chapter discusses the working principle of the PPD structure and enhances its usefulness by combining it with the Correlated Level Shifting (CLS) technique. The second half of the chapter describes the implementation of two-step incremental ADC with the PPD structure. In the first step of IADC is configured as a first order ΔΣ loop and the residue is cancelled with a two-capacitor SAR in the second step. Fabricated in 65 nm CMOS process, the prototype ADC occupies an area of 0.2184 $mm^2$. The sampling frequency of 10.68 MHz and the signal bandwidth of 20 kHz achieves an SNDR of 48 dB from the first step, and it is boosted to 70.5 dB by the second step. Compared to a single ended structure, PPD achieves 8 dB better SNDR for the same power consumption of 230 µW.

## 3.1 Pseudo-Pseudo-Differential (PPD) integrator

The PPD integrator [9,10] is shown in Fig.3.1. The PPD integrator works with two non-overlapping phases. During phase $S_1$, it acts as a non-delayed inverting integrator, and the output of the amplifier is stored in the integration capacitor $C_{2a}$, as well as in the output capacitor, $C_{out}$. During phase $S_2$, the bottom plate of the input capacitor $C_1$ is switched from the input signal to the CM voltage. Thus, the input signal held on $C_1$ is inverted and integrated on the feedback capacitor $C_{2b}$. Meanwhile, the top plate of $C_{out}$ is connected to the output load, and the previous voltage held on $C_{out}$ is subtracted from the new output of the amplifier. Hence it realizes $1-z^{-1/2}$ operation and filters the low frequency noise and suppresses even order harmonic distortion. Fig.3.1(a) shows the implementation of subtraction in analog domain. The subtraction can also be performed in digital domain as shown in fig.3.1(b). The two feedback capacitors are nominally equal, and the input signal is integrated in both phases with the same polarity. Hence, the signal transfer function (STF) of the PPD integrator is given by

$$STF(z) = \frac{V_{out,2}}{V_{in,1}} = 2\frac{C_1}{C_2}\frac{z^{-1/2}}{1-z^{-1}} \qquad (3.1)$$

Here $V_{out,2}$ is $V_{out}$ at the end of phase $S_2$ and $V_{in,1}$ is $V_{in}$ at the end of phase $S_1$. The transfer function indicates that the signal output is doubled, as expected. The half cycle delay in the numerator indicates that the final output is available on phase $S_2$. The noise transfer function (NTF) of the circuit noise $V_n$, introduced at the input of the amplifier, is high pass filtered and is given by

$$NTF(z) = \frac{V_{out}}{V_{n,2}} = \left(1 - z^{-\frac{1}{2}}\right)\left(1 + \frac{C_1/C_2}{1+z^{-1/2}}\right) \qquad (3.2)$$

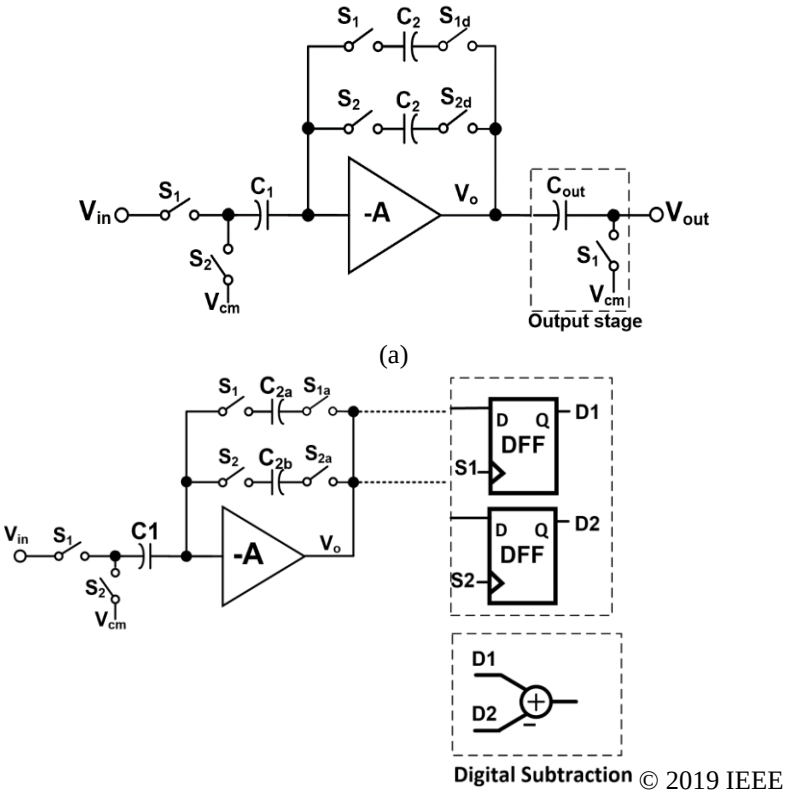





Fig.3.1 PPD implementation with (a) analog subtraction (b) digital subtraction

### 3.2 PPD Structure with CLS

As discussed in the previous section, the pseudo-pseudo differential (PPD) integrator is effective in filtering DC offset and low frequency noise but unlike CDS, doesn't offer gain squaring feature in the circuit. To further improve the linearity of the PPD integrator, correlated level shifting (CLS) technique can be utilized. Implementing a PPD structure with CLS helps to relax the gain and output swing requirement of the OTA. In conventional switched capacitor integrators, CLS is implemented in 3 phases,

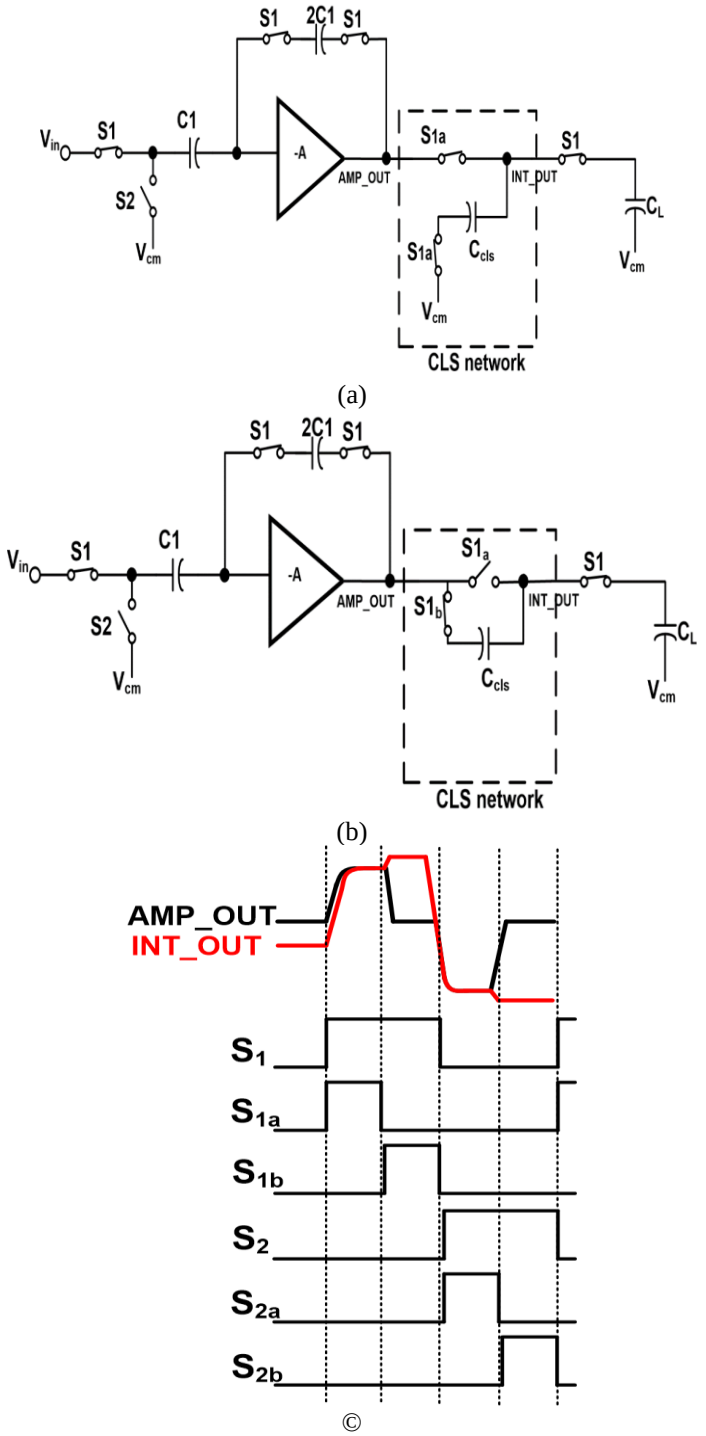



Fig.3.2 PPD Integrator in (a) Estimation phase($S_{1a}$,$S_{2a}$) (b) Level shifting phase ($S_{1b}$,$S_{2b}$) (c) Timing diagram

sampling phase, estimation phase and level shifting phase. In the PPD structure, the integration is performed in both phases, hence CLS operation needs to be performed in both the phases. Each phase ($S_1$ or $S_2$) is divided into two sub phases ($S_{1a}$, $S_{1b}$ or $S_{2a}$,

$S_{2b}$). During the integration phase $S_1$, in the first half of the phase $S_{1a}$, coarse integration of input is performed by the low gain OTA and while $C_{cls}$ capacitor is charged, in the second half of the phase $S_{1b}$, the bottom plate of $C_{cls}$ is connected to the output of the OTA, hence the integrator output is level shifted and settled to the accurate value. The same operation is performed in phase $S_2$ when integrator processes $-V_{in}$. Using CLS technique in PPD structure have another advantage, since as the PPD integrator processes Vin and -Vin, the integrator output change drastically in each phase. With CLS, in the second half of each phase ($S_{1b}$ and $S_{2b}$), the OTA output return to common mode before the integration of the opposite signal in the next phase. This is illustrated in Fig.3.2©. Hence using CLS relaxes the OTA slewing compared to the one implemented without CLS.

## 3.3 PPD Two-step IADC

### 3.3.1 Architecture:

The conceptual block diagram of a two-step incremental ADC [11] using two-capacitor SAR-assisted extended counting is shown in figure 3.3. In the first step, the IADC is configured as a first order ΔΣ loop with an input feedforward architecture. In the second step, a two-capacitor SAR-assisted extended counting enhances the accuracy. A single active integrator is shared in both steps. The detailed block diagram along with timing diagram is shown in fig.3.3. One conversion is divided into two intervals, M1=256 is assigned to the first step and M2=10 is assigned to second step [22]. During the first step IADC configured as first order ΔΣ loop with a input feedforward architecture and 1-bit quantizer is used for high linearity. At the end of step 1 operation (after M1 clock cycles), the quantization residue Vres is stored at the output of integrator. In the second step, when the EN_ST2 goes high, the input path and the feedforward path are disconnected from the circuit, and the two-capacitor DAC is connected to the input and the quantization residue Vres is further quantized using the two capacitor SAR for $M_2$ clock cycles. After $M_1$+$M_2$ clock periods, the conversion cycle is completed and the output bits streams from the two steps are combined by the reconstruction filter.

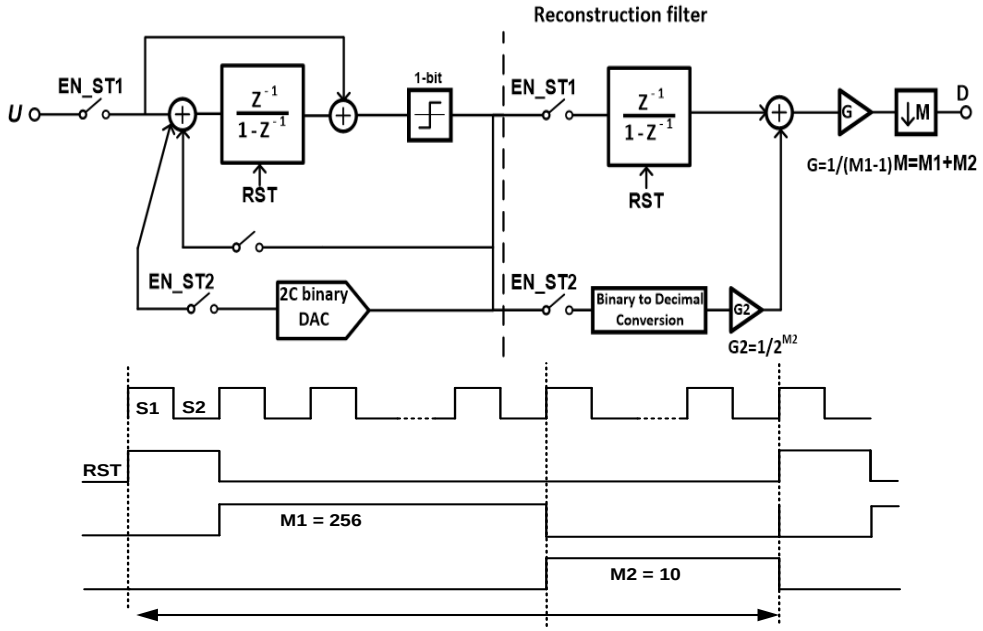



Fig 3.3 System level block diagram

The quantization residue Vres after M1 clock periods is given by:

$$V_{RES}[M_1+M_2]=\sum_{i=1}^{M_1-1}V_{IN}[i]-\left[\sum_{i=1}^{M_1-1}D_{S1}[i]-\frac{1}{2^{M_2}}\sum_{i=1}^{M_2}2^{M_2-i}\cdot D_{S2}[i]\right]\cdot V_{REF} \tag{3.3}$$

Here $D_{s1}$ and $D_{s2}$ are the digital output bits for the first and second steps, respectively. Vref is the reference voltage of the conversion at the end of the second step. The binary counting leaves the residue

$$V_{ref}[M+M2] \le \frac{V_{ref}}{2^{M2}} \tag{3.4}$$

The equivalent $V_{in}$ can be expressed as :

$$\overline{V_{IN}}=\frac{1}{M_1-1}\left[\sum_{i=1}^{M_1-1}D_{S1}[i]+\frac{1}{2^{M_2}}\sum_{i=1}^{M_2}2^{M_2-i}\cdot D_{S2}[i]\right]\cdot V_{FS}+\frac{V_{FS}}{(M_1-1)\times 2^{M_2}} \tag{3.5}$$

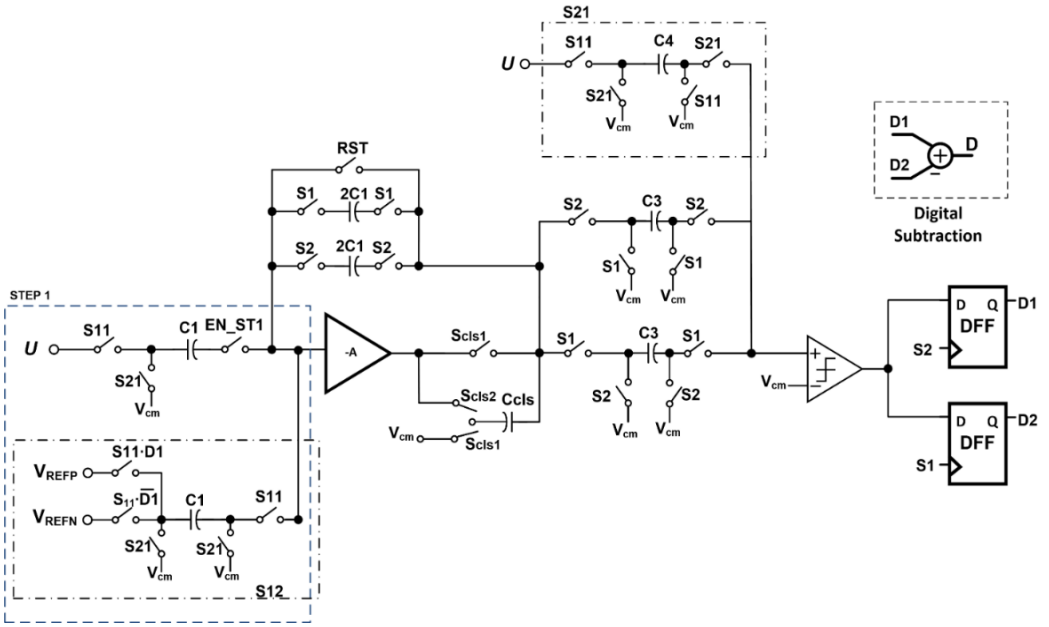
Where $V_{FS}$ is the input full scale input voltage. The first term suggests the digital reconstruction filter shown in Fig 3.2, the second term gives the quantization error of the IADC. Therefore, the ideal SQNR of the two-step IADC is

$$\text{SQNR} = 20\log_{10}(M_1.2^{M_2}) \tag{3.6}$$

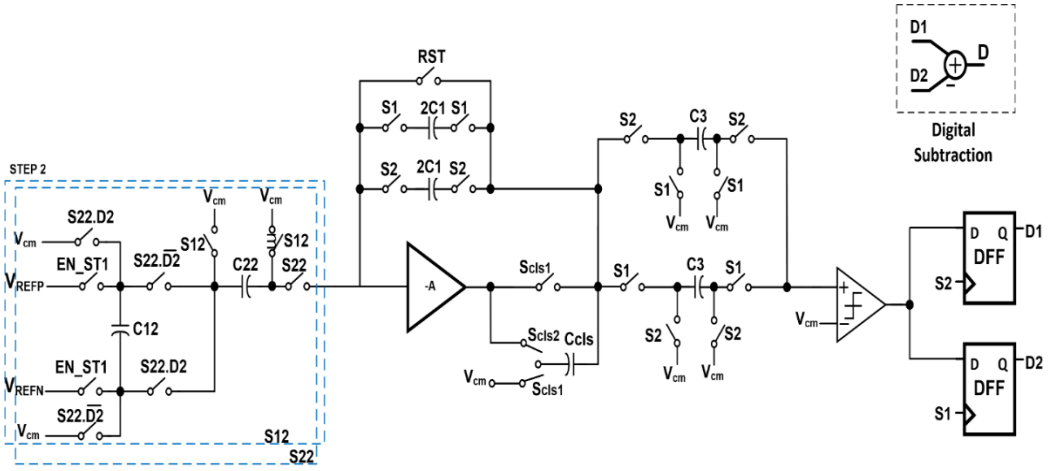
### 3.3.2 Circuit Implementation:

The switched capacitor implementation of two-step incremental ADC using pseudo-pseudo differential (PPD) structure is shown in fig.3.4. The subtraction is implemented in digital domain, the first step is first order IADC with input feedforward architecture as shown in fig.3.4(a). This consists of PPD integrator with CLS technique, two feedback DACs, passive adder and quantizer implemented with one comparator and two latches. The input signal is sampled and integrated in phase S1, and comparator makes a decision followed by latch operating on rising edge of phase S2 and output bit is feedback to DAC during the next phase S1. During clock phase S2, the input signal is disconnected and the top plate of sampling capacitor C1 is connected to the vcm and hence the inverted input stored on C1 is integrated by the second path active in clock phase $S_2$, and processed by comparator and latch operating on the rising edge of clock phase S1 and the output bit is fed back on the next clock phase S2. The output bits D1 and D2 are subtracted in the digital domain. PPD IADC works in time interleaved fashion, processing vin in one phase and the inverted input in the other phase.

The input sampling switch is implemented with NMOS which is bootstrapped for high linearity. The feedback switches towards the output are implemented with transmission gates, whereas the ones connecting to virtual ground are implemented with PMOS devices, these PMOS switches are turned off before the end of clock phase to suppress the effect of charge injection and IO devices have been used to implement




(a)




(b)

Figure.3.4 (a) Step 1 operation: First order IADC (b) Step 2 operation: Extended counting with two-capacitor SAR.

feedback switches as the threshold voltages of regular vt devices are small and cause significant charge leakage between the two phases. The charge pump is used to generate clock phases for feedback switches. All the switches connecting to vcm are implemented with NMOS devices, DAC switches connecting to Vrefp and Vrefn are implemented with PMOS and NMOS devices, respectively. The rest of the series switches are implemented with transmission gates.

The second step is implemented using two-capacitor SAR shown in Fig 3.4(b). The quantization residue Vres stored at the integrator output in the first step is further quantized by the two-capacitor SAR. This contains a two-capacitor DAC and the same integrator and quantizer used in step1. During the step1 operation, the capacitor C12 is pre-charged to the reference voltage. When the step2 operation starts, C12 is disconnected from the reference voltage and the charge in C12 is then shared with C22 based on the previous bit decisions $D_1$ and $D_2$. If the previous bit is 1, the bottom plate is connected to C22 and if the previous bit is 0, the top plate is connected to C22 for the charge distribution. The redistributed charge is then transferred into the integration capacitors, to cancel the residue the voltage. Hence within M2 periods, a set of binary coefficients $1/2^N$ (N=1 to M2) is generated by charge redistribution and the conversion performs a successive approximation. In the actual implementation, to minimize the effect of parasitic capacitances, the capacitor C12 is split into two capacitors and are cross connected.

### A. Integrator Opamp:

The two-step IADC with SAR extended counting technique requires high DC gain in the second step, as the accuracy of the charge transfer is directly related to the DC gain of the OTA in the integrator. The simulation shows that the DC gain of the OTA should be greater than 85 dB. The high DC gain requirement may require some gain enhancement techniques such as gain boosting or adding a second stage (need compensation for stability). These techniques increase the complexity of the design and power consumption. Hence, the CLS technique is used in the PPD integrator which relaxes the gain and output swing requirement of the OTA. The simulation results in Fig.3.6 shows that DC gain 60 dB is sufficient to achieve SNDR of more than 96 dB with CLS technique.

As PPD structure is implemented with a single-ended architecture, single-ended amplifiers can be used for improved power efficiency compared to fully differential amplifiers which requires additional common mode feedback circuitry. A cascoded class-C inverter [12] OTA circuit is designed with a supply voltage of 1.3 V. The requirement of class c operation is to choose supply voltage slightly lower than the sum

of the input transistors threshold voltages of PMOS and NMOS. IO devices are chosen to reduce the leakage current and get higher DC gain. At typical corner, M1 Vth is -0.6 V and M2 Vth is 0.56 V. The OTA consumes 140 µA with DC gain and unity gain

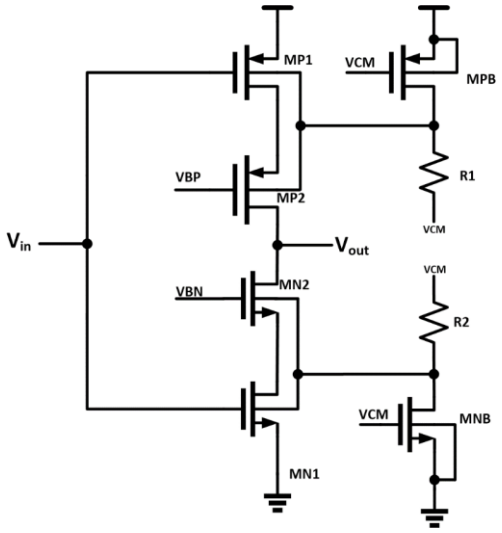



Fig.3.5 Cascoded Inverter OTA with body biasing

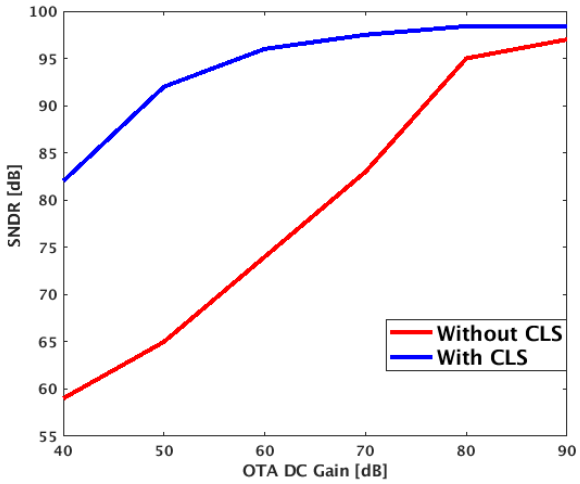



Fig.3.6 Simulated SNDR of two-step IADC vs OTA DC gain with and without CLS

bandwidth are 64 dB and 87 MHz, respectively. On-chip body biasing technique [12] is used to make the inverter OTA less sensitive to PVT variation. The on-chip body bias module consists of transistor M5 and M6 and off chip resistors R1 and R2. M5 and

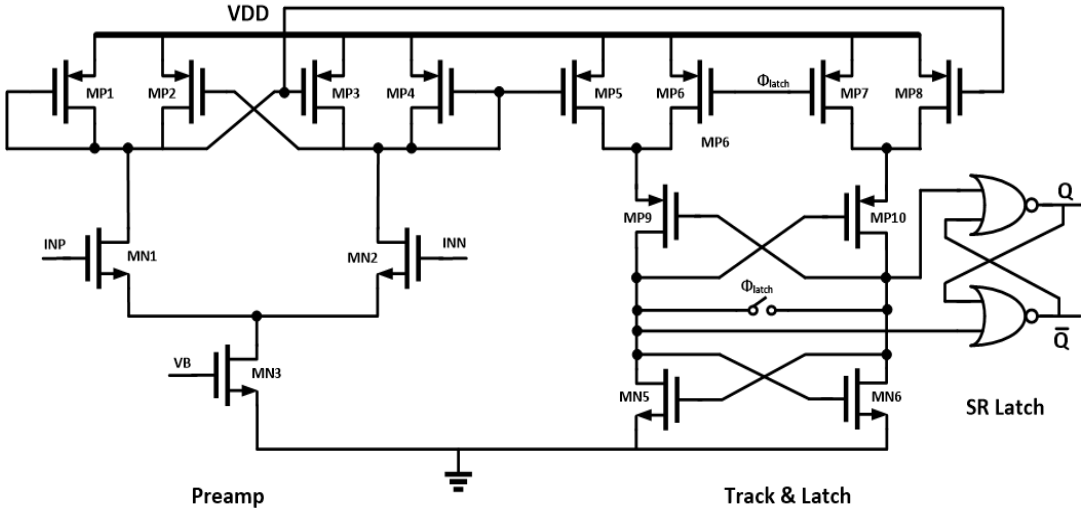



Fig.3.7 Circuit diagram of Comparator used in quantizer

M6 are biased in subthreshold region to detect the parameter variation of M1 and M2, respectively.

### B. Passive Adder and Quantizer

A switched capacitor adder is used at the input of the quantizer to combine the ADC input and the integrator output. Since the PPD implementation consists of two signal processing paths, the passive adder is required to have two paths in two clock phases S1 and S2, one with the input signal and the other with the inverted input signal. Due to charge sharing, signal attenuation takes place at the input of quantizer. Therefore, a preamplifier is used before the comparator. The quantizer is implemented with one comparator and two latches.

### 3.3.3 Simulation Results

The design was implemented in a 65nm CMOS technology. The single-ended class-C inverter suffers from poor power supply noise rejection ratio (PSRR). The pseudo-differential structure can improve the inverter's PSRR, but the improvement depends on the matching between the two branches. In the proposed PPD architecture, the low-frequency power supply noise sampled in both phases is filtered after subtraction, whereas high frequency noise is not suppressed. Then, one crossing point can be

observed in Fig.3.8, where after certain frequency, the PSRR of the PPD scheme becomes worse than that of the PD one. However, this is not an issue for low bandwidth applications. Also, high-frequency noise from supply voltage can be efficiently attenuated by filtering with passive components The PSRR simulation results for switched-capacitor integrators with a single-ended structure, a pseudo-differential structure with a 0.2% mismatch, and for an integrator using PPD

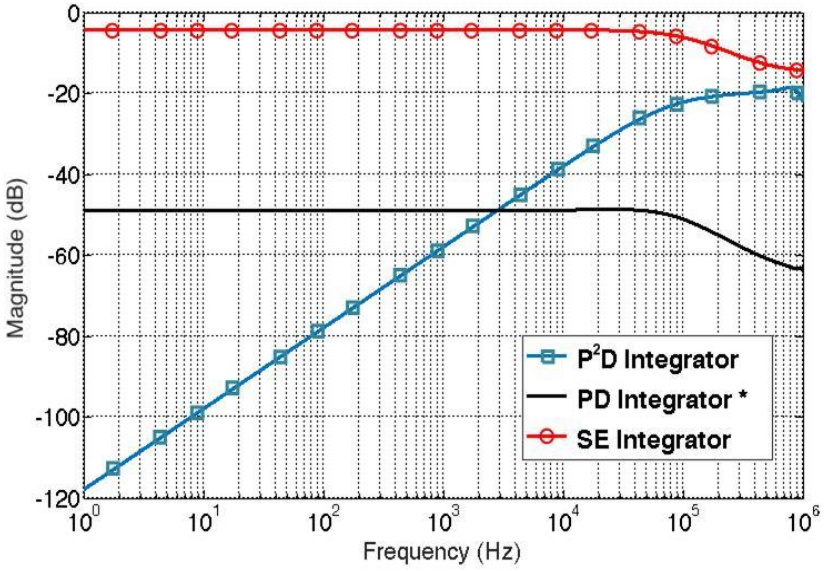





Fig. 3.8. Simulated power supply noise rejection of SC integrators. The pseudo-differential structure had a 0.2 % mismatch.

architecture, are shown in Fig.3.7. The noise suppression provided by PPD scheme is more efficient than that of the PD structure even with significant mismatch.

The PSD of the PPD two-step IADC is shown in Fig. 3.9. In the first step, configured as a first order single bit IADC give and SNR of 48 dB and the two-capacitor SAR in the second step improves the SNR to 98 dB. The sampling frequency is 10.72 MHz, and the signal bandwidth is 20 kHz. Fig 3.10 shows the complete transistor level simulation of two-step IADC with single ended and PPD implementations. We can observe that the DC offset, low frequency noise and second harmonic are suppressed in the PPD implementation compared to the single ended one.

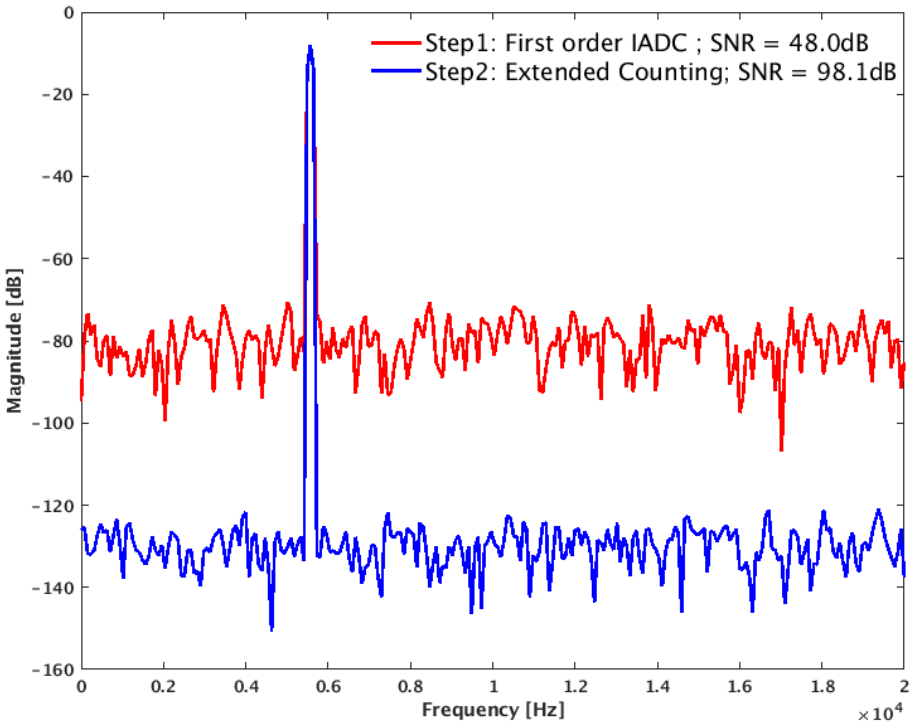



Fig.3.9 Simulated PSD of PPD two-step IADC

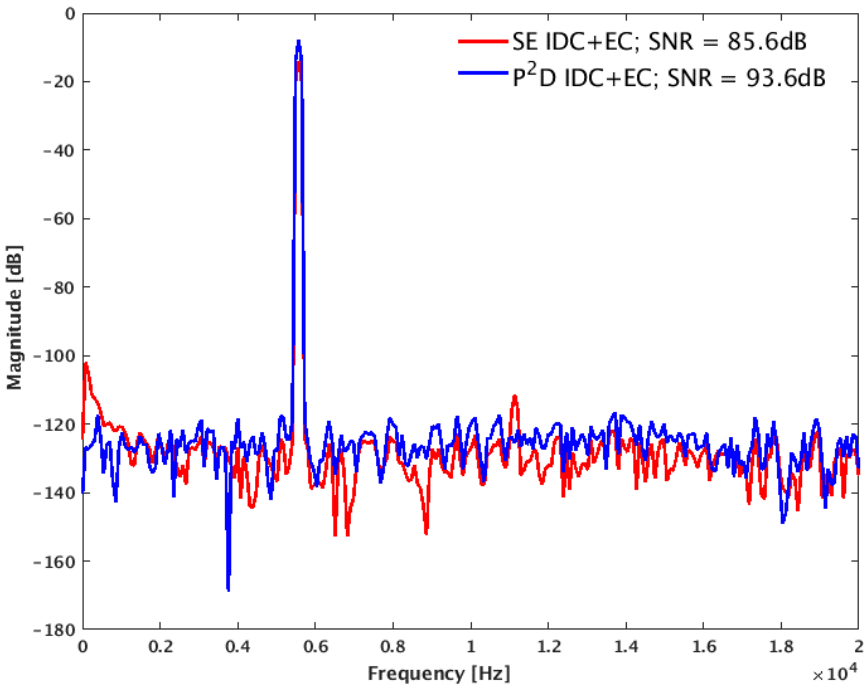



Fig.3.10 PSD of two-step IADC with single ended and PPD implementation.

### 3.3.4 Measurement Results

The prototype chip of PPD two-step IADC was implemented in 65nm CMOS technology. The active area of the chip is 0.2184 $mm^2$. The chip micrograph is shown in Fig.3.11 and it is packaged is 60-pin QFN.

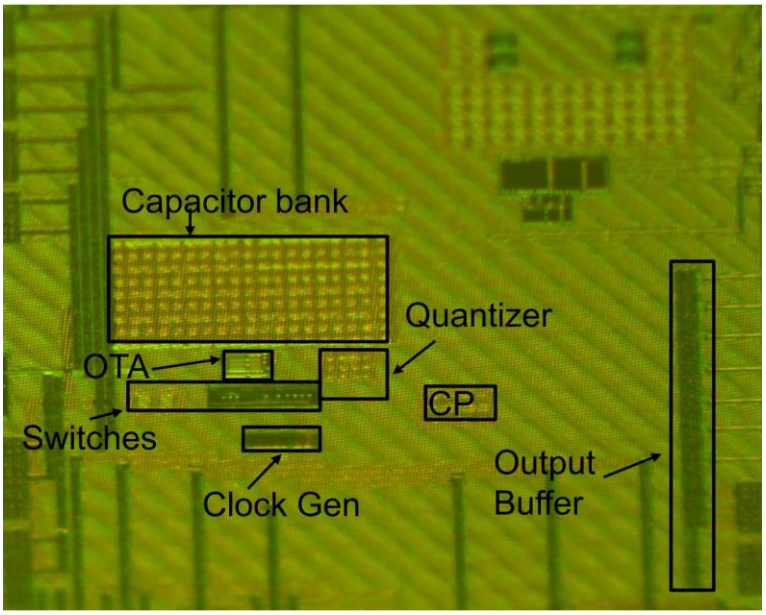



Fig.3.11 Chip Micrograph

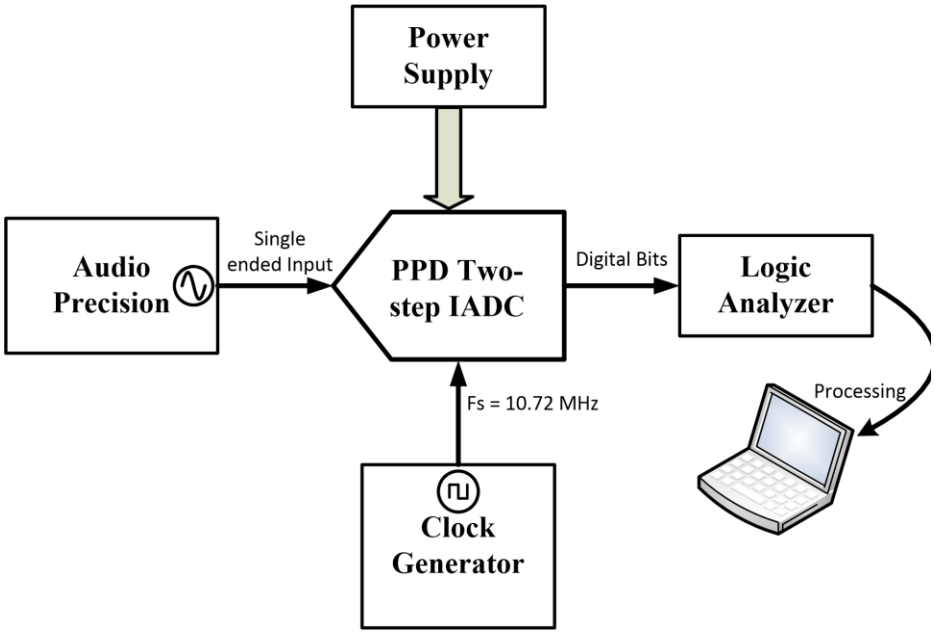



Fig. 3.12 Test Set up

The complete test setup is shown in Fig. 3.12. An Audio Precision signal generator was used to give a single ended input to the ADC. The main supply is used for the

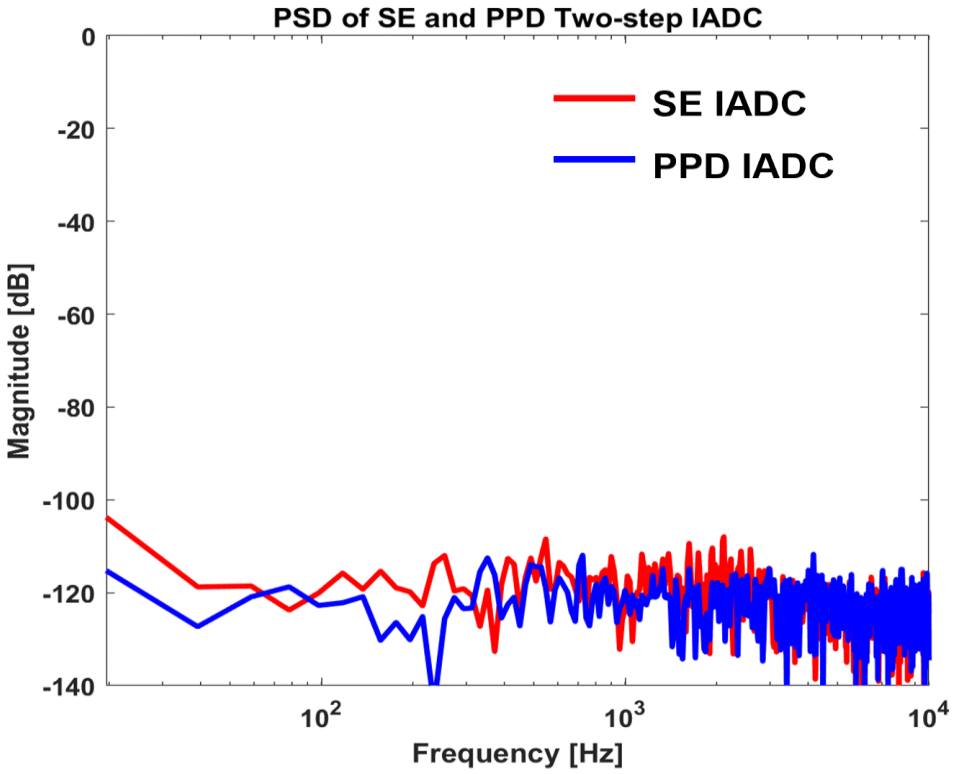
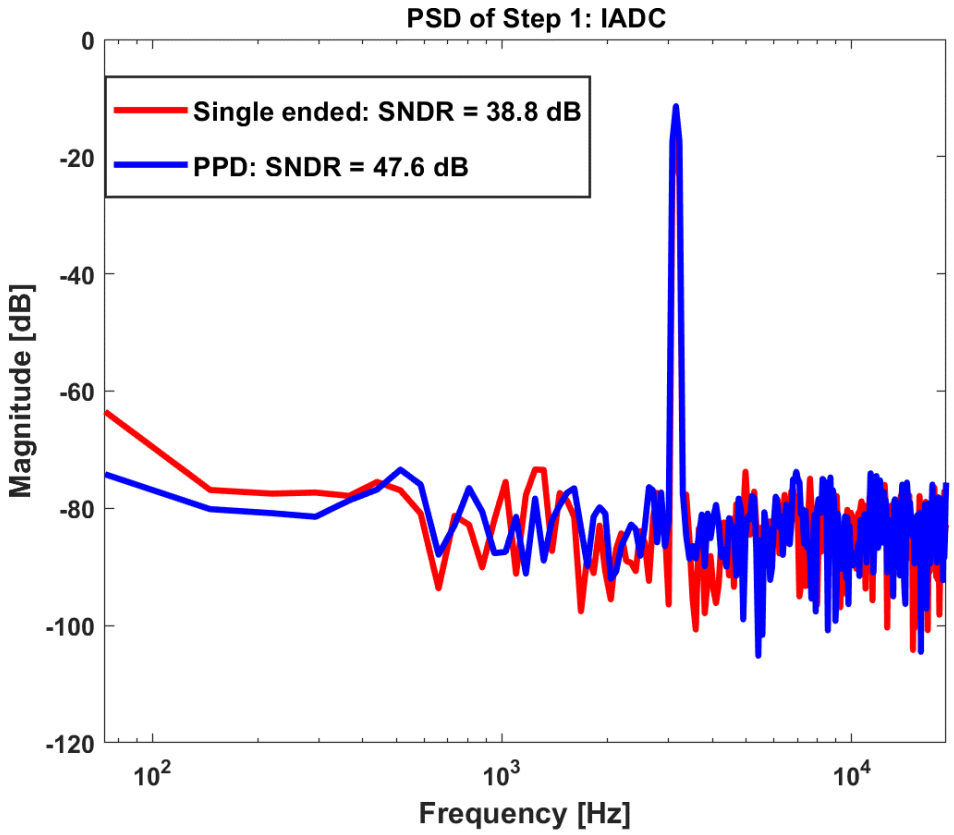


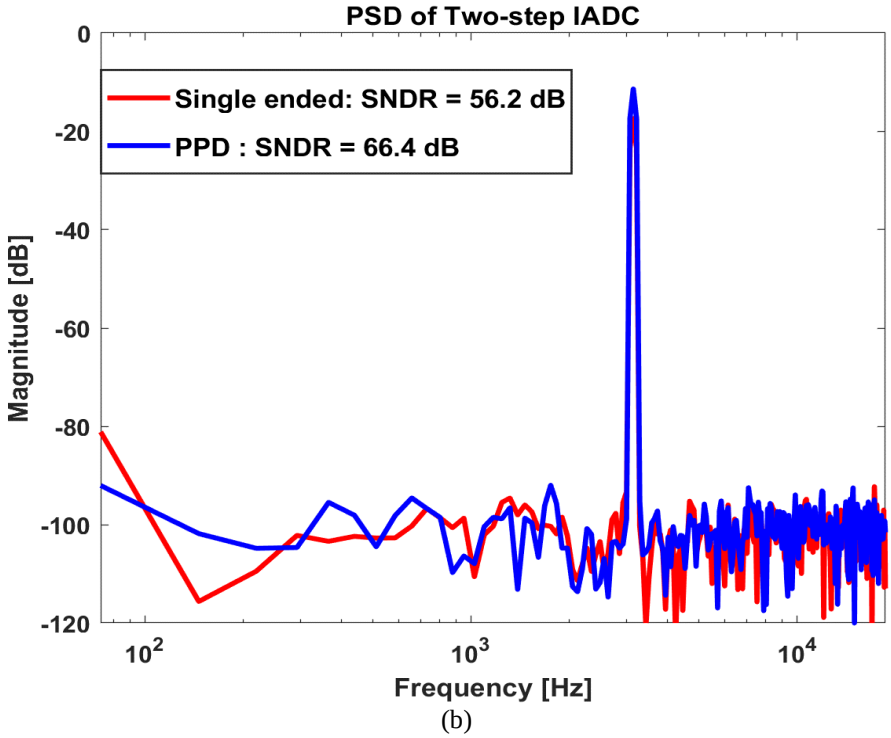

Fig.3.13 Noise floor of Single ended and PPD two-step IADC

PCB board and supply voltages, reference voltages and common mode voltages are generated using LDOs on board.

The chip was tested with sampling frequency of 10.72 MHz, the signal bandwidth of ADC is 20 kHz. The measurement results are shown in fig 3.14. PPD two-step IADC achieves around 9 dB better SNDR compared to the single ended implementation. The PSD shows that the signal is doubled, and the low frequency is suppressed in PPD compared to single ended implementation.




(a)




(b)

Fig.3.14 Measured PSD of SE and PPD (a) IADC in step 1 configuration (b) two-step IADC

# Chapter 4. Charge Compensation Technique for Switched Capacitor Circuits

This chapter introduces several slew enhancement techniques. The first section of the chapter discusses active and passive charge compensation techniques. The second half of the chapter describes the implementation of passive charge compensation technique in single bit second order delta- sigma ADC. The design was simulated in a 65 nm CMOS process. The sampling frequency of 12.8 MHz and the signal bandwidth of 25 kHz achieves an SNDR of 95 db. Post-layout extracted simulations with optimized design show more than 12 dB improvement in signal to noise and distortion ratio (SNDR) for the same static power.

## 4.1. Prior Active Charge Compensation (ACC) Techniques

The active charge compensated (ACC) SC integrator [13] is shown in Fig. 4.1. It contains a pair of auxiliary capacitors of value C1/G, and NMOS and PMOS current mirrors with 1:G ratio, operating in parallel with the conventional integrator. The scale factor G allows to keep the area overhead, dominated by capacitors, reasonably small. During phase S1, an amount of charge proportional to the input is stored in these auxiliary capacitors; during phase S2 the same capacitors are connected to the current mirror input transistors. Provided the voltage on the capacitors is above the MOS thresholds, the current mirror will operate in saturation, injecting an amplified current into the OTA output. This will progressively discharge the capacitors until their voltage reaches the transistors thresholds, entering in subthreshold region, where the injected current is negligibly small.

Charge compensation takes place at the beginning of S2, where the current mirrors inject a large current that flows through the feedback capacitor C2, quickly reducing the voltage difference between the OTA terminals. Hence the trade-off between bias and slewing current is broken, increasing the power efficiency. In [13] it is claimed that the OTA can reduce its current to 50%, without degrading the performance of the system in which it is tested.

Another active scheme using pre-charged load capacitor technique was proposed in [14] and applied to the residue-amplifier of the first stage of a pipeline

ADC. The idea is to reduce the slewing time by injecting charge at the OTA output during the amplification phase. To accomplish this, the load capacitor, composed of the sampling and feedback capacitors of the residue amplifier of the following pipeline stage, needs to be temporarily removed from the signal path and pre-charged to a voltage set by the input and the reference generated by the DAC, without disturbing the operation of the ADC. Thus, compared to a conventional residue amplifier, it needs an extra block to calculate the appropriate voltage, three sets of auxiliary capacitors to avoid interrupting the ADC operation, and additional output latency to pre-charge those capacitors. Despite the additional complexity a 30% speed increase for the same resolution and power is claimed.

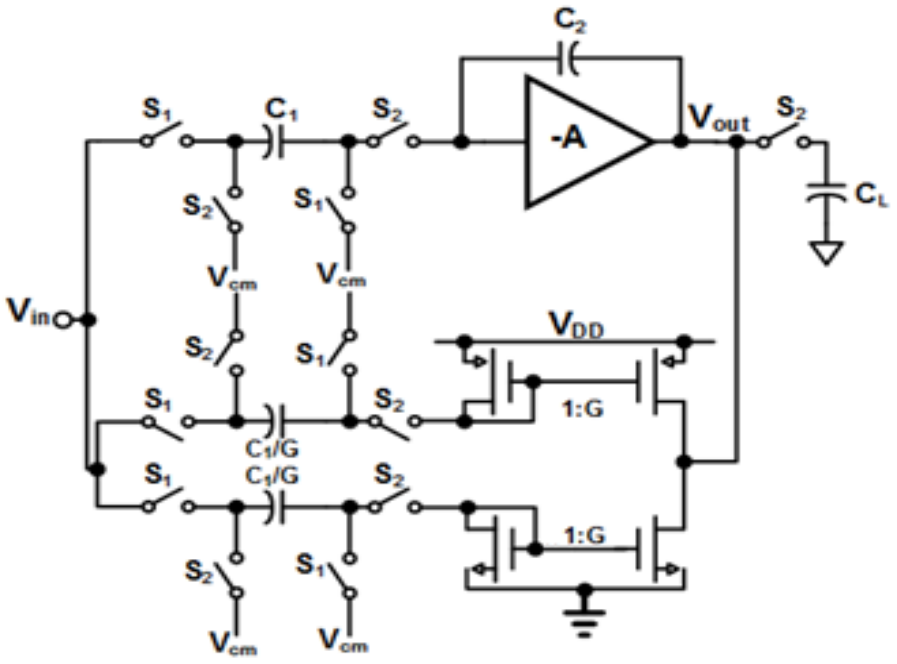



Fig. 4.1: Switched capacitor integrator with active charge compensation. 

Yet another active technique similar to [13] was proposed in [15] and applied to the integrator in a second order delta-sigma modulator. Based on the same fundamental idea to inject charge into the integrator's output, several injection methods were analyzed. Three of those provide the charge from a pulsed current source, differing in the nature of the current amplitude (continuous or discrete with one or three levels) and the pulse duration (fixed or variable). Apart from these, another method (method 3), using a capacitor and a precharge voltage was described. However, the

authors conclude that this method is not practical because it requires high precharge voltage beyond those of the supplies. However, as it will be shown later through derivation and analysis, such a high voltage is not required.

Although active techniques can improve the slew rate, the added active block makes them less attractive. In this paper we propose a fully passive technique which does not require additional Gm block, or a DAC or a buffer. The basic idea is to use the existing buffer (previous stage driver) that drives the input voltage. Such buffer or driver will always be required in any sampled data system.

### 4.2 Passive Charge Compensation (PCC) scheme

The proposed passive charge compensation integrator is shown in Fig. 4.2. An additional path is added at the output of the OTA for charge compensation. During phase $S_1$, the input is sampled onto $C_1$, while the charge compensation capacitor $C_3$ stores the output voltage of the OTA generated in the previous clock phase. During phase $S_2$, the OTA provides a charge equal to $C_1V_{in}$ to the top plate of $C_2$, in addition to charging the load capacitor. The total charge the OTA needs to provide during $S_2$ without using the compensation technique is given by

$$\begin{aligned} q_{OTA}(n) &= C_{LTOT}\left(V_{out}(n)\right. \\ &\quad \left. - V_{out}(n-1)\right) \\ &= C_{LTOT}\,\frac{C_1}{C_2}V_{in}(n) \end{aligned} \tag{4.1}$$

where $C_{LTOT} = C_2 + C_L$. In the charge compensation technique, an additional charge proportional to the input voltage is provided through $C_3$. Since the required charge is a linear function of $V_{in}$, it is intuitive to try to use $V_{in}$ to inject charge at the output of the OTA. Let us introduce a compensating capacitor $C_3$ connected between output of the OTA and $V_{in}$ as shown in Fig. 4.2 (a) and solve for the value of $C_3$ required to inject the required charge. During $S_2$ the charge compensation capacitor voltage switches from $V_{out}(n-1)$ to $V_{out}(n) - V_{in}(n)$. Then the total charge delivered by the compensating capacitor is:

$$q_c(n) = C_3(V_{in}(n) - (V_{out}(n) - V_{out}(n-1))) = C_3\left(V_{in}(n) - \frac{C_1}{C_2}V_{in}(n)\right) \quad (4.2)$$

Now for these charges to be equal, we need:

$$(C_2 + C_L)\frac{C_1}{C_2} = C_3\left(1 - \frac{C_1}{C_2}\right) \quad (4.3)$$

$$C_3 = C_1\frac{1 + \frac{C_L}{C_2}}{1 - \frac{C_1}{C_2}} = C_1\frac{C_2 + C_L}{C_2 - C_1} \quad (4.4)$$

A detailed derivation is given in the Appendix A. If the input varies slowly (i.e. it is oversampled) the OTA can still be greatly relaxed, since only a charge proportional to the difference between of the input voltages in two phases needs to be provided. In such case, as shown in the Appendix, the frequency response of the charge needed from the OTA due to the input can be reduced from $C_{LTOT}\frac{C_1}{C_2}$ to about

$$C_3\frac{\pi}{2 \cdot OSR} \quad (4.5)$$

For reasonably high oversampling ratios (OSR), the required charge from the OTA will be much smaller using PCC than using a conventional integrator.

In the case of a fully differential structure the above results remain valid. In the case of a non-delayed differential integrator the charge from the OTA can be exactly cancelled by connecting the bottom plate of $C_3$ to $-V_{in}$ at the same time as when $C_1$ is connected to $V_{in}$. The optimal value for $C_3$ is the same as before. There will be no effect of delay and the charge compensation will be more accurate and independent of OSR. Although $C_3$ provides the correct charge at the output of the OTA, it also acts as additional load during $S_2$, degrading the integrator's bandwidth and hence slowing the residual settling process. However, since most of the charge through $C_3$ is already transferred at the beginning of $S_2$, it can be disconnected after some time in $S_2$. The amount of time it needs to be connected depends on switch resistances and hence the behavior of the initial transient, which can be optimized during circuit simulation.

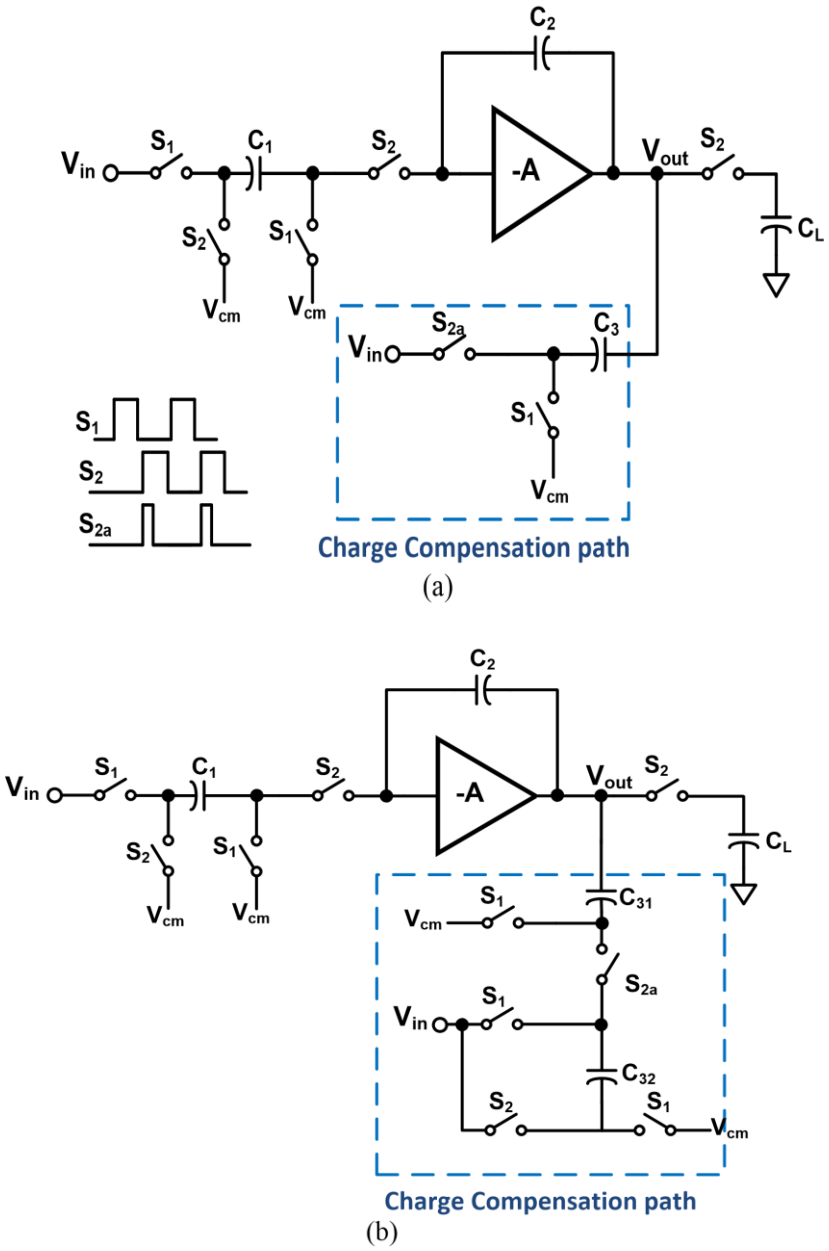



Fig. 4.2: (a) Proposed passive charge compensation scheme for $C_1/C_2 < 1$ (b) proposed passive charge compensation for $C_1/C_2 > 1$. 

### 4.3 PCC for higher SC stage gain

The denominator of $C_3$ in eq (4.4) shows a dependence on the integrator gain $C_1/C_2$. In order to get a realizable value for $C_3$, the gain has to be smaller than 1. However, some applications require a gain larger or equal to 1. One way to achieve this is to replace the compensation circuitry with a set of *n* equal-valued capacitors which

are charged in parallel during phase $S_1$ and connected in series during phase $S_2$. Now, the gain restriction is relaxed to $n > C_1/C_2$, at the cost of additional switches and capacitors. In Fig. 4.2(b) an implementation for a stage gain below 2 ($n$=2) is shown. The values of the compensation capacitor are:

$$C_{31} = C_{32} = 2C_1 \cdot \frac{C_2 + C_L}{2C_2 - C_1} \qquad (4.6)$$

***Simulation and comparison of various schemes***

A set of simulations was run using the transistor level OTA shown in Fig. 4.3. The integrators were implemented in a single ended structure using $C_1$=2 pF, $C_2$=4 pF and $C_L$=0.5 pF. For the PCC integrator, using eq. (4.4), $C_3$ was calculated to be 4.5 pF. Also, in order to avoid degrading the loop bandwidth, as discussed in the previous section, $C_3$ was disconnected from the OTA after 3 ns from the beginning of $S_2$.

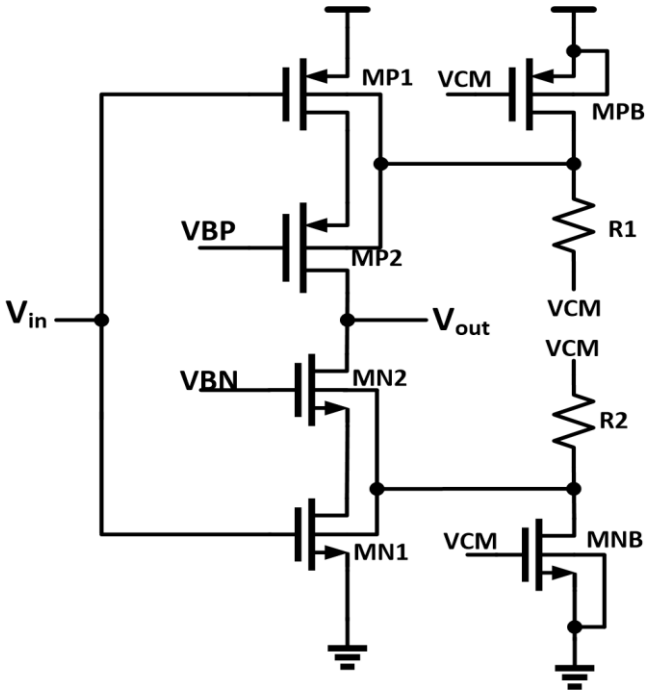



Fig. 4.3: Schematic of the inverter-based OTA 

The step response of the system was simulated, using a positive input step of height $V_{DD}/2$. Fig. 4.4(a) shows the integrator output voltage transient during the charge transfer phase $S_2$. The DC voltage of the OTA (also equal to $V_{DD}/2$) has been removed for clarity. Also, the voltage at the virtual ground node is plotted in Fig. 4.4 (b).

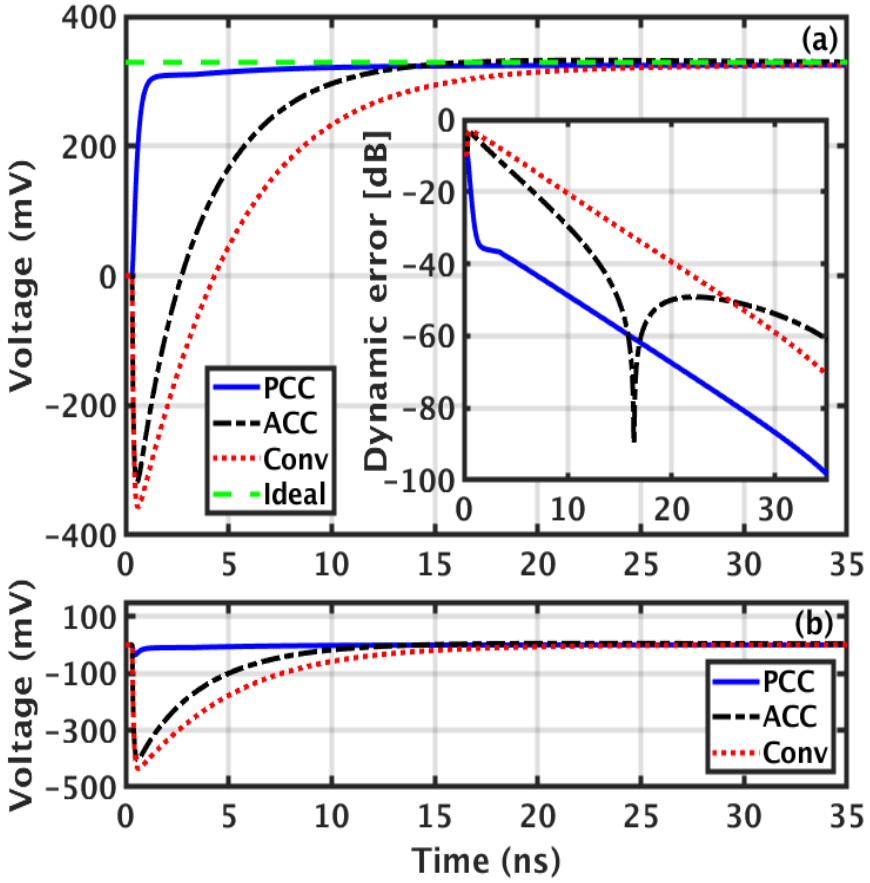



Fig. 4.4: (a) Integrator output voltage and inset shows dynamic error, (b) Voltage at the virtual ground node.



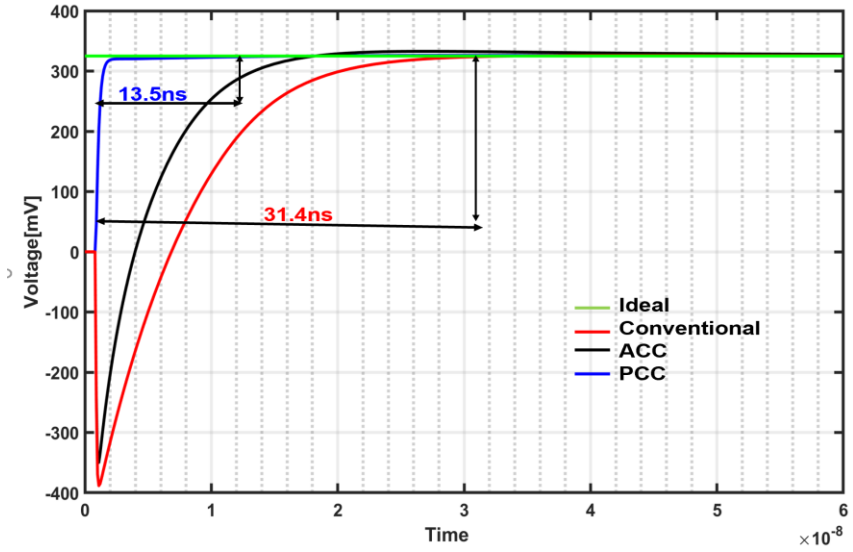



Fig. 4.4: © Settling time for 1 mv accuracy.

It can be seen that initially both ACC and the conventional integrator have a feedforward transient through C2. In the PCC integrator the compensation path counteracts this effect, starting from a more favorable initial condition. Moreover, after 3.5 ns, once the compensation path is disconnected, the dynamic error for PCC evolves with a slope similar to that of the conventional integrator, but with an over 20 dB advantage. It is interesting to notice that the ACC, even though faster than the conventional integrator, seems to overshoot around 17 ns, producing the notch seen in the logarithmic plot shown in the inset of Fig. 4.4(a). Then it quickly degrades to an error level comparable to the conventional integrator. Finally, all three integrators settle to the same overall error determined by the static error, set by DC gain of the OTA, which is 70 dB (yielding a static error of -70 dB).

From the virtual ground voltage plot (Fig. 4.4(b)), it is clear that the disturbance on the PCC integrator is greatly reduced, experiencing a peak of only about -36 mV, compared to -404 mV in the ACC and -434 mV in the conventional one. This makes the PCC integrator a better approximation to an ideal integrator. Fig. 4.4(c) depicts the settling time for 1 mv accuracy. It can be observed that PCC slews fast and reached 1 mv in 13.5 ns whereas the conventional integrator takes around 31.4 ns to settle to the same accuracy. Given sufficient time for settling all integrators settles to the same accuracy depending on the gain of the OTA.

In Fig. 4.5, the OTA's output current is shown, where the convention used represents current and charge through the OTA as positive (negative) if sourced (sank) by it. With a conventional inverting integrator, for a positive input step, it would be expected that the output current is sourced by the OTA. This is confirmed by simulations, both for conventional and ACC, as shown in fig.7. The total charge provided by the OTA in a conventional integrator is 110% of $C_1V_{in,}$ while that for ACC it is only 58%, showing some improvement. However, the PCC OTA only needs to provide 5% of $C_1V_{in,}$ as shown in Fig.4.5. This shows the significant improvement achieved by the proposed charge compensation scheme. Ideally, the total charge provided by PCC OTA should be zero, but practical non-idealities prevent this. This is partly due to mismatch in switch resistances at the initial transient. However, the total charge within such transient is very small.

## 4.4 Second-Order DSM using PCC Scheme

### 4.4.1 Modulator architecture

A delta-sigma modulator with a multi-bit quantizer has reduced quantization noise compared to one with a single-bit quantizer for the same loop order and oversampling ratio. Hence the swing at the output of the feedback DAC is smaller which relaxes the linearity requirements of the loop filter. This benefit is gained at the cost of increased power consumption in the multi-bit quantizer and the mismatch errors in the feedback DAC, which can significantly degrade the linearity. The DAC mismatch error can be shaped using dynamic element matching or corrected using digital calibration. Both techniques require additional power and area. In the case of a single-bit delta-sigma ADC, the feedback DAC is inherently linear. Hence, no extra calibration is required, and only one comparator is needed for the quantizer implementation. But in such design the feedback DAC has a larger output swing

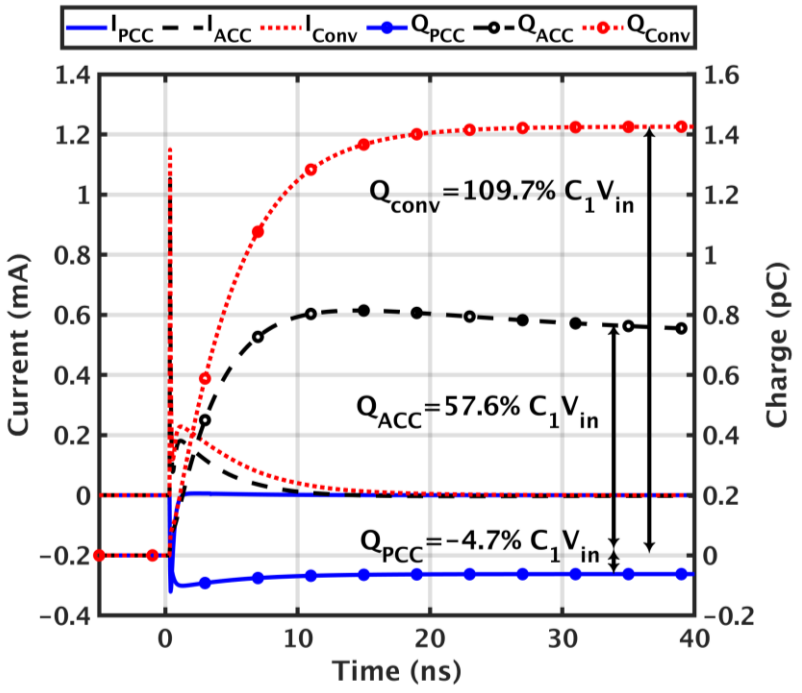



Fig 4.5: Current and charge sourced/sunk by OTA in various integrator schemes.



between $\pm V_{ref}$, and the first integrator must provide a large slewing current or avoid slewing altogether. Hence the design of first integrator in the loop filter becomes challenging, and it usually consumes a significant part of the total power budget. The

proposed charge compensation technique can be applied to the first integrator in discrete-time DSM to relax the OTA design requirement and hence save significant power without compromising performance.

A single-bit second order DSM low distortion structure [15] was chosen as a test case for circuit implementation as shown in Fig.4.6. An OSR of 256 gives an ideal SQNR of 102 dB which is reasonable for a target specification of more than 15-bit resolution.

### 4.4.2 Circuit implementation

The switched-capacitor implementation of the single-bit second-order DSM is shown in Fig. 4.7. The actual implementation is pseudo-differential, but the single-ended version is shown for simplicity. The switched-capacitor common mode feedback is used to correct the output common mode drift. An active adder is used to implement the analog summation at the input of the quantizer. The input sampling capacitor is shared with the feedback DAC and the input network is replicated in the charge compensation path.

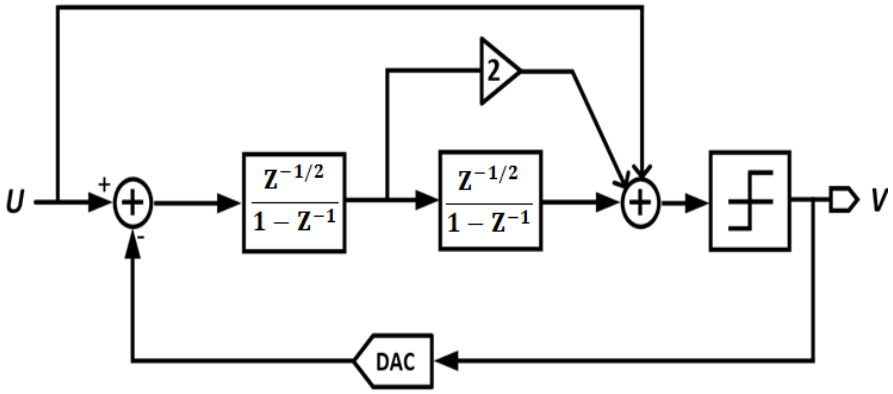



Fig. 4.6: Low distortion second-order DSM architecture



Inverter based OTAs have gained attention in recent times as they are highly power-efficient and achieve good performance in delta-sigma ADCs [16]. There are several attributes which makes them more efficient than conventional telescopic and folded cascode OTAs. Since the input is applied to both PMOS and NMOS devices, the transconductance is doubled for the same bias current, hence achieving better slew-rate, gain bandwidth and noise performance. The main drawbacks of inverter based OTAs are low gain and sensitivity to process, voltage, and temperature (PVT) variations.

Several techniques have been published in recent works to improve the robustness to PVT variations. In [18] a dedicated LDO is used to adjust the inverter supply voltage, and a replica inverter is used in the feedback path to sense PVT variations and adjust the LDO voltage. However, an extra block is required along with the LDO to generate the input common mode voltage, which consumes extra power and area. Dynamic biasing was proposed in [19]; however, switching cascode transistors limit the operating bandwidth of the inverter. An on-chip body biasing technique was proposed in [12], where a separate circuit with a transistor and a resistor is used to track PVT variations, and to adjust the bulk voltage of the transistors in the inverter. The proposed passive charge compensation technique relaxes the OTAs requirements by significant amount, as most of the charge is provided by the charge compensation circuit during slewing. Hence, even at the slow corner when the OTA current is significantly low, the error charge can be compensated by charge compensation circuit.

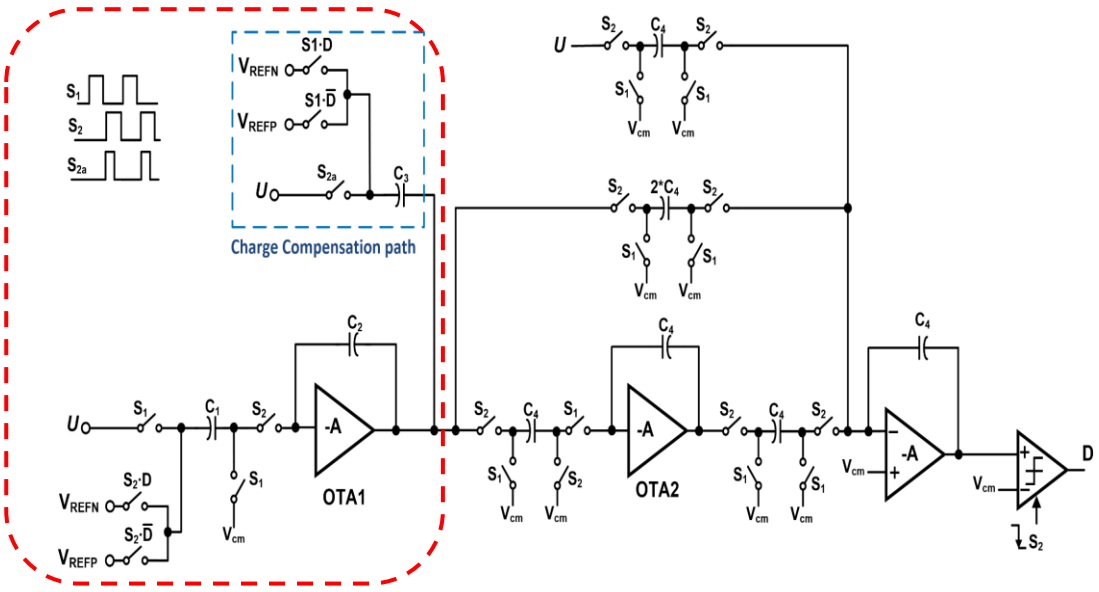



Fig. 4.7: Second-order delta-sigma ADC with a charge compensation path in the first integrator



The first integrator was implemented with the inverter OTA shown in Fig. 5. The OTA in the second integrator is a scaled version of the first OTA. An on-chip body bias is used to reduce the sensitivity to PVT variation. The simulated performances of OTA1 and OTA2 are given in Table I.

The input switch in the charge compensation path was implemented with a transmission gate. Since the linearity of the switch is not critical, bootstrapping was not required. The charge injection is not an issue here, since the switch is turned on only for one half of the clock phase $S_2$. Positive and negative reference switches are implemented with PMOS and NMOS transistors, respectively. The comparator was implemented with a conventional strong-arm latch [21].

Table I: Simulated performance of OTAs

| **Specification** | **OTA1** | **OTA2** |
|---|---|---|
| Supply Voltage | 1.3 | 1.3 |
| DC-gain(dB) | 70.4 | 70 |
| GBW(MHz) | 38 | 26 |
| Phase Margin (degree) | 74 | 80 |
| Static Power Consumption (μW) | 23.4 | 17 |

### 4.4.3 Simulation Results

The proposed second-order DSM with charge compensation technique was designed in a 65nm CMOS technology. The performance of DSM with the charge compensated integrator of Fig. 4.2(a) was compared to the same DSM with conventional integrator. The circuit implementation of the second-order DSM is shown in Fig. 4.7. To further verify the practicality of the proposed technique, the front-end of the DSM was laid out and post layout extracted simulation was performed. The results are presented in Fig. 4.8. The input sampling capacitor was chosen to be $C_1$ = 2 pF based on thermal noise requirement, to achieve more than 15-bit resolution. Also, an integrating capacitor $C_2$ = 4 pF and a charge compensation capacitor $C_3$ = 4.5 pF was chosen. The capacitors in the subsequent stage were $C_4$ = 0.5 pF.

The signal bandwidth is 25 kHz, and the sampling frequency was 12.8 MHz, for an oversampling ratio of 256. The power spectral densities (PSDs) with and without charge compensation are shown in Fig.4.8. The input signal amplitude was -6 dBFS and the signal frequency was 5.47 kHz. There is a significant reduction (15 dB) of the

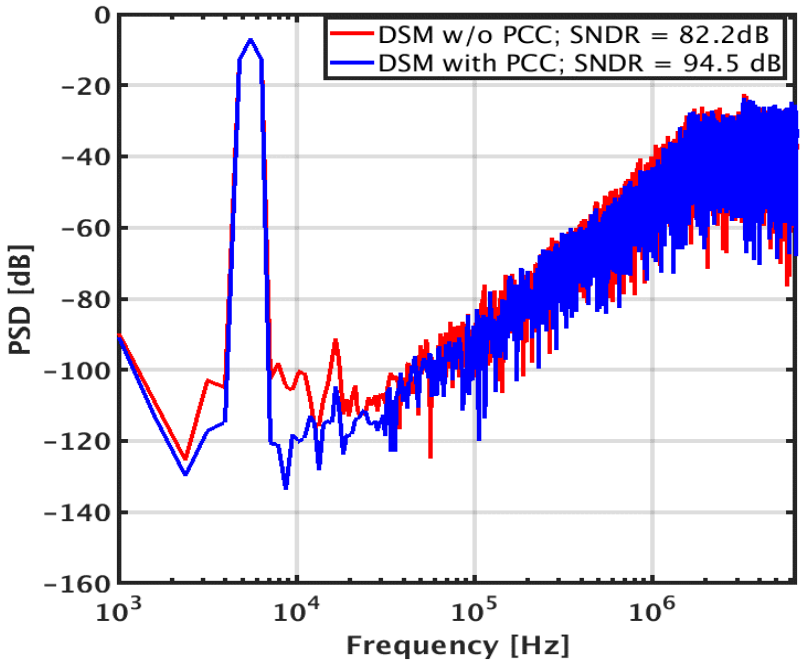



Fig.4.8: PSD of extracted second-order DSM

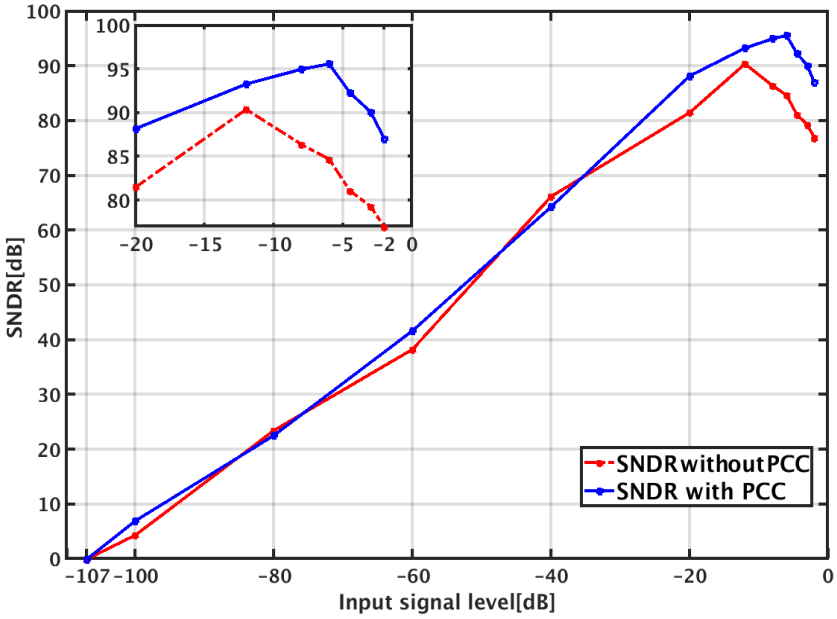
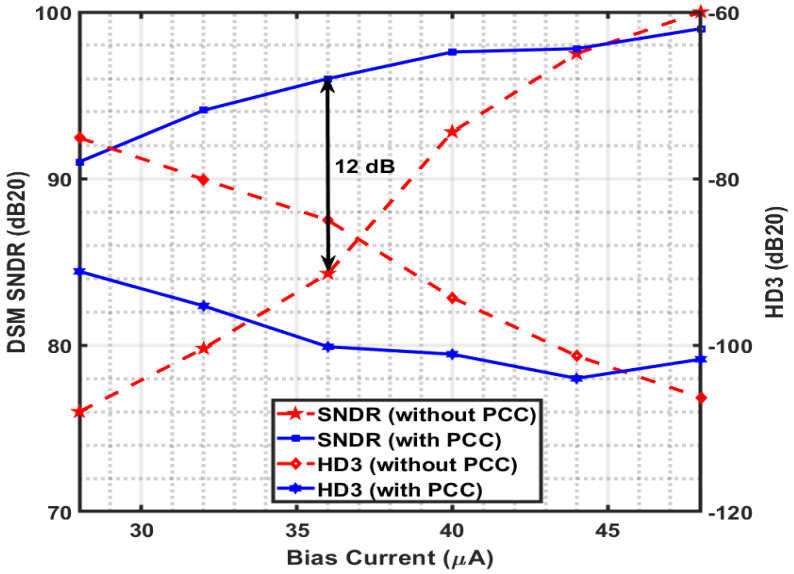



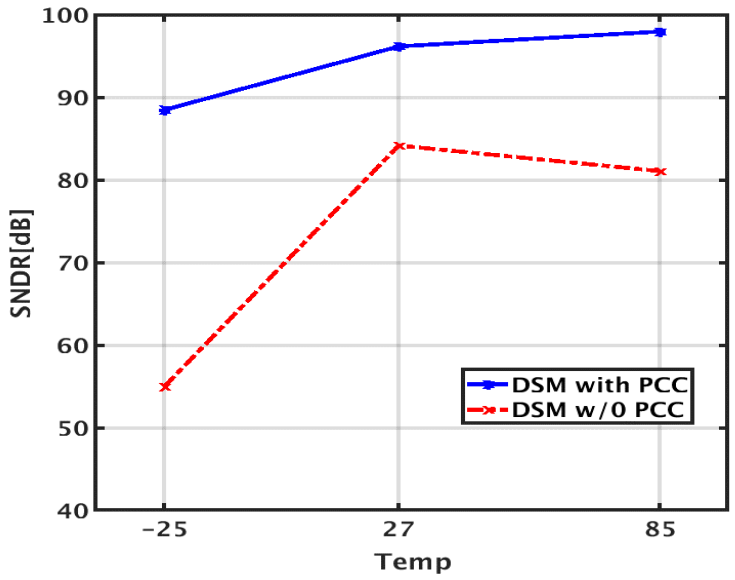

Fig.4.9: SNDR vs input amplitude with and without proposed charge compensation scheme. 

third harmonic (HD3), and an overall SNDR improvement of more than 12 dB compared to the conventional implementation. Fig. 4.9 shows the SNDR vs. input signal amplitude curve. The modulator with charge compensation achieves a peak SNDR of 95.6 dB, whereas that for the conventional DSM it is only 90 dB. Also the

performance of conventional DSM degrades significantly at the larger input signal level compared to that of the charge-compensated DSM. At -6 dBFS input signal level, the SNDR of conventional DSM degrades by 12 dB compared to the charge-compensated DSM. Fig.4.10. (a) shows the simulated HD3 and SNDR versus first OTA current with and without charge compensation. The DSM with charge compensation technique can achieve the same performance as a conventional DSM with ~30% less current.




(a)




(b)

Fig.4.10: (a) SNDR vs OTA current (b) SNDR vs temperature

Fig. 4.10. (b) shows the SNDR at different temperatures. The bulk bias of the inverter OTA was turned off for the first OTA to verify the effectiveness of the charge compensation technique across temperature. There is only a 6 dB degradation in the overall SNDR of the second-order delta sigma ADC.

Table II : Performance comparison

| | **Conventional DSM** | **PCC based DSM** |
|---|---|---|
| Process (nm) | 65 | 65 |
| Supply (V) | 1.2 | 1.2 |
| Bandwidth (kHz) | 25 | 25 |
| SNDR (dB) | 76.2 | 91.4 |
| Power (μW) | 119 | 130 |
| $FOM_{S,SNDR}$ (dB) | 159.5 | 174.4 |

Fig. 4.11 illustrates the robustness of the proposed scheme to variations in the compensation capacitor $C_3$. Across a range of 2 pF change in $C_3$, the performance of the DSM degrades by less than 3dB.

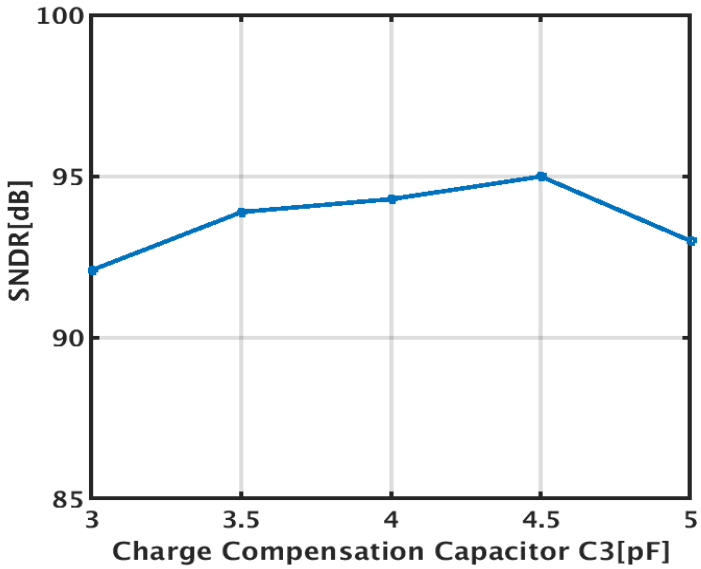



Fig.4.11: SNDR variation with value of charge compensation capacitor



The simulated DSM with the charge compensation technique consumes 105 μW (including static power as well as dynamic power used in charging of capacitors).

However, since the digital logic was not synthesized, the digital power was not included. The first integrator consumes 55 μW, while the second integrator and the comparator together consume 43 μW. The total power consumption of the ADC is 130 μW. Table II gives the performance comparison of second order DSM with and without charge compensation.

**4.5 Charge Compensation with Correlated Level Shifting (CC-CLS Integrator)**

In this section, we propose a circuit which combines the two performance enhancement techniques (a) passive charge compensation, and (b) Correlated Level Shifting, without increasing the hardware cost. It can take on several forms, but the basic principle is the same. It rearranges the slewing mitigation CC circuit in such a way that at the end of the charge transfer the feedback capacitor $C_2$ and the extra capacitor $C_3$ have equal voltages stored. Thus, they can be connected in series with opposite polarities, to reduce the amplifier's output voltage $V_0$ as in correlated level shifting.

The implementation of charge compensation with correlated level shifting (CC-CLS) is shown in Fig. 4.12. During S1, the sampling capacitor $C_1$ is reset, while charge compensation capacitor $C_3$ is connected to the input Vin. In the clock phase $S_2$ the charge proportional to the input is transferred to $C_2$ and $C_L$. As in the conventional CLS scheme, during the estimation phase $S_{2a}$ the bottom plate of $C_3$ is connected to the common mode voltage, and during $S_{2b}$ the bottom plate is connected to output of the OTA, performing level shifting operation and hence squaring the open loop gain of the OTA. The analysis of the operation of this stage is given in the Appendix.

These integrators are compared in the frequency domain, by simulating their periodic frequency characteristic, Fig. 4.13 (a), and on the time domain, by means of their step response, Fig. 4.13 (b). In both cases the amplifier was modelled as a single pole system with a differential open loop gain, $A_{OL}$, of 30 dB and a bandwidth of 40 MHz. A transconductance efficiency of 25 S/A was used to set the max slewing current. The value of $C_1$, $C_2$ and $C_L$ were 0.25 pF, 4 pF and 0.5 pF respectively, $C_3$ followed Eq. (4.4). The sampling frequency was 25.6 MHz, and a differential step of 1 V was used for the transient.

As shown in Fig. 4.13 (a) the gain of the proposed integrators matches that of the CLS one, showing a gain improvement of around 20dB. As explained in [20], the exact gain squaring (here, a 30 dB improvement) in the CLS circuit is not achieved because during the estimation and level-shifting phases the feedback factors change, due to the circuit being reconfigured. Moreover the relationship between both feedback factors can be shown to be

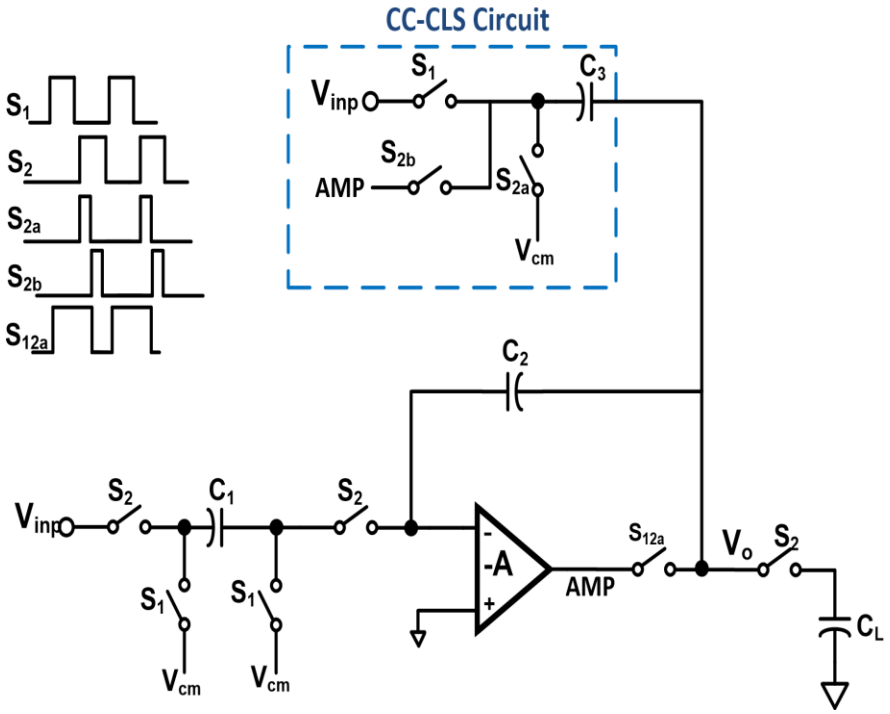



Fig. 4.12: CC-CLS integrator.



$$\beta_{EST} = \frac{C_2}{C_1+C_2}, \beta_{LS} = \frac{\beta_{EST}}{1+\frac{C_L+\beta_{EST}\cdot C_1}{C_3}} \qquad (4.8)$$

Here, $\beta_{LS}$ and $\beta_{EST}$ correspond to the level-shifting and estimation phase feedback factors, respectively. The total static gain [20] can be estimated as

$$Gain_{static} = (1+\beta_{EST}A_{OL})(1+\beta_{LS}A_{OL}) \qquad (4.9)$$

For the values chosen this yields a static gain of 49.5 dB, closely matching the simulated results. On the other hand, both the conventional and CC integrators track the open loop gain of the amplifier, as expected.

Fig. 4.13 (b) shows the transient response of the output voltages for a 1-V input differential step during phases $S_{2a}$ and $S_{2b}$. For a conventional integrator with infinite gain (ideal integrator) this should produce a 62.5 mV output.

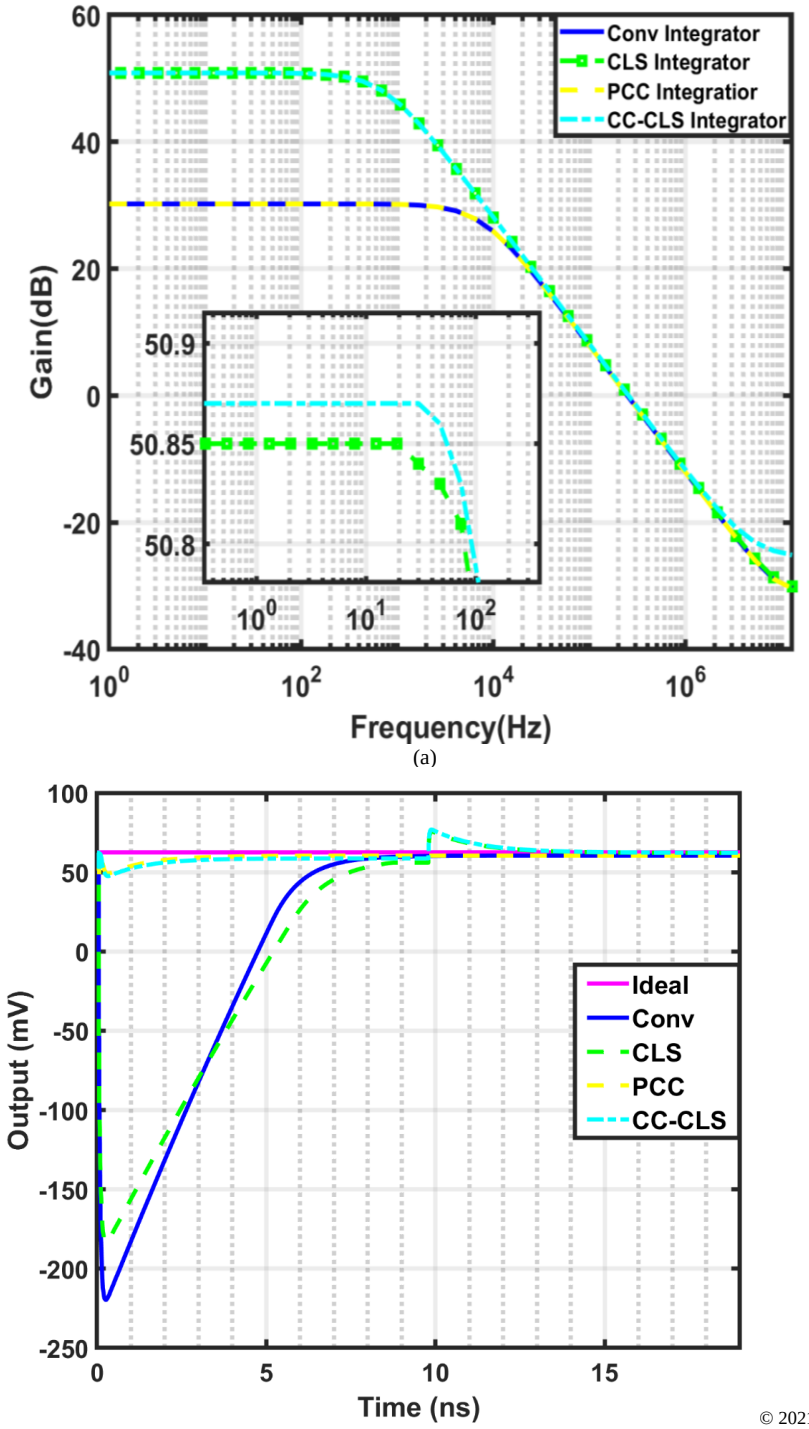





Fig. 4.13: Comparative performance of integrators (a) magnitude of periodic frequeAncy response (b) step response with total relative error.

When $S_{2a}$ is enabled, it takes approximately 8 ns for the conventional (Conventional and CLS integrators to get into the 10mV error region, whereas those with the CC

mechanism are well inside that region much earlier. Between 10 ns to 19 ns, during phase $S_{2b}$, the integrators CLS and CC-CLS are re-configured for level-shifting, producing a voltage jump that settles to an error less than -30 dB. The proposed CC-CLS integrator reaches the -50-dB error level, matching the periodic frequency response simulation. On the other hand, the CLS-only integrator reaches about -46 dB, which is 4 dB below the expected behaviour predicted by Fig. 4.13 (a). This difference can be explained by the limited slew-rate of the CLS integrator during phase $S_{2a}$, which is not accounted for in the periodic frequency response analysis. This reduces the available settling time, hence degrading the achievable error level.

### 4.5.1 SECOND-ORDER DELTA-SIGMA ADC

The design of power-efficient switched-capacitor delta sigma ADCs becomes challenging when the sampling frequency increases to several tens of MHz's. First, the GBW of the OTA used in the first integrator needs to be, roughly, more than seven times the sampling frequency, to settle the output to an accuracy of more than 14 bits. Since the GBW is proportional to the transconductance, which in turn is proportional to the static current, a higher sampling frequency requires a power-hungry OTA. A second factor that degrades efficiency is the use of single bit quantizers. Then, the feedback DAC output swings between $\pm V_{ref}$, and the first integrator must have a sufficiently large slewing current to deal with it. Though using multi-bit quantizers reduces the voltage swing, it increases complexity with additional digital circuitry required to mitigate the DAC nonlinearity. An alternative solution is to use a finite impulse response (FIR) DAC [11] with single bit quantizer. However, this introduces additional delay in the loop which needs to be compensated. The proposed CC-CLS integrator mitigates the slewing of the OTA and provides gain squaring. Hence, by using a CC-CLS integrator in the first stage of delta-sigma ADC, significant power can be saved without reducing the performance. Fig. 4.14 shows the circuit implementation of a discrete time second-order delta-sigma ADC with a CC-CLS integrator. The auxiliary path with CC-CLS circuit consist of an auxiliary DAC and the input signal path. The second integrator is implemented in a conventional way, i.e. with no charge compensation branch, as it does not have high linearity requirements.

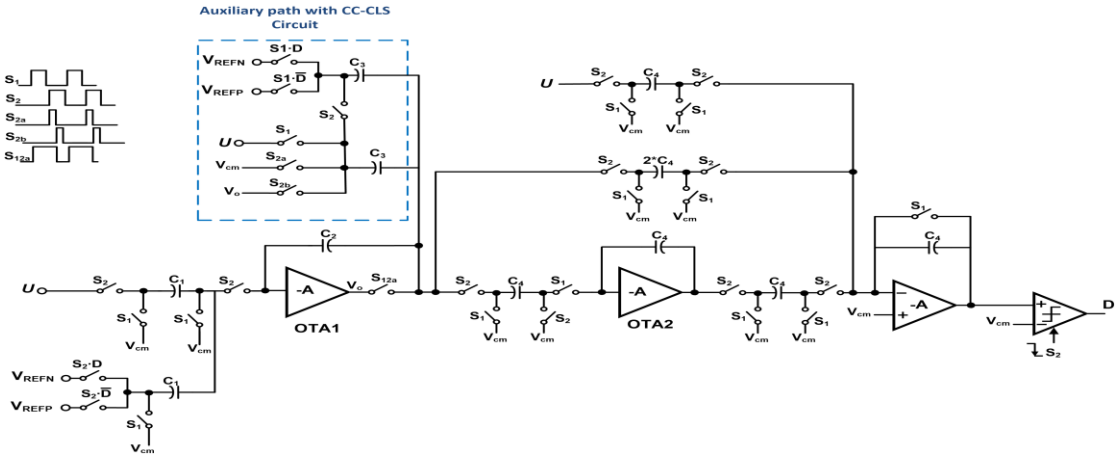





Fig. 4.14 Second order delta-sigma ADC with the charge compensated level shifting (CC-CLS) integrator

### 4.5.2 Simulation results

The performance of the CC-CLS integrator was verified by using it in the second-order delta-sigma ADC shown in Fig. 4.14. Single-ended circuitry is shown for simplicity, but the implementation is fully differential. An OTA with finite gain of 30 dB, finite bandwidth of 80 MHz modelled was used in the simulation. The second-order delta-sigma ADC was implemented with a sampling capacitor $C_1$ = 2 pF, an integrating capacitor $C_2$ = 4 pF, load capacitance $C_L$=0.5 pF and a charge compensation capacitor $C_3$ = 4.5 pF. The signal bandwidth was 50 kHz, and the sampling frequency was 25.6 MHz, for an oversampling ratio of 256. The simulated output power spectral densities (PSDs) of the ADC with three different input integrators: using a low $g_m$ OTA

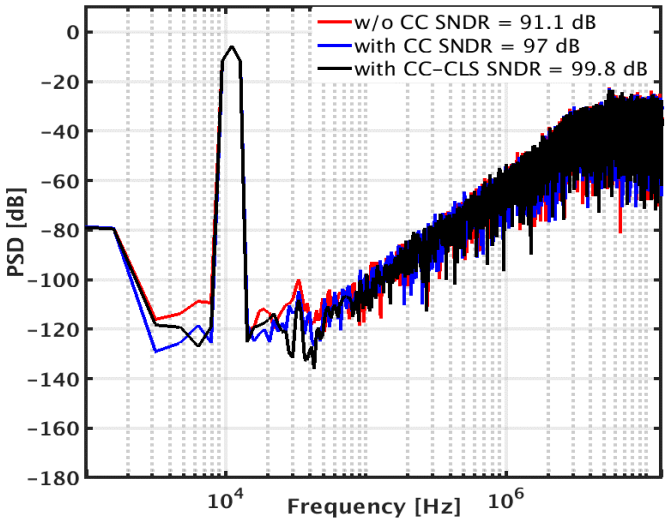



Fig. 4.15 PSD of delta sigma ADC with and without charge compensated first integrator and CC-CLS integrator. 

without charge compensation, with charge compensation and with CC-CLS technique are shown in Fig. 4.15. The input signal frequency was 10.4 kHz. The transient noise simulation results show a 9-dB improvement in SNDR for the ADC using the CC-CLS integrator, compared to the conventional integrator, and 3 dB compared to the CC one.

# Chapter 5. Conclusion

Switched capacitor (SC) circuits are the main building blocks in many structures such as filters, data converters, sampling circuits and sampled-data amplifiers. The key challenge is to design such circuits which are the prime components of any IoT system with low power consumption without compromising on the performance. This research investigated new switched capacitor techniques to reduce the DC offset, flicker noise and mitigate the slewing in switched capacitor-based Analog to Digital Converters (ADC).

*First*, a two-step incremental ADC(IADC) with pseudo-pseudo differential (PPD) structure was presented. The PPD integrator filters out DC offset and low frequency noise and also supresses even harmonics. A PPD integrator is implemented with correlated level shifting technique to further improve the linearity of opamp. The PPD two-step IADC was implemented, with the first step configured as a single-bit first-order IADC and the second step, using a two-capacitor SAR-assisted extended counting to enhances the accuracy. This design prototype is demonstrated by simulations assuming 65nm CMOS technology.

*Second*, several new passive charge compensation techniques were presented. The proposed techniques mitigate slewing in the OTA by providing a controlled amount of charge to the output of the OTA. The effectiveness of the proposed charge compensation technique in a switched-capacitor integrator is demonstrated using a second-order Delta-Sigma modulator. Further, passive charge compensation is reconfigured to perform correlated level shifting operation and hence lower the distortion.

# Appendix A

## Analysis of the Charge provided by Charge Compensation Circuit:

The charge-compensated integrator from Fig. 4.2 (a) is re-drawn in Fig.A.1, showing the specific charge flow through each capacitor. In the following derivation, the OTA is considered to be ideal. Two non-overlapping clock phases $S_1$ and $S_2$, are assumed, each with a period of $T_S$ and a phase difference of $T_S/2$. $S_2$ is identified with index *n* and with index *n-1/2.*

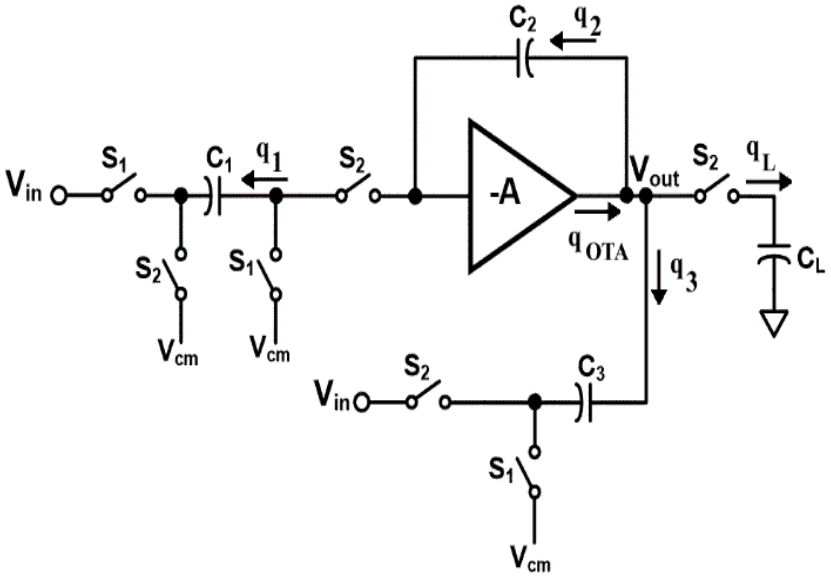



Fig.A.1. Charge compensated integrator with charge flow convention.



During phase S2 the charge flowing through $C_1$, $q_1(n)$, is equal to the one through $C_2$, $q_2(n)$. Besides, due to negative feedback the bottom plate of $C_2$ is connected to a virtual ground node, allowing for the following relations between $q_1$, $q_2$, $V_{out}$ and $V_{in}$.

$$q_2(n) = q_1(n) \qquad \text{(A1)}$$

$$q_1(n) = C_1\left[(0-0) - \left(0 - V_{in}\left(n-\frac{1}{2}\right)\right)\right] \qquad \text{(A2)}$$

$$= C_1 V_{in}\left(n-\frac{1}{2}\right)$$

$$q_2(n) = C_1\left[(V_{out}(n) - 0) - \left(V_{out}\left(n - \frac{1}{2}\right) - 0\right)\right] \quad \text{(A3)}$$
$$= C_1\left[V_{out}(n) - V_{out}\left(n - \tfrac{1}{2}\right)\right]$$

In addition, during phase $S_1$ no charge flows through $C_2$, therefore

$$0 = q_2\left(n - \frac{1}{2}\right) = C_1\left[\left(V_{out}\left(n - \frac{1}{2}\right) - 0\right) - (V_{out}(n-1) - 0)\right] \quad \text{(A4)}$$

Solving, yields

$$V_{out}\left(n - \frac{1}{2}\right) = V_{out}(n-1) \quad \text{(A5)}$$

This can be replaced in (3), and equated with (2), in order to relate $V_{out}$ and $V_{in}$, obtaining

$$V_{out}(n) - V_{out}(n-1) = \left(\frac{C_1}{C_2}\right)V_{in}\left(n - \frac{1}{2}\right) \quad \text{(A6)}$$

Which corresponds to the delayed integrator or discrete time accumulator. Conversely, due to (5),

$$V_{out}(n) - V_{out}\left(n - \frac{1}{2}\right) = \left(\frac{C_1}{C_2}\right)V_{in}\left(n - \frac{1}{2}\right) \quad \text{(A7)}$$

Finding the charge flow through capacitor $C_L$

$$q_L(n) = C_L\left[(V_{out}(n) - 0) - \left(V_{out}\left(n - \frac{1}{2}\right) - 0\right)\right] \quad \text{(A8)}$$
$$= C_L\left[V_{out}(n) - V_{out}\left(n - \frac{1}{2}\right)\right]$$

Replacing the second factor on the right-hand side for (A7) yields the charge in terms of the input

$$q_L(n) = C_L\left(\frac{C_1}{C_2}\right)V_{in}\left(n-\frac{1}{2}\right) \qquad \text{(A9)}$$

Similarly, the charge flow through $C_3$, can be expressed as

$$\begin{aligned} q_3(n) &= C_3\left[\left(V_{out}(n) - V_{in}(n)\right)\right. \\ &\qquad \left. - \left(V_{out}\left(n-\frac{1}{2}\right) - 0\right)\right] \\ &= C_3\left(V_{out}(n) - V_{out}\left(n-\frac{1}{2}\right)\right) \\ &\qquad - C_3 V_{in}(n) \end{aligned} \qquad \text{(A10)}$$

Which, again, can be expressed in terms of the input using (A7)

$$\begin{aligned} q_3(n) = C_3\left[\left(\frac{C_1}{C_2}\right)V_{in}\left(n-\frac{1}{2}\right)\right. \\ \left. - V_{in}(n)\right] \end{aligned} \qquad \text{(A11)}$$

The charge provided by the OTA has to match those of $q_L$, $q_3$ and $q_2$, so

$$q_{OTA}(n) = q_L(n) + q_3(n) + q_2(n) \qquad \text{(A12)}$$

Replacing (A7), (A10) and (A3), and rearranging

$$\begin{aligned} q_{OTA}(n) = \Big[C_1 \\ + (C_3 \\ + C_L)\left(\frac{C_1}{C_2}\right)\Big]V_{in}\left(n-\frac{1}{2}\right) \\ - C_3 V_{in}(n) \end{aligned} \qquad \text{(A13)}$$

Assuming that $V_{in}\left(n-\frac{1}{2}\right) \approx V_{in}(n)$

$$\begin{aligned} q_{OTA}(n) = \left\{\left[C_1 + (C_3 + C_L)\left(\frac{C_1}{C_2}\right)\right]\right. \\ \left. - C_3\right\}V_{in}(n) \end{aligned} \qquad \text{(A14)}$$

Applying the z-transform to both sides yields

$$Q_{OTA}(z) = \left\{\left[C_1 + (C_3 + C_L)\left(\frac{C_1}{C_2}\right)\right] - C_3\right\} V_{in}(z) \quad \text{(A15)}$$

Solving for the $C_3$ that makes $Q_{OTA}(z) = 0$ results in

$$C_3 = C_1 \frac{1 + \left(\frac{C_L}{C_2}\right)}{1 - \left(\frac{C_1}{C_2}\right)} \quad \text{(A16)}$$

Since this $C_3$ was obtained after an approximation, the actual value of $q_{OTA}$ is not exactly zero, therefore (13) is re-calculated, considering the $C_3$ found in (16), which results in

$$q_{OTA}(n) = -C_3 \left[V_{in}(n) - V_{in}\left(n - \frac{1}{2}\right)\right] \quad \text{(A17)}$$

And in the z-domain

$$Q_{OTA}(z) = -V_{in}(z) \cdot C_3 \left(1 - z^{-\frac{1}{2}}\right) \quad \text{(A18)}$$

Evaluating $z = e^{j\omega T_s}$ to obtain the frequency response of the magnitude,

$$\left|\frac{Q_{OTA}}{V_{in}}\right|(\omega) = C_3 \left|1 - e^{-\frac{j\omega T}{2}}\right| \quad \text{(A19)}$$

Considering an oversampled system with bandwidth, *BW*, and sampling frequency, $F_S = 1/T_S$, the oversampling ratio, *OSR*, can be defined as $OSR = \frac{F_S}{2 \cdot BW}$. Evaluating (A19) at the bandwidth of the system yields

$$\left|\frac{Q_{OTA,PCC}}{V_{in}}\right|(2\pi \cdot BW) = C_3 \left|1 - e^{-j2\pi \cdot BW \cdot T_s/2}\right| \quad \text{(A20)}$$

$$= C_3 \left|1 - e^{-\frac{j \cdot \pi}{2 \cdot OSR}}\right| \approx C_3 \frac{\pi}{2 \cdot OSR}$$

The last approximation in (A20), holds when $OSR \gg \frac{\pi}{4} \approx 0.78$ which is always met in oversampled systems.

For the conventional integrator of Fig. 2.5 the charge required from the OTA is

$$q_{OTA,conv}(n) = C_{LTOT}\left(V_{out}(n) - V_{out}(n-1)\right) \quad \text{(A21)}$$

Which can be expressed in terms of the input as

$$q_{OTA,conv}(n) = C_{LTOT}\,\frac{C_1}{C_2}V_{in}\left(n-\frac{1}{2}\right) \quad \text{(A22)}$$

And the frequency response can be expressed as:

$$\left|\frac{Q_{OTA,conv}}{V_{in}}\right|(\omega) = C_{LTOT}\,\frac{C_1}{C_2} \quad \text{(A23)}$$

Comparing (A20) and (A23) it can be seen that the charge demanded to the OTA in a PCC system can be relaxed by increasing OSR, whereas it is independent of OSR in the conventional case.

# Appendix B

## Analysis of finite gain for CC-CLS Integrator

The static errors introduced into the CC-CLS integrator by the finite gain of the amplifier will be estimated next. Assuming A >> 1, and analyzing the circuit of Fig. B.1, the voltages across the capacitors can be found. The results are

*$S_1$ = 1, clock period n – 1*

$$V_{c1} = 0,$$

$$V_{c2} = -(1 + 1/A)\, V_o(n - 1),$$

$$V_{c3} = V_o(n - 1) - V_{in}(n - 1)$$

*$S_{2a}$ = 1, clock period n – ¾*

$$V_{c1} = V_{in}(n - ¾) + V_o(n - ¾)/A \ ,$$

$$V_{c2} = -(1 + 1/A)\, V_o(n - 3/4),$$

$$V_{c3} = V_o(n - 3/4)$$

The finite gain A thus causes an error charge $C_1V_o(n - ¾)/A$ in $C_1$, and a voltage error $(C1/C_2).Vo(n - ¾)/A$ in $V_{out}$.

*$S_{2b}$ = 1, clock period n – ½*

$$V_o(n - ½) \sim V_{c2}(n - ¾) + V_{c3}(n - ¾) \sim -V_o(n - 3/4)/A$$

$$V_{c1}(n - ½) = V_{in}(n - 1/2) + V_o(n - ½)/A = V_{in}(n - ½) - V_o(n - 3/4)/A^2$$

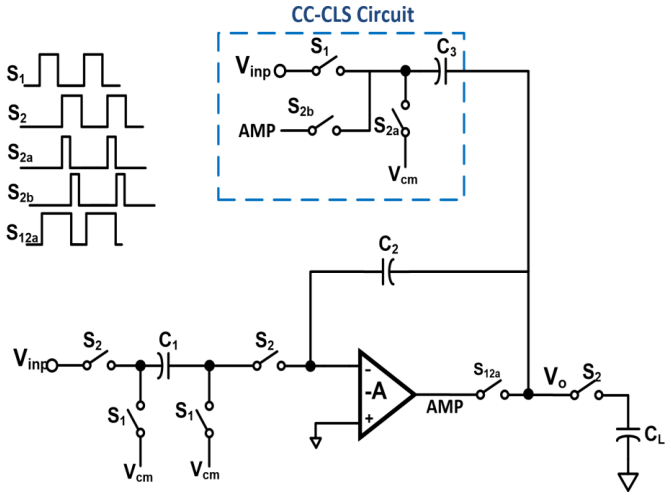



Fig. B.1 CC-CLS integrator

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