AN ABSTRACT OF THE THESIS OF

Soumya Gupta for the degree of Master of Science in Electrical and Computer Engineering presented on December 2, 2021.

Title: Millimeter-Wave Wideband Low-Noise Amplifiers in 22FFL Technology.

Abstract approved: _____

Arun Natarajan

The deployment of advanced technology standards for 5G and beyond in cellular networks has resulted in interest in integrated circuits (ICs) operating at frequencies above 10GHz. This has sparked research on wideband circuits in commercial low-cost silicon technologies, operating at high RF and mm-wave frequencies [1-3]. Given the wide range of operating frequencies (28GHz, 30GHz and 47GHz), such circuits must satisfy performance parameters across wide operating range. This thesis focuses on the implementation of wideband low-noise amplifiers (LNA) and addresses design challenges associated with mm-wave wideband impedance matching networks in state-of-the-art CMOS technologies.

Verifying the design methodology, two chips have been fabricated in 22nm FFL technology. The first chip, occupying 1.5x1.5 mm^2, comprises of an amplifier with single ended in-phase and quadrature output paths, each capable of driving a 50Ω load. Post-layout simulations indicate a peak gain of 19.8dB, a minimum noise figure of 2.7dB, with an input and output return loss of less than 8dB and 5dB, respectively, between 21GHz to 48GHz. The second chip is a receiver design, that combines a wideband low-noise amplifier with a sub-harmonic mixer. The amplifier in this case provides differential in-phase and quadrature output paths, capable of driving 150Ω resistive input impedance of mixer. This receiver design occupies a die area of 2x2mm^2.

Both amplifiers achieve a fractional bandwidth of 80 percent while consuming 33.4mW of power from a 1V supply.

Millimeter-Wave Wideband Low-Noise Amplifiers in 22FFL Technology

by
Soumya Gupta

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented December 2, 2021
Commencement June 2022

Master of Science thesis of Soumya Gupta presented on December 2, 2021

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Soumya Gupta, Author

ACKNOWLEDGEMENTS

I am extremely grateful to my advisor, Prof. Arun Natarajan, for giving me an opportunity to be a part of his research group. I joined the team without any design experience, and Prof. Arun and his team have been teaching me everything along the way, from basic concepts of designing to abilities of critical thinking. His passion for research has continuously inspired me and I feel fortunate to be his student. I feel elated about completing my masters research and extremely excited for the oncoming journey of doctoral research.

I would like to express my sincere gratitude to Prof. David Allstot. The support he has extended towards my learnings at Oregon State University will remain unparalleled. His life lessons and valuable words have motivated me in my research and career choices. I would like to thank Prof. Tom Weller, Prof. Matthew Johnston, and Prof. Serkan Ates for serving on my committee and helping me improve the quality of my research through their valuable feedbacks.

The courses I have studied at Oregon State University have helped me build a strong foundation for my research. I will always be grateful to Prof. Mario E. Magaña, Prof. Un-Ku Moon, Prof. Gabor Temes, Prof. Arun Natarajan, and Prof. Larry Cheng for offering these wonderful courses.

Every member of High-Speed Integrated Circuits (HSIC) group, directed by Prof. Arun Natarajan, has supported me throughout this journey and I feel honored to be working with them.

I am highly indebted to my partner Manjunath, whose love and encouragement has been the driving force behind this thesis. Last and most important, my mother who made this journey possible. Her unconditional love has been an inspiration and I dedicate this thesis to her.

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Chapter 1

INTRODUCTION

With decades of advancement in communication systems and silicon technologies, wireless communication has become a prominent part of daily life [4]. The cellular networks of today have become highly multi-purpose, with hand-held devices capable of providing access to emails, video streaming, location tracking, and access to the internet. In 2020, the estimated number of mobile device users were 6.95 billion and this number is expected to increase by 0.5 billion in the next five years, as can be seen in Fig. 1.1 [5].

The widespread use of wireless data transfer has motivated demand for higher data rates. This in turn has led to a move towards mm-wave carrier frequencies that have wide available bandwidths. However, enabling access to mm-wave spectrum at low-cost requires development of wideband mm-wave integrated circuits in low-cost commercial silicon technologies [6]. This chapter provides a brief summary of wireless system fundamentals and motivates the necessity of wideband integrated circuits at frequencies beyond 20 GHz.

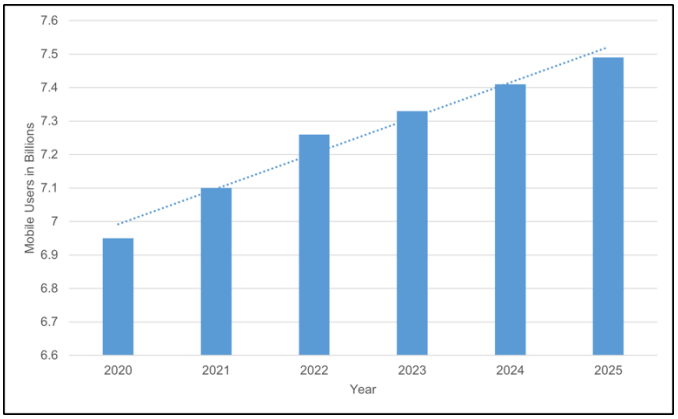


Fig. 1.1. Increment in demand for cellular devices

1.1 Wireless Communication

Every day, we encounter devices utilizing wireless applications such as Global Position System (GPS), Wi-Fi, Bluetooth, and Radio Frequency Identification (RFIDs). While all these applications operate at specific carrier frequencies, the underlying wireless communication fundamentals remain the same for all these applications.

Wireless communication enables transferring of data from source to destination without any physical medium between them. This communication method involves the use of radio waves, and the propagation of signals takes place through space. Though wireless systems are cost-efficient, mobile, easy to install, and reliable, factors such as reliability, security, interference, and health concerns require utmost attention [7].

A wireless system, in general, constitutes three basic elements: antennas, transmitters (TX) and receivers (RX).

An antenna acts as the interface between the radio waves propagating through space and the transmitter/receiver. The functionality of processing the baseband input signal, and propagating it through space is performed by the transmitter, whereas the receiver collects signals from space and processes it to generate the baseband output signal. A block diagram depicting this flow of information is given in Fig.1.2.

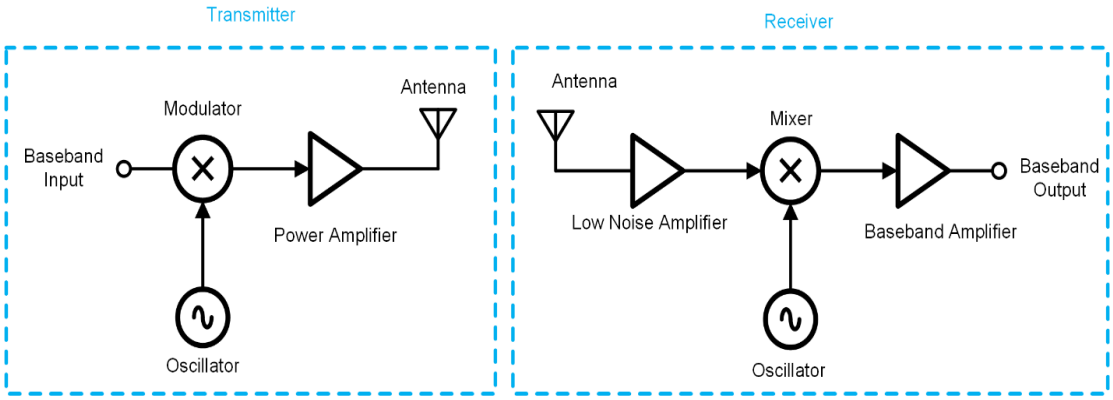


Fig. 1.2. Block diagram of a wireless communication system

The implementation of these wireless systems on silicon involves a more sophisticated arrangement, than the one shown in Fig.1.2. An overall system involves integration of circuits with various functionalities, ranging from oscillators, mixers, power/low-noise

amplifiers to phase-shifters, dividers, and antennas. A representation for such a system is provided in Fig. 1.3 [8].

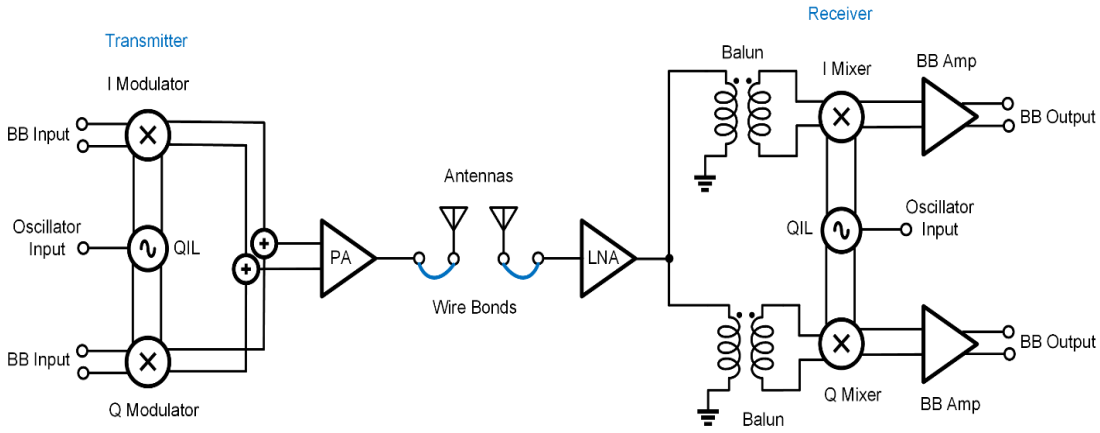


Fig. 1.3. A sophisticated presentation of wireless system

From a system-design perspective, on the transmitter side, the power amplifier (PA) must ensure an output signal with minimal distortion due to non-linearities in the signal path. The quadrature oscillator (QIL) should provide quadrature signals, for in-phase (I) and quadrature (Q) paths, which would then perform the up-conversion of the input signal. On the receiver side, the low-noise amplifier (LNA) plays a major role in determining the signal-to-noise ratio in the system, and hence the LNA must have high gain, low noise, and linear performance. Similar to the transmitter case, the quadrature oscillator should generate quadrature signals; in this case to down-convert the I and Q signals. At the end of the RX signal chain, baseband amplifiers must provide an additional amplitude boost.

The objective of implementing such a wireless system over a wide bandwidth poses various challenges. All transmit and receive circuits have to be wideband, maintaining their core performance metrics, such as gain, linearity, and matching across the entire operating frequency range. Consequently, compared to narrowband systems, additional wideband-specific active and passive circuits are needed in order to achieve wideband operation at the system level.

1.2 Design Technology

Traditionally, III-V compound semiconductors (GaAs and InP), due to their attractive noise and linearity performance, have been used for implementing millimeter-wave front-end ICs. Over the last two decades, there have been efforts to implement such systems in

complementary metal-oxide semiconductor (CMOS) technology and SiGe technology. Leveraging the silicon infrastructure developed for digital systems, such implementations can lead to high yields, higher levels of integrations, and lower costs, broadening potential applications

Such high-performance CMOS front ends have been demonstrated in the literature, serving applications in the GHz range, and researchers are putting considerable efforts into achieving ultra-wideband front ends to meet growing 5G demands [8-10].

A more recent development has been the emergence of FinFET technology that offers advantages compared to MOSFETs [11]. While providing integration and scalability of CMOS, FinFETs also provide lower leakage current and increased voltage gain.

1.3 Motivation for LNA Design

The components of a receiver chain and their independent functionality has been discussed in Section 1.1. As shown in Figure 1.3, the LNA is the first functional block in the RX following the antenna. Therefore, LNA determines multiple system performance specifications, importantly noise, sensitivity, and linearity. To ensure optimum power performance in the receiver, the input section of LNA must be efficiently matched to the antenna impedance. Wide bandwidth operation must be ensured for all performance parameters, such as noise, gain, matching, and linearity.

Given the criticality of the LNA for receiver performance, exploring wideband LNA implementations at mm-wave is a topic of interest for this thesis.

1.4 Summary of Contribution

The contribution of this research can be summarized as follows:

- Millimetre-wave LNA with low noise figure and wideband performance is proposed.
- The concept of utilizing mutually coupled inductors in wideband network designs is explored.
- The impact of layout optimization on the device's gate resistance and noise figure is discussed.

- Two LNA designs, one with single-ended outputs and the other with differential outputs, are presented.

1.5 Organization

An overview of LNA design goals, with the contribution of design parameters on overall performance, has been provided in Chapter 2, Section 2.1. A detailed discussion of the impact of coupled resonant tanks on bandwidth expansion has been given in Section 2.2. Matching networks critical to optimum gain and power performance covers Section 2.3, whereas Section 2.4 discusses noise suppression techniques to improve the amplifier noise contributions. All these discussions have been supported with relevant circuit representations and design equations.

Chapter 3 covers the proposed LNA topology which is presented in Section 3.1. The following sections provide design techniques deployed for implementing LNAs in this work, with the device selection method described in Section 3.2. The modified cascode structure, achieving reduced noise over the conventional cascade is described in Section 3.3. Supporting simulation results have been provided herein. The concepts explored for attaining wideband performances in both the amplifier versions have been covered in Section 3.4 and Section 3.5. Section 3.6 summarizes the overall design methodology for LNA implementation.

Layout designs along with optimization techniques with the simulated noise performance of different layout designs have been discussed in Chapter 4. Section 4.1 contains the layout design of every stage and presents the post-layout results for both versions of the amplifier. The impact of layout optimization on the noise figure of the device has been discussed through simulations, in Section 4.2. EM-simulation-based models of transformers, inductors, and transmission lines, with their quality factors, are included in Section 4.3.

Chapter 5 summarizes the work performed as part of this thesis, presenting conclusions and future avenues of research.

Chapter 2

LITERATURE REVIEW

This chapter introduces the design of the LNA, while providing an overview of its design goals. Concepts that are critical to wideband circuit implementations, such as dual resonance, and impedance match, are discussed. Finally, the use of wideband techniques in LNA design is explored.

2.1 Design Goals for LNA

A system is usually characterized by a figure of merit (FoM) that enables comparison across different approaches by balancing different performance trade-offs. A commonly-used FoM for LNA, involving gain (*G*), linearity (*IIP3*), noise factor (*F*), bandwidth (f_{BW}), and power (*P*), can be given by (2.1) [12].

$$FoM_{LNA} = \frac{G \times IIP3 \times f_{BW}}{(F-1) \times P} \tag{2.1}$$

This FoM captures these trade-offs across performance metrics and highlights that higher gain, better linearity, wide bandwidth, low noise, and low power are desirable for LNA. Each contributing factor is discussed in this section and their impact on overall system performance is assessed [13].

2.1.1 Frequency of Operation

High data throughput has been a major objective for wireless communication systems, as discussed in Section 1. Shannon's theorem describes the relationship between bandwidth (*BW*), signal-to-noise ratio (*SNR*) and data rate (*C*), which is given in (2.2).

$$C = BW \times log_2(1 + SNR) \tag{2.2}$$

This indicates that to design a high-speed system it is very critical to achieve a wideband performance. The fractional bandwidth of a system is defined as the ratio of absolute bandwidth to center frequency. Typically, it is challenging to attain a high fractional bandwidth, and hence designing a wideband network at sub-GHz frequency

is particularly challenging. On the other hand, achieving the same absolute bandwidth at mm-wave frequencies requires a smaller fractional bandwidth due to the higher center frequency, potentially simplifying the design.

On the other hand, path losses for wireless propagation and transistor performance, such as gain and noise figure, degrades with higher operating frequencies. Therefore, though a lower fractional bandwidth reduces design complexity, higher operating frequencies impact noise and gain and hence pose a significant design challenge.

2.1.2 Noise Factor and Gain

In the case of the LNA, the noise factor (F) is the most critical design specification for an amplifier. It is defined as the ratio of SNR at the input to SNR at the output of an amplifier. When computed on a logarithmic scale, the noise factor is referred to as noise figure (NF), as given in equations (2.3) and (2.4).

$$F = \frac{SNR_i}{SNR_o} \tag{2.3}$$

$$NF = 10 \times log_{10}(F) \tag{2.4}$$

Noise factor captures the noise added by the system to the input noise power. The design goal for the LNA is to reduce the added noise so that the system can achieve high sensitivity. Since the LNA is the first block following the antenna in the RX, the noise and gain it offers directly determines the sensitivity of the system. High gain in the LNA can minimize the noise contribution of subsequent blocks. This system functionality can be analyzed based on Fig. 2.1, where F_{LNA} is the noise factor of LNA, G_{LNA} is the gain of LNA, F_{MIXER} is the noise factor of mixer, G_{MIXER} is the gain of mixer, $F_{BB,AMP}$ is the noise factor of baseband amplifier, and $G_{BB,AMP}$ is the gain of baseband amplifier.

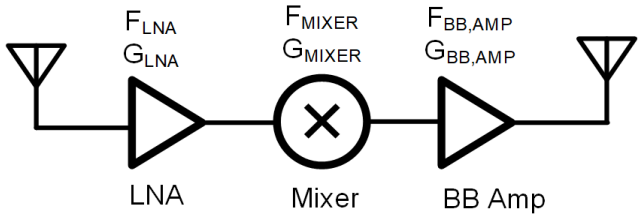


Fig. 2.1. Receiver chain for noise analysis

The overall noise factor of the RX is represented by (2.5).

$$F = F_{LNA} + \frac{F_{MIXER} - 1}{G_{LNA}} + \frac{F_{BB,AMP} - 1}{G_{LNA} G_{MIXER}} \tag{2.5}$$

It is evident that if LNA provides high gain then noise contribution of mixer and baseband amplifier can be reduced. Additionally, if noise contribution of LNA itself is reduced, then system overall can achieve a low noise factor and hence excellent sensitivity.

2.1.3 Linearity and Power

Amplifiers suffer from gain compression which results in intermodulation distortion. Third-order intermodulation distortion is most critical as the intermodulation products lie within the desired signal band. This directly impacts system sensitivity and can cause signal distortion.

The performance metric which accounts for third-order intermodulation distortion is the third-order input intercept point (IIP3). The non-linearities in the amplifier result in the generation of intermodulation products in addition to the desired output signal. The effect of this can be observed by defining the input signal power at which the extrapolated fundamental and third-order intermodulation (IM3) powers intercept. This can be observed through a two-tone test as well, whereby two sinusoids of the same amplitude are applied to the input of the amplifier. This idea is well explained in Fig. 2.2.

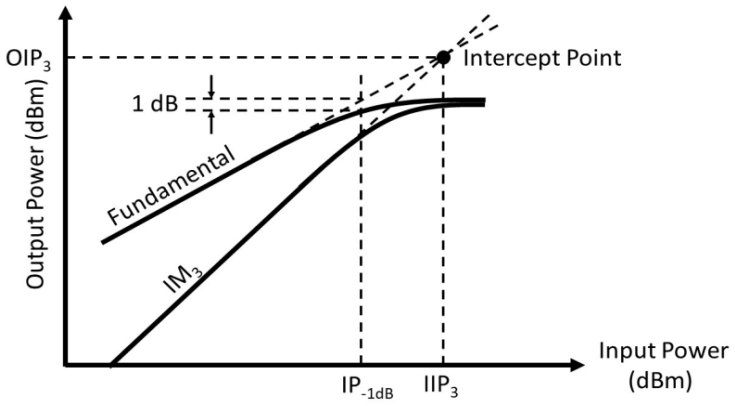


Fig. 2.2. Third-order intercept points and 1-dB compression point [13]

Linearity can also be assessed through 1-dB gain compression point (P_{-1dB}). Amplifiers exhibit output power saturation with increasing input power, which translates to lower gain for higher input powers. Input-referred P_{-1dB} is the input power at which amplifier gain is reduced by 1dB, as shown in Fig. 2.2.

Amplifier linearity can be improved by increasing overdrive voltages and supply voltages to increase headroom. However, this typically comes at the cost of higher power consumption. Linearity and power consumption trade-offs are typically application-specific and both performance metrics must be balanced to achieve desired system objectives.

2.2 Bandwidth Characterization with Double-Tuned Circuits

In a typical tuned amplifier, with parallel RLC resonant network loads (2^{nd} order networks), the center frequency (f) and bandwidth (Δf) define the fractional bandwidth of the amplifier, as given by (2.6).

$$f_{Bw} = \frac{\Delta f}{f} \tag{2.6}$$

Traditionally, such RLC networks with one resonant frequency are narrow band. There are several ways of expanding the bandwidth of a parallel RLC circuit, for instance, the quality factor (Q) of load can be reduced, (as shown in (2.7)), but this impacts other design parameters such as gain and noise, and therefore, only Q as the design degree of freedom is insufficient.

$$Q = \frac{f_0}{BW} \tag{2.7}$$

Where f_0 is the resonant frequency and BW is the bandwidth of RLC network.

An efficient way to broaden the frequency range of operation is to utilize transformers which provide dual-resonance. Such networks are equivalent to coupled parallel RLC loads, and such coupling can be attained electrically, magnetically or through a combination of electric and magnetic coupling [14]. Using similar concepts of coupling, a series-shunt LC design can also be employed for bandwidth extensions [15]. Interestingly, these designs also support impedance transformations and hence are a prominent part of matching networks.

The following section explains these wideband strategies through circuit representations and design equations.

2.2.1 Magnetically-Coupled Resonant Tanks

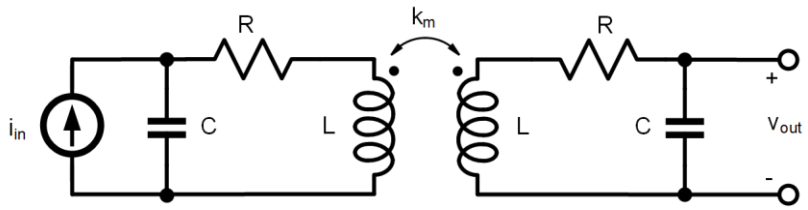


Fig. 2.3. Magnetically coupled resonant tanks

Two magnetically coupled resonant tanks are shown in Fig. 2.3 [14]. The series resistance, *R*, is for modelling the quality factor, *Q*, of the inductor coils. Using node-analysis, the trans-resistance of circuit can be given by (2.8).

$$|Z_{MC}(s)| = \frac{V_{out}}{I_{in}} = \frac{sk_mL}{[1 + sCR + s^2LC(1 - k_m)][1 + sCR + s^2LC(1 + k_m)]} \tag{2.8}$$

Equation (2.8) indicates that there are two resonant peaks, at ω_{n1} and ω_{n2}. The dependence of the frequency of the two resonant peaks on component values is provided in (2.9) and (2.10).

$$\omega_{n_1} = \frac{1}{\sqrt{L(1 - k_m)C}} \tag{2.9}$$

$$\omega_{n_2} = \frac{1}{\sqrt{L(1 + k_m)C}} \tag{2.10}$$

A simplified representation of the trans-resistance equation at these resonant frequencies can be stated as (2.11).

$$|Z_{MC}(j\omega)| = \frac{1}{2}\frac{L(1 \pm k_m)}{CR} \tag{2.11}$$

As seen by the equation, due to magnetic coupling the effective inductances seen at two resonant frequencies changes and the corresponding quality factors for these coils can be derived as (2.12) and (2.13).

$$Q_1 = \frac{\omega_{n_1} L(1-k_m)}{R} = \frac{1}{R}\sqrt{\frac{L(1-k_m)}{C}} \tag{2.12}$$

$$Q_2 = \frac{\omega_{n_2} L(1+k_m)}{R} = \frac{1}{R}\sqrt{\frac{L(1+k_m)}{C}} \tag{2.13}$$

Finally, the trans-resistance seen at the output of this network will be the parallel combination of two resistances, up transformed by the quality factors of the coils. This equivalent resistance is given by (2.14).

$$|Z_{MC}(j\omega)| = \frac{1}{2} Q_1^2 R \tag{2.14}$$

The magnetic coupling (k_m) between coils helps in achieving peak splitting which provides control over the bandwidth of the network. This type of networks suffers from the drawback of amplitude mismatch at two resonant peaks.

2.2.2 Electrically Coupled Resonant Tanks

The equivalent circuit for electrically coupled tanks is shown in Fig. 2.4 [14]. The trans-resistance of this network is given by (2.15).

$$|Z_{CC}(s)| = \frac{1}{2} \frac{sC_c(sL+R)^2}{[s^2L(C_C+C)+sR(C_C+C)+1][s^2LC+sRC+1]} \tag{2.15}$$

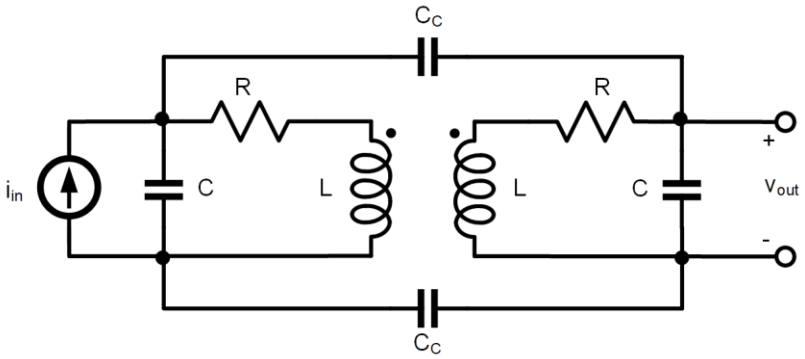


Fig. 2.4. Electrically coupled resonant tanks

The coupling capacitor (C_C) has the ability of shifting one of the resonant peaks, unlike the magnetically coupled tanks where coupling coefficients shift the location of both resonant peaks. The values of resonant frequencies and quality factors for both coils can be derived as (2.16) - (2.19).

$$\omega_{n_1} = \frac{1}{\sqrt{LC}} \tag{2.16}$$

$$\omega_{n_2} = \frac{1}{\sqrt{L(C + C_C)}} \tag{2.17}$$

$$Q_1 = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{2.18}$$

$$Q_2 = \frac{1}{R}\sqrt{\frac{L}{C + C_C}} \tag{2.19}$$

The equivalent trans-resistance in this case will be different at the two resonant peaks. They can be mathematically presented as (2.20) and (2.21).

$$|Z_{CC}(j\omega_{n1})| = \frac{1}{2}Q_1^2 R \tag{2.20}$$

$$|Z_{CC}(j\omega_{n2})| = \frac{1}{2}Q_2^2 R \tag{2.21}$$

Similar to magnetically-coupled tanks, there is an amplitude mismatch at two resonant frequencies.

2.2.3 Gain-Equalized Transformers

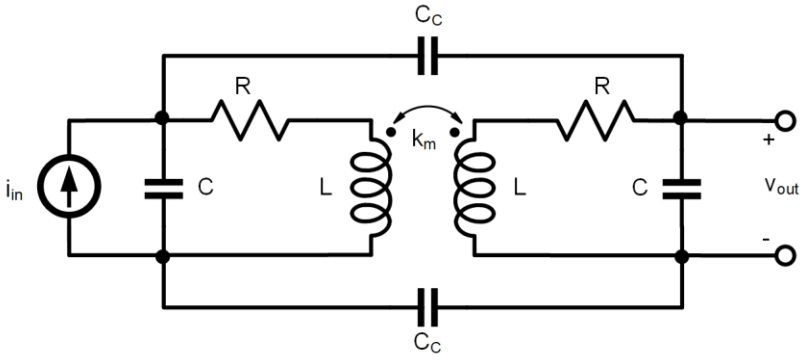


Fig. 2.5. Electrically and magnetically coupled resonant tanks

These are the category of tanks which are magnetically and electrically coupled simultaneously. The amplitude at two resonant frequencies, in this case, is equal and hence they are termed as gain-equalized transformers. Figure 2.5 shows the network design [14]. The trans-resistance of overall network can be derived as (2.22).

$$Z_{MC-CC}(s) = \frac{\frac{sC_c}{2}(sL(1-k_m)+R)(sL(1+k_m)+R)+sLk_m}{[s^2L(C_c+C)(1-k_m)+s(C_c+C)R+1][s^2LC(1+k_m)+sCR+1]} \quad (2.22)$$

The value of electrical coupling can be expressed as (2.23), and to achieve equal amplitudes, relation (2.24) must be satisfied.

$$k_C = \frac{C_C}{C_C + C_2} \quad (2.23)$$

$$k_c = \frac{-2k_m}{1-k_m} \quad (2.24)$$

Like the node analysis performed in previous cases, the trans-resistance for a gain equalized transformer at the natural resonant frequencies, ω_{n1} and ω_{n2}, can be described by (2.25) and (2.26).

$$|Z(j\omega_{n1})| = \frac{1}{2}\frac{L(1-k_m)}{R(C+C_C)} \quad (2.25)$$

$$|Z(j\omega_{n2})| = \frac{1}{2}\frac{L(1+k_m)}{RC} \quad (2.26)$$

Interestingly, in this network k_c is bound between 0 and 1, hence k_m will always be a negative value.

2.2.4 Series-Shunt LC Tanks

Bandwidth extension using series-shunt LC tanks can be explained with the help of Fig. 2.6 [15]. Here, R_L is the load resistance, R_S is the source resistance, L_1 and C_1 are a part of shunt LC tank, and L_2 and C_2 are a part of series LC tank.

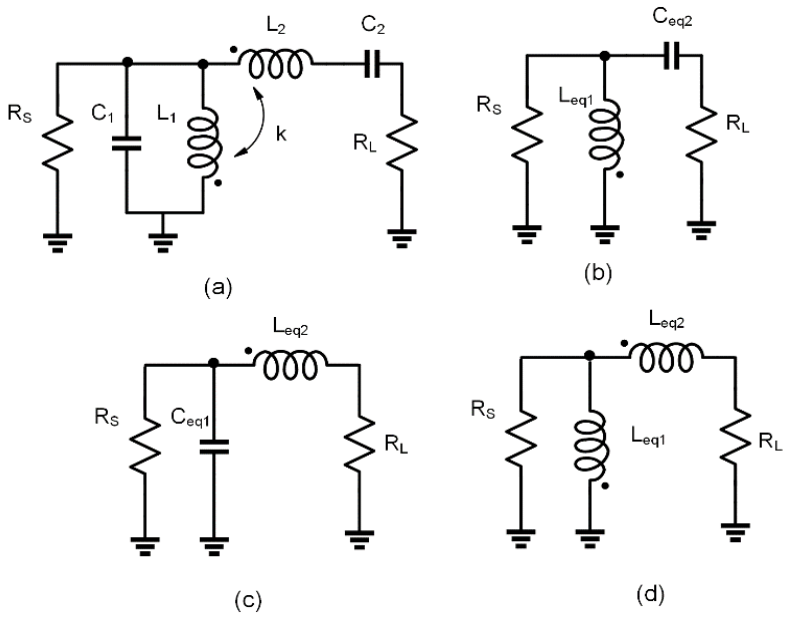


Fig. 2.6. (a) Series-shunt resonant tank. Equivalent circuit for (b) $f < f_2$, (c) $f > f_1$, and (d) $f_2 < f < f_1$

The underlying concept of this circuit design is to provide one resonance frequency (f_1) using L_1 and C_1, while other resonance frequency (f_2) comes from L_2 and C_2. Generally, f_2 is lower than f_1. When frequency, $f < f_2$, then the circuit of Fig. 2.6(a) can be reduced to an equivalent circuit, shown in Fig. 2.6 (b). Here, the series combination of C_{eq2} and R_L, on parallel transformation, becomes parallel to L_{eq1} and R_S. If L_{eq1} and C_{eq2} resonate at a frequency within the bandwidth, then the network can be termed as matched if transformed R_L is same as R_S.

A similar trend is seen for $f > f_1$. The circuit of Fig. 2.6(a) can be represented using the equivalent circuit, shown in Fig. 2.6(c). Here, the series combination of L_{eq2} and R_L, on parallel transformation, becomes parallel to C_{eq1} and R_S. At this point if C_{eq1} and L_{eq2} resonate at a frequency within the bandwidth, then the network can be termed as matched when transformed R_L, $R_{LT} = R_S$. The two resonant frequencies can be selected to provide wideband matching. As discussed in previous section, the location of the resonant frequencies and overall bandwidth can be varied using the coupling coefficient.

A challenge with this network is that the two poles cannot be placed wide apart, as in that case the matching is not performed efficiently. For instance, for $f_2 < f < f_1$, the circuit of Fig. 2.6(a) is equivalent to Fig. 2.6(d). Since there is no capacitance to resonate the inductance, the network will not be matched.

2.2.5 Performance Summary of Wideband Networks

There are several demonstrations of wideband circuits in prior work using transformer networks [14] – [20]. In [14], a mm-wave receiver with 20GHz bandwidth has been proposed. To achieve wideband functionality, a gain equalized transformer was placed between antenna and input of LNA. A mm-wave phased array receive beamformer has been implemented in [15], utilizing the series-shunt LC tank to achieve a bandwidth of 20GHz. In [16], a transformer feedback LNA has been designed by performing coupling between the inductor at gate and inductor between the cascode transistors. This achieved a bandwidth of 7GHz around a center frequency of 3GHz. The wide tuning range oscillator designed in [17] operated on the concept of electrically and magnetically coupled resonant tanks. A different way of mathematically analyzing magnetically coupled resonators, focused on transformer modelling and insertion losses, has been provided in [18]. Utilizing the idea of LC ladder matching network, i.e., series-shunt LC, a 7GHz broad LNA operating around 5GHz has been proposed in [19] and a 15GHz wide LNA operating at mm-wave has been introduced in [20].

2.3 Matching Networks

The noise contribution of LNA can be minimized if the input impedance is matched to the optimum noise impedance of input transistor. Thus, configuration and placement of matching networks (MN) at the gate of input transistor makes a significant impact on its performance. Three possible placements of MN have been depicted in Fig. 2.7. In [21], it has been observed that a parallel MN has a better noise performance, over a structure with no matching, but is inefficient in relation to series MN. The optimum performance can be achieved with simultaneous series-parallel MN, though it introduces a trade-off between frequency capabilities of input transistor and the noise factor.

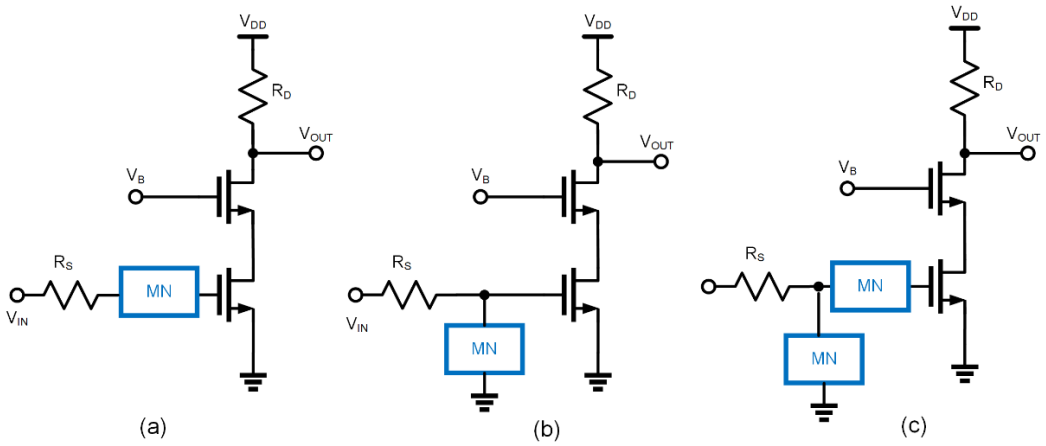


Fig. 2.7. Generic placement of matching network, (a) series, (b) parallel, (c) series-parallel combination

A source degenerated amplifier design, with a series inductor at gate acting as matching network [22], is shown in Fig. 2.8.

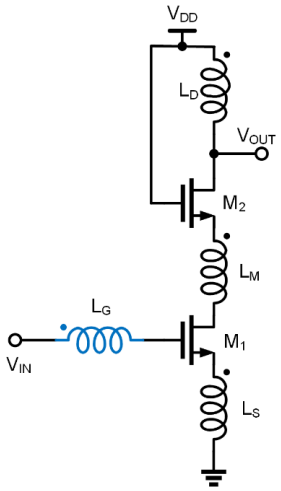


Fig. 2.8. Source degenerated amplifier with series matching inductor

Analyzing this network using standard node analysis method, the input impedance (Z_{IN}) is obtained as (2.27).

$$Z_{IN} = R_s + R_G + \omega_T Ls + j\omega(L_s + L_G) - j\frac{\omega_T}{\omega g_m} \tag{2.27}$$

Where, R_S and R_G are source and gate resistances, respectively, ω_T is transit frequency in radians and g_m is small-signal transconductance. To obtain impedance match, the imaginary components of Z_{IN} can be tuned out and the resistive components

can be matched to antenna impedance. Since such networks have a single resonance, they provide a narrow bandwidth.

A cascode amplifier with a parallel inductor as matching network [16], is given in Fig. 2.9. Wideband operation has been achieved by magnetically coupling the matching inductor with the inductor placed between CG and CS transistors.

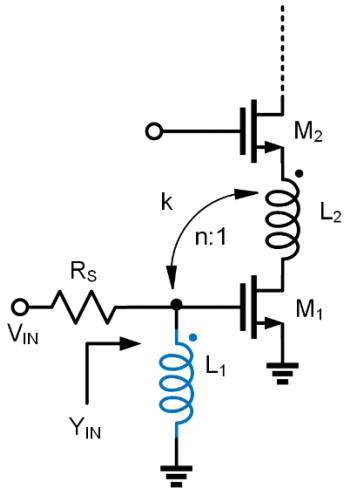


Fig. 2.9. Cascode amplifier with parallel matching inductor

The input admittance in this case can be given by (2.28).

$$Y_{in} = \frac{1}{sL_1} + \frac{k}{n} g_{m1} + sC_{gs} \tag{2.28}$$

Where C_{gs} is the parasitic gate-source capacitance of input transistor. Here, the matching can be implemented by resonating out the imaginary components and adjusting the resistive part to reciprocal of input resistance.

The third circuit under analysis is a combination of series and parallel matching network. Again, inductors are used for creating this design [23], which is shown in Fig. 2.10.

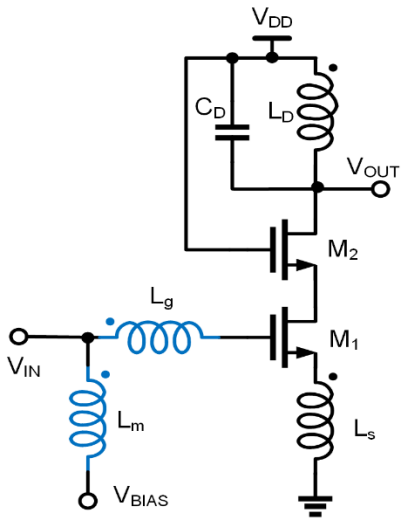


Fig. 2.10. Source degenerated amplifier with series-parallel matching inductor

The mathematical analysis of this network generates the input impedances as

$$Z_{IN} = \frac{s^2 L_m L_g C_{gs1} + s\omega_T L_m L_S C_{gs1} + L_m}{s^2 L_g C_{gs1} + s(\omega_T L_S C_{gs1} + L_m C_{gs1}) + 1} \tag{2.29}$$

Here, C_{gs1} is the gate-source capacitance of the transistor and ω_T is transit frequency in radians. This network has two resonant frequencies, one due to the parallel combination of L_m and pad capacitance, and other due to the series combination of C_{gs1} and (L_g+L_s). The operation of this MN is like a wideband network discussed in 2.2.4.

2.4 Techniques for Noise Suppression

Broadly categorizing, common gate (CG), common source (CS), and cascode of CG-CS are three main topologies for implementing LNAs. Cascode is widely used amongst these because of its ability to provide better isolation, improved bandwidth, and higher gain both at RF and mm-wave frequencies. However, it suffers from the drawbacks of increased noise and reduced transit frequency. One technique to address this tradeoff is to employ an inductor between CG and CS transistors, which aids in reduced noise and improves transit frequency. Another approach is to design a noise cancelling LNAs that provide wideband matching and low noise simultaneously.

2.4.1 Noise Reduction Method

The idea here is to improve the performance of cascode LNA at mm-wave frequencies by placing a series inductor between CG and CS transistors to tune out the middle parasitic capacitances and provide improved noise and frequency metrics [22]. The enhanced cascode structure is shown in Fig. 2.11.

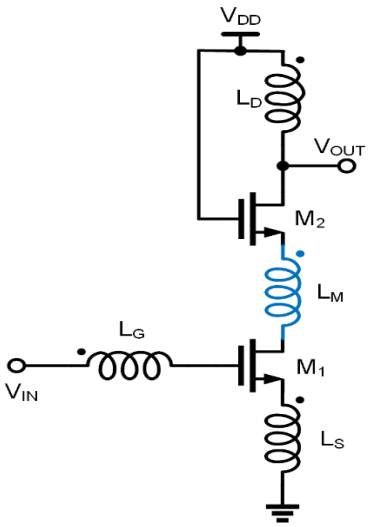


Fig. 2.11. Source-degenerated cascode amplifier with noise reduction inductor

The series inductor L_M creates an artificial transmission line with the parasitic capacitances of transistors M_1 and M_2. The characteristic impedance of this transmission line can be computed as the load impedance of M_1 or source impedance of M_2. The derived impedances can be shown as (2.30) and (2.31).

$$Z_{01} = \sqrt{\frac{L_M}{C_{gs2} + C_{sb2}}} = Z_{M1,load} \tag{2.30}$$

$$Z_{01} = Z_{M_2,in} = \frac{1}{g_{m2}} + \frac{\omega L_{D1} Q}{1 + g_{m2} r_{02}} \tag{2.31}$$

The above equations provide insight into the functionality of the transmission line. However, without the knowledge of load inductance, it's difficult to use these derived equations. Therefore, a more intuitive way of computing the value of L_M is to simulate f_T and NF_{min} as a function of L_M and select the optimal value of L_M based on design objectives.

A mathematical analysis of this modified structure has been provided in [24]. If the parasitic capacitors of M_1 and M_2 are ignored, then the noise contribution of M_2 can be represented as (2.32).

$$F_{d2} = \gamma_2 \left(\frac{\omega}{\omega_T}\right)^2 g_{d02} R_S \frac{1}{g_{m2}^2 r_{01}^2} \tag{2.32}$$

Here, γ is the channel noise coefficient and g_{d0} is the zero bias drain conductance. In this case, noise can be ignored as $g_{m2}r_{o1}$ is a very large quantity. However, the presence of parasitic capacitors alters this noise contribution as (2.33).

$$F_{d2} = \gamma_2 \left(\frac{\omega}{\omega_T}\right)^2 g_{d02} R_S \frac{\omega^2 C_X^2}{g_{m2}^2} \tag{2.33}$$

Here, C_X represents the parallel combination of parasitic capacitances from M_1 and M_2. A large C_X can increase the noise contribution of M_2 and hence a series inductor is needed, either in shunt or series, to tune out C_X. The value of series inductor can be obtained using the following relation, i.e., (2.34).

$$L_M = \frac{C_{p1} + C_{p2}}{\omega^2 C_{p1} C_{p2}} \tag{2.34}$$

2.4.2 Noise Cancelling LNA

Channel thermal noise is the most prominent noise source in CMOS LNAs. Therefore, while designing amplifiers it is targeted to minimize the generation of this noise. The purpose of this section is to briefly discuss some techniques of dealing with channel noise [24].

2.4.2.1 Conventional Noise Cancelling Technique

Shunt-feedback topology in CS amplifiers is the conventional noise cancelling scheme, shown in Fig. 2.12.

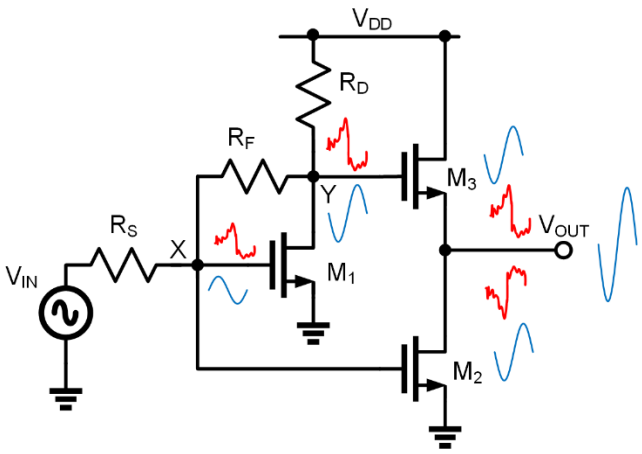


Fig. 2.12. Conventional noise cancelling method in CS amplifiers

This circuit functions in the following manner, the noise current of input transistor, M_1, flows through the feedback resistor, i.e., R_F, and creates a noise voltage at node X, V_{nX}, which is in-phase with noise voltage at node Y, V_{nY}, but have different amplitude. This noise voltage at X, gets amplified and inverted by M_2 and reaches to the output node. At the same time, the noise at Y reaches output node through M_3. Both these noise voltages at output are opposite in phase and same in amplitudes. Hence, adding these up results in cancellation of noise. It is important to track the input signal, which in this case adds constructively at the output node.

The mathematical equations supporting this functionality can be given as (2.35) and (2.36).

$$V_{n,out} = V_{nY}\frac{r_{ds2}}{r_{ds2}+\frac{1}{g_{m3}}} - V_{nX}\frac{g_{m2}}{g_{m3}} = 0 \tag{2.35}$$

$$\frac{R_F + R_S}{R_S} = \frac{g_{m2}}{g_{m3}} \tag{2.36}$$

Where $g_m r_{ds} >> 1$ was assumed.

The drawback of this technique is the need for an additional stage to amplify and invert the noise. This results in increased power consumption and larger chip area.

2.4.2.2 Current Reuse Technique

This technique helps in overcoming the drawback of increased power in conventional noise cancelling method. The current flowing through input transistor can

be reused to bias the auxiliary transistor performing the function of inversion and amplification of input transistor's channel noise. The circuit for this technique is shown in Fig. 2.13.

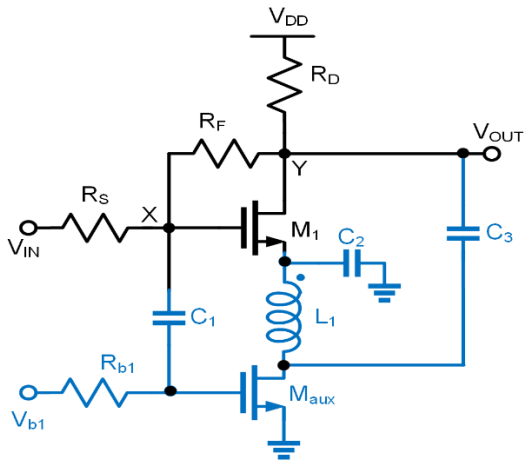


Fig. 2.13. Current reuse noise reduction technique

The channel noise of M_1 creates a noise voltage at node Y, V_{nY}, which reaches node X as V_{nX} through the resistive divider formed by R_F and R_S. This noise voltage at X is then amplified and inverter by the auxiliary transistor (M_{aux}). The interesting function here is that the current of M_{aux} is injected directly to the output node of M_1. Since the noise voltages at drain of M_1 and drain of M_{aux} were opposite in polarities, they cancel out each other at the output node. This implies that by following this technique, the cancellation can be performed without creating an additional branch.

The inductor added between M_1 and M_{aux} provides some ac isolation between the source and drain of respective transistor. Whereas dc-wise, the current through M_1 can be used for biasing M_{aux}. The conditions for performing the cancellation can be obtained as

$$V_{n,out} = V_{nY} - V_{nX} g_{maux} R_D = 0 \tag{2.37}$$

$$\frac{R_F + R_S}{R_S} = g_{maux} R_D \tag{2.38}$$

2.5 Performance Summary of RF/mm-Wave LNAs

Table 2.1 summarizes the performance of existing LNA designs operating at RF and mm-wave frequencies [48]. In [26] and [27], g_m-boosting technique has been applied, and design in [26] is particularly low power due to reuse of current amongst transistors. The topologies in [28]-[31] are variable gain amplifiers, all fabricated in different technology nodes. In [32], a high-frequency, low power amplifier has been proposed using drain-gate feedback technique. An ultra-low NF, and high gain topology has been provided in [33]. In [34], a very high centre frequency has been selected, whereas in [35] an extremely low power design operating at high frequency has been presented. It has been proved by [25] and [37] that amplifiers in 22nm technology nodes can achieve high gain with low power.

Table 2.1. Performance summary of RF/mm-wave LNA designs

Ref.	***Technology***	***f (GHz)***	***BW (GHz)***	***NF (dB)***	***S11 (dB)***	***S21 (dB)***	***IIP3 (dBm)***	***V_{DC} (V)***	***P_{DC} (mW)***
[25]	22nm	77	12	4.6	-9	20	-	1	9
[26]	65nm	18.8	5.6	3.3	-10	14.9	-	1	1.9
[27]	65nm	28.7	7.6	3.25	-10	18.33	-	1.2	20.52
[28]	55nm	9.25	5.5	3.26	-14	20.2	-5.94	1.3	75
[29]	65nm	57	8	4.8	-10	25	-	1.3	36.5
[30]	22nm	5.5	1	1.9	-5	30.5	-19.9	1	39
[31]	40nm	63	6	6	-10	19.8	-19	1.1	18
[32]	45nm	93.75	17.5	4.2	-10	12	-	0.5	4.7
[33]	65nm	10.7	3	1.66	-10	32.48	-25.3	1	22
[34]	28nm	154.5	23	8.5	-10	15.7	-	-	32
[35]	32nm	94.5	11.6	4.5	-10	7.2	-	-	5.2
[36]	22nm	70.5	3	3.7	-10	20	-	1	10.8

Chapter 3

LNA DESIGN

The wideband techniques, discussed in previous section, have been implemented in designing of LNA achieving a bandwidth of 20GHz. Two versions of three stage amplifier, exploiting source degenerated cascode architecture with noise reduction inductor, and transformer based interstage wideband networks have been designed in 22nm FFL technology. A generic design methodology has been provided in the end.

3.1 Proposed Circuit

The three-stage circuit topology with single ended input, in-phase and quadrature outputs, and wideband interstage networks, operating on the concept of dual resonance, is presented in Fig. 3.1.

Two versions of LNA have been fabricated. Design A, occupying a die area of 1.5x.5mm^2, has single ended RF outputs capable of driving resistive loads of 50Ω. Design B, integrated with a sub-harmonic mixer, and occupying a chip area of 2x2mm^2, has differential outputs capable of driving resistive loads of 150Ω. Both amplifiers differ in the wideband output network acting as load in third stage, as shown in Fig. 3.1.

Each stage comprises of two transistors, wherein M_1 is common source input transistor and M_2 is the common gate cascode transistor. Both the devices are operated at optimum current density to minimize their noise contributions. Inductor L_m, placed between M_1 and M_2, contributes to lowering the noise of cascode configuration. Degeneration inductors (L_s) provides a degree of freedom in adjusting the input impedance of the cascode network which supports better matching at the input side. The mutually coupled series-shunt LC tank acts as the interstage network between consecutive stages. The purpose of this design is to provide dual resonance frequencies which aids in widening the bandwidth and simultaneously provides impedance and noise matching over a wide range of frequency. The resistances placed at load of every

stage reduces the constraint on LC values in terms of impedance match. ESD protection is provided at bias node of each stage.

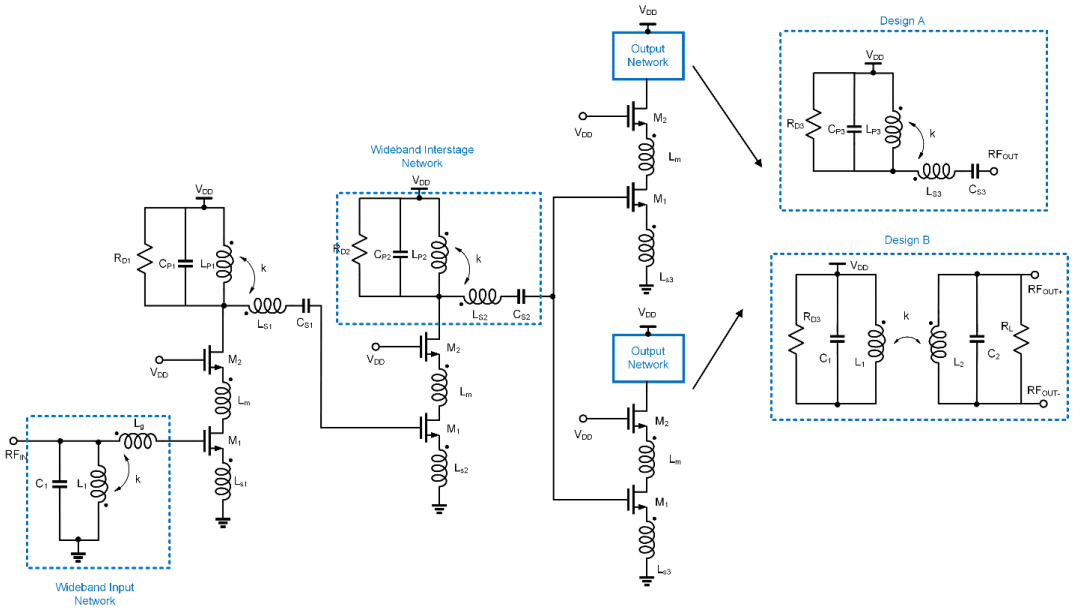


Fig. 3.1. Proposed LNA cascode configuration with double-tuned input and load networks

The following sections will focus on some critical sectors in LNA design, such as device selection, noise reduction techniques, dual resonance transformer designs and matching constraints.

3.2 Device Selection

The process of optimum device selection begins with characterizing every available transistor in the technology, through dc and s-parameter analysis. The purpose is to identify the transistor with lowest intrinsic noise figure at desired frequency. Later, parameters such as optimum current density (J_{OPT}), minimum noise figure (NF_{min}), transit frequency (f_T), and unity gain frequency (f_{max}) are observed. This chapter discusses the procedure to carry out such analysis [37].

3.2.1 Defining Model Parameters

Figure 3.2. shows the small signal model of transistor device, where C_{gd} and C_{gs} are the gate-drain and gate source parasitic capacitances of transistor, respectively, and r_{ds}

is drain-source parasitic resistance. The model parameters essential for characterizing transistors are derived from this small signal model.

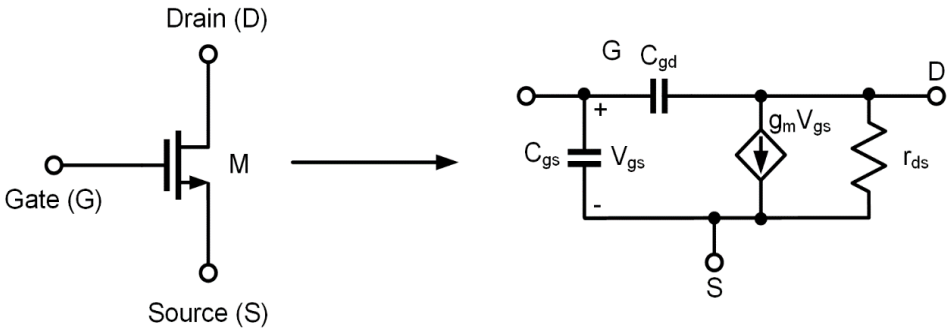


Fig. 3.2. Small signal model of transistor

The model parameters which aid in selecting the optimum device as per design specification are defined as:

a. Gate Source Voltage (V_{gs}) - This is an important parameter which defines the region of operation of transistor and directly affects the current flowing through it.

b. Transconductance (g_m) – This is defined as the change in the drain current due to change in gate-source voltage. It directly impacts a range of design specifications such as gain, frequency of operation, current consumption etc.

c. Drain Current (I_D) – Current that flows through the drain of a transistor is termed as I_D. It defines power consumption of a circuit. Current density, defined as ratio of drain current and width of transistor, is a vital parameter to g_m/I_D process.

d. Transit Frequency (f_T) – Frequency at which the small signal current gain of transistor is unity is termed as transit frequency.

e. Maximum Frequency (f_{max}) – Frequency at which power gain of device is unity is termed as maximum frequency.

f. Minimum Noise Figure (NF_{min}) – This is a measure of the minimum degradation of signal to noise ratio as the signal passes through an amplifier based on the device.

3.2.2 Performing Transistor Analysis

This method involves performing a dc sweep and s-parameter simulations, on each transistor present in the technology node and observing certain specific model

parameters, such as drain current (I_D), current density (J) and minimum noise figure (NF_{min}). Figure 3.3 gives the associated circuit.

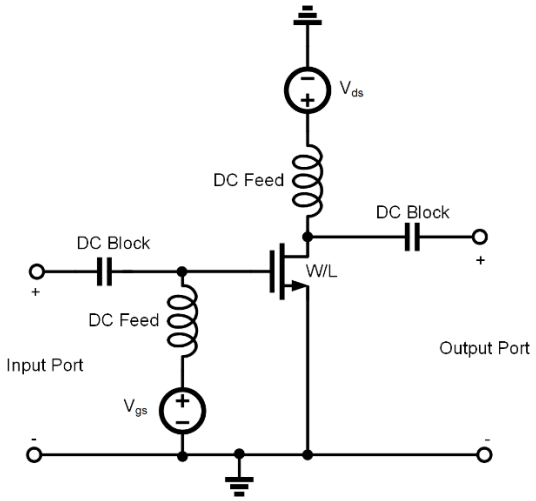


Fig. 3.3. Schematic for DC and s-parameter analysis for transistor characterization

Transistors hold the capability of operating at the lowest NF_{min} at a certain current density, i.e., J_{OPT}. Above analysis obtains this optimum point of operation for every available transistor and indeed concludes which transistor has the lowest NF_{min}, eventually employing it in amplifier design.

In 22FFL technology there are five different types of transistors and characterization of every device was performed. It was observed that around a current density of 0.2mA/um, every transistor attains the best performance in terms of noise figure. The data collected through this analysis has been provided in table 3.1.

Table 3.1. 22FFL technology transistor characterization

Device 1, f_T=210G and f_{max}=236G			
V_{bias} (mV)	Current (I) (mA)	I/W (mA/um)	NF_{min} (dB) (35G)
200	0.19	0.019	1.5
250	0.54	0.054	1.2
300	1.1	0.11	1.06
350	2.045	0.2045	1.01
400	3.1	0.31	1.02
450	4.3	0.43	1.07
500	5.7	0.57	1.14

Device 2, f_T=219G and f_{max}=229G			
V_{bias} (mV)	Current (I) (mA)	I/W (mA/um)	NF_{min} (dB) (35G)
200	0.26	0.026	1.58
250	0.69	0.069	1.27
300	1.4	0.14	1.1
350	2.3	0.23	1.09
400	3.5	0.35	1.1
450	4.9	0.49	1.17
500	6.3	0.63	1.2

Device 3, f_T=230G and f_{max}=217G			
V_{bias} (mV)	Current (I) (mA)	I/W (mA/um)	NF_{min} (dB) (35G)
200	0.005	0.0005	1.26
250	0.03	0.003	2.17
300	0.133	0.0133	1.89
350	0.413	0.0413	1.45
400	0.94	0.094	1.23
450	1.7	0.17	1.15
500	2.7	0.27	1.14

Device 4, f_T=206G and f_{max}=238G			
V_{bias} (mV)	Current (I) (mA)	I/W (mA/um)	NF_{min} (35G)
200	0.002	0.0002	0.8
250	0.015	0.0015	1.59
300	0.074	0.0074	1.8
350	0.26	0.026	1.44
400	0.685	0.0685	1.17
450	1.36	0.136	1.05
500	2.29	0.229	1.01

Device 5, f_T=341G and f_{max}=364G			
V_{bias} (mV)	Current (I) (mA)	I/W (mA/um)	NF_{min} (dB) (35G)
200	0.39	0.039	0.87
250	0.927	0.0927	0.7
300	1.7	0.17	0.632
350	2.8	0.28	0.616
400	4.2	0.42	0.645
450	5.7	0.57	0.694
500	7.2	0.72	0.767

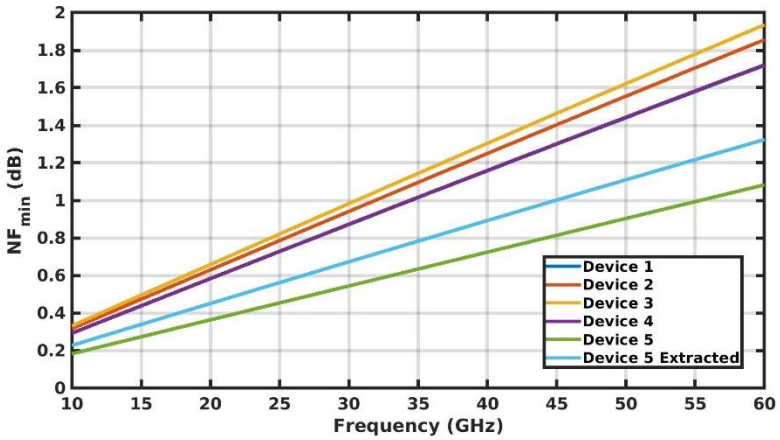


Fig. 3.4. NF_{min} characterization of n-type devices in 22FFL technology

It can be concluded that optimum operating point for every device lies around 0.2mA/um. Figure 3.4 shows that the device 5 has the lowest NF_{min}, along with the best f_T and f_{max} performance. Therefore, this device seemed suitable for mm-wave design. A layout design using device 5 was prepared with a gate width per finger of 2.88um and total width of 46um. The above simulated graphs indicates that, at 35GHz, there is a deviation of about 0.2dB in NF_{min} value of extracted RC results and native transistor.

3.2.3 Performing g_m/I_D Analysis on Selected Device

When designing in sub-micron region, the conventional square law model of transistors cannot accurately define the I-V behavior of them and hence cannot be used as a link between design specifications and model parameters. A robust methodology, capable of characterizing transistor in an optimal fashion needs to be adopted. G_m/I_D is a systematic approach that aids in understanding the performance of transistors under different considerations, such as short channel and long channel transistors, inversion level, bandwidth, high speed operation, noise performance etc.

Transconductance (g_m), transit frequency (f_T), and minimum noise figure (NF_{min}) are the model parameters crucial for attaining lowest noise performance. This section will study the variations in these model parameters with respect to different DC bias voltages/current densities. The results discussed are for the selected transistor (device 5) for amplifier design.

3.2.3.1 Transconductance

Transconductance has direct impacts on gain and frequency capabilities of a device. Thus, optimizing on this parameter is critical. To perform dc simulations, V_{gs} and V_{ds} were kept variable. The idea was to observe the behavior of transconductance against drain current per unit width (I_{ds}/W). The results corresponding to this analysis are included in Fig. 3.5.

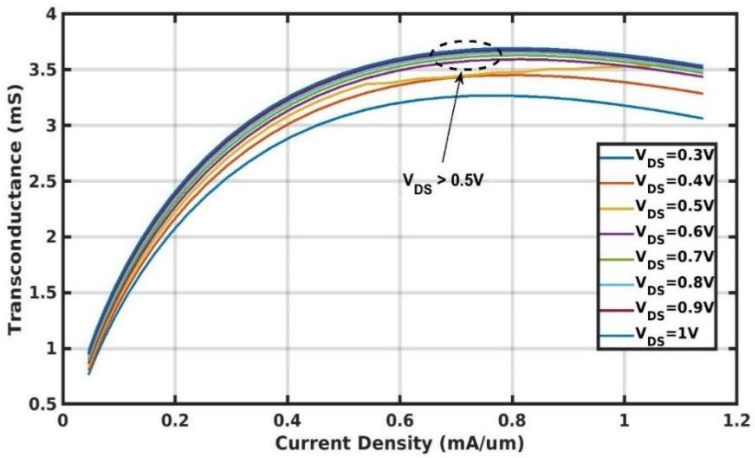


Fig. 3.5. Variations in transconductance with different bias voltages

As indicated, when V_{ds} goes above 0.5V, there is not much significant variation in the g_m of the device. Hence, the power consumption of structure can be reduced by using supply lower than the nominal voltage as g_m changes are not significant after a certain level.

3.2.3.2 Transit Frequency

Since the design goal is to implement an amplifier at mm-wave frequency, it is beneficial to achieve a high transit frequency (f_T) to allow an appreciable gain-bandwidth performance. The behavior of f_T is observed by simulating it against I_{ds}/W for a drain voltage of 0.7V and 0.5V. The generated results have been provided in Fig. 3.6.

The graph concludes that f_T peaks around current density of 0.5mA/um, beyond this point it decreases. Therefore, the transistors can be biased for the current density which provides desired f_T as per the operating frequency.

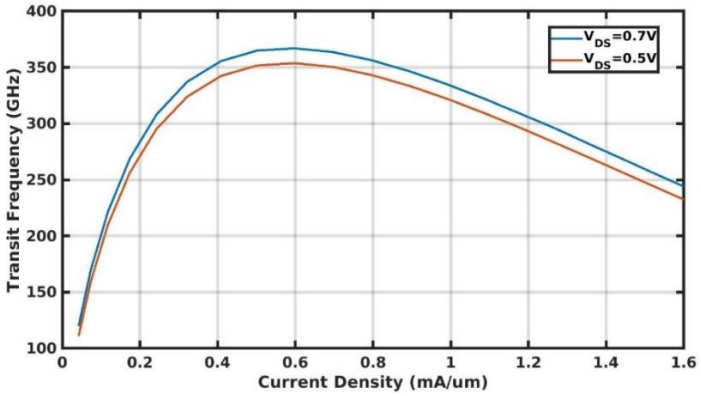


Fig. 3.6. Variations in transit frequency with different bias voltages

3.2.3.3 Minimum Noise Figure

The results presented in section 3.2.2 indicates that minimum noise contribution by transistor happens at a specific I_{ds}/W, which is termed as optimum density point. The NF_{min} performance in previous section was depicted against frequency, hence here the variations are shown against I_{ds}/W. The simulated performance is given in Fig. 3.7.

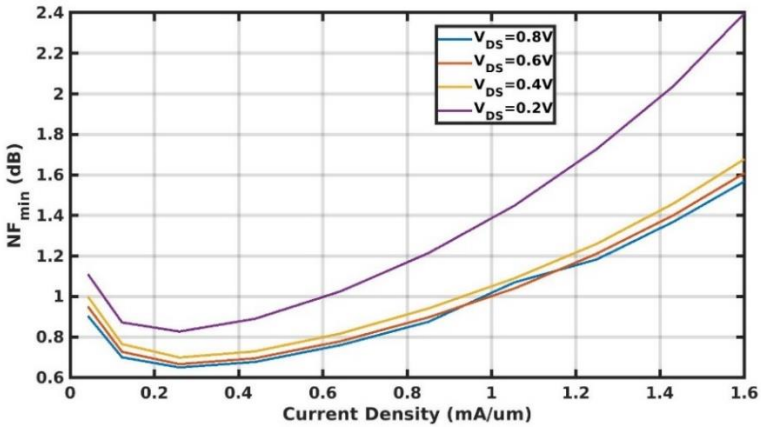


Fig. 3.7. Variations in minimum noise figure with different bias voltages

Lowest NF_{min} can be observed around a current density of 0.25mA/um, which is in accordance with the data shown in previous section.

3.3 Noise Reduction Technique in Cascode Configuration

Cascode structure is beneficial in increasing gain of amplifier stage without much increment in the power consumption. However, it demands a trade-off with noise. When a cascode transistor is placed above the input transistor, the noise from cascode

device starts affecting the output. Consequently, it becomes crucial to adopt noise reduction methods to deal with this trade-off. Figure 3.8 gives the circuit deployed to deal with the issue.

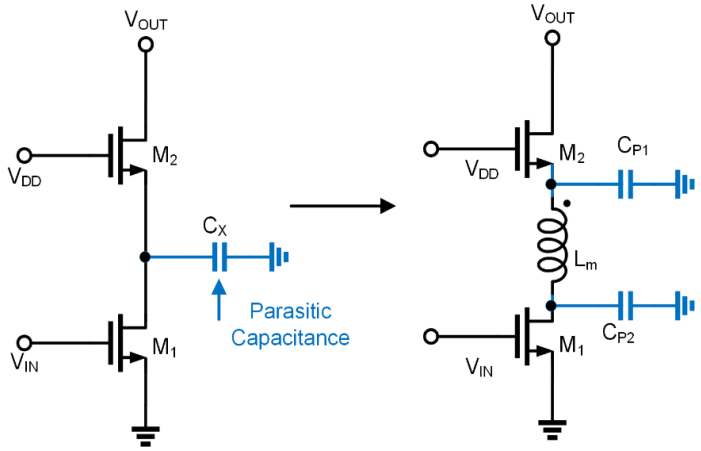
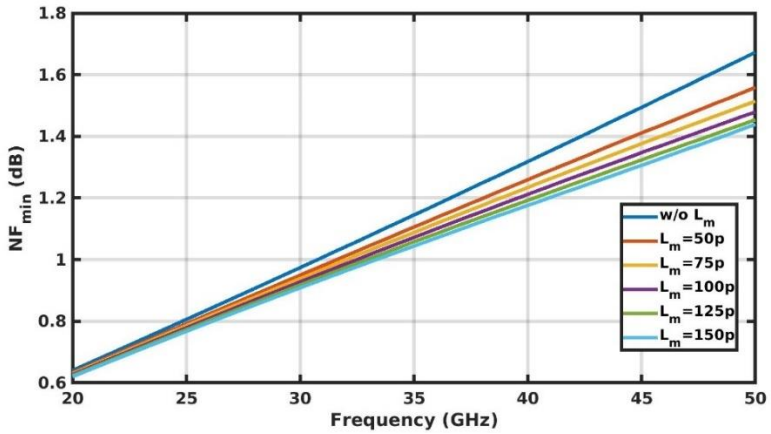


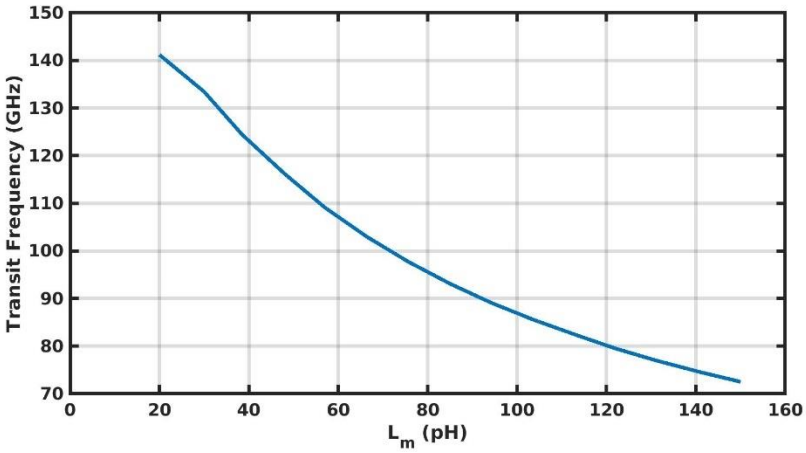
Fig. 3.8. Network for reducing noise in cascode amplifier

The performance of this modified cascode structure has been discussed in detail in section 2.4.

The value of L_m supporting a reduced NF_{min} and improved f_T was obtained through simulations. The curves for different NF_{min} achieved for a range of L_m are shown in Fig. 3.9 (a). Similar variations in f_T with L_m is provided in Fig. 3.9 (b). It is evident that increasing L_m reduces NF_{min}, specifically at frequencies above 40GHz, but it also reduces f_T which is undesirable. Hence, compromising the optimality of both parameters, a reasonable performance for both NF_{min} and f_T was accepted.



(a)



(b)

Fig. 3.9. Effect of modified cascode network on model parameters, (a) NF_{min}, and (b) transit frequency

3.4 Wideband Matching Network

3.4.1 Input Impedance of Device

In its simplest form, the impedance of transistor looking into the gate is purely capacitive. Therefore, devices need to have some additional circuitry around them to attain resistive component in its input impedance. Inductive source degeneration assists in this regard. The circuit widely used for this particular purpose is given in Fig. 3.10.

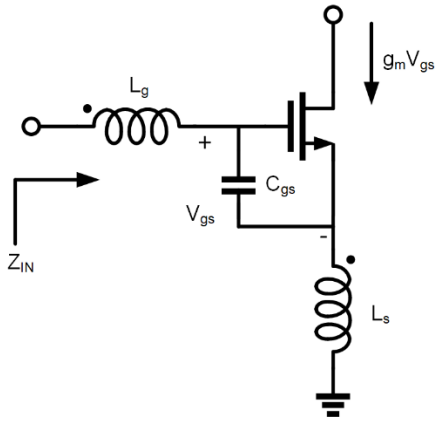


Fig. 3.10. Input network for source degenerated transistor

The input impedance for this configuration is given below in (3.1), here L_s is degeneration inductor whereas L_g helps in tuning out C_{gs} at frequency of interest (ω_0), given by (3.2).

$$Z_{IN} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{3.1}$$

$$\omega_0 = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \tag{3.2}$$

The above impedance equation indicates that with source degeneration inductor better impedance matching with subsequent stages can be obtained. Increasing L_s, to match to a resistive value, lowers the gain of the stage. Also, there is certain lower limit on C_{gs}, set by the parasitic of the transistor. The current consumed by amplifier scales with g_m, which means higher g_m results in higher power consumption. Therefore, value of all three parameters need to be meticulously decided without degrading other performance parameters. This impedance matching network does not help in achieving wide bandwidths and consequently more sophisticated networks would be placed at input to achieve matching over wide band.

3.4.2 Dual Resonance Based Matching Circuit

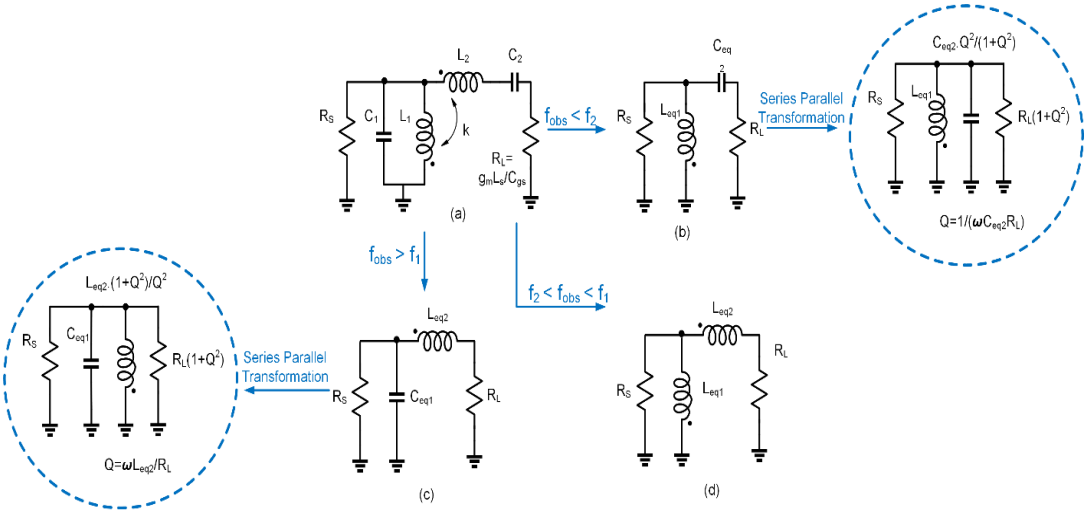


Fig. 3.11. (a) Dual resonance based interstage transformer network. Equivalent circuit for (b) $f_{obs} < f_2$, (c) $f_{obs} > f_1$, (d) $f_2 < f_{obs} < f_1$

The functioning of the mutually coupled series-shunt LC tank network, for obtaining impedance and noise match, over a wide bandwidth is depicted in Fig. 3.11. For analysis purposes, assume this network as a coupling between output of first stage and input of second stage. The load resistance R_L, shown in Fig. 3.11(a), comes from the input side of second stage and can be tuned using the source degeneration inductance

(L_s) of this stage. The capacitance affecting R_L is the gate-source parasitic capacitance (C_{gs}) of the input transistor and for designing flexibility another capacitor may be placed in parallel to C_{gs} to give better controllability over R_L. However, the impact of it over gain and noise must be monitored carefully. The capacitance (C_2) is the series effect of L_s and C_{gs} of second stage input network.

The series LC combination is made to resonate at a frequency (f_2) which must lie within the frequency range of interest. The parallel LC combination resonates at another frequency (f_1) also within the targeted band of frequency. Usually, f_2 is lower than f_1. The idea is to spread these frequencies reasonably within the bandwidth to make the transformation network a wideband design. In the proposed amplifiers, in the coupling network between first two stages, f_2 is set as 25 GHz and f_1 is set at 38 GHz. Towards the lower side of frequency band, i.e., when observation frequency (f_{obs}) is less than f_2, the series-shunt LC network reduces to circuit shown in Fig. 3.11(b). Series parallel transformation concept indicates that with the obtained reduced circuit, it's possible to up-transform the impedance R_L. Similarly, when observation frequency is above f_1, then series-shunt LC network reduces to circuit shown in Fig. 3.11(c), which again can up-transform R_L. The coupling coefficient (k) between L_1 and L_2 provides adjustability of pole locations and hence bandwidth of operation can be varied without tuning L and C values.

3.5 Wideband Differential Output Transformer

In proposed LNA topology, for design B, single ended input is converted to differential outputs for which transformers are used in the output network of third stage. The purpose of this amplifier design was to enable its integration with a differential mixer whose input impedance was around 150 ohms. Hence, the challenge here was to design a wideband transformer which coverts single ended signal to differential whilst achieving wideband impedance transformation. Another critical consideration with wideband transformers is the need of high coupling between the coils, which is very competitive to achieve practically.

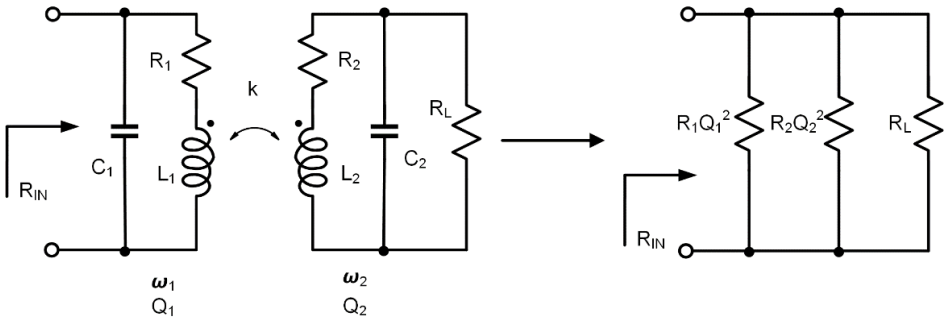


Fig. 3.12. (a) Wideband differential output design, (b) equivalent network at resonant frequencies

The concept of impedance matching using transformers is depicted in Fig. 3.12 (a). Herein, L_1 and C_1 resonates at f_1, while L_2 and C_2 resonates at f_2. With high quality factors for the coils, the series resistance for the inductors transforms to large parallel resistances as shown in Fig. 3.12 (b). This reduces their impact on the transformed value of R_L. Therefore, if all passive components are selected in a way such that f_1 and f_2 lie within the frequency range of interest, then the transformed parallel resistances along with R_L can be made equivalent to R_{IN}. The design equations for such transformation network are as shown in (3.3) - (3.6).

$$\omega_1 = \frac{1}{\sqrt{(L_1(1-k)C_1}} \tag{3.3}$$

$$\omega_2 = \frac{1}{\sqrt{(L_2(1+k)C_2}} \tag{3.4}$$

$$Q_1 = \frac{1}{R_1}\sqrt{\frac{L_1(1-k)}{C_1}} \tag{3.5}$$

$$Q_2 = \frac{1}{R_2}\sqrt{\frac{L_2(1+k)}{C_2}} \tag{3.6}$$

3.6 Design Methodology

A generalized approach towards designing of wideband amplifiers, with noise and impedance matching achieved by transformers, can be defined as follows:

1. *Understanding all Available Transistors in the Technology*: A systematic method, such as g_m/I_D, must be followed to characterize all the available transistors. A

meticulous study of performance parameters, such as f_T, NF_{min}, g_m, J_{OPT}, must be performed and depending on targeted specifications, the device must be selected.

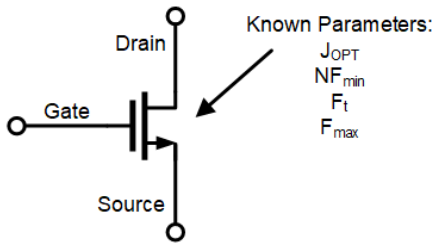


Fig. 3.13(a). LNA design step 1

2. *Noise Analysis of Cascode Structure*: Once transistors with optimum current density are identified, a cascode configuration must be implemented and noise figure of this structure should be calculated. If needed, noise reduction techniques can be utilized here to reduce the noise contribution of combined transistors. Placing an inductor between the transistors is one such technique.

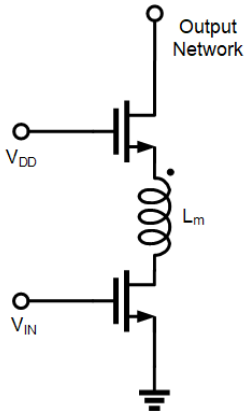


Fig. 3.13(b). LNA design step 2

3. *Deriving Input Impedance of Stages*: The degeneration inductance provides a convenient way of adjusting the impedance seen looking into the gate of input transistor. With keeping power consumption low, and without disturbing the optimum current density attainment, the impedance can be adjusted for wideband matching.

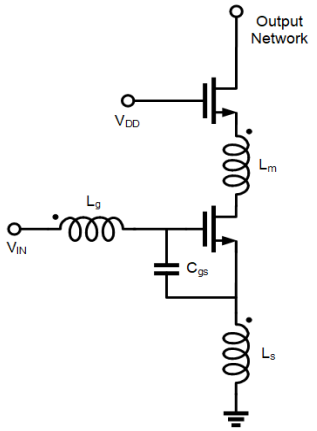


Fig. 3.13(c). LNA design step 3

4. *Designing the Wideband Input Network*: The mutually coupled series-shunt LC design can be implemented at this step. The idea is to achieve dual resonance within the frequency range of interest, carefully achieving impedance and noise matching between antenna and input stage.

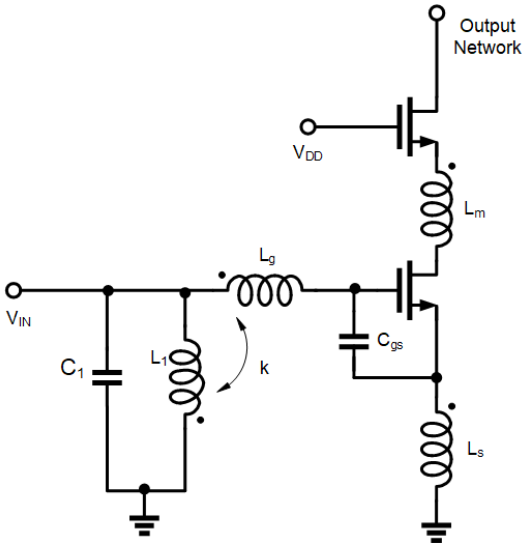


Fig. 3.13(d). LNA design step 4

5. *Designing the Wideband Interstage Network*: The similar concept of dual resonance and matching is applied in designing interstage transformer networks. The difference lies in the targeted impedance values. The size of transistors in the following stages plays a crucial role here. The dimensions can be set depending on noise, power, gain and linearity requirements.

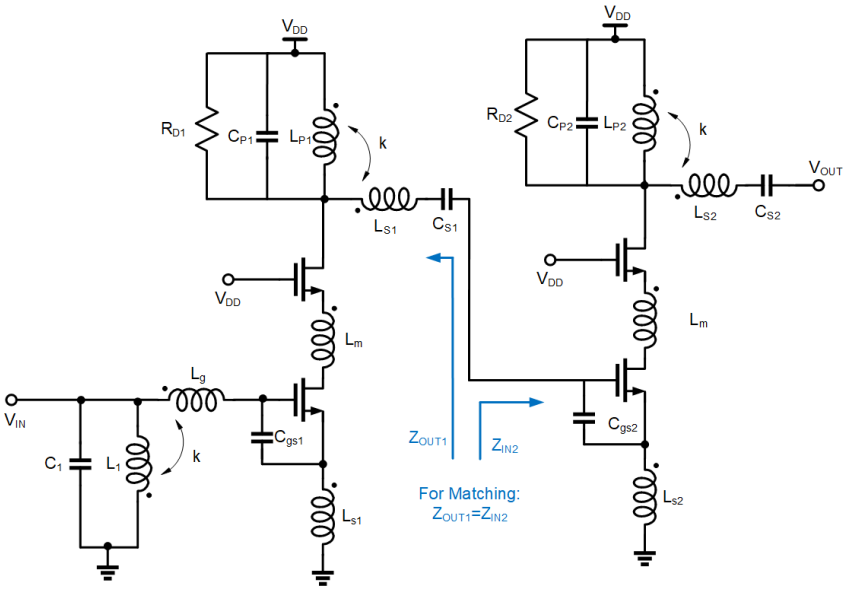


Fig. 3.13(e). LNA design step 5

6. *Designing of Wideband Output Network*: The impedance matching in this case depends on the block that might follow the designed two stage LNA by far. If the purpose is to experimentally test this, then output impedance of stage 2 must be matched to 50 ohms. If another stage of amplification is needed, then step 5 must be iterated till targeted gain is achieved.

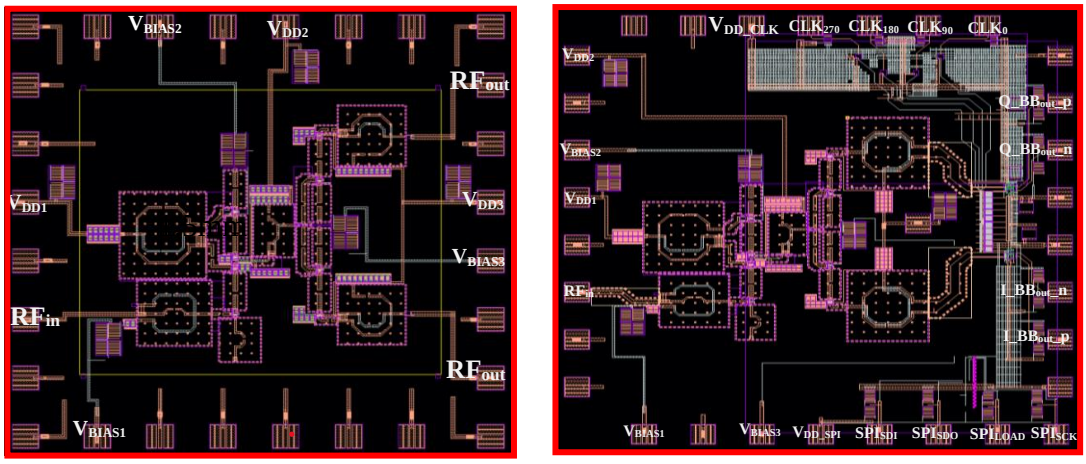
Chapter 4

LAYOUT OF WIDEBAND MILLIMETER-WAVE LNAs

The LNAs are designed in the 22nm FFL process, which offers 8 metal layers and a high-resistivity substrate. Layers M_1-M_6 are thin lower metals and M_7-M_8 are thick top metals with lower sheet resistance. Given the high frequency of operation, the physical layout must minimize parasitic effects, include EM simulations that consider distributed models for interconnect and account for electromigration-induced width constraints

Electromigration in thin wires limits the current-carrying ability of metals. For instance, the width of transistor in proposed LNA is 46um and the current density is 0.2mA/um. This implies that the current flow path, i.e., from *D* to *S*, must have metal interconnects capable of handling 10mA of DC current. Additionally, a wide metal has lower parasitic resistance but higher parasitic capacitance, due to increased metal area. In practice, optimal layout is an iterative process with evaluation of competing options and refinements based on parasitic-aware simulations.

The physical layout for amplifier (design A) is given in Fig. 4.1(a), and for receiver chain (design B) is given in Fig. 4.1(b).



(a) (b)

Fig. 4.1. Physical layout with pad frame for (a) design A, and (b) design B

4.1 Multistage LNA Layout and Results

4.1.1 Design A: Single Ended Input to Single Ended Output

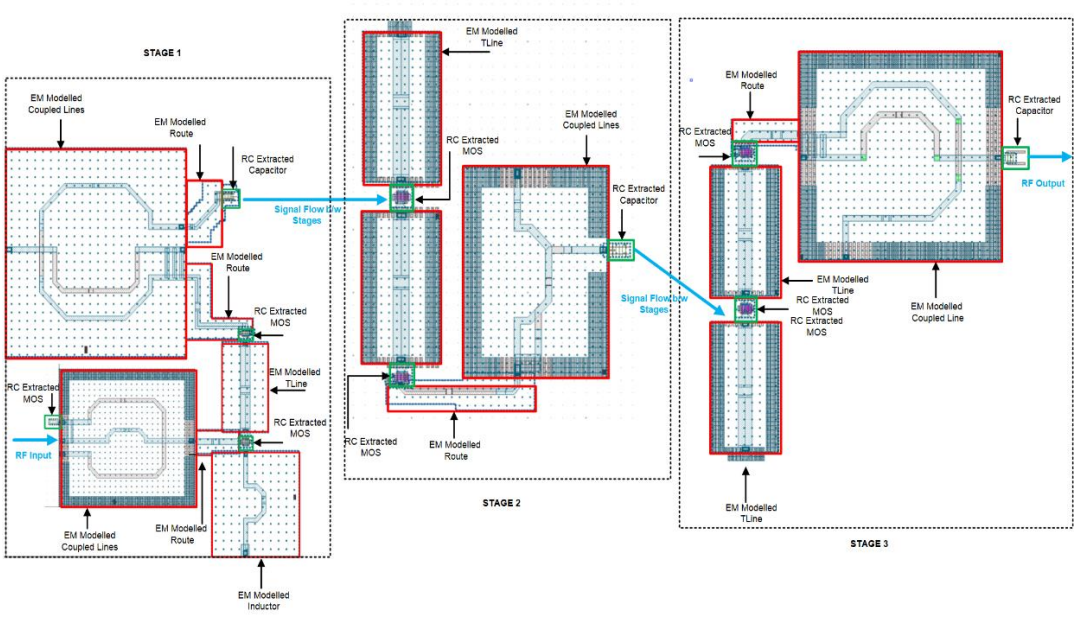


Fig. 4.2. Layout design for amplifier A depicting EM modelled and RC extracted blocks

The layout for every stage of amplifier in design A, specifying the EM modelled and RC extracted blocks, is included in Fig. 4.2. The post layout results are summarized in Table 4.1. With a supply voltage of 1V, this design consumes a power of 33.4 mW. The transistors are biased at optimum current density, and the design achieves the lowest noise figure of 2.7 dB and a peak gain of 19.8 dB, within the frequency range of 27 GHz. Figure 4.3 includes all the obtained simulation results.

Table 4.1. Performance summary for design A

Parameter	***Results***
Bandwidth (f_{BW})	27 GHz
Lowest Noise Figure	2.7 dB
Peak Gain (S_{21})	19.8 dB
Input Match (S_{11})	< -8 dB
Output Match (S_{22})	< -5 dB
Power Consumption (P_{DC})	33.4 mW

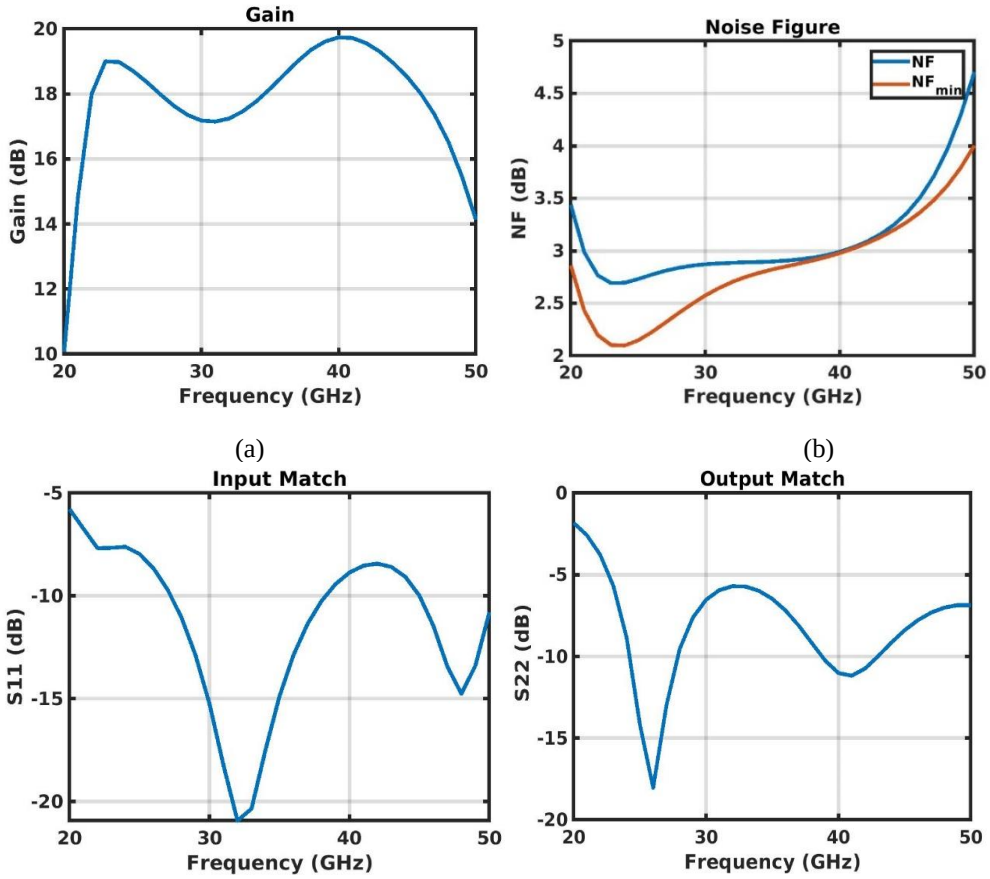


Fig.4.3. Post-layout simulation results for design A

4.1.2 Design B: Single Ended Input to Differential Outputs

Figure 4.4 provides the layout for design B amplifier, depicting EM modelled and RC extracted networks. The post layout results are summarized in Table 4.2. With a supply voltage of 1V, this design consumes a power of 33.4 mW. The transistors are biased at optimum current density, and the design achieves the lowest noise figure of 1.8 dB and a peak gain of 18 dB, within the frequency range of 27 GHz. Figure 4.5 depicts all the obtained simulation results.

Table 4.2. Performance summary for design B

Parameter	***Results***
Bandwidth (f_{BW})	27 GHz
Lowest Noise Figure	1.8 dB
Peak Gain (S_{21})	18 dB
Input Match (S_{11})	< -8 dB
Output Match (S_{22})	< -8 dB
Power Consumption (P_{DC})	33.4 mW

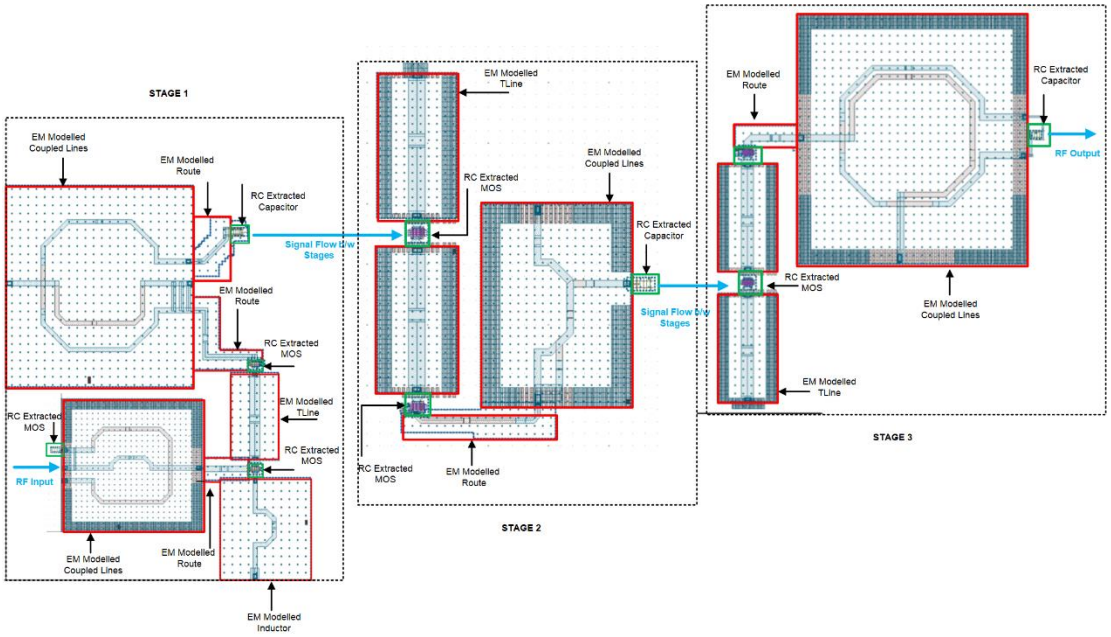


Fig. 4.4. Layout design for amplifier B depicting EM modelled and RC extracted blocks

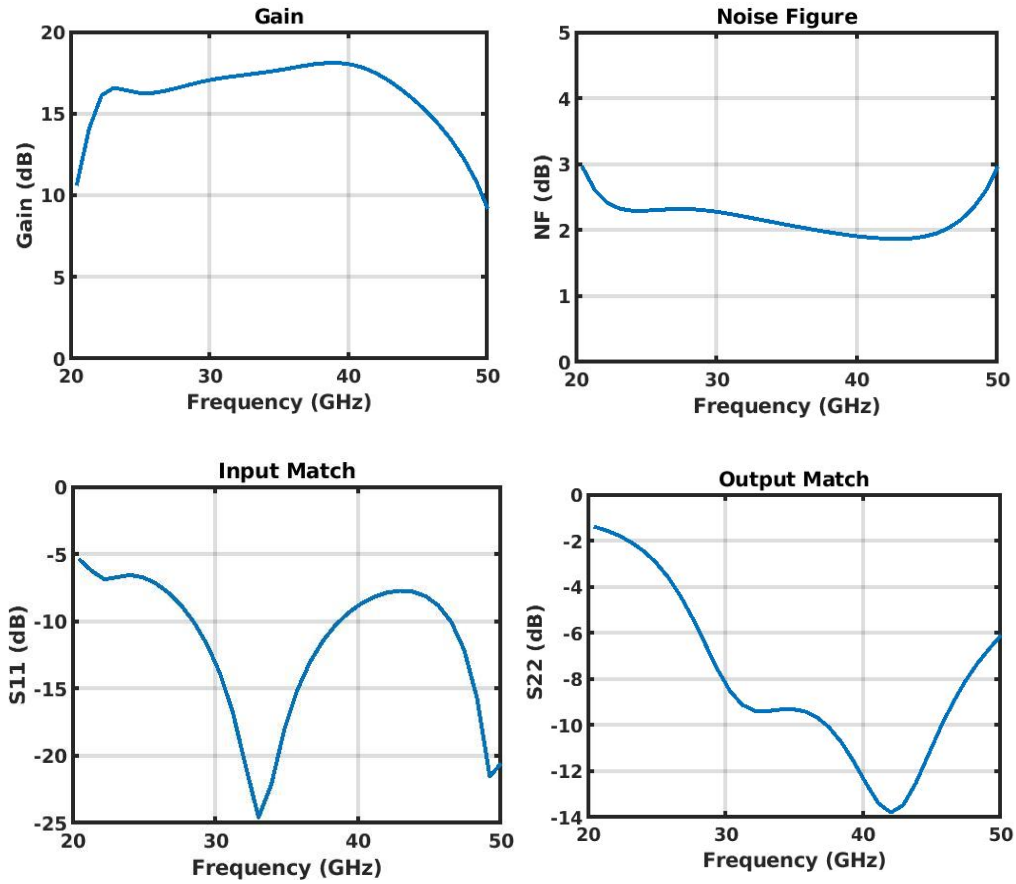


Fig.4.5. Post-layout simulation results for design B

4.1.3 Comparison to State-of-Art for Wideband LNAs at mm-Wave

Table 4.3 summarizes the performance of amplifiers operating at center frequencies ranging from 20GHz to 40GHz, with a bandwidth of more than 10GHz [48]. The data provided in table 4.3 are the measurement results of prior works.

Table 4.3. Performance summary of wideband LNAs

Ref.	***Technology***	***f (GHz)***	***BW (GHz)***	***NF (dB)***	***S11 (dB)***	***S21 (dB)***	***V_{DC} (V)***	***P_{DC} (mW)***
[15]	45nm	32.5	31	2.8	-10	21	1.5	25
[37]	22nm	27	10	1.7	-10	21.5	1.05	17.3
[38]	28nm	30.55	15.3	2.65	-10	14.5	0.9	18.9
[39]	22nm	26.5	15.1	1.46	-4	12	1.3	9.8
[40]	22nm	30	20	3.1	-9	17	1.6	20.5
[41]	28nm	32.6	20.8	3.5	-10	21.1	1	22.3
[42]	22nm	32	24	3.3	-8	23	1	20.5
[43]	45nm	30	20	2.5	-10	21.2	1	18
[44]	22nm	27.2	11.6	2.65	-5	7.8	0.8	6
[45]	65nm	29.05	22.1	3.1	-10	13.5	1.2	6.36
[46]	45nm	36.5	19	2.4	-10	21.2	1.3	25.5
Design A	22nm	35	27	2.7	-8	19.8	1	33
Design B	22nm	35	27	1.8	-8	18	1	33

4.2 Transistor Design for Low Noise

The NF_{min} of transistor device is directly proportional to its gate resistance [25]. Thus, R_g must be kept minimum to achieve lowest NF_{min}.

The NF_{min} of three different layout designs of a transistor of width 46um has been compared to study the impact of R_g on NF_{min}. These layout designs vary either in number of parallel gate finger, total gate width, number of parallel transistors, or metal interconnects for *D*, *S* and *G*.

4.2.1 Layout A

An n-type transistor of width 46 um, with gate width per finger of 360 nm, 32 gate fingers, total gate width of 11.52 um, and 4 parallel transistors, has been laid out using lower metals M_2 and M_3. Figure 4.6 shows the layout structure.

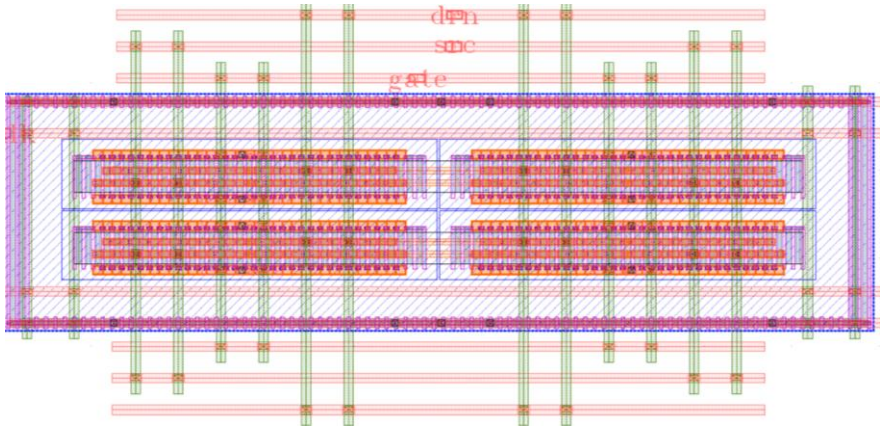


Fig. 4.6. Layout design with 11.52 um gate width and 4 parallel transistors

S-parameter analysis on the parasitic extracted model of the above layout is performed to determine NF_{min} and R_g. The relation between R_g and admittance parameter (Y) is given in (4.1) [47].

$$R_g = \frac{Re(Y_{11})}{(Img(Y_{11}))^2} \tag{4.1}$$

The simulated R_g was 14Ω, and NF_{min} variation with frequency is depicted in Fig. 4.7. In comparison to the native transistor, the addition of layout parasitic for layout A causes an increase of 0.95dB in NF_{min}, at 35GHz.

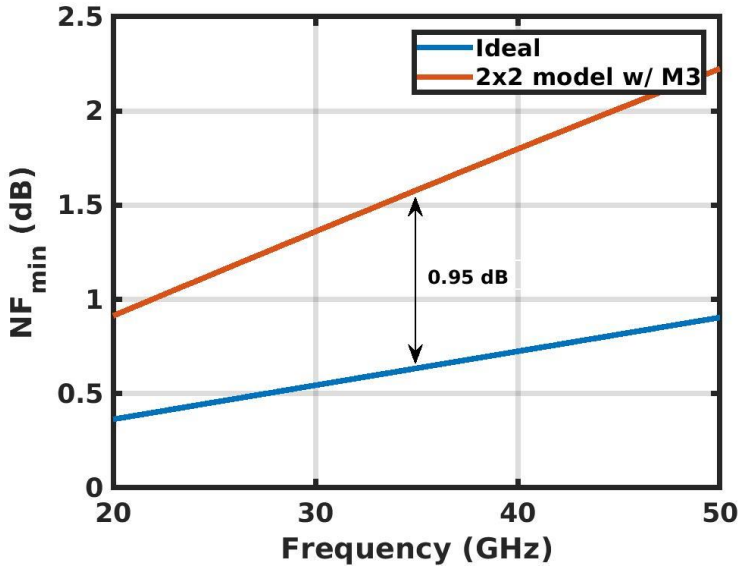


Fig. 4.7. NF_{min} performance of 4 parallel transistors with lower metal interconnects

4.2.2 Layout B

An alternate layout for the same transistor of width 46 um is shown in Fig. 4.8, with gate width per finger of 360 nm, 8 gate fingers, total gate width of 2.88 um, and 16 parallel transistors, with interconnect using lower metals M_2 and M_3. Since there are more parallel interconnect, a lower R_g is expected compared to layout A.

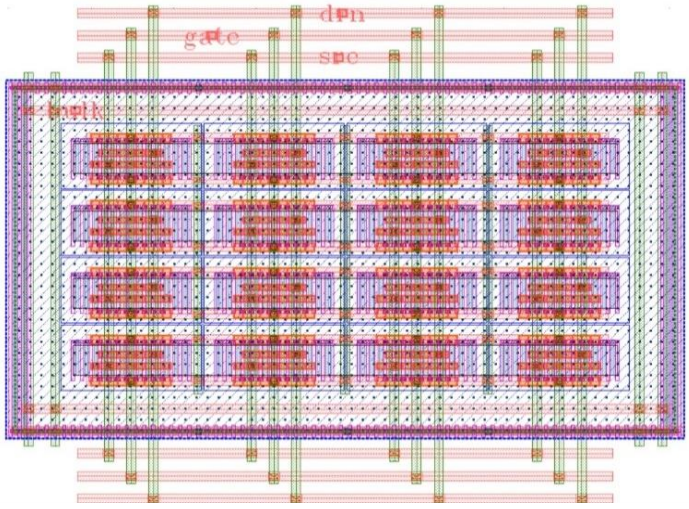


Fig. 4.8. Layout design with 2.88 um gate width and 16 parallel transistors

A reduced R_g of 13Ω, and an increased NF_{min} was observed through simulations. The results are included in Fig. 4.9. At 35GHz, the NF_{min} has increased by 1.06 dB in comparison to ideal model, and by 0.11dB in comparison to layout A. While the parasitic resistance, R_g, does decrease by adopting a parallel transistor structure, the NF_{min} performance degrades.

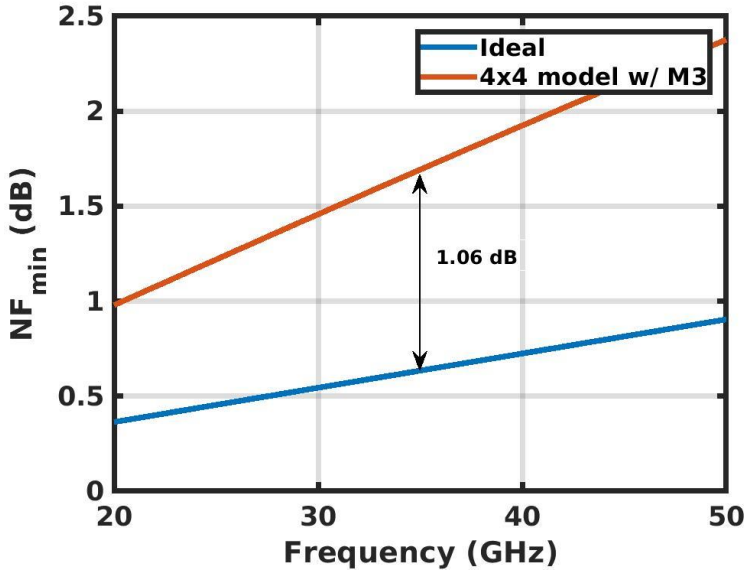


Fig. 4.9. NF_{min} performance of 16 parallel transistors with lower metal interconnects

4.2.3 Layout C

In third prototype, thick top metals which have the lowest sheet resistance were used close to the transistor in layout. The layout for the n-type transistor of width 46 um, with gate width per finger of 360 nm, 8 gate fingers, total gate width of 2.88 um and 16 parallel transistors, has been shown in Fig. 4.10. Transistors are placed closely to minimize the amount of metal lines needed to form the parallel connections.

The R_g in this case is reduced to 3Ω, and the NF_{min} of the layout, which includes parasitics, only increases by 0.15dB, at 35GHz, compared to the native transistor. These results are shown in Fig. 4.11. The importance of minimizing parasitics and impact of R_g on NF_{min} performance is evident from the improved results.

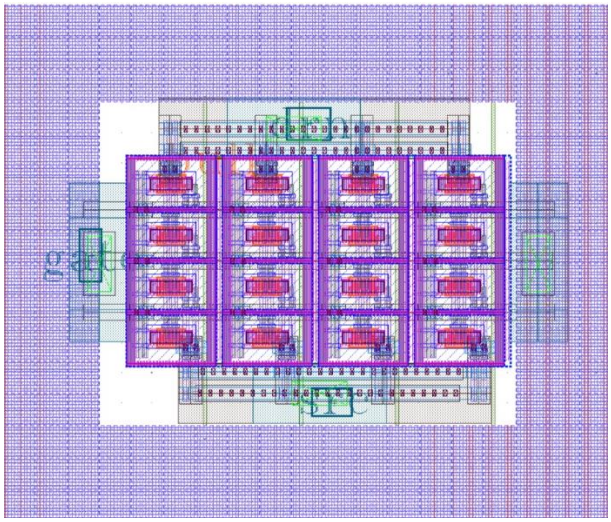


Fig. 4.10. Layout design with G,S and D interconnects in top metal layer (M8)

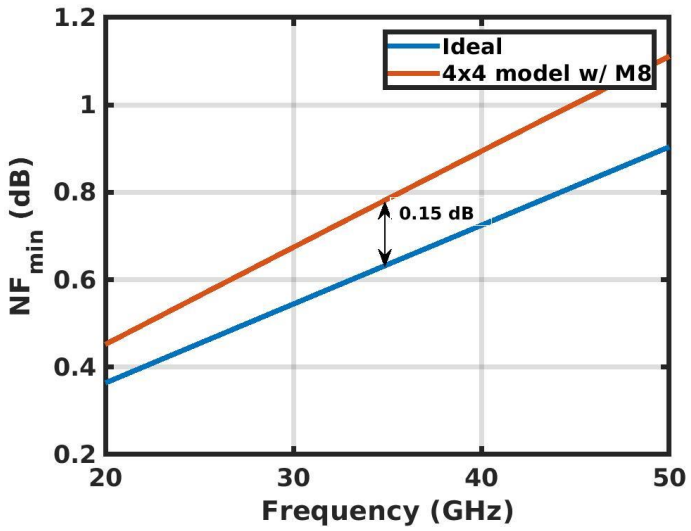


Fig. 4.11. NF_{min} performance of 16 parallel transistors with top metal interconnects

4.3 Inductor Layout

The overall LNA implementations utilizes five transformers, one inductor and one transmission line model. In the case of transformers where high coupling coefficient is desired, metal coils were separated with minimal spacing.

Inductors are modeled using the pi-model shown in Figure 4.12. The parameters in this model are generated based on EM simulations using the 3D model of inductors as

shown in Fig. 4.13 (the models are annotated with pi-model inductances and coupling values).

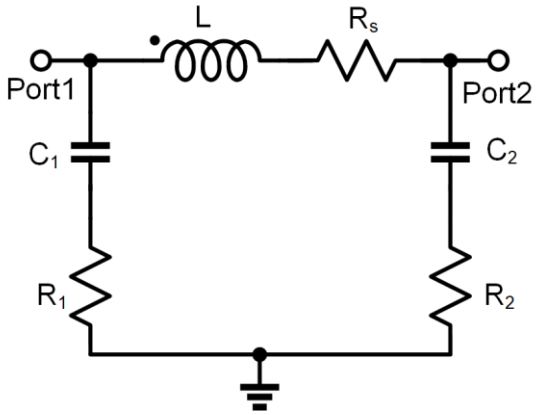


Fig. 4.12. Lumped element pi-model for inductor

Each component of this pi-model can be stated as (4.2) - (4.8), using the admittance parameters (*Y*) and frequency of observation (*f*).

$$L = \frac{img\left(\frac{-1}{Y_{21}}\right)}{2\pi f} \tag{4.2}$$

$$R_S = re\left(\frac{-1}{Y_{21}}\right) \tag{4.3}$$

$$Q = \frac{2\pi f L}{R_S} \tag{4.4}$$

$$C_1 = \frac{-1}{2\pi f . img\left(\frac{1}{Y_{11}+Y_{21}}\right)} \tag{4.5}$$

$$R_1 = re\left(\frac{1}{Y_{11}+Y_{21}}\right) \tag{4.6}$$

$$C_2 = \frac{-1}{2\pi f . img\left(\frac{1}{Y_{22}+Y_{21}}\right)} \tag{4.7}$$

$$R_2 = re\left(\frac{1}{Y_{22}+Y_{12}}\right) \tag{4.8}$$

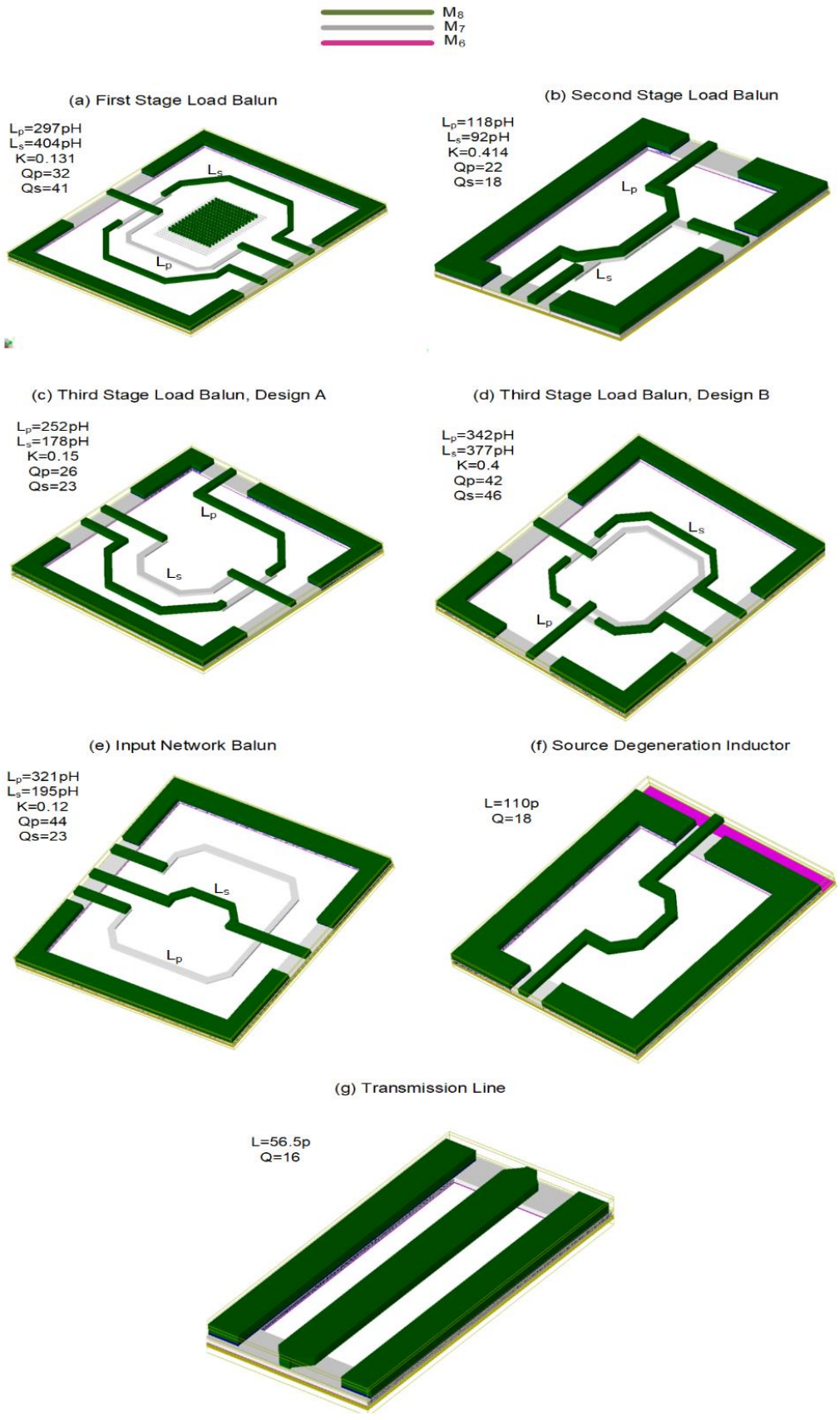


Fig. 4.13. 3D EM models and inductor parameters

Chapter 5

CONCLUSION

A systematic design methodology for mm-wave wideband LNA has been developed, based on optimum current density biasing and wideband impedance matching networks. Two amplifier designs, implemented in 22nm FFL technology, have been demonstrated in this thesis, which addresses the design challenges associated with wideband circuits operating at mm-wave frequencies. Both amplifiers utilize devices with minimum noise figure (NF_{min}) < 1dB and transit frequency (f_T) > 340GHz. The performance metrics, i.e., bandwidth and noise factor, have been enhanced by deploying dual resonance circuits as interstage networks and addition of inductor in each cascode stage, respectively.

The first design is a 3-stage cascode amplifier, with a single ended in-phase and quadrature signal path. This occupies a die area of 1.5x1.5mm^2. This amplifier achieves a peak gain of 19.8dB, a minimum noise figure of 2.7dB, and an input return loss better than 8dB, corresponding to a bandwidth of 30GHz. The second design is a 3-stage cascode amplifier, with differential in-phase and quadrature signal paths. This amplifier has been combined with a sub-harmonic mixer, and the implementation occupies a die area of 2x2mm^2. The amplifier features a peak gain of 18dB, a minimum noise figure of 1.8dB, and an input return loss better than 8dB, over a bandwidth of 30GHz.

5.1 Future Scope

The mm-wave amplifiers discussed in this thesis demonstrate that it is feasible to achieve 80 percent fractional bandwidth with sub-2dB noise figures. The future investigations would focus on examining wideband receiver designs, wherein the challenge would be to operate the mixer over such wide bands. Main emphasis would be to explore methods to reducing power consumption, both in amplifier and mixer. As a part of extension of this work, strategies of combining these amplifiers with highly programmable sub-harmonic mixers operating at 1X, 3X and 5X modes, to implement wideband low power receiver, are being explored.

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