AN ABSTRACT OF THE DISSERTATION OF

Soumya Bose for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on September 13, 2019.

Title: Energy Harvesting and Power Management Integrated Circuits for Self-Sustaining Wearables

Abstract approved: _____
Matthew L. Johnston

Harvesting energy from ambient sources can provide power autonomy to energy efficient electronics and sensors. The last decade has seen a multitude of ways to scavenge energy from various sources like solar, thermal, electromagnetic, electrostatic, piezo-electric and many more. Thermal energy from human body heat is ubiquitous and can be harnessed seamlessly across day and night. Micropower generation from human body heat using thermoelectric generators (TEG) can replace battery to power miniaturized, unobtrusive, energy-efficient wearable devices for preventive health care and vital body signs monitoring and make them self-sustainable. This thesis is focused in realizing such a system and presents different integrated power management circuit techniques to solve the primary challenges associated with energy harvesting from human body heat.

The first part of the thesis demonstrates an on-chip electrical cold-start technique to achieve low-voltage and fast start-up of a boost converter for autonomous thermal energy harvesting from human body heat. Improved charge transfer through high gate-boosted switches by means of cross-coupled complementary charge pumps en-

ables voltage multiplication of the low input voltage during cold start. The start-up voltage multiplier operates with an on-chip clock generated by an ultra-low-voltage ring oscillator. The proposed cold-start scheme implemented in a general-purpose 0.18 µm CMOS process assists an inductive boost converter to start operation with a minimum input voltage of 57 mV in 135 ms, while consuming only 90 nJ of energy from the harvesting source, without using additional sources of energy or additional off-chip components.

A single-inductor, self-starting and efficient low-voltage boost converter is described next, suitable for TEG-based body-heat energy harvesting. In order to extract maximum energy from a thermoelectric generator (TEG) at small temperature gradient, a loss-optimized maximum power transfer (LO-MPT) scheme is proposed that enables the harvester to achieve high end-to-end efficiency at small input voltages. The boost converter is implemented in a 0.18 µm CMOS technology and achieves above 75% efficiency for a matched input voltage range of 15 mV-100 mV, with a peak efficiency of 82%. Enhanced power extraction enables the converter to sustain operation at an input voltage as low as 3.5 mV. In addition, the boost converter self-starts in 252 ms with a minimum input voltage of 50 mV utilizing a dual-path architecture and a one-shot cold-start mechanism.

The final section demonstrates a self-sustainable system where a low-power signal conditioning front-end with a unique dynamic threshold tracking loop is designed to decode heart beats from a noisy ECG signal and is powered by human body heat utilizing an autonomous DC-DC converter embedded in the same chip and an off-chip centimeter-scale TEG.

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Energy Harvesting and Power Management Integrated Circuits for Self-Sustaining Wearables

by

Soumya Bose

A DISSERTATION

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Soumya Bose, Author

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TABLE OF CONTENTS

Page

1 Introduction 1

1.1 Organization 3

2 Power Management Integrated Circuits and Energy Harvesting 6

2.1 Introduction 6

2.2 Linear voltage regulators 7

2.3 Switching voltage converters 11

2.3.1 Switched capacitor DC-DC boost converter 11

2.3.2 Switching inductor DC-DC boost converter 16

2.4 Energy harvesting 19

2.4.1 Sources of energy 20

2.4.2 Thermal energy harvesting 21

2.4.3 Thermal energy harvesting from human body-heat 23

2.4.4 Primary challenges 24

2.5 State-of-the-art thermoelectric energy harvesting 25

3 Integrated Low-voltage Cold-start of a Boost Converter 28

3.1 Proposed one-shot cold start operation 29

3.2 Ultra-low-voltage ring oscillator 31

3.2.1 Limitations of CMOS inverter as delay element 32

3.2.2 Proposed delay element 34

3.3 Start-up voltage multiplier 37

3.3.1 Limitation of conventional charge pumps 37

3.3.2 Proposed cross-coupled complementary gate boosting 39

3.3.3 Non-overlapping boosting of gate clocks 45

3.4 Strobe generation and one-shot start-up 46

3.5 Measurements 50

3.6 Chapter summary 59

4 High Efficiency, Low-Voltage, and Self-Starting Boost Converter 60

4.1 Proposed self-starting boost converter architecture 61

4.1.1 Low-voltage self-start 61

4.1.2 Losses of a boost converter and maximum power transfer . . . 66

TABLE OF CONTENTS (Continued)

Page

4.1.3 Loss-optimized Maximum Power Transfer (LO-MPT) 72
4.2 Circuit Implementations 75
4.2.1 Ultra low-voltage integrated cold-start 75
4.2.2 Zero current switching for high-efficiency synchronous boost converter 79
4.2.3 Variable clock generation for LO-MPT 82
4.2.4 Dual-path operation and output voltage regulation 83
4.3 Measurements 84
4.4 Chapter summary 95

5 Batteryless Heartbeat Detection System Powered by Human Body Heat . . 96
5.0.1 Proposed batteryless heartbeat detection system-on-chip . . . 96
5.0.2 Integrated power management unit for harvesting body heat . 97
5.0.3 Heartbeat detection from a wearable perspective 98
5.1 Measurements 102
5.2 Chapter summary 106

6 Conclusion 108
6.1 Future directions 110

Bibliography 111

LIST OF FIGURES

Figure		Page
1.1	Increase in usage of wearable devices for healthcare [Source: Accenture 2018 consumer survey on digital health].	1
1.2	Self-sustainable body area network by energy harvesting.	2
2.1	(a) Model circuit of a linear regulator, and (b) simple circuit topology of LDO.	8
2.2	Stability of LDO with varying load current.	10
2.3	Dickson charge pump.	12
2.4	Improved charge transfer through boosted gate drive switches in dual phased Dickson charge pumps [1].	13
2.5	Enhanced charge transfer by dynamic biasing of CTSs [2].	14
2.6	Equivalent circuit of an N stage charge pump [3].	15
2.7	(a) Switching inductor boost converter, and (b) critical voltage and current waveforms of the converter.	17
2.8	(a) Asynchronous boost converter, and (b) synchronous boost converter.	18
2.9	(a) Continuous conduction mode (CCM) operation, and (b) discontinuous conduction mode (DCM) operation.	19
2.10	Construct of a thermoelectric generator.	22
2.11	Equivalent electrical model of a TEG.	22
2.12	Power interface circuit in a thermoelectric energy harvester utilizing human body-heat.	23
2.13	Input impedance matching for maximum power transfer from TEG to the boost converter.	25
3.1	(a) Proposed integrated cold-start architecture, and (b) timing diagram of the cold-start sequence utilizing a fast-falling edge of a strobe pulse for quick triggering of the primary inductive boost converter.	30
3.2	Low output voltage rail of a CMOS inverter at low supply.	33

LIST OF FIGURES (Continued)

Figure		Page
3.3	(a) Ultra Low-voltage ring oscillator comprising the proposed stacked-inverters based delay cells, and (b) Leakage current suppression in the delay cell in charging and discharging phases.	35
3.4	Simulated VTC of the proposed delay cell shows improvement of DC gain and output voltage rails over conventional CMOS inverter.	36
3.5	Loading effect in high gate boosting by borrowing voltages from much later stages.	38
3.6	Proposed start-up voltage multiplier, using cross-coupled complementary charge pumps for high gate-boosting and low voltage operation.	40
3.7	Mutual voltage boosting of gate clocks borrowing dual phased outputs of complementary charge pumps.	42
3.8	(a) Generation of non-overlapping gate clocks with boosted voltage swing, and (b) timing diagram for gate clock generation.	44
3.9	(a) Circuit schematics of the strobe generation unit (SGU) with simulated current consumption of each functional blocks, (b) simulated waveforms showing functionality of the SGU.	47
3.10	(a) Die photo of the chip fabricated in 0.18 µm CMOS technology, (b) experimental set up for measurements with commercial TEG attached to human body.	50
3.11	Measured start-up clock generated by the ultra-low-voltage ring oscillator.	51
3.12	Measured transient waveform of V_{CP} (buffered off-chip) with an input supply of 55 mV.	52
3.13	Measured non-overlapping gate clocks with boosted voltage swing.	53
3.14	Measured pumping efficiency and output power of the charge-pump-based voltage multiplier across input voltages.	53
3.15	Measured start-up transient of the proposed cold-start architecture. Zoomed waveform showing triggering of the primary converter with the fast falling edge of strobe pulse, V_{ST}.	54

LIST OF FIGURES (Continued)

Figure Page

3.16 Current drawn from source by the cold-start block at various input voltages 56

3.17 Measured transient of the boost converter with a commercial TEG. . 57

4.1 Proposed high-efficiency single-inductor thermoelectric energy harvester with low-voltage integrated one-shot cold-start utilizing dual-path architecture. 62

4.2 Operation of the boost-converter in (a) phase 1, (b) phase 2, (c) phase 3, and (d) phase 4. 64

4.3 (a) Operation of a boost converter in discontinuous conduction mode (DCM), and (b) Power loss of the converter normalized with respect to input power with varying switching frequency. 67

4.4 (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT. 71

4.5 (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT. 73

4.6 (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT. 75

4.7 (a) One-shot start-up with the proposed on-chip voltage multiplier, and (b) high dual gate-boosting using internal voltages and combination of NMOS and PMOS switches. 76

4.8 Generation of one-shot powered by the output voltage of the charge pump. 79

4.9 (a) Implementation of zero current switching (ZCS) using digital sensing along with the sub-blocks of the delay line, and (b) timing diagram showing operation of ZCS. 80

LIST OF FIGURES (Continued)

Figure Page

4.10 (a) Implementation of loss-optimized maximum power transfer (LO-MPT) using digital circuits, and (b) timing diagram showing adaptive on-time and frequency of switching clock for optimizing loss of the converter while ensuring maximum power transfer at input. 82

4.11 Printed circuit board (PCB) with chip-on-board for testing. Die photograph of the chip fabricated in 0.18 µm CMOS technology is shown in the right. 85

4.12 (a) Measured start-up transients shows cold-start of the harvester: from the input turned on to reaching a regulated output voltage of 1.2 V, with a minimum input voltage of 50 mV in 252 ms, and (b) zoomed waveform shows one-shot triggered cold-start sequences including parllel asynchronous - synchronous operation of the single inductor boost converter. 86

4.13 Measured transients showing adaptive change of on-time and frequency of switching clock with variation of input voltage for loss-optimized maximum power transfer (LO-MPT) at the input of the converter. . . 87

4.14 Disabling the cold-start low-voltage charge pump with the activation of high-efficiency synchronous path of the boost converter. It not only improves the end-to-end efficiency of the converter, but also enables the harvester to accomodate higher input voltages without stressing devices in the high step-up charge-pump. 88

4.15 Load and line regulation of the output of the boost converter. 89

4.16 (a) Measured efficiency of the boost converter with input power and output power for varying TEG voltage, and (b) I-V plot of the output of the harvester at a fixed TEG voltage of 50 mV. The measured peak output power in plot (b) corresponds to the input power point (P) for $V_{TG} = 50\,\text{mV}$ in the plot (a). 90

4.17 Measured Transients showing operation of the converter at the smallest input voltage with an output regulated voltage of 1.2 V. 91

4.18 Power distribution at $V_{TG} = 15\,\text{mV}$: (a) measured power with estimated loss, and (b) simulated control power break-up. 91

LIST OF FIGURES (Continued)

Figure Page

4.19 (a) Measurement setup with commercial TEG, and (b) measured transient of the harvester. 93

5.1 Block diagram of the human body heat powered, motion-resilient heartbeat monitoring system-on-chip. 97

5.2 Proposed adaptive voltage reference generation and tracking technique with double-sided threshold generation for robust heartbeat feature extraction in the presence of motion artifacts. 99

5.3 Implementation of adaptive threshold generation using pulse-width locked loop (PWLL). 101

5.4 Die micrograph of sensor SoC in 180 nm CMOS. 103

5.5 Measured heartbeat detection accuracy using the proposed adaptive feature extraction scheme, and comparison with a fixed-threshold approach. 104

5.6 Measured transient plots showing start-up transient of the PMU initialization of the AFE and VREFs; measured harvested power distribution for different sub-blocks at TEG input voltage of 65 mV. 105

5.7 Measurement set-up for the autonomous batteryless heartbeat detection SoC. 106

LIST OF TABLES

Table		Page
2.1	Power densities of various energy harvesting sources [4]	20
3.1	Summary of minimum operational voltage	55
3.2	Comparison with state-of-the-art cold-start voltages	58
4.1	Startup times at different source voltages	87
4.2	Performance comparison with state-of-the-art thermoelectric energy harvesters	94
5.1	Performance comparison with state-of-the-art	107

To Maa and Baba

Chapter 1: Introduction

"Your theory is crazy, but it's not crazy enough to be true."

- Niels Bohr

With the advancement of mobile technology over the last decade, the electronics industry is witnessing a surge of new portable, miniaturized electronic devices that can be worn on human body and perform various functions to improve the quality of life - *wearables*. Their functions include applications related to sports and entertainment, lifestyle, personal assistance, healthcare, and many more. In particular, there is a rapidly growing demand among consumers to wear these devices for monitoring vital signs, fitness tracking and point-of-care diagnostics [5]. A recent consumer survey on digital health [6] shown in Fig. 1.1 depicts this fascinating trend.

Portability and longer life are the most desired features of wearable devices [7]. However, lifetime of existing devices is limited by the energy available from batteries

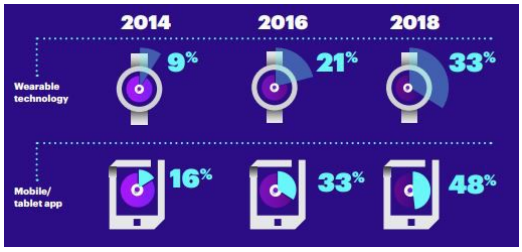


Figure 1.1: Increase in usage of wearable devices for healthcare [Source: Accenture 2018 consumer survey on digital health].

that predominantly power them. Small form-factor is a major constraint to increase usage time of battery-powered wearables. Also, with increasing demand of wireless body area network (WBAN) for ubiquitous healthcare and wellness of human beings [8, 9], more and more sensors are going to be worn to the body. Limited power and hence, lack of self-sustainability of the sensor nodes is one of the major obstacles in realizing such a system.

Energy harvesting and scavenging power from ambient sources of energy like solar, thermal, wind, or vibration, as shown in Fig. 1.2, can provide complete power autonomy to wearable sensor nodes and can help in realizing self-sustaining body area networks (BAN) [10]. Thermal energy from human body-heat is available across day and night, which makes it a potential source to power wearable devices [11]. A thermoelectric generator (TEG) can convert this thermal energy in the form of temperature difference between human skin and neigboring environment into elec-

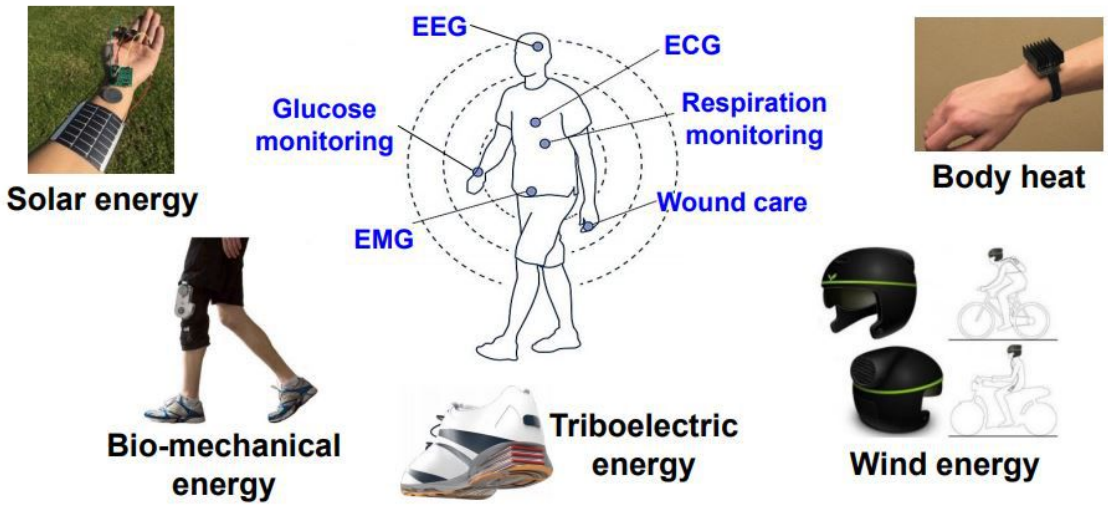


Figure 1.2: Self-sustainable body area network by energy harvesting.

trical voltage and can seamlessly power energy efficient sensors and electronics in wearables.

However, small temperature gradient between human body and environment generates only few 10s of millivolts of open circuit voltage from centimeter-scale TEGs and neccesitates a DC-DC step-up converter to boost the voltage and power the sensor electronics. Also, for maximum power transfer, the input impedance of the DC-DC converter needs to be matched with that of the TEG source, which further reduces input voltage of the converter to half of the open circuit voltage of the TEG. Low input voltage makes efficient operation of the DC-DC boost converter challenging. Also, for complete batteryless operation, the converter must self-start with the small voltage of the TEG.

This dissertation presents new circuit techniques to achieve low-voltage self-start and efficient operation of DC-DC boost converters at small input voltages without using multiple off-chip inductors or bulky transformers. The applicability of the proposed converter architecture is demonstrated by implementing a batteryless heart rate monitor powered by harvested energy from human body heat.

1.1 Organization

A brief overview of basic power management circuit blocks in the context of energy harvesting applications is presented in Chapter 2. This is followed by explanations showing advantages of thermoelectric energy harvesting using human body heat over other harvesting sources for powering wearable devices. A description of the operat-

ing principle of thermoelectric generators (TEGs) is provided next. The fundamental challenges involved in fully autonomous thermoelectric energy harvesting from human body heat is explored. The chapter is concluded with a comprehensive literature survey showing state-of-the-art and neccessity for further research investigation.

Chapter 3 demonstrates an integrated start-up mechanism to achieve low voltage cold-start of a DC-DC converter. Section 3.3 describes the limitations of CMOS inverter-based ring oscillators under reduced supply voltages and explains operation of a new stacked-inverter-based delay element. The subsequent sections of this chapter elaborate shortcomings of conventional charge pumps for on-chip voltage multiplication at reduced input supply voltage and demonstrate operation of a cross-coupled complementary charge pump to achieve higher pumping efficiency at ultra-low input voltages. Along with the detailed circuit architectures of the key building blocks of the proposed start-up regime, the chapter also presents design considerations and extended block-level electrical characterization of the implemented IC.

A single-inductor, self-starting boost converter architecture is presented in Chapter 4 suitable for low voltage thermoelectric energy harvesting. A dual path architecture is demonstrated which utilizes the basic idea of one-shot start-up mechanism described in the previous chapter to start a high efficiency synchronous boost converter. A loss-optimized maximum power transfer (LO-MPT) scheme implemented with energy-efficient control circuits is elaborated that helps in achieving high end-to-end efficiency of the harvester by improving efficiency of the DC-DC converter while ensuring maximum power transfer at input. Later sections of this chapter describe design details of the circuit blocks and performance measurement of the fabricated

prototype.

The potentiality of thermoelectric energy harvesting using body-heat is demonstrated in Chapter 5 by powering a heartbeat monitoring system. It describes the complete implementation of the system comprising a low-power analog front end for ECG signal acquistion, a dynamic threshold generation loop for detecting heartbeats from a noisy ECG, and the embedded power interface circuits to power the whole system with the available thermoelectric energy of a TEG mounted on human skin.

Chapter 2: Power Management Integrated Circuits and Energy Harvesting

2.1 Introduction

Integrated electronics are dead without power supplies. With increasing complexity of electronic systems in the generation of internet of things and artificial intelligence, more and more circuit blocks are embedded into the same chip, requiring multiple voltage levels for efficient and seamless operation. Power management deals with the generation of these supply voltages and regulating them based on the individual requirements of the operating loads. Integrated circuits like linear regulators, switching regulators, and voltage references are the key building blocks of power management. Each of these are essentially control circuits that transfer power across voltage domains. Thereby, the fundamental parameter to evaluate the performance of these circuit blocks is the power efficiency (η) which is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss} - P_{ctl}}{P_{in}}, \tag{2.1}$$

where P_{in} denotes the input power, P_{out} is the net available output power, P_{loss} is the lost power and P_{ctl} is the power consumed by the control circuits. Modes of operation make one of them advantageous over the other from application to application.

In energy harvesting, a transducer converts energy from the ambient source to

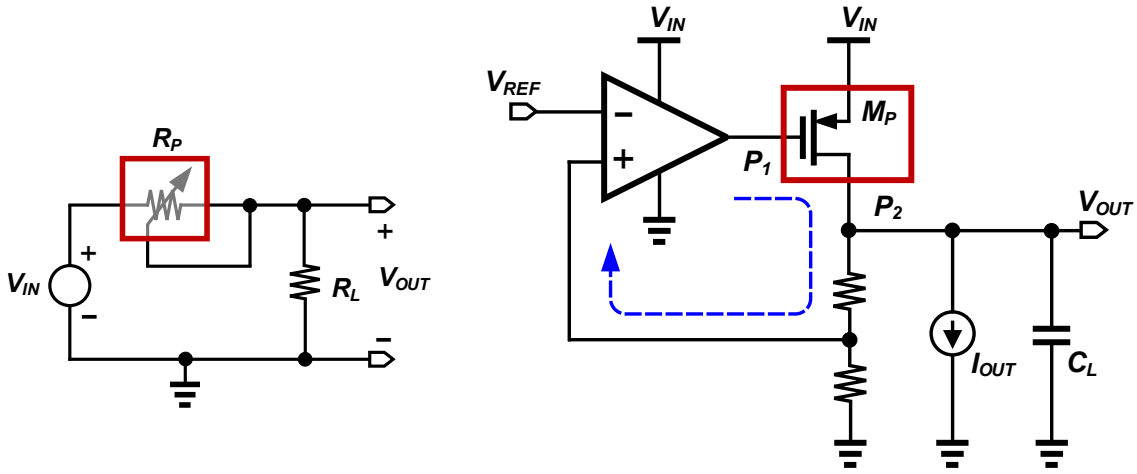
electrical energy in the form of voltage and current. Based on the availability of energy, the generated voltage or current fluctuates and thereby requires regulation to power electronic circuits. In addition, voltage level of the transducer may not be high enough for the operation of integrated electronics in state-of-the-art semiconductor technology and needs additional power conditioning circuits for voltage conversion. This makes power management integrated circuits an integral part of energy harvesters.

In this chapter the basic operating principle of some of the key integrated circuit blocks for power management are revisited with a brief overview of their application in energy harvesters. The latter half of the chapter elaborates thermoelectric energy harvesting as a useful alternative to battery for powering self-sustaining wearables and the associated challenges.

2.2 Linear voltage regulators

In this type of regulator only a low voltage (V_{OUT}) can be generated at the output from a higher input voltage (V_{IN}). The variation of V_{IN} is compensated by continuously varying the resistance (R_P) of a pass element, as shown in Fig. 2.1a, to regulate V_{OUT}. The pass element can be realized utilizing a transistor operating in the linear mode. The resistance of the transistor (M_P) is varied by controlling the gate voltage based on small variation of V_{OUT} sensed by an opamp placed in negative feedback (Fig. 2.1b).

Usage of small number of transistors and relatively simpler circuit makes this



(a) (b)

Figure 2.1: (a) Model circuit of a linear regulator, and (b) simple circuit topology of LDO.

regulator the most widely used voltage regulator in integrated circuits. However, continuous flow of current (I_{OUT}) through the pass element increases the power dissipation [$(V_{OUT} - V_{IN}) \times I_{OUT}$] in the conduction path at higher orders of step-down ($V_{OUT} > V_{IN}$) and causes the topology to be extremely inefficient. A variant of this regulator that operates with small voltage drop across the pass transistor in an efficient way, known as a low-dropout regulator or LDO, is more widely used to generate stable V_{OUT} close to the value of V_{IN}.

The key design considerations of linear regulators are quiescent current, stability across load currents, line and load regulation, output transient for changing load current or line voltage, and power supply rejection ratio (PSRR).

The quiescent current or ground current (I_Q) accounts for the efficiency of the

regulator as

$$\eta = \frac{V_{OUT} I_{OUT}}{V_{IN}(I_{OUT} + I_Q)}. \tag{2.2}$$

The lower the I_Q, the higher is the efficiency. When I_Q remains nearly constant across the load, the regulator is more efficient at higher load compared to low load.

For linear regulator, being a negative-feedback system, stability across the varying load current is an important concern. A simple regulator as in Fig. 2.1a can be modelled as a two-pole system where the first pole, ω_{P1}, is formed at the gate of the pass transistor (M_P) and the second pole, ω_{P2}, is formed at the output such that

$$\omega_{P1} = \frac{g_{amp} . g_{ds,P}}{g_{m,P} . C_{gd,P}} \propto \sqrt{I_{OUT}} \qquad \text{and} \qquad \omega_{P2} = \frac{g_{ds,P}}{C_{OUT}} \propto I_{OUT} \tag{2.3}$$

It indicates that for smaller I_{OUT}, one of the poles decreases by higher amount than the other, as shown in Fig. 2.2, and comes closer to each other, affecting stability. Although a large off-chip C_{OUT} can easily stabilize the negative feedback, the issue becomes more complex for small C_{OUT} or fully integrated cap-less LDOs [12].

This is measured by evaluating the variation of the V_{OUT} with the change in I_{OUT}:

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{2.4}$$

which is effectively the output impedance (R_{OUT}) of the regulator. Due to the negative feedback of the opamp, the R_{OUT} remains lower as long as the feedback stays active.

The line regulation is defined as the variation of V_{OUT} with the fluctuation of

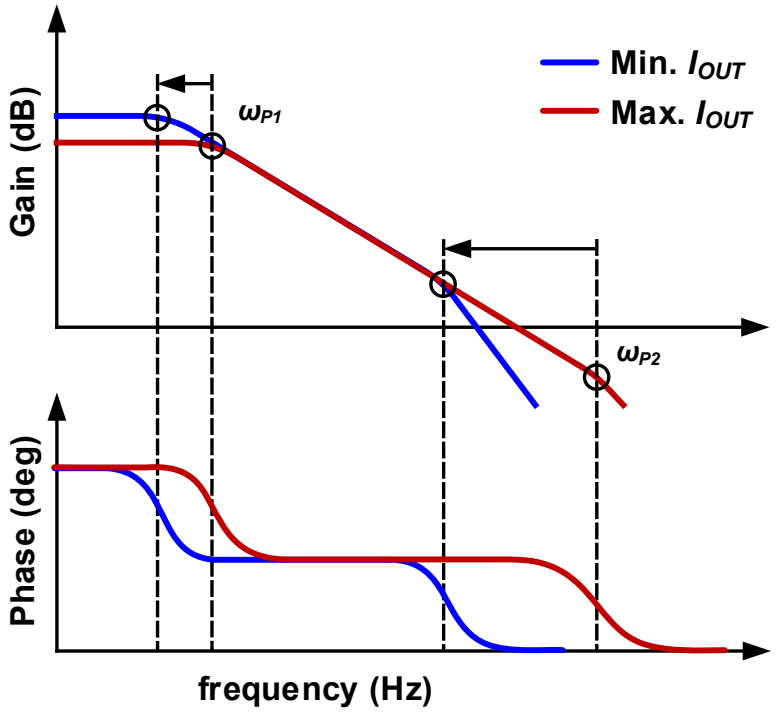


Figure 2.2: Stability of LDO with varying load current.

V_{IN}. While the term line regulation is mostly used for large signal variation, PSRR determines voltage ripples at output, V_{OUT}, due to small signal variation at the input, V_{IN}, and is measured across frequency as

$$PSRR = 20 \log_{10} \left(\frac{dV_{IN}}{dV_{OUT}} \right) \tag{2.5}$$

Compared to PMOS pass transistors, NMOS transistors can provide a better PSRR, especially at higher frequencies, but need additional higher supply voltage for gate drive [13].

Output transient of the regulator depends on the slewing of the output stage and

bandwidth of the closed-loop feedback. During high transitions of load current, the initial part of the transient is controlled by the large signal response of the output stage, which varies with the biasing current. Once the output voltage comes closer to the desired output voltage, the negative feedback bandwidth takes care of the transient.

2.3 Switching voltage converters

The biggest disadvantage of the linear regulator is its inability to boost the input voltage. For applications which need a step-up (boost) in voltage domain, switching regulators are the only option. Switching voltage converters can do both step-up (boost converter) or step-down (buck converter) of voltage level utilizing storage elements like inductors or capacitors. This section is focused on boost conversion, primarily because of its importance in energy harvesting applications.

2.3.1 Switched capacitor DC-DC boost converter

Switched capacitor based dc-dc voltage boosting circuits, also known as charge pumps, started gaining popularity with the invention of Dickson charge pump [14], which showed the possibility of integrating the converter in CMOS technology. Historically, these on-chip voltage multipliers were extensively used for high-voltage biasing of non-voltatile memories [15, 16]. However, with their improving efficiency and ability for on-chip integration, thanks to the high-density capacitor implementation in modern CMOS processes, switched capacitor based voltage multipliers are

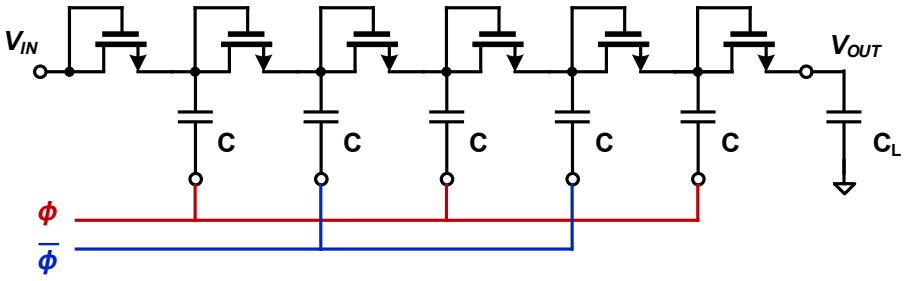


Figure 2.3: Dickson charge pump.

extensively used nowadays in energy harvesters and power converters [17, 18].

The Dickson charge pump as shown in Fig. 2.3 boosts the output voltage, V_{OUT}, by charging multiple stages of capacitors in alternate clock phases. The diode connected MOS switches which are used for transferring charge from one stage capacitor to the next suffer from threshold voltage drop, and the final output voltage V_{OUT} of an N-stage charge pump is limited to:

$$V_{OUT} = (N+1).V_{IN} - N.V_{th} \tag{2.6}$$

where V_{th} is the threshold voltages of the transistors.

Charge transfer between successive stages of the voltage multiplier can be improved by using cascaded Dickson charge pumps in dual phases as shown in Fig. 2.4 [1]. Such a cross-coupled structure can provide a gate-source voltage equal to the voltage swing of the clock, V_{CK}, to turn the charge-transfer switches (CTS) on during the charge transfer phase. It works efficiently with higher input supply voltage when $V_{CK}(= V_{IN})$ is higher than V_{th} of the transistors and the CTSs are completely turned on during the charge transfer phase. With V_{IN} less than 100 mV, the low V_{CK} will

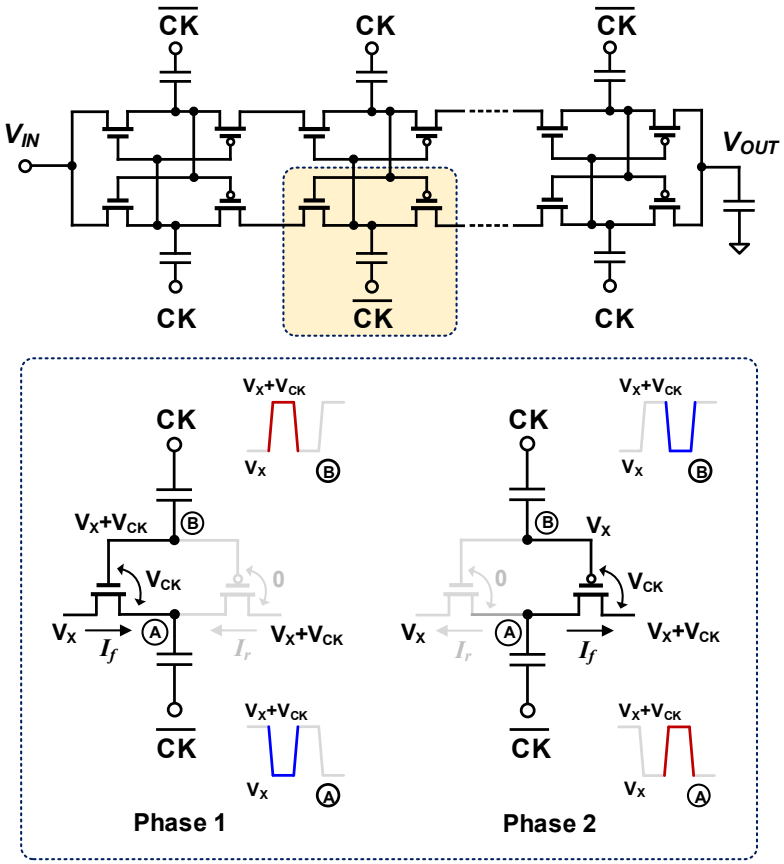


Figure 2.4: Improved charge transfer through boosted gate drive switches in dual phased Dickson charge pumps [1].

turn on the CTSs so weakly that the resulting forward current, I_F, is comparable to reverse leakage current, I_R. This causes ineffective charge transfer between successive stages and significantly reduces the pumping efficiency of the charge pump.

In order to improve pumping efficiency of the charge pump at low input voltage, CTSs are dynamically biased in [2] where boosted voltages are borrowed from higher stages to generate a gate-source voltage of $2V_{CK}$, as shown in Fig. 2.5. As a result, CTSs are better turned on during the charge transfer phase.

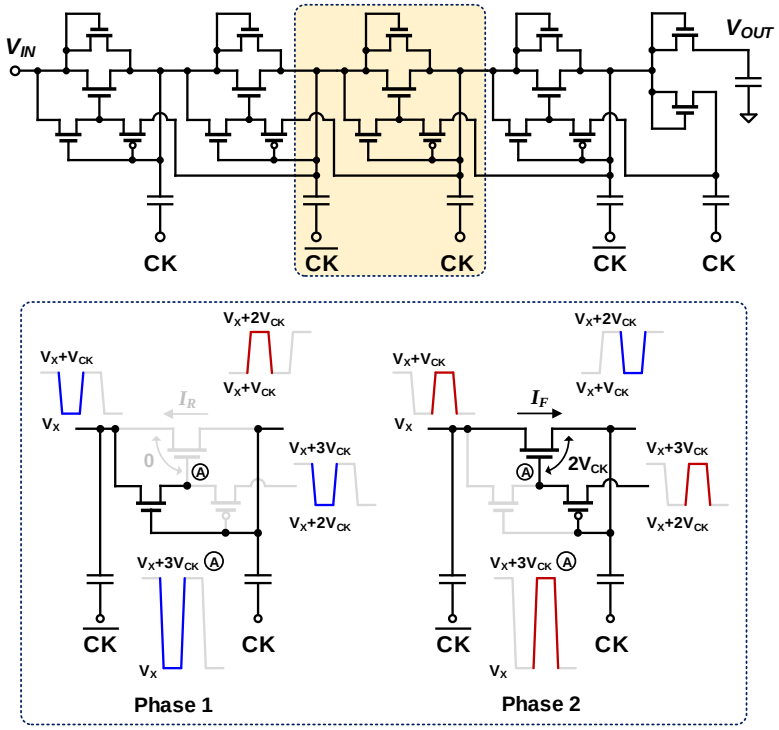


Figure 2.5: Enhanced charge transfer by dynamic biasing of CTSs [2].

The charge pump can be modelled as a transformer, as shown in Fig. 2.6, transfering power from low voltage V_{IN} to high voltage V_{OUT} [3]. The output impedance is ideally equal to $N/(Cf_{CK})$ when complete charge transfer occurs between successive stages. The important part of this circuit is that it shows that the charge pump has an implicit load of C_{pump} which is a function of the number of stages, N, and stage capacitance, C. It can be approximated as $NC/3$ for higher number of stages ($N \geq 4$). The important design parameters of a charge pump are area and power efficiency. For applications with capacitive loads, settling time is also important.

The output resistance of the charge pump determines its performance. Mini-

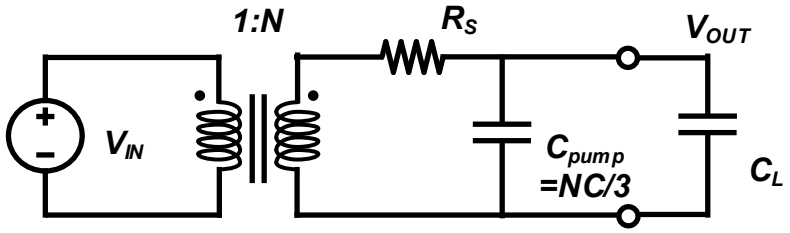


Figure 2.6: Equivalent circuit of an N stage charge pump [3].

mum output resistance results in maximum power transferred to the output. The operation of a switched capacitor DC-DC converter can be classified into two categories: a) slow switching limit (SSL) and b) fast switching limit (FSL) [19]. In SSL, the frequency of pumping is low enough to enable complete charge transfer from one-stage to the other and the R_{OUT} is dominated by $N/(Cf_{CK})$. Whereas in FSL, as the pumping frequency increases, incomplete charge transfer between capacitors makes the R_{OUT} dependent on the switch resistances. Hence, there lies a tradeoff in choosing the value of stage capacitor, and switching frequency, which varies based on applications.

The biggest challenge of the charge pump operation at very small input voltage is to improve the conductivity of the switches for efficient charge transfer. In addition, low frequency of pumping clock at small V_{IN} reduces the R_{OUT} of the charge pump in the SSL condition, effectively reducing its output power. These challenges are addressed in more detail in Chapter 3 in the context of energy harvesting.

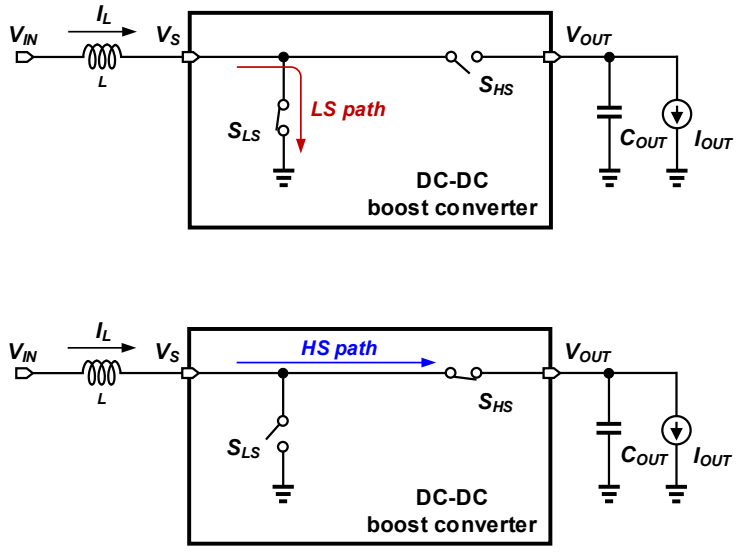
2.3.2 Switching inductor DC-DC boost converter

In an inductive switching converter for boosting V_{IN}, the inductor L is energized by flowing current from the input voltage source turning the low-side switch, S_{LS}, on as shown in Fig. 2.7a. In the complementary phase the stored energy of the inductor is fed to the output by turning on the high-side switch, S_{HS}. The output capacitor stores energy and feeds the load while the L remains disconnected from the output and refills energy from the input. The conversion ratio of V_{OUT} to V_{IN} obtained in this process can be given as,

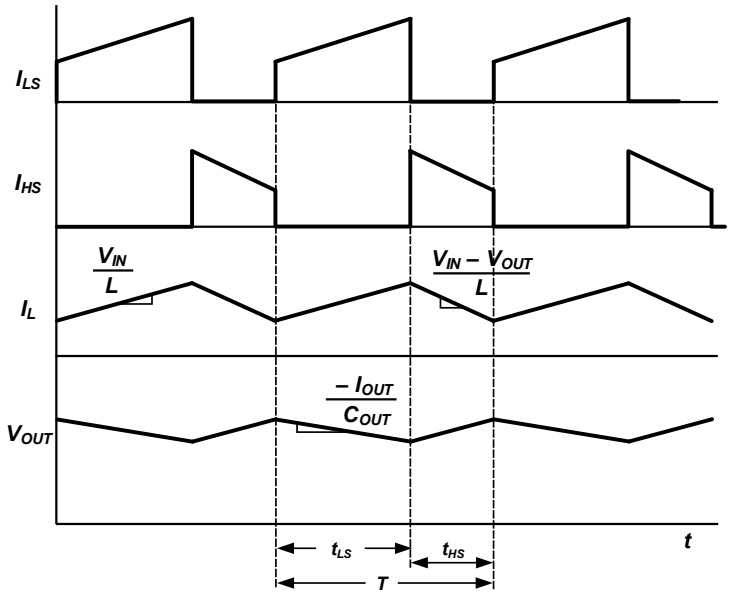
$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{t_{LS}}{t_{HS}}\right) \tag{2.7}$$

where t_{LS} and t_{HS} denotes the LS and HS conduction time.

Based on the implementation of the high-side conduction path, inductive DC-DC boost-converter can be classified into asynchronous and synchronous converters. In an asynchronous converter, as shown in Fig. 2.8a, as soon as the LS switch is turned off, the voltage at node V_S goes high due to the resonance with charged inductor and parasitic capacitor of the node (also called inductive overshoot) and turns on the diode, S_D, to transfer energy from the inductor to the output through the high-side path. While this operation makes the control circuit simple, voltage drop across S_D reduces the efficiency of the asynchronous converter. Whereas, in a synchronous converter as shown in Fig. 2.8b, a high-side switch is synchronously turned on with the closure of LS switch to transfer energy from the input to the output. Low voltage drop across the switch reduces the loss of the converter at the cost of more complexity



(a)



(b)

Figure 2.7: (a) Switching inductor boost converter, and (b) critical voltage and current waveforms of the converter.

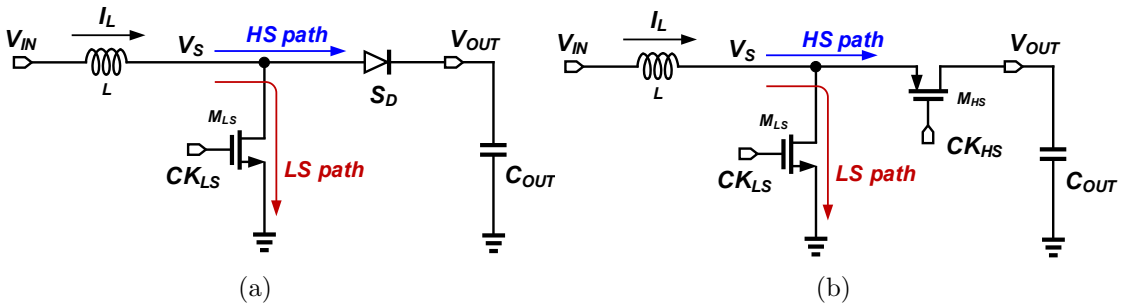


Figure 2.8: (a) Asynchronous boost converter, and (b) synchronous boost converter.

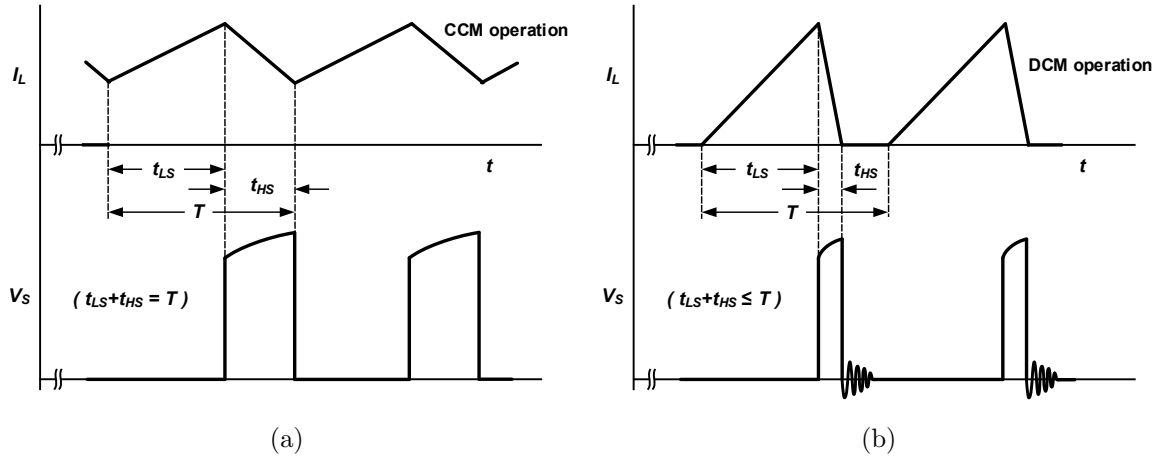
in control circuits.

Depending on the requirement of the load, the boost converter can be operated in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM, suitable for heavy loads, the inductor current never goes to zero, as shown in Fig. 2.9a. Whereas, the inductor energy is completely transferred to the output every cycle in DCM mode (Fig. 2.9b) and the inductor is kept in no conduction mode for a small part of every cycle, making it suitable for low load applications.

For applications with low input voltage and low input power, DCM mode is preferred [20]. As the input voltage is low, it requires a higher conversion ratio to get reasonable supply voltage for the load electronics. This results in higher conduction time of the low-side and more conduction losses. The input power being low, efficient operation of the DC-DC boost converter becomes challenging and results in low net output power. Chapter 4 elaborates this problem with further analysis.

2.4 Energy harvesting

The strong demand for extended lifetime of electronic devices urges new developments in power technology. Although battery technology has gone through substantial development in the past few years, it still lags in terms of integration density compared to transistors [21]. Energy harvesting can complement batteries to increase usage time of electronic devices. In particular, micropower harvesting from ambient sources can provide power-autonomy to energy efficient sensor nodes [22] or wearables for point-of-care diagnostics and biometrics, and can help in realizing self-sustaining electronic healthcare systems [11].



(a) (b)

Figure 2.9: (a) Continuous conduction mode (CCM) operation, and (b) discontinuous conduction mode (DCM) operation.

Table 2.1: Power densities of various energy harvesting sources [4]

Sources	**Power density**
Solar(outdoor)	$100\,\mathrm{mW/cm^3}$
Solar(indoor)	$100\,\mu\mathrm{W/cm^3}$
Vibration(human motion)	$4\,\mu\mathrm{W/cm^3}$
Vibration(machine)	$800\,\mu\mathrm{W/cm^3}$
Wind	$177\,\mu\mathrm{W/cm^3}$
Thermal(human body)	$60\,\mu\mathrm{W/cm^3}$
Thermal(industry)	$10\,\mathrm{mW/cm^3}$
Radio frequency (RF)	$150\,\mu\mathrm{W}$ - $2\,\mathrm{mW/cm^3}$

2.4.1 Sources of energy

Energy can be harvested from various sources present around us. Among them the commonly used sources are solar, thermal, wind, vibrational and radio-frequency (RF). The available power densities from these sources [4] in Table 2.1 gives a brief idea about their usability. Although some of the sources appear to be more powerful, their output power depends on many environmental conditions. For example, solar energy can provide high power densities but only under strong illumination during daylight [23]. Vibrational energy due to human motion is only available during motion and varies highly based on daily life. Wind energy is also dependent on environmental conditions and only available in an outdoor environment, and RF energy needs a secondary power source or electromagnetic source.

2.4.2 Thermal energy harvesting

Thermal energy in the form of wasted heat in industrial applications and automotive has been used to generate electricity [24]. Generating electric power from the thermal energy of nuclear reaction with radioisotopes is also widely used in space missions to power the electronics of the spacecrafts [25]. All of them use thermoelectric generators that converts thermal energy in the form of temperature gradient into electrical energy by means of the Seebeck effect.

Generation of electromotive force between two dissimilar metals by maintaining a temperature difference between them is known as Seebeck effect,

$$EMF = \Delta V = S\Delta T \tag{2.8}$$

where S is the Seebeck coefficient. This method is most widely used to measure temperature utilizing thermocouples. The same phenomenon is exploited to generate electric power from thermal energy using a thermoelectric generator (TEG). Semiconductor materials have significantly higher Seebeck coefficient than metals and can generate more power from a temperature gradient. As such, TEG comprises series of thermocouples made up of n-type and p-type thermoelectric elements [26] connected in series, as shown in Fig. 2.10. For the n-type element, Seebeck effect results in flow of excess electrons from the hot junction to the cold junction. Whereas, in the p-type element, holes migrate toward the cold side, generating a resultant current flow in the direction similar to that of the n-type material.

A TEG can be modelled as DC voltage source (V_{TG}) with a source resistance

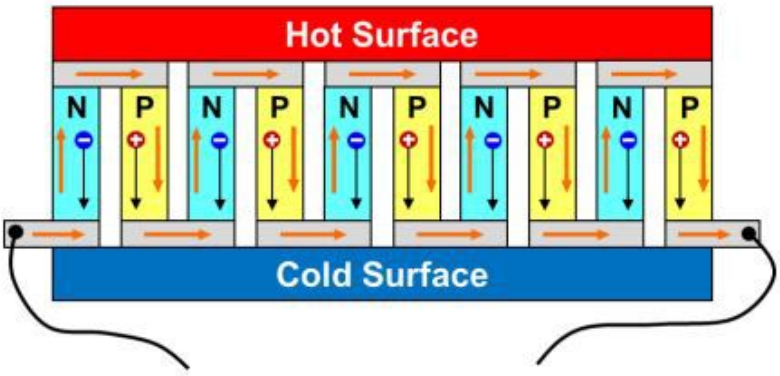


Figure 2.10: Construct of a thermoelectric generator.

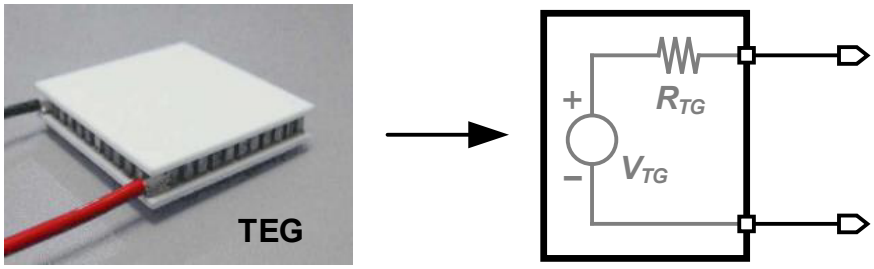


Figure 2.11: Equivalent electrical model of a TEG.

(R_{TG}) in series [27], as shown in Fig. 2.11. The open circuit voltage, V_{TG}, is proportional to the temperature difference across the hot-side and cold-side of the generator. Bismuth telluride is widely used as the thermoelectric material in commercial TEGs for its higher Seebeck coefficient, which is -287 µV/K for n-type and 81 µV/K for p-type compare to other materials. This makes it evident that multiple thermocouples in tandem are needed to generate tangible voltage output from the TEG. However, more elements in series increases the series resistance, R_{TG}.

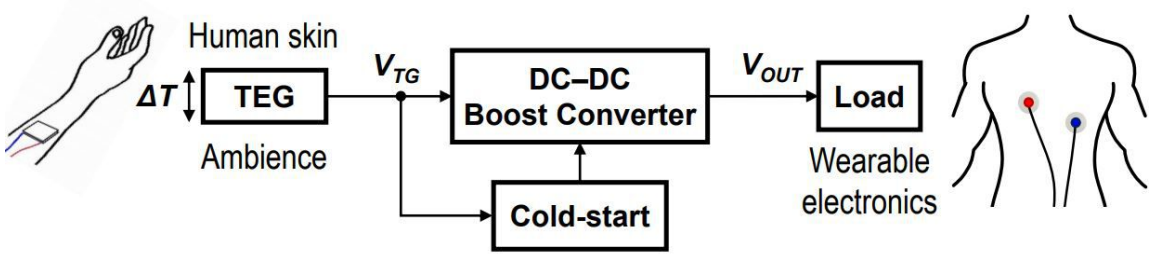


Figure 2.12: Power interface circuit in a thermoelectric energy harvester utilizing human body-heat.

2.4.3 Thermal energy harvesting from human body-heat

Normal human body maintains a steady temperature of 98.6 °F or 37 °C irrespective of the surroundings. The temperature difference between human skin and environment can be leveraged to generate power out of a TEG. Compared to other ambient sources of energy, human body-heat is available across day and night, in indoor and outdoor conditions, and with or without motion. This makes micropower thermoelectric energy harvesting from human body-heat a favorable alternative to battery in powering energy-efficient wearable devices. TEGs placed on human skin can provide higher power densities than solar cells, particularly for applications in indoor environment [28]. However, the small form-factor of wearables requires centimeter-scale TEGs which can generate only 10s of millivolts due to small temperature gradient (1 °-2 °C) and low Seebeck coefficient. This makes it unsuitable to directly power the electronics. A DC-DC boost converter is necessary to interface the TEG with the load electronics, as shown in Fig. 2.12. The converter transfers power from the source to the load while boosting voltage at the output required for operation of conventional CMOS circuits.

2.4.4 Primary challenges

While human body-heat appears as a potential source for providing power autonomy to wearable devices, thermoelectric energy harvesting utilizing the body-heat faces several fundamental challenges.

2.4.4.1 Low-voltage self-start

For realizing complete self-sustaining systems, the harvester must start on its own utilizing the energy from the source. This implies that the power-interfacing circuit must self-start with the small voltage of the TEG. This is extremely challenging, as the control circuits for the DC-DC boost converter operate only when the supply voltage crosses the threshold voltage of the transistors, which is at least a few hundred millivolts for state-of-the-art CMOS processes.

2.4.4.2 Maximum power point tracking

The internal resistance (R_{TG}) of the TEG, although small (a few ohms for centimeter-scale commercial TEGs), limits the maximum power available from the source. The input impedance of the DC-DC converter needs to be matched to R_{TG} in order to maximize the transfer of power from the TEG to the DC-DC converter, as shown in Fig. 2.13. A one-time frequency tuning of the DC-DC converter is sufficient to ensure impedance matching, rather than implementing complex maximum power point tracking (MPPT), thanks to the fairly constant R_{TG} of the TEG across

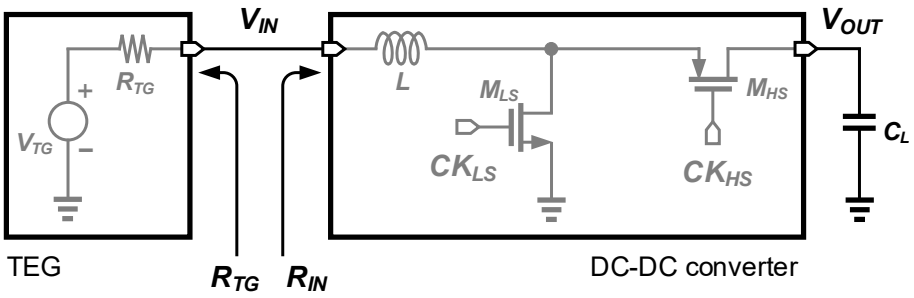


Figure 2.13: Input impedance matching for maximum power transfer from TEG to the boost converter.

temperature.

2.4.4.3 Efficiency of the DC-DC boost converter

Small open-circuit voltage (V_{TG}) is already challenging for operation of the control circuits of the DC-DC converter. In addition, MPPT at input reduces the effective input voltage of the DC-DC converter to half of V_{TG}, further increasing the difficulty of operating the DC-DC converter. Very small input requires high conversion ratio of the converter and results in more conduction time, which is evident from (2.7). This causes more conduction loss and impacts the efficiency of the converter significantly, as the input power from the small TEG is on the microwatts scale.

2.5 State-of-the-art thermoelectric energy harvesting

Several approaches have been recently demonstrated for autonomous cold start of thermoelectric harvesters. Mechanical switching with the assistance of vibrations

from body movement has been utilized to enable low-voltage start-up of the boost converter [17]. Additional sources like RF energy can also be exploited to enable cold-start [29]. A considerable research effort is noticeable in recent years to self-start the boost converter electrically utilizing the small voltage of the TEG itself to eliminate additional component dependency. Transformers are used in [30] and [31] to kick-start the boost converter at 21 mV and 40 mV, respectively. Inductor-based LC oscillators [32] or Colpitts oscillators [33] have also demonstrated start-up from 50 mV and 40 mV input voltages. All these approaches accomplished low-voltage cold-start but require additional off-chip magnetic components that limit device miniaturization.

Fully-integrated electrical cold start at low input voltage is challenging due to the high threshold voltage of transistors in sub-micron CMOS processes. The integrated self-start in [34] requires an input voltage of at least 330 mV to start the converter, and a capacitor pass-on scheme together with post-fabrication threshold-trimming of on-chip oscillator transistors in [35] achieves 95 mV cold start. Alternatively, Schmitt trigger oscillators are used in [36] to achieve integrated cold-start at 70 mV, but reliance on a conventional charge pump and large storage capacitor (1 nF) results in a slow start-up (1.5 s) and prevents further reduction of the cold-start voltage. An integrated oscillator reported in [37] successfully generates start-up clock at input voltage of 45 mV, although converter cold-start is limited to 210 mV.

Low voltage operation and efficiency improvement of DC-DC boost converters is also a growing research area for realizing energy harvesting platforms. One of the first generation boost converters designed for low-voltage thermoelectric energy

harvesting can operate with a small input voltage of 20 mV but does not have maximum power point tracking (MPPT), which reduces total extracted output power of the harvester in spite of high efficiency of the converter [38]. Also, it requires an additional source of energy for starting the converter. Low voltage boost converter architectures sustaining operation at input voltages as small as 10 mV are demonstrated in [29], [37] but fail to self-start at small input voltages, which makes them unsuitable for fully autonomous body-heat energy harvesting. Off-chip transformers are exploited in [30] and [31] to start the boost converter at tens of millivolts from the TEG. However, the implementation in [30] is favorable for high resistance TEGs incapable of generating micro watts of power at very small input voltages, whereas reuse of the transformer in [31] restricts the maximum efficiency of the converter to 61%. High peak efficiency and low-voltage cold-start of the boost converter is demonstrated in [32] and [33] but uses additional inductors for starting the primary converter. Multiple off-chip components like transformers or inductors make the harvesting unit bulky and will increase the cost and form-factor of wearable devices.

Hence, it is evident that high efficiency and self-start of the converter at low voltages are fundamentally difficult problems to address with the same architecture. This motivates further research for implementing thermoelectric energy harvesters exploiting human body heat in order to realize self-sustaining wearable sensors.

Chapter 3: Integrated Low-voltage Cold-start of a Boost Converter

Integrated electrical cold start of a DC-DC boost converter at low input voltage is significantly difficult due to the high threshold voltage of transistors in CMOS processes. Recent research prototypes use an on-chip voltage multiplier initially to boost the low input voltage with the assistance of a start-up clock. The intermediate boosted voltage then powers the control circuits of the inductive converter and the primary converter starts operation slowly. Although it is true that startup in such a process is primarily limited by the minimum supply needed for the start-up clock, cold-start voltage is also highly dependent on the boosting ability and output power of the start-up voltage multiplier.

This chapter demonstrates an alternative integrated start-up mechanism in which a one-shot pulse triggers the inductive converter to start operation. A start-up voltage multiplier is proposed that enables efficient voltage multiplication of the small input voltage by means of a high-gate-boosting scheme, implemented using cross-coupled complementary charge pumps. The multiplier operates with a start-up clock generated by an on-chip ring oscillator using a unique stacked-inverter delay element for ultra-low-voltage operation. The proposed start-up mechanism is implemented in a 0.18 µm CMOS process and achieves cold-start of an inductive boost converter at an input voltage as low as 57 mV, which is the lowest cold-start voltage reported to date using a fully-integrated electrical circuit [39].

Detailed circuit architectures of the key building blocks of the proposed start-up regime, including ultra-low-voltage clock generation, start-up voltage multiplier, and strobe generation, as well as low-voltage design challenges and extended block-level electrical characterization of the IC are described in the following sections.

3.1 Proposed one-shot cold start operation

Limited on-chip capacitance constrained by silicon area and low input voltage reduce charge transfer ($Q = CV$) through a charge-pump-based voltage multiplier. This is exacerbated by the low start-up clock frequency at low supply voltage, which results in a low output current. As such, charging a large storage capacitor with the diminished output power of a charge pump is not prudent for low-voltage cold start. However, while a TEG provides low output voltage, it can provide a moderate amount of current due to its low source impedance (typically a few ohms); charging an inductor with this current can generate higher energy per cycle. To exploit this, rather than relying solely on a start-up charge pump, power transfer is quickly handed over to an inductive converter to achieve a low-voltage and fast cold-start operation.

The proposed cold-start architecture is shown in Fig. 3.1a. A start-up voltage multiplier initially boosts the input voltage to power a strobe generation unit (SGU). The voltage boosting ability of the multiplier is improved by using cross-coupled complementary charge pumps to enhance gate drive of the charge transfer switches. A low-voltage, on-chip ring oscillator generates the start-up clock for operation of the charge pumps. A strobe signal, V_{ST}, from the SGU turns on an auxiliary low-side

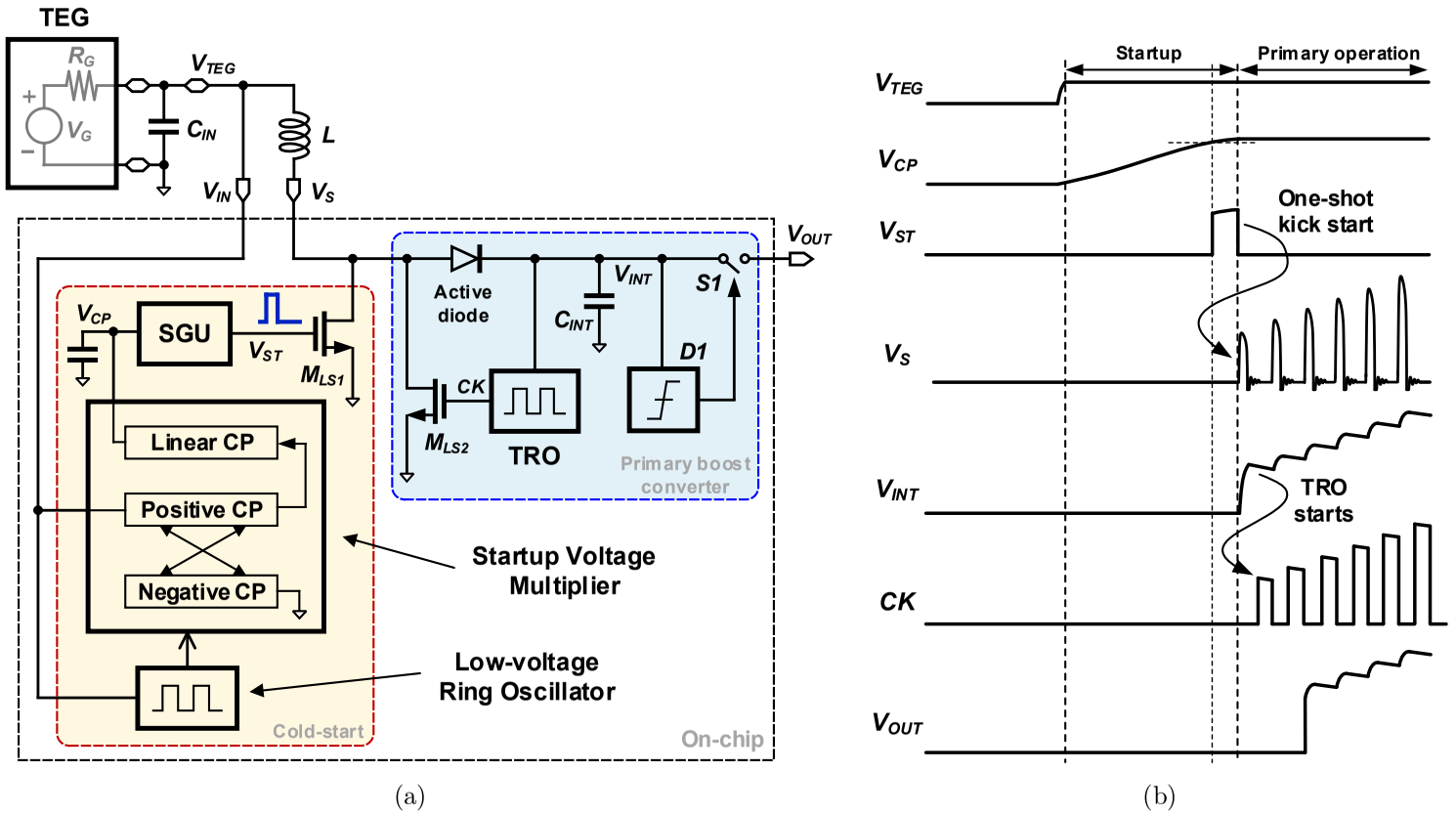


Figure 3.1: (a) Proposed integrated cold-start architecture, and (b) timing diagram of the cold-start sequence utilizing a fast-falling edge of a strobe pulse for quick triggering of the primary inductive boost converter.

(LS) switch, M_{LS1}, and charges the inductor with current from the TEG. As shown in Fig. 3.1b, a sharp falling edge of the one-shot pulse, V_{ST}, forces the voltage, V_S, to rise and forward-bias an active diode. The inductor current immediately charges a small on-chip storage capacitor, C_{INT} (350 pF), to a voltage $V_{INT} > 400$ mV in the strobe-cycle itself.

A thyristor-based ring oscillator (TRO), designed to start oscillation with a low supply (400 mV) is powered immediately by V_{INT} and takes over control to operate the inductive converter. A wider LS switch, M_{LS2}, is now used to charge the inductor with higher current per cycle. V_{INT} is not connected to the output until it crosses a voltage threshold detected by the voltage detector D1. This ensures that all inductor energy is used to start the TRO during start-up. M_{LS1} is disabled during primary operation as V_{ST} goes low.

The proposed start-up scheme reduces the power burden on the voltage multiplier and achieves low-voltage start-up. In addition, the one-shot kick-start mechanism quickly hands over the power transfer process to a more efficient current-mode inductive boost converter and thereby speeds up the start-up process.

3.2 Ultra-low-voltage ring oscillator

An oscillator is required for operation of the start-up voltage multiplier. Ring oscillators, comprising a series of delay stages in closed loop are easy to integrate and have been used to generate start-up clocks [34–36]. To create sustained oscillation, the required gain (A) of each delay stage and total number of stages (n) can be

derived from Barkhausen criteria for oscillation as

$$A \geq \sqrt{1 + \left(\frac{\omega_o}{\omega_p}\right)^2} \quad \text{and} \quad n = \pi / tan^{-1}\left(\frac{\omega_0}{\omega_p}\right) \tag{3.1}$$

where ω_0 is the frequency of oscillation and ω_p is the pole frequency contributed by each stage. As such, a smaller gain (A) requires a higher number of delay stages (n) for oscillation and results in a low output frequency (ω_o) of the ring oscillator.

3.2.1 Limitations of CMOS inverter as delay element

At very low supply voltage, CMOS inverters suffer from low DC gain due to the significant deterioration of transconductance of the transistors. From Meindl's limit [40], minimum supply required for an inverter in a 0.18 µm bulk CMOS process to achieve DC gain greater than unity is 48 mV at 300 °K [41]. Hence, this sets the theoretical limiting supply voltage for operation of a CMOS inverter-based ring oscillator.

Low supply voltage also degrades the output voltage rails of an inverter. As shown in Fig. 3.2, during an output transition, the difference current ($I_{ON} - I_{OFF}$) between active and inactive transistor charges or discharges the output. As V_{OUT} changes, $|V_{DS}|$ of the active transistor decreases and I_{ON} falls, whereas $|V_{DS}|$ of the inactive transistor increases. Finally, V_{OUT} settles to V_H or V_L when $I_{ON} = I_{OFF}$. For a transistor in sub-threshold operation with device width, W, and length, L,

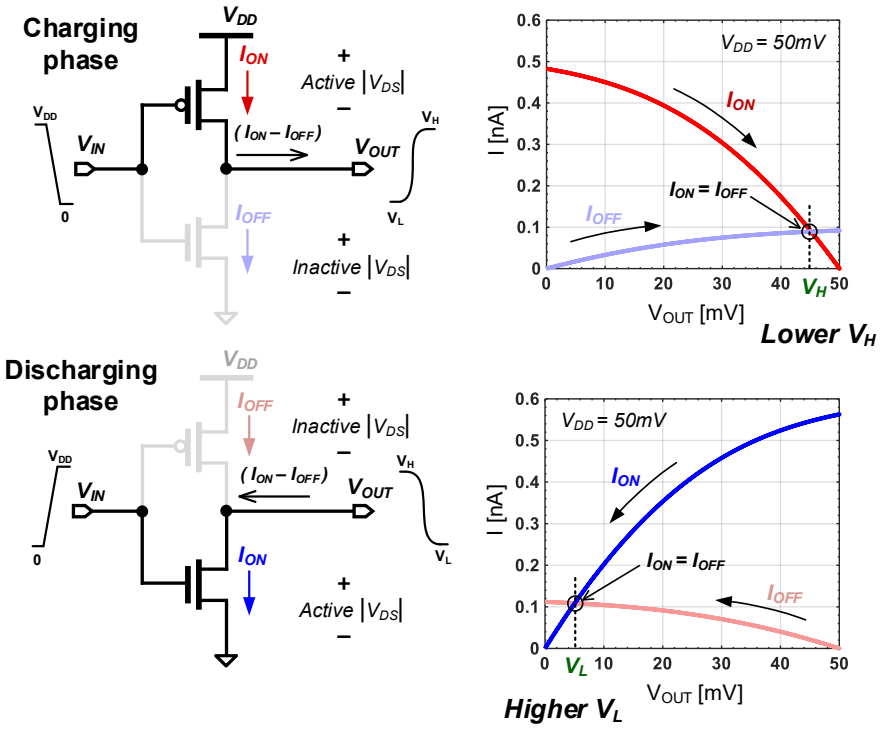


Figure 3.2: Low output voltage rail of a CMOS inverter at low supply.

drain current, I_D, is given by

$$I_D = I_0.\frac{W}{L}.e^{\left(\frac{|V_{GS}|-|V_{th}|}{\gamma V_T}\right)}.\left(1-e^{-\frac{|V_{DS}|}{V_T}}\right) \tag{3.2}$$

where I_0 $(= \mu_0.C_{ox}.(\gamma-1).V_T^2)$ is constant, γ is the sub-threshold swing factor, V_{th} is the threshold voltage, and V_T is the thermal voltage [42]. At very low supply, when $|V_{GS}|<<|V_{th}|$ and $V_{DS} \sim V_T$, I_D strongly depends on $|V_{DS}|$. Thus, an increase in $|V_{DS}|$ of the inactive transistor during V_{OUT} transition results in significant increase of I_{OFF}. Thereby, the difference current vanishes well before V_{OUT} reaches the supply rail (V_{DD} or GND) and reduces the output voltage rail ($V_H - V_L$) of the inverter

(Fig. 3.2); simulated output rail is 20% lower than supply rail (50 mV) in 0.18 µm CMOS. As a consequence, the output clock of a CMOS inverter-based ring oscillator exhibits degraded voltage swing at low supply.

3.2.2 Proposed delay element

Dynamic reduction of the leakage current, I_{OFF}, can improve output voltage swing at low supply. To achieve this, a delay element is proposed [43] comprising three inverters, arranged as shown in Fig. 3.3a. Outputs of INV1 and INV3 are connected to the sources of PMOS and NMOS transistors of INV2, respectively.

During the charging phase, a high-to-low transition of V_{IN} causes INV3 to pull node B to V_{DD}, as annotated in Fig. 3.3b. This reduces V_{DS} and V_{GS} across the NMOS transistor M4 of INV2 and suppresses the leakage current I_{OFF}. During the discharging phase, as V_{IN} transitions from low to high, INV1 pulls node A down to GND and suppresses I_{OFF} through the PMOS transistor M3 of INV2 by reducing both V_{SD} and V_{SG} across it. However, the $|V_{DS}|$ drop across M1 or M6 in the path of I_{ON} will reduce effective $|V_{GS}|$ across the active transistors, M3 and M4, respectively, in the corresponding phases. This would reduce effective I_{ON} and nullify the effect of lowering I_{OFF}. To alleviate, M1 and M6 are sized three times of the width of M3 and M4, respectively, while M2 and M5 are of same dimensions as M4 and M3.

Compared to other leakage suppression techniques, such as Schmitt trigger logic [44], the proposed stacked-inverter delay cell provides more effective leakage current bypassing at low supply by applying maximum $|V_{GS}|$ to M5 and M2 in the respective

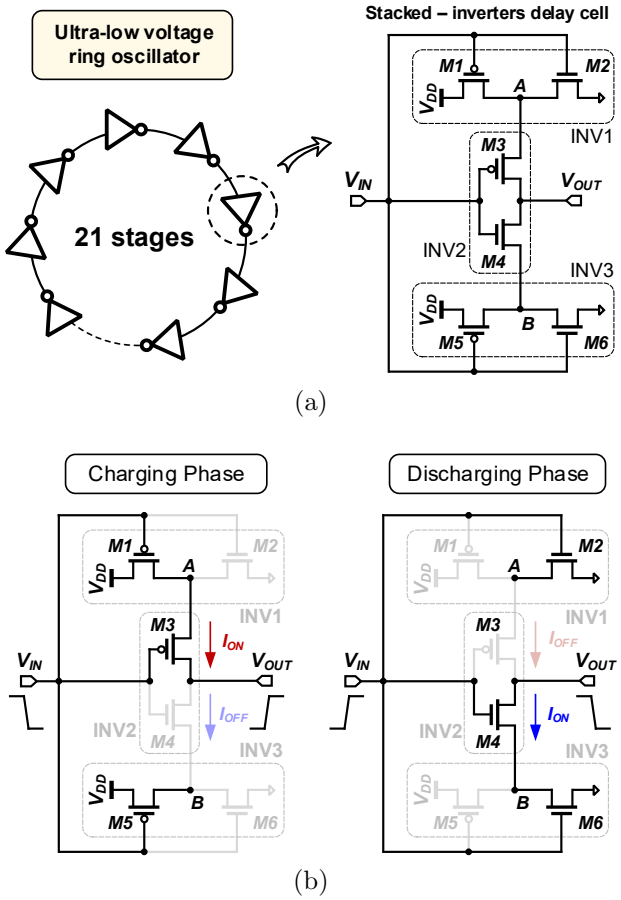


Figure 3.3: (a) Ultra Low-voltage ring oscillator comprising the proposed stacked-inverters based delay cells, and (b) Leakage current suppression in the delay cell in charging and discharging phases.

phases. It also yields faster pull up and pull down actions of M5 and M2; with the transition of V_{IN}, I_{OFF} is blocked at the onset of the V_{OUT} transition. A similar leakage bypassing technique adopted for designing a low-voltage ring oscillator in recent work [37] also demonstrates the effectiveness of the technique. It is important to note that, although leakage current, I_{OFF}, is suppressed from the output in both the phases, additional leakage currents through the bypass transistors, M2 and M5,

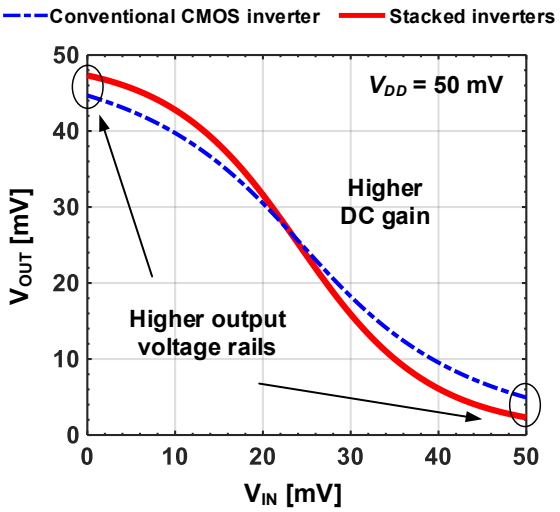


Figure 3.4: Simulated VTC of the proposed delay cell shows improvement of DC gain and output voltage rails over conventional CMOS inverter.

increase total current consumption of the delay block as compared to a simple CMOS inverter. However, the increase in power consumption is negligible compared to other blocks when used in a complete energy harvester architecture.

Low-V_{th} transistors are used to increase conduction at the low supply voltage. Simulated VTC of the stacked-inverter delay block in a 0.18 µm CMOS process is shown in Fig. 3.4, which demonstrates a 13.3% improvement in output voltage rails and 32.5% higher DC gain compared to those of a CMOS inverter (INV2 alone) at a supply of 50 mV. The enhanced gain is due to the higher output impedance, R_o, at the final output of the delay element, which can be expressed as

$$R_o = \left[r_{o3} + (1 + g_{m3}r_{o3})R_{o1}\right] || \left[r_{o4} + (1 + g_{m4}r_{o4})R_{o3}\right] \tag{3.3}$$

where R_{o1} and R_{o3} are the output impedances of INV1 and INV3, respectively, at

the DC operating point. While the cascoding effects of M3 and M4 are small due to the small intrinsic gains, $g_{m3}r_{o3}$ and $g_{m4}r_{o4}$, at the low supply voltage, R_o of the stacked-inverter delay cell is still higher than the output impedance ($r_{o3}||r_{o4}$) of INV2 alone. The g_m of M1-M6 together contribute to the delay cell transconductance.

A ring oscillator was implemented using 21 stages of the stacked inverter delay element to generate the start-up clock. At a supply of 50 mV, the simulated frequency of the clock is 9.4 kHz at the typical corner; the frequency ranges between 2 kHz−38 kHz across process corners.

3.3 Start-up voltage multiplier

A voltage multiplier is required during start-up to boost the input voltage and power the cold-start control circuits. Low swing and low frequency of the pumping clock make designing such a multiplier especially challenging at low voltage.

3.3.1 Limitation of conventional charge pumps

On-chip voltage multipliers such as the Dickson charge pump [14] can boost input voltage but incur a voltage drop across each stage diode. A cascaded dual-phase charge pump [1] mitigates this problem by providing a gate drive (V_{GS}) equal to the voltage swing of the clock (V_{CK}) to turn on the charge transfer switches (CTS). This works efficiently at nominal input voltage, but at low supply, V_{CK} ($< V_{DD}$) turns on the CTS only weakly. The resulting forward current in the ON phase is not much larger than the reverse leakage current in the OFF phase, causing inefficient

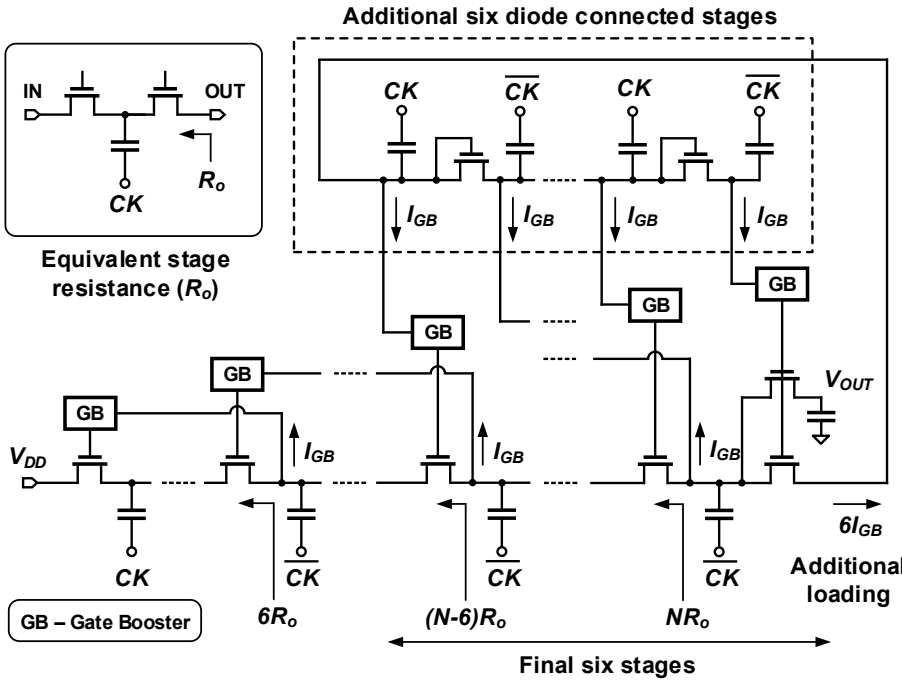


Figure 3.5: Loading effect in high gate boosting by borrowing voltages from much later stages.

charge transfer. Dynamic biasing of CTS [2], where boosted voltages are borrowed from higher stages of the charge pump to generate a V_{GS} of $2 \cdot V_{CK}$ for the CTS can further improve charge transfer. However, at tens of millivolts of V_{DD}, the boosted V_{GS} still does not sufficiently improve on-conductance of the CTS. For instance, with $V_{DD} = 50\,\mathrm{mV}$, more than $6 \cdot V_{CK}$ is needed to cross the threshold voltage of even low-V_{th} devices available in a $0.18\,\mu\mathrm{m}$ CMOS technology. In addition, overlapped phases of the pumping clock and the CTS gate clock in [2] result in reverse charge sharing, reducing pumping efficiency. Dynamic body biasing [45,46] can also improve CTS on-conductance but is only effective for input voltages above 100 mV.

For ultra-low-voltage operation, the high V_{GS} needed for each CTS can be gener-

ated by borrowing voltages from much later stages of the charge pump, as illustrated in Fig. 3.5. The gate boosters (GB) represent circuit blocks such as dynamically-biased inverters used to generate the gate clocks [2]. Additional diode-connected stages are needed to generate gate clocks for the final stages, which suffer from inefficient voltage boosting and will reduce CTS gate drive in the final stages. Also, loading of these stages (6 shown here) will result in a voltage drop of $6NI_{GB}R_o$ at the output, V_{OUT}, where N is the number of primary stages, I_{GB} is equivalent current consumption of each GB, and R_o is the equivalent resistance per stage. For 20-stage voltage multiplication, the voltage drop will be $120I_{GB}R_o$. As such, conventional gate-boosting techniques are insufficient at very low input voltage.

3.3.2 Proposed cross-coupled complementary gate boosting

In this work, a high-gate-boosting technique is demonstrated using cross-coupled complementary charge pumps for ultra-low-voltage operation. As shown in Fig. 3.6, the first section of the proposed start-up charge pump comprises a six-stage positive charge pump (CP^+) and a six-stage negative charge pump (CP^-), each operating in dual phases. The supply voltage, V_{DD}, is applied to the CP^+ input, and input of the CP^- is connected to GND.

PMOS switches are used as CTSs in CP^+, whereas isolated deep-n-well NMOS switches are used as CTSs in CP^-. The complementary charge pumps mutually boost the gate drive of their CTSs, as described below.

Dual-phase voltages from later stages of CP^- are borrowed to generate CTS

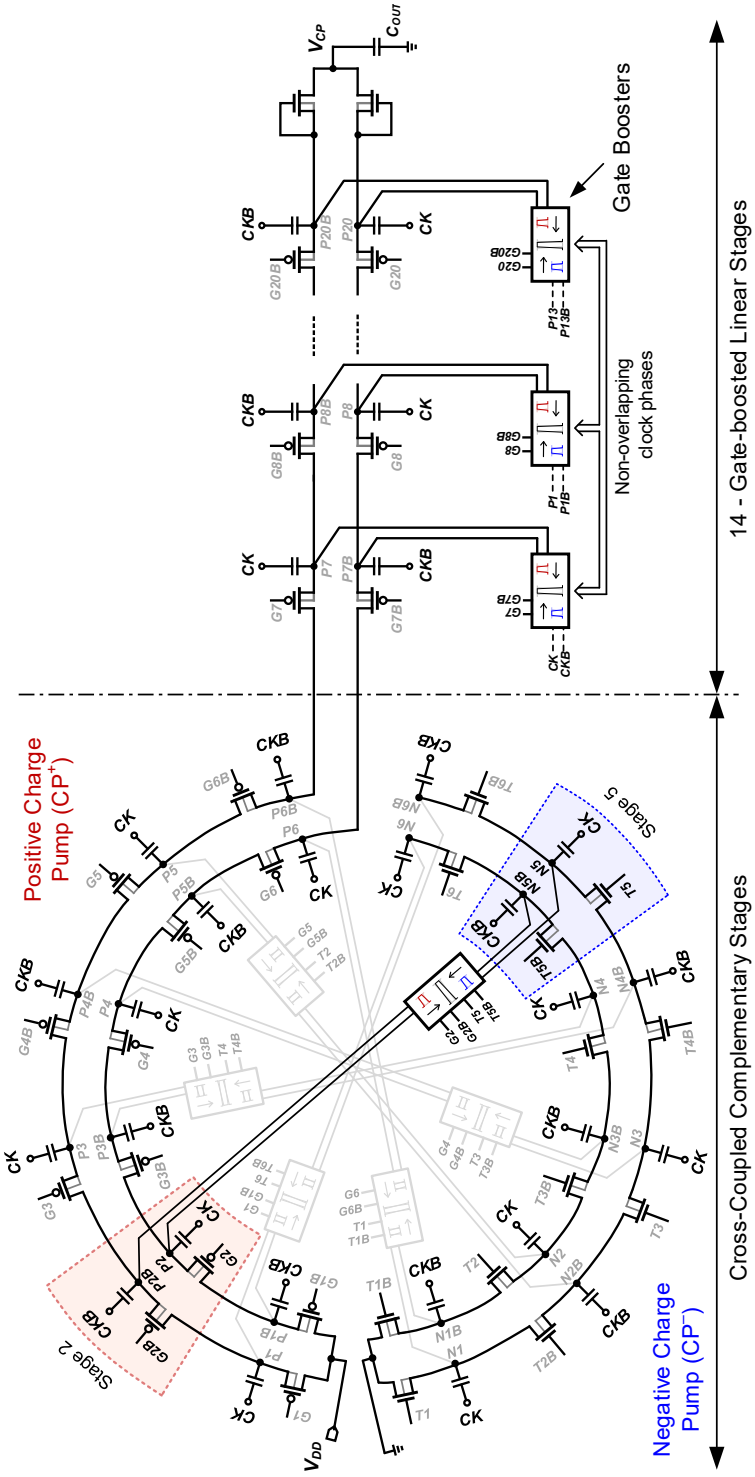


Figure 3.6: Proposed start-up voltage multiplier, using cross-coupled complementary charge pumps for high gate-boosting and low voltage operation.

gate clocks for earlier stages of CP^+. As illustrated in Fig. 3.7, negative dual-phase voltages $N5$ and $N5B$ from the 5th stage of CP^- and positive dual-phase voltages $P2$ and $P2B$ from the 2nd stage of CP^+ are used to generate gate clocks $G2$ and $G2B$ that swing between a higher voltage level of $P2 - P2B$ and a lower voltage level of $N5-N5B$ for the PMOS switches of the 2nd stage of CP^+ using a gate booster circuit. The high negative voltage swing of the gate clock will boost the gate drive, V_{SG}, of the PMOS switch to $V_{DD}+6V_{CK}$ in the charge transfer phase, while ensuring $V_{SG} = 0$ in the non-conduction phase. However, as CP^- also exhibits poor CTS conductance at low voltage, negative voltage rail of the gate clocks will be affected, thereby lowering the effective V_{SG} of the CTSs in CP^+. A fully-complementary structure of the charge pumps addresses this problem, where dual-phase voltage outputs of the complementary charge pump CP^+ are utilized to improve CTS conductance of CP^-. With the drain and source of the NMOS switch of CP^- connected to boosted negative voltages, the positive voltage of gate clocks $T5$ and $T5B$ utilizing a higher voltage level $P2-P2B$ from CP^+ will increase the gate drive, V_{GS}, of NMOS switches of the 5th stage of CP^- to $V_{DD} + 6V_{CK}$ during the charge transfer phase, enhancing conduction. In a similar fashion, complementary outputs of the 1st CP^+ stage and 6th CP^- stage, 3rd CP^+ stage and 4th CP^- stage, and so on, generate CTS gate clocks of respective stages with the help of gate boosters, as shown in Fig. 3.6. This complementary gate boosting action improves the pumping efficiency of both charge pumps.

As shown in Fig. 3.6, the final 14 stages of the start-up charge pump further boost the output of CP^+ using PMOS switches whose gate clocks are generated borrowing

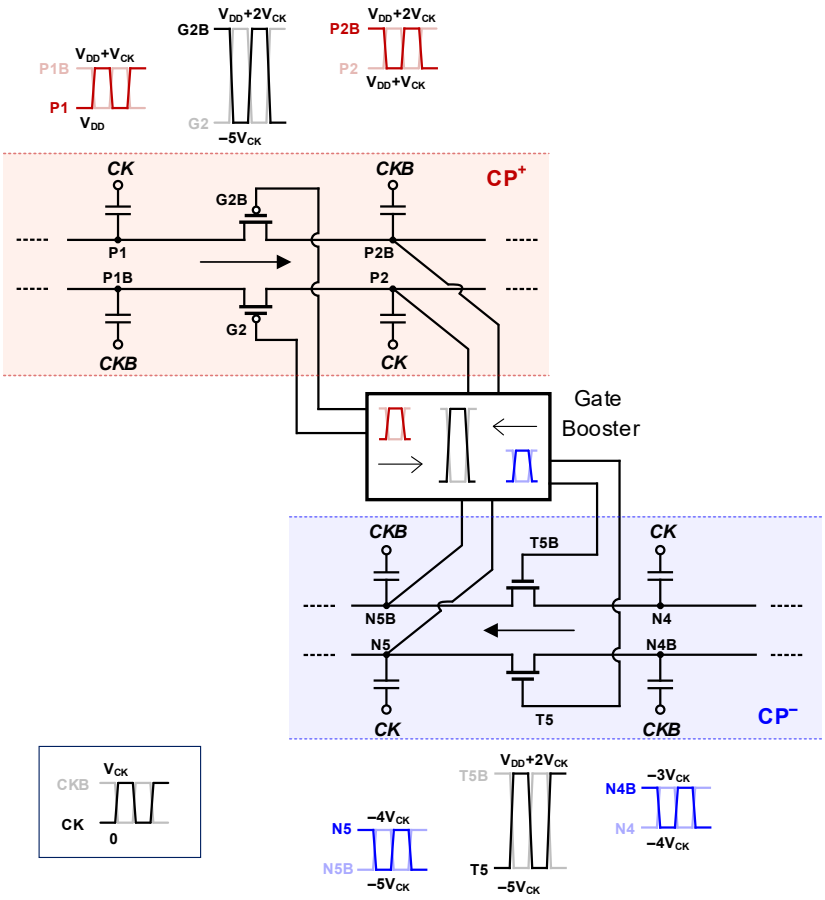
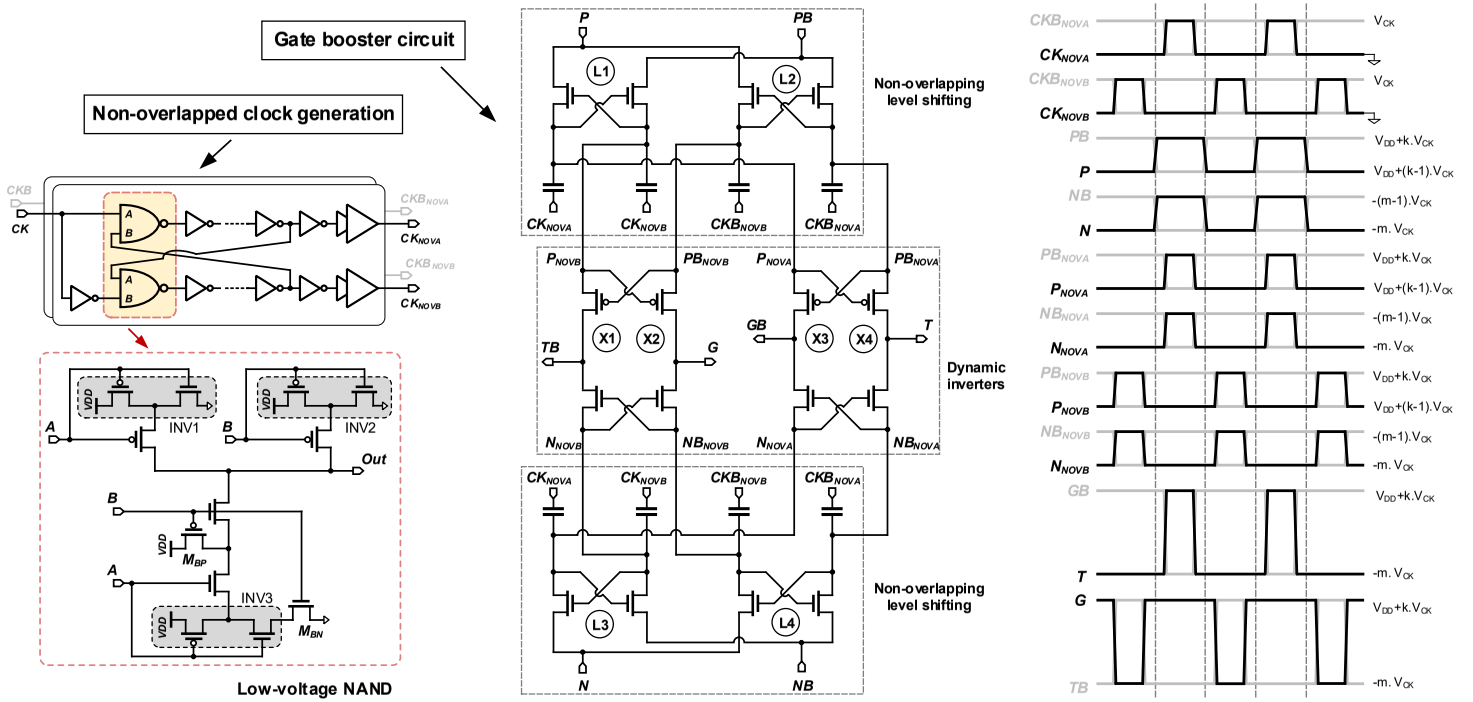


Figure 3.7: Mutual voltage boosting of gate clocks borrowing dual phased outputs of complementary charge pumps.

lower voltages from earlier stages. The final stage of the charge pump uses diode-connected deep-n-well NMOS devices to prevent reverse charge flow during output voltage droop due to load transients. It is important to note that, although gate boosting of the negative charge pump causes additional loading, voltage drop in the load path from this effect is small ($I_{GB}.[1+2+...+6]R_o = 21I_{GB}R_o$), as voltages are borrowed from the initial 6 stages. Compared to a conventional gate-boosting

technique, which borrows voltage from later stages, the proposed technique borrows voltages from earlier stages to boost the gate clock of CTSs of CP^{+}. As such, no stage needs to wait for an increase in voltage at later stages for enhanced charge transfer, which makes the gate boosting action faster. Nonetheless, during initial cold-start state, the charge pump boosts the voltage using leakage current of the CTS with the available low-voltage swing ($\sim V_{DD}$) of the intrinsic gate clocks; however, the regenerative action of the cross-coupled CP^{+} - CP^{-} assists the voltage multiplier to emerge quickly from this slow initial state.

Low-V_{th} devices are used for CTSs to improve charge transfer. While these exhibit higher leakage current compared to regular-V_{th} devices, enhanced conductivity with boosted gate drive makes reverse leakage negligible. The deep-n-well of the isolated NMOS devices in CP^{-} are shorted to GND, whereas the local body is shorted to the source and connected to the nearest minimum voltage terminal. This allows the NMOS switches to handle negative voltages without forward biasing the deep-n-well junction and without V_{th} degradation due to body bias. High-density MOS capacitors, each 20 pF, are used as pumping capacitors, optimizing switching resistance, $1/(Cf_{CK})$, while ensuring slow switching limit operation by keeping charging time constant ($CR_{on} \ll 1/f_{CK}$) [19]. A 120 pF decoupling capacitor, C_{OUT}, is added to the final output, V_{CP}, using MOS capacitors.



(a) (b)

Figure 3.8: (a) Generation of non-overlapping gate clocks with boosted voltage swing, and (b) timing diagram for gate clock generation.

3.3.3 Non-overlapping boosting of gate clocks

Gate clocks of the CTSs are generated using the gate-booster circuit illustrated in Fig. 3.8a. The boosted gate clocks must be non-overlapping with the pumping clocks to avoid reverse charge flow in the non-charge-transfer phase. The level shifters L1-L2 and L3-L4 take dual-phase outputs of the charge pump ($P - PB$ and $N - NB$) and generate corresponding non-overlapped phases using clocks CK_{NOVA}, CK_{NOVB}, CKB_{NOVA}, and CKB_{NOVB}, as shown in the timing diagram in Fig. 3.8b. These clock phases are generated using low-voltage NAND logic, implemented with a similar leakage suppression technique as discussed in Section 3.2.2. As shown in Fig. 3.8a, $INV1$ and $INV2$ suppress leakage currents of the pull-up transistors; $INV3, M_{BN}$, and M_{BP} suppress leakage currents of the pull-down transistors. MOS capacitors, each 2 pF, are used in the non-overlapping level-shifters.

Outputs of the level-shifters, P_{NOVB}, PB_{NOVB}, N_{NOVB} and NB_{NOVB}, are fed to the dynamic inverter X1 to generate gate clock TB that swings between the higher positive voltage levels of $P - PB$ and lower negative voltage levels of $N - NB$ as shown in Fig. 3.8b. Similarly, gate clocks G, GB, and T are generated using X2-X4. For the final 14 stages of the voltage multiplier, the same gate booster circuit is used, where $N - NB$ are replaced by positive voltage outputs of lower stages.

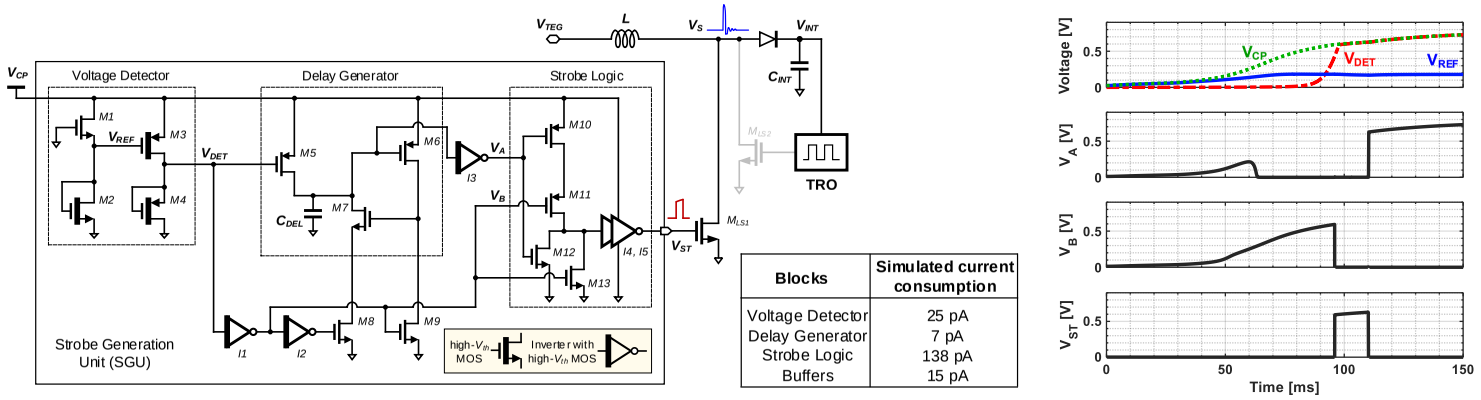
Poor gate drive of transistors in X1-X4 causes slow transition of the boosted gate clocks; to ensure non-overlap of the final gate clocks with the pumping clocks, the delay between falling edges of CK_{NOVA} and CK is designed to be larger than the delay between their rising edges. Timing of other phases are set accordingly. The clocks are driven by higher strength stacked-inverter cells to drive long routing paths.

Routing is laid out symmetrically to ensure correct phases and minimal skew at the final destinations.

3.4 Strobe generation and one-shot start-up

A strobe generation unit (SGU) is powered by the output of the start-up voltage multiplier, V_{CP}, to generate the control pulse, V_{ST}, required to kick-start the inductive boost converter. The SGU consists of a voltage detector, delay generator, and strobe logic circuit. As the output power of the charge pump is low, the SGU must operate with very small quiescent current.

The voltage detector output, V_{DET}, asserts V_{ST} once V_{CP} crosses a threshold sufficiently higher than the V_{th} of M_{LS1} to energize the inductor with required start-up current. A low-power reference generator is implemented using low-V_{th} and high-V_{th} transistors, M1 and M2, respectively [47]. Static current is minimized by using long-channel (10 µm) devices for M1 and M2; settling of V_{REF} is still fast compared to the slow rise of V_{CP}, as shown in Fig. 3.9b. The detector comprises high-V_{th} PMOS transistors M3 and M4. Current through M3 is compared against leakage current through M4 (gate-source shorted); with the rise of V_{CP}, V_{SG} of M3 increases, and as current through M3 goes above the leakage current of M4, the output V_{DET} starts rising and follows V_{CP}. The width of M4 is set 10 times the width of M3 for higher effective threshold, $V_{REF}+V_{SG,M3}$. M_{LS1} is sized to energize the inductor with required start-up current without substantially slowing the falling-edge transition of V_{ST} due to larger gate capacitance.



(a) (b)

Figure 3.9: (a) Circuit schematics of the strobe generation unit (SGU) with simulated current consumption of each functional blocks, (b) simulated waveforms showing functionality of the SGU.

V_{DET} is delayed to generate V_A using a thyristor-based latch formed by transistors M6-M7 [48] . The capacitor C_{DEL} is precharged to V_{CP} by M5 before V_{DET} rises. Once M5 turns off, the latch is enabled by turning M8 on and M9 off using V_{DET}. As C_{DEL} is discharged by leakage current while V_{CP} rises, V_{SG} of M6 increases, which charges the gate of M7; the M6-M7 regenerative feedback quickly discharges C_{DEL}. The thyristor latch avoids crowbar current during voltage transitions and minimize power consumption.

V_{ST} is finally generated from V_A and V_B using NOR logic (M10-M13) and buffered to the gate of M_{LS1}. All internal buffers ($I1 - I3$) are designed with high-V_{th} transistors to reduce leakage current. Simulated current consumption of the sub-blocks of the SGU is shown in Fig. 3.9a.

An active diode with low static current consumption [49] is used to reduce voltage drop in the current path from the inductor to the capacitor, C_{INT}. An energy-efficient thyristor-based oscillator (TRO) [50] is designed to oscillate at a supply voltage as low as 400 mV. This enables the clock, CK, immediately following the strobe cycle and it takes over control of the inductive boost converter. As the TRO takes the control, the inductor is energized using a wider LS switch M_{LS2}. Following cold start, the inductive boost converter is operated in discontinuous conduction mode (DCM), favorable for the low power level of the application.

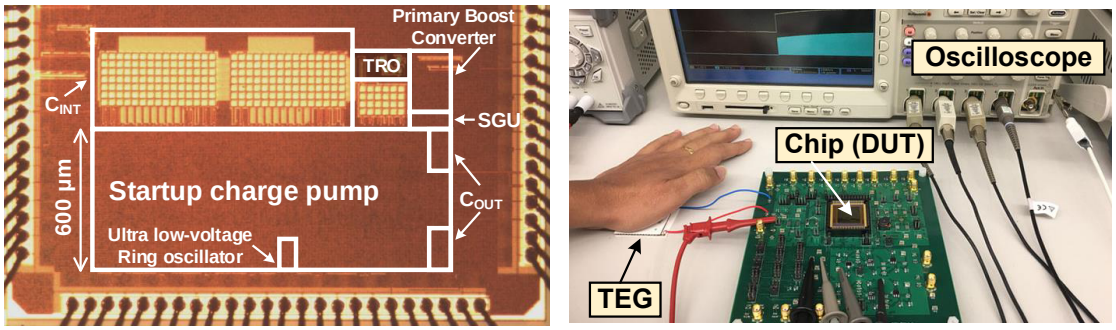
In order to kick-start the inductive boost converter successfully with the one-shot strobe pulse, the energy stored in the inductor during the strobe cycle must be sufficient to power the TRO, which can be expressed as:

$$\frac{1}{2} \cdot L \left(\frac{V_{TEG}}{R_{LS1}} \right)^2 > \frac{1}{2} \cdot C_{INT} V_{INT}^2 + \frac{V_{INT} I_{TRO}}{f_s} \tag{3.4}$$

where R_{LS1} is the on-resistance of M_{LS1} during the strobe cycle, f_s is the frequency of CK, and I_{TRO} is the current drawn by the TRO. Conduction loss and leakage current through the active diode are negligible and are not included in the above condition for simplicity. R_{LS1} is dependent on the voltage drive (V_{ST}) and size of M_{LS1} during the strobe period, whose upper limits are bounded by the available output power of the start-up voltage multiplier at the cold-start voltage.

The inductor value, L gives another degree of freedom to meet this condition, as expressed in (3.4). While higher f_s seems favorable to reduce the start-up energy requirement in (3.4), this increases I_{TRO} and minimum value of V_{INT} to start the TRO. Based on the available output power of the voltage multiplier and on setting gate drive and size of M_{LS1} accordingly, it is calculated that an inductance value of higher than 100 µH is enough to meet the condition expressed in (3.4).

A frequency of 25 kHz is chosen for CK to optimize the conduction and switching losses of the converter, along with meeting the requirement of starting up the TRO with a small supply of 400 mV. Although CK has a duty cycle of 66.67%, it still ensures DCM operation of the boost converter due to the high conversion ratio ($t_{OFF} >> t_{ON}$). This creates a t_{ON} of 26.8 µs, and the peak inductor current is kept much below the saturation current limit of the inductor for the whole input voltage range.



(a) (b)

Figure 3.10: (a) Die photo of the chip fabricated in 0.18 µm CMOS technology, (b) experimental set up for measurements with commercial TEG attached to human body.

3.5 Measurements

The proposed cold-start architecture was fabricated in a 0.18 µm CMOS process. Fig. 3.10a shows the die photograph of the implemented chip, where the cold-start block occupies 0.6 mm × 1.6 mm silicon area.

The start-up clock, CK_{STUP}, generated from the ultra-low-voltage ring oscillator is buffered to an output pin for measurements; buffers are powered using a separate test-only supply rail. Output transient of the start-up clock in Fig. 3.11 shows that oscillation starts at an input supply voltage as low as 40 mV, which demonstrates effective leakage suppression using the proposed stacked-inverter delay cells. The measured voltage swing of the clock is lower than the internal clock swing due to the loading of the low-voltage test buffers by pad and probe parasitics.

A test output of the start-up voltage multiplier is buffered using an off-chip buffer to minimize probe loading during characterization. Measured output transient in Fig. 3.12 shows that an input voltage of 55 mV is boosted by the multiplier to an

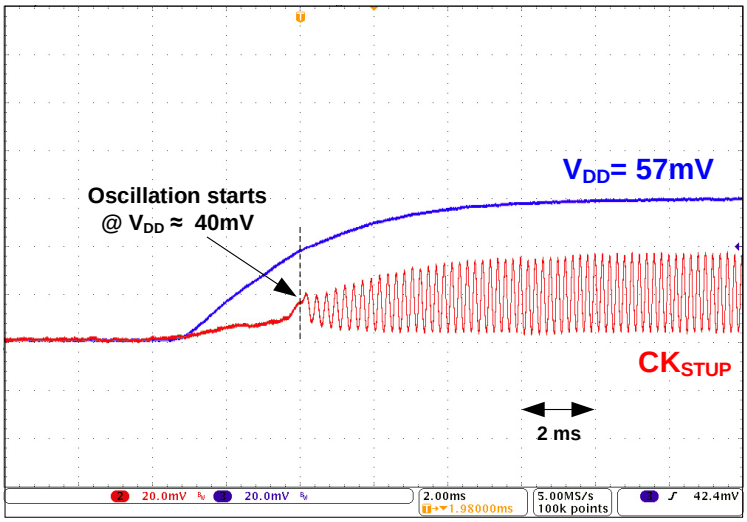


Figure 3.11: Measured start-up clock generated by the ultra-low-voltage ring oscillator.

output of 840 mV, with an estimated load current of hundreds of picoamps due to the finite input impedance of the off-chip buffer. Boosted gate clocks cannot be measured at minimum input supply due to low drivability. As such, boosted gate clocks of the 7th stage of CP^+ and the 3rd stage of CP^- are shown in Fig. 3.13 using an input supply of 120 mV.

Pumping efficiency of the charge-pump-based voltage multiplier was measured across varying input voltage using a digital multimeter with an input impedance >1 GΩ to measure output voltage. The output power was measured using a source meter (Keithley 2450) as a current sink. The measurement was done for an input voltage range relevant for the target application, body-heat energy harvesting, where the cold-start block will be exposed mostly to sub-100 mV TEG voltages due to the small ΔT between skin and ambient. As shown in Fig. 3.14, the proposed start-up voltage multiplier achieves a pumping efficiency higher than 78% across an input

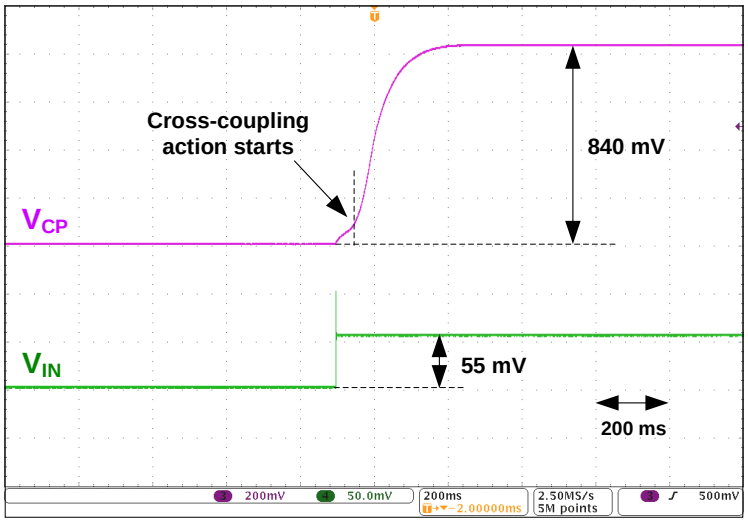


Figure 3.12: Measured transient waveform of V_{CP} (buffered off-chip) with an input supply of 55 mV.

voltage range of 50 mV - 100 mV, with a peak value of 93% at an input voltage of 65 mV. Pumping efficiency of the voltage multiplier is maximized at low input voltages to reduce the minimum cold-start voltage. At higher input voltages, large swing of the boosted gate clocks causes the gate boosters to draw more current driving CTS gates and increases internal loading. Additionally, low pumping-clock frequency due to large number of delay stages in the ring oscillator reduces pumping effciency of the voltage multiplier at higher input voltages. Nevertheless, boosted output of the voltage multiplier at higher input voltages can easily power the SGU to generate the start-up strobe.

The start-up performance of the proposed architecture is characterized using a bench-top power supply with added 5 Ω series resistance to imitate a typical TEG source. A 220 µH off-chip inductor is used for the primary boost converter. The value of the inductor is chosen higher than the minimum required value derived in Section

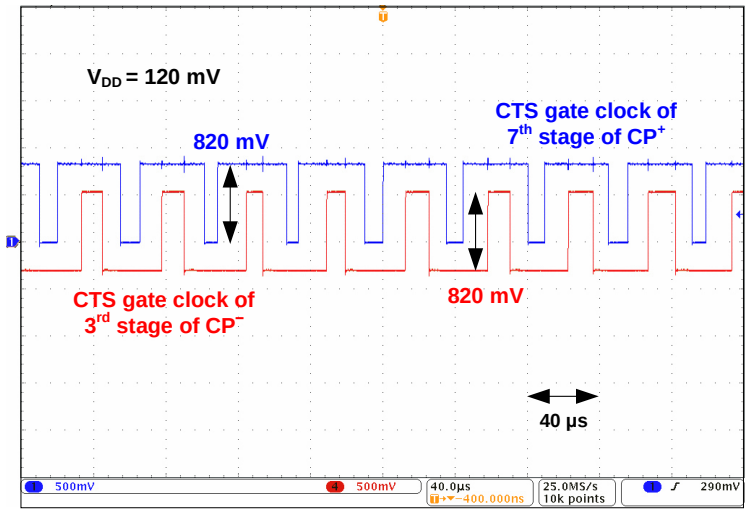


Figure 3.13: Measured non-overlapping gate clocks with boosted voltage swing.

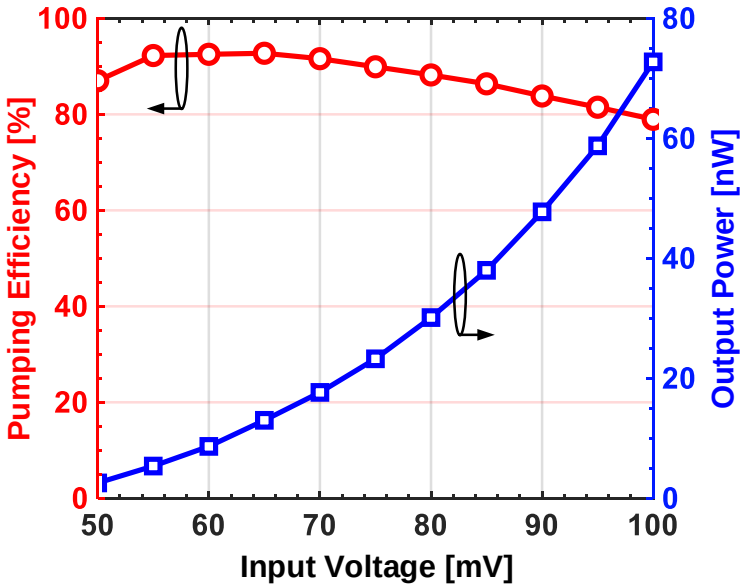


Figure 3.14: Measured pumping efficiency and output power of the charge-pump-based voltage multiplier across input voltages.

Section 3.4 to mitigate additional conduction losses due to inefficient routing. As shown in Fig. 3.15, the primary converter starts with a minimum source voltage of

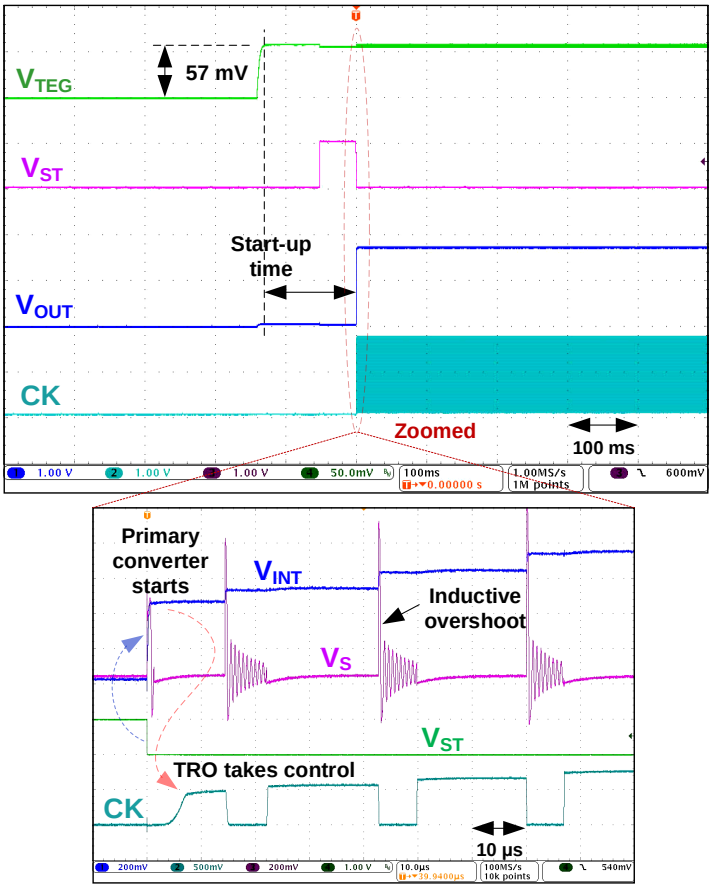


Figure 3.15: Measured start-up transient of the proposed cold-start architecture. Zoomed waveform showing triggering of the primary converter with the fast falling edge of strobe pulse, V_{ST}.

57 mV. Although the standalone voltage multiplier operates at lower input voltage, leakage current of the SGU loads the multiplier output and prevents start-up at lower voltage. The minimum operational voltage of the key blocks are summarized in Table 3.1.

Due to the fast one-shot start-up mechanism, it takes only 135 ms for cold-start. The zoomed waveform in Fig. 3.15 shows inductive overshoot at V_S with the falling

Table 3.1: Summary of minimum operational voltage

Block	**Min. operational voltage**
Start-up ring oscillator	40 mV
Start-up voltage multiplier	50 mV
Cold-start	57 mV
Inductive boost converter	25 mV (once started)

edge of V_{ST}. A rise in V_{INT} above 400 mV following the strobe-cycle starts the TRO immediately, and CK takes control of the inductive boost converter. Once started, the output voltage rises to an unregulated 1.8 V with no load.

The measured efficiency of the boost converter is 20% at the 57 mV cold-start voltage, and the efficiency increases to 47% at input voltage of 100 mV. As observed, the efficiency of the converter is relatively low due to comparatively high conduction losses, including the on-resistance of the low-side switch, M_{LS2}, that charges the inductor following the cold-start, as well as parasitic routing resistance that can be improved in future implementations.

While the cold-start block draws current from the source during the normal operation of the boost converter, this small input current (Fig. 3.16) is drawn from the low-side input voltage, and power consumed by the cold-start block is negligible compared to the input power of the boost converter and does not affect overall efficiency. As such, the cold-start block is not functionally de-activated during normal operation. Nevertheless, disabling the cold-start block with the start of the inductive converter will increase the maximum input voltage range of the boost converter, ensuring that devices in the start-up voltage multiplier remain within voltage stress tolerance at higher input voltages (>100 mV).

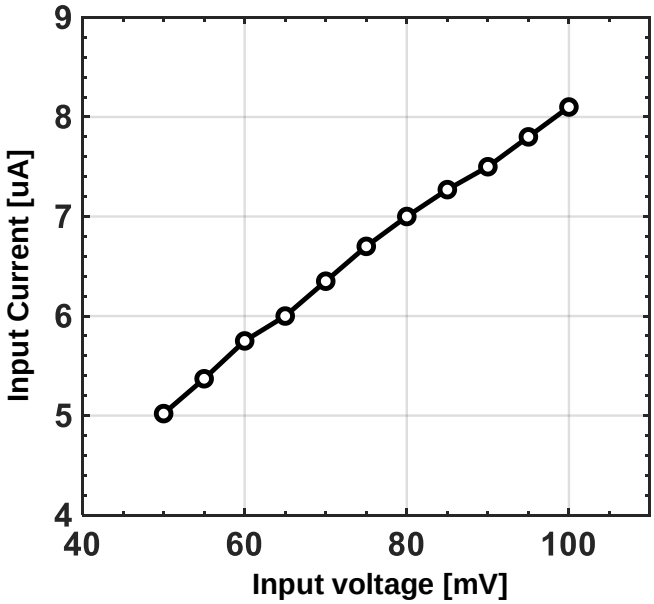


Figure 3.16: Current drawn from source by the cold-start block at various input voltages

Cold start was also demonstrated using a commercial TEG (Marlow TG12-6-01L); the experimental setup is shown in Fig. 3.10b. The measured input and output transient waveforms in Fig. 3.17 show that the boost converter starts at an input voltage of 57 mV, as expected, which corresponds to a temperature gradient of ΔT=1.6°C, and sustains operation until input voltage falls below 25 mV (ΔT = 0.8°C). The total energy used from the TEG for cold start is 90 nJ.

Prior to the operation of the inductive converter, the cold-start block is the only active block and draws less than 6 μA of current from the source, as shown in Fig. 3.16. Once started, the inductive converter draws an input power of 20 μW at the cold-start voltage and sustains operation with a minimum input power of 2.5 μW. The minimum input voltage for cold-start of the converter was checked across 5 chips

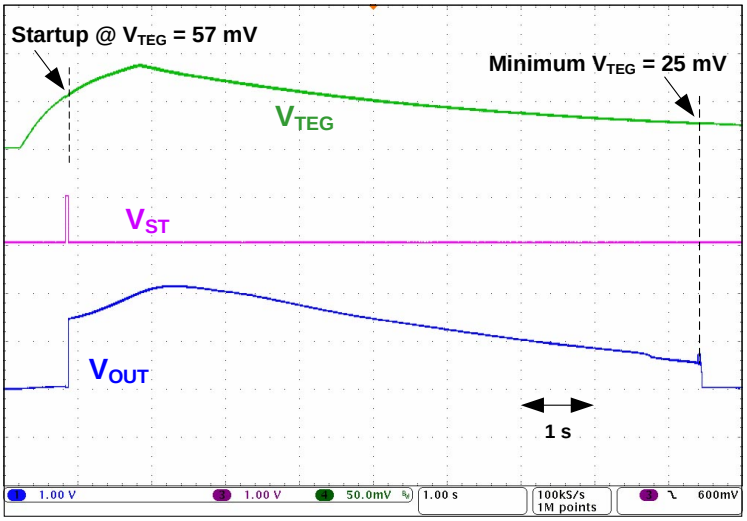


Figure 3.17: Measured transient of the boost converter with a commercial TEG.

and varies from 57 mV to 61 mV.

Performance of the proposed cold-start architecture is compared against state-of-the-art in Table 4.2. While [51] achieved low-voltage cold start with the aid of mechanical vibrations, [32] and [33] used additional off-chip inductors. The cold-start time, defined as the time required from power-on to starting the primary boost converter, is determined by the ability of the low-power start-up voltage multiplier to power start-up control circuits of the inductive boost converter. While the rise time of the final output depends on the inductor current and the output load cap, a majority of the start-up time is consumed by the slow, low-voltage cold-start. The proposed fully-integrated cold-start architecture achieves cold-start of the boost converter at 18% lower input voltage and in 48% less time, even at 1.6× lower input voltage, compared to previously demonstrated on-chip implementations [35, 36].

Table 3.2: Comparison with state-of-the-art cold-start voltages

Cold-start Integration	Off-chip			On-chip				
References	JSSC'11 [51]	JSSC'13 [32]	JSSC '18 [33]	JSSC'12 [35]	JSSC '15 [29]	JSSC'16 [36]	ISSCC '19 [52]	**This work**
Process	0.35 µm	65 nm	65 nm	65 nm	0.13 µm	0.13 µm	0.18 µm	**0.18 µm**
Start-up mechanism	Mechanical vibration	LC oscillator & charge pump	Colpitts oscillator & charge pump	Ring-oscillator(1) & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	Ring-oscillator & charge pump	**Ring-oscillator & charge pump**
Cold-start voltage	35 mV	50 mV	40 mV	95 mV	220 mV	70 mV	129 mV	**57 mV**
Start-up time	18 ms	30 ms (2)	22 ms (2)	262 ms	3.5 s (2)	1.5 s	150 s (2)	**135 ms**
Intermediate storage capacitor(4)	470 pF (On-chip)	– (On-chip)	4.7 nF (Off-chip)	10 nF (Off-chip)	100 uF (Off-chip)	1 nF (On-chip)	– (Off-chip)	**350 pF (On-chip)**
Boost Inductor	22 µH	4.7 µH + 100 µH	3.3 µH	6.8 µH	22 µH	>200 µH	–	**220 µH**
Additional element(3)	MEMS	Inductor	Inductor	None	None	None	None	**None**

(1) Post fabrication V_{th} trimming. (2) Estimated from transient plots. (3) For cold-start purpose only. (4) Used during cold-start.

3.6 Chapter summary

An integrated cold-start architecture was presented to start inductive boost converters at very low input voltage toward realizing autonomous body heat energy harvesting using thermoelectric generators. Challenges of on-chip voltage multiplication at small input voltage have been addressed by applying a unique cross-coupled gate boosting technique using complementary charge pumps. An efficient leakage suppression technique was also demonstrated using stacked inverters to generate a start-up clock using an integrated ring oscillator at 40 mV input supply voltage. The one-shot start-up mechanism achieves integrated cold-start of the boost converter at an input voltage as low at 57 mV, and it takes only 135 ms to start an inductive boost converter.

In general, the proposed architecture and described design efforts were focused on implementation and optimization of the cold-start architecture, demonstrating a fast and low-voltage one-shot cold-start technique with the aid of the proposed voltage multiplier. Once started, additional features can be added to further enhance the primary inductive boost converter efficiency, including maximum power transfer and zero-current sensing.

Cold-start and handover to a primary boost converter were also demonstrated using a commercial TEG as input with a temperature gradient $<2^{\circ}$C, illustrating the utility of the proposed architecture for realizing fully-autonomous thermal energy harvesting from human body heat.

Chapter 4: High Efficiency, Low-Voltage, and Self-Starting Boost Converter

Small temperature gradient (ΔT) between human body and environment generates few 10s of millivolts of open-circuit voltages from centimeter-scale TEGs. In addition, input impedance matching for maximum power transfer further reduces available voltage from the source. These altogether make it challenging to improve the efficiency of the DC-DC boost converter, inherent to such energy harvesters. Integrated cold-start regime demonstrated in the previous chapter achieves start-up of the boost converter at 57 mV [39], but suffers from low efficiency due to the usage of an asynchronous boost converter.

In this chapter, a single-inductor boost converter architecture is presented that is capable of harvesting energy efficiently and can also self-start at small TEG voltages [53]. A unique loss-optimized maximum power transfer (LO-MPT) scheme is proposed that optimizes the efficiency of the boost converter while ensuring maximum power point tracking (MPPT) at the input and improves the output power of the harvester by enhancing the end-to-end efficiency. The boost converter achieves more than 75% efficiency at a small input voltage of 15 mV and achieves a peak efficiency of 82% with a 50 mV input. Efficient low-voltage operation of the converter enables sustained operation at an input voltage as low as 3.5 mV, which is the smallest operational input voltage for a boost converter reported to date. In addi-

tion, a dual path architecture is proposed which assists in self-starting the converter with a TEG voltage as low as 50 mV with the aid of an integrated one-shot startup technique. The harvester generates a regulated output voltage of 1.2 V and operates over a TEG voltage range of 7 mV - 200 mV.

4.1 Proposed self-starting boost converter architecture

The primary objective of the proposed converter is efficient operation and self-start at low voltage. A dual-path architecture is designed as shown in Fig. 4.1 that utilizes a single inductor to achieve both. The TEG is essentially a DC voltage source that generates voltage, V_{TG}, proportional to the temperature difference (ΔT) between human body and environment with few ohms of source impedance, R_{TG}. A capacitor, C_{TG}, is connected at the output of the TEG to keep input voltage ripple small enough during switching operation of the converter.

4.1.1 Low-voltage self-start

A one-shot cold-start technique implemented in [39] demonstrates fast and low-voltage cold-start of an asychronous boost converter. Although it addresses one-half of the problem, the inherently inefficient asynchronous boost converter and no MPPT at input results in low output power from the harvester during normal operation. In this work we adopted the basic idea of the startup technique in [39] but utilized a dual-path architecture to self-start a highly efficient DC-DC boost converter without using additional bulky off-chip components like inductors or transformers.

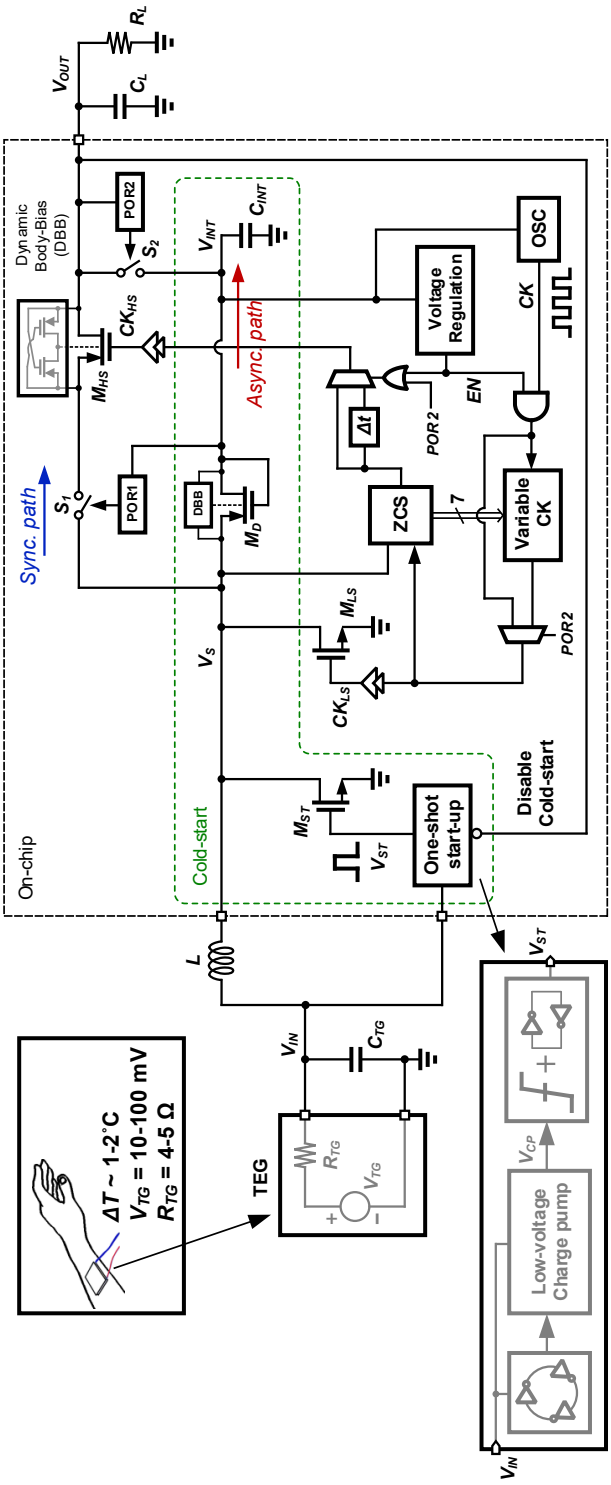


Figure 4.1: Proposed high-efficiency single-inductor thermoelectric energy harvester with low-voltage integrated one-shot cold-start utilizing dual-path architecture.

In the beginning, as shown in Fig. 4.2a, a charge-pump-based voltage multiplier operated by a start-up clock from a low-voltage on-chip ring oscillator boosts the input voltage V_{IN}. The boosted output of the charge pump, V_{CP}, is utilized to generate a start-up strobe pulse, V_{ST}. This pulse turns on the start-up low side switch M_{ST} for a small duration and charges the inductor L with current from the TEG. With the falling edge of V_{ST} inductive overshoot at V_S turns on the PMOS diode, M_D asynchronously and the inductor current charges the on-chip storage capacitor, C_{INT}. This intermediate storage capacitor is chosen small enough (200 pF) so that the inductor energy accumulated during the strobe cycle can charge it to generate a voltage, V_{INT}, above 500 mV momentarily following the falling edge of V_{ST}. A secondary oscillator (OSC) is powered by V_{INT} and generates switching clock, CK. Now, the inductor is charged with more current every CK cycle using a wider low-side switch, M_{LS} and continues to transfer energy from source to C_{INT} by the asynchronous mode of operation as shown in Fig. 4.2b. It is noted that with this asynchronous path enabled, a voltage regulation block is activated to track V_{INT}, whose functionality will be elaborated in the subsequent description of the operation.

A power-on-reset (POR1) circuit senses the rise of V_{INT} and turns on the switch, S_1 as soon as V_{INT} crosses 1 V. This activates a secondary path of energy transfer utilizing the same primary inductor, L. The switch S_1 is implemented with a PMOS transistor and is kept off during the start-up phase utilizing the boosted voltage, V_{CP} from the start-up voltage multiplier. As shown in Fig. 4.2c the secondary path operates synchronously using a high-side PMOS switch, M_{HS} and transfer energy from the source to the final output, V_{OUT}. The input power from the TEG at

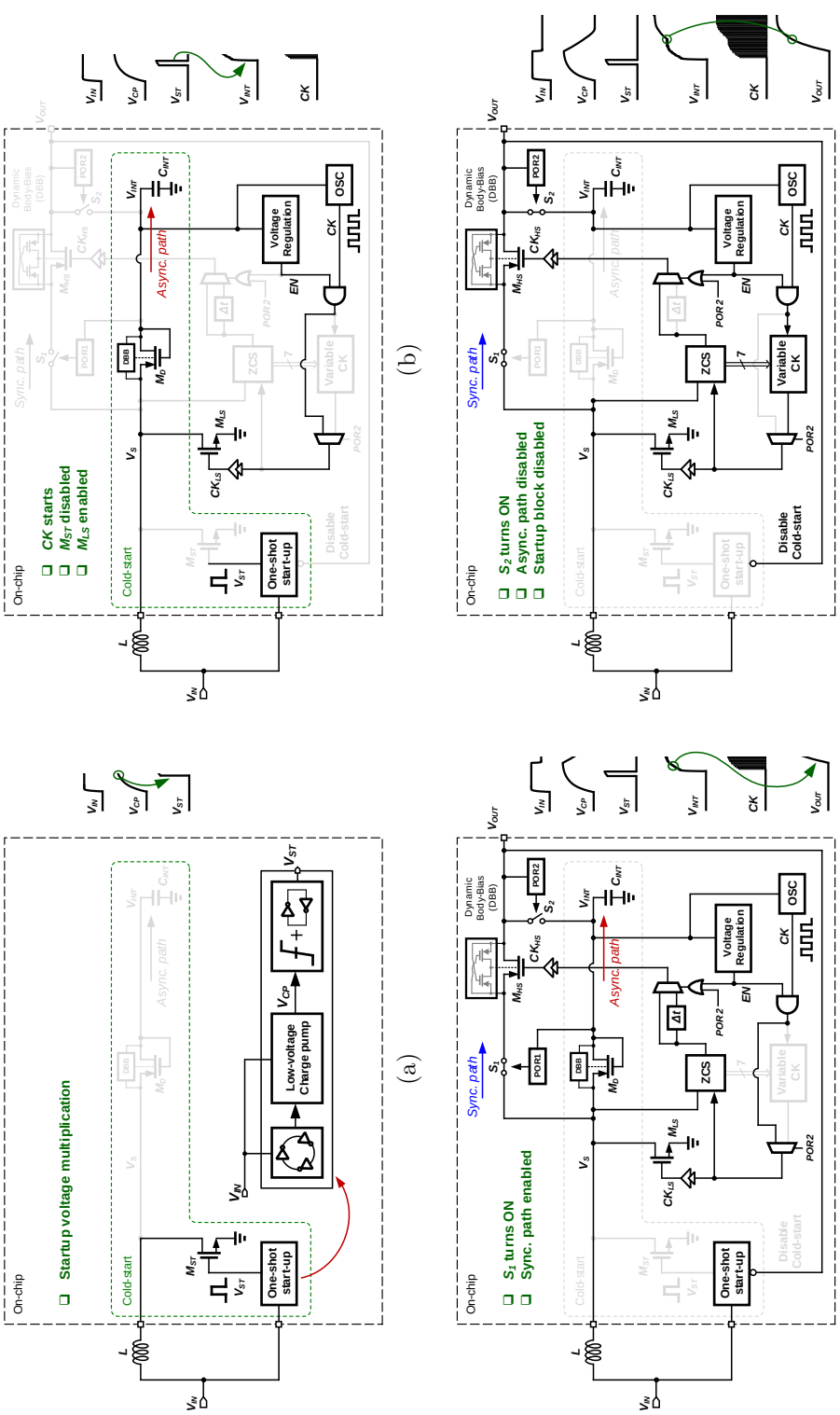


Figure 4.2: Operation of the boost-converter in (a) phase 1, (b) phase 2, (c) phase 3, and (d) phase 4.

low voltages being low, a discontinuous conduction mode (DCM) of operation is chosen, which is efficient for low-power synchronous boost conversion [38]. In order to implement DCM, a zero current sensing (ZCS) block is also enabled by POR1 to sense the instant of zero crossing of the inductor current and adjusting the on-time (t_{HS}) of M_{HS}. During this phase, while the high efficiency synchronous path charges the large output capacitor, C_{OUT} (1µF), the asynchronous path is kept live to power the control circuits like ZCS, voltage regulation, and OSC. The dual path is operated in a time-multiplexed way controlling a dead time, Δt, between turning off M_{LS} and turning on M_{HS}. The voltage regulation already enabled senses V_{INT} and compares against internally generated reference voltages. If V_{INT} falls below, it indicates that control power is running short and the dead time is activated by the EN signal to force M_D to turn on during that time. The inductor current is briefly rerouted to the asynchronous path and charges C_{INT}. With the falling edge of CK_{HS} the inductor current reverts back to the synchronous path through M_{HS} and charges C_{OUT}.

In the final phase, as V_{OUT} crosses 0.7V detected by POR2, the power switch S_2 is turned on and shorts V_{OUT} with V_{INT}. The POR2 signal also disables the dead time forever using the multiplexer as shown in Fig. 4.2d. As such, the boost converter now enters into exclusively synchronous mode and operates efficiently to provide control power as well as output power. The rising V_{OUT} disables the start-up clock and turns off the start-up voltage multiplication to avoid unnecessary control power consumption during normal operation of the primary boost converter. The same voltage regulation block regulates the final output voltage V_{OUT} by means of an on-off hysteretic control where proportion of V_{OUT} is compared against two

threshold voltages to decide whether to continue the converter operation or turn it off by controlling the switching clock, CK. When the converter goes off, C_{OUT} provides the output power to the load.

The proposed architecture utilizes the asynchronous path to speed up the start-up process, leveraging the one-shot cold-start mechanism and finally starts a high-efficiency synchronous boost converter at low voltage without using additional inductors.

4.1.2 Losses of a boost converter and maximum power transfer

While harvesting energy from human body heat, the available power from the TEG at small ΔT being low, the DC-DC converter should transfer most of the source power to the output to provide usable power to the load electronics. Final extracted output power of the harvester depends on (a) efficiency of the boost converter as well as (b) matching of the input impedance of the converter with the source impedance of the TEG for maximum power transfer. Hence, it is important to figure out the key design parameters and the trade-offs associated with efficiency of the converter and input matching.

4.1.2.1 Losses in a DC-DC boost converter

In a synchronous inductive boost converter shown in Fig. 4.3a, the inductor (L) is energized in one phase (t_{LS}) by flowing current (I_L) from the source, as soon as the low-side (LS) switch (M_{LS}) is turned on with the help of a switching clock (CK_{LS}).

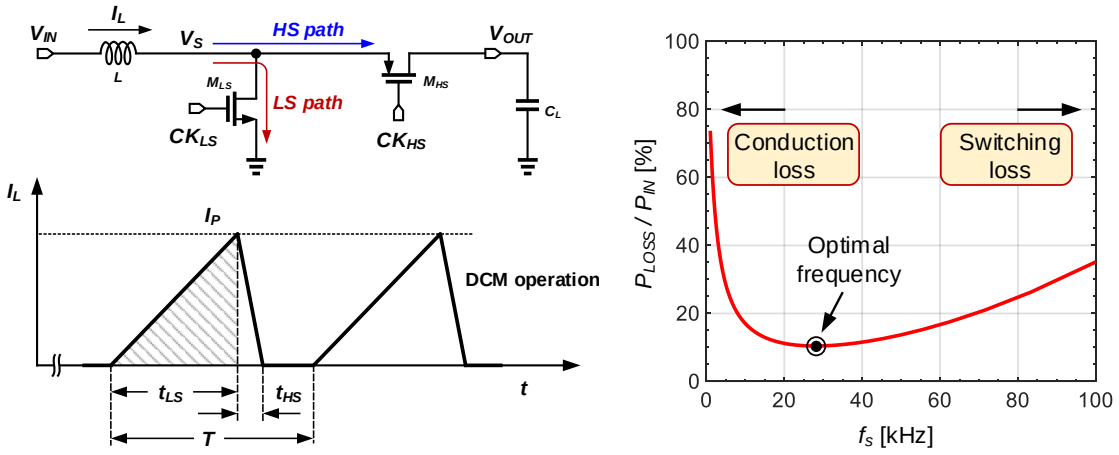


Figure 4.3: (a) Operation of a boost converter in discontinuous conduction mode (DCM), and (b) Power loss of the converter normalized with respect to input power with varying switching frequency.

In the other synchronous phase (t_{HS}), the high-side (HS) switch (M_{HS}) is turned on using clock, CK_{HS}, and energy from the inductor flows to the output in the form of current to charge the load capacitor (C_L). In DCM operation, the stored inductor energy is completely transfered to the output every cycle and is done by keeping L connected to C_L in the t_{HS} phase until I_L reaches zero. For the remaining part of a cycle when L is disconnected from the output, stored energy in C_L feeds the load until freshly charged inductor replenishes C_L with energy. The conversion gain (K) of the boost converter can be formulated as

$$K = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{t_{LS}}{t_{HS}}\right) \tag{4.1}$$

For applications with small V_{IN}, the required conversion gain, K, is high and requires $t_{LS} >> t_{HS}$. The current, I_L, is assumed to be linearly changing with time during

t_{LS} and t_{HS} and hence $I_P = V_{IN}t_{LS}/L$. The linearity holds true as long as $t_{LS} << L/R_{LS}$, where R_{LS} represents the on-resistance of M_{LS}. The amount of input power, P_{IN} that flows into the DC-DC converter during this process can be calculated as,

$$P_{IN} = \frac{1}{T}.\frac{1}{2}.V_{IN}I_P\left(t_{LS} + t_{HS}\right) \approx \frac{1}{2}.\frac{{V_{IN}}^2{t_{LS}}^2}{LT} \tag{4.2}$$

where T is the time period of the switching clock.

At the same time, a considerable amount of power is lost due to the conduction through the on-resistance of M_{LS} while energizing the inductor during t_{LS}, and through that of M_{HS} during charging C_L in t_{HS} which can be derived as follows:

$$\begin{aligned} P_C &= P_{C,LS} + P_{C,HS} \\ &= \frac{1}{T}\int_0^{t_{LS}} \left(\frac{I_P t}{t_{LS}}\right)^2 R_{LS}dt \\ &\qquad + \frac{1}{T}\int_0^{t_{HS}} \left(I_P - \frac{I_P t}{t_{HS}}\right)^2 R_{HS}dt \\ &= \frac{1}{3}.\frac{{I_P}^2}{T}.\left(R_{LS}t_{LS} + R_{HS}t_{HS}\right). \end{aligned} \tag{4.3}$$

Expressing t_{HS} and I_P in (4.3) in terms of t_{LS} we get,

$$P_C = \frac{1}{3}.\frac{{V_{IN}}^2{t_{LS}}^3 R_S}{L^2 T} \tag{4.4}$$

where $R_S = (R_{LS} + R_{HS}/K)$ represents the cumulative switch resistance contributed by LS and HS switches. It should be noted here that the DC resistance of the inductor being in the conduction path also contributes to the total conduction loss,

P_C, and can be considered as a part of R_S but is usually small. It is evident that for high values of K, conduction loss contributed by the LS path dominates over that of the HS path, as depicted by the hashed area in Fig. 4.3a.

The control circuits being powered by the converter consume a portion of the output power and appear as control losses. A majority of this is the switching loss of the drivers for the large LS and HS switches. Other quiescent power consumption due to leakage currents is small and can be neglected. If the total lumped switch gate capacitance of the control circuit is C_{SW}, the switching loss of the control circuits is

$$P_{SW} = C_S V_{OUT}^2 . f_S = C_S K^2 {V_{IN}}^2 . f_S \tag{4.5}$$

where $f_S = 1/T$ is the switching frequency.

Apart from these two primary losses, there exist other losses like synchronization losses and losses due to parasitics. The synchronization losses are incurred due to the timing errors of the switching clocks, CK_{LS} and CK_{HS}, during transitions. Whereas, residual inductor energy due to timing error of ZCS will resonate with the parasitic capacitor at node V_S right after the t_{HS} phase and dissipate through the body diode of the LS switch and the DC resistance of the inductor, resulting in parasitic losses. But all these losses are significantly small compared to the two primary losses explained earlier. Hence the total power loss of the converter can be

summed as

$$\begin{aligned} P_{LOSS} &= P_C + P_{SW} \\ &= \frac{1}{3}.\frac{{V_{IN}}^2 {t_{LS}}^3 R_S}{L^2 T} + C_S K^2 {V_{IN}}^2.f_S. \end{aligned} \tag{4.6}$$

Normalizing P_{LOSS} with P_{IN} using (4.2) and (4.6) we get,

$$\frac{P_{LOSS}}{P_{IN}} = \frac{2DR_S}{3L}.\frac{1}{f_S} + \frac{2C_S K^2 L}{D^2}.f_S^2 \tag{4.7}$$

indicating the concave nature of the loss of the converter with respect to the switching frequency, where conduction loss dominates at lower frequency and switching loss dominates at higher frequency, as shown in the simulated plot in Fig. 4.3b. Hence, there exists an optimal f_S at which P_{LOSS}/P_{IN} is minimum for a fixed conversion ratio, duty-cycle, switch resistance and inductor value. Minimum normalized loss maximizes the efficiency of the DC-DC converter (η_{DCDC}) as

$$\eta_{DCDC} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} = 1 - \frac{P_{LOSS}}{P_{IN}} \tag{4.8}$$

4.1.2.2 Maximum power transfer at input

The internal resistance, R_{TG}, of the TEG limits the amount of power that can be extracted from the generator. For maximum power transfer (MPT) from the TEG to the converter, the input resistance, R_{IN}, of the boost converter should be matched with R_{TG} as shown in Fig. 4.4a. The extent of matching can be expressed as the

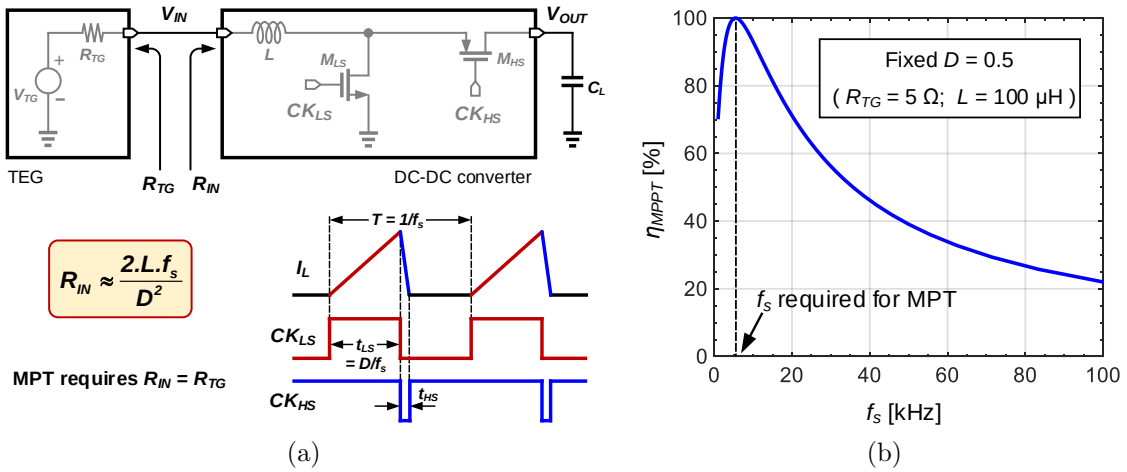


Figure 4.4: (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT.

efficiency of maximum power point tracking, η_{MPPT}, defined as the proportion of the theoretical maximum power entering the converter. TEG being a fairly linear source for small values of ΔT [54], R_{TG} can be assumed constant for body-heat harvesting application. Hence, one-time tuning of the power converter to make $R_{IN} = R_{TG}$ is sufficient to ensure MPT to the input of the boost converter. It saves the additional control power losses consumed in complex continuous MPPT circuits [55] and thereby enhances the end-to-end efficiency.

The input resistance of the DC-DC boost converter operating in DCM mode can be derived by calculating the average input current drawn by it [56]. The expression of R_{IN} when written in terms of D becomes

$$R_{IN} \approx \frac{2Lf_S}{D^2}. \tag{4.9}$$

It is important to mention here that V_{IN} needs to be constant for the approximated expression of R_{IN} in (4.9) to be true. In order to ensure that, a capacitor, C_{TG} (shown in Fig. 4.1) must be connected across the TEG source. The value of C_{TG} has to be chosen depending on the value of the inductor such that, $\sqrt{LC_{TG}} >> t_{LS}$. A steady V_{IN} contributes to the linearity of I_L during t_{LS}. Following (4.9), the f_S of a symmetrical clock ($D = 0.5$) for the DC-DC converter with a fixed value of L can be easily tuned to match R_{IN} with R_{TG} and maximize η_{MPPT} as shown in Fig. 4.4b.

4.1.3 Loss-optimized Maximum Power Transfer (LO-MPT)

Although a fixed f_S of the switching clock with $D = 0.5$ may ensure MPT at the input, it may not be optimum for the normalized loss and results in a low η_{DCDC}. On the flipside, optimum value of f_S for (4.7) with $D = 0.5$ may maximize η_{DCDC} but can result in impedance mismatch at the input and reduces η_{MPPT}. The end-to-end efficiency of the harvester, η_{HARV}, is determined by the ratio of the output power and the theoretical maximum power available from the source. It can be expressed as

$$\eta_{HARV} = \eta_{MPT} \times \eta_{DCDC} \tag{4.10}$$

As such, mere input matching by 'one-dimensional' frequency tuning may not be able to maximize the final output power of the harvester. The efficiency of the converter needs to be maximized while ensuring MPT at the input. The effect is more prominent at ultra-low V_{IN}, when the output power becomes so low that the converter fails to sustain operation. This makes it unsuitable for body-heat energy

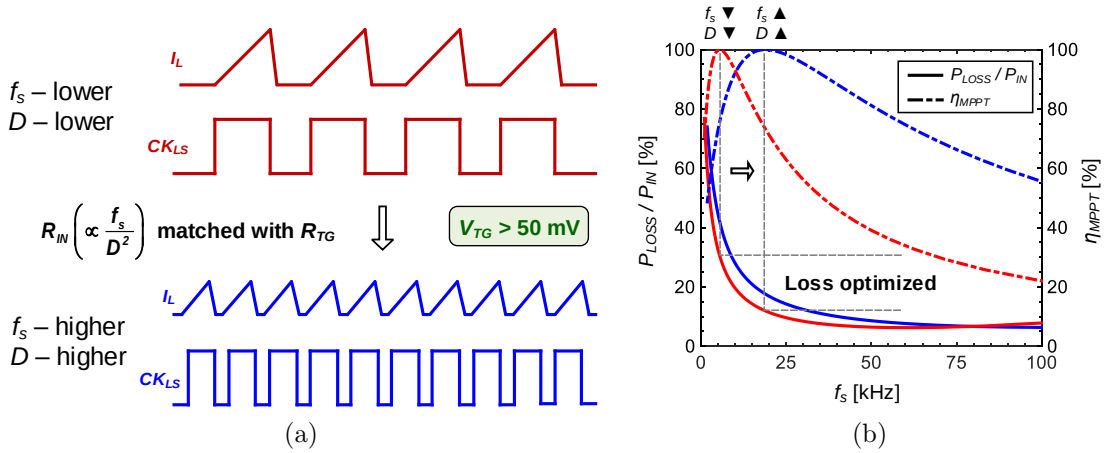


Figure 4.5: (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT.

harvesting.

In this work, we have proposed a loss-optimized maximum power transfer (LO-MPT) approach where η_{DCDC} is maximized by optimizing losses of the converter while keeping R_{IN} matched to R_{TG}. It improves η_{HARV} across the input voltage range and enables the harvester to operate at V_{IN} of few milivolts.

At perfect input matching, $R_{TG} = R_{IN}$, utilizing (4.7) and (4.9), normalized loss can be re-formulated as

$$\frac{P_{LOSS}}{P_{IN}} = \left(\frac{4R_S}{3R_{TG}}\right).\frac{1}{D} + \left(C_S K^2 R_{TG}\right).f_S \tag{4.11}$$

Centimeter-scale TEGs have internal resistance, R_{TG}, of a few ohms [54]. For moderately low TEG voltage, $50\,\text{mV} < V_{TG} < 200\,\text{mV}$, low values of D result in higher conduction loss, as evident from (4.11). In other words, it results in a lower f_S for

input matching (4.9) and increases conduction time. This is illustrated in Fig. 4.5a by the red timing diagram. An increase in D can reduce the conduction loss, but the same f_S will make R_{IN} different from R_{TG}. So, f_S has to be increased accordingly to keep R_{IN} unchanged. This effectively reduces the conduction time as illustrated by the blue plot of Fig. 4.5a. Increase in f_S does not affect the switching loss significantly, as evident in the simulated plot in Fig. 4.5b due to the moderate value of K.

However, for very small TEG voltages, $V_{TG} < 40\,\text{mV}$ the same pair, $\{D, f_S\}$ may not result in an optimal efficiency of the converter. At such low voltages, the input power being small, switching power loss of the converter becomes comparable to the input power and starts to dominate. This is evident from (4.7), where value of the normalized switching loss term increases significantly with the increase of K. The blue continuous line in the simulated plot of Fig. 4.5b exhibits such a behavior. A lower f_S is beneficial in this case as longer conduction time does not affect much in terms of losses due to smaller V_{IN}. However, for MPT the decrease in f_s has to be compensated by a proportional decrease in D, as shown in Fig. 4.5a, and results in optimizing both η_{MPT} and η_{DCDC} depicted by the red lines in Fig. 4.6b.

Hence, in order to improve the end-to-end efficiency of the harvester across the low input voltage range applicable for body-heat energy harvesting application, an adaptive duty-cycle and frequency switching scheme has been chosen for the boost converter.

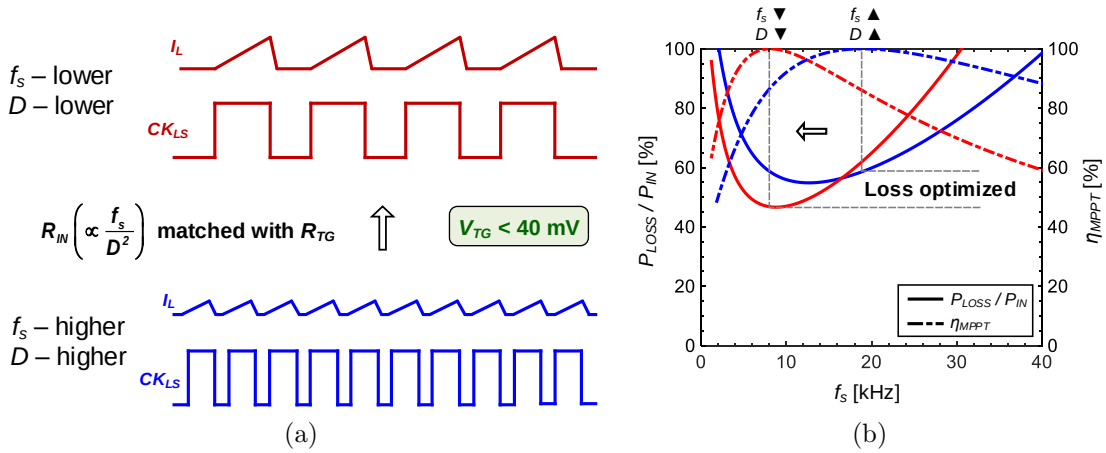


Figure 4.6: (a) Input resistance matching for maximum power transfer (MPT) at the input of the converter, and (b) Tuning switching frequency to a fixed value for 1-dimensional MPPT.

4.2 Circuit Implementations

Autonomous operation of the boost converter needs low-voltage startup circuits to kick-start the asynchronous path of operation of the boost converter. Once the synchronous path of the converter becomes operational, the key circuit blocks that determine the total control power losses need to be designed with special care to sustain ultra low voltage operation needed for thermoelectric energy harvesting from body heat. The following sections describe design of the key circuit blocks to achieve low voltage cold-start and high efficiency of the converter at small input voltages.

4.2.1 Ultra low-voltage integrated cold-start

A voltage multiplier capable of starting operation with small input voltage is primarily needed to power the control circuits of the inductive converter for startup

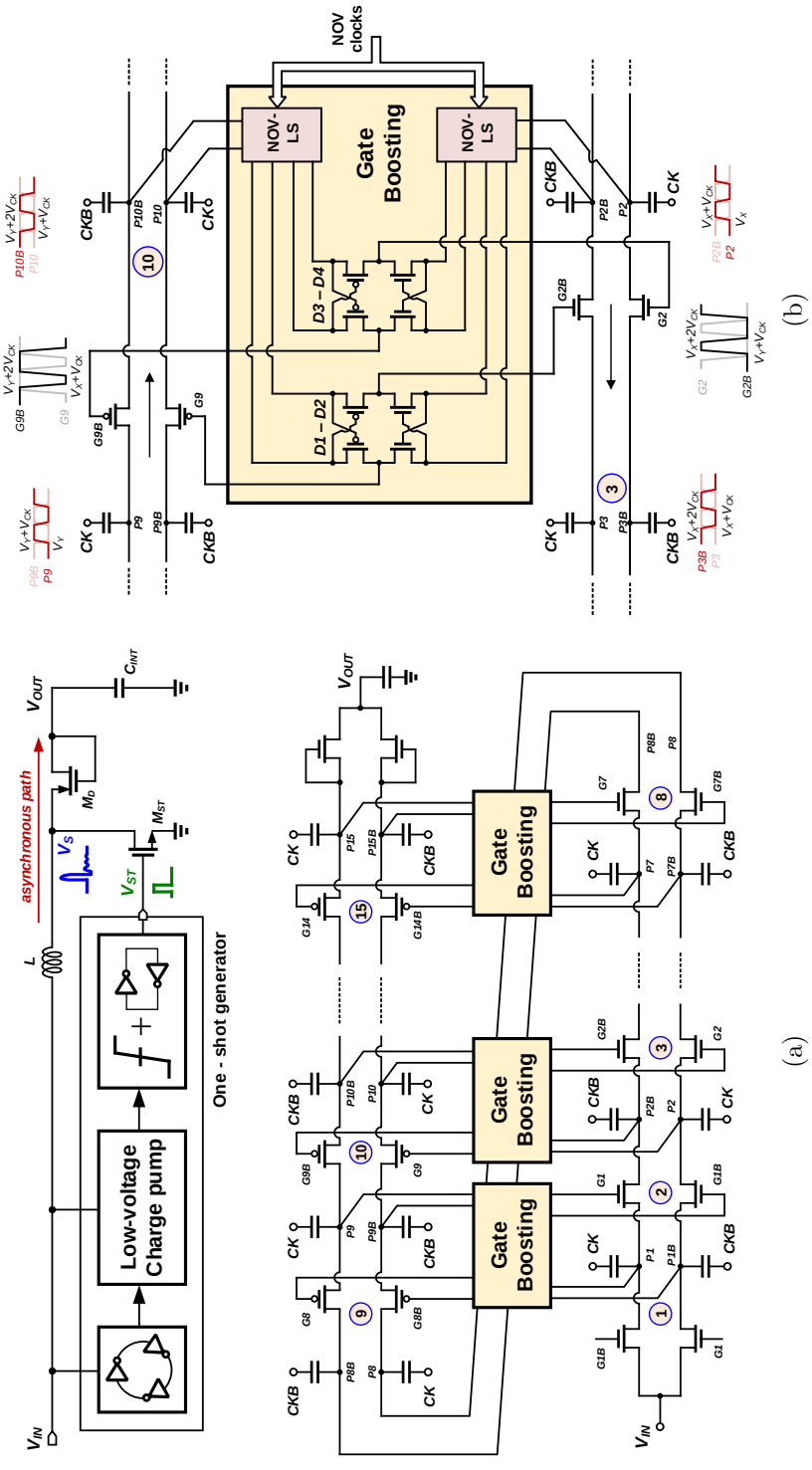


Figure 4.7: (a) One-shot start-up with the proposed on-chip voltage multiplier, and (b) high dual gate-boosting using internal voltages and combination of NMOS and PMOS switches.

[32,35,36]. On-chip voltage multiplication using charge pumps at small input supply is challenging due to the ultra-sub-threshold conduction of the switches. A high-gate boosting technique is demonstrated in [57] to improve the gate overdrives of the switches for improved conduction at small supply. However, it needs multiple charge pumps to achieve the required voltage boosting and thereby consuming area. In this work we present a single charge pump to achieve boosted overdrive for the charge transfer switches (CTS) during the conduction phases of the charge pump stages.

A dual gate boosting architecture is designed where the initial stages of the charge pump use NMOS switches and the later stages use PMOS switches for charge transfer as shown in Fig. 4.12. The charge pump is a dual-phased Dickson architecture [14] with 15 stages in total. The first eight stages use NMOS switches in deep-n-well for charge transfer between successive stages, whereas the later seven stages use PMOS switches. Higher voltages from later stages are fed back to improve gate overdrive of the NMOS switches of the earlier stages. At the same time, lower voltages from earlier stages are utilized to improve the gate overdrive of PMOS switches of the later stages. The dual gate boosting action eliminates the need for additional charge pump stages for gate voltage boosting of the switches of the main charge pump and avoids additional loading improving output resistance and pumping efficiency.

The gate-boosting action of the switches are done in a symmetric way where output nodes of stage 1 & 9, stage 2 & 10, and so forth, are used to generate gate drives of the respective CTSs. As shown in Fig. 4.7b, dual-phased voltages, $P2$ and $P2B$ at the output of stage 2 and $P10$ and $P10B$ at the output of stage 10 are used to generate gate clocks $G2 - G2B$ and $G9 - G9B$, respectively us-

ing dynamic inverters, $D1 - D4$. The gate clocks, $G1$ and $G1B$ for the second stage are reutilized in the first stage with appropriate phases to avoid additional stages of charge pump. The final stage of the charge pump is comprised of a diode-connected deep-n-well NMOS to avoid reverse charge flow during a voltage droop at the output. The boosted gate clocks are required to be non-overlapping with the pumping clock phases, CK and CKB to avoid reverse charge flow between consecutive stages of the charge pump during non-charge transfer phases. In order to generate the non-overlapping phases of the internal dual phased voltages clocks $CK_{NOVA}, CK_{NOVB}, CKB_{NOVA}$ and CKB_{NOVB} and level shifters are used [57]. A stacked-inverter based ring-oscillator [43] is adopted to generate on-chip start-up clock at small input voltages. The stage capacitance is chosen as 22 pF to achieve low enough SSL output impedance, $N/(Cf_s)$ [19] with the smallest possible sizes of the CTS to avoid higher loading of the weakly driven gate clocks. The non-overlapping phases of the gate clocks are designed with proper care to avoid reverse charge flow during the slow rising as well as the falling edge of the large swing gate clocks. It is important to note that although a high gate-boosting action takes place as the internal voltages gradually increase towards the steady state value, initial voltage boosting is slow and is dependent only on the leakage current of the switches. However, usage of PMOS switches for the later stages allows boosting of the later stages quickly, that follows boosting of the NMOS switches and the circular action results in a sudden dual gate boosting resulting in a faster build up of the output voltage, V_{CP}.

The boosted voltage, V_{CP} is utilized to power a one-shot generator implemented

with ultra-low power circuits. The basic building block of the one-shot generator, as shown in Fig. 4.8, comprises a two transistor reference generator [47], leakage based comparator, and a thyristor based delay element [48] to generate a one-shot. The sharp falling edge of the one-shot creates inductive overshoot at V_S and kick starts the inductive boost converter by turning on the diode, M_D.

4.2.2 Zero current switching for high-efficiency synchronous boost converter

The boost converter is operated in DCM mode favorable for low power operations [20]. In this mode of operation the inductor needs to be disconnected from the output once the current, I_L, reaches the zero point to avoid reverse flow of current from output to the inductor. Compared to analog sensing of the inductor current digital flip-flop based sensing [38] is highly power saving and is adopted in this implementation.

The ZCS circuit block as shown in Fig. 4.9a consists of a digital flip-flop that detects the inductive overshoot at node V_S to sense the condition of I_L. The flop is

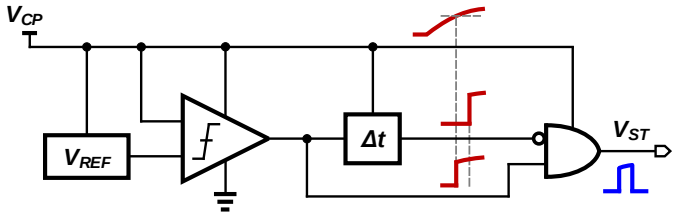
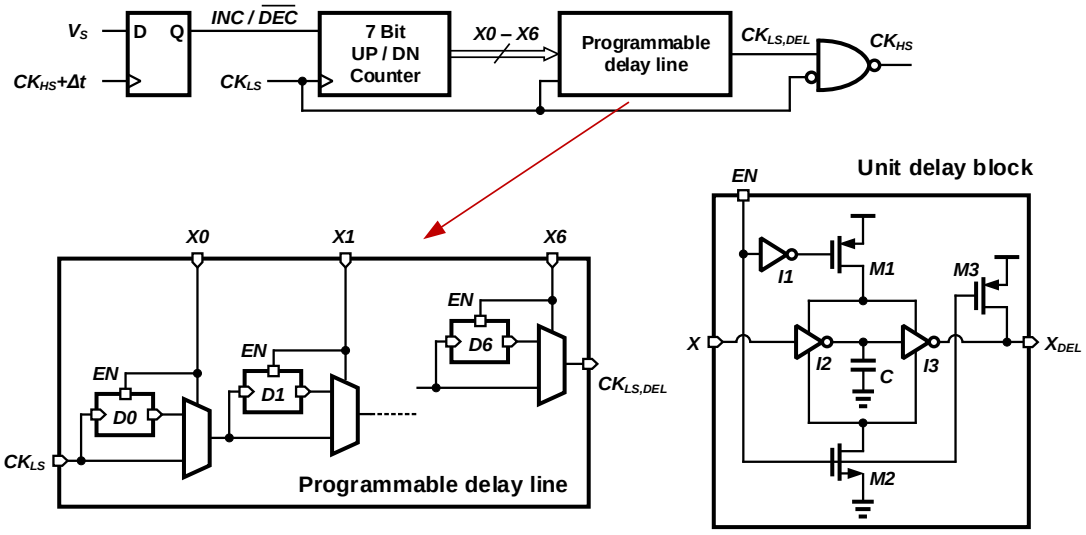
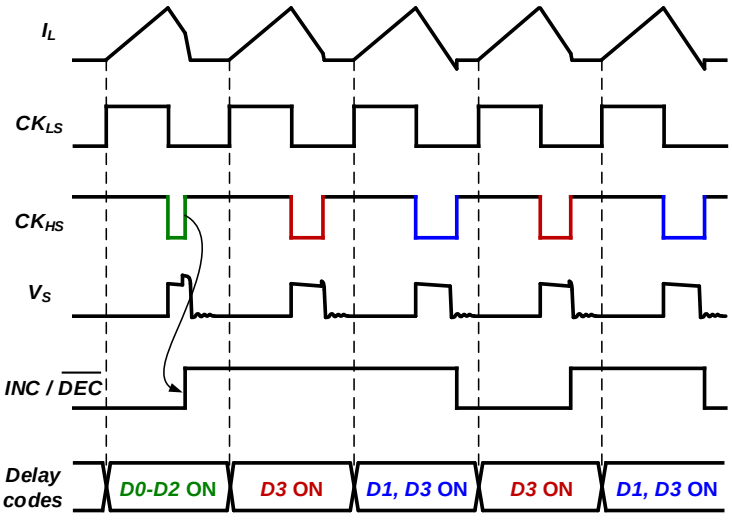


Figure 4.8: Generation of one-shot powered by the output voltage of the charge pump.



(a)

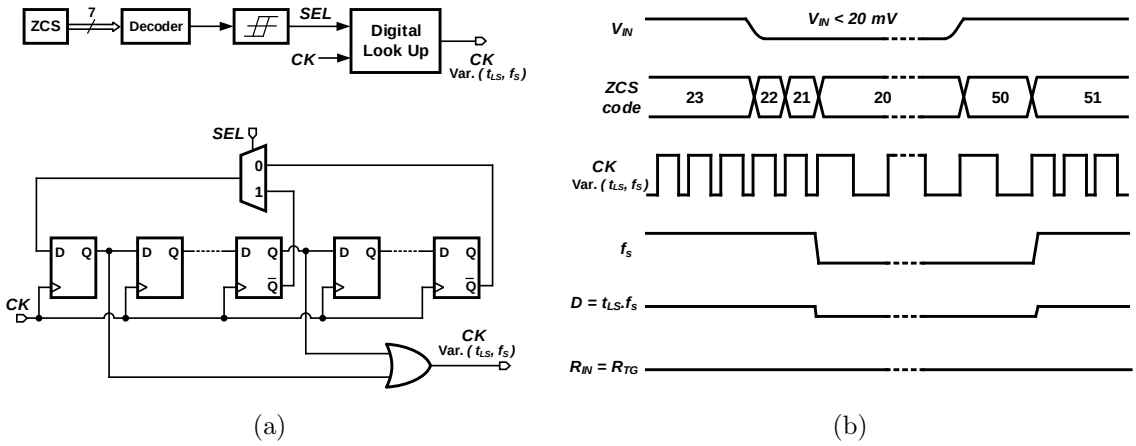


(b)

Figure 4.9: (a) Implementation of zero current switching (ZCS) using digital sensing along with the sub-blocks of the delay line, and (b) timing diagram showing operation of ZCS.

triggered with the rising edge of CK_{HS} as to sense V_S serving as the data input to the flop. As illustrated by Fig. 4.9b, a rising edge of CK_{HS} will sense a high output when the inductor energy is not transferred fully to the output, and I_L is yet to reach the zero value. The resulting output ($INC/\overline{DEC}$) directs a counter to increment its current state. The incremented value of the counter selects a higher delay from a programmable delay block to create a wider low time of CK_{HS} to allow complete transfer of the inductor energy to the output in the consecutive cycle. A low in the $INC/\overline{DEC}$ signal indicates that inductor energy has already transfered to the output and current has started to flow from the output to the input. This directs the counter to decrement its current value and the delay is reduced to generate a smaller time window of HS switch on-time in the following cycle. At steady state, the counter value oscillates between two nearest values. This kind of digital sensing avoids any static current and reduces the power consumption significantly. However, in order to accomodate a wide range of input voltage, the delay line needs to be well programmable to generate very small delay to large delay for high to low conversion ratios, respectively.

Implementation of a delay line with RC delay elements incurs high power consumption due to higher switching loss ($fCV_{DD}{}^2$) and also high shoot-through or crow-bar current due to slow transition. In order to avoid this, a programmable delay line comprising a low power unit delay block is designed as shown in Fig. 4.9a. The pull-up ($M1$) and pull-down transistor ($M2$) are controlled in such a way that no shoot through current is drawn from the supply during the delay time. Also, the delay blocks are disabled when not in use, saving a lot of power for very low input



(a) (b)

Figure 4.10: (a) Implementation of loss-optimized maximum power transfer (LO-MPT) using digital circuits, and (b) timing diagram showing adaptive on-time and frequency of switching clock for optimizing loss of the converter while ensuring maximum power transfer at input.

voltages. The timing diagram in Fig. 4.9b shows how the delay blocks are enabled and disabled selectively based on the sensing outcome of the flip-flop.

4.2.3 Variable clock generation for LO-MPT

The proposed LO-MPT scheme requires sensing of the input voltage, V_{IN} to vary the duty-cycle (D) and switching frequency (f_s)of the clock. Instead of spending power in sensing V_{IN}, we reused the ZCS circuit to achieve a comprehensive tracking of V_{IN}. As long as output voltage V_{OUT} and on-time of the LS switch, t_{LS}, is fixed the on-time of the HS switch is directly proportional to V_{IN}, as evident from (4.1). Hence, the current t_{HS} value can be used to sense the V_{IN}.

The output of the counter of the ZCS circuit is used to decode V_{IN} using a

decoder as shown in Fig. 4.10a. When V_{IN} goes below 20 mV, a lower f_s clock is generated with a smaller D to optimize the loss of the converter, as described in Section 4.1.3. Whereas, for higher V_{IN} a switching clock with higher f_s and higher D is chosen. The (D, f_s) pair of the clock are generated with the help of a digital circuit as shown in Fig. 4.10a comprising a series of flip-flops to generate different f_s. A logical operation of the internal signals generate two different D for the two zones of V_{IN}. In order to avoid to-and-fro across a particular V_{IN} that may lead to a wrong switching clock, a hysteresis loop needs to be added. A digital hysteresis is designed using combinatorial logic that takes the counter state as input and decides to select the lower (D, f_s) value only when V_{IN} goes below 20 mV. When V_{IN} increases, the higher (D, f_s) pair is only chosen when the V_{IN} crosses 30 mV. The timing diagram Fig. 4.10b illustrates the operation of the LO-MPT circuit with an example situation when a sudden change in input results in a change of the code, and the clock adapts to newer (D, f_s) pair to optimize the efficiency of the boost converter while keeping the input impedance of the converter matched to R_{TG}.

4.2.4 Dual-path operation and output voltage regulation

The dual path converter architecture proposed in this work helps in achieving fast cold-start at small input voltage as well as high efficiency boost conversion during normal mode of operation utilizing the same off-chip inductor. In order to make sure the asynchronous path feeds the required control power when V_{OUT} is yet to reach a stable voltage, the voltage regulation loop needs to be active right after the

cold-start. The voltage regulator gets activated immediately with the rise in V_{INT} following the strobe cycle and starts tracking V_{INT}.

A switched capacitor voltage divider is used to sense change in V_{INT} without consuming static power. The $V_{INT}/2$ is compared against two on-chip leakage based voltage references, $V_{REF,LO}$ and $V_{REF,HI}$. The reference voltages are generated using ultra-low power reference generator [58] which reaches the steady state at a decently fast time. The output of the comparators are fed to RS latch to generate a control signal that decides whether V_{INT} needs power or not. During the start-up this information is used to control the dead-time (ΔT) between CK_{LS} and CK_{HS}. Enabling ΔT results in flowing of the inductive current through the diode, M_D, for a short time and refill V_{INT} before the current is steered to the V_{OUT}. This process continues until V_{OUT} crosses 1 V and get shorted with V_{INT}. The same voltage regulation loop now senses V_{OUT} and uses its decision to enable or disable the whole converter by gating the clock, resulting in a energy-efficient hysteretic mode of regulation. The ripple of V_{OUT} depends upon the accuracy of the two thresholds, $V_{REF,LO}$ and $V_{REF,HI}$, and the comparator offset.

4.3 Measurements

The self-starting boost converter is implemented in a 0.18 µm CMOS process and occupies an active area of 1.02 mm^2. The die micrograph is showin in Fig. 4.11. An off-chip inductor of 100 µH is used along with off-chip storage capacitors C_{TG} and C_L. The performance of the chip is characterized with a bench top power supply

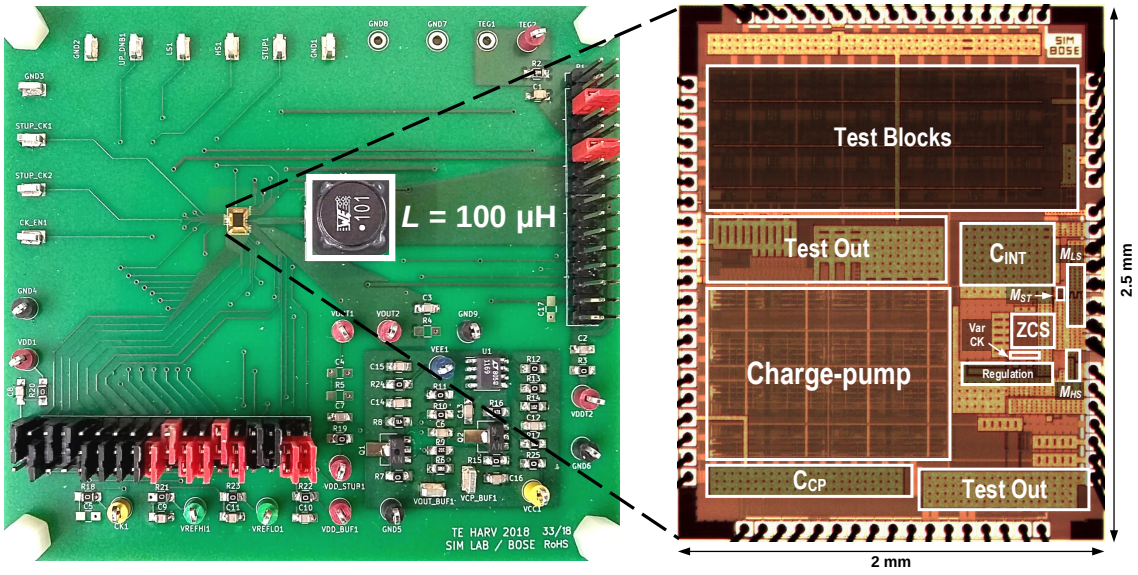
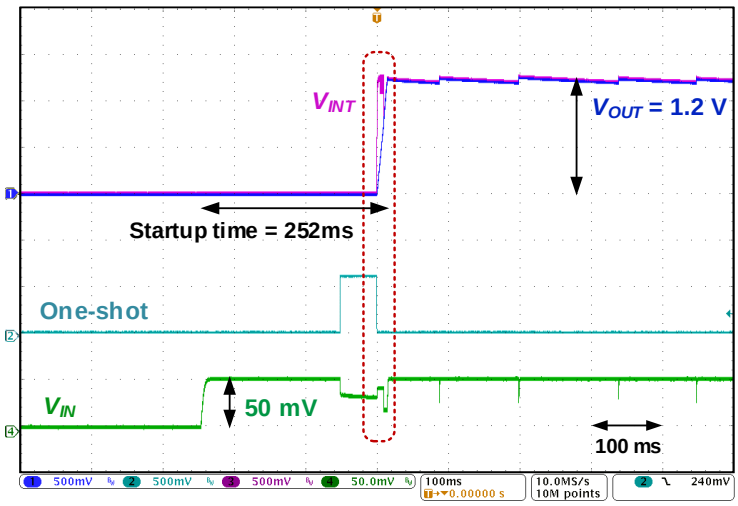


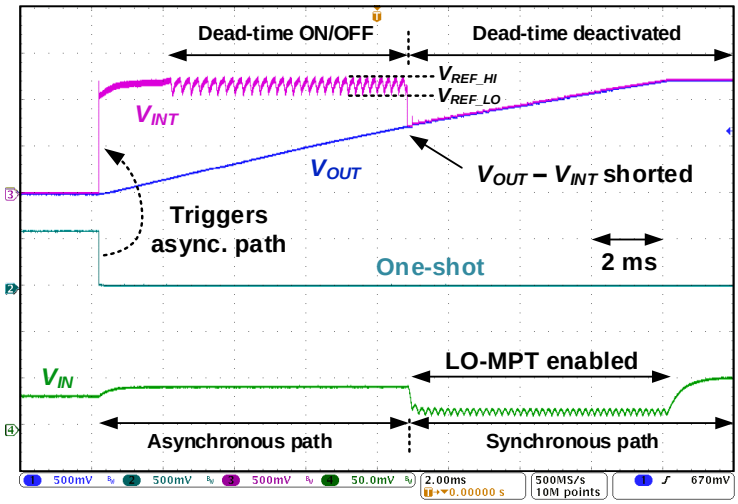
Figure 4.11: Printed circuit board (PCB) with chip-on-board for testing. Die photograph of the chip fabricated in 0.18 µm CMOS technology is shown in the right.

with a series resistance equivalent to the source resistance of the TEG. Also, the chip is tested with a commercial TEG.

Measured start-up transients are shown in Fig. 4.12a. It shows that the boost converter self-starts with a minimum TEG voltage (V_{TG}) of 50 mV and takes only 252 ms to start-up. The output load capacitor is 1 µF. Magnified waveform in Fig. 4.12b shows the parallel operation of the asynchronous and the synchronous path of the boost converter. The falling edge of the strobe triggers the asynchronous path, which feeds power to the control circuits for the synchronous path of operation. Dead-time based V_{INT} regulation continues until V_{OUT} gets shorted with it, and the converter enters into high-efficiency primary mode. The LO-MPT is enabled only after this and the hysteretic on-off voltage regulation regulates V_{OUT} at 1.2 V. The start-up time varies with V_{TG}, the higher the voltage, the more output power of the voltage-



(a)



(b)

Figure 4.12: (a) Measured start-up transients shows cold-start of the harvester: from the input turned on to reaching a regulated output voltage of 1.2 V, with a minimum input voltage of 50 mV in 252 ms, and (b) zoomed waveform shows one-shot triggered cold-start sequences including parllel asynchronous - synchronous operation of the single inductor boost converter.

Table 4.1: Startup times at different source voltages

Source voltage	Startup time
50 mV	252 ms
75 mV	42 ms
100 mV	21 ms

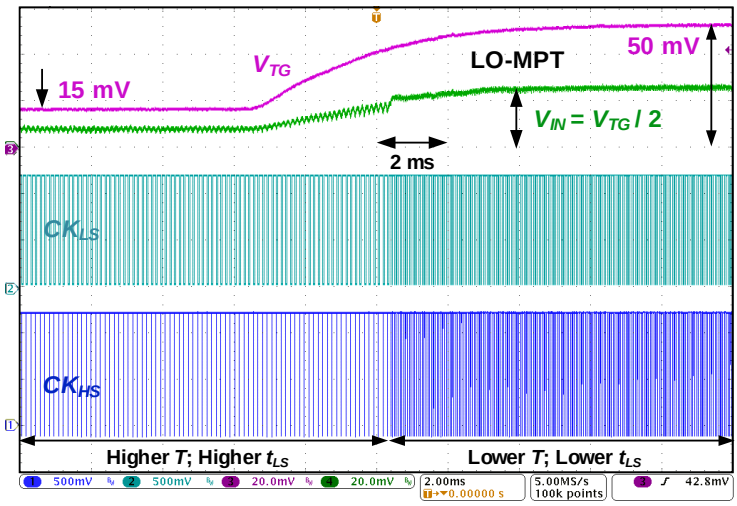


Figure 4.13: Measured transients showing adaptive change of on-time and frequency of switching clock with variation of input voltage for loss-optimized maximum power transfer (LO-MPT) at the input of the converter.

mutiplier, the faster is the cold-start. The variation of start-up time for different values of V_{TG} are tabulated in Table 4.1

The operation of the LO-MPT is shown in the measured transient plot in Fig. 4.13. It shows that as soon as the TEG voltage transits from 15 mV to 50 mV, the switching clock changes the (D, f_s) pair to optimize the efficiency of the converter. The new pair still maintains the matching of input resistance and ensures maximum power transfer at the input of the converter.

Once the converter enters into the primary mode of operation, the cold-start block

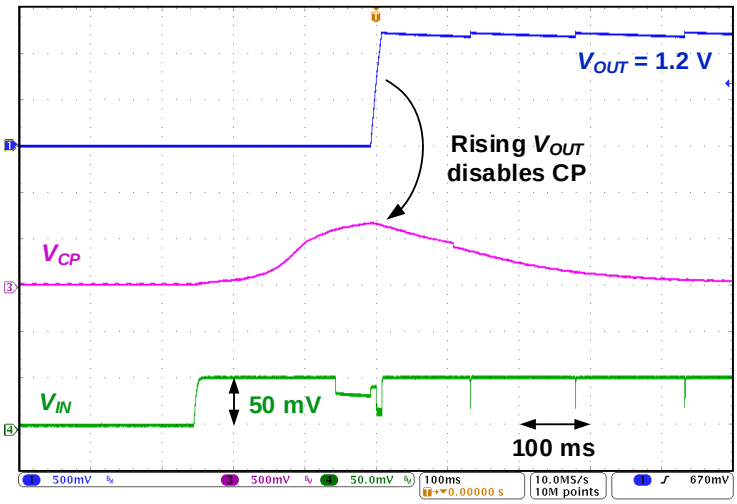


Figure 4.14: Disabling the cold-start low-voltage charge pump with the activation of high-efficiency synchronous path of the boost converter. It not only improves the end-to-end efficiency of the converter, but also enables the harvester to accomodate higher input voltages without stressing devices in the high step-up charge-pump.

is disabled by disabling the start-up clock. Figure 4.14 shows how the rising V_{OUT} disables the start-up voltage multiplier and avoids unneccessary power consumption during the normal mode of operation.

The load and line regulation of the boost converter are shown in Fig. 4.15 where V_{OUT} is regulated by the on-voltage regulation when V_{TG} changes from 20 mV to 50 mV and 80 mV. Load current transient from 1 µA to 60 µA and then to 10 µA do not affect the V_{OUT} as shown assuring line regulation. The ripple of the V_{OUT} depends upon the input power from V_{TG} and output power drawn by I_L.

The efficiency of the boost converter and the end-to-end efficiency of the harvester are characterized using a source meter (Keithley 4120). For each V_{TG}, the output current I_L is varied and the unregulated V_{OUT} is noted down. One such I-V plot of

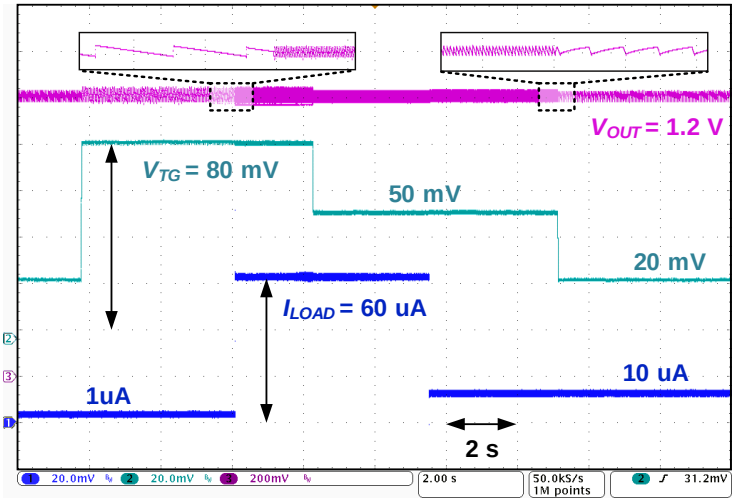
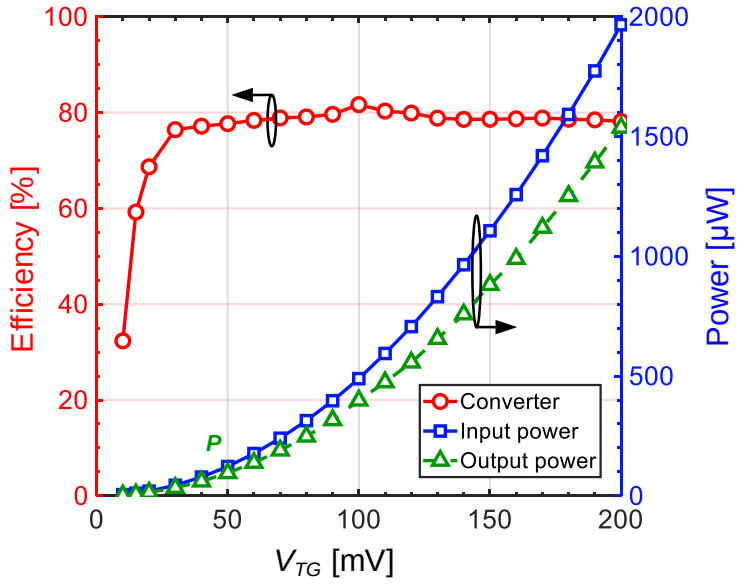
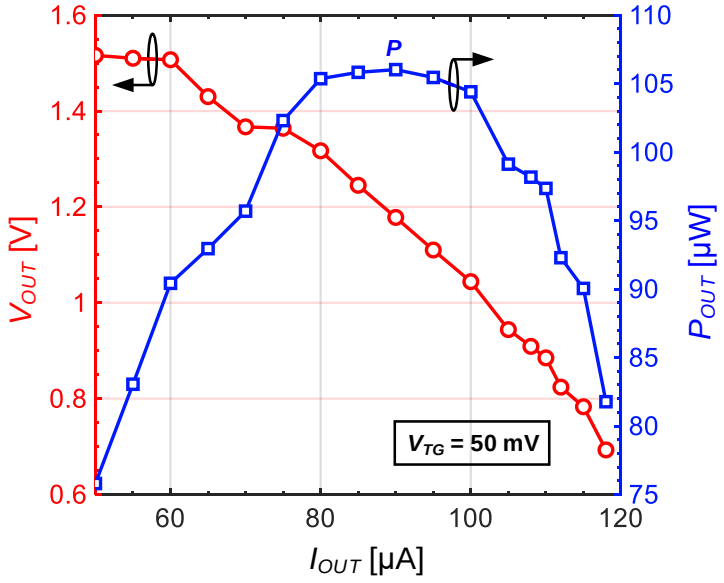


Figure 4.15: Load and line regulation of the output of the boost converter.

the output is shown in Fig. 4.16a where the TEG voltage, V_{TG}, is kept at 50 mV. The maximum output power point (P for $V_{TG} = 50\,\text{mV}$) of each of those individual plots for different values of V_{TG} are used to plot the final efficiency of the boost converter, as shown in Fig. 4.16b. The converter achieves an efficiency of more than 75 % for a V_{TG} above 30 mV and a V_{IN} above 15 mV. The peak efficiency of the boost converter is 82 % and is achieved with a V_{IN} of 50 mV ($V_{TG} = 100\,\text{mV}$). The corresponding end-to-end peak efficiency is 80 %. The high end-to-end efficiency of the harvester at low input voltage enables the converter to sustain operation at a V_{IN} as low as 3.5 mV, thanks to the LO-MPT scheme. The operation of the harvester at that condition is shown in the measured transient plot in Fig. 4.17. The converter can provide an output regulated voltage of 1.2 V with a load current of 20 mA and an efficiency of less than 10 %. The operation of the converter at such a small input voltage makes it suitable for thermoelectric energy harvesting from human body heat.



(a)



(b)

Figure 4.16: (a) Measured efficiency of the boost converter with input power and output power for varying TEG voltage, and (b) I-V plot of the output of the harvester at a fixed TEG voltage of 50 mV. The measured peak output power in plot (b) corresponds to the input power point (P) for $V_{TG} = 50$ mV in the plot (a).

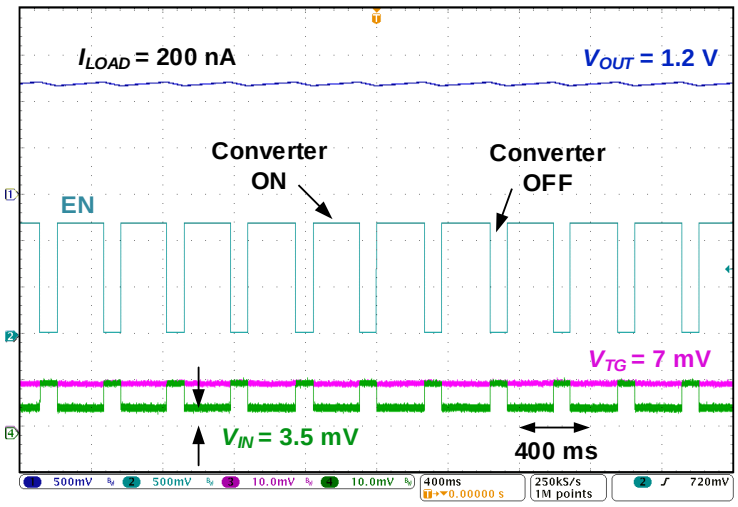


Figure 4.17: Measured Transients showing operation of the converter at the smallest input voltage with an output regulated voltage of 1.2 V.

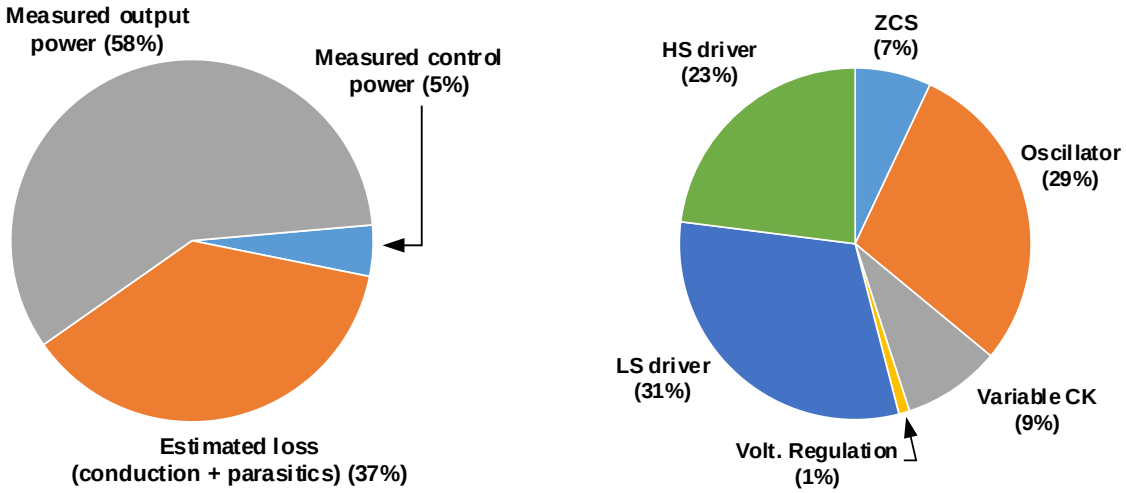


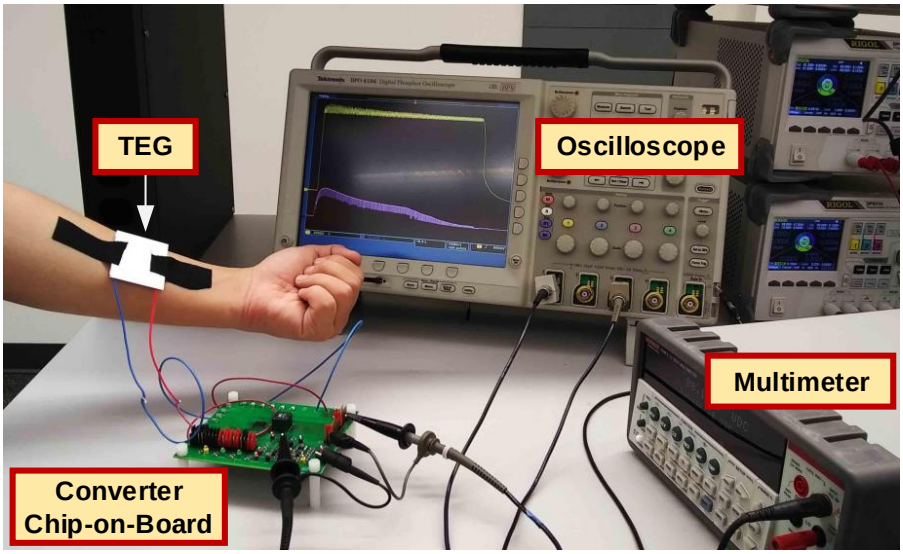
Figure 4.18: Power distribution at $V_{TG} = 15\,\text{mV}$: (a) measured power with estimated loss, and (b) simulated control power break-up.

The distribution of the harvested power utilization in Fig. 4.18a shows that a majority of the loss is dominated by the conduction loss. The control power loss

is comparatively less and is contributed by the different sub-blocks which is shown in the simulated distribution in Fig. 4.18b. The converter consumes a quiescent current of 470 nA at a V_{TG} of 50 mV and scales down to 240 nA for a V_{TG} of 7 mV by adopting the LO-MPT technique using adaptive duty-cyle and frequency of the switching clock.

The startup performance of the harvester is also tested with a commercial TEG (Marlow TG12-6-01L). The measurement setup of the experiment is shown in Fig. 4.19a and the measued transient scope output is shown in Fig. 4.19b. It shows that the harvester self-starts with a temperature gradient of just 1.4 °C and sustains operation until the temperature difference between skin and environment falls below 0.2 °C. The varying ripple at the beginning of the measured transient is due to the coupling of output change to the on-chip reference voltages, changing the hysteresis value for regulation.

The performance of the implemented harvester is compared against state-of-the-art thermoelectric harvesters in Table 4.2. It shows that the proposed architecture achieves a high efficiency across a wide range of milivolts of input and can sustain operation at the smallest input voltage (3.5 mV) reported so far. In addition, the self-start of the converter at 50 mV without using additional off-chip bulky elements make the proposed boost converter suitable for powering portable micro-power wearables using body-heat only.



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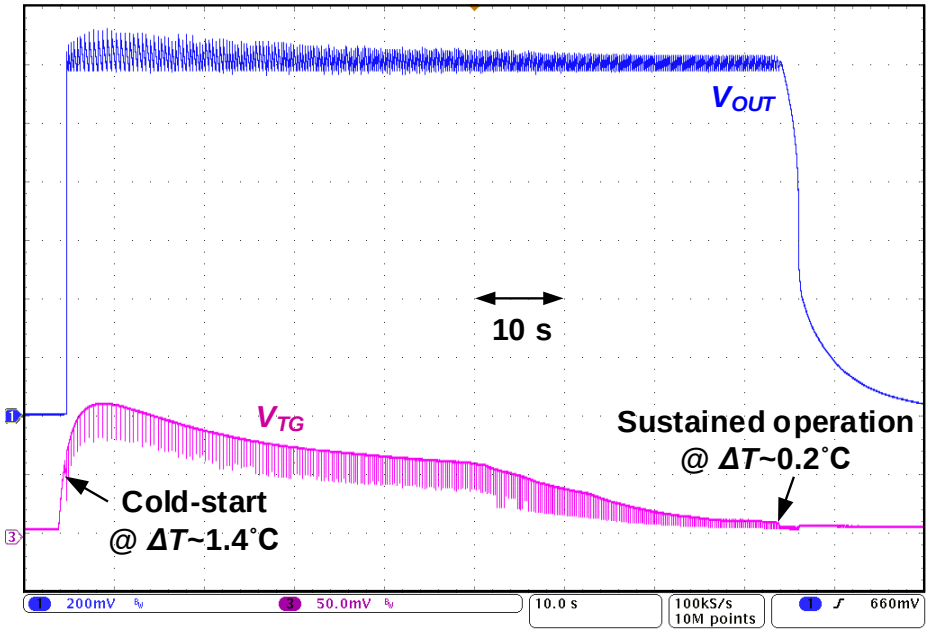

(b)

Figure 4.19: (a) Measurement setup with commercial TEG, and (b) measured transient of the harvester.

Table 4.2: Performance comparison with state-of-the-art thermoelectric energy harvesters

References	JSSC'13 [32]	JSSC'18 [33]	JSSC'12 [31]	JSSC'15 [29]	TCAS'18 [37]	JSSC'16 [36]	JSSC'19 [59]	**This work**
Process	65 nm	65 nm	0.13 µm	0.13 µm	65 nm	0.13 µm	0.18 µm	**0.18 µm**
Start-up integration	Off-chip Inductor	Off-chip Inductor	Off-chip Xformer	On-chip	On-chip	On-chip	On-chip	**On-chip**
Min. V_{TG} for cold-start	50 mV	40 mV	40 mV	220 mV	210 mV	70 mV	129 mV	**50 mV**
Start-up time	22 ms (1)	180 ms (1)	22 s (1)	3.5 s (1)	2.3 s (1)	1.5 s	150 s (1)	**252 ms**
Min. V_{TG} for operation	30 mV	40 mV	-	20 mV	14 mV -	-	50 mV	**7 mV**
V_{OUT}	1.2V	1.1 V	2 V	1.1 V	1.4 V	1.25 V	0.8 V	**1.2 V**
Regulation	Yes	Yes	Yes	No	Yes	Yes	Yes	**Yes**
MPPT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Peak efficiency	73 %	75 %	61 %	83 % (2)	71.5 %	59 %	84 %	**80 %**
Efficiency @ low V_{TG}	45 %	12 %	32 %	21 % (2)	50 %	-	23 %	**58 %**
No. of Inductors	3	2	1	1	1	1	1	**1**

(1) Estimated from transient plots, (2) Converter efficiency only.

4.4 Chapter summary

A single-inductor boost converter is demonstrated capable of achieving high efficiency at small input voltages from a TEG attached to human body. Enhanced efficiency of the converter while ensuring maximum power transfer at the input enables the complete harvester to achieve high end-to-end efficiency across the input voltage range, thanks to the proposed LO-MPT scheme using variable switching clock with adaptive on-time and frequency. This not only helps to achieve the peak efficiency at lower input voltage but also to sustain operation at a voltage as low as 7 mV from the TEG, which corresponds to a ΔT of 0.2 °C. One-shot integrated cold-start with the aid of dual-path converter architecture achieves low voltage cold-start and makes the harvester completely autonomous by removing the need of battery at any stage of operation. Cold-start of the proposed harvester with a minimum TEG voltage of 50 mV is the lowest startup-voltage reported to date with single inductor architecture. All these features together make the implemented TEG-based harvester ideal for powering energy-efficient wearables utilizing human body heat.

Chapter 5: Batteryless Heartbeat Detection System Powered by Human Body Heat

Wearables are emerging as more than just a form of entertainment. Miniaturized body worn devices can be used for continuous monitoring of vital signs in point-of-care diagnostics because of their convenience compared to fixed clinical environments. However, prolonged usage is difficult with battery-powered devices at the wearable form-factor. Ambient energy harvesting can provide power autonomy to wearables and enable infinite lifetime. But accurate measurements in unfavorable conditions can be power consuming [60], which challenges autonomous wearables medical competency under rigid constraints of harvested micro-power.

5.0.1 Proposed batteryless heartbeat detection system-on-chip

In this work, we present a batteryless heart beat monitoring system that solely sustains on energy harvested from human body heat. The autonomous system-on-chip (SoC) shown in Fig. 5.1 comprises a power management unit (PMU) that starts with less than 60 mV output of a centimeter-scale thermoelectric generator (TEG) and keeps transferring maximum power available from the body heat. A signal processing analog front-end acquires, amplifies and shapes ECG signal to derive the heartbeat information. An energy-efficient adaptive threshold and decision scheme is proposed that is utilized to detect heartbeats with higher than 99% accuracy in

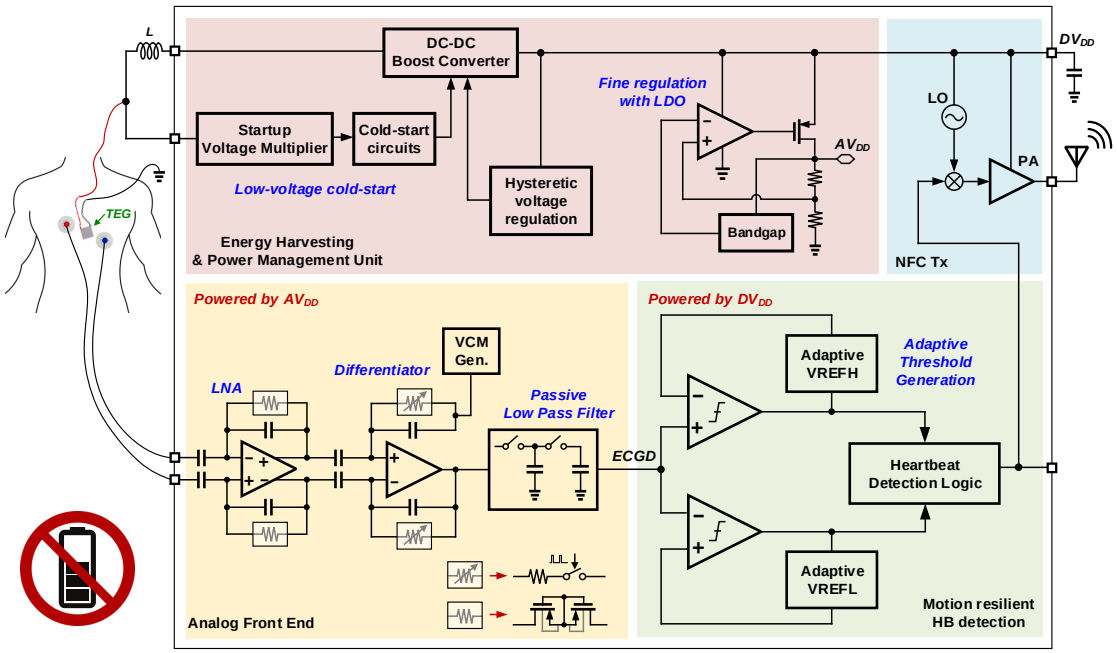

Figure 5.1: Block diagram of the human body heat powered, motion-resilient heartbeat monitoring system-on-chip.

presence of motion artifacts. The detected heartbeats are wirelessly transmitted to a base station receiver using near field communications (NFC) for power intensive post processing. The proposed batteryless wearable is able to detect and transmit heart beats with a minimum power of 20 µW and is favorable for preventive healthcare.

5.0.2 Integrated power management unit for harvesting body heat

Thermoelectric energy harvesting exploiting human body heat is favorable for powering wearables due to its continuous availability across indoor and outdoor conditions [10]. Low-voltage and low power from a wearable form-factor TEG at small

temperature difference (ΔT) between skin and environment requires efficient DC-DC boost conversion. A low-voltage boost converter is designed to operate in discontinuous conduction mode (DCM) conducive for power constrained applications. The converter self-starts with the aid of low voltage on-chip voltage multiplier [57] and energy efficient integrated cold-start circuits as shown in Fig. 5.1. A single inductor topology of the self-starting boost converter eliminates additional bulky elements and makes the harvester wearable compatible. The switching frequency of the DC-DC converter is tuned one time to match its input impedance with that of the fixed TEG resistance to extract maximum power. Once cold-start is done, the output voltage (DV_{DD}) is regulated at 1.5 V by means of power efficient voltage mode hysteresis loop using two on-chip thresholds. The larger voltage ripple due to hysteretic regulation makes DV_{DD} unsuitable for powering low-noise ECG signal acquiring analog front end (AFE). A low-I_Q linear regulator with high PSRR (> 50 dB) is designed with an embedded nanowatt bandgap reference circuit powered by the same regulated supply. This generates ripple-less steady voltage (AV_{DD}) of 1.2 V for powering the AFE. The DV_{DD} being connected to a large decoupling off-chip capacitor of 1 µF can support higher switching current and is used for powering digital blocks without wasting unnecessary power for fine regulation.

5.0.3 Heartbeat detection from a wearable perspective

Heartbeats are essentially occurrences of the QRS complex in an ECG and can be detected simply by comparing a clean signal against a fixed voltage threshold

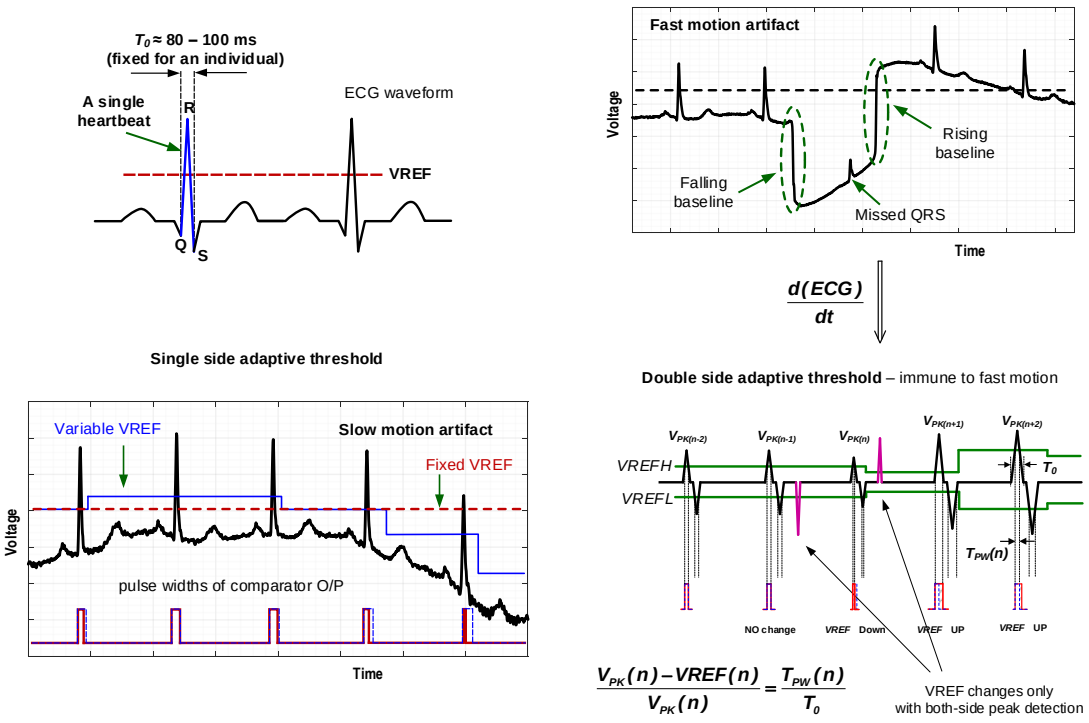

Figure 5.2: Proposed adaptive voltage reference generation and tracking technique with double-sided threshold generation for robust heartbeat feature extraction in the presence of motion artifacts.

(VREF) as shown in Fig. 5.2. A noiseless clean ECG is easy to record by a robust low-noise AFE in the clinical-setup of a hospital, but is most unlikely to be captured by an ultra-low power AFE of a self-sustaining wearable in the noisy atmosphere of everyday work. An AC-coupled low noise amplifier (LNA) and additional analog filter in the front end can only filter out DC offset of the electrodes and fixed frequency line noise, but is incapable of filtering arbitrary motion artifacts. In this work, a power efficient simple digital loop is proposed that can generate threshold voltage adaptive to human motion.

5.0.3.1 Proposed adaptive threshold generation for motion resilient heartbeat detection

The duration of the QRS complex is fairly constant for an individual. Motion artifacts can be characterized by increasing amplitude of the QRS complex and sudden rise or fall of the ECG signal as illustrated in Fig. 5.2. Comparison with a fixed VREF will result different pulse widths (PW) of the comparator output implying motion of the subject. On the contrary, comparison of present PW against a fixed PWREF and generation of a voltage (ΔV_{PK}) proportional to the pulse width error ($\Delta T_{PW} = T_{PW} - T_{PWREF}$) can be utilized to update VREF in the next cycle. Therefore, the voltage shifts in the QRS peak value of ECG caused by motion can be translated to time information and fed back to update threshold voltage of detection. However, such a VREF update will be slow and limited by the heartbeat rate. Sudden movements may cause instant rising or falling of the ECG baseline. Those high-frequency edges will not be captured by the PW comparison described earlier. A differentiator, realized with a high-pass filter in the AFE (Fig. 5.1), can easily mark out those edges. Also, it produces a bipolar peak for each occurrences of QRS complex, as shown in Fig. 5.2. Detection of both the peaks can validate a true heart beat and distinct from the one-side peaks due to fast motion artifacts. In the proposed motion resilient heart beat detection technique, an adaptive threshold voltage generation is implemented to sense the change in the pulse width of the differentiator output (ECGD) on both high and low sides rather than doing the same on single-sided QRS peaks of the ECG signal. As such, the generated VREFs

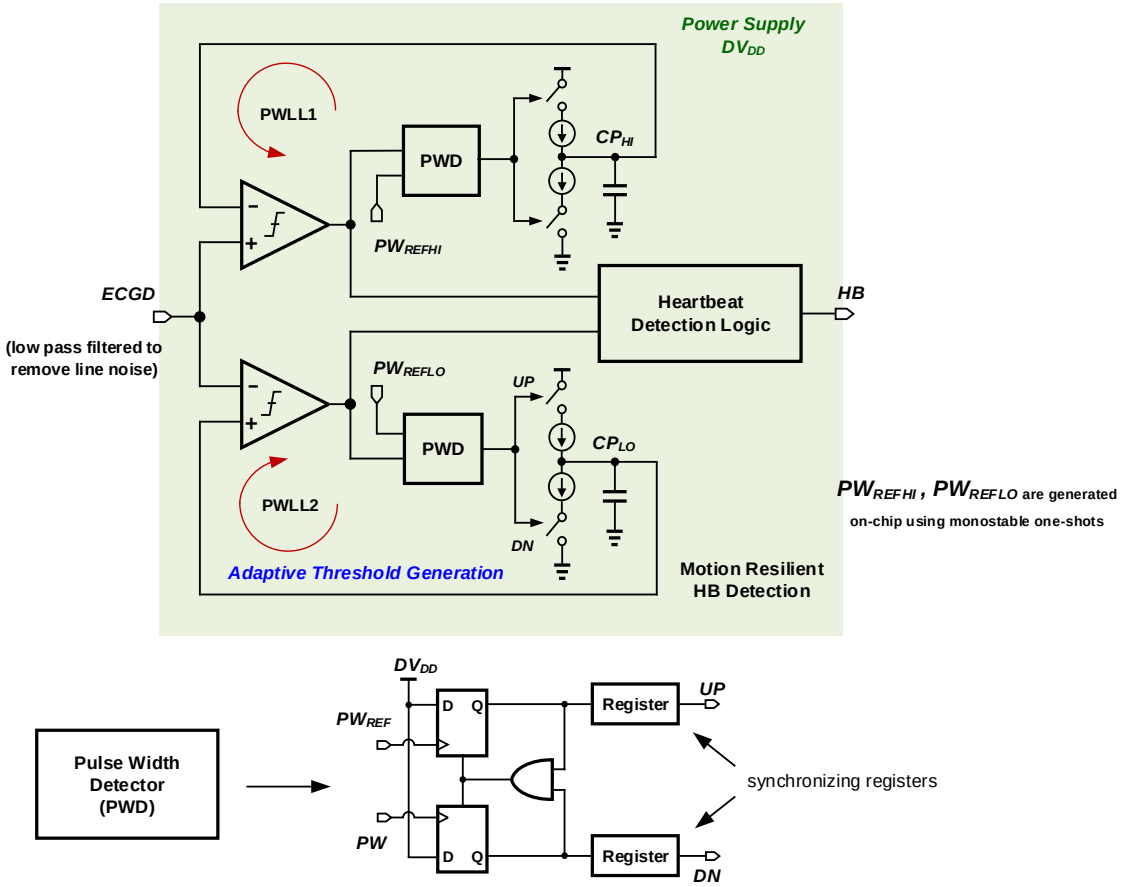

Figure 5.3: Implementation of adaptive threshold generation using pulse-width locked loop (PWLL).

(VREFL and VREFH) adapt to slow as well as fast motion artifacts.

5.0.3.2 Energy-efficient circuits for adaptive threshold generation

The implementation of the adaptive VREF generation is shown in Fig. 5.3. It comprises a pulse width locked loop (PWLL) which works in the same fashion as a

simple phased locked loop (PLL). Pulse-width ($T_{PW}(n)$) of the comparator output on comparing ECGD against current VREF will be subtracted from a preset reference pulse-width, T_{PWREF}. The difference, ΔT_{PW}, is converted to a proportional voltage, ΔV, and added to the present $VREF$ using a pulse width detector (PWD) and a charge pump (CP). The next comparison is done against the updated $VREF$. Although double-side peak detection results in dual PWLLs, the increase in power consumption is negligible due to the low frequency updating of the $VREF$. In addition to motion resilience, the proposed technique eliminates the need to generate a PVT-tolerant fixed voltage reference and reduces static power consumptions. Nevertheless, an initial $VREF$ is required to start the loop, which is generated with relaxed tolerances using ultra-low power leakage based voltage reference generators. $VREF$, resulting from the proposed technique, trains itself within the first few cycles of the ECG and settles to a particular value based on the QRS duration of a certain individual, removing the need for calibration. Detected heart beats in the form of 1 ms bursts are finally transmitted wirelessly by near field communication (NFC) at 13.56 MHz using a simple on-off keying (OOK) modulation scheme. A prototype of the system is implemented in a 0.18 µm CMOS process, and the die photo is shown in Fig. 5.4.

5.1 Measurements

A motion resilience experiment is performed where the heartbeat of a healthy individual is monitored with the prototype chip at different moving conditions during

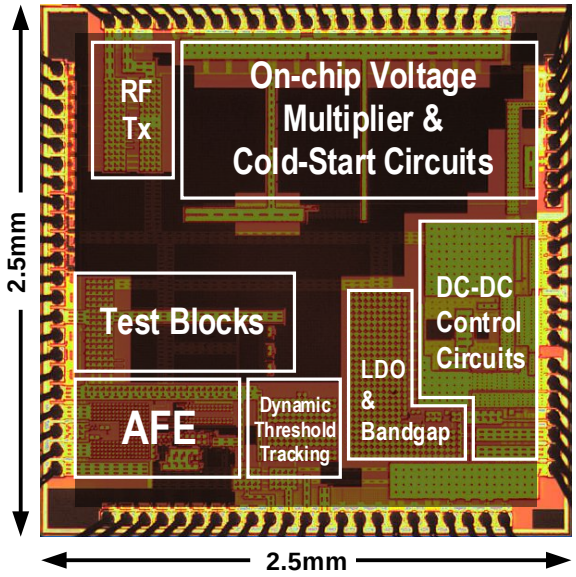

Figure 5.4: Die micrograph of sensor SoC in 180 nm CMOS.

day and night. The result is shown in Fig. 5.5. The proposed threshold voltage generation scheme adapts quite well to the motion of the subject and achieves a high accuracy of 99% in detecting heartbeats across different kinds of motions. As shown, a simple fixed threshold based ECG comparison can detect heartbeats satisfactorily at steady seating condition, but deteriorates drastically with fast motion of the body.

The system starts with a TEG voltage of 60 mV, which requires a temperature difference of 1.4 °C between skin and environment. Following cold-start, the power converter boosts the TEG voltage to a 1.5 V DV_{DD} within 100 ms. The ripple-less supply, AV_{DD}, at the output of the LDO ramps up slowly to 1.2 V as shown in Fig. 5.6. It ensures settling of initial $VREFL$ and $VREFH$, generated with DV_{DD} powered leakage-based voltage references well before the AFE starts operation and initializes the PWLLs. With the incidence of ECG pulses, $VREF$s on both sides start self-

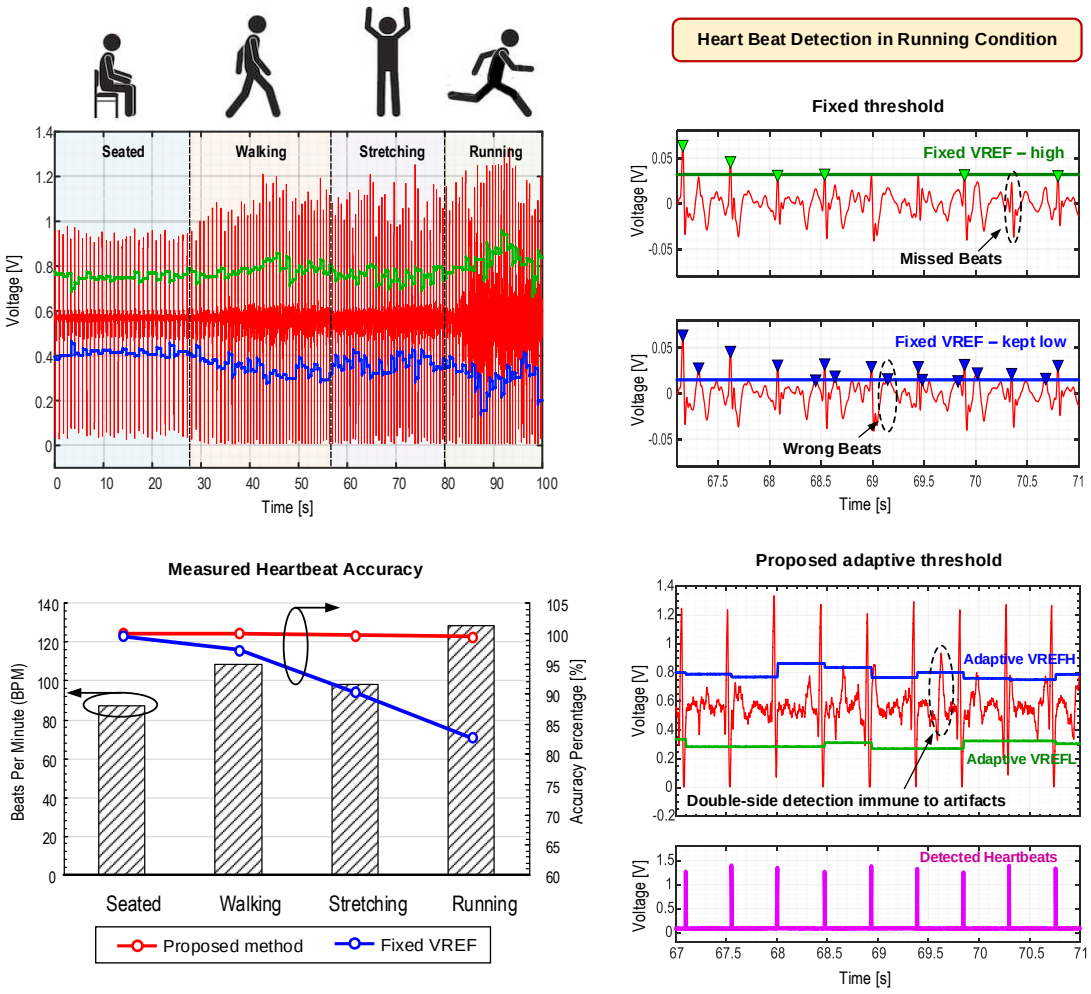

Figure 5.5: Measured heartbeat detection accuracy using the proposed adaptive feature extraction scheme, and comparison with a fixed-threshold approach.

training and adapt to the motion of the subject. Consumption of the harvested power by individual blocks in Fig. 5.6 depicts that the LO is the most power consuming block of the system due to the continuous $fCV_{DD}{}^2$ power consumption. Maximum power point at input and efficient operation of DC-DC converter ensures operation of

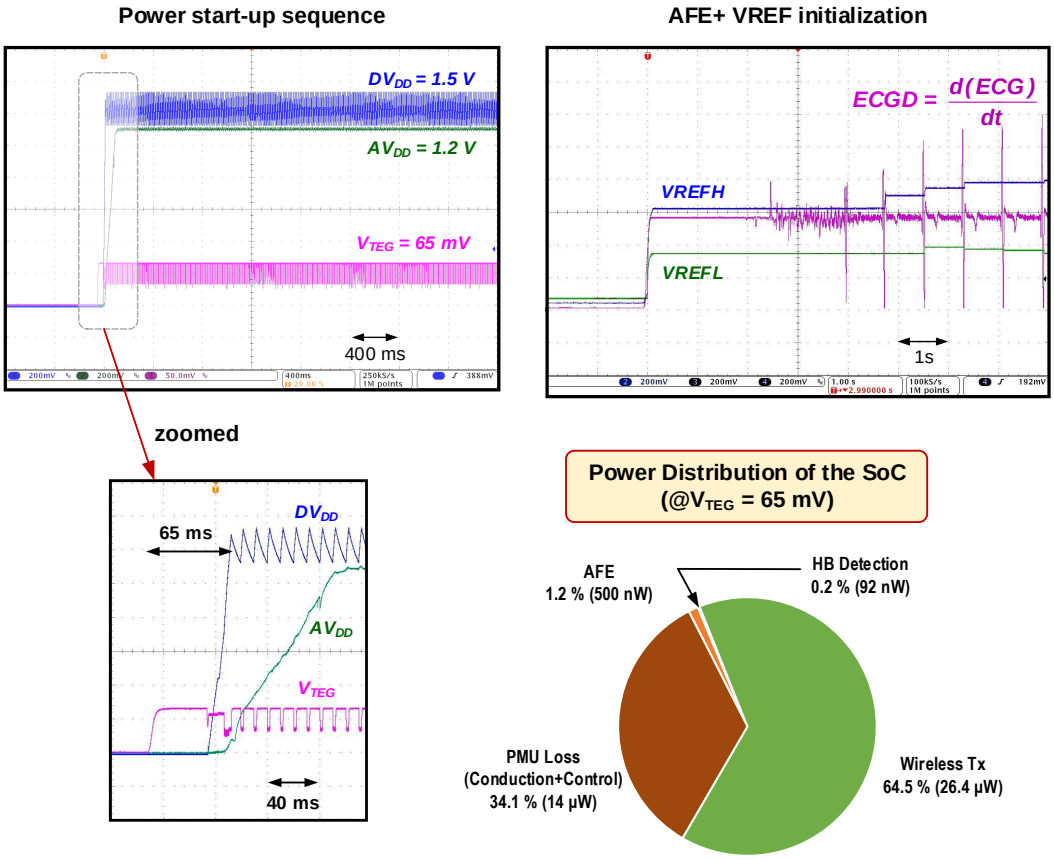

Figure 5.6: Measured transient plots showing start-up transient of the PMU initialization of the AFE and VREFs; measured harvested power distribution for different sub-blocks at TEG input voltage of 65 mV.

the whole system at an input voltage as low as 20 mV with an input power of 20 µW from the TEG. A comparison of the performance of the ECG signal processing circuit is shown in Table 5.1, and measurement setup with a subject is shown in Fig. 5.7. The proposed self-sustaining system reports the first demonstrated autonomous wearable for point-of-care diagnostic solely sustaining on human body heat.

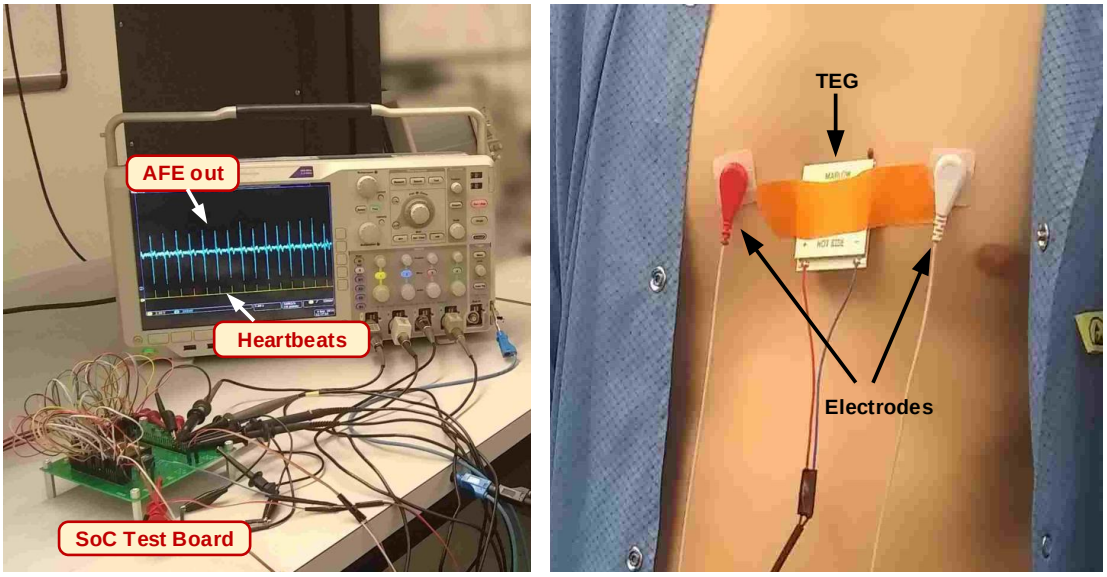

Figure 5.7: Measurement set-up for the autonomous batteryless heartbeat detection SoC.

5.2 Chapter summary

A battery-less and motion resilient heartbeat monitoring system is presented that provides 99% accurate heartbeat detection from two-electrode ECG. The SoC is powered by harvesting thermal energy from human body heat using centimeter-scale TEGs. The power management unit comprises an autonomous DC-DC converter, designed with a single inductor and can self-start with the body heat itself with a ΔT of only 1.4 °C between skin and environment. The small form-factor of the system makes it suitable to wear on body without adding discomfort during the normal activities of daily life. The self-sustaining heartbeat monitor operates with a minimum power of 20 µW from the TEG and represents the first demonstrated heartbeat detection system powered entirely and continuously by human body heat.

Table 5.1: Performance comparison with state-of-the-art

Parameters	TBioCAS'14 [61]	JSSC'15 [62]	ISSCC'15 [63]	JSSC'10 [64]	**This work**
Process	0.18 µm	0.18 µm	0.18 µm	0.18 µm	**0.18 µm**
Target Signal	ECG	EMG	ExG	ECG	**ECG/Heartbeat**
Total Input Power	680 nA	24 µW	2.27 µW	12 µW	**4 µW**
End-to-end PMU efficiency	-	64 %	74.9 %	54.9 %	**80 %**
Input Boost Voltage	-	0.8 V	10 mV	-	**9 mV**
Start-up Voltage	-	-	-	-	**60 mV**
Start-up Time	-	-	-	-	**100 ms**
Power Source	Benchtop	RF	TEG/Solar	RF	**TEG/Body Heat**
Integrated Feature Extraction	Yes (w/ external DSP)	-	No	No	**Yes**
Supply Voltage	1.3 V - 1.8 V	1 V - 1.8 V	1.4 V	1.8 V	**1.2 V (Analog); 1.5 V (Digital)**
Data Transmission	Wireless	Wireline	Wireless	Wireless	**Wireless**

(1) Estimated from transient plots, (2) Converter efficiency only.

Chapter 6: Conclusion

Energy harvesting has opened up myriads of possibilities for electronic applications where stable electrical power is unavailable. While in some applications it has the potentiality to power the whole system, in others it can complement the battery power and reduce the form-factor of the system, adding comfort and human safety. With increasing numbers of sensor nodes and wearables, battery operated devices are surely going to run out of fuel because of their larger form factor.

Humans, being homeothermic, maintain a stable body temperature irrespective of the surrounding and that makes thermoelectric energy harvesting utilizing body heat an attractive alternative for powering micro-power wearables. This thesis is motivated on utilzing body heat to make self-sustaining bio-systems that can be leveraged for preventive healthcare and point-of-care diagnostics. It addresses the primary challenges related to thermoelectric energy harvesting from small temperature difference between human skin and environment. A low voltage integrated cold-start mechanism is presented first which achieves the lowest reported cold-start voltage of 50 mV with completely integrated circuits. Low voltage cold-start with small form-factor of the micro-power management unit makes the architecture suitable for powering wearable sensors and electronics. The proposed one-shot start-up mechanism also achieves a fast startup of the boost converter and results in less waste of energy just for startup.

A single inductor high-efficiency boost converter architecture is presented next that operates efficiently at very low input voltage (10s of millivolts) while ensuring matching of the input impedance with that of thermoelectric generator to enable maximum power transfer. The technique assists the harvester to achieve high end-to-end efficiency even at low input voltage and the harvester survives even with a small TEG voltage of 7 mV, making the topology the lowest input voltage boost converter reported so far.

Finally, the self-starting autonomous boost converter architecture is embedded in a system-on-chip (SoC) with additional fine grain power management blocks like LDO to demonstrate the potentiality of harvested power from body heat. The extracted power is utilized to detect human heartbeat by acquiring ECG signal from human body. The implementation of the SoC also demonstrates the mutiple design constraints that need to be co-optimized to achieve a fully self-sustaining system. An energy efficient way of detecting accurate heartbeats even in presence of motion artifacts is presented. The significant power consumption on the wireless transmission part shows that limitation on the transmission part is more severe than the signal processing part and is a potential area of improvement. The simple motion-resilient architecture presented consumes less than microwatts of power while achieving 99% accurate heartbeat detection irrespective of the moving condition of the body.

6.1 Future directions

Thermoelectric energy harvesting from body heat can generate higher power density in indoor conditions compared to other ambient sources. Hence, the energy can be used for multiple low-power applications. Monitoring other vital signs like respiration rate and blood pressure can be easily added to make sustainable body-area healthcare networks. However, the biggest challenge is the transmission of the sensing data to the base station for further processing. Continous data transmission is power consuming and difficult to sustain; duty-cycled transmission can survive under such low power conditions. The future direction of this work will be to extend the functionalities of the SoC and powering them with body heat or even with other ambient energies in a multiplexed way to realize self-sustaining wearable healthcare.

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