Microwave Front-End Component Codesign:

Filter-Amplifiers, Integrated Passives and Rectifying-Radiators

by

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Thesis directed by Professor Zoya Popović

The ever-growing need for improved wireless communications motivates innovation in miniaturization and integration of microwave front-end components. This thesis addresses miniaturization by co-design methods that enable simultaneous size reduction, improved efficiency, diverse technology integration, and enhanced safety. First, a new theoretical treatment for simple design of narrowband filters with arbitrary complex impedance ports is introduced and validated through 2.4 GHz designs with 2^{nd}-order all-pole and 4^{th}-order elliptical response. The theory is then extended to filters with port impedance tuning capabilities and validated with a 2^{nd}-order Chebyshev filter with varactor-tunable input impedance over a pre-defined impedance range with maintained filter response. The theory is also applied to impedance-matching filters for power amplifiers (PAs) with the goal of improving efficiency and reducing footprint. A high-efficiency 4.7 GHz single-stage 4-W hybrid GaN filter-PA (FPA) shows a measured gain of 15 dB and PAE=55 % with a pre-specified 9 % fractional bandwidth. The approach is further validated on a GaAs MMIC FPA at 28 GHz with a measured saturated gain of 8 dB, 200 mW of output power and PAE=30 %.

For further integration of components with miniaturized footprint, a heterogeneous integration process called metal-embedded chip assembly (MECA), developed by HRL, is exploited to combine ceramic passive circuits, surface-mount capacitors and GaN MMICs with a unique interconnect network. The interconnects outperform standard wirebonds and are also used to implement transmission lines, referred to as bridge-lines, with reduced loss and higher possible characteristic impedances compared to microstrip. Various couplers in the 8-10 GHz range are designed and characterized to demonstrate the additional design capabilities provided by the MECA process. Thermal performance improvement of PAs is shown, and increased gain and efficiency for an X-band GaN MMIC is reported. Finally, the FPA design approach from the first part of the thesis is used to design a quasi-MMIC FPA with a predicted gain of 7.4 dB, peak PAE of 23% and output power above 30 dBm from 23.65 to 24.4 GHz. Additionally, a 20-GHz dual-mode rectangular cavity

resonator filter with insertion loss under 0.25 dB is designed in the MECA process, and is in fabrication at the time of writing of this thesis.

Wireless systems rely on batteries or wired charging, which limits the operational time. In the second part of the thesis, co-design and integration of wireless charging and harvesting is researched. Another application of wireless charging is for electric vehicles, where methods analogous to microwave antenna arrays, amplifiers and rectifiers can be used to provide a means for charging batteries of stationary or moving vehicles at lower frequencies and high power levels. A new method for reducing fringing fields in a capacitive wireless power transfer (CWPT) system using a near-field phased array is demonstrated using a multi-module approach on a 1.1 kW system at 13.67 MHz at a 25-cm energy-transfer distance with over 80% efficiency. To meet safety standards, a fringing field reduction of 24% with a two-module system and 43% with a four-module system, is demonstrated at 7, 14 and 29 MHz. This system applied co-design of capacitor arrays with matching networks for the high-power inverters and rectifiers on the circuit side, and energy-transfer and fringing fields on the free-space side.

In the low-power regime, co-design of both narrowband and broadband rectifiers and antennas for harvesting ambient power for wireless devices is demonstrated. Harvesting power from airplane altimeter radar antenna sidebands with a rectifier-antenna (rectenna) for aircraft health monitoring sensors demonstrates the possibility of charging a storage device at incident power levels below $2\,\mu$W/cm^2 at 4.3 GHz. The narrowband harvesting device applies co-design to the antenna, rectifier and maximum power point tracking power-management circuit to provide a usable voltage level. For wideband energy harvesting from unknown and variable sources, wearable rectenna arrays screen-printed on clothing are demonstrated for harvesting 4-130 μW/cm^2 power densities over more than an octave bandwidth in the sub-6GHz frequency range. Measurements on 36 and 64-element arrays show up to $P_{DC} = 32\,\mu$W for incident power densities of $4\,\mu$W/cm^2. For low incident power densities, the efficiency is in the 5-10% range, and reaches 32% for $100\,\mu$W/cm^2. In these arrays, the rectifiers and tightly-coupled antennas are co-designed for broadband performance.

Dedication

A mi madre Silvia y mi abuela Elba.

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Part I

Integration in RF Front Ends

Chapter 1

Introduction

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1.1 RF Front Ends

Analog RF front ends are present in all wireless communications devices such as cellphones, radios and television, as well as in RF identifications (RFID) [1] and radar systems [2]. The Internet of Things (IoT) expands the use of RF front ends to industrial, medical, transportation, agriculture, infrastructure, energy, telemetry, environmental and military applications among others. Projections point towards 38.6 billion connected IoT devices by the year 2025 and 50 billion by 2030 [3]. The coming years will also see the rise of 5G communications which will lead to increased bandwidth and latency for mobile communications. This presents a series of challenges that require addressing previously ignored problems, as well as increased innovation in the way that the RF front end hardware is designed and fabricated. For instance, 4G bandwidths

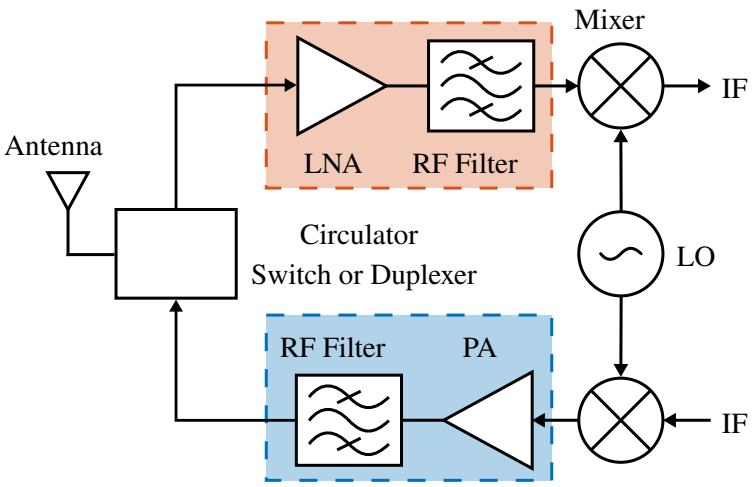


Figure 1.1: General front end transceiver block diagram. This thesis focuses on the integration of the shaded filter-amplifier blocks.

are 5-20 MHz and can go up to 100 MHz with carrier aggregation. 5G increases the signal bandwidth to 100 MHz on FR1 (frequency range 1, also referred to as sub-6 GHz range), 400 MHz on FR2 (frequency range 2, also referred to as millimeter wave range), and bandwidths as large as 800 MHz can be obtained with carrier aggregation as specified by the standards [4]. Latency will go from 50 ms to as low as 1 ms in the transition from 4G to 5G systems. Technologies such as MIMO (Multiple-Input and Multiple-Output) and NOMA (Non-Orthogonal Multiple Access) [5], among others, add to the challenges of RF front end design in 5G systems. Additionally, the energy used by wireless networks has become an important amount of the total energy used in the world [6, 7] and that share will continue to increase as the communications sector keeps growing. For this reason highly efficient RF systems are necessary for efficient use of energy resources. Radar applications both in military and commercial industries are also growing and have increasingly demanding specifications. Automotive radar [8] has seen a particularly accelerated rise and will be key in the deployment of self-driving vehicles. These ubiquitous front ends in various types of systems, and their associated challenges, require continuous improvement of the existing technology and design techniques.

A typical RF front end, as the one shown in Fig. 1.1, consists of a combination of passive and active components, including antennas, bandpass filters, amplifiers (low noise for receivers and high power for transmitters), oscillators and mixers. One of the challenges of RF design for front-end components is energy efficiency. For example, in a satellite 40 % of the total power is used by the communications transmitter.

Higher efficiencies also lead to reduced heat dissipation, making thermal management simpler and further reducing size. Additionally, low loss, high frequency interconnects are necessary, mechanical stability and compatibility between the various components is essential, and all these must be addressed in a unified way. Increased efficiency also leads to smaller, or even nonexistent (as is the case in wirelessly powered systems), batteries. These reduced battery requirements translate to reduced size and weight of the system.

Many wireless systems are portable and need to have a small form factor. Size reduction can be accomplished in many ways: improving the materials used allowing smaller designs (for instance with higher permittivity substrates), improving fabrication techniques to fit more components in smaller volumes (making lumped designs instead of distributed, for example), and integrating the various components in the front end for size reduction of the full system. Typically all microwave components that form part of a front end are designed with 50 Ω input/output port impedances for practical reasons. However, if this requirement can be eliminated, lower loss (improved energy efficiency), and size reduction can be obtained without using a standard interconnecting impedance and therefore reducing the overall size of the matching networks.

This thesis addresses the challenges of size reduction and energy efficiency enhancement in RF front end design with two approaches: (1) using a new heterogeneous integration fabrication process developed by our industrial collaborator HRL; and (2) integrating portions of the front end using co-design of filters and amplifiers, as well as antennas and rectifiers.

1.2 RF Filters

RF filters are frequency selective 2-port networks designed to reject unwanted portions of the spectrum while passing the desired bands. Fig.1.2 shows an illustration of how the filtering process modifies signals. Filter design can be done using various techniques but in this work the focus is on the most used and widespread one, the coupling matrix method. References for coupling matrix methods that explain the whole process from the synthesis of the coupling matrix to the implementation of the coupled resonators filters in various technologies are numerous and well established. Among them [9, 10] are notable ones. In this thesis, the method is extended to enable direct co-design and integration with amplifiers. Here fundamental concepts

and definitions for filter design using coupling matrices are reviewed for completeness.

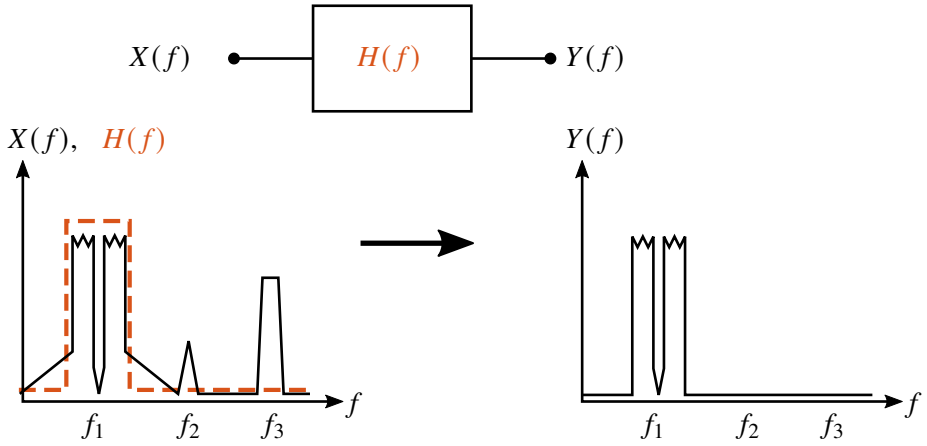


Figure 1.2: Filter operating principle. A signal $X(f)$, with some desired and undesired spectral regions, is the input to a filter with frequency response $H(f)$ (dashed red line), and the output signal $Y(f)$ only contains the desired part of the spectrum while rejecting the rest.

The coupling matrix is an immittance (normalized impedance or admittance) matrix that provides the information necessary to connect (couple) resonators in a specific configuration that provides a defined frequency response of filters composed of coupled resonators [10]. Fig. 1.3 shows diagram of a general filter of the type addressed in this thesis. The parallel and series implementations correspond to the coupling matrix representing an admittance or impedance matrix, respectively.

The basic components of the filter are resonators and immittance inverters (which provide the couplings between the resonators). The geometry and technology used to build the resonator dictate its behavior. A resonator can be characterized in terms of its resonant frequency and loss, described as a quality factor Q given by

$$Q = 2\pi f_0 \frac{W_{stored}}{P_{loss}} \tag{1.1}$$

where f_0 is the resonant frequency, W_{stored} is the maximal energy stored, and P_{loss} is the average power dissipated in the resonator. The quality factor is also inversely related to the bandwidth of the resonance

$$Q = \frac{f_0}{\Delta f} = \frac{1}{BW} \tag{1.2}$$

where Δf and BW are the absolute and fractional bandwidths of the resonator at f_0. Resonators can be implemented in a variety of ways, some of which are shown in Fig. 1.4. The resonators are shown in Fig.

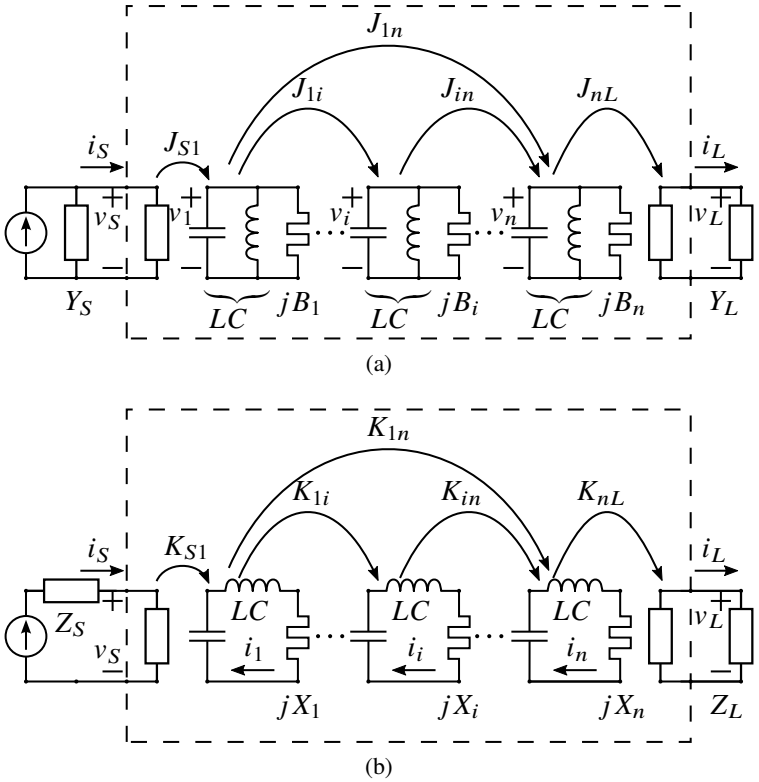


Figure 1.3: General coupled resonators filter circuit showing the resonators and couplings between them. (a) parallel and (b) series resonators implementation.

1.3 as ideal LC circuits, all with identical inductances and capacitances that resonate at the center frequency of the filter. The resonators are detuned by the use frequency invariant reactances (FIR), which as the name indicates are purely imaginary reactances that do not vary over frequency.

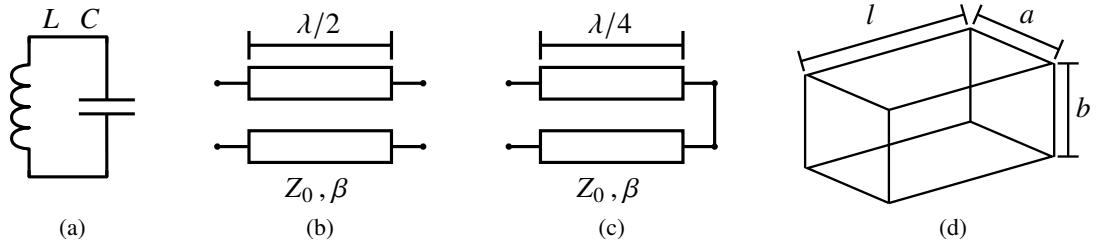


Figure 1.4: Various resonators used in filter design: (a) lumped LC resonator, (b) half wavelength transmission line resonator, (c) quarter wavelength transmission line resonator and (d) rectangular waveguide cavity.

An immittance inverter is a network that performs an inversion of the load [11], that is

$$\begin{aligned} Z_1 &= \frac{K^2}{Z_2} \\ Y_1 &= \frac{J^2}{Y_2} \end{aligned} \tag{1.3}$$

where K and J are the characteristic impedance and admittance of the inverter, respectively, and Z_i and Y_i (i=1,2) are the impedances and admittances at the ports of the inverter. Immittance inverter circuits are usually characterized by their ABCD matrices

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 0 & \mp jK \\ \pm\frac{1}{jK} & 0 \end{bmatrix} \\ \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 0 & \mp\frac{1}{jJ} \\ \pm jJ & 0 \end{bmatrix}. \end{aligned} \tag{1.4}$$

Inverters used to couple the resonators can be implemented in numerous ways. Several examples are shown in Fig. 1.5, like a quarter wave inverter (a quarter wavelength long transmission line), a π-network with inductors and capacitors, a hole between two cavities, a proximity gap between planar resonators and even a screw coupling various resonating modes in a resonating cavity, among others.

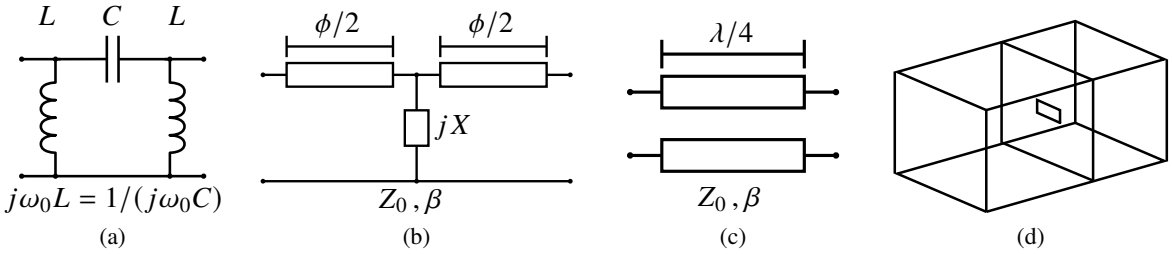


Figure 1.5: Various inverters used in filter design: (a) lumped π inverter, (b) distributed transmission line inverter with center reactance, (c) quarter wavelength transmission line inverter and (d) iris coupling two cavities.

The coupling matrix, synthesized for a specific frequency response, provides the information necessary to design the resonators and how to couple them between each other and to the input and outputs. The

general $N+2$ coupling matrix is

$$[m_0] = \begin{bmatrix} m_{SS} & m_{S1} & m_{S2} & \cdots & \cdots & m_{Sn} & m_{SL} \\ m_{S1} & m_{11} & m_{12} & \cdots & \cdots & m_{1n} & m_{1L} \\ m_{S2} & m_{12} & m_{22} & \cdots & \cdots & m_{2n} & m_{2L} \\ \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & \vdots & \vdots & & \ddots & m_{(n-1)n} & m_{(n-1)L} \\ m_{Sn} & m_{1n} & m_{2n} & \cdots & m_{(n-1)n} & m_{nn} & m_{nL} \\ m_{SL} & m_{1L} & m_{2L} & \cdots & m_{(n-1)L} & m_{nL} & m_{LL} \end{bmatrix} \tag{1.5}$$

where the m_{ij} are the couplings between the resonators, the source and the load. In this case there are a total of n resonators, and the source and load are denoted as S and L. A null coupling (m_{ij}) means no coupling between those resonators. The m_{ii} elements indicate the deviation of the resonator i from the center frequency of the filter. When $m_{ii} = 0$ the resonant frequency of resonator i is the center frequency of the filter. Note that the coupling matrix in (1.5) is symmetric; this is to be expected as the immittance matrix of a reciprocal circuit like a filter is going to be symmetrical. Nonetheless, sometimes this is not the case, for instance the non-reciprocal bandpass filter presented in [12].

The elements of the coupling matrix are used to find the elements shown in Fig. 1.3. The LCs are selected to resonate at the center frequency of the filter ($\omega_0 = 2\pi f_0$) and are not uniquely defined. The FIRs are found as

$$B_i = m_{ii} C \omega_0 \Delta \tag{1.6}$$

$$X_i = m_{ii} L \omega_0 \Delta \tag{1.7}$$

where Δ is the fractional bandwidth of the filter. The inverters are calculated as

$$J_{ij} = m_{ij} C \omega_0 \Delta \tag{1.8}$$

$$K_{ij} = m_{ij} L \omega_0 \Delta \tag{1.9}$$

and the couplings to source and load are found as

$$J_{S1} = m_{S1} \sqrt{\frac{C \omega_0 \Delta}{R_S}} \tag{1.10}$$

$$J_{nL} = m_{nL}\sqrt{\frac{C\omega_0\Delta}{R_L}} \tag{1.11}$$

$$K_{S1} = m_{S1}\sqrt{\frac{L\omega_0\Delta}{G_S}} \tag{1.12}$$

$$K_{nL} = m_{nL}\sqrt{\frac{L\omega_0\Delta}{G_L}} \tag{1.13}$$

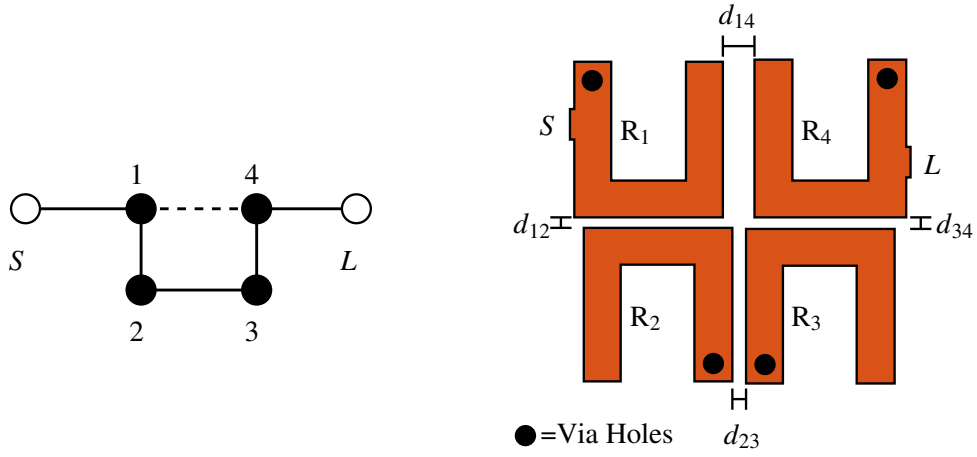
where R_S, R_L, G_S and G_L are the real parts of the source and load impedances and admittances, respectively.

A common representation used for illustrating coupled resonator circuits is the node diagram, where each node is a resonator, the source, or load of the filter. Fig. 1.6a shows a specific example of a node diagram. The coupling matrix for that diagram is

$$[m_0] = \begin{bmatrix} 0 & m_{S1} & 0 & 0 & 0 & 0 \\ m_{S1} & m_{11} & m_{12} & 0 & m_{14} & 0 \\ 0 & m_{12} & m_{22} & m_{23} & 0 & 0 \\ 0 & 0 & m_{23} & m_{33} & m_{34} & 0 \\ 0 & m_{14} & 0 & m_{34} & m_{44} & m_{4L} \\ 0 & 0 & 0 & 0 & m_{4L} & 0 \end{bmatrix}. \tag{1.14}$$

The black nodes in Fig. 1.6a represent the resonators while the white nodes are the input and output ports (source and load). The lines connecting the nodes stand for the inverters, a line between resonator i and resonator j is a coupling between them. In the example implementation shown in Fig. 1.6b the couplings are done by proximity (coupled line sections) where the coupling is controlled by adjusting the distance between the resonators (d_{ij}). The dashed line indicates a different nature of the coupling, this means that if the solid couplings are, say, electrically dominant couplings then the dashed one will need to be magnetically dominant and vice versa. In the matrix this difference is manifested as different signs of the m_{ij} elements. The example implementation in Fig. 1.6b has a coupling between resonators "1" and "4" where the electric field is dominant, while the magnetic field is small. This is due to being near the open side of the resonator where the current is small and the voltage is large. The other coupling sections exist in mixed field regions where the result ends up being magnetically dominant, closer to the shorted end of the resonator where the current is larger and therefore the magnetic field is larger too. The couplings to the outside world are done by

taping the input ("1") and output ("4") resonators at a specific point. Sliding the tapping spot up and down leads to larger or smaller coupling.



(a) (b)

Figure 1.6: Filter example showing (a) node diagram, (b) microstrip implementation with folded quarter wavelength resonators in close proximity. The R_i are the resonators and the couplings are controlled by adjusting the distances d_{ij}. The source and load ports are indicated as S and L, respectively. These input and output couplings to these are realized by tapping the resonator at a specific point (closer to the shorted end for lower impedances). This design is explained in more detail in Chapter 2.

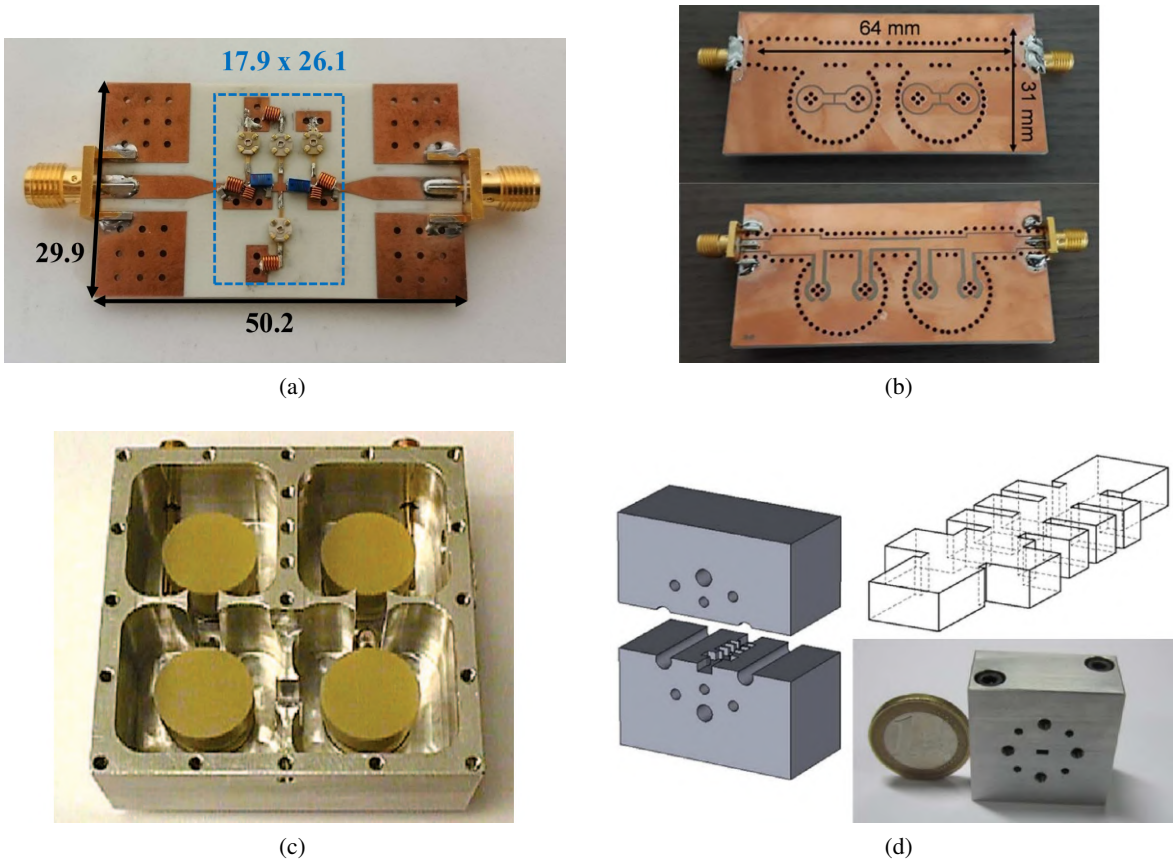
Some of the filters discussed in this thesis are mainline coupled filters, also known as all-pole filters, which only have couplings between adjacent resonators. The coupling matrix for such a filter is

$$[m_0] = \begin{bmatrix} 0 & m_{S1} & 0 & \cdots & \cdots & 0 & 0 \\ m_{S1} & m_{11} & m_{12} & \cdots & \cdots & 0 & 0 \\ 0 & m_{12} & m_{22} & \cdots & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & \vdots & \vdots & & \ddots & m_{(n-1)n} & 0 \\ 0 & 0 & 0 & \cdots & m_{(n-1)n} & m_{nn} & m_{nL} \\ 0 & 0 & 0 & \cdots & 0 & m_{nL} & 0 \end{bmatrix} \tag{1.15}$$

where all the couplings that are zero in this matrix are referred to as cross couplings, since they connect non-adjacent resonators. In this thesis all the cross couplings that are not part of the outer elements, that is all the m_{Sj} and m_{iL} excepting m_{S1} and m_{nL}, will be referred to as "internal" cross couplings.

A wide variety of filters can be designed using the coupling matrix method, and Fig. 1.7 shows some

examples of coupled resonators filters. Fig. 1.7a shows a lumped-element bandpass filter (BPF) with multiple levels of transfer-function tunability including bandwidth (BW), center frequency, and intrinsic RF switching [13]. Fig. 1.7b shows a compact substrate integrated waveguide (SIW) bandstop filter that uses substrate-integrated-(SI)-coaxial resonators [14]. The filter in Fig. 1.7c is a four-pole dielectric resonator filter designed for wireless base station applications [15], since dielectric resonators can be small and have large quality factors (low loss). Finally, Fig. 1.7d displays a 100 GHz waveguide pseudo-elliptical four-poles asymmetric response filter with 10 % of fractional bandwidth [16].



(a) (b)

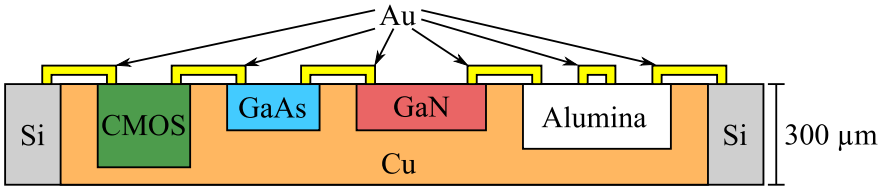
(c) (d)

Figure 1.7: Various RF filters. (a) Lumped elements UHF-Band (800 MHz) bandpass filter [13], (b) SIW dual-resonant SI-coaxial resonator-based bandstop filter centered at 3.75 GHz [14], (c) four-pole dielectric resonator filter [15] and (d) 100 GHz four-poles asymmetric response filter [16].

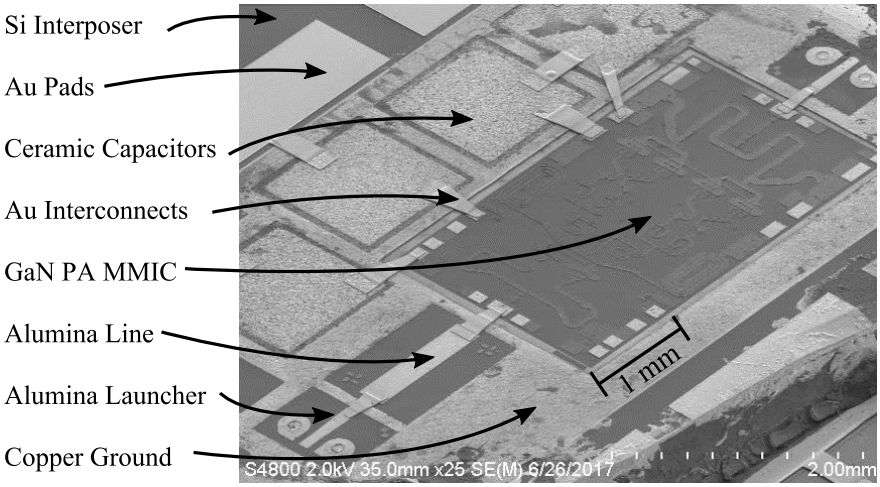
1.3 Heterogeneous Integration

As mentioned in the opening of this Chapter, RF front end size reduction is one of the main challenges that are addressed in this work. Heterogeneous integration is gaining increased interest for miniaturized radio frequency (RF) front-ends [17, 18]. The goal is to enable integration of RF compound semiconductor (GaAs, GaN and InP) monolithic microwave integrated circuits (MMIC), with digital and analog CMOS circuits and low-cost high-performance passives implemented in alumina, aluminum nitride, silicon or glass, with good thermal performance. An approach developed by HRL Laboratories (formerly Hughes Research Laboratories) is discussed in this thesis, Fig. 1.8 which shows a variety of chips embedded in a common thick copper ground. The heterogeneous integration process is referred to as Metal Embedded Chip Assembly (MECA). Previous demonstrations of heterogeneous integration include a double heterojunction bipolar transistor (DHBT) InP 300-GHz amplifier that is heterogeneously integrated with a 130-nm RF CMOS chip without performance degradation by HRL [19]. In another integration process, InP heterojunction bipolar transistor (HBT) chiplets were interconnected to Si CMOS chips in [20] in a differential amplifier with a slew rate of 2.56×10^4 V/μs and an output swing of 3.42 V. Integration of InP HBTs grown next to Si CMOS transistors on a Si substrate is demonstrated in [21]. The integration allows tight device placement with a separation between the HBTs and CMOS transistors as small as 2.5 μm. Another example of InP integration with GaN and CMOS is shown in [22], with a Q-band InP HBT voltage-controlled oscillator (VCO) and a GaN high electron mobility transistor (HEMT) amplifier on a common 65 nm CMOS substrate.

Several "quasi-MMIC" circuits have been demonstrated, where GaN PAs are integrated with partial matching networks implemented in a different material. For example, [23] demonstrates a 0.25-μm GaN MMIC with pre-matching performed on chip and wirebonded to a partial matching circuit on a Rogers 4350B substrate. The results using limited GaN-on-SiC area show a power-added efficiency (PAE) of 71% with a saturated gain of 12 dB and output power of 3 W (power density of 4.5 W/mm) at 9.8 GHz in continuous wave (CW) operation. GaN HEMTs wirebonded to GaAs passive matching circuits and mounted on a common carrier metal plate form a quasi-MMIC Doherty PA operating from 1.7-2.7 GHz with a 37% back-off efficiency [24]. A similar Doherty quasi-MMIC at 5.5-6.5 GHz is demonstrated in [25]. In [26], GaN



(a)



(b)

Figure 1.8: (a) Metal Embedded Chip Assembly (MECA) process cross-section example showing different technologies integrated into a single thermal and RF ground within a Si interposer wafer (not to scale). (b) Photo of GaN MMIC power amplifier integrated with alumina launchers, an alumina transmission line and ceramic off-chip capacitors.

HEMTs are interconnected heterogeneously with Si matching networks, resulting in a 170 W output power and PAE > 40% using a copper interconnect structure. A single stage copper embedded X-band PA quasi-MMIC with improved efficiency is also demonstrated in [27] using a GaN transistor, Si matching networks and an interconnect layer. In this thesis, several passive and active circuits in the MECA process are designed and validated. Various X-band couplers are designed and characterized, MECA interconnects are compared to wirebonds and used in multiple ways, ceramic capacitors are integrated, and X-band GaN MMICs are integrated in the process and performance improvement related to the enhanced thermal environment is reported.

1.4 Thesis Organization

The contents of this thesis focus on finding creative ways of integrating components of an RF front end as well as wireless power delivery to these systems. The thesis is organized in two parts where the first one deals with integration of components in RF front ends and the second part describes the work related to wireless powering of electric, electronic and microwave systems.

Part I

Chapter 2 presents a method for the design of filters with complex port impedances. The method uses standard coupling matrix design techniques with a simple modification of the denormalization process to incorporate the imaginary parts of the port impedances while maintaining the frequency response and enforcing simultaneous conjugate matching on both ports. Two microstrip filters are designed, fabricated and measured to validate the technique developed in this Chapter.

Chapter 3 shows a general design method for tunable matching networks that have a prescribed filter characteristic over a range of complex port impedances. The approach enables prediction of the achievable tunable impedance range, given a filter topology and tuning element values. As experimental validation, a varactor based filter demonstrator is designed, fabricated and measured.

Chapter 4 applies the technique from Chapter 2 to introduce a method for co-design of filtering matching networks for PAs with a desired frequency response, improved efficiency and reduced footprint. The microwave transistor operates with high efficiency when a specific complex impedance load is presented. This requires the use of the filter matching network design technique, with arbitrary complex impedance ports developed in Chapter 2. A single-stage 4.7 GHz high-efficiency hybrid GaN filter-PA (FPA) is designed using high-Q ceramic resonators. The port impedances are determined by load- and source-pull for an efficiency-power tradeoff. The filter is built and characterized, and the measured results are shown in the Chapter.

Chapter 5 uses the method from Chapter 4 to design a 28 GHz GaAs MMIC FPA with a microstrip filter.

The design is explained in detail showing the filter, amplifier and co-design aspects. Measured results are shown for the MMIC FPA which, to the best of the author's knowledge, is the first implementation of a MMIC FPA.

Chapter 6 presents the RF performance benefits of a heterogeneous integration technique for multi-chip modules. Passive components are integrated in a MECA process together with GaN MMICs in a way that provides a common RF and thermal ground. Simulations show that photolithographically defined interconnects can out-perform wirebonds from 10 to 100 GHz. The interconnect layer of the MECA process forms bridge transmission lines with lower loss, higher characteristic impedances and comparable dispersion to microstrip lines. Microstrip couplers are designed partially on alumina, and completed with MECA interconnects during the integration process, resulting in good performance in agreement with simulations. Finally, measurements of a GaN PA MMIC integrated in the MECA process show gain and PAE improvements of up to 3 dB and 3.2 percentage points, respectively.

Part II

Chapter 7 describes a method for reducing fringing electric fields in a capacitive WPT system using a near-field phased array consisting of multiple CWPT modules. Field reduction of up to 43 % is demonstrated at distances closer than 25 cm and for frequencies of 7, 14 and 29 MHz.

Chapter 8 demonstrates energy harvesting from very low incident power levels at 4.3 GHz ($< 2\,\mu\mathrm{W/cm^2}$). The harvested power is sufficient to power unattended sensors on an aircraft. These results validate the co-design methodology for the rectenna, which combines full-wave EM modeling and nonlinear circuit simulations.

Chapter 9 presents 16- and 81-element broadband bow-tie rectenna arrays screen printed on a cotton tee-shirt for harvesting 4-130 $\mu\mathrm{W/cm^2}$ power densities between 2 and 5 GHz. It is found that screen printing on fabric with conductive ink can be used for functional rectenna array harvesters and the shirt is shown to withstand hand-washing. The effect of varying air gaps between the fabric and skin and body curvature are studied and taken into account, showing small changes in performance. Full-wave

antenna simulations are performed with specific tissue electrical parameters for the torso, as well as for a body phantom. Measurements using a saline-filled phantom show up to $P_{DC} = 32\,\mu$W for incident power densities of $4\,\mu\text{W/cm}^2$. The measurements on the phantom compare well with those obtained with the tee-shirt rectenna worn on an actual body.

Chapter 10 has a summary of the thesis and contributions as well as directions for future work. The work from Chapters 5 and 6 is combined in a proposed 24 GHz MECA quasi-MMIC FPA design with gain of 7.4 dB, peak PAE of 23 % and output power of over 30 dBm. A 20 GHz MECA integrated dual-mode rectangular cavity resonator filter with very low loss is also presented. This filter is proposed as the starting point for a high-efficiency MECA-FPA. A filter-LNA design is implemented in a MMIC and is currently under test with the goal of showing an extension to the theory presented in Chapter 4 to LNAs for enhanced performance. Other future work directions are suggested (e.g. harmonic terminations, broader bandwidth and extension to multiple ports). Finally the contributions of this work are summarized.

Chapter 2

Filters with Arbitrary Impedance Terminations

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2.2 Experimental Validation 25

2.3 Chapter Summary 30

In this chapter, the theory for filters with complex ports is detailed. This is followed by experimental validation on a couple of hybrid 2.4 GHz filter circuits. The theoretical approach follows the coupling matrix concept described in Section 1.2. The $N \times N$ coupling matrix concept was introduced by Atia and Williams in a series of papers [28, 29, 30, 31] and it is extended to a $N+2$ coupling matrix which includes the source and load couplings in [9]. The matrix synthesis process is also extended in [9] to the case of matrices designed to operate with complex terminations where very general examples of a fully canonical 4^{th} order asymmetric filter and a non-canonical fourth-degree asymmetric Chebyshev filter with two transmission zeros are given. In the first case, it is shown that all the coupler values for filters terminated in real-valued impedances are different than those of filters with complex terminations. For the latter, it is shown that only the first and

last resonators and the input and output couplings are affected by the change in terminating normalized impedances and the work in this Chapter explores this feature in detail. This generalized coupling matrix synthesis procedure can be applied in principle to any case, but does not give simple intuition or insight about the filter.

Further work has been done to incorporate complex impedances into coupling matrix filter design by modifying coupling matrices already designed to work with real-valued terminations. The research presented in [32] and [33], shows 2^{nd} and 3^{rd} order all-pole filter networks with one complex termination while leaving the other one unchanged (50 Ω). The work in [34] extends what was done in [32] by adding a source to load coupling, which allows a more extravagant frequency response with two symmetric transmission zeros to be added to the frequency response of the filter. An active $N+3$ coupling matrix is introduced in [35] consisting of a cascade of a filter, transistor and another filter. The transistor is modeled for small signal operation and that model is incorporated in the active coupling matrix. Both filters are designed in a similar way as done in [33] while also generalizing the theory to n-th order mainline filters.

In this Chapter the previous work is generalized for n-th order filters that include internal cross-couplings and both complex ports. It is proven that only the two elements next to the source and load need to be changed and closed-form formulas that give the exact modification necessary to match the filter to the complex impedances are provided. The coupling matrix formulation is extended and an intuitive circuit-level treatment for complex impedance ports is presented as well. A simple modification of the standard coupled-resonator filter design approach is presented which is valid for complex port impedances, synthesized with traditional techniques for real loads. The result is an extra step that can be taken in the denormalization process to incorporate the imaginary part of the port terminations. The theory is validated with proof-of-concept 2^{nd} and 4^{th} order filters.

2.1 Theoretical Treatment

An n-th order filter node diagram with no direct source-to-load coupling is displayed in Fig. 2.1a. The $N+2$ coupling matrix ($[m_0]$) for such a filter is given by equation (2.1). The frequency response of this filter is

designed in normalized space (1 Ω reference impedance and $\omega = 1$ normalized angular frequency), where it does not depend on the source and load terminations. The circuit elements in Fig. 2.1b can be obtained from the coupling matrix $[m_0]$ for a given center frequency, bandwidth and port resistances, following the procedure explained in Section 1.2 and detailed in [9, 10].

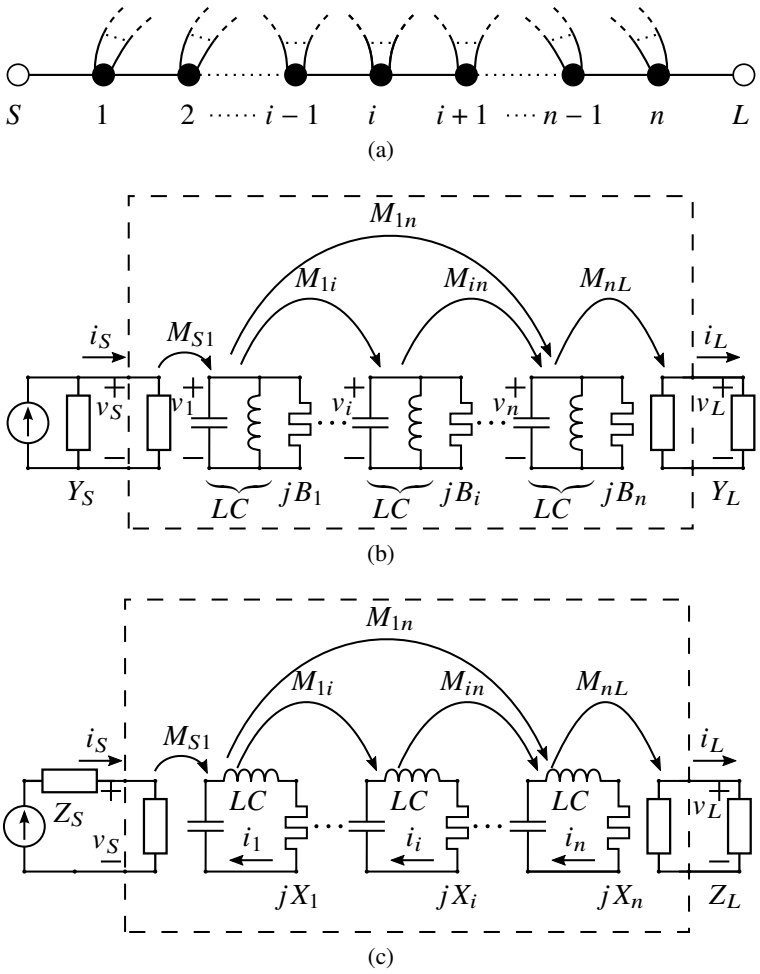


Figure 2.1: (a) General filter node diagram for an n-th order filter where nodes (resonators) i can connect to $n-1$ nodes, while nodes 1 and n can connect to n resonators. The exceptions are nodes S and L, which only connect to nodes 1 and n, respectively. Circuit representation with (b) parallel and (c) series resonators.

$$[m_0] = \begin{bmatrix} 0 & m_{S1} & 0 & \cdots & \cdots & 0 & 0 \\ m_{S1} & m_{11} & m_{12} & \cdots & \cdots & m_{1n} & 0 \\ 0 & m_{12} & m_{22} & \cdots & \cdots & m_{2n} & 0 \\ \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & \vdots & \vdots & & \ddots & m_{(n-1)n} & 0 \\ 0 & m_{1n} & m_{2n} & \cdots & m_{(n-1)n} & m_{nn} & m_{nL} \\ 0 & 0 & 0 & \cdots & 0 & m_{nL} & 0 \end{bmatrix} \tag{2.1}$$

The input and output port impedances in Fig. 2.1b are complex, and for filter-amplifier integration they correspond to the transistor impedances that maximize gain, efficiency, etc. For a power amplifier, for example, the input impedance of the filter matching network is found through load-pull and is a complex impedance that is typically a tradeoff between efficiency and power. The goal of the analysis shown below is to develop a method that allows standard filter design to be applied to ports with pre-determined complex impedances.

The filter described by $[m_0]$ will be referred to as the "original design", which can be obtained using any coupled-resonator synthesis technique [9, 10] and is traditionally designed for real-valued port impedances. A new coupling matrix, given by (2.2), is created by adding variations Δm_1 and Δm_n in the m_{11} and m_{nn} terms, respectively

$$[m] = [m_0] + [\Delta m] = \begin{bmatrix} 0 & m_{S1} & 0 & \cdots & \cdots & 0 & 0 \\ m_{S1} & m_{11} + \Delta m_1 & m_{12} & \cdots & \cdots & m_{1n} & 0 \\ 0 & m_{12} & m_{22} & \cdots & \cdots & m_{2n} & 0 \\ \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & \vdots & \vdots & & \ddots & m_{(n-1)n} & 0 \\ 0 & m_{1n} & m_{2n} & \cdots & m_{(n-1)n} & m_{nn} + \Delta m_n & m_{nL} \\ 0 & 0 & 0 & \cdots & 0 & m_{nL} & 0 \end{bmatrix} \tag{2.2}$$

The normalized input admittance of the filter is

$$y_{in} = \frac{m_{S1}^2}{s + j\left(m_{11} + \Delta m_1\right) + h_L\left(s, [m_0], \Delta m_n, z_L\right)} \tag{2.3}$$

where $h_L\left(s, [m_0], \Delta m_n, z_L\right)$ is the equivalent admittance seen by the first resonator looking into the rest of the terminated filter and depends on the topology of the filter.

The reactance of the last resonator is always in parallel with the admittance of the load transformed by the last inverter, resulting in

$$\begin{aligned} y_n &= j\left(m_{nn} + \Delta m_n\right) + m_{nL}^2 z_L \\ &= j m_{nn} + \left(j\Delta m_n + m_{nL}^2 z_L\right) \end{aligned} \tag{2.4}$$

where y_n is the admittance of the n-th resonator in parallel with the inverted load. From (2.3) and (2.4), the dependence of the input admittance on Δm_n and z_L is contained in y_n. With a little foresight the independence of y_{in} on Δm_n is enforced and later it is shown that this is equivalent to the simultaneous conjugate match. This is done as

$$\begin{aligned} j\Delta m_n + m_{nL}^2 z_L &= K_L \\ z_L &= \frac{K_L}{m_{nL}^2} - j\frac{\Delta m_n}{m_{nL}^2} \end{aligned} \tag{2.5}$$

without loss of generality, the real part of z_L is normalized, which leads to

$$K_L = m_{nL}^2 \tag{2.6}$$

and consequently making h_L independent of z_L and Δm_n as long as condition (2.5) is held, that is

$$\begin{aligned} h_L\left(s, [m_0], \Delta m_n, z_L\right) &= h_L\left(s, [m_0], y_n\right) \\ &= h_L\left(s, [m_0], m_{nn}, K_L\right) \\ &= h_L\left(s, [m_0], m_{nn}, m_{nL}^2\right) \\ &= h_L\left(s, [m_0]\right) \end{aligned} \tag{2.7}$$

where the last simplification is done because m_{nn} and m_{nL} are contained within $[m_0]$.

The input impedance is obtained from (2.3) and (2.7) as

$$z_{in} = \frac{1}{y_{in}} = \frac{h_L\left(s,[m_0]\right) + s + jm_{11} + j\Delta m_1}{m_{S1}^2}$$
$$= \left[\frac{h_L\left(s,[m_0]\right) + s + jm_{11}}{m_{S1}^2}\right] + j\frac{\Delta m_1}{m_{S1}^2} \tag{2.8}$$

given that the load impedance is

$$z_L = 1 - j\frac{\Delta m_n}{m_{nL}^2} = 1 + jx_L. \tag{2.9}$$

The output impedance of the filter can be simultaneously derived as

$$z_{out} = \left[\frac{h_S\left(s,[m_0]\right) + s + jm_{nn}}{m_{nL}^2}\right] + j\frac{\Delta m_n}{m_{nL}^2} \tag{2.10}$$

given that the source impedance is

$$z_S = 1 - j\frac{\Delta m_1}{m_{S1}^2} = 1 + jx_S \tag{2.11}$$

The terms in brackets in (2.8) and (2.10) do not explicitly depend on the resonator variations Δm_1 and Δm_n and are the frequency responses of the original design ($\Delta m_1 = \Delta m_n = 0$), for resistive terminations. In band, these terms are very close or equal (at the poles) to unity, indicating a good match. Section 2.1.1 proves that the frequency response of the reflection coefficient of the modified filter terminated in the complex impedances (2.9) and (2.11) is exactly that of the resistively-terminated original filter design.

The reactive part of the input and output port impedances can now be controlled by detuning the input or output resonators, 1 and n, respectively, while maintaining the same filter response. The real part of the port impedance remains normalized to the port resistance, and the necessary modification of the resonators for conjugate matching can be obtained from (2.8)-(2.11) as

$$\Delta m_1 = -x_S m_{S1}^2 = -\frac{X_S}{R_S} m_{S1}^2 \tag{2.12}$$

$$\Delta m_n = -x_L m_{nL}^2 = -\frac{X_L}{R_L} m_{nL}^2 \tag{2.13}$$

where X_S and X_L are the reactive parts of the source and load impedances, respectively, while R_S and R_L are the real parts and are also the normalizing resistances of the input and output ports, respectively.

This derivation works for parallel resonator topologies where the coupling matrix represents an admittance matrix (node equation formulation of the coupling matrix [10]). For the series resonator case (loop

equation formulation of the coupling matrix [10]) shown in Fig. 2.1c, the coupling impedance matrix variation terms can be similarly derived as

$$\Delta m_1 = -b_S m_{S1}^2 = -\frac{B_S}{G_S} m_{S1}^2 \tag{2.14}$$

$$\Delta m_n = -b_L m_{nL}^2 = -\frac{B_L}{G_L} m_{nL}^2 \tag{2.15}$$

where B_S and B_L are the reactive parts of the source and load admittances, respectively, while G_S and G_L are the real parts and are also the normalizing conductances of the input and output ports, respectively. It is worth noting that the frequency shift in the resonators is the same in the two cases, but with a different sign, since

$$\frac{B_S}{G_S} = -\frac{X_S}{R_S}. \tag{2.16}$$

2.1.1 Reflection Coefficient Equivalence

Given a normalized impedance $z_0(f)$, the reflection coefficient is given by

$$\Gamma_0(f) = \frac{z_0(f) - 1}{z_0(f) + 1} \tag{2.17}$$

this reflection coefficient is equal to that of another normalized impedance $z_f(f) = z_0(f) + jx$ for a source impedance $z_S = 1 - jx$. To prove this, the new reflection coefficient is expressed as [36]

$$\Gamma_f(f) = \frac{z_f(f) - z_S^*}{z_f(f) + z_S} \tag{2.18}$$

and substituting the impedance values, we obtain

$$\begin{aligned} \Gamma_f(f) &= \frac{[z_0(f) + jx] - (1 - jx)^*}{[z_0(f) + jx] + (1 - jx)} \\ &= \frac{z_0(f) - 1}{z_0(f) + 1} = \Gamma_0(f) \end{aligned} \tag{2.19}$$

therefore showing that the frequency response of the filter remains unaltered after adding an imaginary part to the port impedance as long as conjugate matching is still enforced.

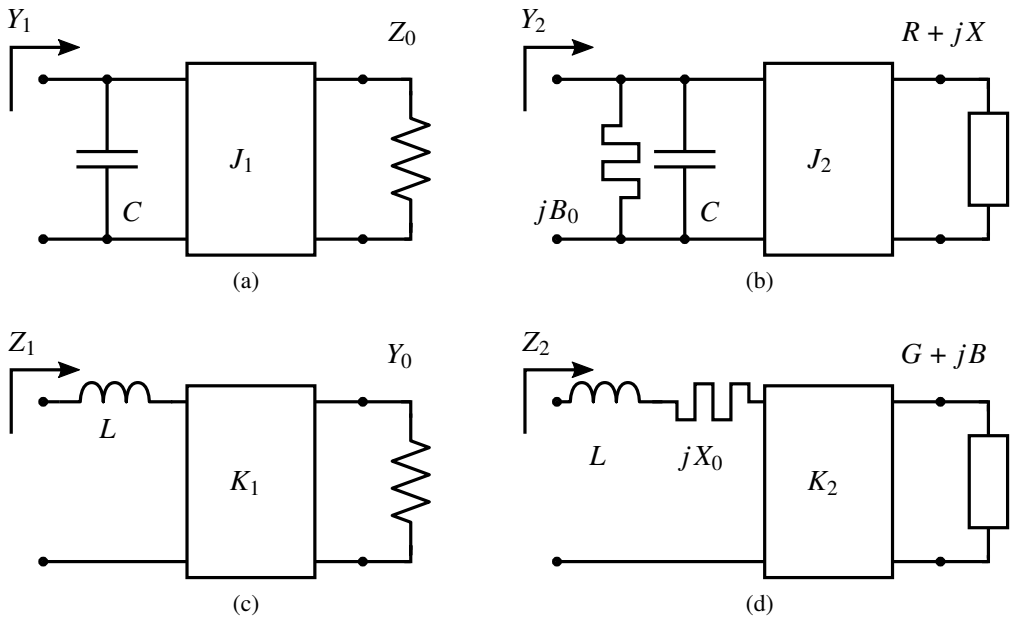


Figure 2.2: Low-pass representation of an edge resonator, inverter and termination for (a) parallel case and real termination, (b) parallel case and complex termination, (c) series case and real termination and (d) series case and complex termination.

2.1.2 Circuit-Level Analysis

Knowing that only the first and last resonators are modified, a simple and intuitive circuit analysis gives the same results as the coupled-resonator filter theory. Fig. 2.2a shows the low-pass representation of a resonator at one end of a filter and the inverter that couples that resonator to a resistive load. Fig. 2.2b shows the modified circuit where the resonator is altered by adding a frequency invariant reactance (FIR) B_0, which shifts the center frequency of the resonator. The equivalent input admittances are

$$Y_1 = j\omega C + Z_0 J_1^2 \tag{2.20}$$

$$Y_2 = jB_0 + j\omega C + (R + jX)\, J_2^2 \tag{2.21}$$

equating these and solving for B_0 and J_2, we obtain the modified values that will conserve filter performance:

$$B_0 = -\frac{X}{R} Z_0 J_1^2 \tag{2.22}$$

$$J_2 = \pm J_1 \sqrt{\frac{Z_0}{R}}. \tag{2.23}$$

If we follow the same approach as in the previous part and make the real part equal to the original resistance ($R = Z_0$) it can be seen that the inverter value remains unchanged within a sign, $J_2 = \pm J_1$ and the FIR value is given by

$$B_0 = -XJ_1^2 \tag{2.24}$$

which is analogous with (2.12) and (2.13).

Similarly, a filter with series resonators has the following equivalent impedances

$$Z_1 = j\omega L + Y_0 K_1^2 \tag{2.25}$$

$$Z_2 = jX_0 + j\omega L + (G + jB)\, K_2^2 \tag{2.26}$$

which can be combined to find the new FIR X_0 and impedance inverter K_2 as

$$X_0 = -\frac{B}{G} Y_0 K_1^2 \tag{2.27}$$

$$K_2 = \pm K_1 \sqrt{\frac{Y_0}{G}} \tag{2.28}$$

If $G = Y_0$, the following is obtained:

$$X_0 = -BK_1^2 \tag{2.29}$$

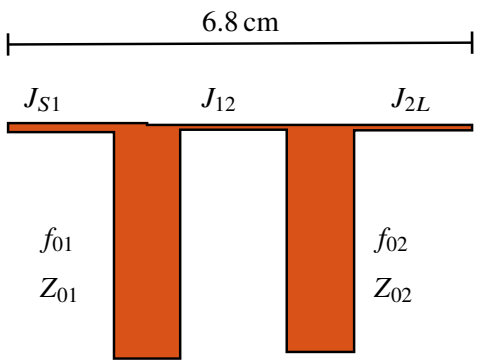
which is analogous to (2.14) and (2.15).

2.2 Experimental Validation

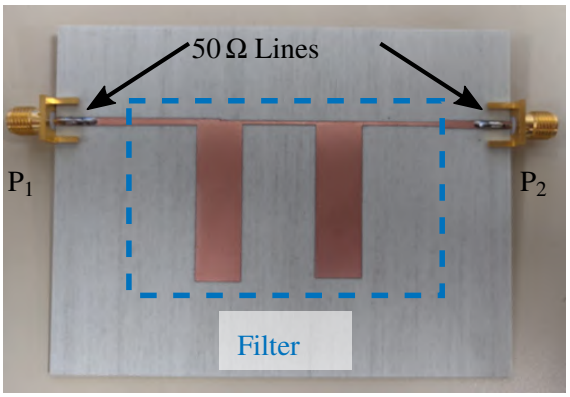
To verify the theory, we show two complex-to-complex impedance microstrip filter implementations: a 2^{nd} order all-pole filter, and a 4^{th} order elliptical filter, both Chebyshev-type. They use the same 762 μm-thick Rogers 4350B substrate with 35 μm-thick copper traces and ground plane.

2.2.1 Second-Order Filter Example

A simple microstrip filter using quarter-wave inverters and half-wave resonators is designed for arbitrarily chosen impedances $Z_S = (35 - j10)\ \Omega$ and $Z_L = (60 + j15)\ \Omega$. The filter is a 2^{nd} order all-pole Chebychev-



(a)



(b)

Figure 2.3: (a) Layout and (b) photograph of the 2^{nd} order filter. The dashed rectangle bounds the filter and indicates the position of the reference planes. The added 50 Ω line sections are deembedded using TRL calibration for accurate measurement of the filter at the appropriate reference planes.

type, with in-band return loss of $RL = 15$ dB, represented by the admittance coupling matrix

$$[m_0] = \begin{bmatrix} 0 & 1.0369 & 0 & 0 \\ 1.0369 & 0 & 1.2868 & 0 \\ 0 & 1.2868 & 0 & 1.0369 \\ 0 & 0 & 1.0369 & 0 \end{bmatrix} \tag{2.30}$$

which after modification for the complex impedance loading using (2.12) and (2.13), becomes

$$[m] = \begin{bmatrix} 0 & 1.0369 & 0 & 0 \\ 1.0369 & 0.3072 & 1.2868 & 0 \\ 0 & 1.2868 & -0.2688 & 1.0369 \\ 0 & 0 & 1.0369 & 0 \end{bmatrix} \tag{2.31}$$

and this matrix is referenced to the real part of the port impedances ($z_{0i} = r_i$). The filter response is centered at $f_0 = 2.4$ GHz with 8 % fractional bandwidth. Fig. 2.3 shows the layout and photo of the fabricated device.

This filter was designed using Cadence AWR for circuit and full-wave electromagnetic simulations (Axiem). The measured frequency response is compared to the simulations in Fig. 2.4, showing good agreement. The port impedances are the complex values previously specified. Fig. 2.5 shows the complex reflection coefficients at the filter ports when the other port is terminated in the design complex impedances.

It can be seen that the impedances looking into the filter are conjugately matched to $Z_S = (35 - j10)\ \Omega$ and $Z_L = (60 + j15)\ \Omega$ in the passband (loop).

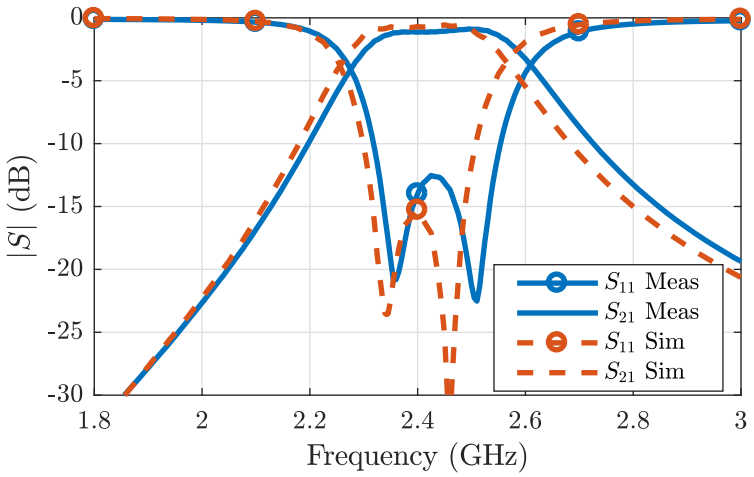


Figure 2.4: Simulation and measurement results for the 2^{nd} order Chebyshev microstrip filter seen in Fig. 2.3 with complex port impedances Z_S and Z_L. The measurement is performed in a 50-Ω environment and referenced to the complex port impedances in post-processing.

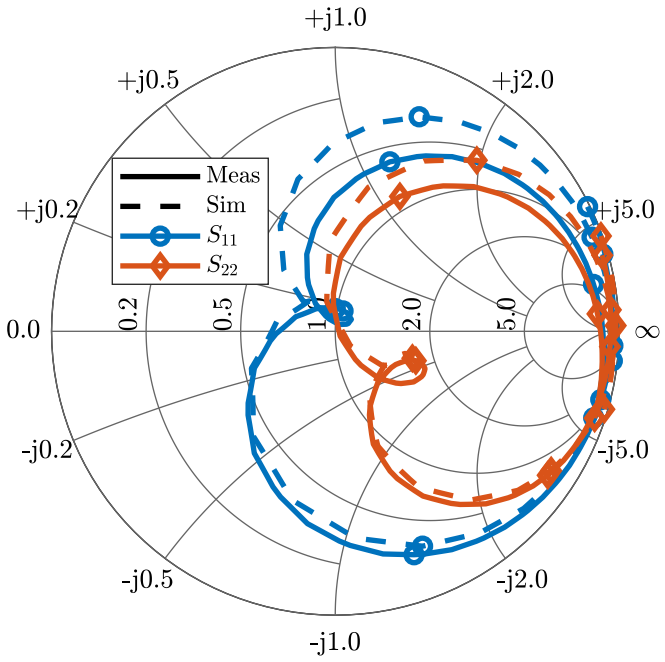


Figure 2.5: Simulated and measured S_{11} and S_{22} for the 2^{nd} order filter, Fig. 2.3 terminated in Z_S and Z_L. The measurement is performed in a 50-Ω environment and referenced to the complex port impedances in post-processing.

2.2.2 Fourth-Order Filter Example

A Chebychev-type 4^{th} order elliptical filter is designed next, with two transmission zeros at $s_{1,2} = \pm j1.9$ (normalized angular frequency) and $RL = 20\,\text{dB}$. Fig. 2.6a shows the node diagram for this filter where the original coupling matrix is

$$[m_0] = \begin{bmatrix} 0 & 1.0223 & 0 & 0 & 0 & 0 \\ 1.0223 & 0 & 0.8642 & 0 & -0.1926 & 0 \\ 0 & 0.8642 & 0 & 0.7757 & 0 & 0 \\ 0 & 0 & 0.7757 & 0 & 0.8642 & 0 \\ 0 & -0.1926 & 0 & 0.8642 & 0 & 1.0223 \\ 0 & 0 & 0 & 0 & 1.0223 & 0 \end{bmatrix}. \tag{2.32}$$

The filter is centered at $f_0 = 2.4\,\text{GHz}$ with 7.5 % fractional bandwidth. The, arbitrarily selected, port

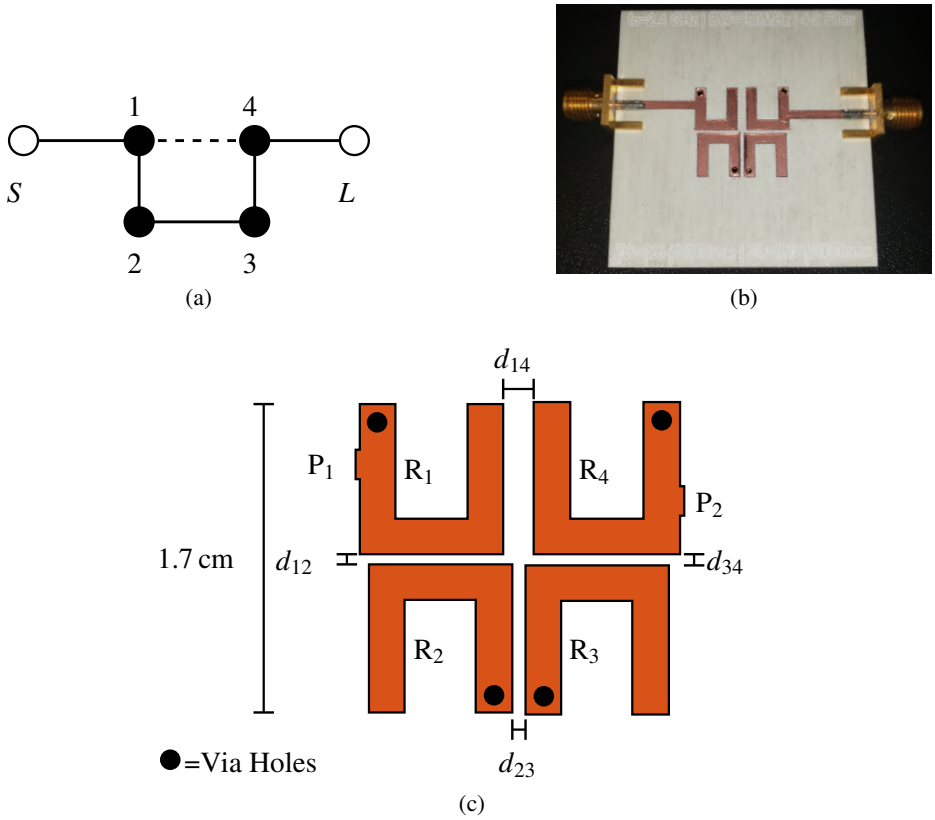


Figure 2.6: 4^{th} order elliptical microstrip filter (a) node diagram, (b) photograph and (c) layout.

impedances are $Z_S = (25 - j10)\ \Omega$ and $Z_L = (80 + j20)\ \Omega$, and the modified coupling matrix is:

$$[m_0] = \begin{bmatrix} 0 & 1.0223 & 0 & 0 & 0 & 0 \\ 1.0223 & -0.4180 & 0.8642 & 0 & -0.1926 & 0 \\ 0 & 0.8642 & 0 & 0.7757 & 0 & 0 \\ 0 & 0 & 0.7757 & 0 & 0.8642 & 0 \\ 0 & -0.1926 & 0 & 0.8642 & 0.2613 & 1.0223 \\ 0 & 0 & 0 & 0 & 1.0223 & 0 \end{bmatrix}. \tag{2.33}$$

The fabricated filter is shown in Fig. 2.6, where the resonators are folded quarter-wave microstrip lines and the couplings between the resonators are realized by adjusting the proximity (d_{ij}) between them. Resonators R_2 and R_3 are identical and resonate at the center frequency, while R_1 and R_4 are detuned according to (2.14) and (2.15) resulting in a higher resonant frequency (2.438 GHz) for the first resonator and a lower resonant frequency (2.377 GHz) for the last. Fig. 2.6 also shows a photo of the fabricated filter and the layout.

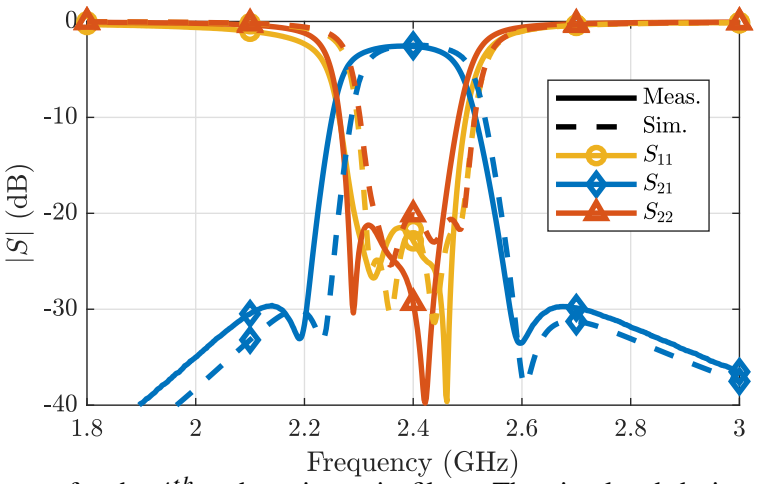


Figure 2.7: S-parameters for the 4^{th} order microstrip filter. The simulated design works with a source impedance of $25 - j10\,\Omega$ and load impedance of $80 + j20\,\Omega$. The fabricated filter impedances are shifted to $25 - j5\,\Omega$ and $76 + j14\,\Omega$ for the source and load, respectively.

The filter measured scattering parameters are compared to simulated ones in Fig. 2.7. The four poles and two transmission zeros can be clearly seen. Fig. 2.8 shows the input and output reflection coefficients of the filter when terminated in Z_S and Z_L. Variation from simulations is due to the fabrication tolerances and high sensitivity to filter dimensions which lead to small shifts in the operating impedances, center frequency

and fractional bandwidth.

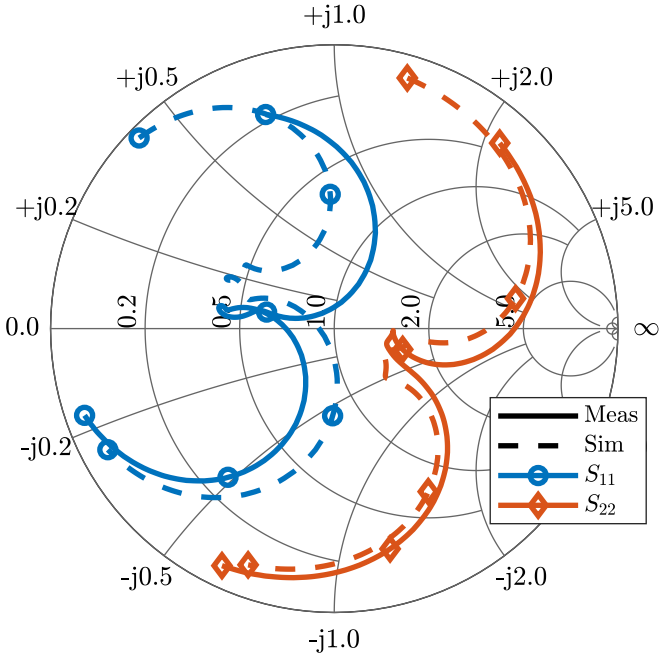


Figure 2.8: Complex input and output reflection coefficients of the 4^{th} order filter from Fig. 2.6. Data displayed goes from 2.2 to 2.6 GHz.

It is worth noting how the out-of-band filter impedances in Fig. 2.5 go towards the open, while the impedances in Fig. 2.8 go towards the short. This is an indication of a filter topology using parallel (Fig. 2.3) or series (Fig. 2.6) resonators.

2.3 Chapter Summary

This chapter develops the foundation that is used in the rest of the thesis for designing filters with complex terminations. The theoretical derivation shows that an imaginary (reactive) part can be added to the port impedance be means of a simple modification of a previously existing coupling matrix. The only constraint in this general method is that only internal cross-couplings between the resonators are allowed. The complex-impedance port formulation is first applied to a simple 2^{nd} order filter and a 4^{th} order filter with cross-couplings and transmission zeros. Two filters are implemented in microstrip at 2.4 GHz with all-pole and elliptical response, respectively, both with different complex impedances at the two ports. The filter

design and simulations agree well with experiments, validating the theory. The technique is used in the next Chapter to design filter matching networks with tuneable/adjustable port impedances. In later chapters, the methodology is applied to the design of power amplifiers with filtering characteristics. The contributions presented in this Chapter were originally presented in [37] and the full theory was published in [38].

Chapter 3

Tuneable Filter-Matching Networks

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3.3 Chapter Summary 41

In microwave front ends, as stated in Section 1.2, filtering is required between cascaded components, e.g. a power amplifier (PA) and antenna in a transmitter as shown in Fig.3.1. Many situations where the impedance of a component varies in time can be found, for example, the antenna impedance can vary due to scanning in a phased array (e.g. [39]) or changing surroundings as in a hand-held device (e.g. [40, 41]). Fig. 3.2 shows the VSWR variation of the antenna impedance in an array for different scanning angles and Fig. 3.3a displays the impedance variation of a handheld antenna under various parasitic loading conditions.

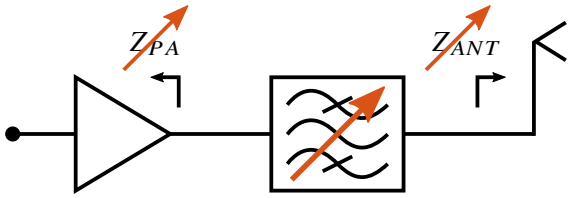
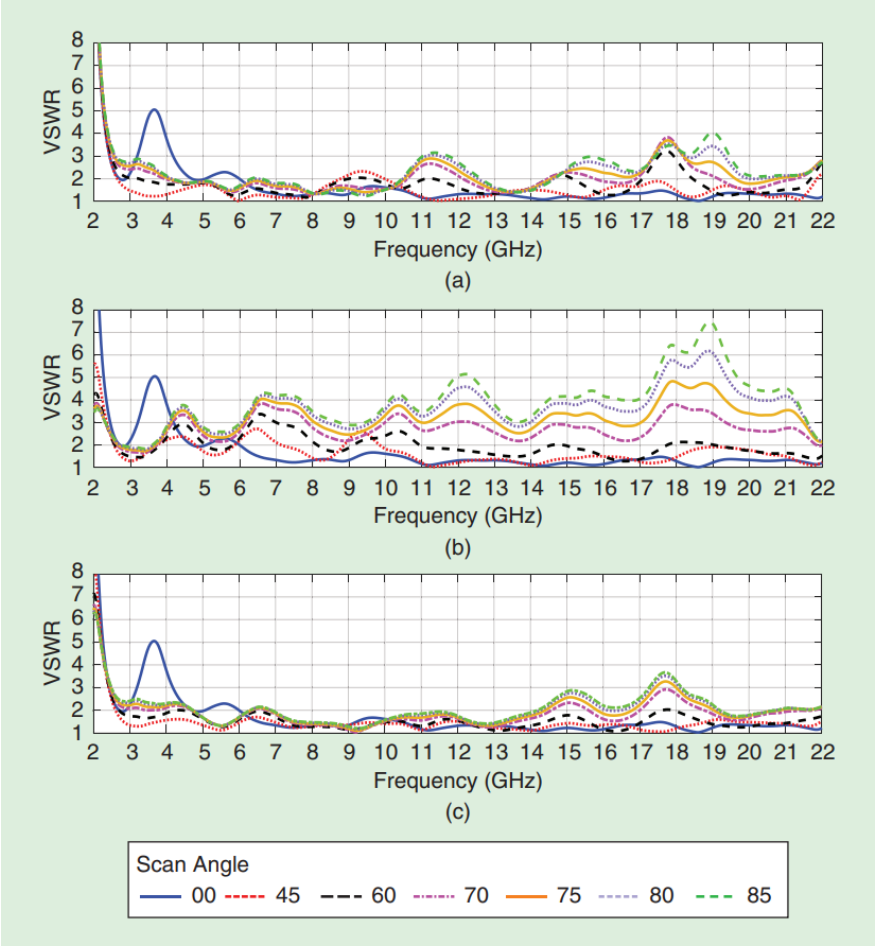


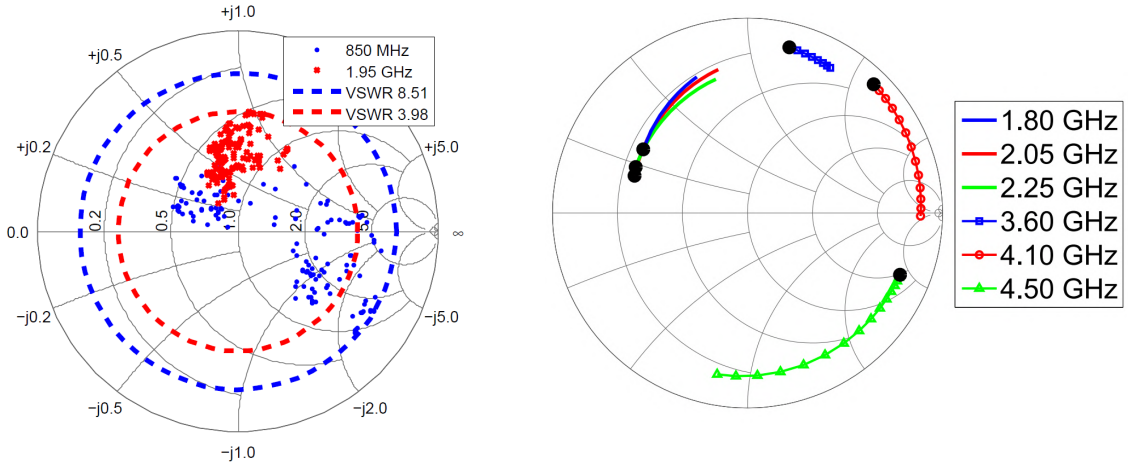
Figure 3.1: Transmitter front end, where both antenna impedance and PA output impedance can vary and can be matched with the tunable filter-matching network.



(a)

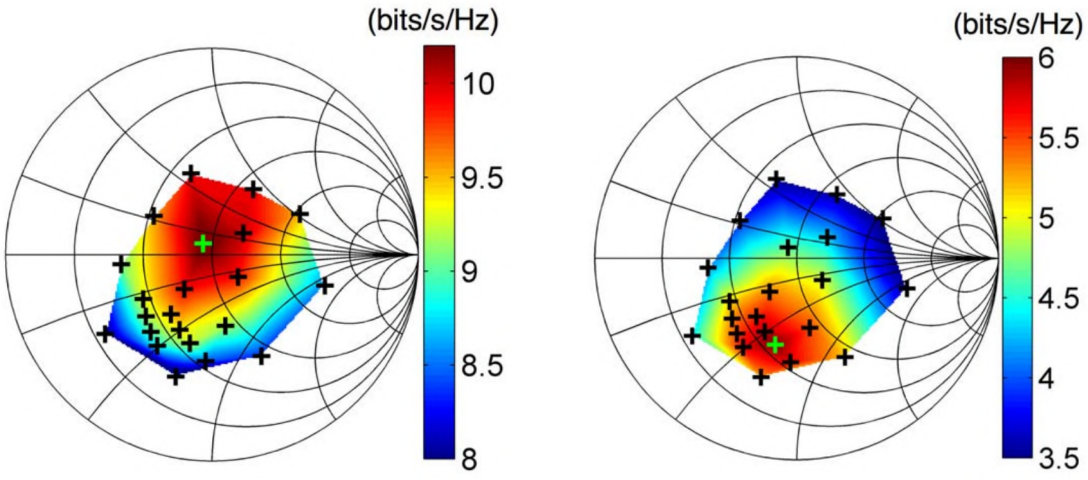
Figure 3.2: Measured active scan VSWR [39] for array embedded element [8, 8] of the 16 × 16 notch array in the (a) E-plane, (b) H-plane, and (c) D-plane.

The active device of a PA generally requires a complex impedance match for maximum power, gain or efficiency and this can vary over output power and supply voltage in applications such as envelope tracking (e.g. [44]). In dynamic load-modulation of PAs, tunable load impedances [45, 43] are also required to maximize the amplifier parameters at different power levels. Fig. 3.3b shows the variation of the optimum impedance to present to a 15 W bare die GaN HEMT (CGH60015D) from Cree (Wolfspeed), for maximum power added efficiency (PAE) at different frequencies and power levels. Beamforming MIMO [46] is another application where loads can vary in time and require adaptability. Fig. 3.4 shows the channel capacity variation heat map on a Smith chart for two different scenarios of a MIMO handset, such impedance variations can be compensated with tuning networks, which are typically lossy, e.g. [47, 46, 48]. To deal with



(a) (b)

Figure 3.3: (a) Measured impedance variations of a Nokia 6010 cell phone antenna [42] under various near-field loading conditions (near head, covered by hand, on metal table, etc.). (b) Simulated optimum impedance to present to a GaN HEMT transistor (CGH60015D) from Cree (Wolfspeed) for maximum PAE at different frequencies and for different power levels [43]. The black solid circles mark maximum output power.



(a) (b)

Figure 3.4: Average MIMO capacity: (a) Free space in shielded room and (b) firm grip in shielded room; black (+)—states measured; green (+)—optimal state. As seen in [46].

these impedance variations an impedance tuner would need to be added. A filter with tunable impedance eliminates the need for an additional tuning network by already incorporating said feature.

Previous efforts in using filters for impedance transformation are reported in the literature, filters designed

as real-to-real impedance transformers are discussed in, e.g. [49, 50, 51], and a filter that frequency tunes to a complex antenna is shown in [52]. In [53] the antenna is integrated with the filter achieving frequency tuneability.

The goal of this Chapter is to demonstrate codesign of an impedance-tuning network with a filter in order to reduce the footprint and loss of the front end. This filter should be capable of tuning the impedance over a specified region of the Smith chart. The fixed network design approach from the previous Chapter is extended to a tuneable network design here. The approach is demonstrated on a 2.5 GHz second-order Chebyshev filter with one fixed 50 Ω port, and one impedance variant port. The impedance is varied in both real and imaginary parts between 15 and 150 ohms.

The following Section will cover the general design methodology proposed for the design of impedance matching filters. A specific demonstrator circuit was designed and fabricated to validate the theory and it is presented in Section 3.2.

3.1 Design Methodology

From the theory developed in Chapter 2 it can be seen that the port impedance of a coupled resonator filter can be modified by adjusting the resonant frequency of the resonator that couples to said port and the value of said coupling [38]. The resonant frequency of the resonator is used to control the imaginary part of the port impedance. The coupling (inverter) to the first resonator is used to control the real part of the port impedance and also affects the imaginary part. The impedance modification does not alter the frequency response of the filter as long as it remains conjugately matched on both ports as shown in Subsection 2.1.1. Fig. 3.5 shows the diagram of a filter with a tuneable port impedance, displaying the tuneable elements needed.

The first admittance inverter value is inversely proportional to the square root of the real part of the port impedance and it is given by [9, 10]

$$J_{S1} = m_{S1}\sqrt{\frac{2\pi f_0 C\Delta}{R_S}} \tag{3.1}$$

where m_{S1} is the coupling matrix element for the source to resonator 1 coupling, f_0 is the center frequency, Δ is the fractional bandwidth, C is the base resonator capacitance and R_S is the reference port resistance. In

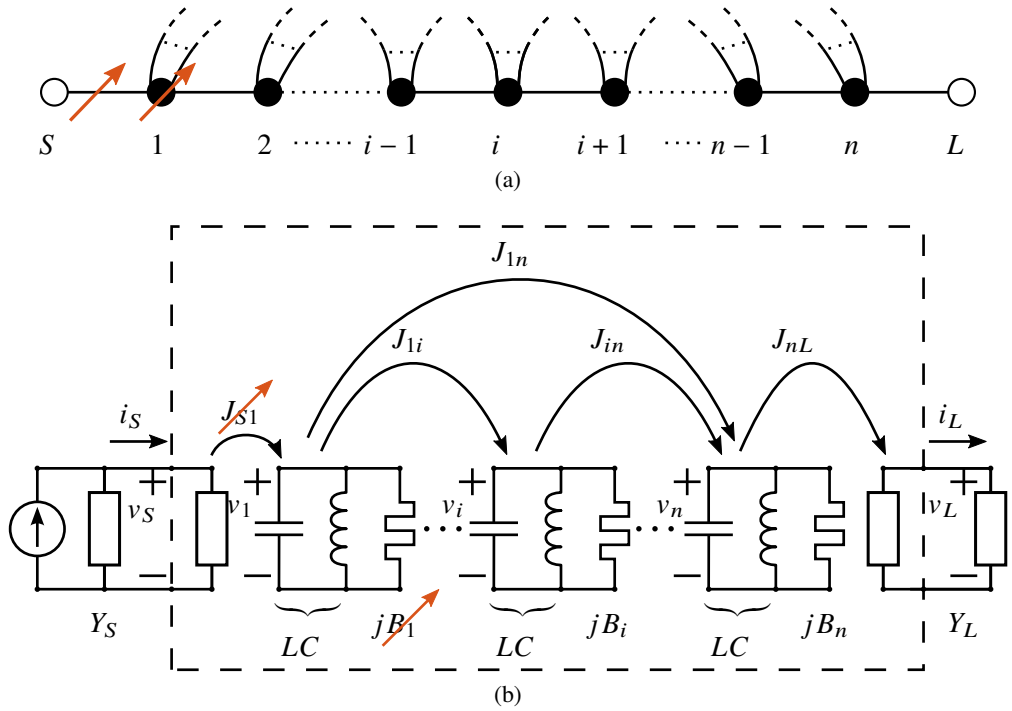


Figure 3.5: Filter diagram for an impedance tuneable filter. The two necessary tuneable elements are indicated with arrows. (a) Node representation and (b) ideal lumped-element circuit representation.

our case R_S is the real part of the target complex impedance $Z_S = R_S + jX_S$, which is the complex conjugate of the impedance the filter will present at its poles.

The resonant frequency of the first resonator as a function of the coupling matrix element can be found from the admittance of the resonator at resonance

$$Y_i = j\omega_{0i}C + \frac{1}{j\omega_{0i}L} + jB_i = 0 \tag{3.2}$$

which combined with equation (1.6) and the resonant frequency of the base resonator $\omega_0 = 1/\sqrt{LC}$ leads to

$$f_{01} = f_0 \left[\sqrt{1 + \left(\frac{m_{11}\Delta}{2} \right)^2} - \frac{m_{11}\Delta}{2} \right] \tag{3.3}$$

where $m_{11} = m_{110} + \Delta m_1$ is the coupling matrix element of the tuneable resonator and m_{110} is the original coupling matrix element of the filter terminated in a real impedance. This element can be used to adjust the imaginary part of the port impedance by using equation (2.12)

$$\Delta m_1 = -x_S m_{S1}^2 = -\frac{X_S}{R_S} m_{S1}^2, \tag{3.4}$$

it is worth noting that the source to resonator 1 coupling (m_{S1}) modifies both the real and imaginary parts, as evidenced by equations (3.1) to (3.4).

The resonant frequency can be controlled by using a capacitively terminated stub, Fig. 3.6a, and provides control over the imaginary part of the impedance. A tuneable inverter can be approximated using transmission line inverters [10] with a tunable stub, Fig. 3.6b. Both of these can be controlled using electronically controlled capacitors or even static tunable ones for manual tuning.

Other topologies and implementations for these tuneable elements can be used, such as, piezoelectric elements [54], MEMS [55, 56], liquid metal [57, 58], PIN diodes [59, 60], etc., depending on the specific application (e.g. high power, low loss, small footprint). In this work, varactors are used for the proof of concept.

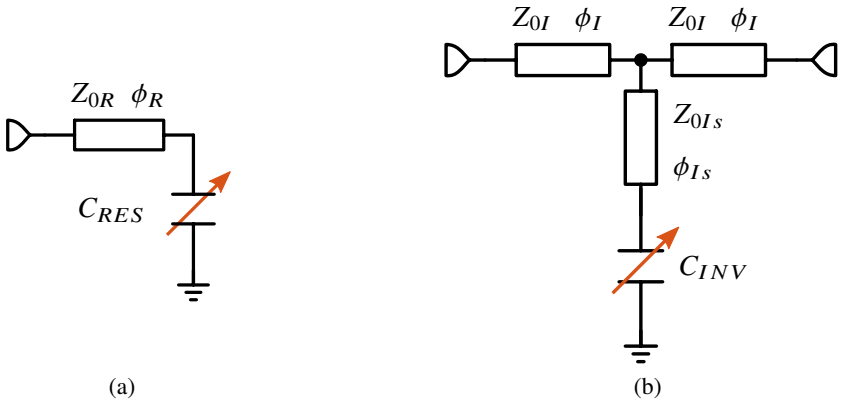


Figure 3.6: Tuneable elements used for the proof of concept design. (a) Capacitively terminated stub resonator and (b) transmission line inverter where the middle reactance is implemented with a capacitively terminated stub.

3.2 Varactor Based Demonstrator

The demonstrator filter schematic is shown in Fig. 3.7. The input inverter (J_{S1}) and the first resonator (f_{01}) are implemented with varactor-loaded stubs as the ones in Fig. 3.6, while the other two inverters (J_{12} and J_{2L}) are implemented with quarter-wavelength lines. The second resonator f_{02} is a half-wave open stub resonator.

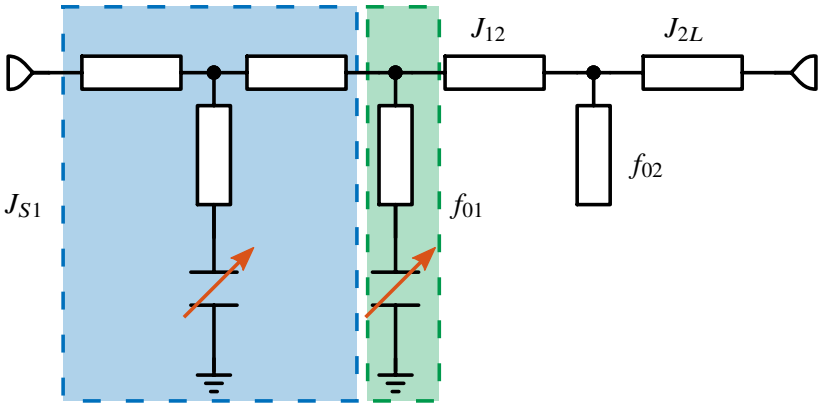
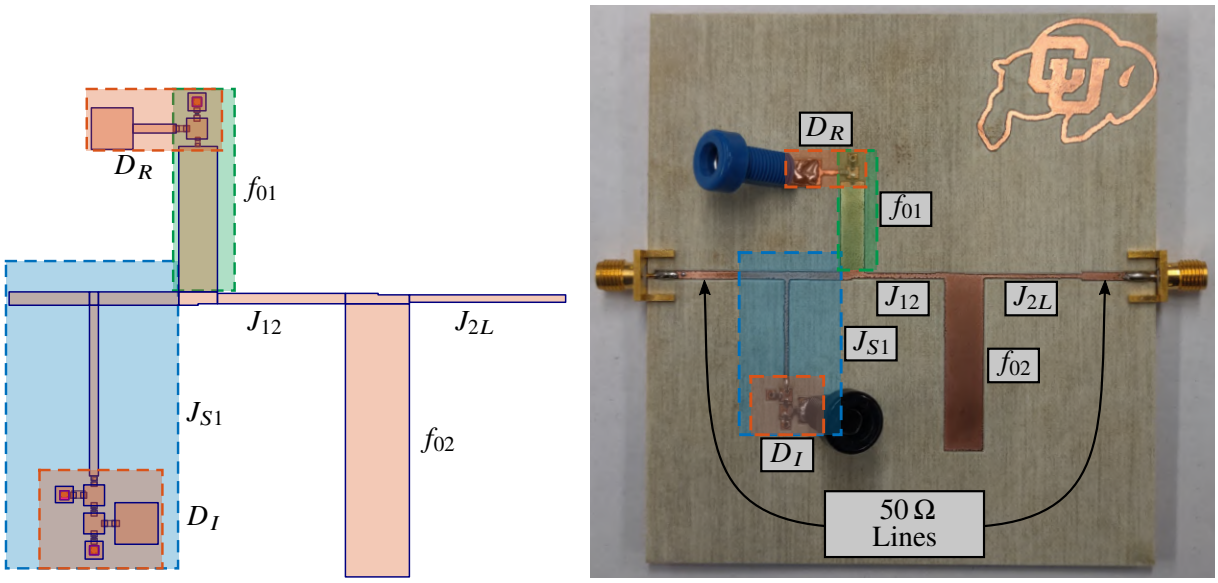


Figure 3.7: Schematic of the second order filter. The shaded areas are the tuneable input inverter (blue) and the tuneable resonator (green), same ones as in Fig. 3.6.

The fabricated filter is implemented in microstrip technology and can be seen in Fig. 3.8. A varactor is used to tune the resonator, and an anti-series varactor connection is used for inverter tuning.



(a) (b)

Figure 3.8: (a) Layout and (b) photo of the implemented filter, where the blue and green shaded rectangular areas correspond to the tuning elements in Fig. 3.7. D_R is the varactor used to tune the resonator and D_I are the anti-series varactors for inverter tuning.

3.2.1 Design and Simulations

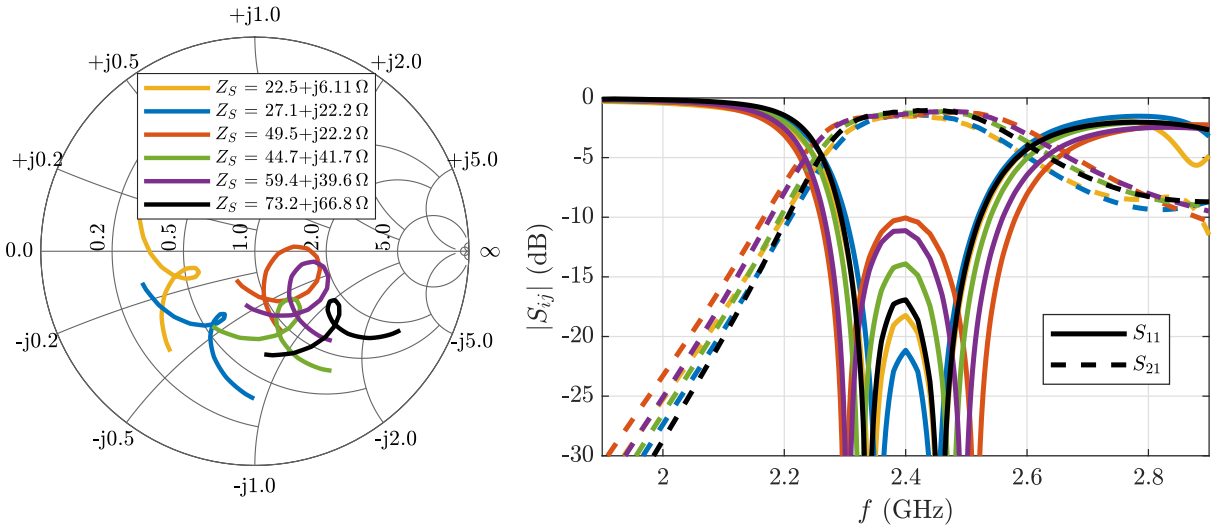
The filter is designed to be an in-line all-pole filter with 15 dB return loss. The coupling matrix for that filter is

$$[m] = \begin{bmatrix} 0 & 1.0369 & 0 & 0 \\ 1.0369 & 0 & 1.2868 & 0 \\ 0 & 1.2868 & 0 & 1.0369 \\ 0 & 0 & 1.0369 & 0 \end{bmatrix}. \tag{3.5}$$

and the filter is centered at 2.4 GHz with 9 % bandwidth. The port impedance of the filter is designed to cover a region in the lower (capacitive) half of the Smith chart, "centered" around a nominal impedance of $(45 + j42)\,\Omega$. Simulations are performed in Cascade AWR, the circuit is EM simulated using Axiem, the diodes and discrete passive (packaged) components are simulated using Modelithics models. The resulting layout is seen in Fig. 3.8 where the different components of the circuit are labeled according to Fig. 3.7.

The filter uses a Rogers RO4350B substrate with 762 μm dielectric thickness and 35 μm copper thickness. The variable capacitors are SMV2205-040LF varactor diodes from Skyworks which use a continuous control voltage from 2 to 10 V. The capacitance values for the design are closer to those of a single varactor for the resonator (3-15 pF) and an anti-series configuration for the inverter capacitance (1.5-7.5 pF). The diode biasing networks are implemented with lumped-element packaged inductors and capacitors.

The simulated performance of the filter for different port impedances is displayed in Fig. 3.9. Fig. 3.9a shows the port complex impedance around the passband. The loops cross at the filter poles which are located at each side of the center frequency of the filter. These poles occur when the impedance looking into the filter is the complex conjugate of the port impedance (Z_S). Fig. 3.9b shows the frequency response which maintains shape for the different varactor voltages. The loop size on the Smith chart is related to the match at the center frequency and the bandwidth. For the larger loops, where the impedance is the farthest from the loop crossing, the return loss is worse. The bandwidth and insertion loss of the filter do not change considerably, as the inverter and resonator are varied. The main limitation in the filter impedance tunability is the tuneable inverter which deviates from inverter behavior as the capacitance is changed, affecting the



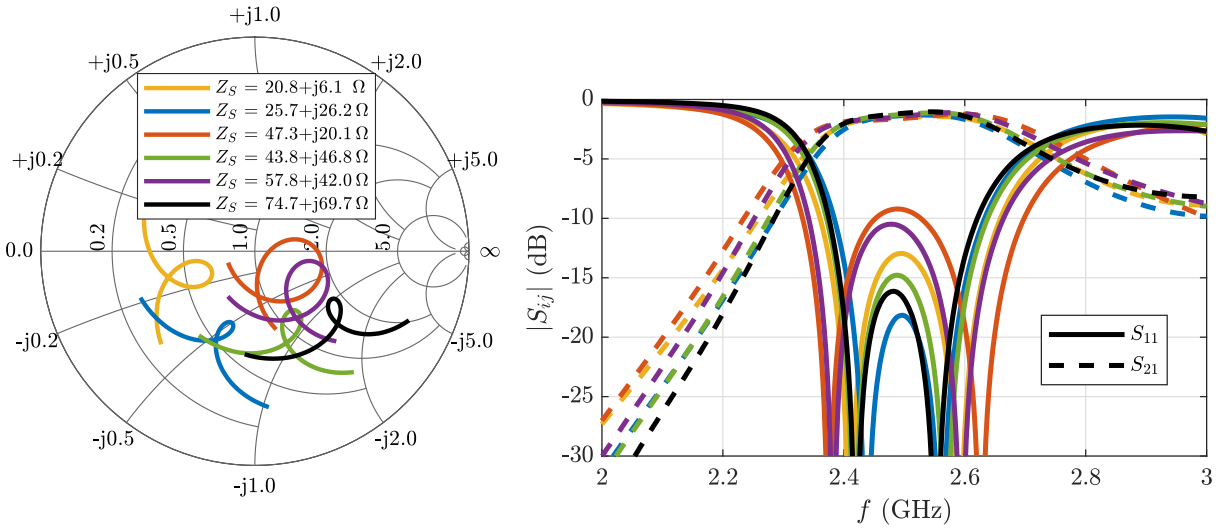
(a) (b)

Figure 3.9: Simulated filter performance (a) input reflection coefficient from 2.26 to 2.54 GHz on the Smith chart for different varactor bias voltages, and (b) frequency response for the different filter configurations. As the impedance deviates from the nominal $Z_L = (45 + j42)$ Ω, the quality of the match and the bandwidth present small variations, as expected.

behavior of the filter when tuned to a value far from the "center" impedance where the inverter is truly behaving as an inverter.

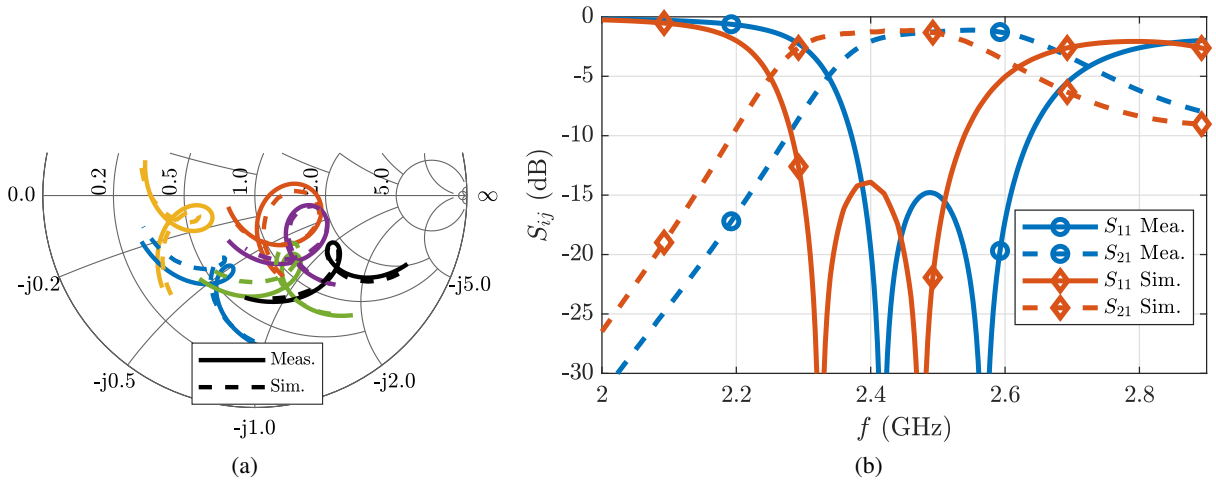
3.2.2 Measurement Results

The fabricated filter is shown in Fig. 3.8b. Additional 50 Ω transmission line segments are added at the input and output to transition to the connectors, and a TRL calibration is performed with reference planes exactly at the filter, which is critical when measuring a circuit with a non-standard port impedance to guarantee the correct measurement of not only the phase but also the amplitude of the measured S-parameters. The measured performance is shown in Fig. 3.10 where it can be seen that the filter center frequency is shifted upwards by 4%, compared to the simulations. The return loss remains larger than 10 dB in the passband with a large portion of the Smith chart covered. The the worst case, among all the tuning states, for the in-band insertion loss is 1.5 dB and can improved by replacing the resonators with higher Q-factor ones. Fig. 3.11 shows a comparison of simulation and measurement.



(a) (b)

Figure 3.10: Measured filter performance (a) input reflection coefficient, from 2.35 to 2.65 GHz, on the Smith chart for different configurations and (b) frequency response for those different filter configurations.



(a) (b)

Figure 3.11: Measured and simulated comparison filter performance (a) input reflection coefficient, around the center of the bands, on the Smith chart and (b) frequency response for the case with $Z_S = 44 + j47$.

3.3 Chapter Summary

This chapter presents a second-order Chebyshev filter with a tuneable input impedance over a range of the Smith chart. Measurements validate the feasibility of impedance tuning on a coupled resonator filter using a variable resonator and inverter with maintained filter response. The demonstrator filter uses varactor diodes as tuning elements, but the proposed technique can be extended to other technologies depending on

the application. The impedance tunability can be extended to the other port in a straightforward manner. The method shown here is valid for a relatively narrow bandwidths, and scaling to larger bandwidths and impedance range is under investigation. The contributions made in this Chapter are published in [61]. Filters with complex terminations can be used to eliminate the need of matching networks between system components. One example are filters at the output of power amplifiers meant to clean up the spectrum to satisfy a given spectral mask. In the next Chapter the co-design of filters and power amplifiers is explained and demonstrated.

Chapter 4

Integrated Filter Amplifiers

Contents

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The power amplifier (PA) is often the dominant power consumption component in the RF front end, because of this the efficiency of the PA is the crucial parameter of the front end design. For that reason, many high efficiency design techniques are used to minimize the losses in the PA. In high-efficiency PAs, the transistors are driven into saturation, resulting in linearity degradation [62, 63], exhibited as both in-band and out-of-band distortion [64]. Both of these can be partially addressed with analog or digital predistortion (DPD), e.g., [65, 66, 67], and some band-limited DPD schemes can be used to simplify system complexity with sophisticated 5G signals [68], but in many cases the PAs require additional filtering at the output to satisfy spectral masks. For example, out-of-band nonlinearities, including those further from the signal up to harmonic frequencies, are addressed by filtering in [69]. As more capacity is required in wireless communication, features like carrier aggregation make the problem of nonlinearities worse and filtering becomes more important [70]. Controlled filtering adjacent to an amplifier can also help with stability

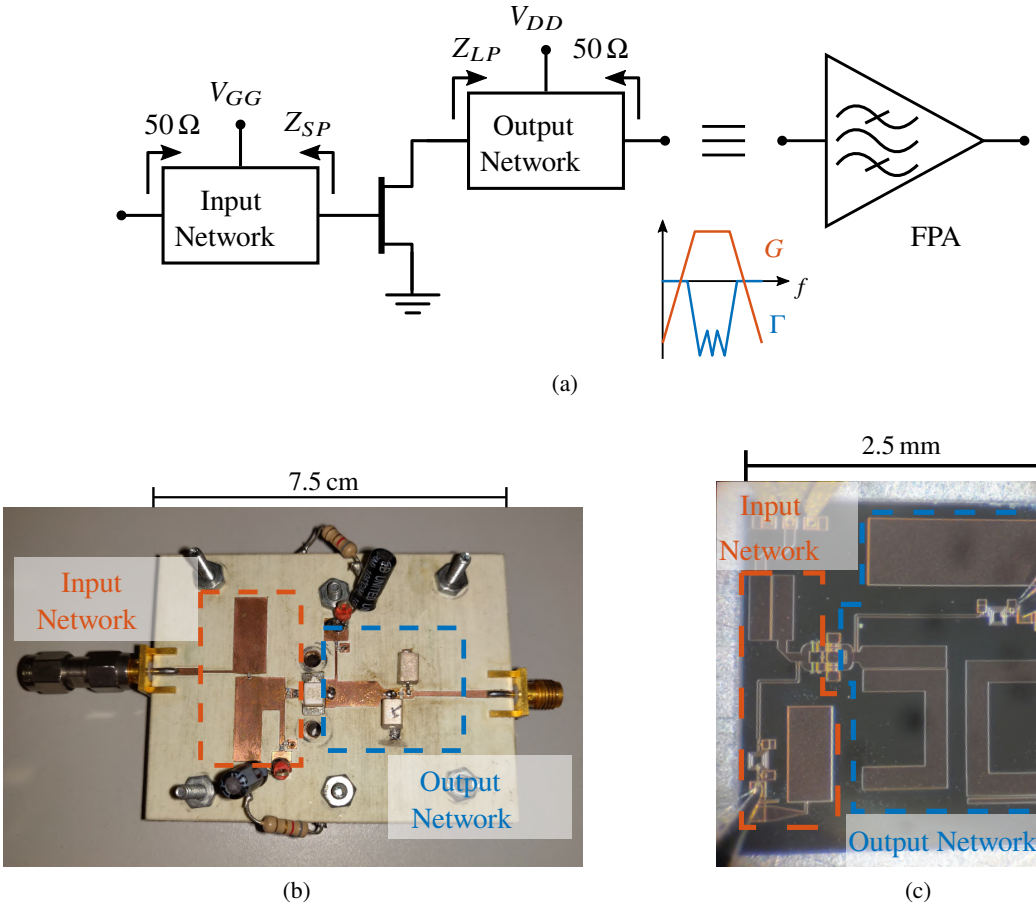


Figure 4.1: (a) Block diagram of the filter power amplifier (FPA), where the input and output networks are co-designed fundamental matching, harmonic termination, stability and bias networks, with a specific filter frequency response. (b) Hybrid implementation of an FPA designed for operation at a center frequency of 4.7 GHz (5G-FR1) with a 9 % bandwidth. (c) MMIC implementation of a FPA designed for operation at a center frequency of 28 GHz (5G-FR2) with a 9 % bandwidth.

and provide an extra degree of freedom during the design [71]. Filters cascaded at the input and output of microwave amplifiers in RF front ends [72] increase the overall loss and size of the system. Different applications favor either reduced loss, e.g. in high-power base-station transmitters [73] and in low-noise receivers [74], or reduced size, e.g. in portable devices [75] or space applications [76], where both size and weight are of vital importance.

Integration of the lossy matching network and filter can improve efficiency and reduce the size of a PA, as illustrated in Fig. 4.1. Here the matching, harmonic terminations, bias and stability networks are all considered together and designed to have a specific filter-type frequency response, as shown in more detail

in Fig. 4.2. Since transistors need to be matched to complex impedances for optimal operation, the first challenge is to establish a design method for complex terminations, rather than the real-valued source and load impedances that are used in standard filter design. This was done in Chapter 2 and the resulting method is used here.

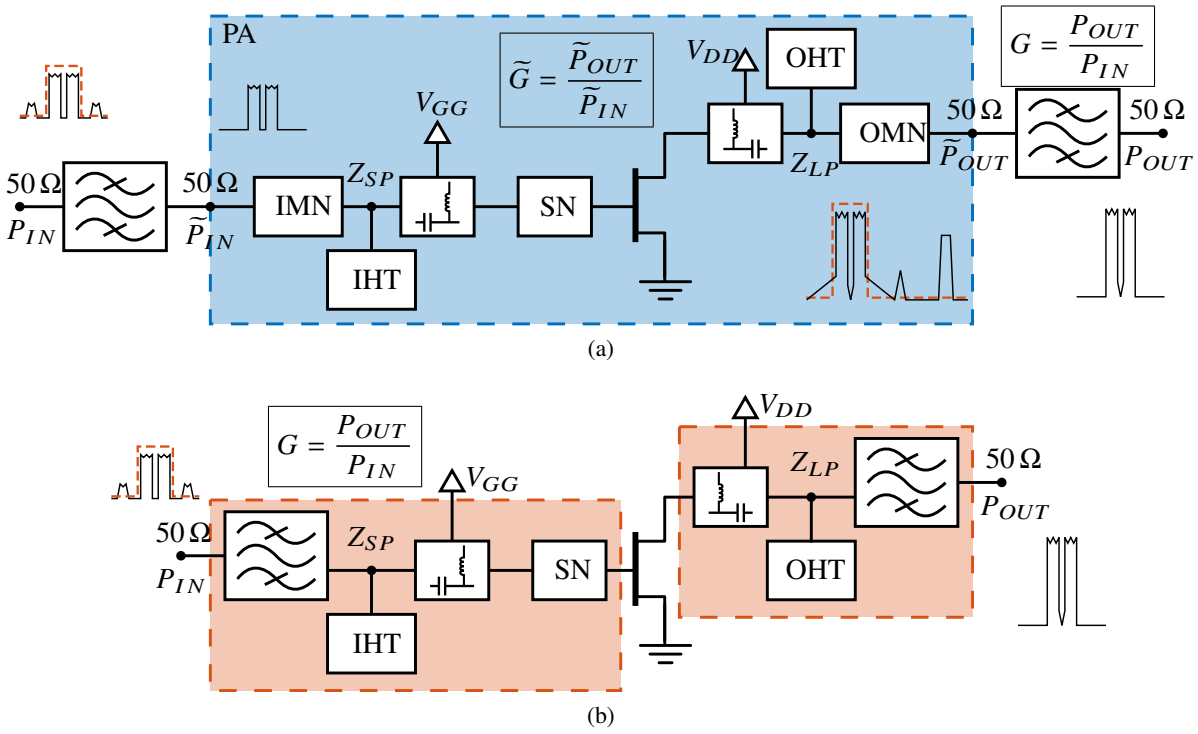


Figure 4.2: (a) Block diagram of a PA cascaded with filters at input and output, where the shaded area shows the PA alone. (b) Block diagram of the integrated filter with PA (FPA), where the input and output filters are the co-designed impedance matching filters (IMF). The shaded input and output networks correspond with the ones shown in Fig. 4.1a.

Previous efforts in this direction for amplifier design include [32] and [33], where 2^{nd} and 3^{rd} order output PA filter networks are implemented with evanescent-mode (EVA) cavity resonators around 3 GHz. Both are narrowband (less than 3 % fractional bandwidth, FBW) with 10 W of output power, efficiencies around 70 % and greater than 10 dB gain. The corresponding equations for filter design are shown for the specific cases of 2^{nd} and 3^{rd} order all-pole transfer functions with only one complex terminated port. [34] extends the work in [32] by adding a source to load coupling, which allows two symmetric transmission zeros to be added to the frequency response.

Additional research in [35] presents an active $N + 3$ coupling matrix that extends the work in [33] by

generalizing to an n-th order mainline filter, while incorporating a transistor model for small-signal input conjugately-matched amplifier design. This work is expanded in [77] to include a filter output match, and in [78] to include the effect of gate-drain feedback and estimate the noise figure from the coupling matrix. In this thesis the work from Chapter 2 generalizes the existing filter theory to include complex input and output impedances for n-th order filters with internal cross-couplings and can be applied to the co-design of filter PAs (FPA). Two designs are presented to validate the design method, first a hybrid FPA at 4.7 GHz shown in this Chapter and second a GaAs MMIC FPA at 28 GHz, shown in the next Chapter. Both FPAs are shown in Fig. 4.1b and 4.1c, respectively.

4.1 Impact of Output Loss in Amplifier Efficiency

The resulting efficiency of a PA cascaded with an output block, like a filter or a matching network, is largely affected by the loss of the output block. The power added efficiency (PAE) of an amplifier is given by

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}}\left(1 - \frac{1}{G}\right) \tag{4.1}$$

where P_{OUT}, P_{IN} and P_{DC} are the output, input and DC powers, respectively, and $G = P_{OUT}/P_{IN}$ is the amplifier gain. The PAE of the cascaded system is then given by

$$PAE' = \frac{P'_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}L - \frac{P_{OUT}}{G}}{P_{DC}} \tag{4.2}$$

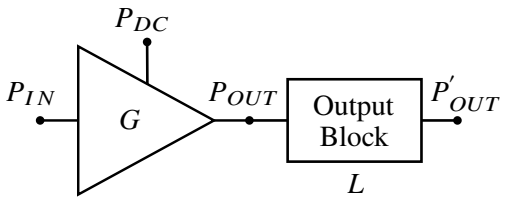
$$PAE' = \frac{P_{OUT}}{P_{DC}}\left(L - \frac{1}{G}\right) \tag{4.3}$$

where P'_{OUT} is the output power leaving the output block, PAE' is the cascaded system PAE and L is the loss of the output block. The PAE of the cascade can then be written as a function of the amplifier's PAE, the output block loss, and the gain of the amplifier as

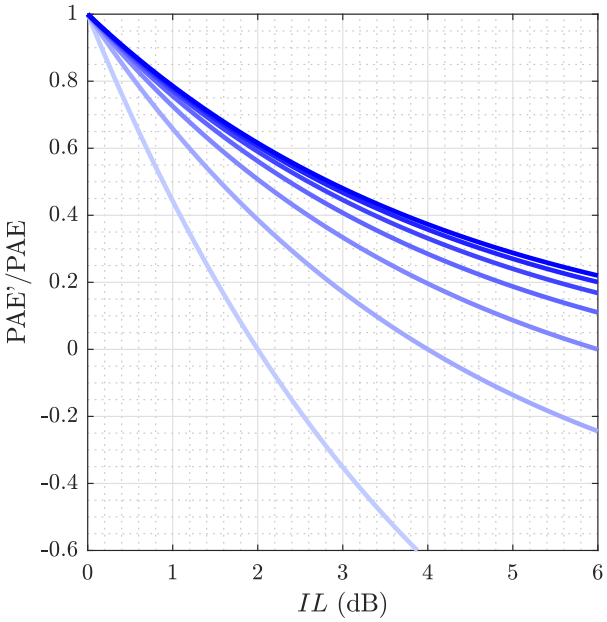
$$PAE' = PAE\left(\frac{L \cdot G - 1}{G - 1}\right) \tag{4.4}$$

which is reduced to 4.1 when the output block has no loss ($L = 1$). The quantities involved are shown in Fig. 4.3, as well as plots illustrating 4.4. The resulting PAE is plotted vs the insertion loss, defined as

$$IL = -10\log(L)\,. \tag{4.5}$$



(a)



(b)

Figure 4.3: Power added efficiency of cascaded components. (a) Block diagram of the cascade of an amplifier and a lossy output block. (b) PAE degradation vs output block insertion loss for various gain values from 2 dB to 14 dB with a 2 dB step.

It can be seen that there is a large impact of the output block loss in system efficiency. As expected the efficiency drops to zero when the loss of the output block is equal to the gain of the amplifier, i.e. the output is power is the same as the input power. An amplifier with a PAE of 70 % and 10 dB gain will see an efficiency drop of 16, 29 and 39 percentage points if cascaded with a network that has a loss of 1, 2 and 3 dB, respectively. For this reason it is important to reduce the losses at the output of the amplifying device, this is true for filters cascaded with amplifiers, for matching network losses and any other component cascaded after the PA.

4.2 Hybrid Validation (Ceramic Coaxial FPA)

The FPA is designed for operation in the sub-6 GHz (FR1) range of the 5G technical specification [4] utilizing filters as the matching networks as illustrated in Fig. 4.1a and 4.2. The sub-6 GHz design is centered at 4.7 GHz with 36 dBm output power, and is implemented as a hybrid circuit with a packaged GaN device.

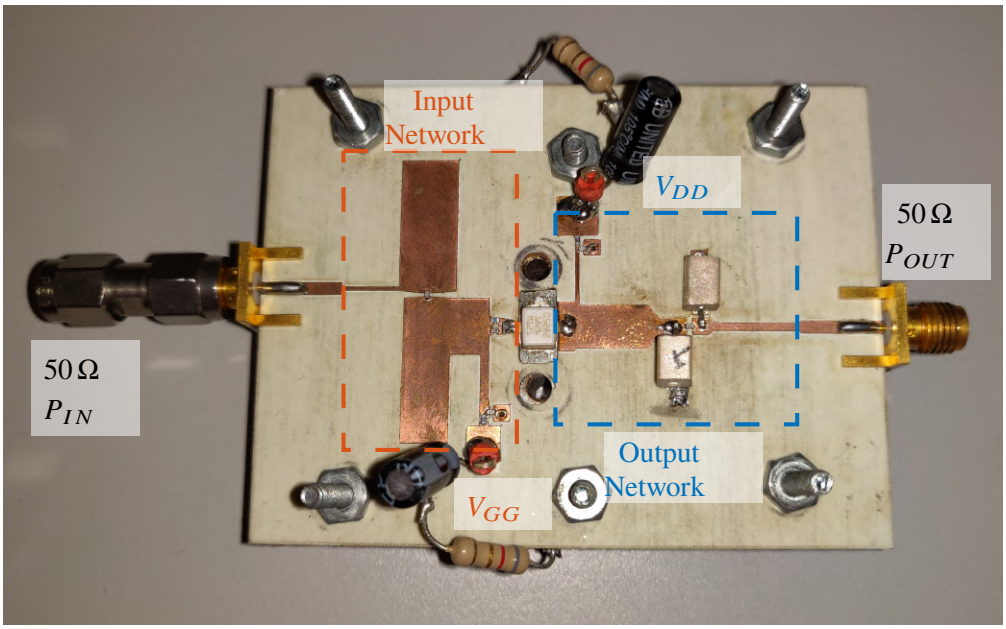


Figure 4.4: Photo of the hybrid GaN FPA designed for operation at a center frequency of 4.7 GHz with a 9 % bandwidth.

4.2.1 Filter-Power Amplifier Design

The fabricated hybrid FPA can be seen in Fig. 4.4. Due to the low Q-factor of microstrip resonators, and large impact of the output matching network loss on PA efficiency, discussed in Section 4.1, ceramic coaxial resonators (Q = 700, manufactured by T-Ceram) are used in the output matching filters. These have a dielectric constant of 20, giving them a small form factor, and are custom made to work at the specific frequencies necessary for the design. The PA is designed around Qorvo's T2G6000528-Q3 GaN packaged transistor and is simulated using Cadence AWR's harmonic balance for the non-linear simulations with a Modelithics non-linear transistor model. The substrate is Rogers 4350B with a relative permittivity of ϵ_r = 3.75, thickness of 762 μm and with 35 μm copper metallization.

The impedance matching filters (IMF) at the input and output are designed to load the transistor with impedances for an efficiency and output power compromise. The fundamental impedances of the filters and harmonic terminations [79] are found using load-pull harmonic balance simulations and Fig. 4.5 shows the load- and source-pull contours.

The IMFs are designed to have a 2^{nd} order Chebyshev-type response with RL = 15 dB using the coupling

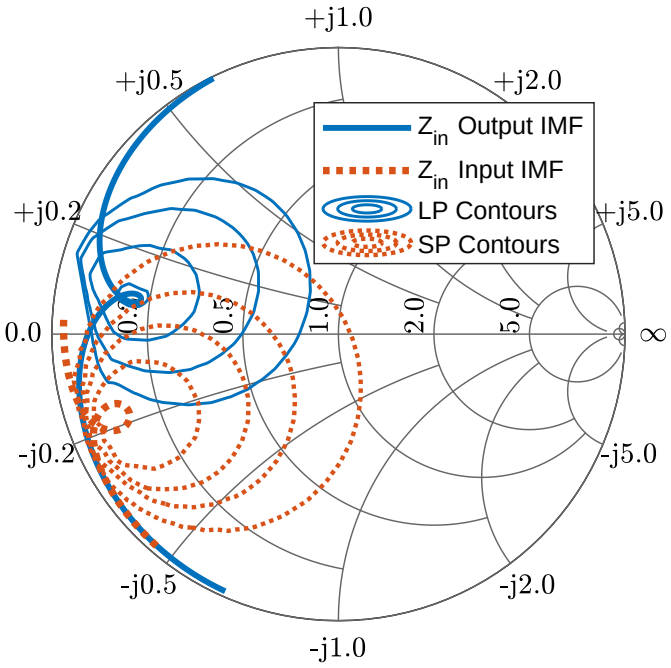
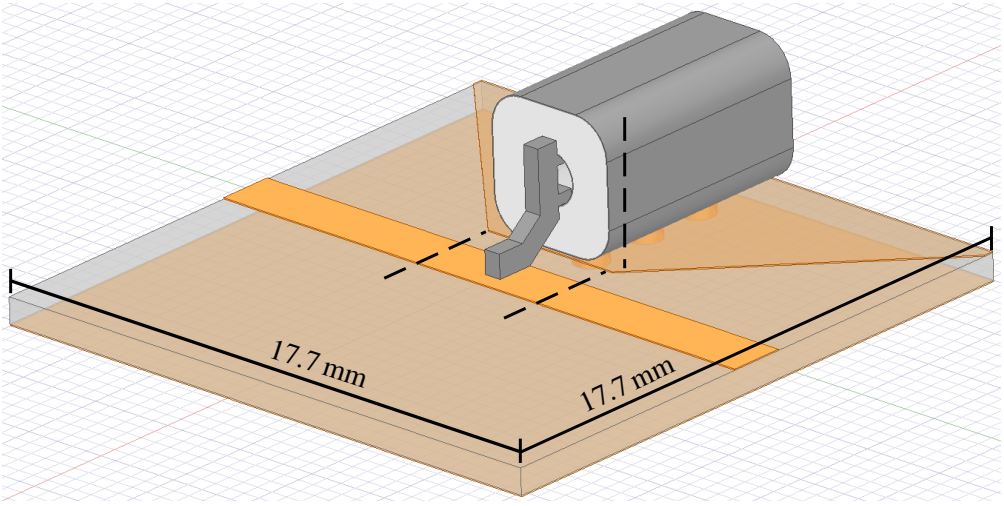


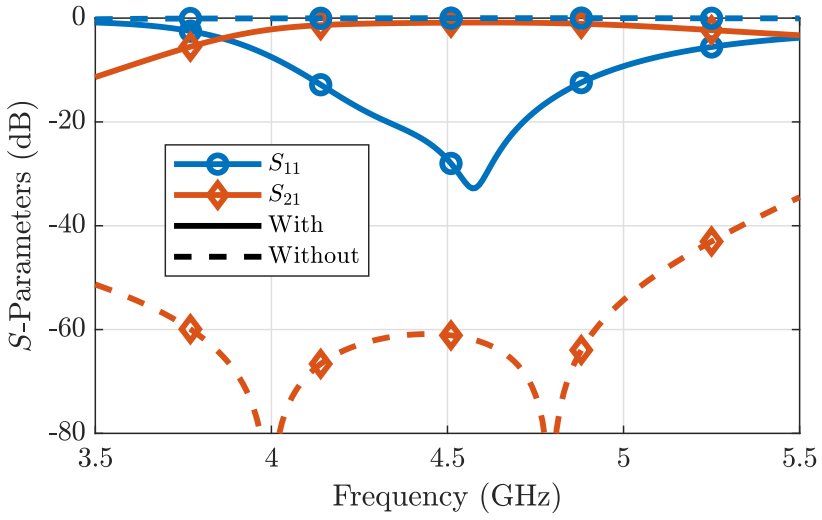
Figure 4.5: Simulated IMF responses overlaid with 4.7 GHz load- and source-pull contours for Qorvo's T2G6000528-Q3 GaN transistor. IMF responses are plotted from 3.4 to 6 GHz.

matrix in Eq. (2.30). Both IMFs have a center frequency of 4.7 GHz and 9 % fractional bandwidth. The use of filters at the input and output increase the FPA out of band rejection. The filters use open half-wavelength resonators and quarter-wavelength inverters at the input and output couplings. The coupling between the resonators is implemented with a capacitive inverter. The negative capacitances in the π-network inverters are incorporated as a frequency shift in the resonators (i.e. they are substracted from the equivalent resonators capacitances). The inverter also serves as the dc block in the transistor biasing network, providing additional integration of PA components.

The modeling of the transition through the resonator tab in the output filter is essential. Here it is modeled as a three-port network by 3D EM simulations in Ansys HFSS (FEM), as shown in Fig. 4.6a. A comparison of the simulation with and without inclusion of the geometry of the tab is given in Fig. 4.6b, showing the importance of accurate modeling of parasitic and propagation effects in this transition. The open end of the resonator is also characterized using 3D simulation, and is very close to an ideal open circuit, as expected due to the high permittivity of the dielectric. Finally, the harmonic terminations are implemented with a



(a)



(b)

Figure 4.6: (a) Resonator tab transition simulation model (HFSS) showing the deembedding planes for the three-port network. (b) Comparison of output IMF performance with and without modeling the tab transition.

shorted (grounded capacitor) stub that also serves as an RF choke for dc biasing of the gate and drain.

4.2.2 Measurement Results

A PNA E8364C microwave network analyzer was used with an automated high power measurement setup based on [80], example B. The small-signal measurements in Fig. 4.7 show that the FPA exhibits a filter response in both small-signal gain and input reflection coefficient (Γ_{IN}).

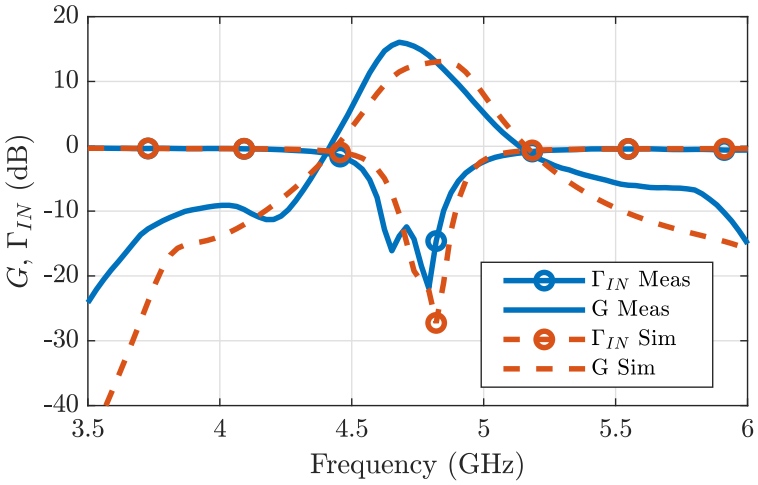


Figure 4.7: Measured and simulated small-signal gain and input match of the hybrid 4.7 GHz FPA from Fig. 4.4, showing gain and frequency selectivity.

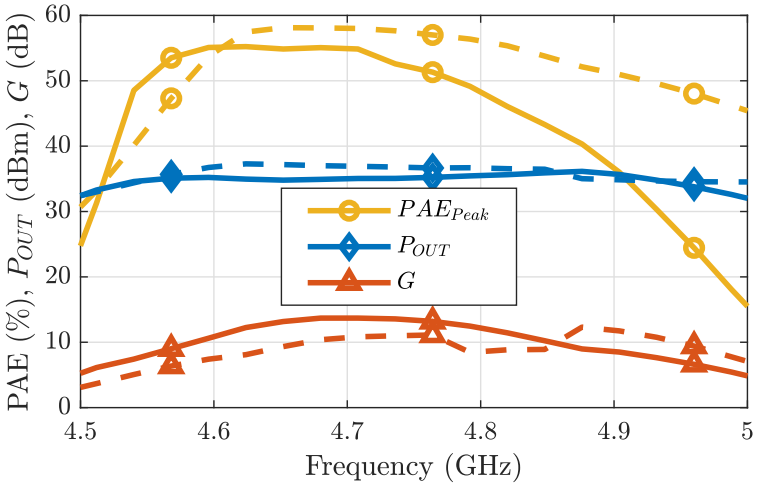


Figure 4.8: Hybrid GaN FPA large-signal simulations and measurements as a function of frequency, where the dashed lines represent simulations. The efficiency, output power, and gain are all given at the peak efficiency point for all frequencies.

Fig. 4.8 presents the large-signal performance of the hybrid FPA as a function of frequency. For each frequency point all curves are plotted at the output power (P_{OUT}) level that results in peak-PAE. The measured gain and PAE for the FPA at the center (4.7 GHz) and the edges (4.5 and 4.9 GHz) of the band are shown in Fig. 4.9. The PAE reaches 55 % at 4.7 GHz with a saturated gain of 13.7 dB. Measurements and simulations have good agreement and the small discrepancies between them can be attributed to fabrication tolerances in the pcb milling process, as well as the imperfect transistor nonlinear model.

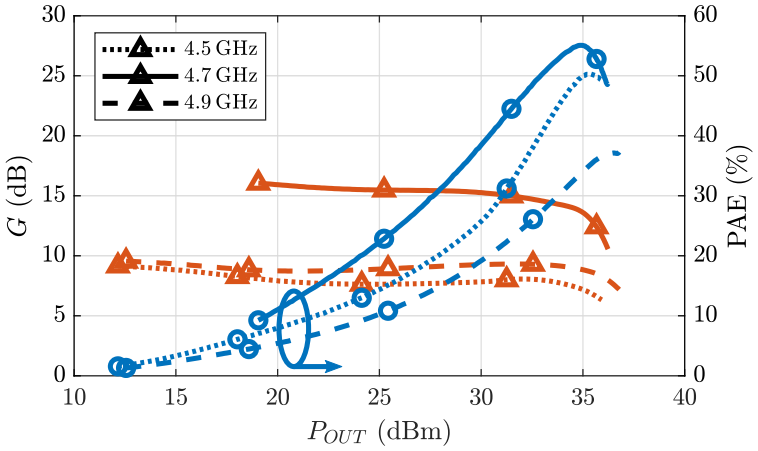


Figure 4.9: Measured PAE as a function of P_{OUT} for the hybrid GaN FPA at the center and edges of the band.

4.3 Chapter Summary

This chapter introduces a method for co-designing filters and power amplifiers (PAs) with a desired frequency response, improved efficiency and reduced footprint. In order to implement this type of co-design, the theory from Chapter 2 is used. The approach is applied to a single-stage high-efficiency 4.7 GHz, 4 W hybrid GaN filter-PA (FPA) within a sub-6 GHz 5G band. The measured performance shows a gain of 15 dB, PAE=55 % with 9 % fractional bandwidth, and 10 dB rejection at 4.5 and 5 GHz.

Fig. 4.10 is a simulation comparison of the 4.7 GHz microstrip FPA with a PA designed using the same load-pull impedance and harmonic terminations but using a traditional matching network, cascaded with a 50 Ω filter with the same exact frequency response, topology and implementation as the OMF in the FPA for a fair comparison.

A comparison of the state-of-the-art in co-designed filters and amplifiers with arbitrary complex impedances is shown in Table 4.1. Some of the examples in the table are general allowing n-th order filters, while others only show only 2^{nd} or 3^{rd} order cases. [81] and [69] do not have complex filter terminations, but rather use a transmission line section to transform the impedance to a real value. [32] and [33] employ 2^{nd} or 3^{rd} order main-line filter topologies and use evanescent-mode cavity resonators for output matching at 3 GHz. [34] presents an output 2^{nd} order matching filter with source-to-load coupling at

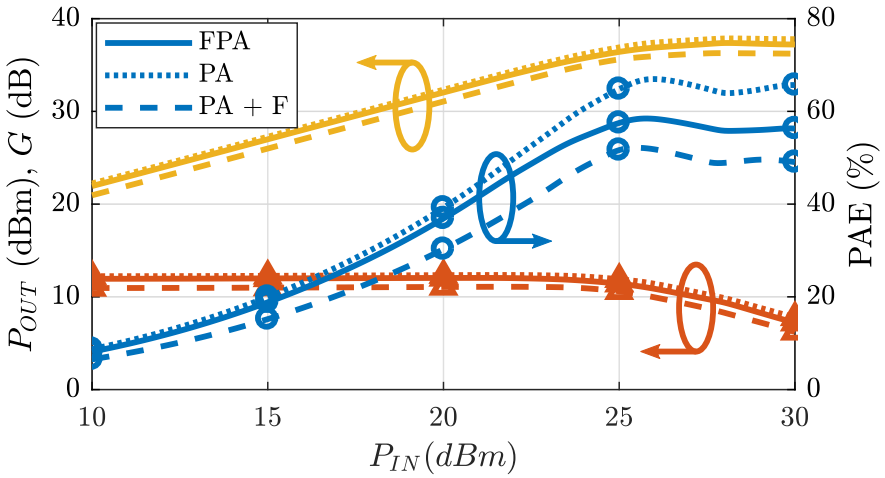


Figure 4.10: Simulation comparison between the designed FPA, a PA where the output matching network is made with a more traditional stub matching and that same PA cascaded with a filter designed in the same way as the one in the FPA but using 50 Ω ports on both sides. The footprint of the FPA is reduced by approximately 20 % when compared to a cascaded PA and filter.

2.4 GHz. Work described in [35],[77] show X-band filters using large rectangular waveguide cavities with conjugate matching of the transistors. An extension to substrate-integrated waveguide (SIW) cavity filters with a feedback in the transistor is shown in [78], including a method to estimate the noise figure from the coupling matrix. The dimensions of the filter amplifiers mentioned in Table 4.1 are very hard to compare due to the vastly different implementations and are therefore omitted. The last row of Table 4.1 is a MMIC integrated FPA, which is the first MMIC integrated FPA and the highest frequency implementation to date. This MMIC design is the subject of the next chapter. The method presented in this Chapter is general and applies to both input and output complex-impedance filter matching networks, showing that reduced size and loss can be achieved by filter-amplifier co-design. The theory and experimental validation presented here is shown for narrowband transmitter power amplifiers with the goal of filtering out-of-band spectral content. The contributions given in this Chapter were published in [38]. An interesting extension of this work to broadband transmitters should include the frequency-dependent active device impedance, and is a topic of future research.

Table 4.1: Comparison of FPA work. * theory allows n-th order designs. † only cross-coupling is the source to load one. ‡ theory only allows internal cross-couplings.

Ref.	Order	Cross Couplings	Complex Ports	Resonator Technology	Amplifier Type	f_0 (GHz)	FBW (%)	G (dB)	P_{out} (dBm)	PAE (%)
[81]	2	-	No-O	Microstrip	Hybrid MOSFET PA	2.6	3.8	14.3	42.5	46
[69]	4	-	No-O	Microstrip	Hybrid GaN PA	2	20	16.2	40.5	62
[32]	2	No	Yes-O	EVA Cavity	Hybrid GaN PA	3	3	> 10	40	68
[33]	3	No	Yes-O	EVA Cavity	Hybrid GaN PA	3.1	1.7	15.5	40	67
[34]	2	Yes†	Yes-O	Coaxial Cavity	Hybrid GaN PA	2.4	11	18.2	41	71
[35]	2*	No	Yes-I	Rectangular Cavity	Hybrid GaAs GS	10	5	11.7	-	-
[77]	2*	No	Yes-IO	Rectangular Cavity	Hybrid GaAs GS	10	5	11.1	-	-
[78]	2*	No	Yes-IO	SIW	Hybrid GaAs GS	10	5	9	-	-
This work	2*	Yes‡	Yes-IO	Microstrip (Input) Ceramic Coax. (Output)	Hybrid GaN PA	4.7	9	15	36	55
This work	2*	Yes‡	Yes-O	Microstrip On-chip	MMIC GaAs PA	28	5	8	23	30

Chapter 5

Filter Power Amplifier MMIC

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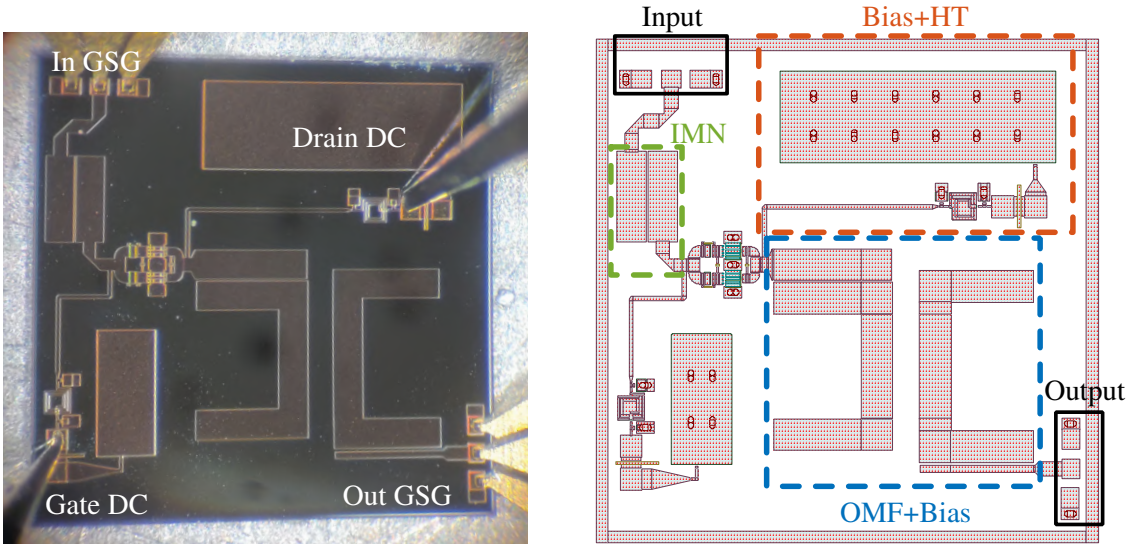
A monolithic microwave integrated circuit (MMIC) is an active or passive microwave circuit formed in situ on a III-V semiconductor by a combination of deposition techniques including diffusion, evaporation, epitaxy, implantation and other means [82]. MMICs are able to provide very small circuits with tremendous design flexibility, small cost and large-scale manufacturability with high yield. The size of the circuits enables design at very high frequencies such as millimeter waves. Most microwave components can be implemented in MMIC form (i.e. amplifiers, switches, attenuators, phase shifters, circulators, etc.) due to the availability of most necessary circuit elements (transistors, diodes, resistors, capacitors, inductors and transmission lines) and the freedom of precise geometry control of the circuit. The most mature MMIC semiconductor technology is Gallium Arsenide (GaAs) [82]. Gallium Nitride (GaN) has gained popularity due to its wide-bandgap that allows higher voltage operation that leads to 3-5 times the output power of GaAs [83]. For frequencies above 200 GHz Indium Phosphide (InP) is commonly used, these MMICs can

implement devices with cuttoff frequencies above 400 GHz [84].

In this Chapter a GaAs MMIC FPA at 28 GHz is designed for operation in the millimeter wave (FR2) range of the 5G technical specification [4] utilizing filters as the matching networks as explained in Chapter 4. The resulting MMIC amplifier has an output power of 23 dBm with 8 dB gain and power added efficiency (PAE) of 30 %, with a rejection of 8 dB at 26.5 and 29.6 GHz.

5.1 MMIC Design

The MMIC is implemented in WIN Semiconductor's 150-nm GaAs PIH1-10 enhancement-mode HEMT process and it is shown in Fig. 5.1. The active device is an 8×75 μm HEMT obtained by combining two 4×75 μm devices with a via between them for improved thermal performance. As in the hybrid design, the gate and drain impedances to be presented to the device are determined from load-pull simulations using the manufacturer-provided nonlinear model and EM-simulated manifolds. All simulations are performed in Cadence AWR with EM simulations of the critical passive portions of the MMIC simulated with Axiem in AWR and resonator optimization simulated in Ansys HFSS (eigenmode simulation).

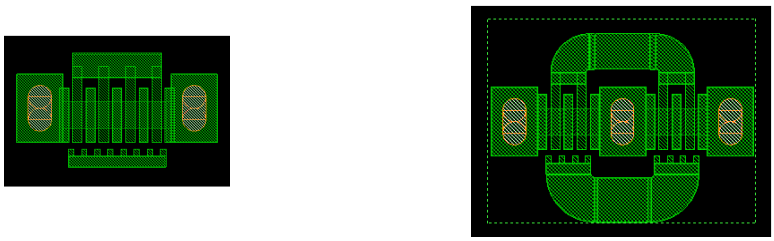


(a) (b)

Figure 5.1: (a) Photo and (b) layout of the GaAs MMIC FPA showing the input matching network (IMN), biasing (Bias), harmonic terminations (HT) and output matching filter (OMF). The die size is 2.5 mm × 2.5 mm.

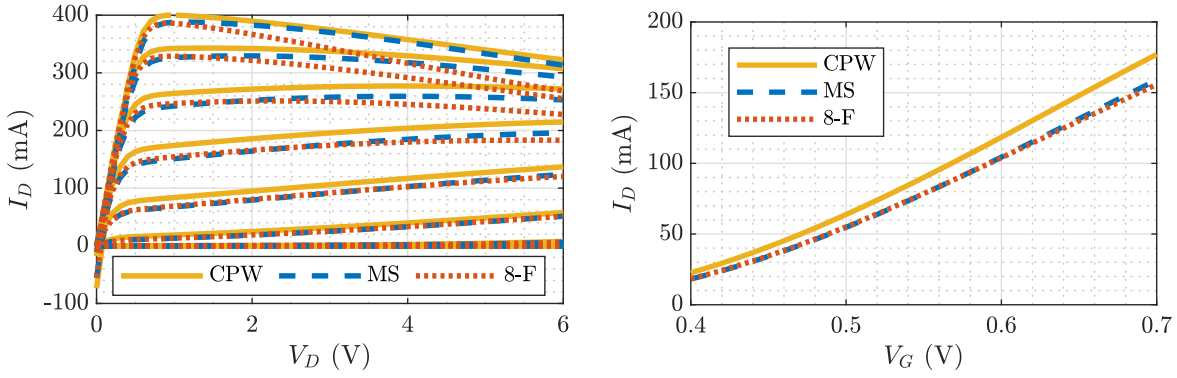
5.1.1 Device Selection

The first step for designing the MMIC is the device selection. An 8-finger device with 75 μm gate width is used with a ground via in the middle, this is done to reduce the source to ground impedance while providing an improved thermal path for the heat dissipated in the device. The WIN process design kit offers two different models that can be used to simulate such device. One approach is to use two 4×75 μm "microstrip" models, the possible problem with this is the incorporation of two ground vias per device, the real design will only have three vias, not four, and will make the modeling inaccurate. The other method is to use a "CPW" model, which has no vias. The three vias can then be EM simulated and incorporated to the design. An 8×75 μm transistor is also used as a benchmark for comparison purposes. Fig. 5.2 shows the two possible layouts.



(a) (b)

Figure 5.2: Layout of (a) 8×75 μm device and (b) 4×75 μm devices combined with gate and drain manifolds and added center and side grounds.



(a) (b)

Figure 5.3: Comparison between the different transistor models (a) IV-curves with 0.15 V steps in gate voltage going from -0.3 to 1.2 V, and (b) drain current vs gate bias voltage for a drain voltage of 4 V.

Fig. 5.3 shows the DC comparison plots for the three models. The IV-curves show that all three models behave very similarly at smaller voltage values. The CPW model is the most different one but follows the same trends as the microstrip model, pointing towards differences in the via modeling. At higher voltages the 8-fingers model trend separates from the other two models implying divergent behavior at higher powers, which is to be expected due to the improved thermal behavior or the combined 4-fingers models.

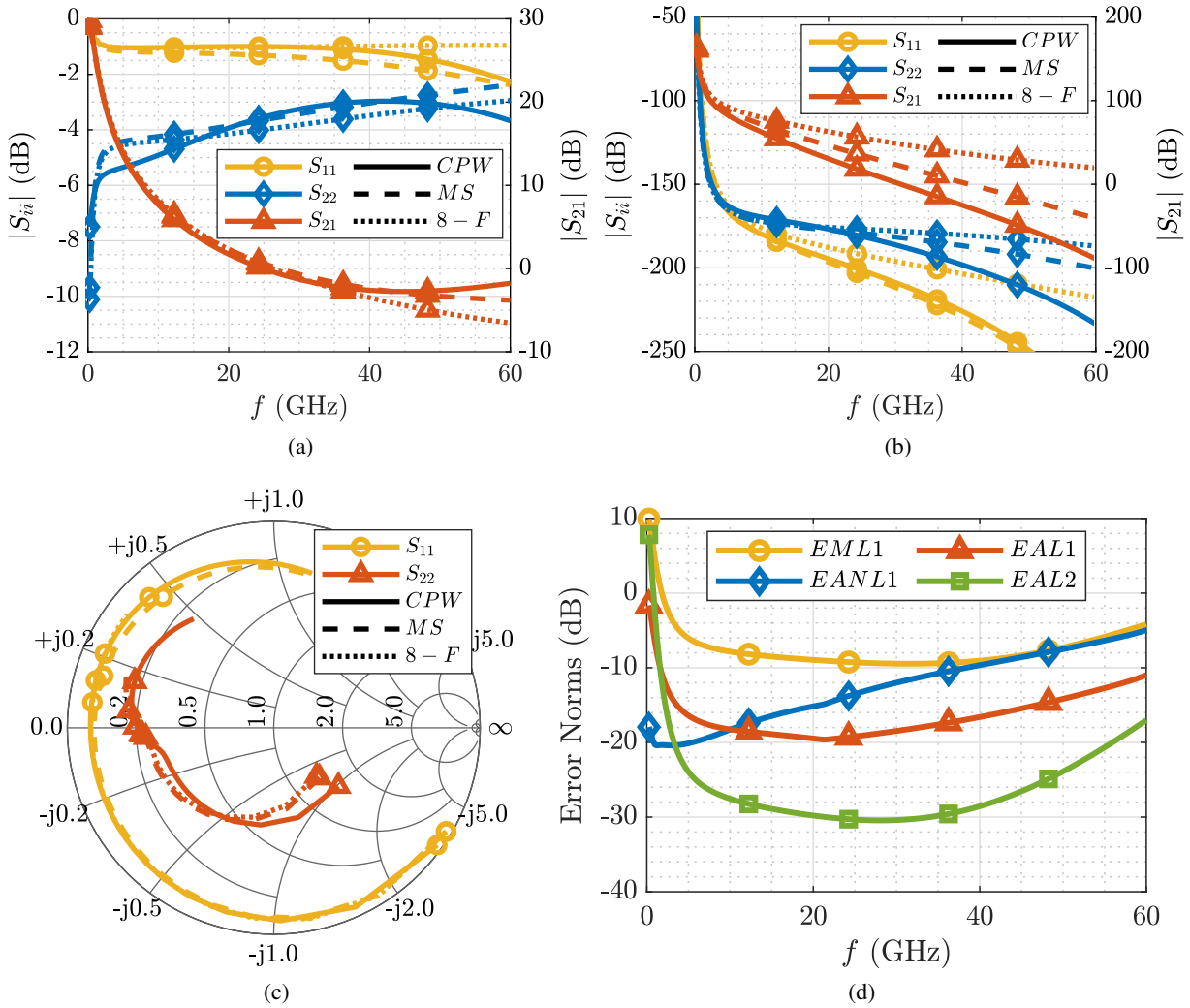


Figure 5.4: S-parameters comparison between the different transistor models (a) magnitude, (b) phase, (c) Smith chart and (d) Norms comparison, defined in equations (5.1)-(5.4) for the "microstrip" and "CPW" models.

The small-signal comparison of the models is shown in Fig. 5.4, for all three models. The models are very similar across the simulated band with the CPW model deviating the most in magnitude and the

8-fingers model differs the most in phase. At lower frequencies the CPW model diverges the most from the other two and this can be seen clearly in the Smith chart as the parameters start from different spots for that model.

Fig. 5.4d shows the norm comparisons for the "microstrip" and "CPW" models, the formulas used for calculating these norms are

$$EML1 = Error_{max\ L1} = \max\left(\left|S_{ijA}\right| - \left|S_{ijB}\right|\right) \tag{5.1}$$

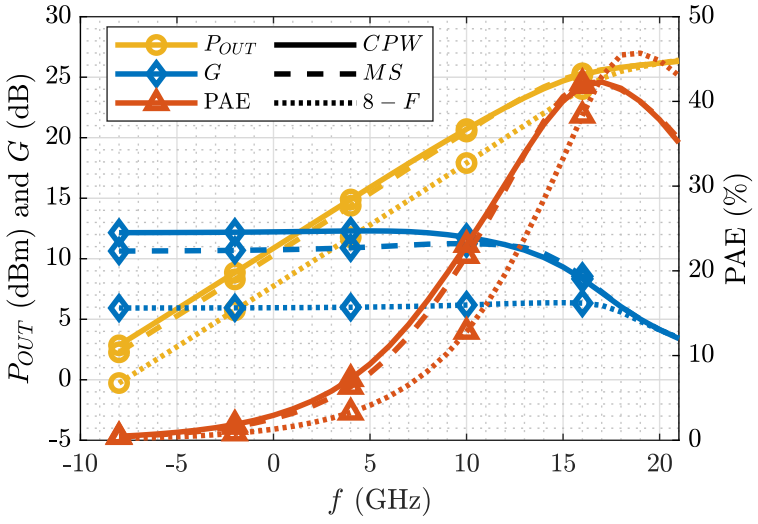
$$EANL1 = Error_{avr\ norm\ L1} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\frac{\left|S_{ijA}-S_{ijB}\right|}{0.5\left(\left|S_{ijA}\right|+\left|S_{ijB}\right|\right)}\right)}{N^2} \tag{5.2}$$

$$EAL1 = Error_{avr\ L1} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\left|S_{ijA}-S_{ijB}\right|\right)}{N^2} \tag{5.3}$$

$$EAL2 = Error_{avr\ L2} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{N}\left(\left|S_{ijA}-S_{ijB}\right|\right)^2}{N^2} \tag{5.4}$$

for the maximum L1 norm, average normalized L1 norm, average L1 norm and average L2 norm respectively.

Finally, the large-signal comparison is shown in Fig. 5.5. Here the output power, PAE and gain of the transistors under ideal terminations at both input and output are plotted. The "microstrip" and "CPW" models follow similar trends with the biggest difference being the gain before compression.



(a)

Figure 5.5: Large-signal comparison of different device models.

5.1.2 Stability

The CPW model is selected and the next step is incorporating the stability tanks and odd mode resistors to the device manifolds. Fig. 5.6a shows the final "device" with stability networks incorporated. Small signal stability is analyzed and the transistor RC stability tanks are designed accordingly to ensure in band unconditional stability while keeping the gain as high as possible. Fig. 5.6 shows the stability plots. Since this is a single-stage amplifier, K-factor analysis is appropriate and results are a good estimation of the device stability in the conditions where the model is accurate. Low frequency stability is addressed in the biasing lines and can be additionally enforced with off chip capacitors. The maximum available gain (MAG) and maximum stable gain (MSG) are also plotted and carefully monitored.

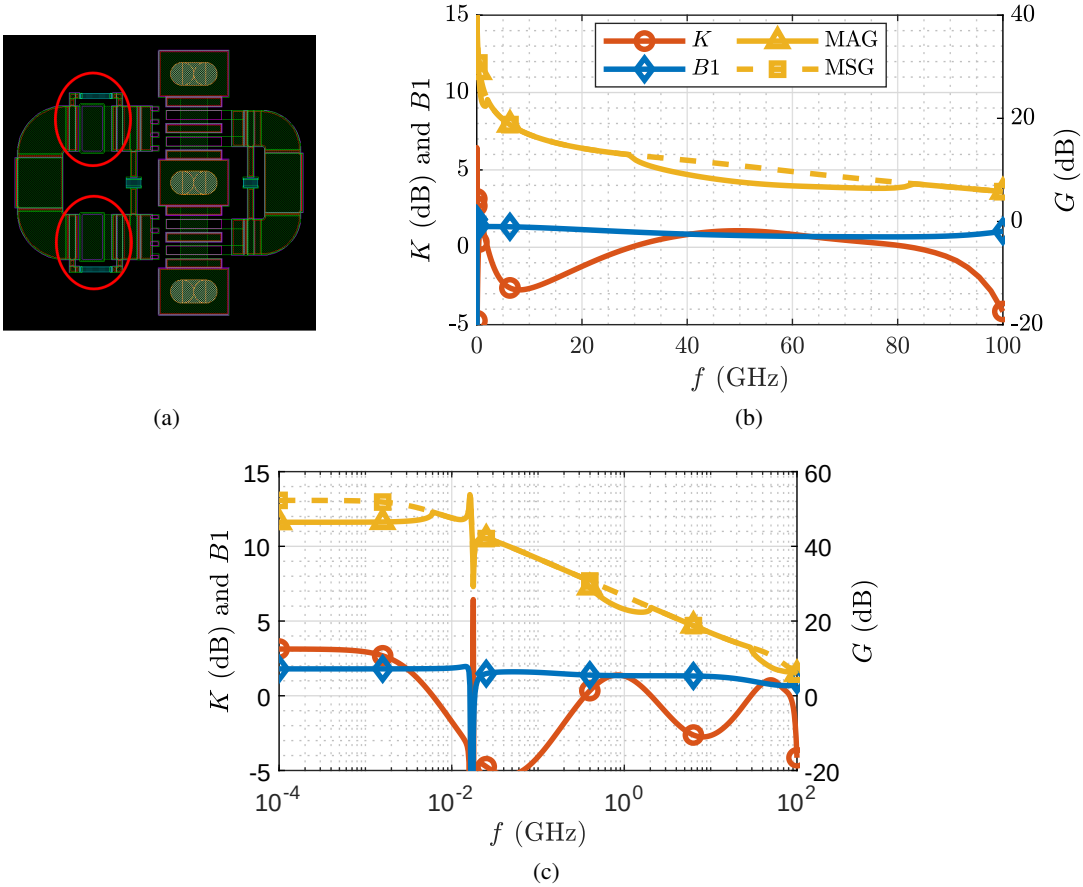
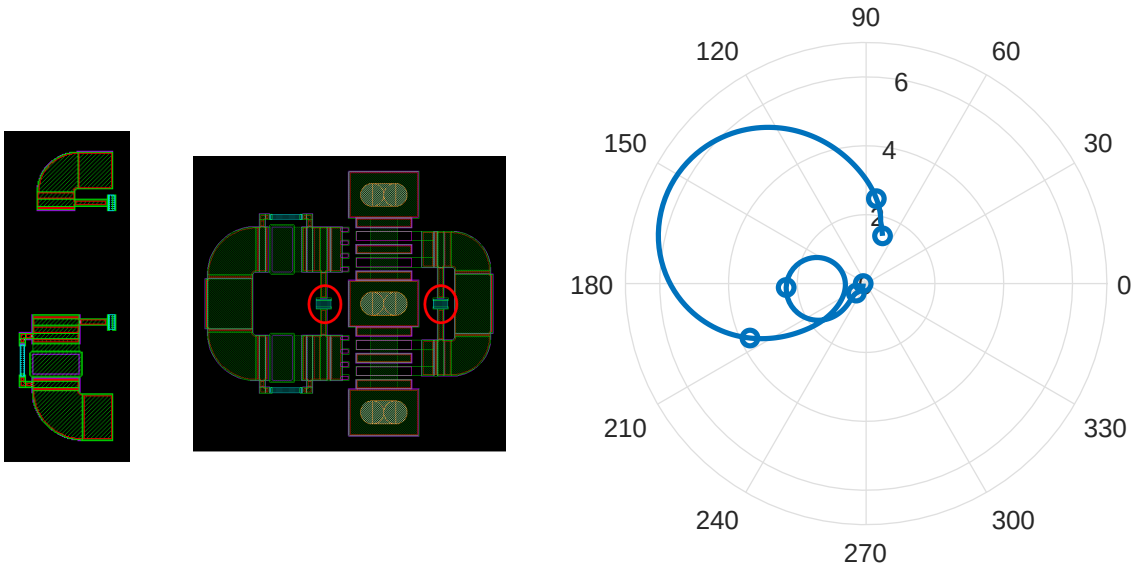


Figure 5.6: Small signal in-band stabilization of transistor. (a) Transistor layout with the RC stability tanks circled, (b) linear stability plots and (c) logarithmic stability plots for low frequency detail.

Odd mode stability is investigated by means of loop gain analysis, Fig. 5.7. For this the manifold from Fig. 5.6a is split in two through the symmetry plane as shown in Fig. 5.7a. Two odd mode resistors, Fig. 5.7b, are added at the gate and drain manifolds, to suppress any odd mode signal being excited. The loop gain locus is shown in Fig. 5.7c.



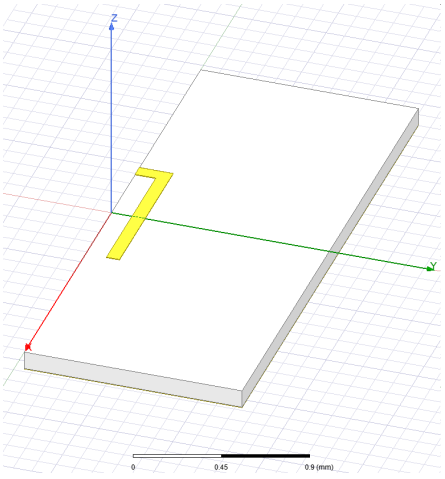
(a) (b) (c)

Figure 5.7: Odd mode stability analysis of the device. (a) Manifold split in half, (b) transistor layout with the odd mode resistors circled and (c) loop gain plot.

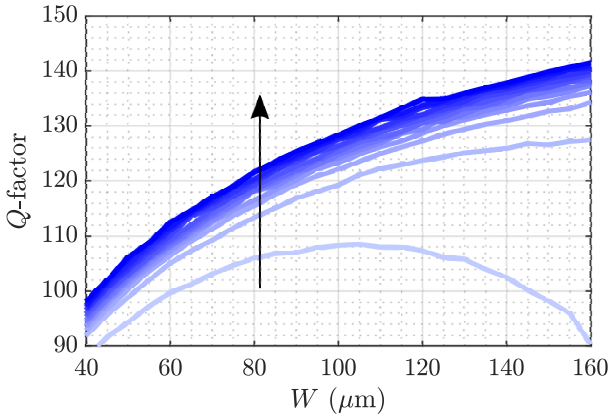
5.1.3 Matching Networks Design

After stabilizing the transistor, load-pull is performed to obtain the optimum impedances to present to the gate and drain of the device at the fundamental and harmonic frequencies for maximum PAE. The input matching network (IMN) is implemented with a simple and compact coupled-line section, providing a dc block [85], and additional out of band rejection since this is a resonant network itself. The output matching filter (OMF) is designed using the theory presented above with the same coupling matrix as given in Eq. (2.30), resulting in a 2^{nd} order Chebyshev filter with RL =15 dB. The center frequency of this filter is 28 GHz and the fractional bandwidth is 5 %. The resonators in the OMF are designed for high Q-factor using thick metal layers and varying resonator dimensions within the allowed MMIC process range. Careful choice of widths of the resonator lines (W) and coupling section lengths (x) minimizes the insertion loss and results in

high efficiency and output power. Fig. 5.8 shows the model and the simulation results. It can be seen that larger widths and larger coupling section widths tend to produce higher quality factors.



(a)



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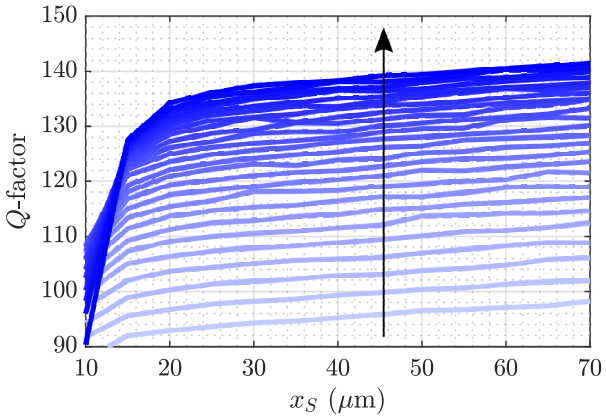
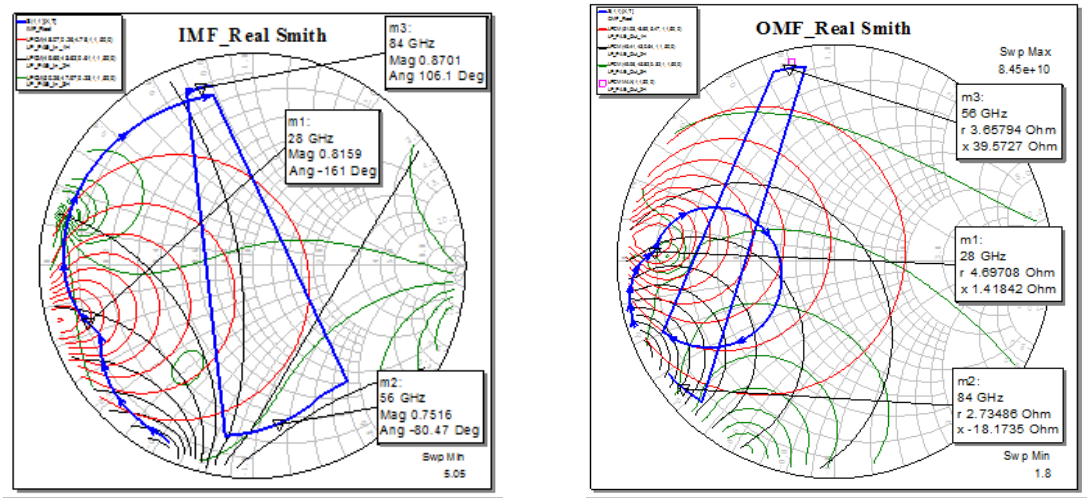


(c)

Figure 5.8: Resonator eigenmode simulations for optimizing quality factor. (a) Resonator model, only half of the geometry since the fundamental mode presents field symmetry, (b) quality factor as a function of resonator width for various coupling section lengths, arrow in the direction of growing x_S, and (c) quality factor as a function of resonator coupling section length for various widths, arrow in the direction of growing W.

The coupled-resonator OMF provides a dc block for the drain bias. The RF choke and harmonic terminations are also co-designed following the concept from Chapter 4 (Fig. 4.2) and with a grounded capacitor shorted stub at the operating frequency, as in the case of the hybrid FPA, details in the next subsection. Fig. 5.1b shows the layout and highlights the IMN, OMF and output biasing/harmonic terminations. Fig. 5.9

shows the load and source pull contours overlaid with the matching networks frequency responses.



(a) (b)

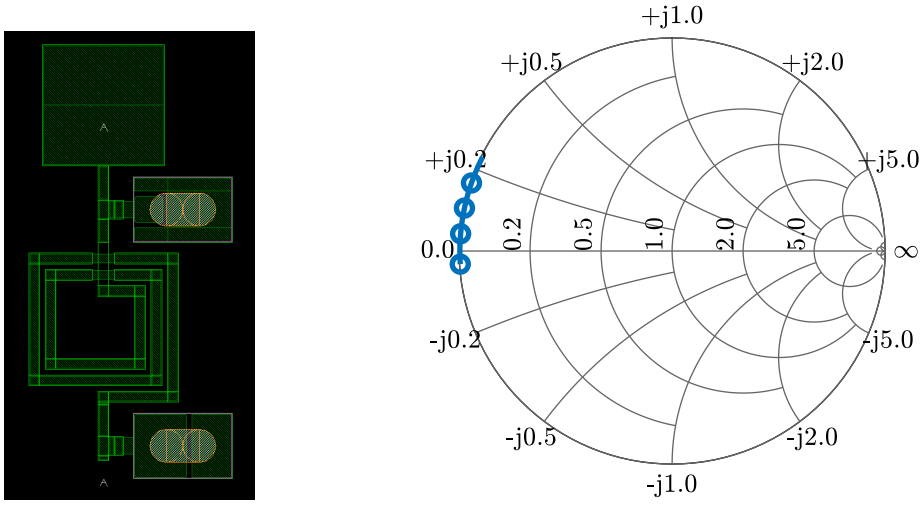
Figure 5.9: Load- and source-pull contours and frequency responses plotted on Smith charts for (a) input and (b) output.

5.1.4 Biasing Design

The biasing and harmonic terminations for both input and output are realized using a CLC network shown in Fig. 5.10. The network is designed to present a well known impedance to the transistor that is independent from what is connected to the feeding line, by presenting a known short at the fundamental and second harmonic of the operating frequency. After that the biasing network is designed by selecting the length and width of the line that connects the CLC network and the transistor. The goal is to present an open at the fundamental (the filter takes care of the impedance) and appropriate reactive termination at the second harmonic.

5.2 Simulation and Measurement Results

The MMIC FPA is measured on-wafer with a two-tier coaxial power and *S*-parameter calibration, followed by an SOLT on-wafer calibration using a PNA E8364C microwave network analyzer with an automated high power measurement setup based on [80], example B. Fig. 5.11 displays the simulated and measured *S*-



(a) (b)

Figure 5.10: CLC (capacitor-inductor-capacitor) designed to present a very controlled impedance at the fundamental and second harmonic of the operating frequency, showing (a) layout and (b) impedance looking into the CLC network while sweeping the impedance seen from the DC side, plotted from 25 to 60 GHz. The impedance magnitude is swept from 0.05 to 0.95 in steps of 0.1 and the phase from -180° to 180° in steps of 30°.

parameters of the amplifier presenting good agreement. It is worth noting that although the IMF is presenting the appropriate impedance to the transistor output for maximizing PAE, this is not a conjugate match and results in $|S_{22}| < -15$ dB not being met across the whole band. A 400 MHz (<1.5 %) frequency shift in S_{11} affects the gain at the lower end of the band as well.

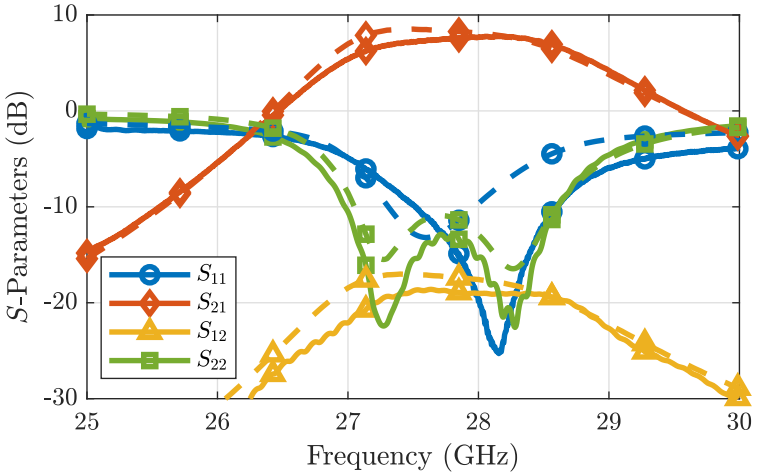


Figure 5.11: Measured (solid) and simulated (dashed) S-parameters of the MMIC FPA from Fig. 5.1. All measured parameters track the simulated ones very closely.

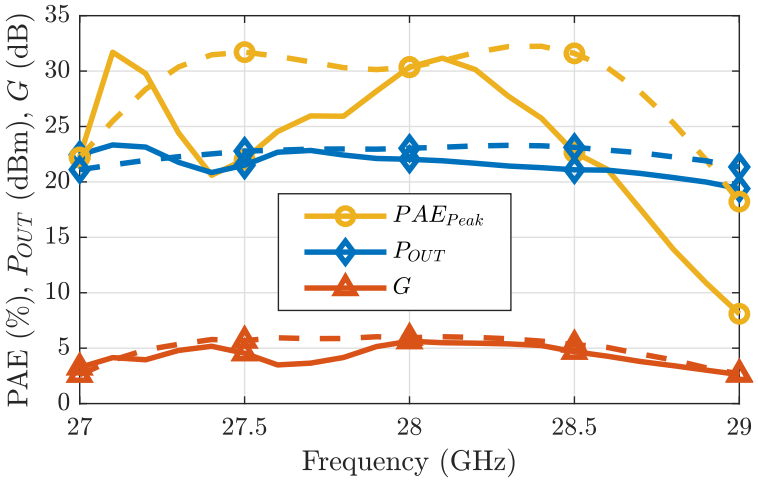


Figure 5.12: MMIC FPA large-signal simulations and measurements as a function of frequency, where the dashed traces represent simulations. All traces are plotted at the point of peak PAE.

Fig. 5.12 presents the measured and simulated large signal performance of the MMIC FPA, once again showing agreement between measurement and simulation. The efficiency, output power and gain are all given at the peak efficiency point for all frequencies. The decrease in measured large-signal gain compared to simulations from Fig. 5.12 of about 2 dB near 27.6 GHz, points to a possible decrease in PAE in large-signal operation. This is seen in the measurements in Fig. 5.12, where there is a dip in PAE around 27 GHz. This is likely due to a frequency shift in the response as well as the sub-optimal thermal environment, as the MMIC was measured directly on the chuck of the probe station without additional thermal management which in turn typically reduces the gain. Lastly, the gain and PAE vs. output power measured at three different frequencies can be seen in Fig. 5.13.

5.3 Chapter Summary

This chapter shows the design of a 28 GHz GaAs MMIC-FPA following the design method outlined in Chapter 4 for co-design of filters and amplifiers. The design works in the millimeter-wave 5G band (28 FR2) and the measured performance shows a gain of 8 dB, 200 mW of output power and PAE=30 % with a rejection of 8 dB at 26.5 and 29.6 GHz. The work presented in this Chapter demonstrates the first MMIC integrated FPA and the highest frequency implementation. The contributions are published in [38].

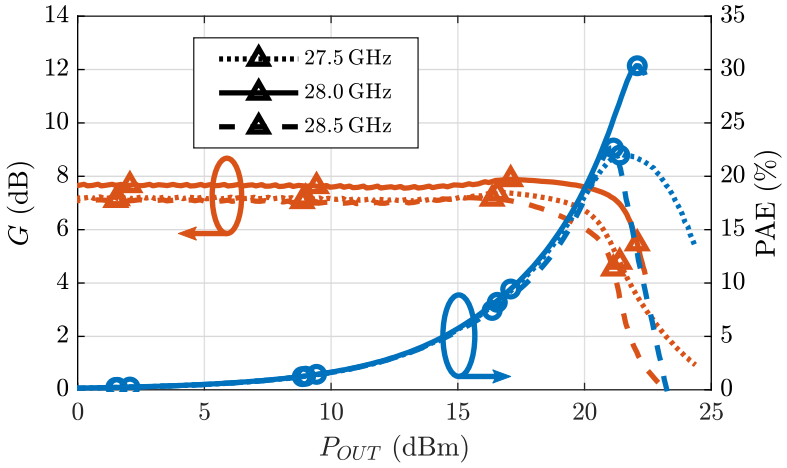


Figure 5.13: Measured PAE as a function of P_{OUT} for the GaAs MMIC FPA at three different frequencies in the band of operation.

Implementing the FPA using heterogeneous integration could result in further miniaturization and reduced loss. The next Chapter introduces a method for heterogeneous integration that can be used to further integrate front end components while gaining design tools and improving performance.

Chapter 6

Miniaturized Heterogeneously Integrated Front-Ends

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6.6 Chapter Summary 84

The Metal Embedded Chip Assembly (MECA) process, formerly Integrated Thermal Array Plate (ITAP) [86, 87], from HRL is a technique for heterogeneous integration that provides an excellent thermal and RF grounding. Fig. 1.8 shows an example MECA cross section and a photograph of a portion of an implemented module. The approach integrates various chips into a copper heat spreader block within the thickness of a silicon interposer wafer. The minimum demonstrated distance between the chips in the process is 70 μm, with a possibility of reduction to 30 μm through further process optimization. An intimate contact between

the backside of the chips and the heat spreader, with no thermal interface materials (TIM), improves the thermal management compared to traditional technologies. This intimate contact is achieved by directly growing the copper on the bottom side of the chips. A lithography-based interconnect layer replaces the traditionally used wirebonds, resulting in enhanced interconnect performance.

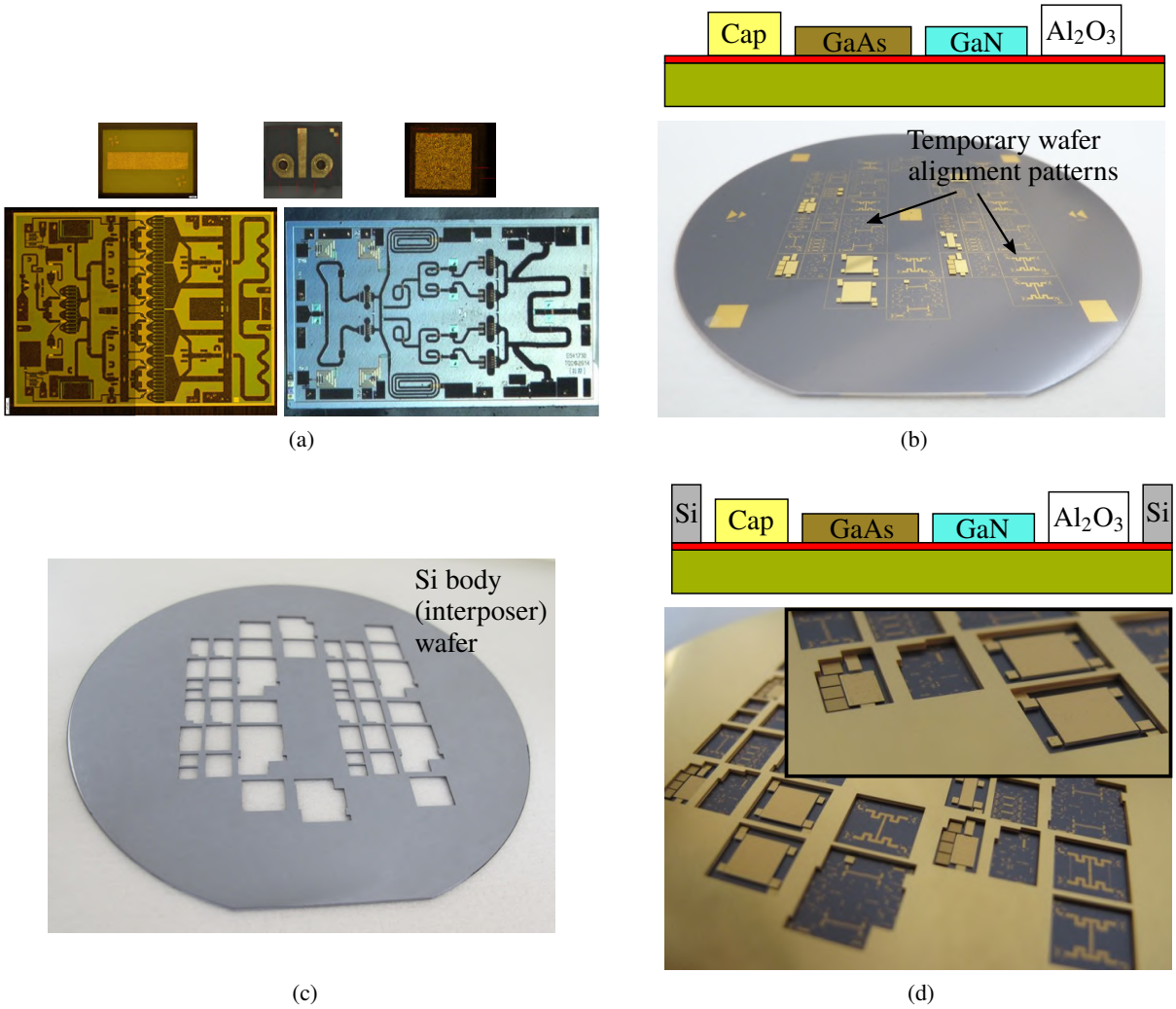
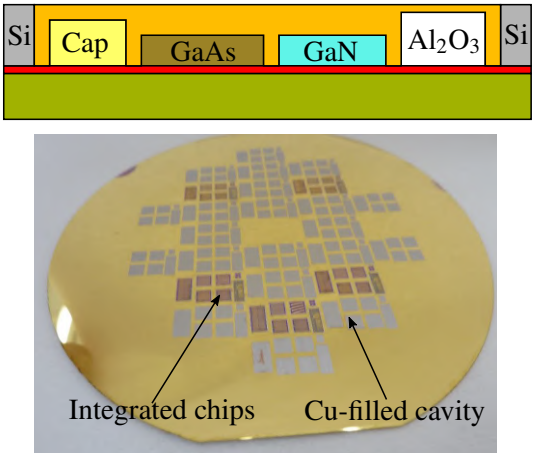


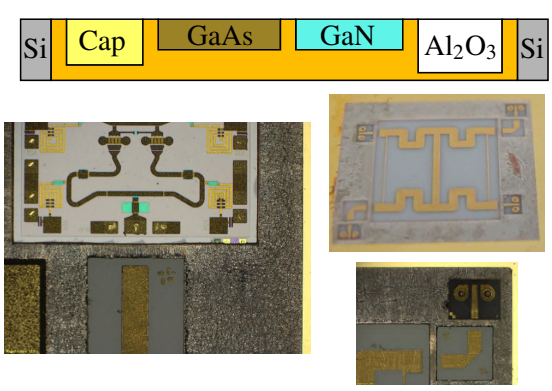
Figure 6.1: High-level illustration of the Metal Embedded Chip Assembly (MECA) process flow. (a) Chips of diverse technologies. (b) Face-down placement and bonding of chips on a temporary carrier wafer. (c) Metalized interposer Si wafer with etched cavities. (d) Assembled chips and temporary wafer with the interposer wafer.

6.1 Process: Metal Embedded Chip Assembly

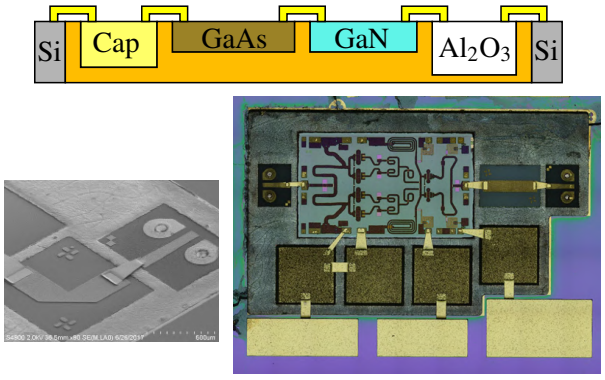
The first part of the MECA process is illustrated in Fig. 6.1, which describes the pre-processing steps required for copper plating that enables an outstanding thermal and electrical ground connection. Various chips, shown in Fig. 6.1a, are mounted face-down on a temporary carrier wafer. Fig. 6.1b shows several temporarily bonded circuits (alumina, GaN MMICs and ceramic capacitors), as well as some alignment marks used for chip placement. In parallel, a silicon interposer wafer is etched, Fig. 6.1c, allowing for a number of different heterogeneous modules to be fabricated simultaneously in the various Si cavities. The interposer (body) wafer is then bonded to the temporary carrier wafer, as illustrated in Fig. 6.1d.



(a)



(b)



(c)

Figure 6.2: Continuing from Fig. 6.1d. (a) The copper heat spreader is electroformed into the cavities. (b) MECA wafer released from the temporary carrier wafer and flipped. (c) Finally, single-layer air-bridge Au MECA interconnects for chip-to-chip, chip-to-body, and intra-chip electrical connections are fabricated.

At this point in the process, the cavities and ground planes of the individual circuits are prepared for copper plating which will provide the common thermal and electrical ground. The copper heat spreader is then electroformed into the cavities as shown in Fig. 6.2a and the MECA wafer is released from the temporary carrier wafer, Fig. 6.2b, and flipped. Finally, single-layer air-bridge gold MECA interconnects for chip-to-chip, chip-to-interposer, and intra-chip are fabricated, resulting in the heterogeneously integrated module displayed in Fig. 6.2c.

6.2 Photolithographically Defined MECA Interconnects

The most common interconnects between chips and packages are wirebonds. Gold wirebonds are used at high frequencies for interconnecting microwave transistors and MMICs to passive circuits, with typical diameters of 0.75, 1 and 2 mils (19, 25.4 and 50.8 μm), depending on operating frequency and required current density (power handling). The impedance due to the self and mutual inductance of multiple wirebonds needs to be taken into account in circuit design [88, 89] and limits the performance at high frequencies [90]. Due to the three dimensional nature and limited tolerances of bonding machines it is difficult to accurately predict wirebond behavior at high frequencies. MECA interconnects allow the placement of precisely controlled bridge interconnects that can be designed to maximize the matching between the two components and this comes at no added cost. Fig. 6.3 shows the geometry of the typical MECA interconnect.

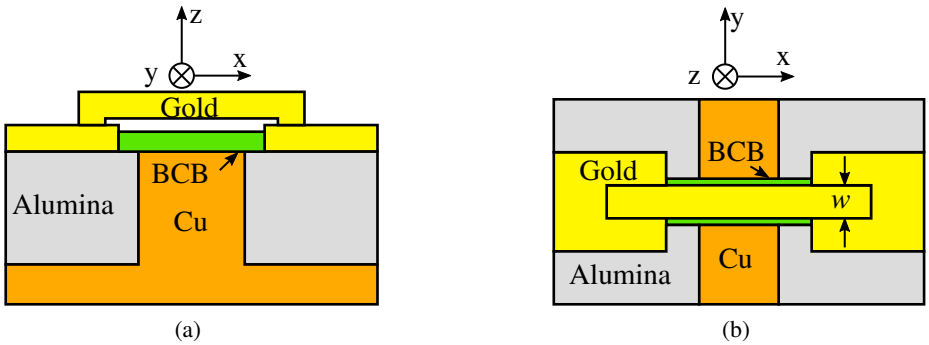
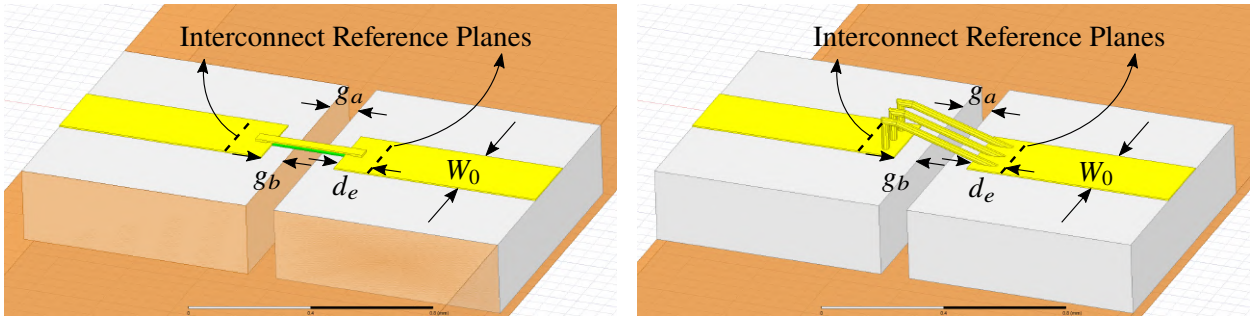


Figure 6.3: (a) Side and (b) top views of the interconnect geometry showing the different materials (not to scale). For this work, a 254 μm alumina substrate is used with 3 μm thick BCB layer, 5 μm air gap and 5 μm gold thickness for both microstrip lines and bridges.

The interconnects are fabricated using conventional photolithography to deposit a stackup of benzocyclobutene (BCB), air (through a sacrificial material) and gold as indicated in Fig. 6.3.

6.2.1 Performance

The simulation model geometries used to evaluate and compare several MECA interconnects and wirebonds can be seen in Fig. 6.4. Simulations were performed using Ansys HFSS (full-wave 3D electromagnetic simulation utilizing Finite Elements Method). These simulations show the interconnect performance between two 50 Ω microstrip transmission lines typically found in MMICs and microwave integrated passive devices (IPD).



(a) (b)

Figure 6.4: Interconnect geometries used in simulations. The ports are deembedded to the interconnect plane which is d_e = 130 μm away from the strip edge. The widths (W_0) of the microstrip lines are 254 μm (50 Ω lines). The width of the MECA interconnect is w and the wirebond has standard dimensions: 25.4 μm diameter, 100 μm height and 360 μm bridged distance. (a) MECA interconnect, (b) wirebond.

Fig. 6.5 shows the simulated performance. It can be seen that the all the MECA interconnects outperform wirebonds, with dimensions given in Fig. 6.4, at all simulated frequencies. MECA interconnects can also be designed to resonate in a particular bandwidth with improved performance. In Fig. 6.5 it can be discerned that for interconnect widths of 20, 30, 40 and 50 μm the return losses are distinctly minimal for a 360 μm long bridge near 97, 76, 48 and 23 GHz, respectively.

Fig. 6.6 presents the S-parameters of the interconnects as a function of width at different frequencies. It is readily apparent that there is an optimum width for matching in a particular frequency band and for a particular length. The interconnect can be thought of as a microstrip line in a multi-layered substrate that

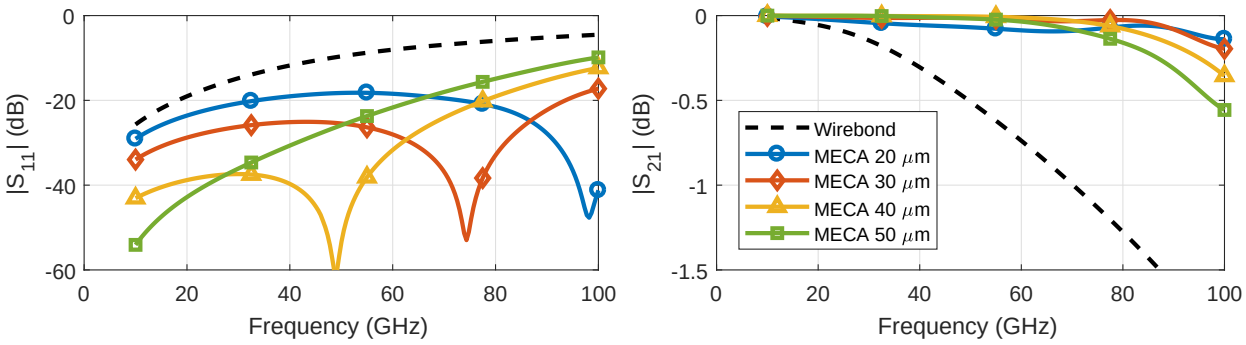


Figure 6.5: Simulated frequency response for the S-parameter magnitudes of the MECA interconnects for different interconnect widths with a standard wirebond shown for comparison, as shown in Fig. 6.4. (a) Matching magnitude $|S_{11}|$ and (b) transmission magnitude $|S_{21}|$.

is much thinner than the chips being interconnected. The optimum interconnect width is small compared to the traces on the substrates. That is because the ground of the interconnect is very close to the bridge and therefore the capacitance per unit length of that line is large compared to the traces on the chips, while the inductance per unit length has a comparable magnitude. Interconnects can also be tapered to improve matching over larger bandwidths at high frequencies.

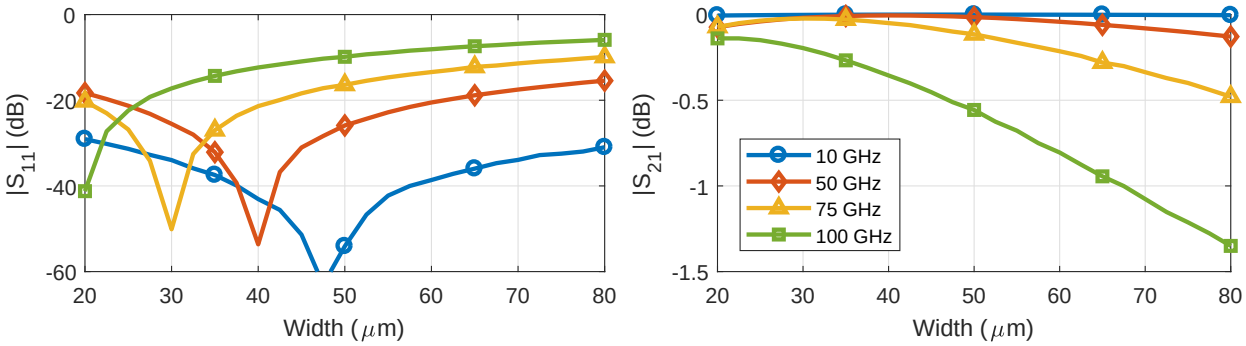


Figure 6.6: Plots of the S-parameter magnitudes for the MECA interconnects vs. width simulated at different frequencies, where the interconnect length is kept at 360 μm. (a) Matching magnitude $|S_{11}|$ and (b) transmission magnitude $|S_{21}|$.

6.2.2 Power Handling

MECA interconnects can handle larger power levels than gold wirebonds. In both cases the maximum current density is about 1 mA/μm^2 which accounts for the joule heating, electromigration and slow diffusion effects. Direct current (dc) interconnects can be designed to have the same cross-section as a wirebond by using an equivalent width of

$$w = \frac{\pi d^2}{4 h_{gold}} \tag{6.1}$$

where d is the wirebond diameter and h_{gold} is the gold thickness of the MECA interconnect. For a 25.4 μm diameter wirebond the equivalent MECA width is $w = 101\,\mu$m. At higher frequencies the skin depth of gold is smaller than 1 μm (e.g. the skin depth for gold at X-band is smaller than 0.9 μm) and the cross-section perimeter becomes the dominant parameter. The line width that provides the same perimeter as a wirebond is

$$w = \frac{\pi d}{2} - h_{gold} \tag{6.2}$$

and for 25.4 μm wirebonds this width is $w = 35\,\mu$m. Therefore a 40 μm wide MECA interconnect can handle more current than a 25.4 μm diameter wirebond.

Breakdown in MECA interconnects is dominated by the air gap which has a 100 times smaller dielectric strength than the BCB, as well as a lower relative permittivity and therefore less field intensity. Assuming a homogeneous field distribution across the micro-scale (5 μm) air gap and using a breakdown field strength of 20 MV/m [91], the breakdown voltage is estimated to be 100 V. Full-wave field simulations show that for a 50 Ω interconnect the error introduced by assuming a homogeneous field distribution is within 6 % and therefore negligible. The breakdown voltage is more than three times larger than the typical 20-30 V used for biasing GaN transistors. Those 100 V correspond to 100 W in a 50 Ω interconnect assuming low frequnecy excitation. For higher frequencies the power handling in terms of breakdown will exceed this value given the higher breakdown voltage for RF [92] signals. For higher power designs, the interconnect process may be modified to increase current handling and breakdown voltage even further, one way would be to eliminate the air layer of the interconnect and replace it with a dielectric layer with larger dielectric strength.

6.2.3 Wirebonds in the MECA Process

Some off-the-shelf MMICs are designed for wirebond interconnects and these can also be included in a heterogeneously integrated module. The case where MECA and wirebonds coexist is examined and the quality of the wirebonds is considered. MECA processing improves the matching of wirebond interconnects, due to increased proximity of the ground plane to the wire which in turn increases the wire-to-ground capacitance and decreases the interconnect characteristic impedance. Additionally, when chips of different heights are embedded in metal, their top surfaces are flush against the plated copper surface and require shorter wirebonds with lower inductance. Fig. 6.7 shows four different cases used for comparing the behavior of wirebond interconnects in chips that are embedded in metal with those that are traditionally mounted on a heatsink.

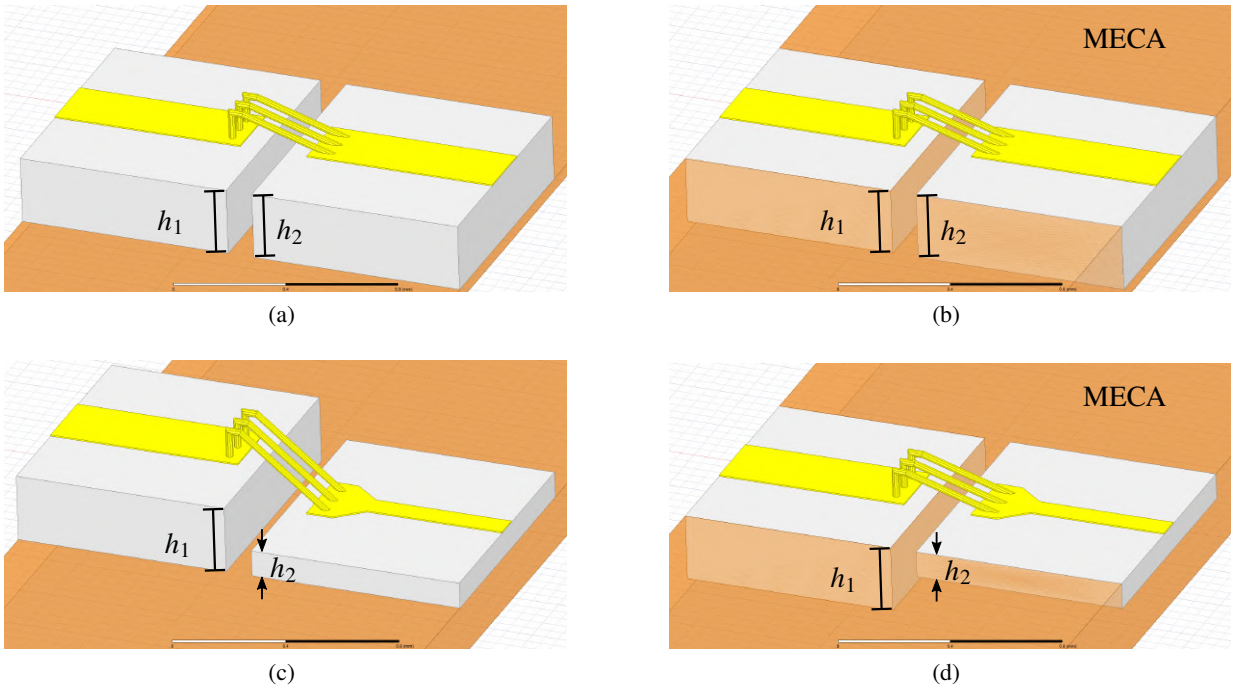


Figure 6.7: Four wirebond geometries with substrate heights of 254 and 100 μm. Wirebonds between two chips (a) of the same height ($h_1 = h_2$), (b) embedded in copper and of the same height, (c) of different heights ($h_1 > h_2$) and (d) of different heights and embedded in copper. The spacing between the two substrates is 360 μm for all cases.

The S-parameters of the interconnects shown in Fig. 6.7 are displayed in Fig. 6.8. It can be seen that, as

predicted, the wirebonds are better matched when used to interconnect metal embedded chips. The simulated frequency at which the insertion loss becomes larger than 0.5 dB for a standard wirebond increases from 51 to 87 GHz.

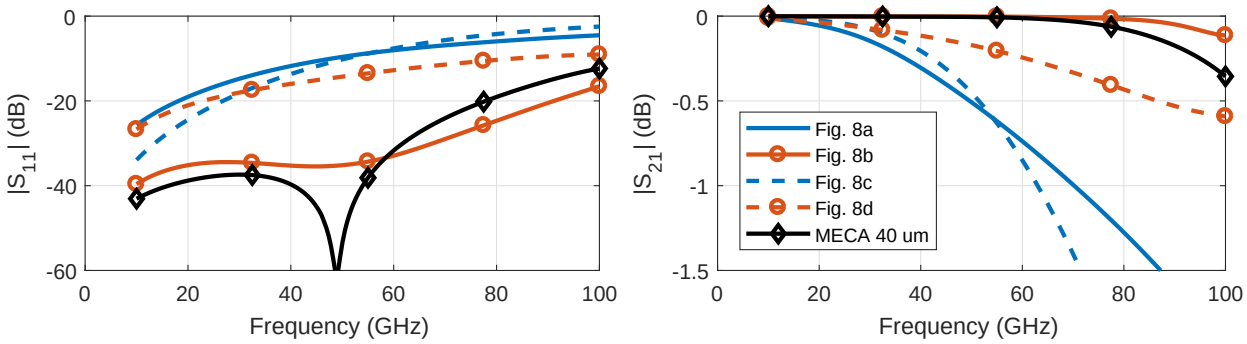


Figure 6.8: Plots of the wirebond S-parameters for the different configurations shown in Fig. 6.7 and a 40 μm wide MECA interconnect for comparison.

6.3 Bridge-Line Microstrip

The same processing steps used to form the chip-to-chip interconnects (Section 6.2) can be used to form inhomogeneous transmission lines on top of existing chips which in this work are referred to as a "bridge-line" microstrip, with cross-sections illustrated in Fig. 6.9.

The lines are simulated using Ansys HFSS to find the available characteristic impedances as a function of line width w. The simulation results for a given spacing between support posts $L = 220\,\mu$m and strip thickness of 5 μm is shown in Fig. 6.10 for a bridge-line with and without the BCB layer and compared to conventional microstrip on 254 μm thick alumina. Notice that higher impedances can be accomplished with the bridge-lines due to a decrease in capacitance per unit length [94], these higher impedance lines can be used to increase the design space for microwave components. The next section takes advantage of this.

The range of realizable impedances for a bridge-line and a microstrip are given in Table 6.1. Bridge-line microstrip can thus be used to increase the maximum realizable impedance from 108 Ω to 147 Ω (a 36 % increase) for the same line width.

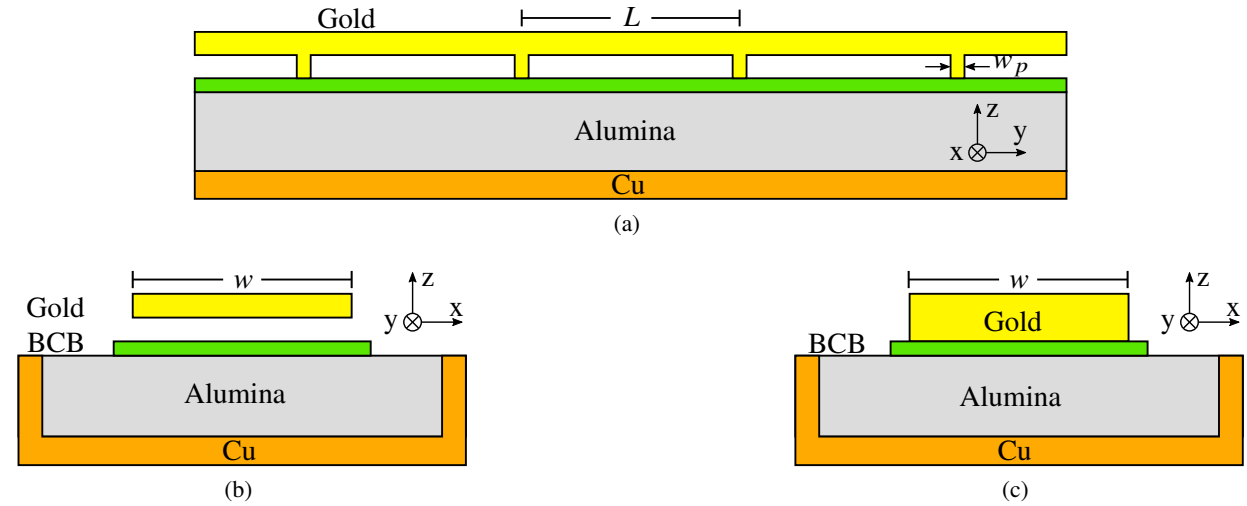


Figure 6.9: Bridge-line microstrip geometry (not to scale) after [93]. (a) side cross-section; (b) strip cross-section; and (c) post cross-section. w is the strip width and L is the length of one section measured between the centers of two adjacent posts. In this work, 254 μm alumina is used with 3 μm BCB, 5 μm air, 5 μm gold thickness. The post length is $w_p = 20\,\mu$m and $L = 220\,\mu$m.

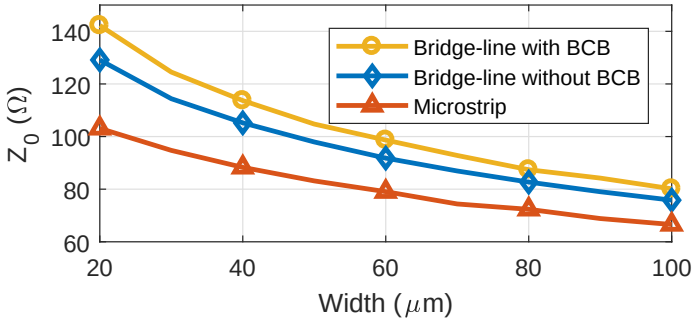


Figure 6.10: Characteristic impedance at 10 GHz as a function of line width for different microstrip geometries based on full-wave electromagnetic simulations.

Table 6.1: Realizable impedances with different microstrip widths based on full-wave electromagnetic simulations and Fig. 6.9.

Line type	$w = 400\,\mu$m	$w = 20\,\mu$m
Microstrip	38 Ω	108 Ω
Bridge-Line Microstrip	43 Ω	147 Ω

Since this is a non uniform transmission line it is important to understand the limitations in frequency where the line cannot be assumed to be uniform. The phase velocity of a transmission line is given by

$$v_p = \lambda_g f = \frac{L}{\tau}, \tag{6.3}$$

where λ_g is the guided wavelength, f is the frequency and τ is the group delay of the section. The frequencies where the length of this section is P % of the wavelength are given by

$$f = \frac{\left(\frac{P\lambda_g}{100}\right)}{\lambda_g \tau} = \frac{P}{100\tau}. \tag{6.4}$$

Full-wave electromagnetic simulations show that the group delay for one section of line is around $\tau = 2$ ps, resulting in $P = f_{\mathrm{GHz}}/5$. From here it can be seen that frequencies under 25 GHz have a section length that is smaller than 5 % of the guided wavelength and therefore the bridge-line behaves as a uniform distributed transmission line. Simulations also show that higher order and transverse modes limit the maximum operating frequency and appear at about 140 GHz, which is comparable to the cutoff frequency of a microstrip line on the same substrate [95].

The periodic posts that provide structural stability also increase the capacitance per unit length of the line therefore decreasing the characteristic impedance. For high characteristic impedances these posts should be made as small and far apart as possible. For example, the simulated characteristic impedance of a bridge-line with 254 μm thick alumina, 3 μm BCB, 5 μm air, 5 μm gold and line width of 330 μm decreases from 45 Ω to 43 Ω when the posts (20 μm post length and $L = 220\,\mu$m) are included.

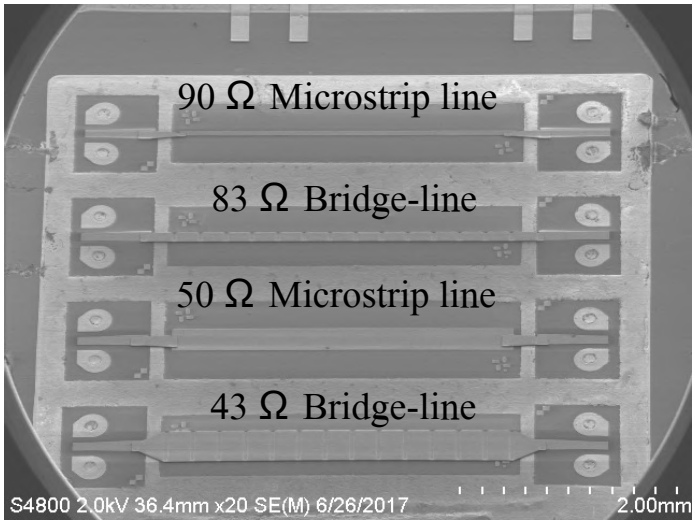
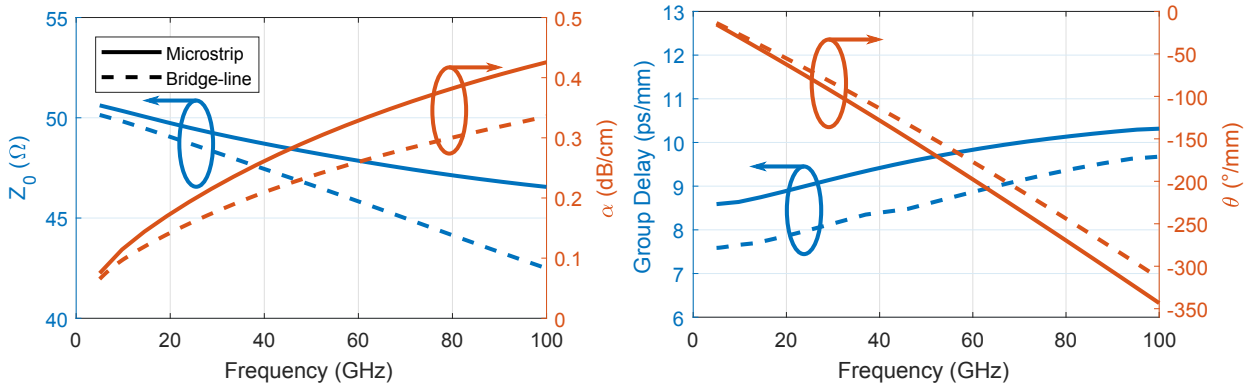


Figure 6.11: Photograph of the fabricated test transmission lines [93]. The second and fourth lines are bridge-line microstrips, the posts can be distinguished in this photo. The launchers are alumina ProbePoint™ 0503.

Bridge-lines are fabricated on alumina substrates, along with control microstrip lines for comparison and are shown in Fig. 6.11. The measured characteristic impedance, attenuation and group delay of the

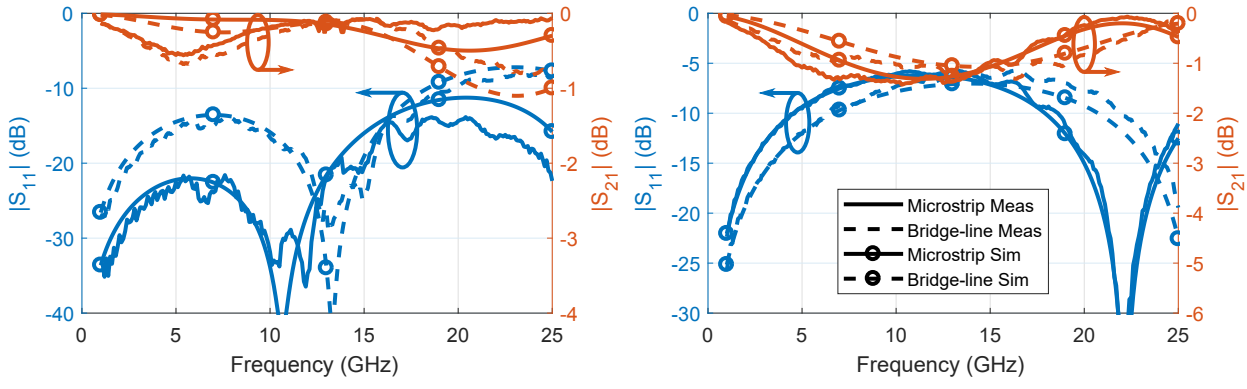
bridge-lines as a function of frequency are plotted in Fig. 6.12, along with plots for microstrip lines for comparison. Dispersion is similar in both bridge-lines and microstrip while the bridge-lines have lower loss. The bridge-line group delay is slightly smaller because of the smaller effective permittivity.



(a) (b)

Figure 6.12: Plots of the line parameters for one section of a bridge-line vs. frequency and compared to a conventional microstrip. (a) Characteristic impedance and attenuation constant and (b) group delay and phase angle.

Lines with 50 and 90 Ω characteristic impedances were designed to have respective widths of 350 and 116 μm. Due to the experimental nature of the MECA process, in this particular fabrication run the BCB layer was omitted, resulting in a reduction of bridge height from 8 to 5 μm. As a result, the line impedances



(a) (b)

Figure 6.13: S-parameter magnitudes of the (a) 43 − Ω line with $W = 240\,\mu$m for the microstrip and $W = 330\,\mu$m for the bridge line, and (b) 83 − Ω line with $W = 46\,\mu$m for the microstrip and $W = 96\,\mu$m for the bridge line. The rest of the parameters are the same as in Fig. 6.9. The measurements are calibrated with a Cascade Microtech 101-190 C impedance standard substrate and the launchers and interconnects are deembedded.

dropped from $Z_0 = 50\,\Omega$ to $43\,\Omega$ and from $Z_0 = 90\,\Omega$ to $83\,\Omega$. These bridge-lines have 12 sections with posts that are 5 μm tall. The removal of the BCB layer should not substantially affect the performance of the lines. Commercial alumina launchers (ProbePoint™ 0503) are included and interconnected to the bridge-lines by a tapered MECA interconnect and Fig. 6.13 shows a comparison of the measurement and simulation results. For these simulations the interconnects to the lines are also modeled and no BCB layer is used.

6.4 Hybrid Couplers

In this section two types of broadband quadrature hybrids are discussed, showcasing the usefulness of the MECA interconnects and bridge-lines for enhancing performance of microwave components and providing extra design flexibility. Lange couplers are limited in frequency by the gap between coupled lines and the air-bridge between coupled-line sections. Multi-section broadband branch-line couplers can be designed for higher frequencies, but are larger in size and are limited by the highest implementable characteristic impedance [96]. Here, bridge-lines fabricated in the interconnect step of MECA are used as an additional degree of freedom in the design of broadband couplers on alumina. Two X-band multi-section branch-line couplers are designed following the design procedure in [96]; one using high-impedance bridge-lines and the other employing entirely conventional microstrip lines on alumina for benchmarking. The fabricated couplers can be seen in Fig. 6.14.

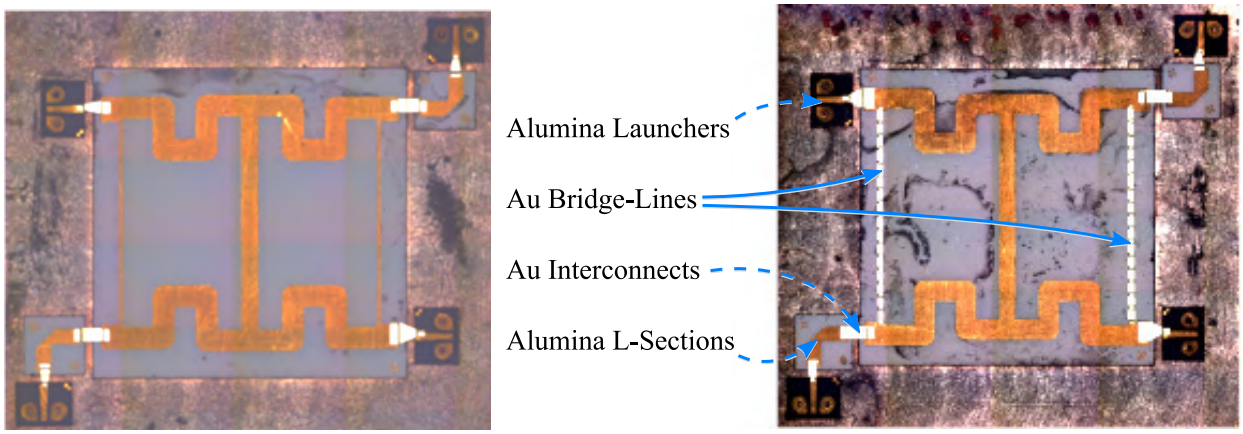
The measured and simulated results for the fabricated branch-line couplers are shown in Fig. 6.15, where the amplitude and phase balances are calculated as

$$|\Delta\,|S|| = ||S_{31}| - |S_{21}|| \tag{6.5}$$

$$\Delta\phi = \angle S_{31} - \angle S_{21} \tag{6.6}$$

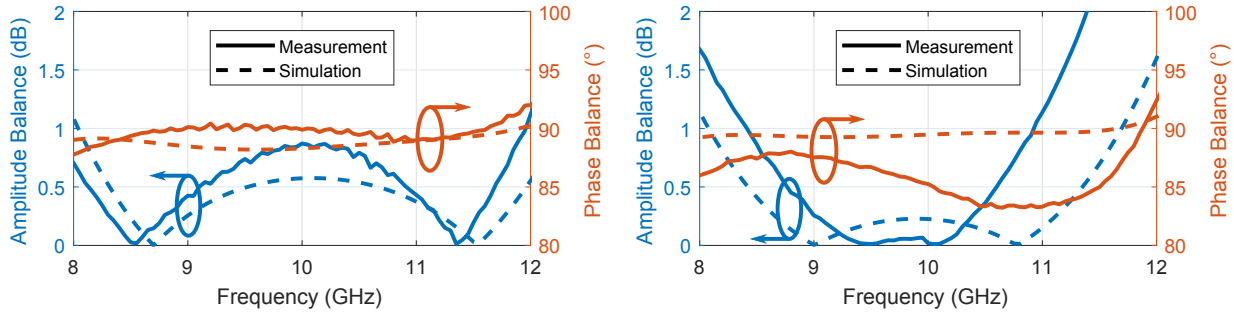
Table 6.2 summarizes their characteristics. The designs are equivalent but due to the omission of the BCB layer in this particular MECA run, the bridge-line design slightly under-performs the traditional one. Proper design for the appropriate materials stackup would yield identical performance.

Due to the experimental nature of the MECA process, in this particular fabrication run the BCB layer was omitted, resulting in a reduction of bridge height from 8 to 5 μm.



(a) (b)

Figure 6.14: Photograph of Alumina multi-section branch-line couplers integrated in the MECA process. (a) Traditional coupler for comparison and (b) coupler with high impedance exterior lines implemented using bridge-lines. The total length of the couplers is 5 mm. The launchers are alumina ProbePoint™ 0503. Alumina L-sections were used to enable 4-port on wafer probing of the couplers, these are deembedded in all the reported measurements.



(a) (b)

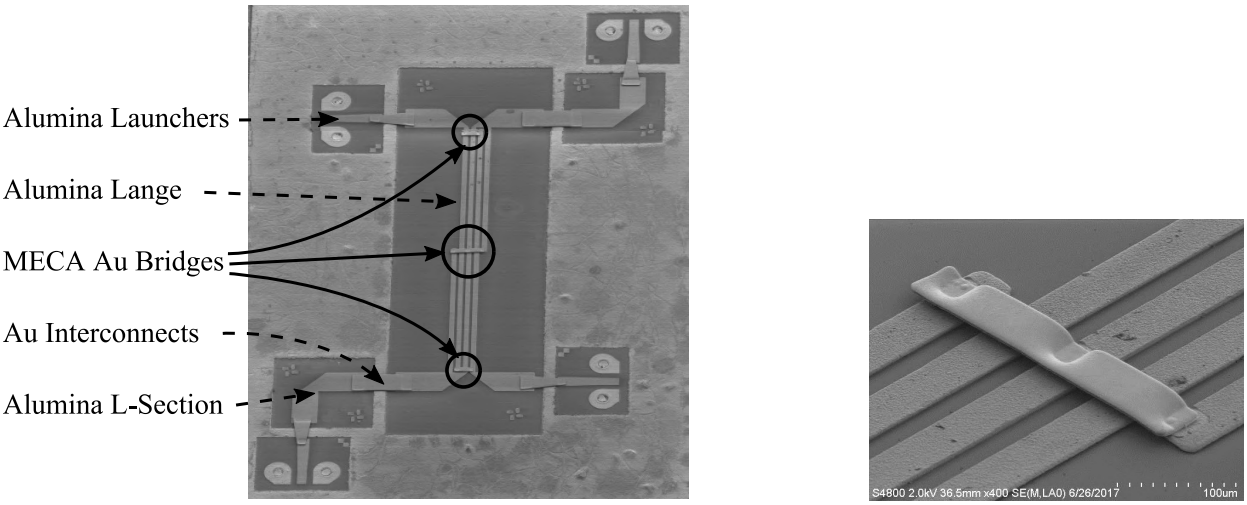
Figure 6.15: Multi-section branch-line coupler measurements for (a) a coupler fully implemented in microstrip and (b) a coupler with high-impedance lines implemented as bridge-lines.

Table 6.2: Measured bandwidth, return loss (RL), insertion loss (IL) and isolation (I) of the branch-guide couplers. The bandwidth is the range in which the amplitude balance is less than 1 dB.

Coupler	f_L (GHz)	f_H (GHz)	RL (dB)	IL (dB)	I (dB)
Microstrip	7.8	12.0	18	0.2	18.8
Bridge-Line	8.4	10.9	15	1.4	17.4

Another straightforward way to take advantage of the interconnect layer in the heterogeneous integration process is to use it for bridges in Lange couplers. The fabricated Lange coupler can be seen in Fig. 6.16 with

measured results shown in Fig. 6.17. The coupler has a frequency range from 7.9 to 11.8 GHz over which the amplitude balance is less than 1 dB and the phase balance is within 90.7 ° and 91.5 °. The insertion loss is 0.5 dB, return loss and isolation are both greater than 22.5 dB and 24.6 dB, respectively.



(a) (b)

Figure 6.16: (a) Photograph of the fabricated Lange coupler after [93] (total length 5 mm) and (b) zoom into bridge. The launchers are alumina ProbePoint™ 0503. Alumina L-sections were used to enable 4-port on wafer probing of the coupler, these are deembedded in all the shown measurements.

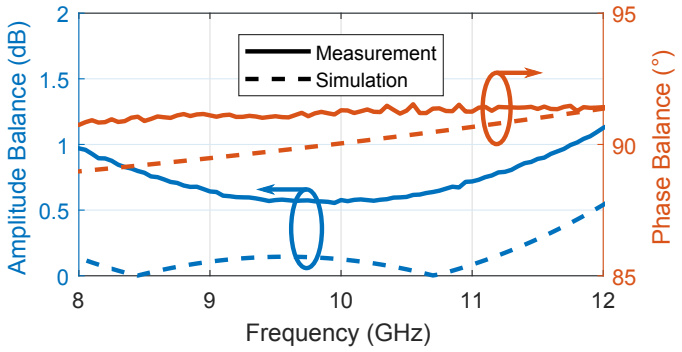
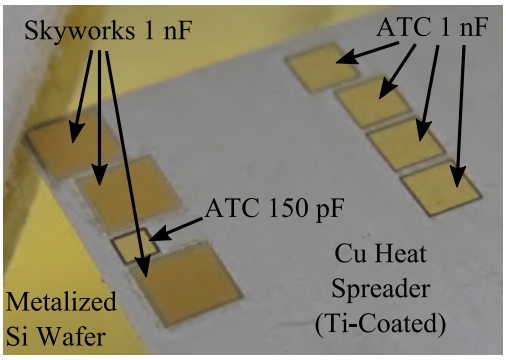


Figure 6.17: Lange coupler measurement results [93], displaying good agreement with simulations. RL = 22.5 dB, IL = 0.5 dB and I = 24.6 dB.

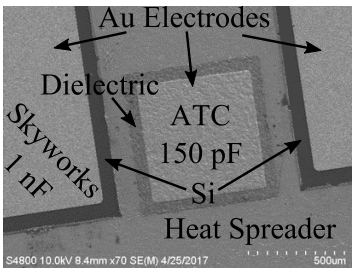
6.5 MMIC Power Amplifier Integration

In this section, an X-band power amplifier (PA) is integrated with off-chip capacitors and alumina passives. Off-chip capacitors are required in many circuits, e.g. in stabilization networks and bias lines of power

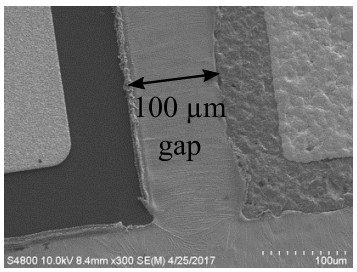
amplifiers. High dielectric constant capacitors can be integrated as off-chip capacitors using MECA. The top capacitor electrode is recessed from the edge while the bottom electrode is directly in contact with the heat spreader. The recessed top electrode avoids shorting of the top plate of the capacitor. Skyworks 1 nF low profile silicon metal-insulator-semiconductor (MIS) capacitors and ATC ceramic 150 and 1000 pF capacitors were integrated and tested in the MECA process as shown in Fig. 6.18. The MECA integrated capacitors were characterized at low frequency using an LCR meter (1-2000 kHz).



(a)



(b)



(c)

Figure 6.18: (a) Photograph showing the Skyworks 1 nF MIS capacitors (SC99906068), ATC ceramic 150 pF (118FGA151M100TT) and ATC ceramic 1 nF capacitors (118JL102M100TT) integrated in the MECA process. (b) Zoom into the ATC 150 pF capacitor showing the recessed electrodes and the dielectric. (c) Zoom into the gap between the capacitors.

For measurements, the capacitors were probed from the top and through the heat spreader. All three capacitor designs perform as expected and the results can be seen in Fig. 6.19, confirming that the MECA process is compatible with high dielectric constant ceramic and silicon-based MIS capacitors.

A two-stage GaN power amplifier MMIC [97] designed in Qorvo's 150 nm GaN on SiC process is used to test the MECA processing. This chip operates at X-Band (10 GHz), has a gain of 25 dB and peak power added efficiency (PAE) of 45%. The chip was characterized prior to going through the MECA process to

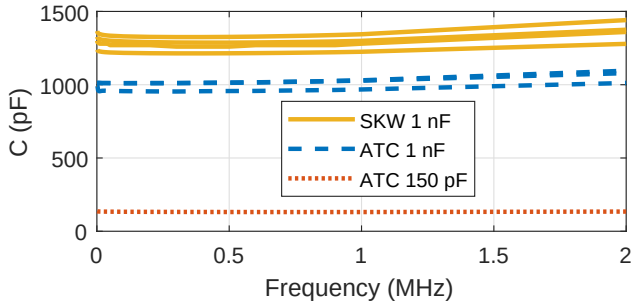
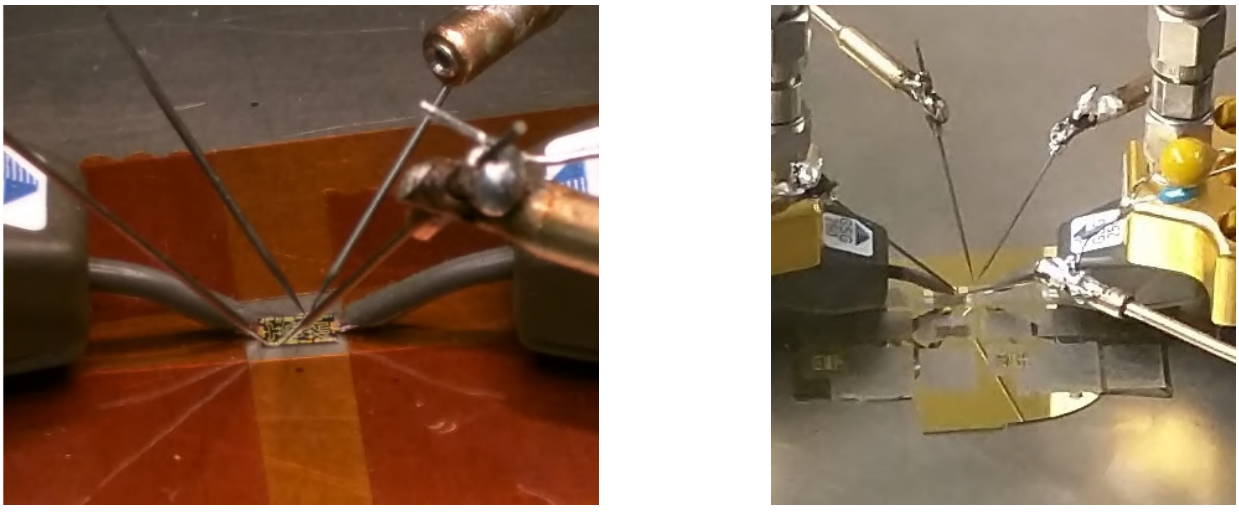


Figure 6.19: Low frequency measurements for the capacitors shown in Fig. 6.18(a).

determine the effects of processing and improved thermal operating conditions on MMIC performance. Fig. 6.20 shows the photos of the setup used to measure the MMIC before and after heterogeneous integration. In both cases the thermal contact to the ground of the die is made using vacuum on a Cascade Microtech Summit 9000TM probe station. A PNA E8364C microwave network analyzer is used with an automated high power measurement setup based on [80], example B. The MMICs are probed using Cascade Microtech ACP50 probes with 250 μm pitch and tungsten dc probes for biasing. Off-chip capacitors are also added to the setup to provide low frequency stability for the amplifiers. Additionally, a bare-die MMIC was measured alongside the MECA die to validate the measurement setup repeatability.



(a) (b)

Figure 6.20: Photos of the MMIC measurement setups: (a) before MECA and (b) after MECA integration.

Fig. 6.21a shows the gain and PAE comparison for the MMIC before and after being metal embedded.

Improvement in gain as well as in efficiency can be seen due to the improved thermal environment. The carrier mobility (and velocity) in the transistor is a function of temperature and it is higher at lower operating temperatures, this translates into increased device current and gain. The gain is increased by up to 3 dB, this has a positive impact in the PAE, as can be seen in eq. (4.1), which increases by up to 3.2 percentage points. Fig. 6.21b shows the driven drain currents for both stages of the MMIC PA, showing the reduction in dc power consumption that leads to the increased efficiency.

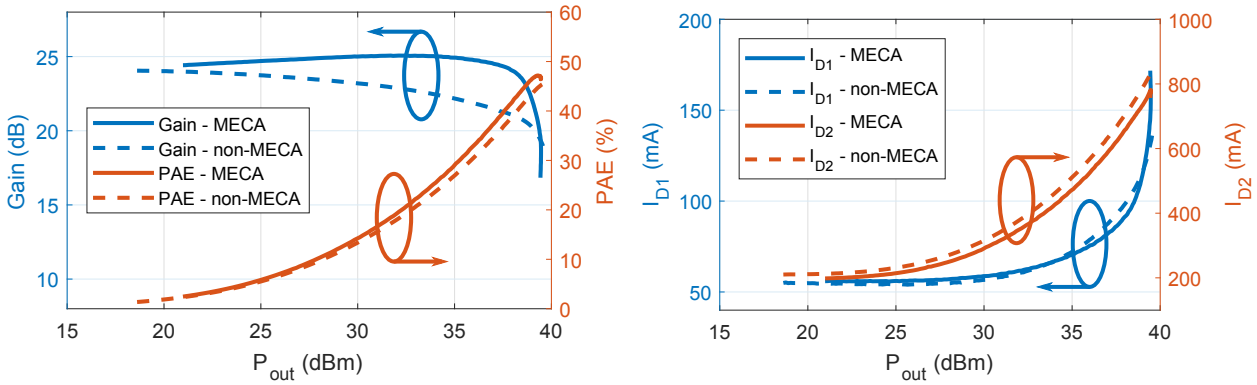


Figure 6.21: Measurement results of the integrated GaN MMIC PA system before and after heterogeneous integration. (a) Gain and PAE comparison and (b) driven drain currents for both stages.

6.6 Chapter Summary

In this Chapter the benefits of the metal-embedded chip assembly (MECA) heterogeneous integration technique for multi-chip modules are demonstrated. Measurements are shown for integrated alumina passives, surface mount capacitors and GaN MMICs connected with a unique interconnect network fabricated as the last step of the MECA process. The interconnect layer is shown to provide additional degrees of freedom for the design of microwave components.

Since MECA interconnects are photolithographically defined, their shape can be precisely controlled to provide enhanced return loss and transmission. The flexibility of interconnect shapes enables integration of MMICs that are designed to be wire-bonded, such as the ones demonstrated in this Chapter. Full-wave simulations show that they can be easily designed to out-perform wirebonds over a broad frequency range

(10 to 100 GHz). MECA interconnects are additionally useful as bridges within a single circuit such as a Lange coupler, demonstrated here on alumina at X-band.

The interconnect layer can also be used to implement transmission lines, referred to as bridge-lines, with reduced loss and higher possible characteristic impedances compared to traditional microstrips. A multi-section branch-line coupler incorporating bridge-lines of the interconnect layer combined with microstrip on alumina is implemented and characterized to demonstrate the additional design capabilities provided by the MECA process. A similar approach can be applied to a wide range of microwave components like filters, couplers, hybrids, matching networks, etc.

The benefits of the MECA interconnects come at no added cost for heterogeneously integrated RF front-end modules using the MECA process. In this Chapter, integration of power amplifiers, couplers, capacitors and launchers in the MECA process is also demonstrated. The improvement of thermal performance of PAs is shown by increased gain and efficiency for an X-band GaN MMIC. For MMICs designed with wirebond interconnects it is shown that these can be also integrated in the MECA process with improved wirebond performance allowing higher frequency operation. The current process is well suited for III-V chip integration with CMOS control chips, with a 10-μm wide 10-μm spaced interconnect process. For digital applications, a more advanced multi-layer and higher-resolution interconnect process is required.

In summary, the interconnect layer of the MECA process gives additional design parameters that can improve performance and footprint of passive components necessary in RF front ends while the intimate thermal contact of MECA improves the performance of the active circuitry. The components designed and measured in this Chapter can directly be used to implement a more complex circuit, e.g. an X-band balanced amplifier. The contributions from this Chapter are reported in [93] for the passives and then extended to actives in [98]. In the last Chapter, a MECA integrated FPA design is proposed as an example of how the results from Chapter 5 can be combined with those of this Chapter.

Part II

Integration of Rectifiers and Radiators

In this part, co-design and integration of wireless charging and harvesting is researched. A new method for reducing fringing fields in a capacitive wireless power transfer (CWPT) system using a near-field phased array with a multi-module approach is demonstrated. In the low-power regime, co-design of both narrowband and broadband rectifiers and antennas for harvesting ambient power for wireless devices is demonstrated. Harvesting power from airplane altimeter radar antenna sidebands with a rectifier-antenna (rectenna) for aircraft health monitoring sensors demonstrates the possibility of charging a storage device at low incident power levels. For wideband energy harvesting from unknown and variable sources, wearable rectenna arrays screen-printed on clothing are demonstrated for harvesting energy over more than an octave bandwidth in the sub-6GHz frequency range.

Chapter 7

Near Field Wireless Powering

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Electric vehicles (EV) are the most promising substitutes for internal combustion engine vehicles (ICEV). EVs have greater well-to-wheel efficiency than ICEVs and since their global market share remains under 1 % [99] there is a great necessity for innovation. Although advances are made in battery technology (particularly Lithium-ion) and charging systems [100, 101], many problems related to greater EV market penetration remain to be solved. One of the challenges is the short driving range of EVs compared to ICEVs. A typical ICEV has a range of about 500 km while a typical EV has on average about 150 km of range and the highest values are around 450 km for the higher-end EVs [102]. One of the possible solutions to this problem is wireless powering of the EV in motion on the road, which also reduces battery requirements. Power transfer on the order of 20 kW can be used to power an EV at cruising speeds and is usually the design

specification for these systems [103]. Additionally, wireless power transfer (WPT) is an attractive alternative for charging EVs in parking lots, garages and other static scenarios where a wireless system can prove to be more convenient and reliable. So far efforts have been made to demonstrate wireless power transfer to electric vehicles using inductive power transfer, e.g. [103, 104, 105], and a few limited cases of capacitive power transfer, as in [106, 107].

7.1 Capacitive Wireless Power Transfer

The goal of the work presented in this Chapter is to develop a capacitive wireless power transfer (CWPT) System that can provide 50 kW over a 12 cm gap using an area of less than 1 m^2 with an efficiency above 90%. Fig. 7.1 shows the overall geometry for Wireless Power Transfer (WPT) to an EV with a capacitive near field phased array.

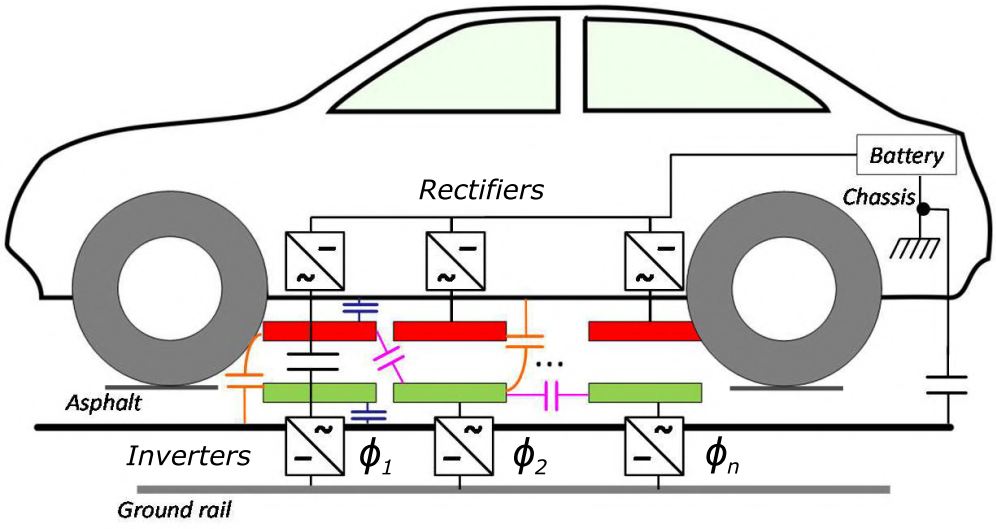


Figure 7.1: Overall geometry for capacitive wireless powering in electric vehicles, showing multiple phased CWPT modules that consist of a power inverter in the road, a pair of coupling capacitive plates, and a rectifier in the vehicle that charges the on-board battery. Parasitic capacitances from plates to chassis, plate to road-rail, chassis to road-rail and between adjacent plates are also shown.

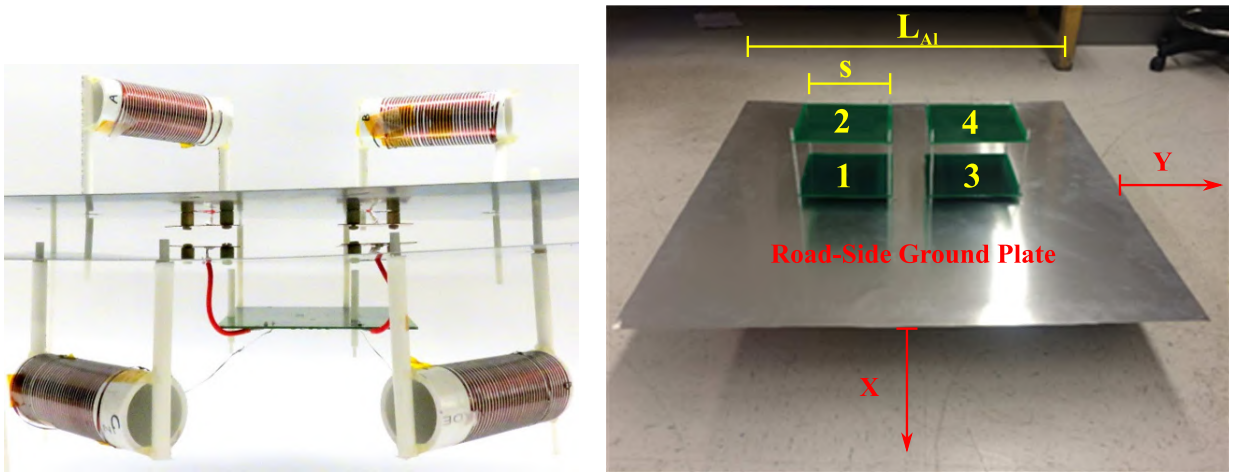
Approaches to fringing field reduction using near-field phased arrays of inductive have been attempted in the past [108, 109]. CWPT has several advantages over inductive WPT systems: (1) does not require the use of heavy and expensive ferrites for field concentration; (2) benefits from higher frequencies of operation

since the capacitive reactance between the vehicle and the road is inversely proportional to frequency; (3) the displacement current corresponding to high power transfer requires a lower electric field at higher frequencies; and (4) sensitivity to misalignment can be reduced using an appropriate geometry [106].

Due to the large electromagnetic fields that are associated with high power transfer, safety is an important issue that remains to be solved. Exposure limits like the ones found in [110] restrict the electromagnetic fields that humans can be exposed to, and these must be met for any product commercialization.

7.2 Single Module Design

A photograph of a single module in the CWPT system is shown in Fig. 7.2a, where the parallel plates used for WPT and the inductors that form the matching networks can be seen. In order to form a practical vehicle charging system, 'Road-Side" and "Vehicle" aluminum sheets are added above and below the coupling plates. Fig. 7.2b shows the system with the respective labels on each component, the top aluminum sheet has been removed for visibility. These sheets are used and accounted for in design and simulations of the system.



(a) (b)

Figure 7.2: Single module CWPT system photos. (a) Photo of the four capacitive plates along with the matching networks, and the 'Road-Side" and "vehicle" conducting sheets. (b) Photo of CWPT system with labels, the top aluminum sheet that models the vehicle has been removed for visibility. The side length of the aluminum sheet is L_{Al} =100 cm. The red arrows indicate the two measurement axis locations.

To simplify the analysis an equivalent circuit can be found that incorporates the parasitics of the WPT

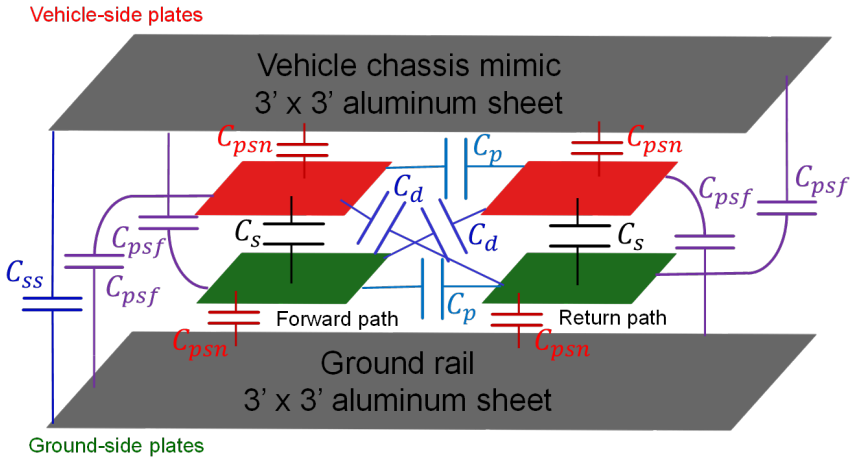
coupling parallel plates and the aluminum sheets. Fig. 7.3a explicitly shows the capacitances involved in the system, these capacitances can be simplified as

$$C_{s,eqv} = C_s - C_d \tag{7.1}$$

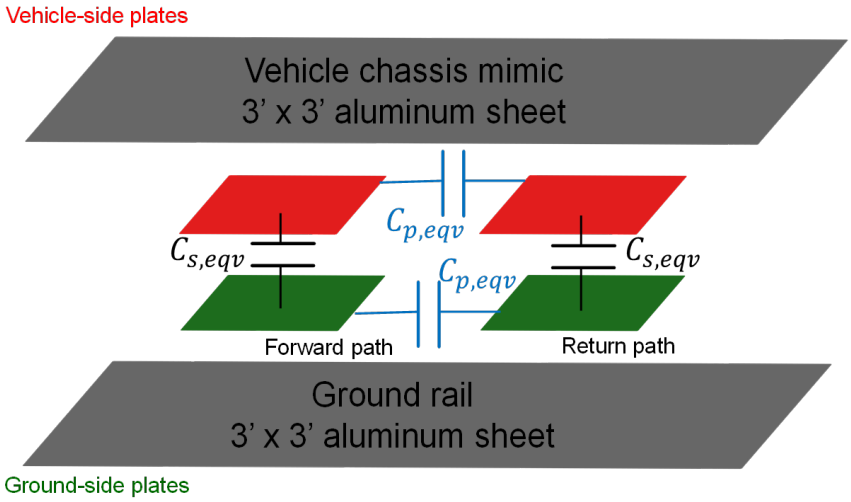
$$C_{p,eqv} = C_{par} + C_d \tag{7.2}$$

$$C_{par} = C_p + \frac{C_{psn} + C_{psf}}{2} \tag{7.3}$$

leading to the equivalent circuit in Fig. 7.3b



(a)



(b)

Figure 7.3: Single module CWPT system from Fig. 7.2, with explicitly drawn capacitances. (a) Drawing showing all capacitances involved in the WPT system. (b) Equivalent circuit of the WPT system.

The corresponding circuit diagram for the circuit in Fig. 7.2a can be seen in Fig. 7.4, where equivalent π circuit model for the various capacitances between the charging plates and road/car sheets can be clearly seen. The primary and secondary side matching networks are then designed to transfer power through the equivalent series capacitances (C_S) of this π-network and the parallel capacitances (C_P) are absorbed into the L-section matching networks as shown in the equivalent circuit. The power inverter has an H-bridge topology and is implemented with 650 V, 15 A GaN on Si FETs (GaNSystem GS66504B). The frequency of operation is 6.78 MHz (ISM band). This module transfers power through a pair of coupling plates, one in the forward path and one in the return path. To minimize circulating current and enable soft-switching in the power inverters, it is desired to have a near-resistive input impedance. Therefore, compensation is required and is implemented using L-section matching networks at the primary and secondary side, designed to achieve high efficiency by the method proposed in [111].

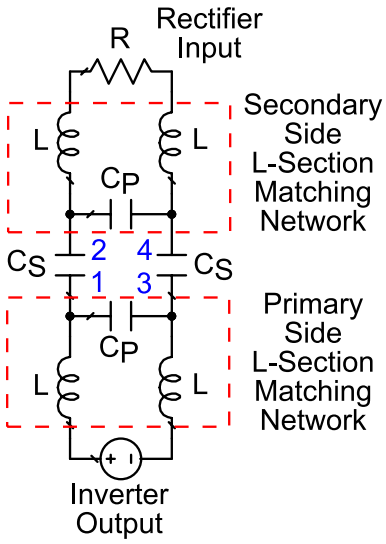


Figure 7.4: Equivalent circuit of the CWPT system including equivalent circuit of the parallel plates and the L-section matching networks. C_S and C_P represent the effective capacitive coupling of the CWPT system.

The experimental system shown in Fig. 7.2a has square plates with a side s =17.68 cm, and the L-section matching network has a parallel capacitance C_S =14.2 pF, a series capacitance C_P =0.8 pF and series inductors L =22.4 μH designed according to [111]. The prototype provides 110 W of output power with an efficiency of 90% to an RF load R =42 Ω that simulates the input of the on-board vehicle rectifier. Fig. 7.5 shows the measured output power as a function of input DC voltage. This single-module system is capable

of wirelessly and efficiently transfer high power from the road to a vehicle.

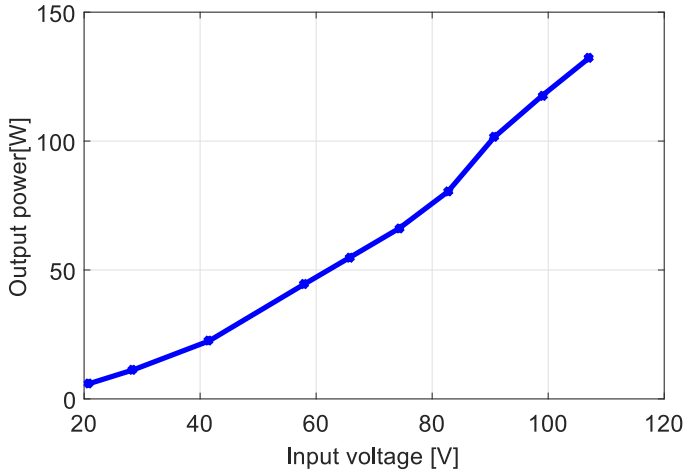


Figure 7.5: Measured output power of the single module system with versus input DC voltage. Output powers above 110 W correspond with 90% efficiency.

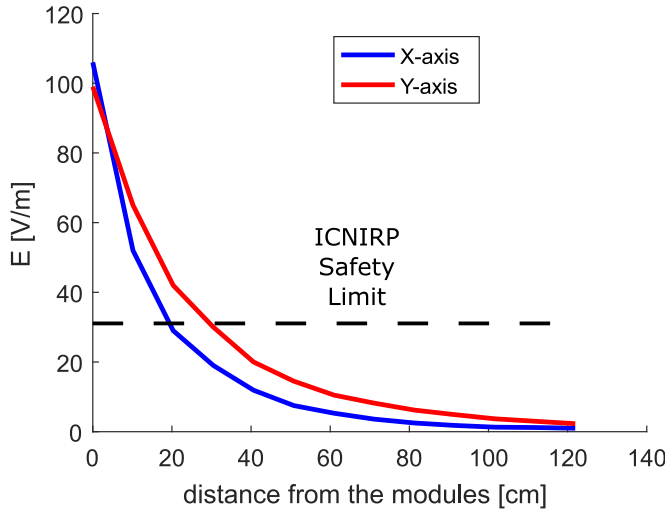


Figure 7.6: Measured electric field magnitude (RMS) of the single-module CWPT system, for an output power of 110 W. The distance references are the edges of the ground plane, which can be seen in Fig. 7.2a. The origin corresponds to the edges of the aluminum sheet.

7.3 Multi-module System

The total magnitude of the electric field vector inside and around the vehicle, where people may be present, has to be below the limits set by the International Commission on Non-Ionizing Radiation Protection (ICNIRP) [110]. The fringing electric field produced by the single-module prototype from the previous section, when transferring 110 W of output power, is shown in Fig. 7.6. The fields exceed the ICNIRP safety limit of 33.4 V/m (RMS) at 6.78 MHz and will increase as the output power is increased to the required kW levels. To comply with the exposure limits in [110], the spillover electric field must be reduced. To this end a multi-module CWPT system is used, with the architecture as simulated in [112] and shown in Fig. 7.7.

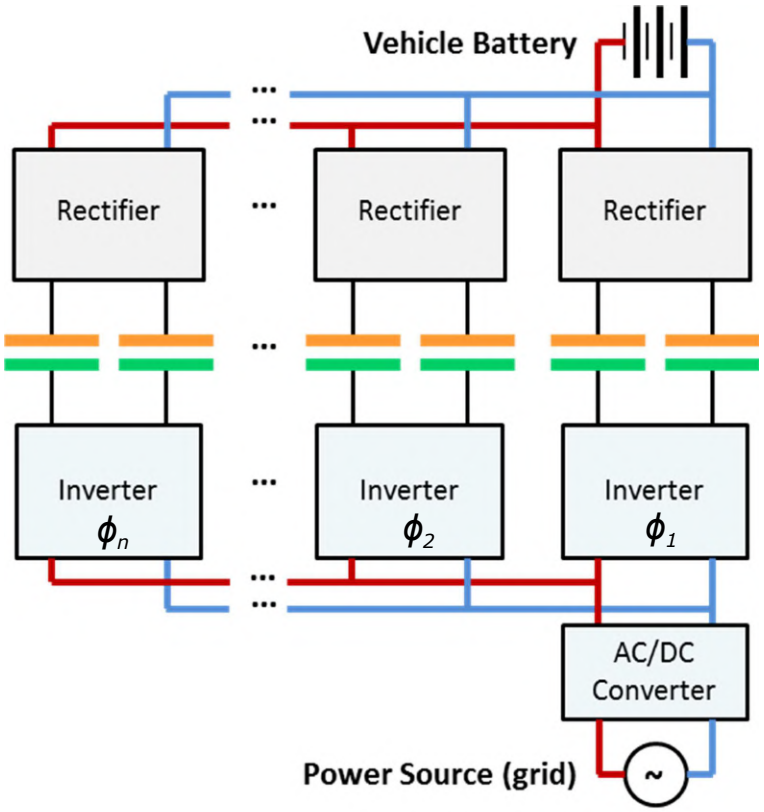
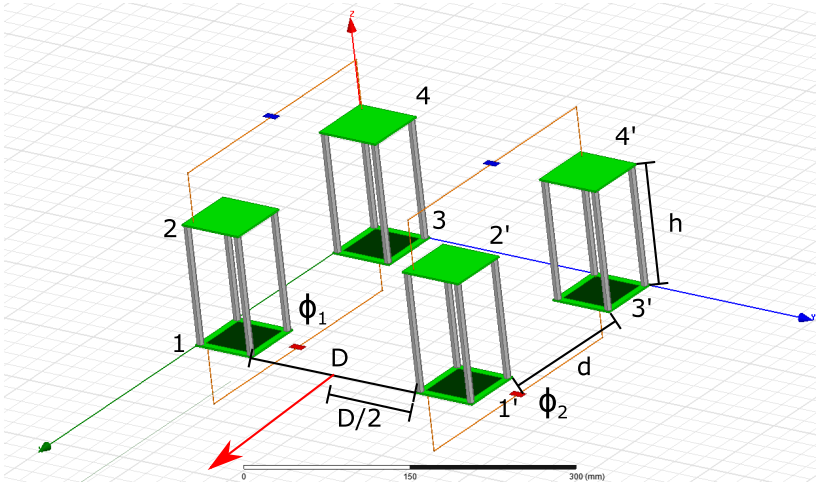


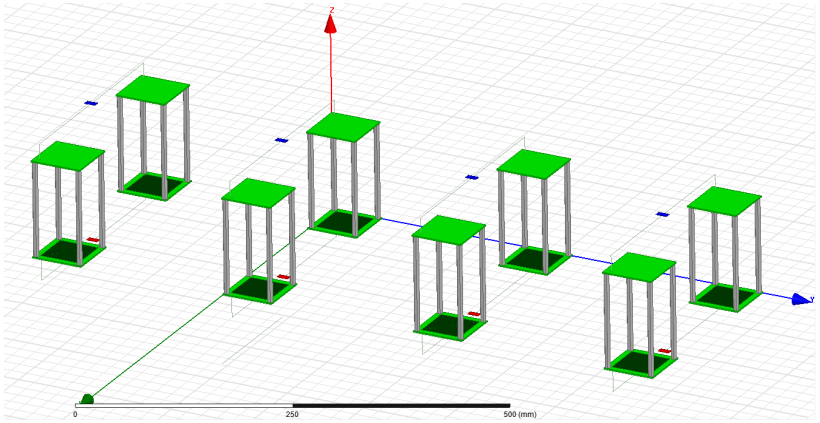
Figure 7.7: Block diagram of a multi-module CWPT system, with receiving-side capacitor plates shown in orange, and road-side plates shown in green. Phase shifts are applied within the power inverters in order to reduce the fringing fields and meet safety requirements.

The near field reduction is achieved by a relative phase between adjacent identical modules, analogous to beam steering in the far field of phased array antennas. In [112] it is shown by full-wave simulations that the

optimum field cancellation is obtained when the phase shift is 180°, making the feeding of the modules very simple, as long as the feeding is done in a balanced way. Full-wave EM simulations of the CWPT system with plate geometry corresponding to the measured module were performed using ANSYS HFSS, Fig. 7.8 shows the models used for the simulations.



(a)



(b)

Figure 7.8: HFSS simulation setup, where a 50 V voltage source (red) is used on the power inverter side (bottom), and the rectifier side is represented with a 2 kΩ (blue) load. The plates are printed on the green FR4 substrate and the gray dielectrics are nylon standoffs used for structural stability and alignment. The red arrow references the location where the field is measured. The plates denoted with 1', 2', 3' and 4' belong to the second module. (a) Two- and (b) four-module system simulation models.

7.4 Field Reduction Measurements

Fig. 7.9 shows a photograph of a two-module experimental setup used to measure the electric field generated by the parallel plate CWPT modules. The plates are 5 cm×5 cm in size and with separations of $h = 12$ cm between plates and $d = 15$ cm between pairs of plates of the same module. The modules are located at a distance $D = 20$ cm from each other. A load resistance of 2 kΩ represents the input of the secondary side L-section matching network loaded with the rectifier. The feeding signal is generated using an RF transmitter to emulate the output of the power inverter and provide a reasonably high power level. An external tuner is used to match the generator to the WPT system. The plates are fed with a 50 V peak sine wave generated by a ICOM IC-7410 frequency locked RF transmitter at 7, 14 and 29 MHz. These frequencies are within amateur radio designated bands and are selected because of amplifier availability and proximity to the ISM bands (6.78, 13.56 and 27.2 MHz). The voltage applied to the plates is monitored using an oscilloscope with differential probing. The electric field is measured using an ETS HI-6005 electric field probe. The plates are fed using high-power baluns (W2AU) to ensure balanced feeding of the modules.

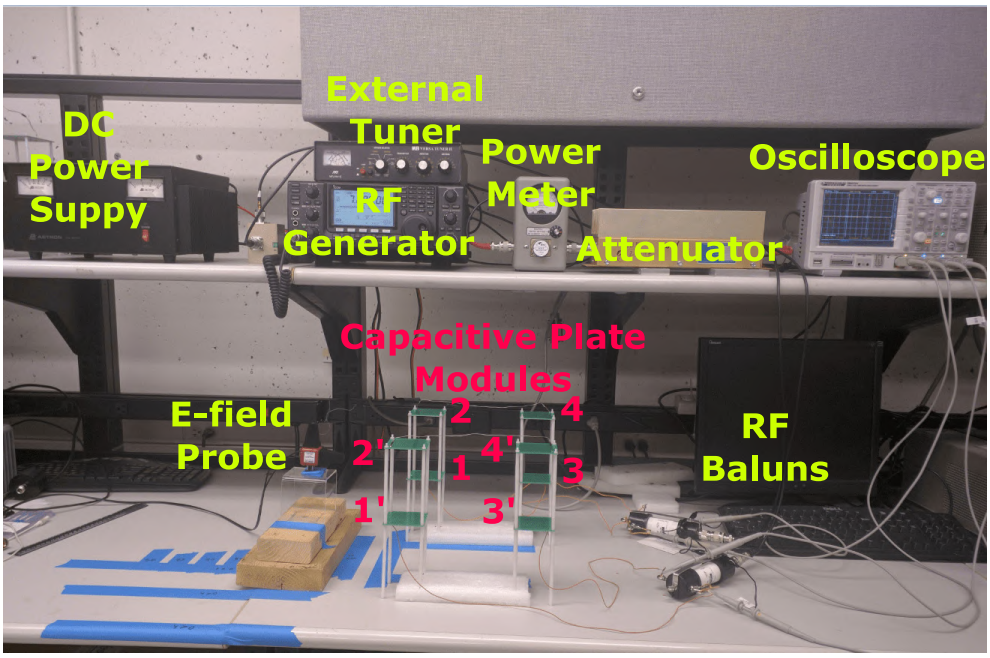


Figure 7.9: Multi-module CWPT system photograph, showing 8 plates corresponding to the two CWPT modules as well as the E-field probe and baluns used to provide out-of-phase feeding. The photo also shows the rest of the important hardware used in the measurement.

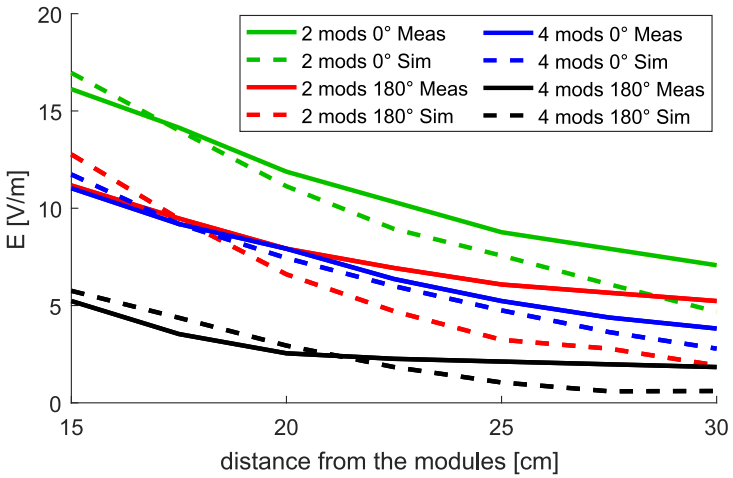


Figure 7.10: E-field measurement (solid) and simulations (dashed) at 7 MHz as a function of distance along x axis for two modules (green and red), four modules (blue and black), and different phases.

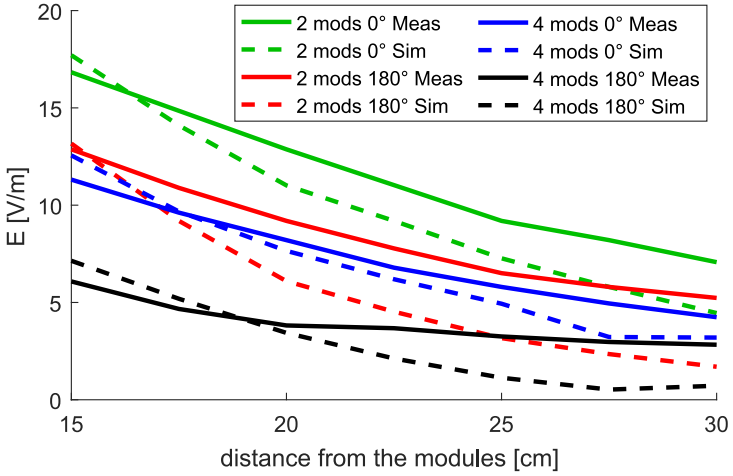


Figure 7.11: E-field measurement (solid) and simulations (dashed) at 14 MHz as a function of distance along x axis for two modules (green and red), four modules (blue and black), and different phases.

Fig. 7.10, 7.11 and 7.12 show the electric field as a function of distance from the CWPT system near three ISM band frequencies for systems consisting of 2 and 4 CWPT modules, and for different relative phases between modules. Measurements and simulation show good agreement and field reduction can be easily appreciated for both systems.

Fig. 7.13 consolidates the measurement results by showing the field reduction computed as

$$\Delta E = \frac{E_{0^\circ} - E_{180^\circ}}{E_{0^\circ}} \times 100 \tag{7.4}$$

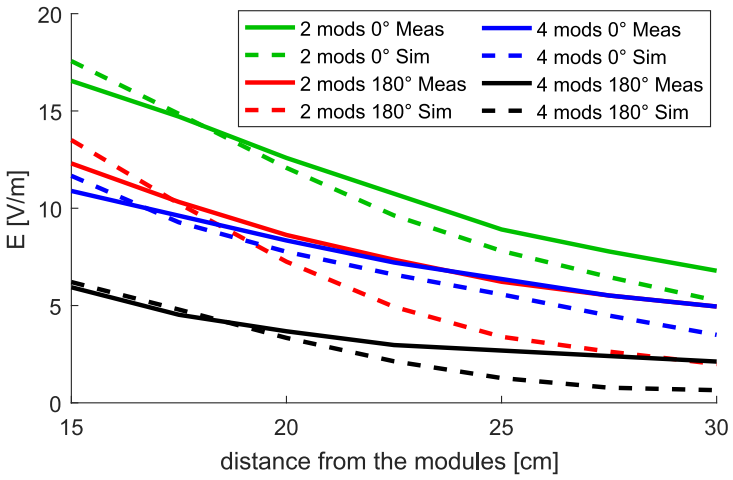


Figure 7.12: E-field measurement (solid) and simulations (dashed) at 29 MHz as a function of distance along x axis for two modules (green and red), four modules (blue and black), and different phases.

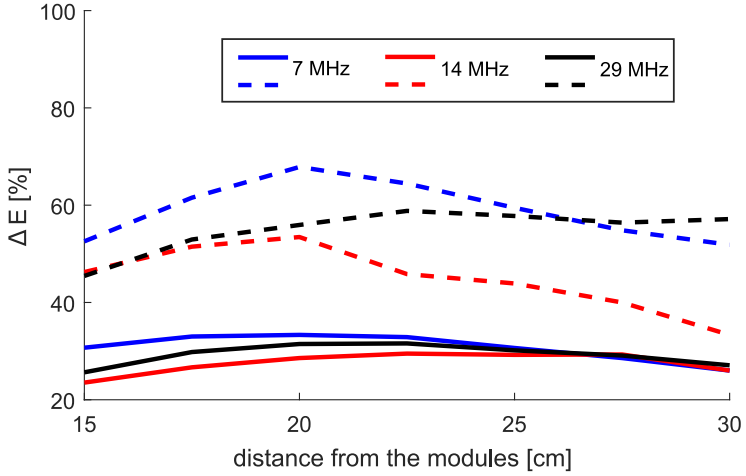
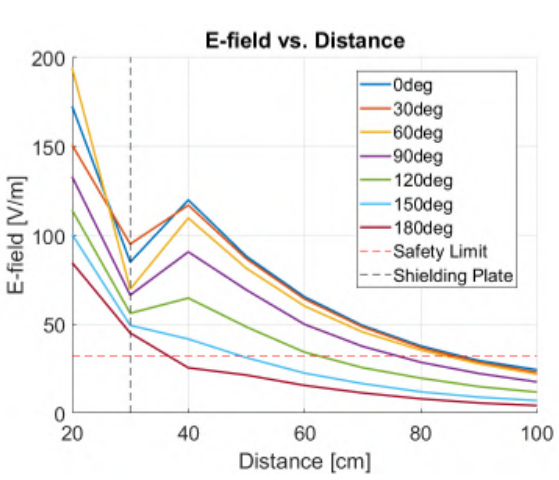


Figure 7.13: Two- and four-module systems electric field difference (ΔE) between the 0° and the 180° phase shifted feed; the solid and dashed traces correspond to the two- and four-module systems, respectively.

where E_{0° and E_{180° are the magnitudes of the electric field generated by the system when the feeding is done in phase and with phasing of 180°. The field reduction is above 24% for the two-module system and 32% for the four-module system at three different frequencies. At closer distances (less than 25 cm), where the fields are more intense, the reduction is above 24% and 43% for the two and four module systems, respectively. The results of the simulations diverge from the measurements at larger distances due to the decreased sensitivity of the field measurement at lower field strengths and lack of modeling of surrounding objects. As expected the four-module system provides a larger field reduction due to more electric field interference.

Finally a two-module 1.1 kW CWPT system was fabricated and tested, Fig. 7.14a displays a photo of the system wirelessly powering light bulbs. The system was measured for different phase shifts and at a constant output power if 1.1 kW. The measured electric field can be seen in Fig. 7.14b. As previously shown, the field reduction is maximized at 180° phase shift. Fig. 7.14c shows the efficiency plotted as a function of phase shift, demonstrating that not only is the maximum field reduction accomplished at 180° phase shift but the efficiency of the multi-module system is almost unaffected in this operating conditions, with a maximum dip in efficiency happening at 90° phase shift.

(a)



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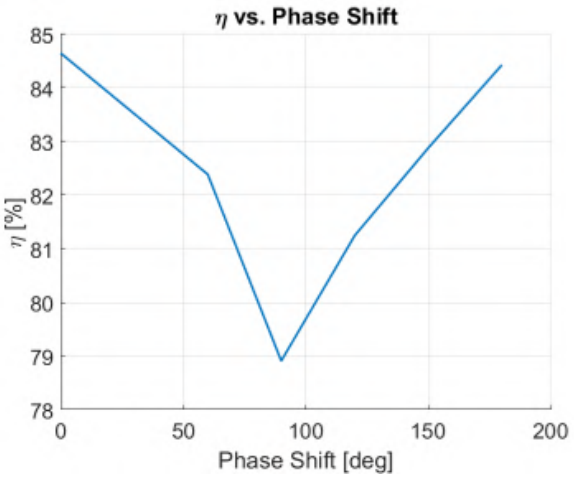

(c)

Figure 7.14: 1.1 kW CWPT system. (a) Photo of the system and measurement setup. (b) Electric field measured during operation of the CWPT system, the red horizontal dashed line is the safety limit and the black vertical dashed line is the edge of the aluminum plates (some measurement were taken in between these plates). (c) Measured power transfer efficiency as a function of phase shift.

7.5 Chapter Summary

In this Chapter a method for reducing fringing electric fields in a capacitive WPT system using a near-field phased array consisting of multiple CWPT modules is introduced and demonstrated. CWPT was explained, including its benefits compared to inductive near-field WPT and a single module system with 110 W of output power and 90 % efficiency was presented. A simplified model for the coupling plates is also discussed. The multi-module approach for field reduction is introduced and experimentally validated on a proof of concept experiment using RF equipment and later a fully working 1.1 kW system is used to further validate the concept through measurements. These measurements also validate the 180° phase shift as the optimum for field reduction and also WPT efficiency. Field reduction is 24% with a two-module system and 43 % with a four-module system, at distances closer than 25 cm and for frequencies of 7, 14 and 29 MHz. Full-wave EM simulation trends agree well with measurements and any deviations can be attributed to lack of modeling of the surroundings. The contributions from this Chapter are reported in [112, 113, 114].

Chapter 8

Narrowband Energy Harvesting

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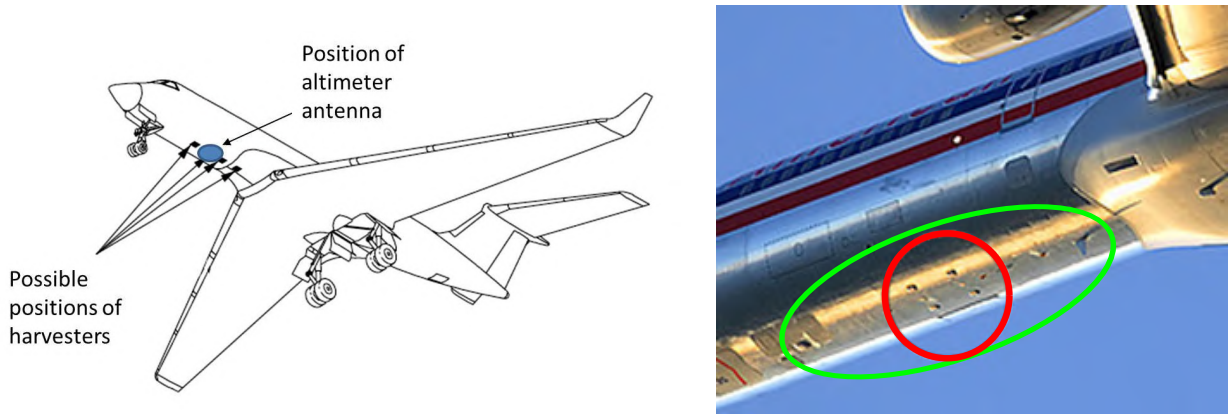
Harvesting RF power from side-lobes of an aircraft altimeter can enable low-maintenance unattended sensing of various quantities relevant to aircraft structural health [115, 116]. Fig. 8.1 shows a photograph of the aircraft body with the position of the altimeter radar and potential placement of sensors. Altimeter antenna radiation patterns obtained from the manufacturer [117] show a gain of 10.4 dBi in the direction of ground and sidelobes with -13 dBi gain in the direction of the aircraft skin, the radiation pattern can be seen in Fig. 8.2.

The RF power density available ranges from 0.04 μW/cm^2 to 2.2 μW/cm^2 at 4.3 GHz and at a distance of 30 cm from the altimeter's antenna [117, 118, 119]. Low-power structural integrity sensors can be powered by delivering 300 μJ of energy every 10 minutes. The average power requirement at the DC side is

$$P = \frac{300\,\mu\text{J}}{10\,\text{min}} = 0.5\,\mu\text{W} = -33\,\text{dBm}. \tag{8.1}$$

In this chapter, the co-design of the antenna, single-ended diode rectifier, and harvester power manage-



(a) (b)

Figure 8.1: Typical location of the altimeter radar on a commercial aircraft. (a) Location on the plane. (b) Photograph of plane, the red circle shows the location of the altimeter antennas and the green oval is the approximate region where the harvesters can be located.

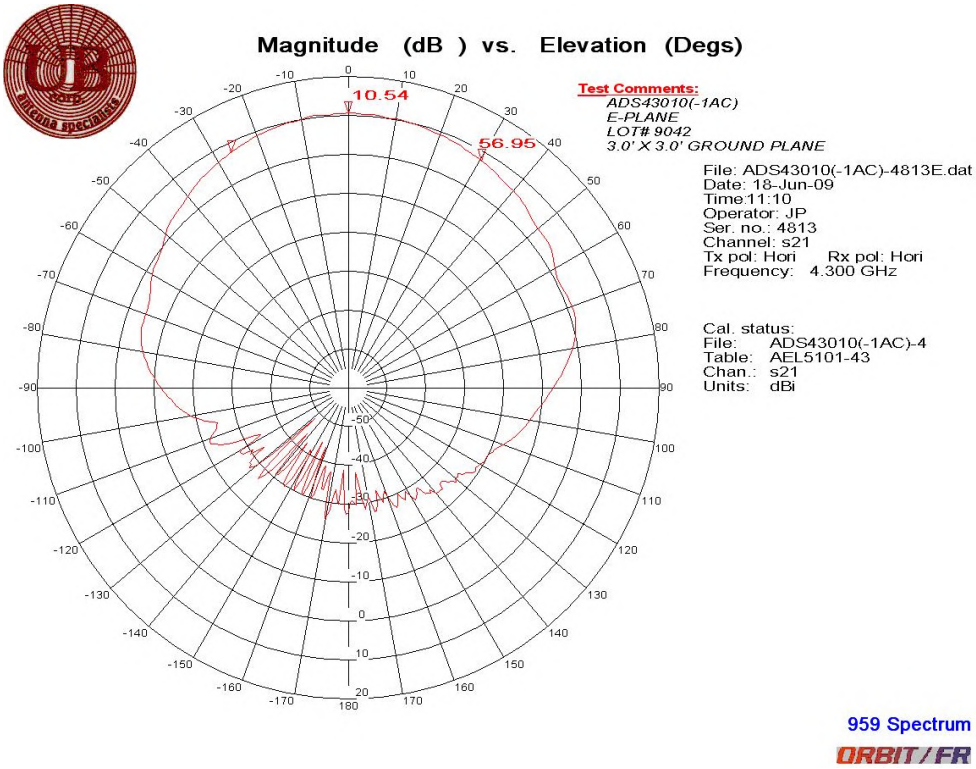


Figure 8.2: Microstrip RAA ADS43010(-1A) & (-1AC) altimeter radar antenna radiation pattern taken from [117].

ment are detailed. Integration of a full system capable of harvesting the required energy is demonstrated.

8.1 Rectenna Design

The rectenna design can be split into two parts, first the high-frequency rectifier design, followed by the antenna design. Codesign of both allows for compact and more efficient performance of the rectenna, similar to the filter power amplifiers from Chapter 4. A codesigned rectenna avoids the use of a matching network between the rectifier and the antenna by directly designing the antenna to present the required impedance to the rectifier. Likewise, the low-pass filter needed to extract the DC from the rectifier can be codesigned into the antenna. This section explains the complete rectenna design.

8.1.1 Rectifier

Based on the the average power the rectifier has to provide, a number of commercial diodes were considered. Source-pull simulations were performed in Cadence AWR Microwave Office harmonic balance simulator, using available nonlinear models from Modelithics and manufacturer provided spice models. The optimum RF impedance that needs to be presented to every diode to obtain the highest rectifier efficiency was determined, and the results are summarized in Table 8.1. The device that requires the smallest input power is selected: SMS7630-061 GaAs Schottky diode.

Table 8.1: Simulation results from the considered diodes listing the RF impedances and input powers needed to get the required -33 dBm of output power at the DC side. The output DC power in all cases is −33 dBm at 4.3 GHz.

Model	Manufacturer	Input Power (dBm)	Optimum Source Resistance (Ω)	Optimum Source Reactance (Ω)
SMS7630-061	Skyworks	-23.5	38.0	251.6
SMS7621-079 Modelithics	Skyworks	-20	4.7	118.0
SMS7621-079 Spice	Skyworks	-21	44.1	326.0
HSMS-286x	Avago	-19.5	36.0	192.3
HSCH-5314	Avago	-16.5	52.0	307.1
MA4E1317	MACOM	-13.5	382.1	763.5

The rectenna uses a single SMS7630-061 GaAs Schottky diode as a half-wave rectifier connected in parallel with the antenna. These diodes are commonly used in rectennas due to their high frequency operation and low on voltages, which are very appropriate for low power rectification. The rectifier is simulated using harmonic balance (HB) source-pull analysis. During the source pull simulations, the RF input impedance at the diode is swept, while the input power and DC load are varied. The contours of constant DC rectified power for a 5 kΩ DC load and at -15 dBm input power are shown in Fig. 8.3, indicating that the optimal complex antenna impedance under these conditions is $Z_a = (38 + j252)\,\Omega$.

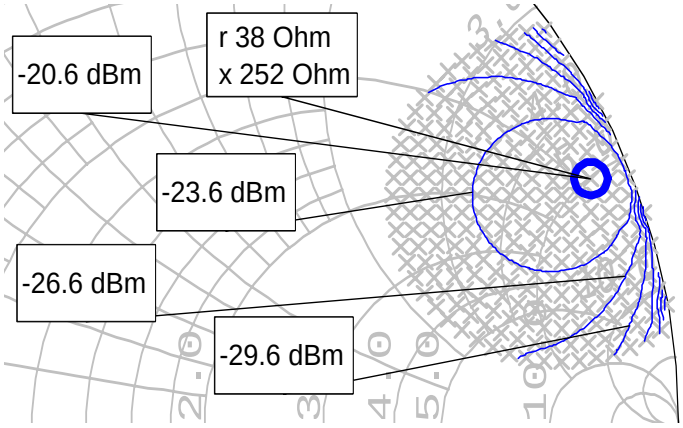
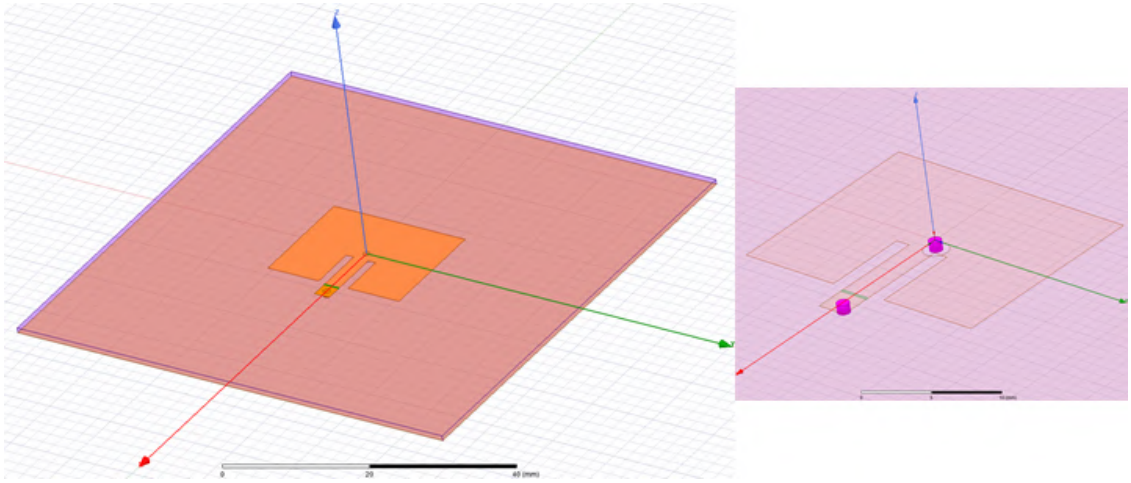


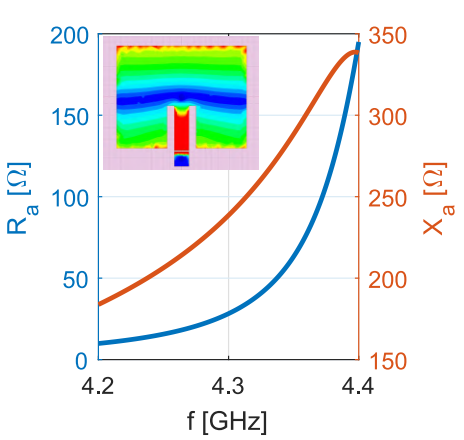
Figure 8.3: Rectifier HB source-pull simulation results. It shows contours of constant rectified power, in dBm, for -15 dBm input power and a DC load of 5 kΩ for the Skyworks SMS7630-061 GaAs Schottky diode.

8.1.2 Antenna

The antenna is a radiating-edge fed linearly polarized rectangular patch antenna on a Rogers RO4350B™ substrate, designed for maximum power transfer to the rectifier. Ansys HFSS is used to design the feed point that directly matches the antenna to the diode complex impedance, removing the need for a matching network. Fig. 8.4 shows the simulation model and results. The antenna impedance at 4.3 GHz is $Z_a = (30 + j240)\,\Omega$ with an antenna gain of 5 dBi. The rectifier DC collection circuit uses the RF null of the patch as DC-RF isolation, serving as a low-pass filter and further reducing the size and loss of the rectenna passive circuit. The DC power delivered by the rectenna at 4.3 GHz with an incident power density of 0.65 μW/cm^2 is -23.2 dBm



(a)



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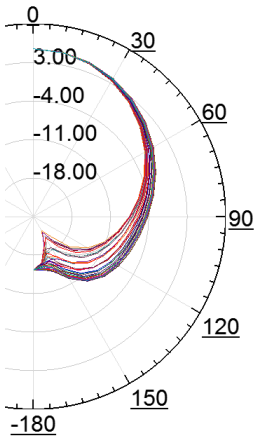


(c)

Figure 8.4: Antenna design simulation results. (a) HFSS patch antenna model. (b) Antenna impedance showing both real and imaginary part and surface current density amplitude distribution. (c) Radiation pattern in θ and for a ϕ sweep.

8.1.3 Measurements

Three rectennas were built for validation of simulation models. Prototype for SMS7630-061 is shown in Fig. 8.5, the other two are for the SMS7621-079 diode. Measurements were carried out inside an anechoic chamber with calibrated power densities at the plane of the rectenna of $0.13\,\mu\mathrm{W/cm^2}$ and $0.65\,\mu\mathrm{W/cm^2}$, both within the lower range of the estimated power density in the harvesting environment. Two values of capacitors are used as energy storage devices, $100\,\mu\mathrm{F}$ and $1\,\mathrm{mF}$. Fig. 8.6 shows the test setup for the measurements.

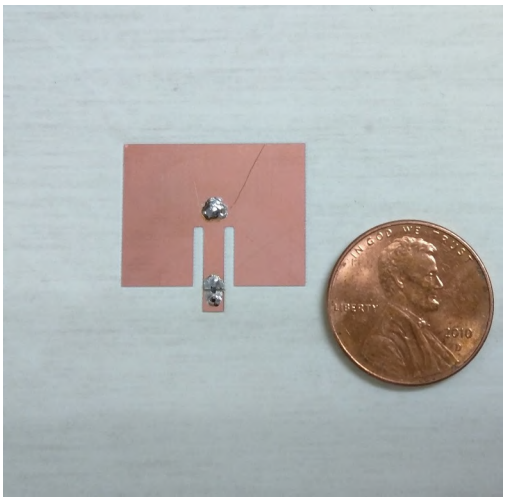


Figure 8.5: Skyworks SMS7630-061 rectenna prototype.

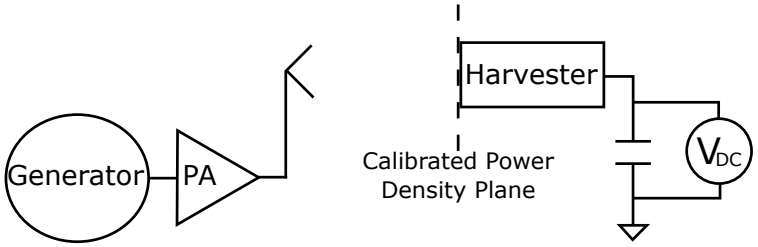


Figure 8.6: Sketch of far-field test setup for the measurements of the rectenna prototypes showing all components used in the measurement. Measurements were performed inside of an anechoic chamber.

Fig. 8.7 shows the open circuit voltages for all the prototypes. Since prototype SMS7630-061 has the best performance, as will be shown later[1] , measurements at the higher power were only done with this prototype. The open circuit voltage is used to find the resonant frequency of the device and to calculate the stored energy in the capacitor. From the three prototypes, SMS7630-061 is also the one that resonates closer to the design frequency (at 4.31 GHz). The frequency shift can be attributed to tolerances from both the substrate and the milling process as well as to imprecisions in the modeling of the diode.

The energies that can be stored in a capacitor at the peak voltages for all cases are shown in Table 8.2. For 0.13 μW/cm^2 incident power density a 100 μF capacitor is used while for the 0.65 μW/cm^2 incident power density a 1 mF capacitor is used.

Open circuit voltage and energy are not enough to characterize the behavior of the devices since the

[1] The open circuit voltage can only be used to find the resonant frequency. The output impedance information is necessary to know exactly what is the available power of the equivalent source.

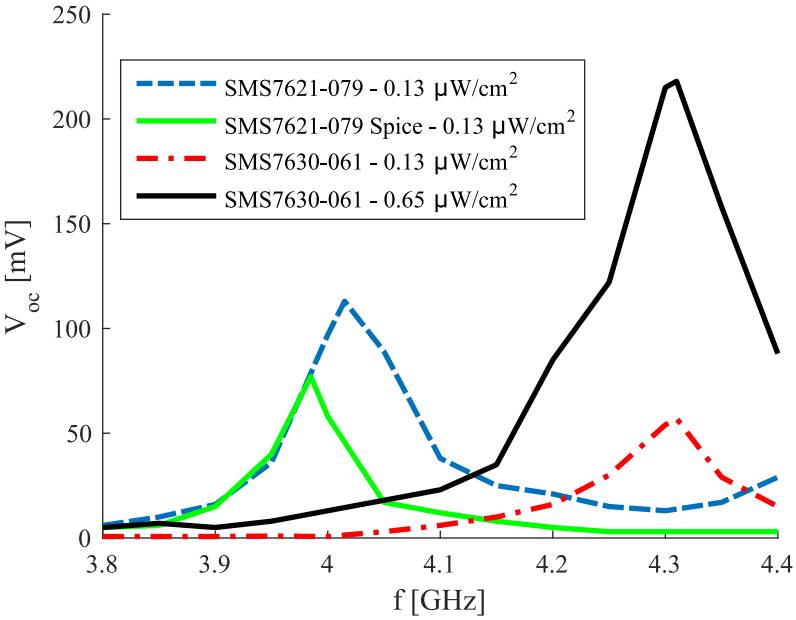


Figure 8.7: Measured open-circuit voltage of the rectenna prototypes, as a function of frequency, when illuminated with 0.13 and 0.65 μW/cm^2. Each rectenna resonant frequency is obtained from this plot.

Table 8.2: Energy stored in a capacitor at the maximum open circuit voltage measured, Fig. 8.7.

Prototype	Power Density (μW/cm^2)	Capacitance (μF)	Voltage (mV)	Stored Energy (μJ)
SMS7621-079 Modelithics	0.13	100	113	0.64
SMS7621-079 Spice	0.13	100	77	0.30
SMS7630-061	0.13	100	57	0.16
SMS7630-061	0.65	1000	218	23.8

stored energy must be collected in a fixed amount of time. For this reason the time constants of the charging circuits were also measured. Fig. 8.8 shows a plot of the time constants for all the prototypes. Once again for 0.13 μW/cm^2 incident power density a 100 μF capacitor is used while for the 0.65 μW/cm^2 incident power density a 1 mF capacitor is used. The time constants are defined as the time it takes for the output voltage to reach 63.2 % $(1 - e^{-1})$ of the open circuit voltage. It is evident in Fig. 8.8 that the prototype that uses the SMS7630-061 diode is considerably better and can store the energy in shorter bursts than the other two prototypes, i.e. it can deliver more power. The average power delivered to the capacitor in one time

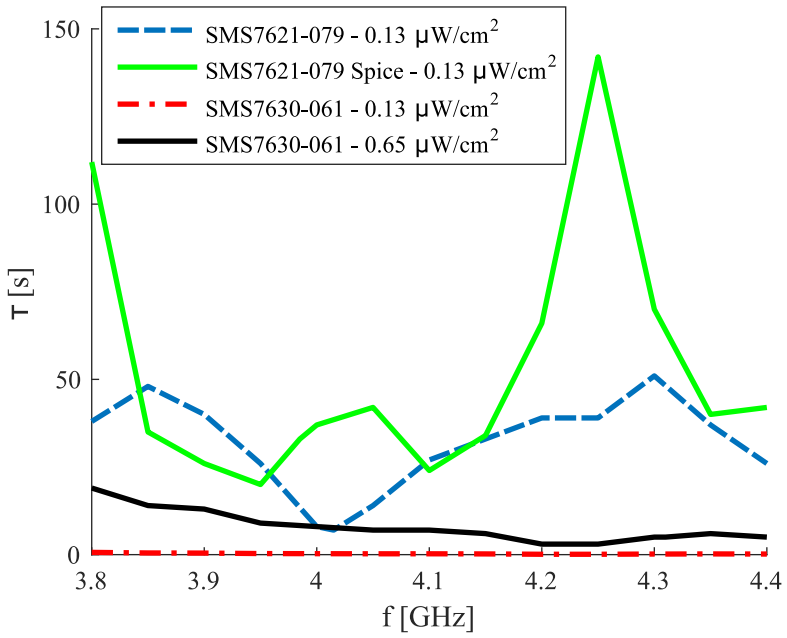


Figure 8.8: Time constant τ, as a function of frequency, measured as the time it takes the circuit to reach 63.2 % of its open-circuit voltage.

constant is shown in Fig. 8.9, where it can be seen that the device delivers more than -31.5 dBm in the whole bandwidth of interest (from 4.2 to 4.4 GHz).

8.2 Full Harvesting System

The voltage available from a single Schottky diode at low power levels is too small for most electronic functions, therefore some power management with voltage boosting is necessary. Additionally, when the available RF power varies, the output source resistance of the rectifier also varies. Maximum power point tracking (MPPT) can be used to dynamically adapt the load for maximum power extraction [120], a technique commonly used in, e.g., photo-voltaic systems [121]. In our case, the power variation is not substantial and the load seen by the rectifier is not dynamically adjusted but instead is fixed to the experimentally obtained 20 Ω optimum DC loading. Using a Texas Instruments BQ25504 PMM chip, the effective resistance seen by the rectifier is set to the optimum value. The BQ25504 chip also has a high efficiency boost converter that increases the voltage level to a more usable 3.2 V. The BQ25504 can efficiently manage microwatts of power and it also has a cold start up operation mode which can start with voltages as low as 330 mV. After

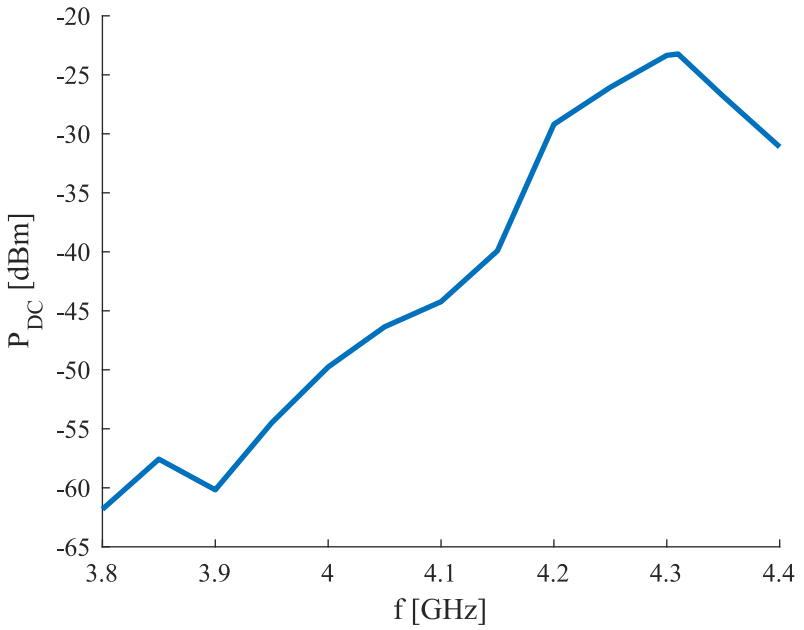


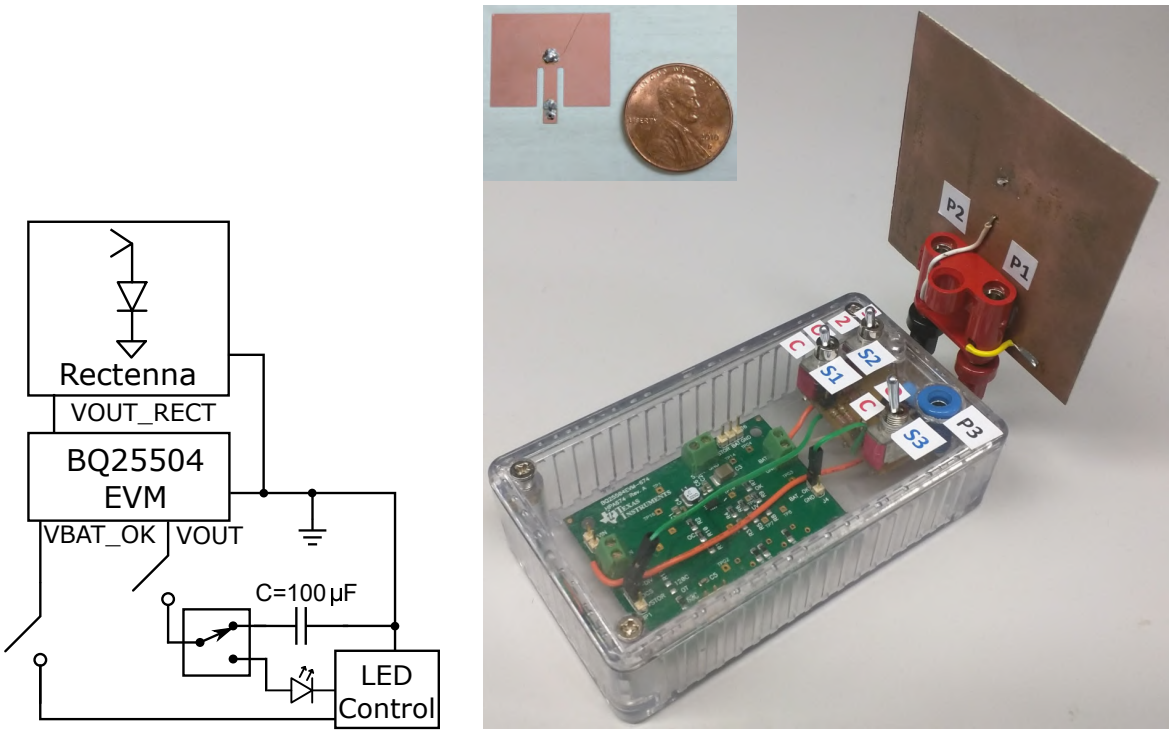
Figure 8.9: DC power output as a function of frequency for the SMS7630-061 prototype with an incident power density of 0.65 μW/cm^2 and loaded with a 1 mF capacitor.

the main boost charger turns on and efficient operation begins the system can work with input voltages as low as 80 mV.

A demo for the full harvesting system was built, and it is capable of charging a 100 μF capacitor (built into the evaluation module) or a 200 μF capacitance (a 100 μF capacitor in parallel with the built in one). A simple efficient circuit also allows the system to be configured to blink an LED for visual demonstration of the harvested power. The experimental unit is shown in Fig. 8.10.

The energies stored in the two capacitors when charged to 3.2 V are $E_{100} = 512\,\mu$J and $E_{200} = 1024\,\mu$J, respectively. The time it takes for the system to fully charge the 100 and 200 μF capacitors from a fully discharged state (cold-start operation) is 8 and 9 min, respectively. The module starts efficient operation when the output voltage reaches 1.7 V, which occurs after 7 and 8 min for the 100 and 200 μF capacitors, respectively. This indicates that most of the time is spent in cold-start operation, and after this the system can harvest energy at a faster rate. These measurements are performed with a 2 μW/cm^2 incident field that is calibrated using an ETS HI-6005 electric field probe.

Another test is performed with a blinking LED as the load, to demonstrate the efficient mode operation.



(a) (b)

Figure 8.10: Harvesting system circuit (a) diagram and (b) photos of both the rectenna and the power management module.

A 100 μF capacitor is charged to 3.2 V and then discharged through an LED to 1.8 V (right above the efficient operation threshold). While in efficient operation and for an incident field of 2 μW/cm^2, the LED turns on and off with a period of 20 s. Since the voltage drops to 1.8 V after each blink, the energy at the end of the cycle is $E' = 162\,\mu$J. This implies that the energy delivered after each blink is $\Delta E = 350\mu$J. The experiment shows that the energy that is specified to be delivered to a sensor every 10 min can be done every 20 s and the average harvested power is:

$$P = \frac{\Delta E}{T} = \frac{350\mu\text{J}}{20\,\text{s}} = 7.78\,\mu\text{W} = -21\,\text{dBm}. \tag{8.2}$$

Once efficient operation has started the system can harvest energy at lower incident power densities. A dedicated source could be used to bypass the cold start time.

8.3 Chapter Summary

It is demonstrated that a rectenna device can successfully harvest enough energy from a radar altimeter to energize low power/slow duty cycle sensors. Several diodes are considered and the best performance is given by Skyworks SMS7630-061. The demonstrated energy harvesting from very low incident power levels at 4.3 GHz ($< 2\,\mu\mathrm{W/cm^2}$) is sufficient to power unattended sensors on an aircraft. These results validate the co-design methodology for the rectenna, which combines full-wave EM modeling and nonlinear circuit simulations. A bigger array of rectennas can be used to power sensors with higher energy requirements as is shown in [122, 123]. The contributions from this Chapter are reported in [119, 124].

Chapter 9

Wearable Broadband Energy Harvesting

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9.5 Chapter Summary 129

Wearable devices for fitness and sports, entertainment, healthcare, defense, and industrial monitoring are gaining popularity, as companies such as Apple, Fitbit, Adidas, Garmin, Nike, Google, Samsung, Sony, etc. are placing more devices on the market daily. The global wearable devices market is expected to exceed US$51 billion by 2022 at a growth of 15% according to some market studies [125]. The devices include foot, wrist, eye, neck, and body-wear, and many include wireless functions thus requiring antennas. For example, a 2×2 MIMO antenna for 5G is demonstrated in a wrist watch with greater than 85% efficiency [126].

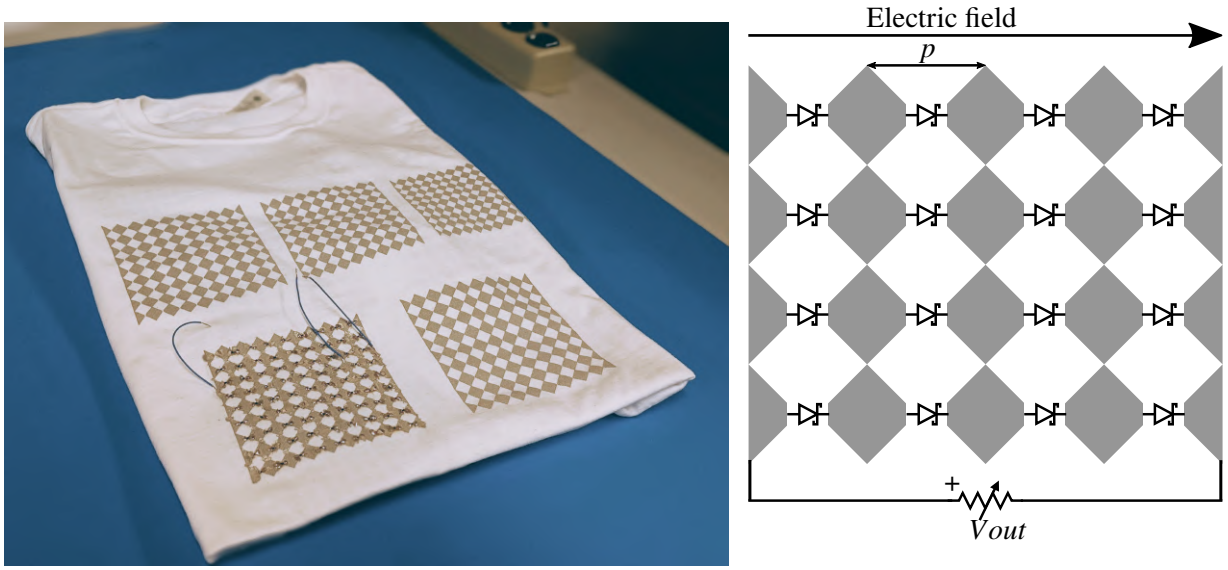
Wearable antennas related to on-body telemetry include, e.g. implantable wireless capsule endoscopy, insole shoe monitoring, and eyeglass frame monitoring sensors [127, 128, 129]. Different materials amenable to antenna integration are under investigation. In [130], a silver-coated nylon ripstop fabric patch antenna

with detachable radiating elements is presented, while [131] demonstrates embroidered antennas with pcb resolution. Antenna integration is demonstrated in denim [132], as well as military berets for GPS, fabricated on a conductive metallized nylon fabric over a felt substrate [133]. In [134] a UHF RFID tag was tested over the human body after several washing and drying cycles of a cotton T-shirt, and screen-printed antennas with washing effects are presented in [135]. Extensive characterization of different textile materials for wearable antennas is described in [136], and a comparison of various technologies in [137] and [138], where challenges associated with soldering electronic devices to conductive textile patterns are highlighted.

Antennas integrated with rectifiers, or "rectennas", were developed in the 1950s and there are many excellent reviews of this topic, e.g. [139]. Wearable rectennas include dual-polarized screen-printed patches on cotton substrates [140], a 2.45 GHz patch antenna and array on a cordura fabric for power levels down to -40 dBm [141], a 2.45-GHz textile patch for watt-level incident power [142], and a UHF patch on a bi-layer jeans substrate [143]. In addition to these narrowband rectennas, some broadband implementations have been demonstrated, e.g., a 0.9 to 4 GHz circularly-polarized archimedean spiral [144], and a 0.5 to 8 GHz logarithmic spiral embroidered with conductive yarn into denim [145].

Harvesting ambient RF power has been of interest for energizing low power sensors for several decades [123, 146, 147]. Applications for harvesters range from powering aircraft sensors from altimeter antenna sidelobes [124], to multiband rectennas integrated in a kitchen quartz clock and environmental sensor [148], as well as wearable devices that can harvest multiple frequencies [149]. The incident power densities are typically variable and in the range of 1-10 μW/cm^2, as quantified in an urban environment in [150]. Several rectennas for power densities of 1 μW/cm^2 have been demonstrated with efficiencies greater than 30%, including a 2-gram design on a flexible substrate [151] and a directive antenna with an unconventional reflector [152]. In a harvesting scenario when incident power densities can vary over a wide range, the rectifier element impedance at the fundamental frequency varies dramatically [153]. Co-design of the rectifying element and dual-polarized antennas is discussed for a 2-GHz narrowband rectenna in [154] and for a 2-18 GHz broadband spiral array in [123]. At these low power levels, integrated design of the rectifier, antenna and power management circuit has been shown to result in the highest efficiency, requiring extensive rectenna characterization as a function of the dc load [155].

In this Chapter, simulations and measurements are presented for a wearable screen-printed rectenna array shown in Fig. 9.1. The antennas couple harvested microwave broadband radiation to an array of rectifiers, providing power for low-power wearable wireless sensors. The self-complementary, tightly-coupled bow-tie array is geometrically similar to the non-wearable design in [156]. The period of the array is 1.25 cm, which is approximately $\lambda_0/6$ at the highest frequency considered in the measurements. Each array element feed is connected to a packaged Schottky diode using silver paint and solder.



(a) (b)

Figure 9.1: (a) Photo of RF harvesting tee-shirt with several screen-printed rectenna arrays. (b) Circuit diagram of a 4×4 sub-array showing the Schottky diode connections to a dc load that represents the electronic application. The period (p) of the array is much smaller than a wavelength and is about $\lambda_0/6$ at the highest frequency of operation. The horizontal polarization is referred to as the co-polarized, consistent with diode orientation.

9.1 Ambient Characterization for RF Harvesting

To inform rectifier design, knowledge of the available incident power density levels, as well as their variation over time, is required. Electric field measurements were performed, first indoors in two laboratories and then outdoors on the roof of the building. A calibrated Keysight N6850A broadband omnidirectional antenna operating from 0.5 to 5 GHz was used with a N9918A FieldFox 26.5-GHz handheld microwave analyzer for

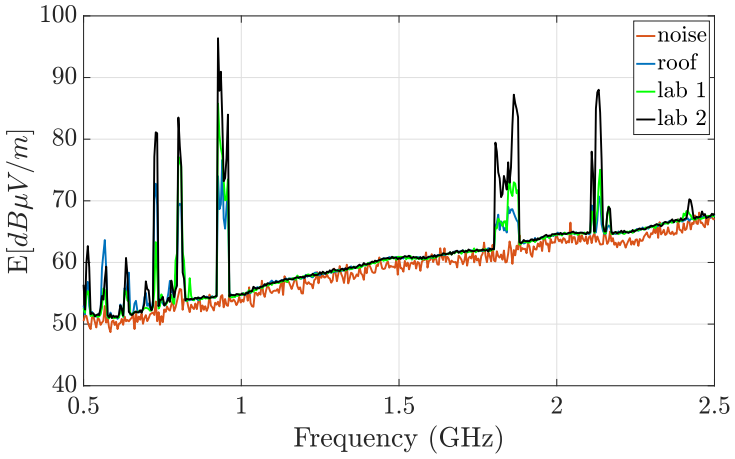
monitoring field levels outdoors at the roof of the building, and indoors at two different laboratories. Photos of the measurement setups are shown in Fig. 9.2.

(a) (b) (c)

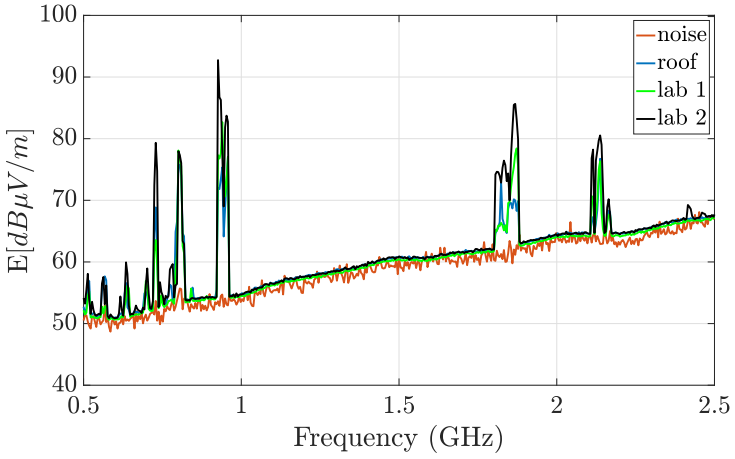
Figure 9.2: Ambient RF spectrum monitoring locations for three different scenarios: (a) roof, (b) laboratory 1 and (c) laboratory 2. Measurements were performed using a calibrated Keysight N6850A broadband omnidirectional antenna and a N9918A FieldFox 26.5-GHz handheld microwave analyzer.

Measurements were taken in two linear orthogonal polarizations (horizontal and vertical) every 30 seconds over 1004 frequency points. With a resolution bandwidth of 10 kHz, the measurements were averaged over three hours during a normal week day. The field measurements are calibrated using the antenna factor provided by the manufacturer, defined by the ratio of the magnitude of the electric field incident on the antenna to the voltage at the 50-Ω antenna port and expressed in V/m, or dBμV/m [157]. The data collected is presented in Fig. 9.3.

In Fig. 9.4, the minimum and maximum electric field values measured at each considered scenario are presented to show the variation of field levels. The frequency bands over which the power density was measured are 0.5 to 1 GHz, 1.5 to 2 GHz and 2 to 2.5 GHz. The data shows that it is possible to harvest RF energy in the sub-6 GHz range in current electromagnetic environments. As more wireless devices are connected in sub-6 GHz 5G bands (FR1) [158], it is expected that these levels will rise. The frequency range



(a)



(b)

Figure 9.3: Electric field measurement results at the locations shown in Fig. 9.2 for (a) horizontal polarization, (b) vertical polarization.

above 2 GHz is investigated to include the highest band in Fig. 9.4 and extend the harvesting frequencies to an octave above it.

The measured electric field values shown in Figs. 9.3 and 9.4 corresponds to power densities up to $S = E^2/120\pi = 3\,\mu\text{W/cm}^2$ in a single polarization at one frequency. To obtain the total power density, these values are integrated over frequency and polarization. Acknowledging that it is unlikely that a Schottky diode rectifier will turn on at the lowest field levels, a few $\mu\text{W/cm}^2$ was used as a starting point for the wearable rectenna design, as described in the next section. Note that these values are well below the safety recommendations for general public exposure given by the International Commission on Non-Ionizing Radiation Protection (ICNRP) [110].

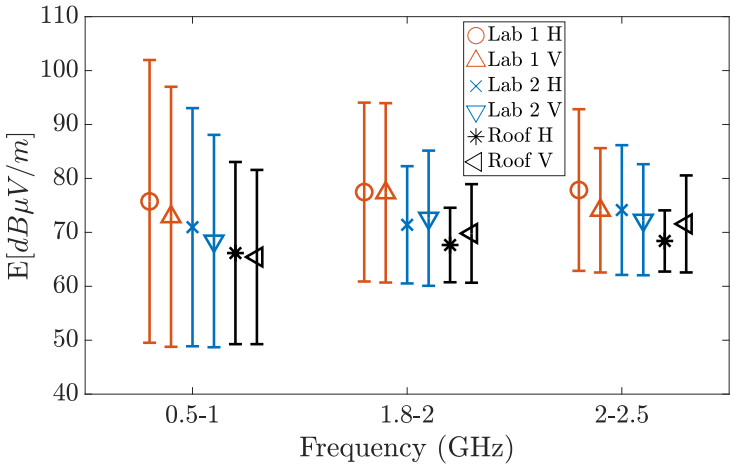


Figure 9.4: Variation of measured electric field values over time for the considered frequency bands for the three measured sites, in both horizontal and vertical polarizations. The measurements are taken every 30 s over three hours with a 10-kHz resolution bandwidth.

9.2 Diode Rectifier Simulations

The simulations of a single-ended diode rectifier based on a commercially available Schottky diode are described, over a range of power levels, frequencies and dc loads. The determined diode impedance for best efficiency can then be used to design a broadband antenna array. A Skyworks SMS7630-079LF zero-bias Schottky diode [159] is selected as the rectifying element and is characterized using non-linear harmonic balance simulations in Cadence/AWR over a range of expected frequencies and incident power densities. In [124], this diode is compared to several other commercially available packaged diodes in the 4-GHz range, while in [123] it is shown to have the highest efficiency of several commercial diodes for the incident power levels and frequency range used here.

The simple source-pull analysis schematic is shown in Fig. 9.5a, where the tuner also presents a dc block and the input power, frequency and dc load are varied. Fig. 9.5b shows the diode package model with its corresponding parasitics [160] used in the harmonic balance simulations.

The range of RF impedances that the antenna should present for best rectification efficiency across a fixed 2-kΩ load is shown in Fig. 9.6a with contours of constant output dc power for a fixed input power of 100 μW at 2 and 5 GHz, the edges of the frequency band. Fig. 9.6b shows the impedance obtained from diode source-pull for best efficiency at peak dc output power for varying frequencies and dc load. This

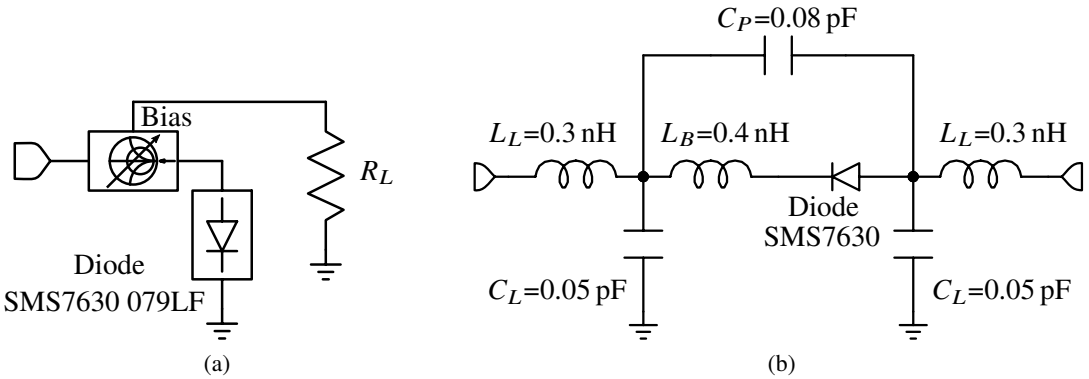


Figure 9.5: Circuit schematic for diode simulations (performed in Cadence/AWR). (a) Source-pull setup and (b) diode package (SC-79 or SOD523) model taken from the application note [160] for use with the diode Spice model [159].

determines the approximate range of impedances that the antenna needs to present over a broad frequency and input power density range for best rectification efficiency.

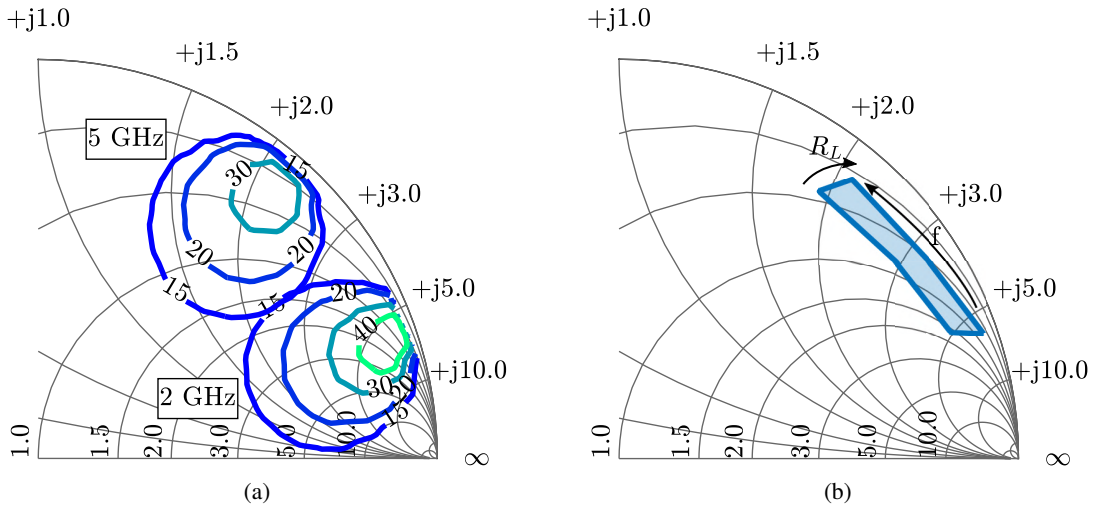


Figure 9.6: Simulated source-pull results showing (a) contours of constant rectified power (in μW) at 2 and 5 GHz with an input power and dc load of 100 μW and 2 kΩ, respectively. (b) Region of optimum impedance to present to the diode for peak dc output power, obtained using source-pull, showing the trend in frequency (f) and load (R_L). f is swept from 2 to 5 GHz while R_L goes from 500 to 3000 Ω and the input RF power is 100μW

Fig. 9.7 shows the rectified power vs. dc load for several incident powers close to the center of the band at 2.9 GHz. The frequency band under consideration for this work ranges from 2 to 5 GHz. At the lowest power level, the best rectification efficiency occurs for a 2-kΩ dc load. At increased power the best load is

around a few hundred ohms. A 2-kΩ load which is the best value for the lowest power level is therefore chosen. Efficient maximum power point tacking (MPPT) can be used to dynamically vary this load in a practical setting [161].

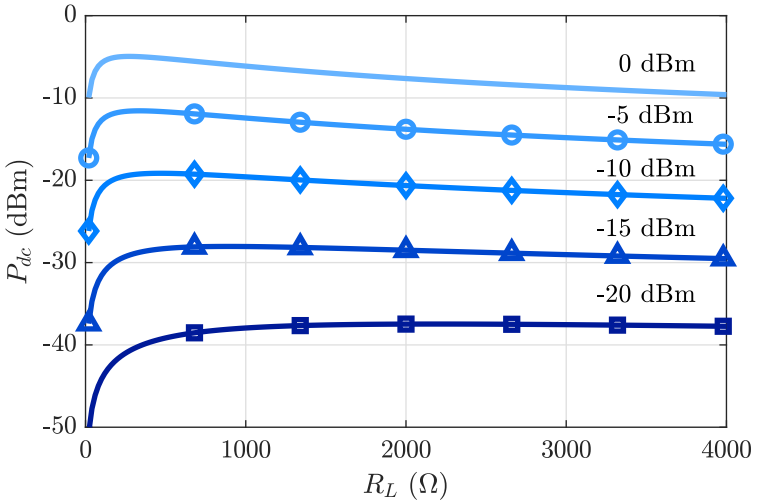


Figure 9.7: Simulated rectified dc output power vs. dc load resistance R_L for various RF input powers. The maximum occurs at around 2 kΩ at the lowest input power level.

9.3 Antenna Array Simulations

Because of the large incident power variation and broad bandwidth, a tightly coupled quasi self-complementary antenna array loaded with rectifiers is chosen with a period of $\lambda_0/6$ at 5 GHz, as shown in Fig. 9.1b. The diodes are connected to the antenna feed points in series along the co-polarized electric field vector and the rows are connected in parallel to the dc load. The antenna elements are tightly coupled in order to average out the variations across frequency ,power and shape, making the array an equivalent active impedance sheet. The antenna array is simulated using CST and several cases are compared. The general simulation geometry is shown in Fig. 9.8.

Results with 4×4 and 9×9 finite square arrays, of equal periodicity are shown. For wearable applications, the tee-shirt is placed on a realistic body torso tissue stack-up in the simulations, with a cross-section shown in Fig. 9.9a. Measurements are performed on a phantom for repeatability, so the simulations are also performed for the stackup of the water phantom, Fig. 9.9b.

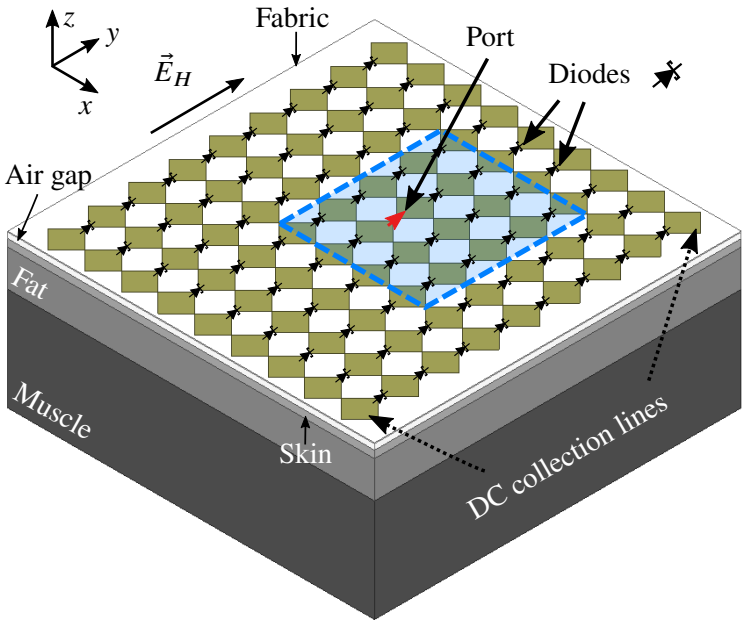


Figure 9.8: Simulation geometry for 9×9 array showing tissue stackup, orientation (horizontal polarization shown as $\vec{E}_H$), diodes in each element and main port for impedance and radiation pattern simulations. The 4×4 element sub-array is highlighted in dashed lines.

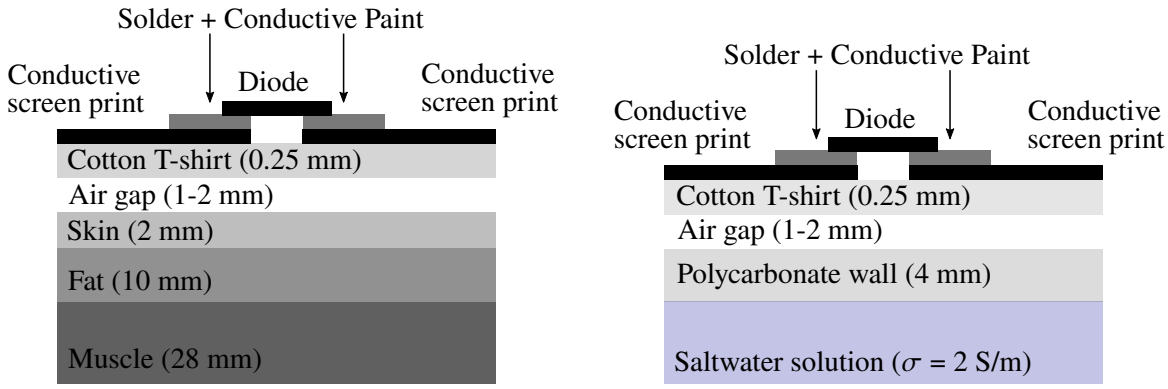
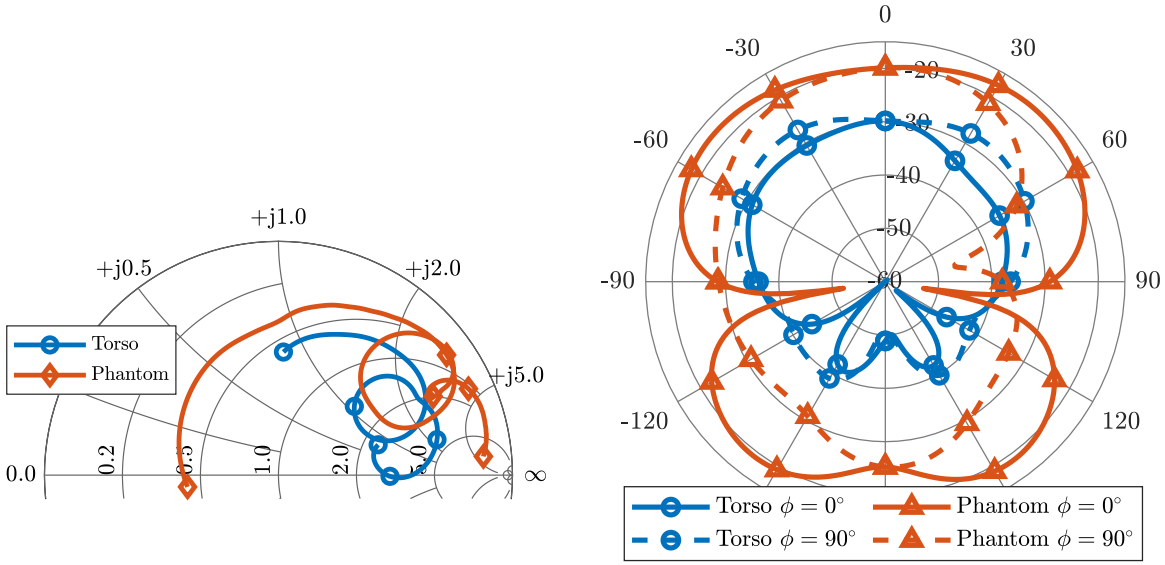


Figure 9.9: (a) Cross-section of realistic body tissue stackup with rectenna on tee-shirt placed on top of the model. The relative permittivities and conductivities of the skin, fat and muscle are 39.7, 5.4, 54.1 and 1.035, 0.064, 1.142 S/m, respectively, and are taken from [162]. (b) Stackup of the water phantom model used to aid in measurement repeatability.

The impedance and gain of the center element of a finite array on lossy tissues and phantom model are compared in Fig. 9.10. Fig. 9.10a displays the input impedance of a 4×4 element array simulated over a phantom and over a torso tissue stackup. The diode impedance is modeled from 2 to 5 GHz as a series RLC network where R=0.1 Ω, L=0.423 nH and C=0.27 pF. Note that the impedances for the center element of

the phantom and torso tissue stackup are not identical, but are in the same region of the Smith chart with a similar resonance, indicating that the phantom is a good qualitative model for this tissue stack-up. In Fig. 9.10b, the radiation patterns for these cases at 2.9 GHz are shown. The asymmetry of the radiation pattern is due to the offset position of the feed element in a 4×4 array, as indicated in dashed line in Fig. 9.8.



(a) (b)

Figure 9.10: Simulated results for the antenna with a single feed in the middle of a 16-element array and for two cases: on-phantom and on-body (skin, fat and muscle) with all other feed points terminated in the complex impedance of the diode. (a) Simulated antenna impedance seen at the port labeled in Fig. 9.8 from 2 to 5 GHz, (b) Antenna radiation pattern gain (realized) at 2.9 GHz.

Fig. 9.11 shows the driving-point impedance from 2-5 GHz of the middle element in the two finite arrays (4×4 and 9×9), an infinite array and a single element. In the case of the arrays, the plot shows the impedance of the driven element from Fig. 9.8, where the other elements are loaded with the input impedance of the diode. Note that the single element impedance is capacitive and consistent with that of a thick dipole, while the impedance of the arrays is significantly different, due to the electrically-small period that results in tight coupling. Also note that the impedance of the larger array is closer to that of the infinite array, as expected.

Fig. 9.12 shows the simulated gain patterns for a 4×4 array on cotton above a torso tissue stack-up with a 1-mm air layer between the shirt and skin. The center element is fed, while the remaining elements are terminated in the diode impedance. The patterns are shown for three frequencies across the band. The

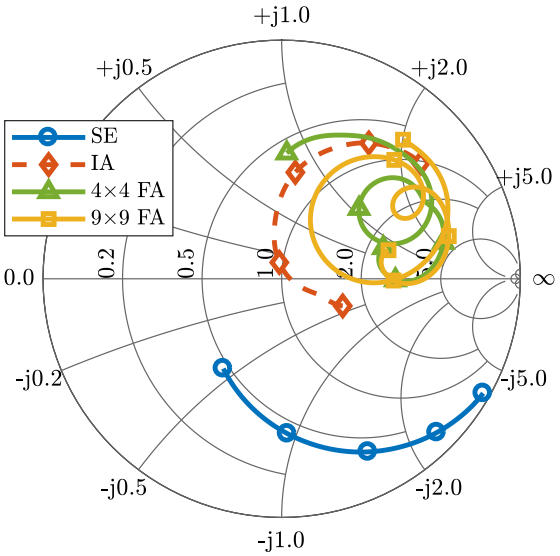


Figure 9.11: Driving-point impedance for a single element (SE), an infinite array (IA) and two finite arrays (FA) of 4×4 and 9×9 elements over a torso with air gap h =1 mm. Each element is loaded with the complex impedance of the diode and the array impedance is for the center element. The frequency is swept from 2 to 5 GHz.

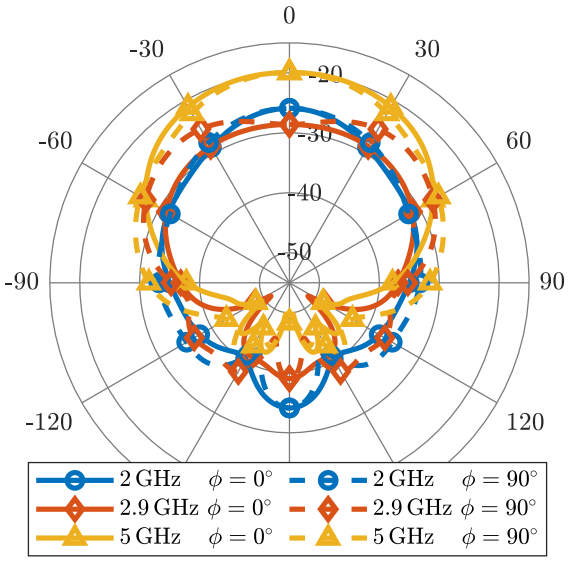
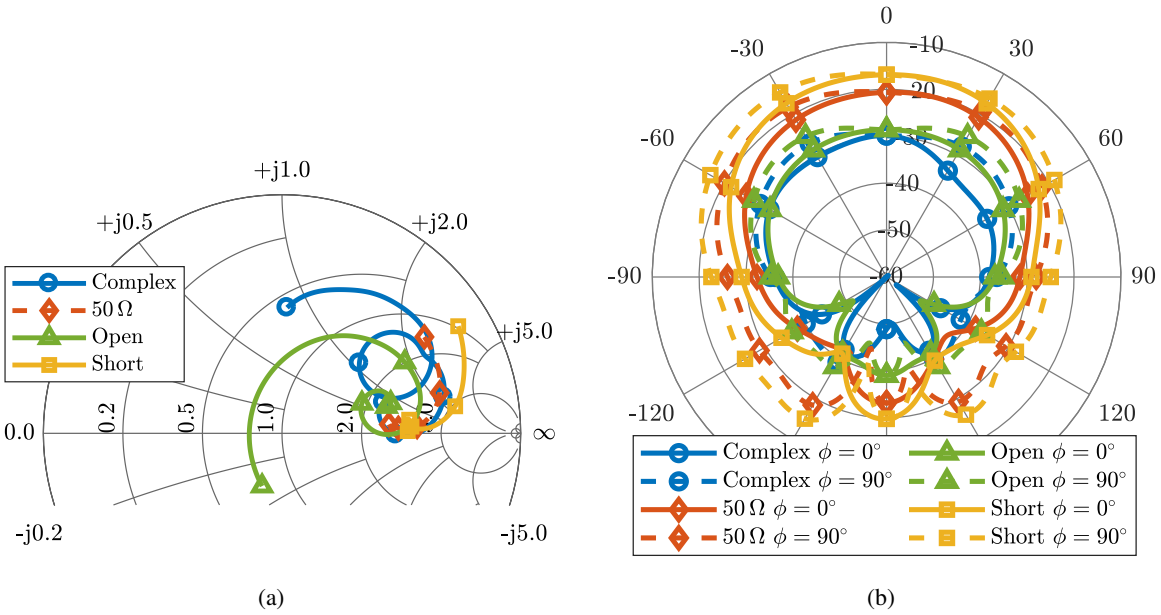


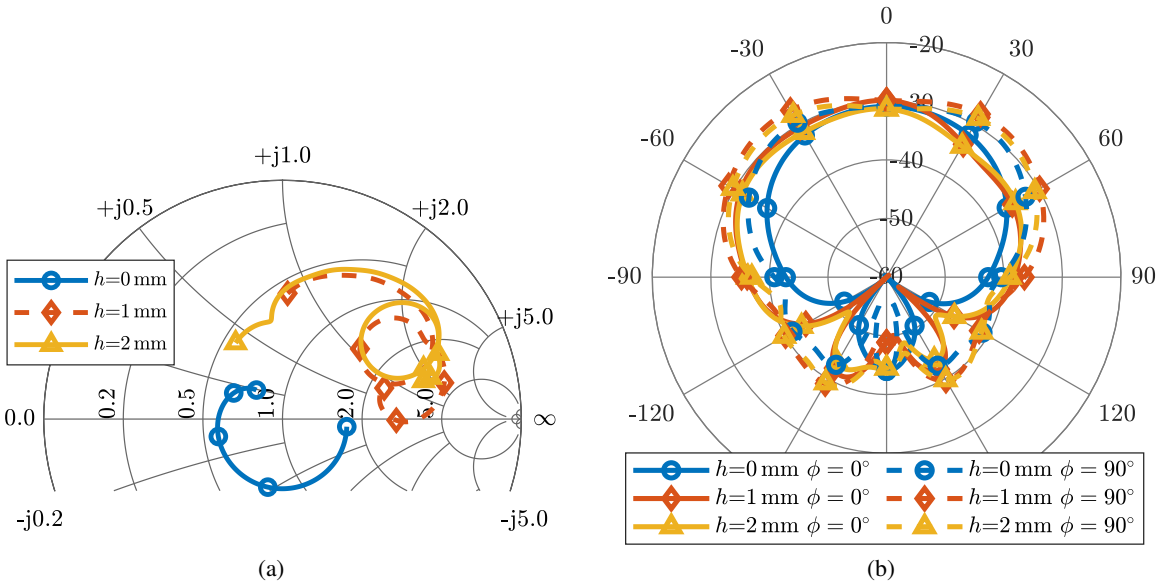
Figure 9.12: Simulated co-polarized (ϕ=0°) and cross-polarized (ϕ=90°) gain patterns (realized) for the 4×4 array on cotton above an air layer of 1 mm and torso tissue stackup. The center element is fed, while the remaining elements are terminated in the diode impedance.

highest gain is observed at the upper end of the band where the coupling is the weakest. Back radiation is greater at lower frequencies due to the electrical dimension of the finite substrate and tissue stackup.



(a) (b)

Figure 9.13: Simulation results of a 4×4 array over a torso with a 1-mm air gap between the cotton and skin layers, with various port terminations. (a) Input impedance looking into a single port (as shown in Fig. 9.8) from 2-5 GHz and (b) radiation pattern gain (realized) at 2.9 GHz.



(a) (b)

Figure 9.14: Simulation results of a 4×4 array over a torso loaded with the complex impedance of the diode for various air gaps (h). (a) Input impedance looking into a single port (as shown in Fig. 9.8) from 2-5 GHz and (b) radiation pattern gain (realized) at 2.9 GHz.

Fig. 9.13 shows the input impedance and radiation pattern of a 4×4 array over a torso with 1-mm air gap for various terminations on the other ports, in this case an open, short, 50 Ω load and the complex impedance of the diode. The short and 50 Ω terminations produce similar results because the 50 Ω loads are a small impedance and closer to the short than to the diode and antenna impedance magnitudes, which are in the hundred ohm range. Likewise, the open and diode impedances produce similar results in both impedance and radiation pattern. The different terminations are included in order to point out the impact of port terminations in a tightly-coupled array. The complex diode impedance terminations are the most appropriate to use in this case, although they are incident-power, frequency and load dependent as shown in Fig. 9.6b.

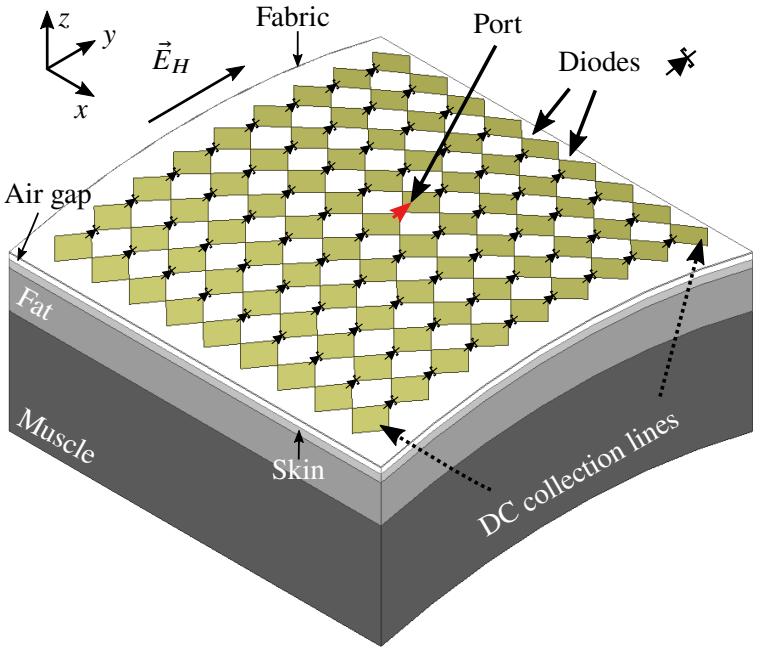


Figure 9.15: Simulation geometry for a curved 9×9 array showing tissue stackup, orientation (horizontal polarization shown as $\vec{E}_H$), diodes in each element and main port for impedance and radiation pattern simulations. The array is deformed in a cylindrical manner with the axis along the x direction, a radius of curvature of 319 mm and a 30° angle.

Since clothing tends to be loose, the spacing between the cotton tee-shirt and skin will vary in general. The impedance and pattern dependence on the thickness of the air layer is examined as a first-order approximation to real-world behavior. Fig. 9.14 shows the simulated input impedance and radiation pattern of the same array as Fig. 9.13 with varying air gap (h). The performance of the array does not vary much from 1 to 2 mm

but it does change when the gap is reduced or disappears. This suggests that on materials such as fleece or other thicker fabrics, the variation would not be noticeable.

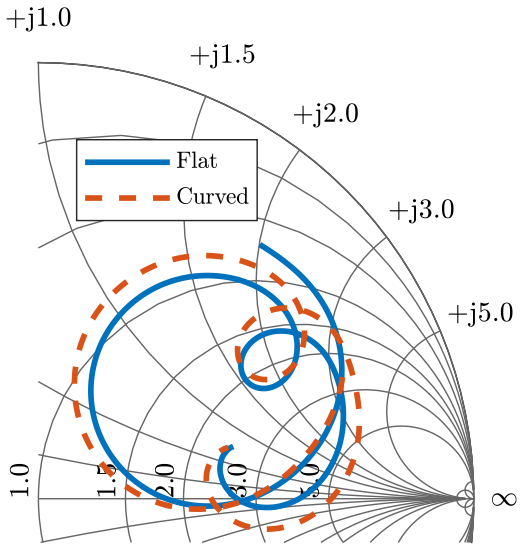


Figure 9.16: Comparison of input impedance looking into a single port (as shown in Fig. 9.15) from 2-5 GHz for flat and curved arrays when the rest of the elements are loaded with the diode complex impedance.

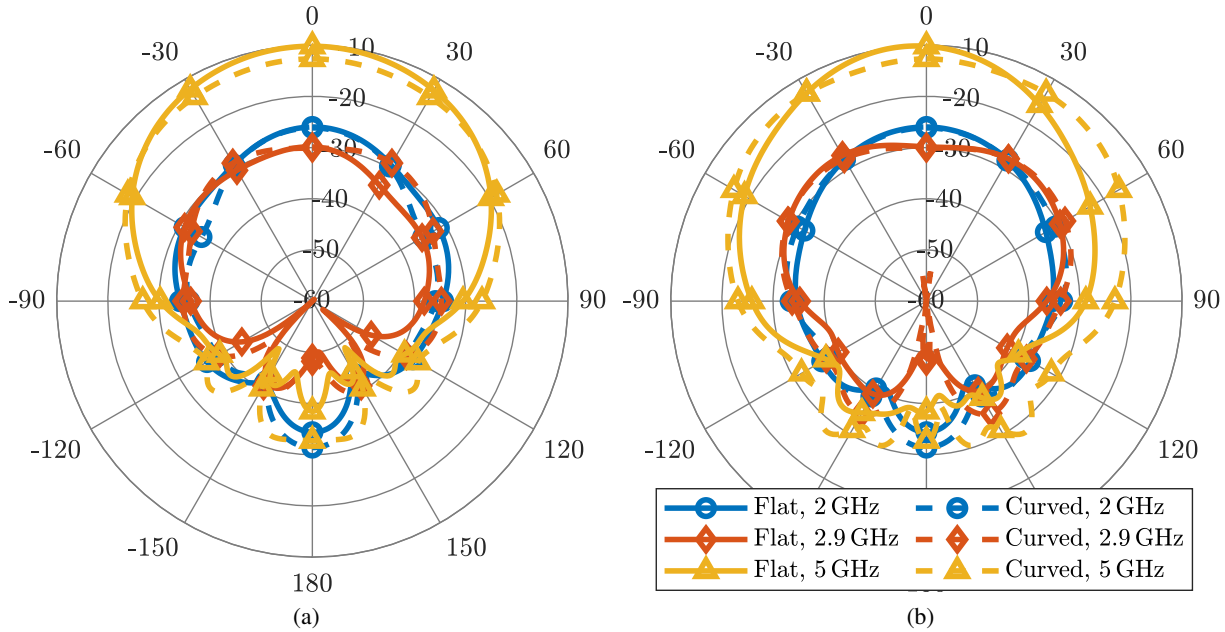


Figure 9.17: Comparison of realized gain for a flat and a curved array. (a) Co-polarized (ϕ=0°) and (b) cross-polarized (ϕ=90°).

Another practical consideration is the effect of curvature of various parts of the body. A simulation of the rectenna curved with a radius of 319 mm extending over 30° is performed for the 9×9 array with a 1 mm air gap, as illustrated in Fig. 9.15. The resulting driving-point impedance of the center element, with complex loads terminating the rest of the ports, is shown in Fig. 9.16. The radiation pattern comparisons are shown in Fig. 9.17. Only a small shift in performance is seen, and the curved array has more side radiation with a small reduction in the main lobe maximum.

9.4 Implementation and Measurements

To implement the bow-tie array on wearable material, metallized ink (NovaCentrix Metalon HPS-FG57B) is deposited on a cotton tee-shirt using standard screen printing [163] methods. The surface-mount diode package (SC-79) proved difficult to attach to the conductive ink using solely solder or conductive epoxy. An adhesion method was developed which utilizes conductive silver paint that was then soldered to following curing of the paint. The temperature of the soldering iron was maintained at 375°C during this process. The surface resistance of the silver paint is $0.01\,\Omega/\square$, which maintains greater performance in terms of repeatability and low resistance due to lower viscosity of the paint compared to that of conductive epoxy.

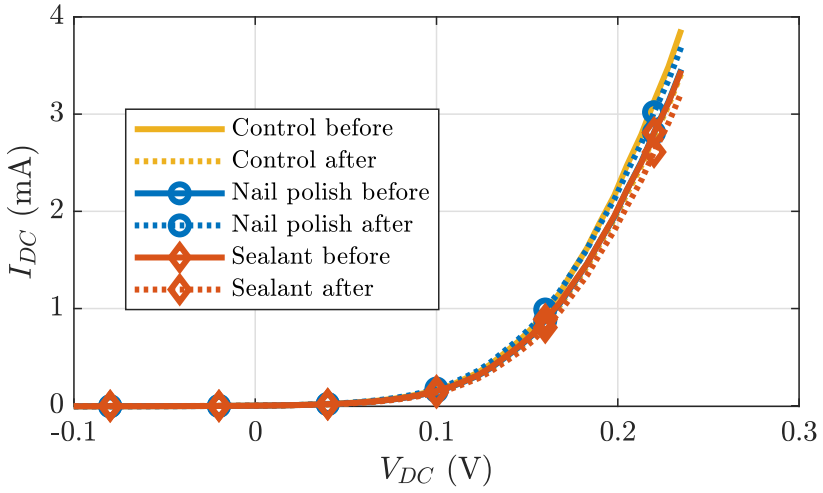


Figure 9.18: Comparison of IV curves for different treatments before and after hand-washing.

To investigate effects of fabric washing, three diodes were mounted in unit cells on a different Tee-shirt and without connections between them. One was then covered with nail polish and a second one with fixative

spray for pastels and charcoal drawings (by Grumbacher). Both materials are resistant to washing. The IV curves of all three diodes were measured before and after hand-washing in water and there was no observable change in dc electrical characteristics, Fig. 9.18.

Figure 9.19: Photo of tee-shirt on phantom in the anechoic chamber during measurements, with the phantom shown on the bottom right. A detail of a fabricated single array element is shown on the upper right.

A 4×4 array was initially populated with diodes and characterized and then expanded to a 9×9 array. The rectenna is first characterized on a phantom body using a container of saline solution. The conductivity of the solution is taken to be the weighted average of the human tissues at 2.9 GHz as given in [162], with the cross-section of the setup shown in Fig. 9.9b. The photo in Fig. 9.19 shows the setup in the anechoic chamber, detail of the phantom, as well as detail of a single array element.

The rectenna arrays are characterized in an anechoic chamber using the setup sketched in Fig. 9.20 where the tee-shirt is mounted on the phantom and the dc output is connected to a variable load. A power calibration is performed up to the plane of the transmit antenna to determine incident power on the transmit antenna as a function of RF source power and frequency. The incident power density on the rectenna array is then estimated with a well-characterized linearly-polarized transmit antenna using Friis' line-of-sight equation. The energy harvester and transmit antenna are in each other's far fields at the lowest frequency of interest

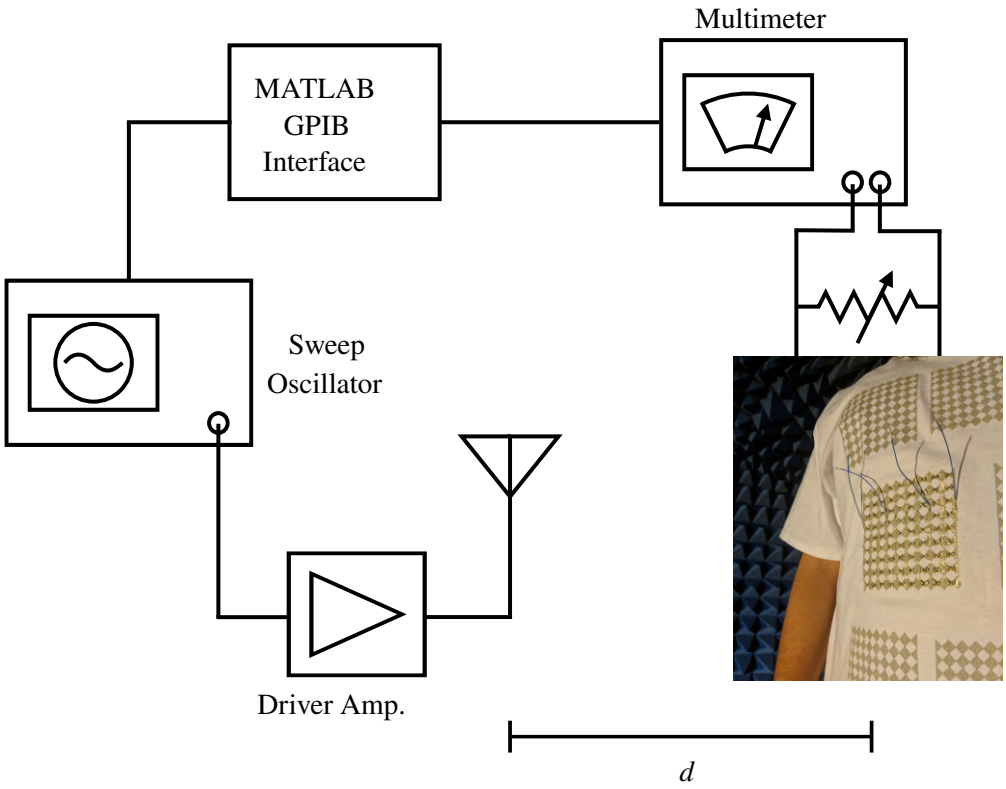
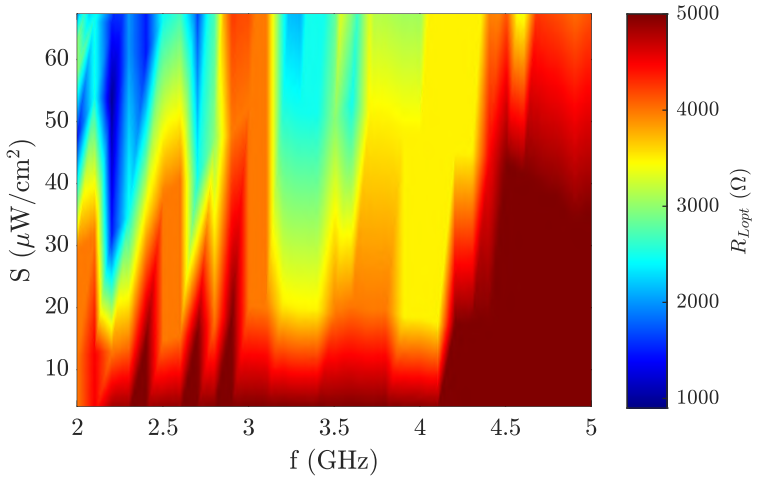


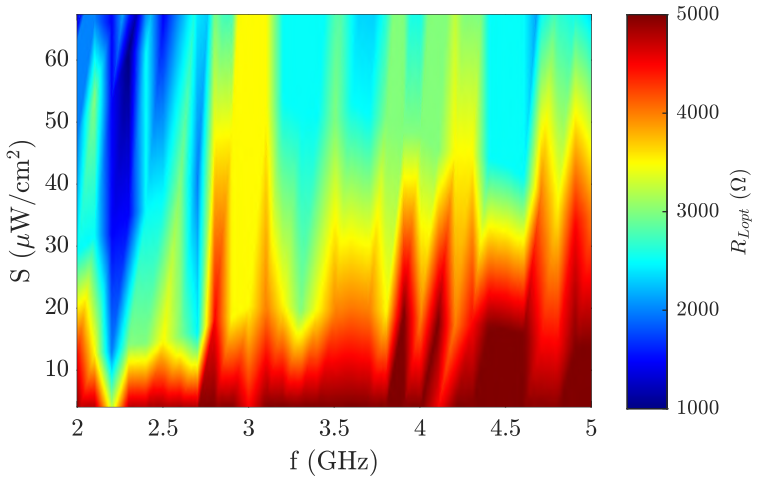
Figure 9.20: Measurement setup, $d = 69\,\text{cm}$. The tee-shirt is measured inside of an anechoic chamber in several configurations: mounted in air (free space), on a phantom, and while being worn (on-body). The calculated far-field distance, d_f, is approximately 26 cm at 2 GHz.

($d = 69\,\text{cm}$). The power available at the antenna port is calibrated and the resulting power density incident on the rectenna array is varied from $3\,\mu\text{W/cm}^2$ to $130\,\mu\text{W/cm}^2$ at each frequency point between 2 and 5 GHz in 100-MHz steps.

The dc load is varied between $100\,\Omega$ and $5\,\text{k}\Omega$. The dc power is measured as a function of frequency, incident power density, and dc load. Results showing the optimal load resistances for both polarizations are shown in Fig. 9.21. It is seen that for lower power levels, the optimal load is large. Additionally, the load is different for the two polarizations, which is related to the antenna gain. Importantly, we observe that the power is not very sensitive to the load resistance. The extensive characterization as a function of dc load is important information for design of the power management circuit, which is typically based on a boost converter that emulates the optimal load over various power levels, as in [155]. Although here we do not focus on the power management, all relevant rectenna array characterization is performed and presented, and previously published approaches, e.g.[164], can be directly applied.



(a)



(b)

Figure 9.21: Optimum load resistance for the 81-element array in (a) vertical and (b) horizontal polarization.

Fig. 9.22 displays measured results for 16-element and 81-element bow-tie rectenna arrays for the two polarizations and as a function of frequency with and without the body phantom. Output dc voltage, V_{DC}, and power, P_{DC}, were measured using a multimeter placed in parallel with a variable resistive load connected to the rectenna array. As expected, the phantom does not significantly affect the rectified power level due to the air gap and container thickness which reduce loading by the saline. Second, the horizontal polarization (referring to Fig. 9.22a) gives a higher dc output, as expected from the radiation pattern. Third, the 81-element array does not produce significantly higher power compared to the smaller array. It is believed that the efficiency drops due to the relatively high dc resistivity of the conductive ink, which becomes more

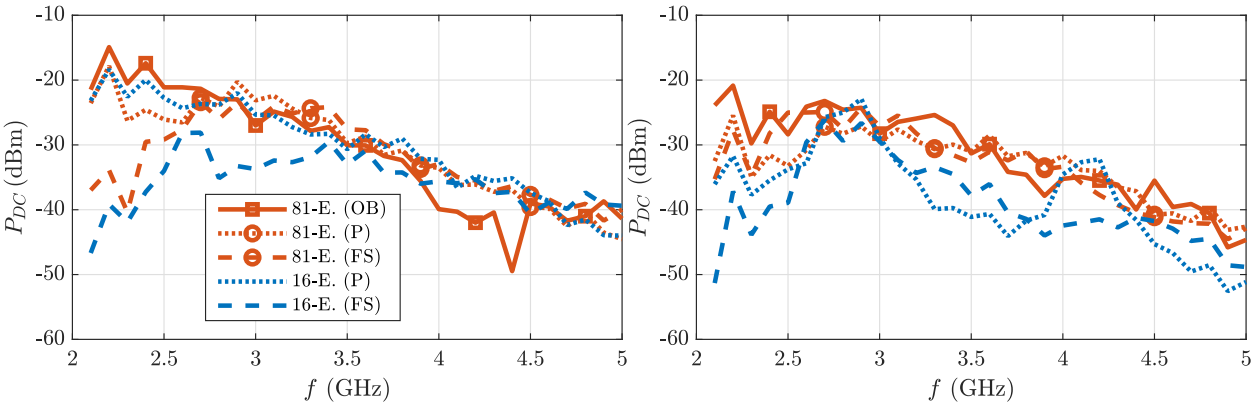


Figure 9.22: Rectified DC power vs. frequency for the 16 and 81-element arrays measured on-body (OB), with a phantom (P) and in free space (FS) for both (a) horizontal and (b) vertical polarization. The incident power density is 4 μW/cm^2 and DC load is 2 kΩ.

dominant as the array is scaled up in size. Conversion efficiency is defined as:

$$\eta = \frac{P_{DC}}{S(0°, 0°) \cdot A}$$

where A is the geometric area of the arrays, which results in a conservative efficiency estimate. Fig. 9.23 shows the comparison between the two arrays for both polarizations. This indicates that in terms of efficiency, it is better to combine the power of several small arrays than to create a single large array. Fig. 9.24 shows dc output voltages for various power densities, polarizations, and array sizes.

9.5 Chapter Summary

This Chapter presents 16- and 81-element broadband bow-tie rectenna arrays screen printed on a cotton tee-shirt for harvesting 4-130 μW/cm^2 power densities between 2 and 5 GHz. Source-pull diode simulations over a large range of dc resistances and input powers are performed to predict rectifier impedance. It is found that for lower input power levels, a larger dc load gives better efficiency. Full-wave antenna simulations are performed with specific tissue electrical parameters for the torso, as well as for a body phantom. The tightly coupled array is investigated as a function of finite size, port terminations, and separation of fabric above body. When the input impedance is simulated for the center element of a finite array, it is found that

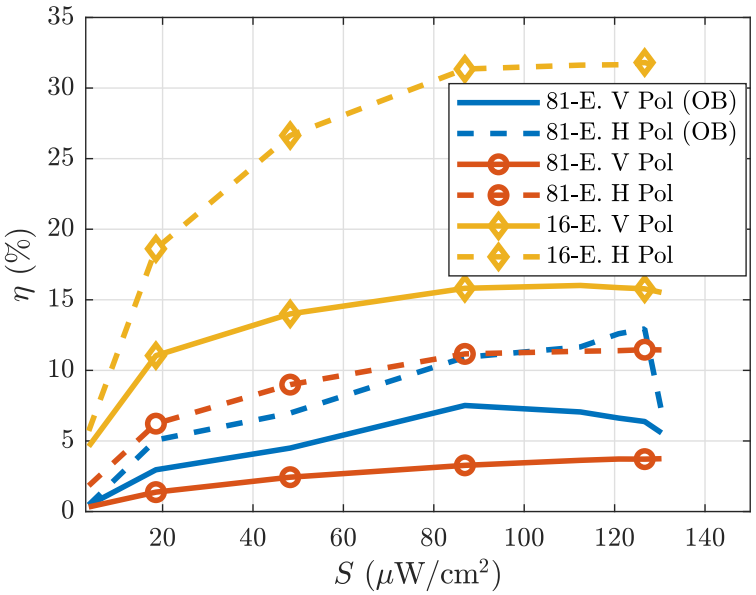


Figure 9.23: Measurement results of efficiency vs. incident power density at 2.9 GHz with a dc load of 2 kΩ, showing that the fairly large resistance of the conductive ink reduces efficiency for larger arrays. On-body (OB) and on-phantom measurements are shown.

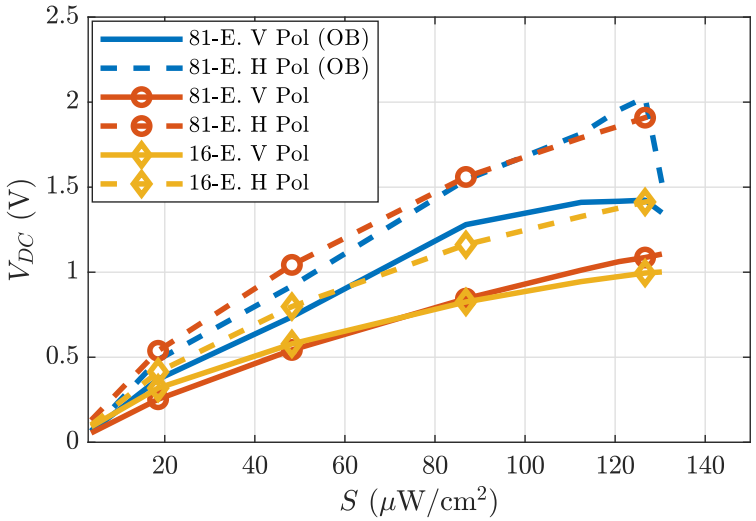


Figure 9.24: Output DC voltage vs. incident power density at 2.9 GHz with a dc load of 2 kΩ. On-body (OB) and on-phantom measurements are shown.

the rectifier diode complex impedance termination of all other ports results in the best match to the diode source-pull impedance. For air gaps between the fabric and skin larger than 1 mm, there is little variation in the impedance and radiation pattern. Additionally, simulations are performed for arrays with body curvature taken into account, showing small changes in performance.

It is found that screen printing on fabric with conductive ink can be used for functional rectenna array harvesters, despite the fairly large surface resistance of the ink. Silver paint was found to be a reliable method for connecting surface-mount diodes to a conductive fabric substrate and is shown to withstand hand-washing in water. Measurements using a saline-filled phantom show up to $P_{DC} = 32\,\mu$W for incident power densities of $4\,\mu$W/cm^2, with a dc load of $R_{DC} = 2\,$kΩ. The measurements on the phantom compare well with those obtained with the tee-shirt rectenna worn on an actual body. For low incident power densities the efficiency is in the 5-10% range, and reaches 32% for $100\,\mu$W/cm^2. Although the bow-tie array is the same for two linear polarizations, the diode orientation gives a preferred polarization, which is clearly seen in simulations and measurements. This approach can be extended to dual polarization by adding diodes to the remaining feedpoints. The contributions in this Chapter are reported in [165, 166].

Chapter 10

Contributions and Future Work

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The main contributions of Part I of this thesis are the development of a new methodology for filter design with complex ports (Chapters 2 and 3), demonstration of the methodology applied to co-design of filters and power amplifiers in both hybrid (Chapter 4) and MMIC (Chapter 5) forms, and co-design of RF front end components for heterogeneous integration (Chapter 6). The goal of these contributions is reduction of the footprint and improvement of overall circuit and component performance. Some of the key performance enhancements include: reduced loss, reduced footprint, increased available characteristic impedances, and improved efficiency and gain through thermal management.

Part II develops various methods for wireless transfer of energy. Starting with the development of a near-field phased array of capacitive wireless power transfer modules meant to transfer kilowatt level power with safe fringing electric field intensity for human exposition (Chapter 7). The main contribution in that work is the development of the multi-module approach for harmful field reduction. Various methods for energy

harvesting are also described, narrowband energy harvesting for airplane altimeter radar power recycling (Chapter 8), demonstrating sufficient power to energize low power sensors, and broadband wearable energy harvesting (Chapter 9), showing wide band harvesting capabilities using screen printed wearable rectennas.

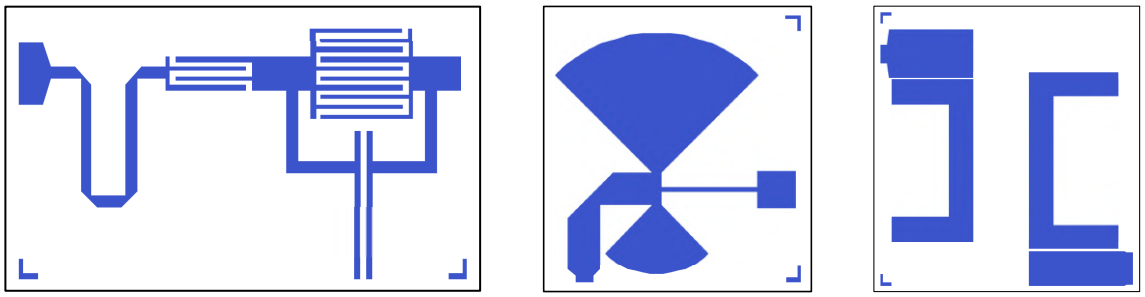
10.1 Future Work

There are several obvious extensions of the research described here, and in the context of the front end introduced in Chapter 1. For example, the MECA process can be used to integrate a transistor with high-quality passives for a quasi-FPA. This facilitates additional component integration in the front and back ends of an RF system. The GaAs MMIC FPA approach can be easily extended to a design of a low-noise amplifier (LNA) integrated with filtering. Additional extensions include optimization of insertion loss of an amplifier-filter cascade, extensions of complex-port impedance filter theory to a broadband case and control of impedance at the harmonics, as well as extensions to multiport filter networks (e.g. diplexers and multiplexers), described in Subsection 10.1.4.

10.1.1 MECA FPA

An FPA can be designed using heterogeneous integration which is here referred to as "quasi-MMIC" amplifier, as the ones discussed in [23, 24, 25]. In this case, only the transistor is a compound semiconductor component while the passive part of the amplifier circuit is implemented in a lower-loss and less expensive substrate. The reduced compound semiconductor real state provides reduced cost of components and the use of high performing integrated passive devices (IPDs) for the passive part of the PA gives improved performance. In Chapter 6 integration of GaN and Alumina chips was demonstrated and this shows a path to designing a quasi-MMIC FPA and it is explored in this Section.

The MECA-FPA design is performed using a Qorvo GaN bare die transistor (TGF2941) with output matching filter, input matching network and biasing networks designed in Alumina. It is designed for operation at 24 GHz with 3 % bandwidth and a second order filter as the output matching network. The design is similar to the one presented in Chapter 5. The optimum impedance for maximum power added



(a) (b) (c)

Figure 10.1: Layouts of the passive Alumina components of the MECA-FPA including (a) input matching network and RC stability tank (2×1.2 mm), (b) biasing network (1.4×1.5 mm), and (c) output matching filter (2.1×2.3 mm).

efficiency (PAE) is obtained through load-pull simulations using a Modelithics transistor model. The input of the FPA is conjugately matched for amplifier gain. The biasing is designed using radial stubs and ceramic capacitors. Fig. 10.1 shows the various components of the FPA.

The input matching network (IMN) also has an RC tank formed with an interdigitated capacitor and surface resistor for FPA stability. The interconnects were EM modeled using Ansys HFSS and were taken into account during load pull, stability design, to finalize the biasing design and to ensure appropriate second harmonic termination. The width and length of the interconnects provides and extra design tool. Fig. 10.2 displays the MECA-FPA layout with all the components and MECA interconnects that form it.

The simulated small signal performance of the FPA is shown in Fig. 10.3 where a small signal gain of 7.4 dB can be observed. The output match is more than 7 dBm across the band, the degradation of output match is caused by the non-conjugate match at the output. The large-signal performance of the MECA-FPA can be seen in Fig. 10.4 and the large-signal behavior as a function of frequency of the MECA-FPA is shown in Fig. 10.5 for three different power levels. The peak PAE achieved is 23 % at 24 GHz with a saturated gain of 5.8 dB and the output power is above 30 dBm from 23.65 GHz to 24.4 GHz for an input power of 26 dBm.

10.1.2 Dual-Mode Resonator MECA Filter

The output matching filter shown in the previous Section is very similar to the one in the MMIC-FPA presented in Chapter 5 and for that reason the performance will be comparable. The MECA process provides

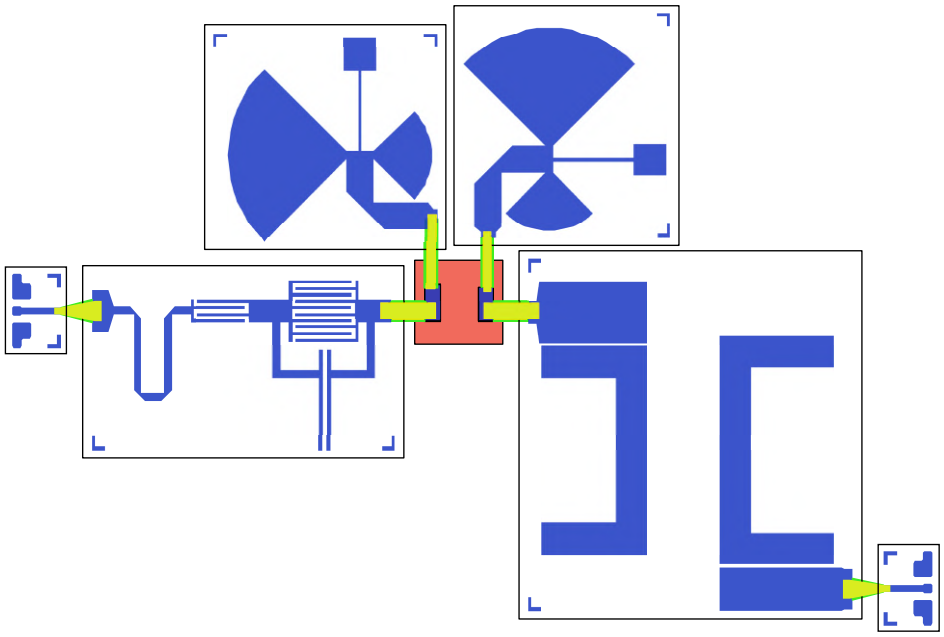


Figure 10.2: MECA-FPA layout showing the TGF2941 transistor in red at the center, passive components from Fig. 10.1, GSG launchers (for on-wafer probing) and MECA interconnects in yellow with green BCB.

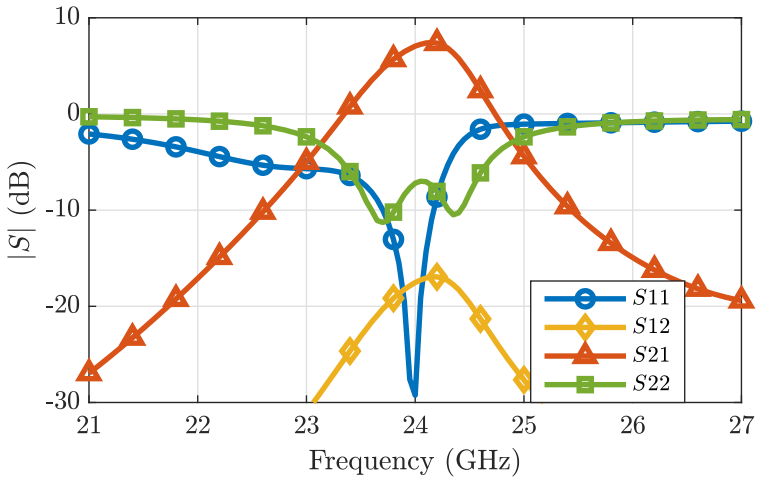


Figure 10.3: Simulated small-signal S-parameters of the MECA-FPA from Fig. 10.2. The frequency selectivity is seen from $|S_{21}|$, $|S_{11}|$ and $|S_{22}|$. Rejection is aided by the frequency selectivity of the input matching network, the resulting roll-off is steeper than the one provided by the 2^{nd}-order Chebyshev OMF.

the opportunity to design filters using other types of resonators than the microstrip ones that are the only available ones in a MMIC design. If larger sizes are allowed one can implement cavity resonators in the MECA process, similar to the "pizza box" resonators in [167, 168]. These resonators can be implemented by embedding rectangular pieces of substrate in MECA and later covering the top with the metal interconnect layer part of the process.

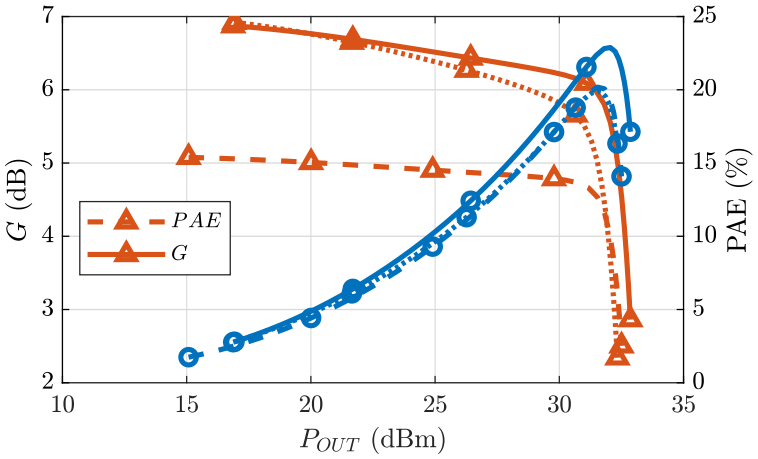


Figure 10.4: MECA-FPA large-signal simulations as a function of output power. The traces are shown for three different frequencies: 23.75 GHz (dashed), 24 GHz (solid) and 24.25 GHz (dotted).

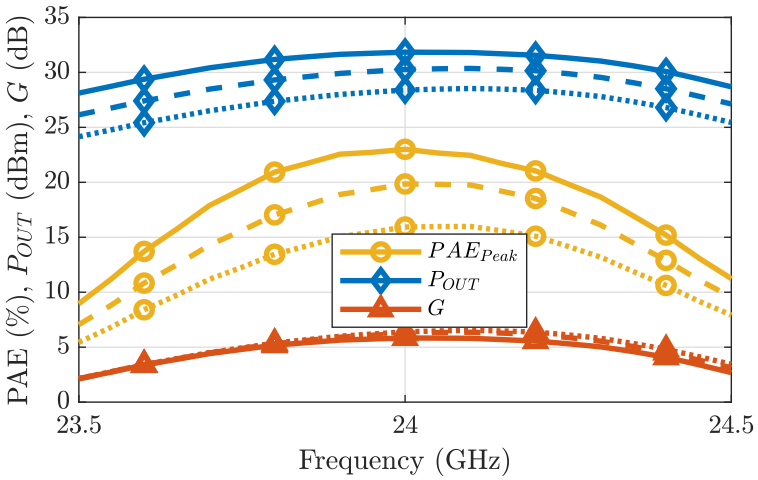
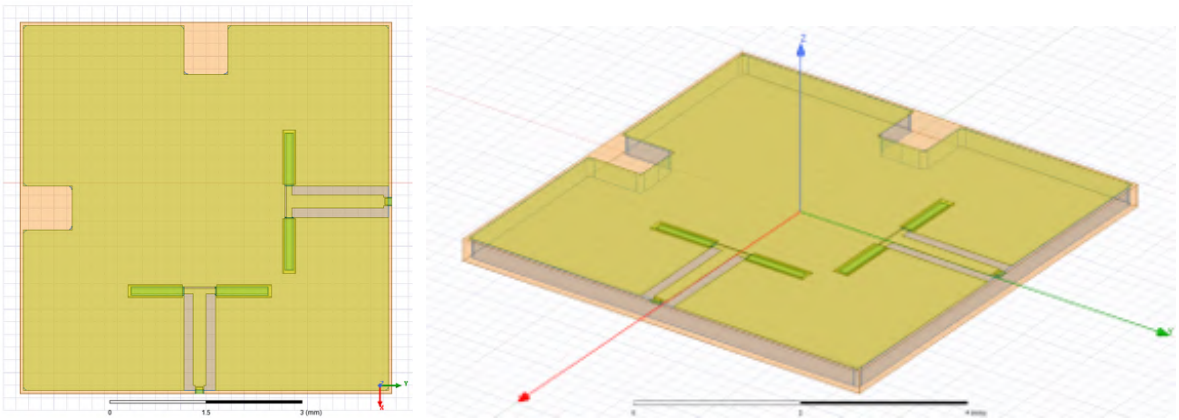


Figure 10.5: MECA-FPA large-signal simulations as a function of frequency. The traces are shown for three different input power levels: 22 dBm (dotted), 24 dBm (dashed) and 26 dBm (solid).

A filter is designed in an Alumina substrate and in a similar fashion as the rectangular dual-mode resonator filters described in [169, 170]. The dual-mode resonators provides additional size reduction by implementing two resonators in the same physical space. These can also be strategically cascaded for higher order filter responses. Fig. 10.6 shows the filter model where it can be seen that the input and output couplings are implemented with dipole probes and the coupling between the modes are realized through the notches on the sides opposite to the input and output ports. There is also an additional coupling from the source to the load (m_{SL}).

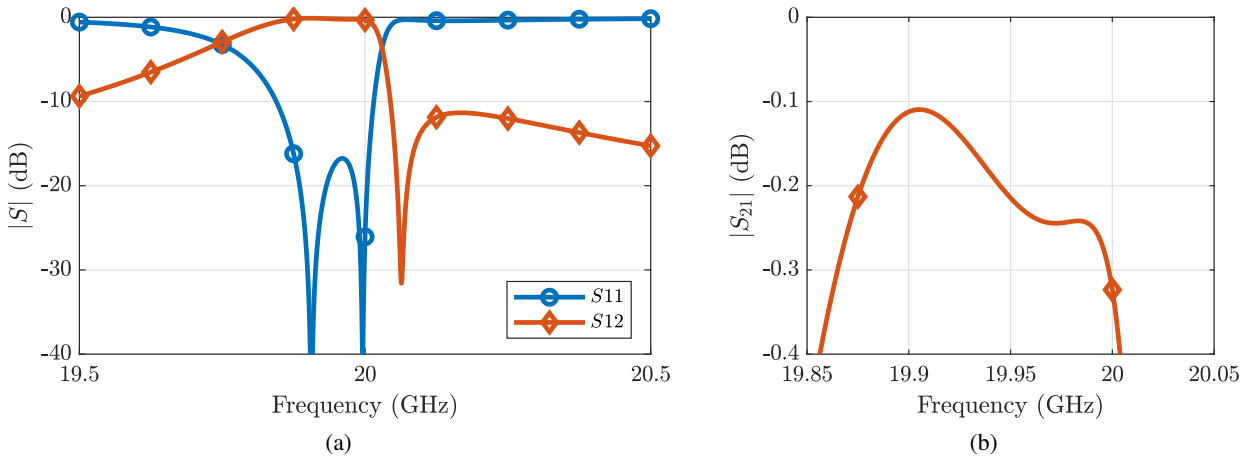
The filter is simulated using Ansys HFSS and the simulated frequency response of the filter can be seen



(a) (b)

Figure 10.6: (a) Top and (b) angled view of the MECA dual-mode rectangular cavity resonator filter showing the input and output probes as well as the side notches that couple the two resonating modes.

in Fig. 10.7. The existence of a source-to-load coupling conveniently incorporates a transmission zero to the frequency response. The simulations predict resonating modes with quality factors above 10000 which lead to the very low insertion loss seen in Fig. 10.7. This filter can be designed to work as a matching network for a frequency-selective high-efficiency FPA.



(a) (b)

Figure 10.7: Simulated S-parameters of the designed dual-mode rectangular cavity resonator filter from Fig. 10.6. (a) Broadband response and (b) zoom into S_{21} in the passband showing the very low insertion loss of the filter.

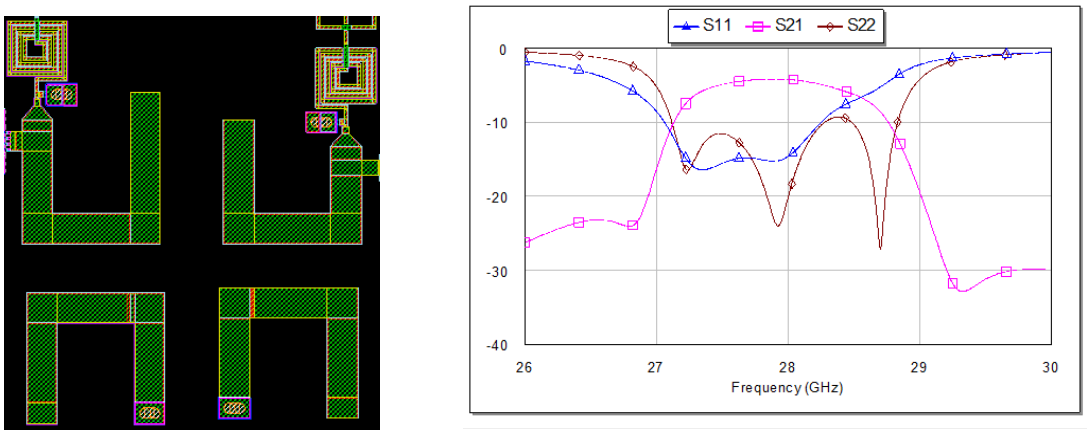
10.1.3 Filter Integrated with LNA

Integration of filters and LNAs is a direct extension of the work carried out in this thesis with power amplifiers (PA). In amplifiers the filtering is mostly done at the output to guarantee a filtered and clean output signal. For PAs this means that the loss in the filter can have a significant impact in the power added efficiency (PAE) of the amplifier, as explained in Subsection 4.1. For an LNA, a low-loss input matching network is critical to maintaining the lowest possible noise figure. The total noise factor of a cascade of amplifiers and other components is given by the Friis formula

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{10.1}$$

where F_i and G_i are the noise factors and available power gains if the i-th stages of the cascade, respectively. Since a lossy filter has a gain smaller than unity, a filter at the input of an amplifier can significantly reduce the noise factor. However, an output matching filter of the first LNA stage does not require the strict low loss performance that a PA demands for maintaining good PAE and can be implemented without substantially damaging the noise figure. Furthermore, the filter loss is compensated by LNA gain, which already must be large to guarantee small degradation of the noise figure. Additionally LNAs are conjugately matched in small signal at the output, which is better suited to filter integration. Namely, it has less potential to degrade the filter's frequency response, which could be matched to the LNA's output transistor and the $50\,\Omega$ output port impedance.

A proposed Filter-LNA (FLNA) MMIC was designed to serve as an initial step towards a full FLNA design. The designed FLNA uses a fourth order filter inspired by the one in Subsection 2.2.2 as an interstage matching network between the second to last and last stage of the LNA. The final stage of the FLNA is a gain stage and therefore it is conjugately matched on both ports. The simultaneous conjugate match prevents degradation of the filter response. The filter is shown in Fig. 10.8a, where it can be seen that the filter acts as the matching network between the two complex impedances required by the transistors' drain and gate. The filter also incorporates the biasing, on the filter sides, of both transistors connected through the interstage matching filter. The lack of electrical connection between input and output naturally provides a DC block between the transistors. The shorts in both input and output resonators can be implemented with an LC



(a) (b)

Figure 10.8: Filter for the FLNA. (a) layout and (b) frequency response.

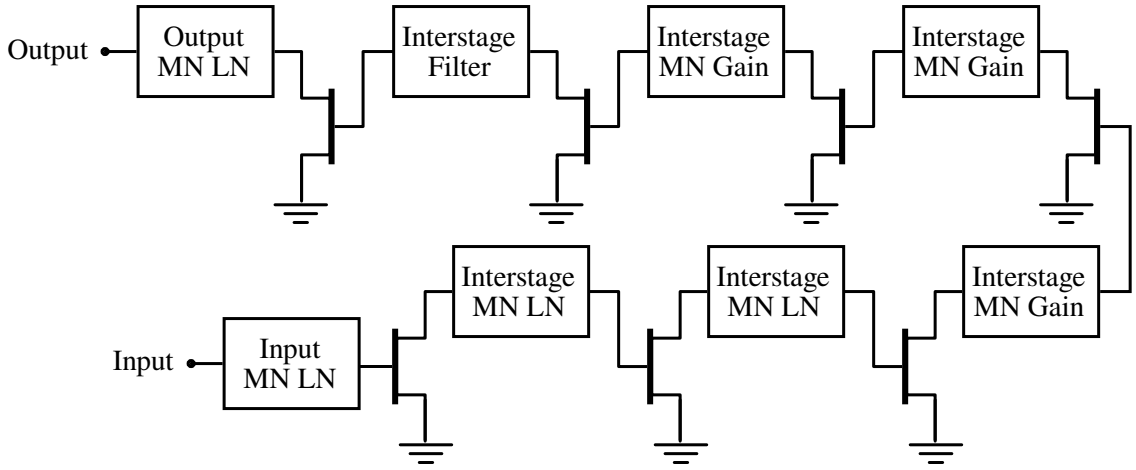
network that presents a virtual short and acts as an RF choke. Fig. 10.8b shows the simulated performance of the filter.

The full FLNA is shown in Fig. 10.9. The first three stages are designed to have low noise factor and ensure a low total noise figure. The other stages provide additional gain. An electric wall made from vias is placed to reduce coupling from input and output and avoid oscillations. The MMIC was designed in WIN Semiconductor's 150-nm GaAs PIH1-10 enhancement-mode HEMT process. This design serves as a simple demonstration of co-design, but is expected to be unstable due to the very high gain and proximity of the LNA stages in the die layout. However, with careful simulations and stability analysis, the same approach can be followed to implement a LNA with frequency-selective low-noise performance.

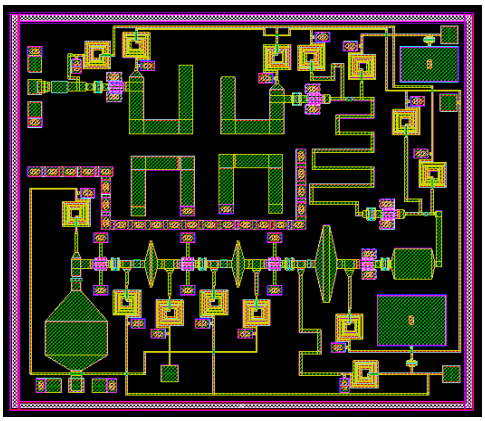
10.1.4 Other Future Challenges

Some extra challenges remain to be tackled and represent straightforward extensions to the work done in this thesis, the main ones being:

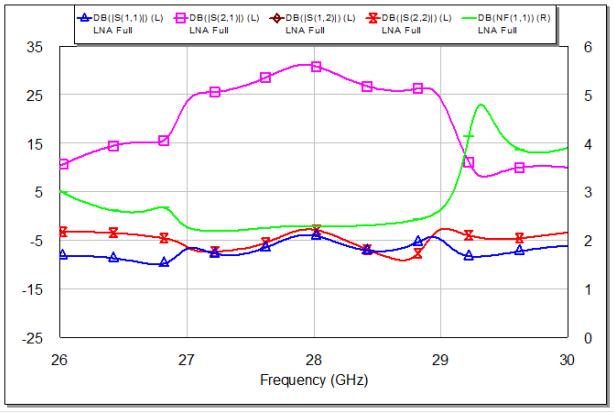
- The work presented here only deals with narrowband designs and the technique assumes a fixed and constant complex impedance at the port. However, for broadband circuits (e.g. PAs), the impedance varies across the band and a different strategy is needed. Fig.10.10a shows the load-pull simulations for a discrete transistor device, where it can be seen that a constant impedance approach is insufficient



(a)



(b)



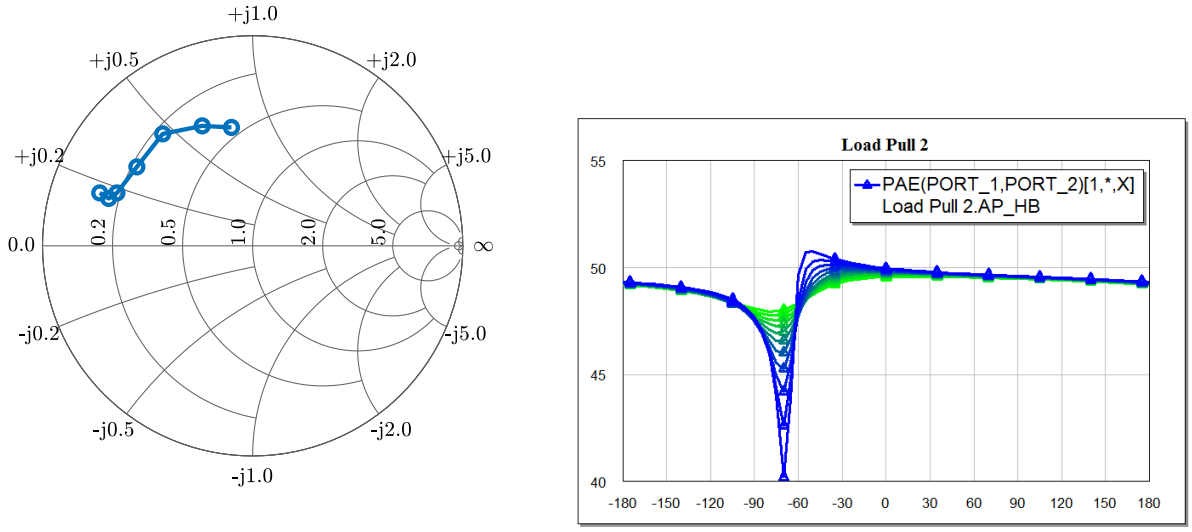
(c)

Figure 10.9: MMIC FLNA: (a) schematic, (a) layout and (b) small signal frequency response.

for properly matching this transistor across the whole band (3 to 6 GHz in this case). An approach for broadband FPA design is currently being investigated.

- In this work the harmonic terminations for efficiency enhancement of the FPA are co-designed into the biasing network of the FPA. Incorporating this feature to the filter design itself would increase the integration and possibly reduce size of the FPA. Fig. 10.10b illustrates the impact of the second harmonic on the efficiency of a PA, it can be seen that up to 10% points of PAE can be controlled using second harmonic termination.

- The impact of the output filter in PA efficiency is a consequence of the insertion loss of the filter. The use of higher quality factor resonators was mentioned as a straightforward way of improving



(a) (b)

Figure 10.10: (a) Broadband PAE load-pull for Qorvo's T2G6000528-Q3 GaN packaged transistor from 3 to 6 GHz. (b) Load-pull simulation of the second harmonic of Qorvo's TGF2941 GaN bare die transistor at 24 GHz. The amplitude of the second harmonic impedance is swept from 0.6 to 1 in steps of 0.04, while the phase is swept from -180° to 180° in steps of 5°.

this. Another problem that arises is the filter not being conjugately matched when connected to the transistor. The transistor is matched for maximum PAE, output power or a compromise between those two parameters. This has an effect in the filter's effective insertion loss when operated in that condition. A new analysis reveals the origin of this and points to a method that can overcome it and improve performance even further. By incorporating the insertion loss to the load-pull results, a modified load-pull can be obtained and lead to improved efficiency [171].

- An impedance tuneable filter using the technique demonstrated in Chapter 3 can be used as the output matching filter of an FPA and provide load modulation. A load modulated FPA can be used for enhanced efficiency when operating in back-off.

- A MECA integrated FLNA would provide additional benefits to the design. Lower filter loss reduces the amount of required low noise stages for the FLNA to conserve low noise operation and more compact FLNAs can be implemented. The reduced temperature thermal environment resulting from embedding in metal also benefits noise performance.

- The work in Chapter 2 can be generalized to multiport networks, i.e. multiplexers. In [172] diplexers are used to implement broadband high efficiency amplifiers. Complex impedance diplexers would reduce the size of the design and improve efficiency.
- The work from Chapter 7 remains to be extended to dynamic scenarios, where the vehicle is in motion. The multi-module field reduction approach has only been explored in linear arrays, two-dimensional arrays remain to be examined for additional field mitigation.
- The wearable energy harvester presented in Chapter 9 can be combined with the power management shown in Chapter 8 to implement a full harvesting system.

10.2 Thesis Summary and Contributions

The contributions of this thesis are summarized as follows:

Chapter 2 develops the foundation used in the rest of the thesis for designing filters with complex terminations. The theoretical derivation shows that an imaginary (reactive) part can be added to the port impedance be means of a simple modification of a previously existing coupling matrix. The complex-impedance port formulation is first applied to a simple 2^{nd} order filter and a 4^{th} order filter with cross-couplings and transmission zeros, validated by experiments. The contributions presented in this Chapter were originally presented in [37] and the full theory was published in [38].

Chapter 3 establishes a method for designing impedance matching filters with tunable input impedance. A second-order Chebyshev filter with a tunable input impedance over a range of the Smith chart is designed, fabricated, and characterized. Measurements validate the feasibility of impedance tuning on a coupled resonator filter using a variable resonator and inverter with maintained filter response. The demonstrator filter uses varactor diodes as tuning elements. The contributions made in this Chapter are accepted for publication in [61].

Chapter 4 introduces a method for co-designing filters and power amplifiers (PAs) with a desired frequency response, improved efficiency and reduced footprint, using the theory from Chapter 2. The approach is applied to a single-stage high-efficiency 4.7 GHz, 4 W hybrid GaN filter-PA (FPA) within a

sub-6 GHz 5G band. A comparison of the state-of-the-art in co-designed filters and amplifiers with arbitrary complex impedances is shown in Table 4.1. The comparison singles out the FPA approach presented in this thesis as the most general with comparable or better performance. The contributions given in Chapters 4 and 5 are published in [38].

Chapter 5 describes the full design of a 28 GHz, 200 mW GaAs MMIC-FPA in the millimeter-wave 5G band using the method from Chapter 4. The MMIC was fabricated and characterized, showing good agreement between measurements and simulations. This design was published in [38].

Chapter 6 demonstrates the benefits of the metal-embedded chip assembly (MECA) heterogeneous integration technique for multi-chip modules. Measurements are shown for integrated alumina passives, surface mount capacitors and GaN MMICs connected with a unique interconnect network fabricated as the last step of the MECA process. The interconnect layer is shown to provide additional degrees of freedom for the design of microwave components. The flexibility of interconnect shape enables integration of MMICs that are designed to be wire-bonded, such as the ones demonstrated in this paper. Full-wave simulations show that they can be easily designed to out-perform wirebonds over a broad frequency range (10 to 100 GHz). The interconnect layer can also be used to implement transmission lines, referred to as bridge-lines, with reduced loss and higher possible characteristic impedances compared to traditional microstrip lines. These lines with larger characteristic impedances can be used to increase the design space for various microwave components. Multi-section branch-line couplers are microwave components that highly benefit from availability of lines with large characteristic impedance. A multi-section branch-line coupler incorporating bridge-lines of the interconnect layer combined with microstrip on alumina is used to validate the use of bridge lines for microwave component desing. These additional design capabilities can be extended to a wide range of passive microwave components like filters, couplers, hybrids, matching networks, etc. Integration of power amplifiers, couplers, capacitors and launchers in the metal embedded process is demonstrated as well. The contributions presented in this Chapter are reported in [93] for the passives and extended to actives in [98].

Chapter 7 discusses the development of a capacitive wireless powering system capable of safely providing kilowatts of energy from the ground to an electric vehicle. A multi-module near-field array approach is used to reduce the fringing electric field to levels that are safe for human exposition. The optimum phasing

between the elements of the array was demonstrated to be 180°, which provides maximum field reduction with almost no efficiency decline. The contributions from this Chapter are reported in [112, 113, 114].

Chapter 8 presents the design of an energy harvester capable of recycling energy from an airplane altimeter radar. The design demonstrates the feasibility of using energy harvesting for powering unattended low power sensors. The design of the rectenna is shown and a demo is given that shows with measurements how a practical system can be implemented to provide the required power with output voltages appropriate for energizing existing circuitry. The work presented in this Chapter was published in [119, 124].

Chapter 9 deals with the design of a wearable broadband energy havester, that uses a bow-tie rectenna array screen printed on a cotton tee-shirt. Harvesting of incident power densities between 4-130 μW/cm^2 between 2 and 5 GHz is demonstrated. A survey of the available ambient RF energy is also presented as a starting point for the rest of the design. The tightly coupled array is investigated as a function of finite size, port terminations, and separation of fabric above body. Additionally, simulations are performed for arrays with body curvature taken into account, showing that the change in performance is negligible, validating the use of a bow-tie array as a surface that is approximately matched to free space and therefore can conform to different shapes. For low incident power densities the efficiency is demonstrated to be in the 5-10% range, and reaches 32% for 100 μW/cm^2. The work presented in this Chapter is published in [165, 166].

10.3 Conclusion

In conclusion, codesign of system components can be used for performance enhancement of microwave and RF front ends. The use of filters as matching networks provides an opportunity for integration of filters and other microwave components, as evidenced in the design of filter power amplifiers and tunable matching filters presented in this thesis. Heterogeneous integration can not only be used for integrating diverse chip technologies but also for front end components codesign, providing additional thermal, gain, efficiency and matching benefits, as well as increasing the design options available for microwave component designers. Through codesign of antennas and rectifiers, compact rectenna systems can be implemented for harvesting energy from known and unknown sources. These rectennas can be placed in inconspicuous locations like

an altimeter radar sidelobe radiation harvester that can be embedded flushed with the airplane's body and a broadband wearable harvester array that can be screen printed into a tee-shirt. The work presented in this thesis opens many opportunities for more component integration work paths that will hopefully be researched and developed in the near future.

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