Assessment of Outphasing Power Amplifiers and Their MMIC Implementations

by

Daniel N. Martin

M.S., University of Texas at Dallas, 2016

B.S., University of Texas at Dallas, 2015

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

September 2020

Committee Members:

Taylor Barton

Zoya Popovic

Gregor Lasser

Paolo De Falco

Michael Roberg

Martin, Daniel N. (Ph.D., Electrical Engineering)

Assessment of Outphasing Power Amplifiers and Their MMIC Implementations

Thesis directed by Professor Taylor W. Barton

Power amplifier (PA) applications consistently require increased performance for bandwidth, power, and efficiency. Modern communication and telemetry systems are required to operate across multiple bands that can span octaves while scaling down unit power amplifier cells to fit on the back-end of phased array systems. Phased array implementation scales branch complexity for both signal generation and linearization. This creates problems with conventional approaches for back-off efficiency enhancement techniques as well as increasing the importance of linearity optimization. This reduces the complexity of the digital pre-distortion (DPD) required to operate the system while maintaining high average efficiency for large peak to average power ratio (PAPR) signals.

This thesis presents advanced outphasing PA architectures. Each of the architectures answers a different design challenge for modern communication and telemetry systems. Analog signal separation reduces the need for a digital signal split removing cost, size, weight, and power (C-SWaP). Improved modeling and understanding of the design of the inphasing splitter allows for optimization of linearity and efficiency. This work looks at utilizing novel power combining implementations with reconfigurable matching networks to operate outphasing PA's across multiple bands spanning an octave allowing for functional flexibility and reduced system complexity.

The thesis works on two distinct outphasing implementations: the RF-input outphasing power amplifier (RFIO PA) and the dual-input reconfigurable outphasing power amplifier (DIRO PA). The designs presented in this work are as follows:

- Hybrid X-band RFIO PA utilizing a previously designed dual-input X-band outphasing monolithic microwave integrated circuit (MMIC) in an unreleased Qorvo GaN 150 nm process
- Hybrid X-band RFIO PA utilizing three different non-linear elements (PIN diode, diode-connected transistor, and mesa resistor) in the signal splitter design to optimize for linearity and efficiency in

conjunction with a custom designed dual-input outphasing PA MMIC in Qorvo 150 nm GaN es process

- MMIC RFIO PA utilizing diode-connected transistors for integrated signal splitter design in Qorvo 150 nm GaN es process
- MMIC 6-12 GHz reconfigurable outphasing combiner with a switchable shunt line to control reactive loading in Qorvo's GaAs 250 nm process
- MMIC DIRO PA which is reconfigurable from 18-38 GHz with >2 GHz of instantaneous bandwidth in the WIN semiconductor PIH-110 process

Dedication

To my family, especially my parents (Maria and Tim), for all the love and support they have given me throughout my educational journey.

Acknowledgments

I am extremely thankful for my graduate advisor Prof. Taylor Barton for the excellent guidance, assistance, and education throughout my graduate experience spanning two universities. I am extremely honored to have had the privilege to experience the group being built up from the beginning.

I would like to thank Prof. Zoya Popovic and Prof. Gregor Lasser who have helped through numerous classes and side projects with advice and guidance on research topics as well as making me feel welcome into the group when first transferring into the University of Colorado Boulder at the beginning. In addition, I would like to thank Dr. Michael Roberg and Dr. Scott Schaffer for their professional and technical guidance through my Ph.D. and my internship at Qorvo.

I thank all my close friends and colleagues both current and graduated during my time at CU Boulder - Shane, Mike, Maxwell, Gregor, Eric, Patrick, Nina, Allison, Paolo, Prathamesh, and Scott for their friendship and all the great times. I would also like to thank everyone else across all research groups for their technical and emotional support. I would like to thank my amazing girlfriend Anna Nixon for her continuous love and support.

Finally I would like to thank Qorvo and WIN Semiconductors for their assistance on many numerous MMIC fabrication issues and access to the amazing processes.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Maintaining high power amplifier (PA) efficiency for wide dynamic range signals is becoming increasingly critical in many applications including RADAR systems with enhanced spectral confinement and next generation high speed communication systems. The increased signal requirements on both PAPR as well as instantaneous operating bandwidth are driving factors in modern PA design. Moving towards active phased array system implementations for both high-speed communications and telemetry applications from single antenna designs has redefined current integration and module design challenges due to spatial design constraint driven by fundamental wavelength.

1.1 Background and Motivation

The proliferation of RF/microwave wireless technology for the use of telemetry and communications has exploded in the last decade. The expansion of automotive RADAR into the standard vehicle safety technology offerings and the continuing advancement of wireless communication standards for high speed data transmission has lead to an increase in demand for active phased array system design. The increasing demands on the wireless infrastructure for increased transmission speeds and reduced latency presents new RF and microwave design problems and challenges [5].

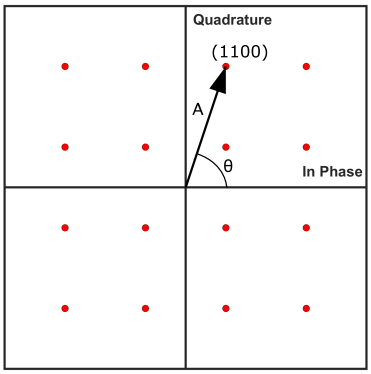


Figure 1.1: 16-QAM modulated signal constellation with voltage vector representation showing time-instantaneous package value.

1.1.1 Data Transmission

Wireless data transmission has continued to evolve as use cases become more complex over time. More recently, spectrum is difficult to obtain leading to requirements for high spectral efficiency of modulation schemes in next generation communication standards. There are many different forms of signal modulation schemes in order to encode digital data into symbols. A symbol is defined as a magnitude (A) and a phase (θ) that represents a string of bits as shown in Fig. 1.1 represented by red dots. The two most common forms of signal modulation include phase shift keys (PSK) and quadrature amplitude modulation (QAM). PSK modulation schemes are a special case of QAM schemes which encode data by setting the magnitude (A) to a constant value and varying the phase (θ) value. This style of data encoding allows for optimal operation out of a traditional PA where it is necessary to operate at maximum output power in order achieve the highest possible power efficiency. PSK modulation schemes are spectrally inefficient, especially when compared to full QAM modulation schemes. Higher-order QAM modulation schemes are highly spectrally efficient and are commonly used for the high data rate communication standards such as 4G LTE and the future 5G standard. QAM achieves high spectral efficiency through utilization of both amplitude and phase to encode information allowing for longer bit streams per symbol for a similar bandwidth. This increases the number of discrete amplitude and phase levels that are passed through the amplifier increasing the complexity for the transmitter path, especially the PA (shown in the transmit chain in Fig. 1.2), when attempting to make

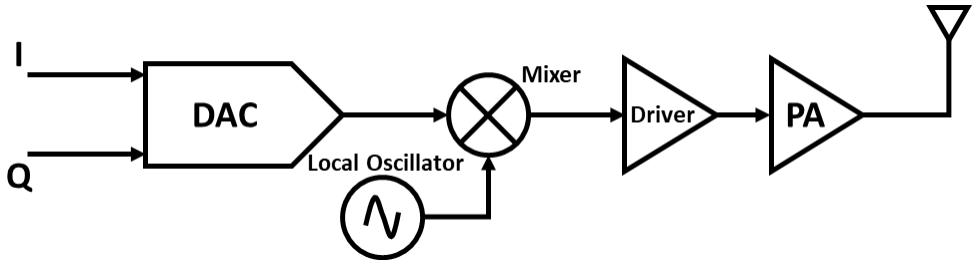


Figure 1.2: Simplified block diagram of a standard RF/microwave transmitter architecture.

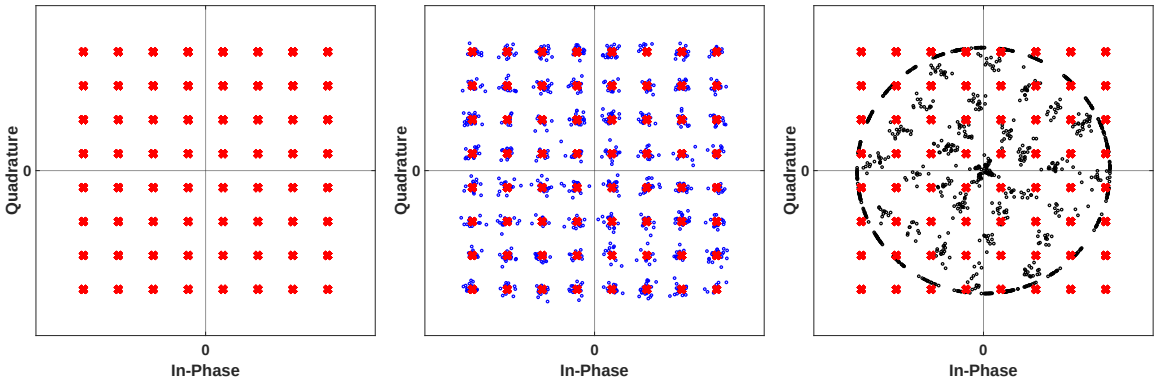
the system efficient due to the requirement for higher symbol accuracy (directly related to PA linearity performance).

PAs operate at a significantly reduced linearity when operating at higher power levels. The PAs create both amplitude and phase distortion referred to as AMAM and AMPM distortion respectively. These effects are input drive dependent for the power amplifier and are created through the intrinsic device current-voltage relationship. As the device starts reach current and voltage limits, the current and voltage waveforms begin to clip generating a non-linear AMAM characteristic. The closer to saturation a PA is being operated, the stronger the AMAM characteristics are. In addition to AMAM characteristics, AMPM characteristics are also observed in power amplifiers. AMPM typically occurs due to non-linear device capacitances that are modulated due bias modulation effects and overall drive level. These effects combine to create problems for the overall linearity and symbol integrity of the transmit chain. Fig. 1.3 shows the symbol integrity reduction due to major non-linear transmit chain contributions, specifically aggregated Gaussian noise and PA AMAM/AMPM effects, in Fig. 1.3 (c).

The relationship between the efficiency of a power amplifier in two traditional modes of operation and its output power is shown in Fig. 1.4a. There is a steep drop-off in efficiency (η) as the output power of the PA is backed-off through reducing input drive. The lower efficiency is due to the reduction of output power (P_{OUT}) while at any given point the same amount of DC power is being consumed:

$$\eta = \frac{P_{OUT}}{P_{DC}} \tag{1.1}$$

When combining the reduced power efficiency shown in Fig. 1.4a with a 64-QAM LTE modulation scheme in Fig. 1.3b and Fig. 1.4b it is apparent that even though the traditional classes of PAs can exhibit high



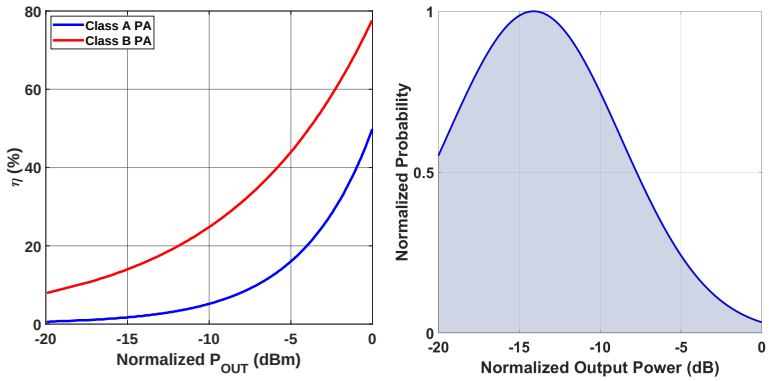
(a) (b) (c)

Figure 1.3: (a) 64-QAM ideal transmit constellation, (b) 64-QAM transmit constellation including Gaussian noise (blue), and (c) 64-QAM transmit constellation with aggregated Gaussian noise and AMAM/AMPM distortion of a highly efficient PA model (black).

theoretical efficiency, the average efficiency when operating under higher order QAM (subsequently large PAPR) signals will be poor. Power amplifier average efficiency is a major factor on the overall transmitter and base station efficiency as shown in Fig. 1.5. The PA and the equipment used to keep the PA cool account for up to 50% of the total power consumption of a 4G LTE base station [1]. Improving the average efficiency of the PA for a given modulated signal can heavily reduce the total DC power consumption not only allowing for reduced operating costs, but reducing the carbon footprint of each base station. This provides for a double reduction in DC power since improving power efficiency of the PA reduces DC power consumption of the PA itself as well as the cooling system due to reduced heat dissipation inside the PA. These large dynamic range signals require high peak efficiency out of an amplifier and the ability for it to operate at high efficiencies across a wide range of output power back-off (OBO).

1.2 Load Modulation

Traditional power amplifiers control output power as a function of input power $P_{OUT}(P_{IN})$ [6]. This gives linear control of the output power since an ideal linear PA can be modeled as a simple gain block $P_{OUT} = AP_{IN}$ where A is the power gain of the amplifier. Power amplifiers designed this way can operate with a high efficiency at a specific output power point. All other output power points will suffer a degradation



(a) (b)

Figure 1.4: (a) Theoretical PA efficiency vs output power for different traditional classes of operation. (b) Corresponding PDF of normalized 64-QAM signal from Fig. 1.3 output power (dB).

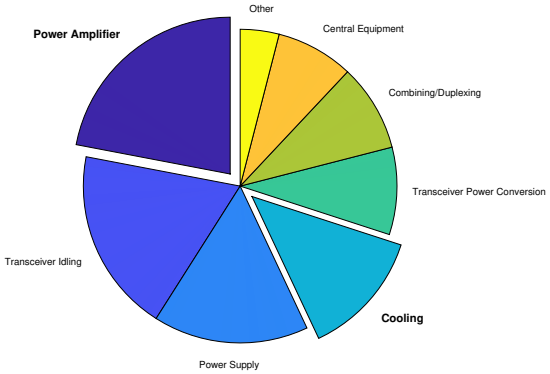
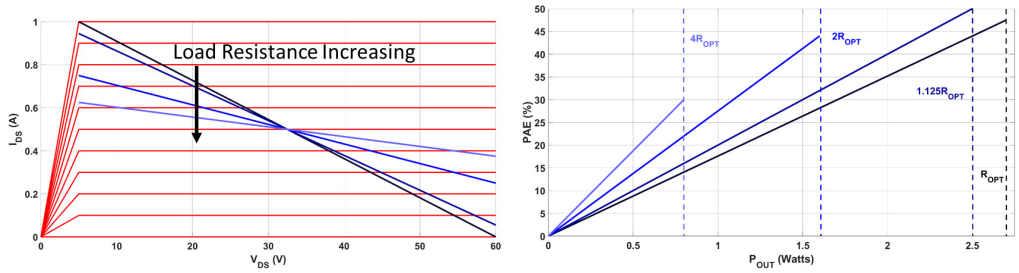


Figure 1.5: Pie chart of the power consumption within a typical 4G base-station. Highest power consuming component is the power amplifier itself with a close fourth highest consumer being the cooling system for the power amplifier [1].

in efficiency due to reduced output power (which corresponds to reduced load line utilization) and constant DC power consumption. Another method for output power control is needed in order to improve the efficiency at lower output power levels. Fig. 1.6a shows how the effective load line can be controlled through increasing load resistance (corresponds to lighter shades). The output power of an idealized linear PA can be written as:

$$P_{OUT} = \frac{V_o^2}{R_L} \tag{1.2}$$

where V_o is the fundamental component of the voltage across the output load. In controlling the output power with P_{IN} the V_o is effectively being modulated. The output power is also a function of R_L. By



(a) (b)

Figure 1.6: (a) Load line varying as a function load resistance. (b) Theoretical PAE as a function of output power at different load impedance values for an idealized Class A PA. Lighter shades correspond to increasing load impedance. shows control of the load line can be used to achieve higher efficiencies at a given output power in comparison to controlling P_{IN}.

varying the effective load resistance at the output of the PA the output power can be controlled. The benefit to this technique is that while the output power is being reduced you are optimizing the voltage swing of the system by an inverse relationship of P_{OUT} and R_L as shown in Fig. 1.6b. By fixing R_L and reducing the input power to reduce output power, the efficiency of the PA is significantly reduced when compared to actively manipulating the load as the output power is reduced. This technique is called load modulation and is commonly used to improve the average efficiency of PA's for large peak to average power ratio (PAPR) signals [6].

An important consideration when utilizing load modulation as a technique for improved back-off efficiency is the trajectory of load modulation. Trajectory refers to the direction the load varies as a function of output power. In the idealized case this is limited to the single dimension of the real component of the complex impedance plane. In the case of a real transistor the optimal load modulation trajectory can be obtained through load pulling the transistor and exists as a vector in the complex impedance plane. Fig. 1.7 shows the idealized case of a load modulation trajectory [7]. The peak power added efficiency (PAE) of the PA is located at 50 ohms and the peak output power is located at 45 ohms. As you increase the load resistance the output power falls off faster than the PAE. This maintains efficiency even as the output power is reduced. If the load resistance is reduced instead of increased from the peak output power and PAE points the PAE reduces at a faster rate than the output power. This provides a poor efficiency performance at reduced output power levels. This effect is even more important to consider when dealing with a real transistor whose load

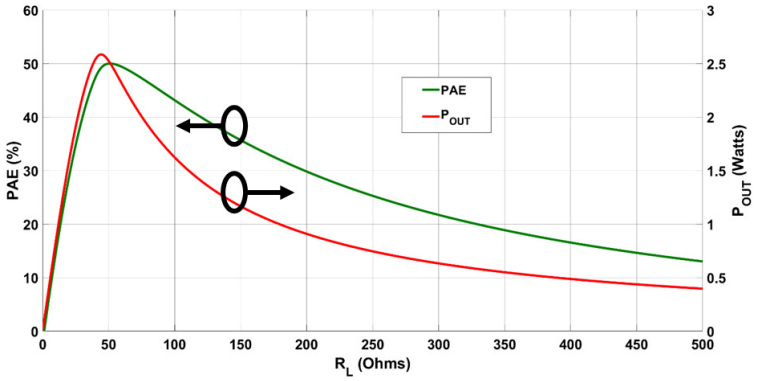


Figure 1.7: PAE (left) and P_{OUT} (right) of an idealized class A PA as a function of the load impedance. Shows that load modulation only works in a specific trajectory (in the ideal case an increasing load impedance).

modulation trajectory will be a complex vector due to the non-linear parasitic output and input capacitances of the device. [8].

Load modulation is a heavily implemented technique for improved average efficiency of PA's when operating under large PAPR signals. The PA architectures that utilize the technique can be found from handsets to base stations. Typical architectures include Doherty [9], envelope tracking [10], and LMBA [11]. This thesis will focus on a another form of load modulation architecture known as outphasing [12].

1.3 Outphasing

Outphasing is a load modulation PA architecture that was initially published by H. Chireix in 1935 [13]. The architecture utilizes load modulation for output power control. This allows the architecture to be constantly operating the PAs in saturation (maximum load line swing) and therefore at peak efficiency. This is accomplished by completing a vector decomposition. A single RF amplitude modulated (AM) and phase modulated (PM) signal is deconstructed into two constant envelope phase modulated signals:

$$A_{IN}(t) = A(t)cos(\theta(t)) \tag{1.3}$$

$$A_{IN}(t) = \frac{A_{MAX}}{2}cos(\theta(t) + \phi(t)) + \frac{A_{MAX}}{2}cos(\theta(t) - \phi(t)) \tag{1.4}$$

The amplitude data of the original signal is stored in the relative phase shift between the two vectors 2ϕ and the original phase data is maintained in θ which represents a rotation of the vector coordinate

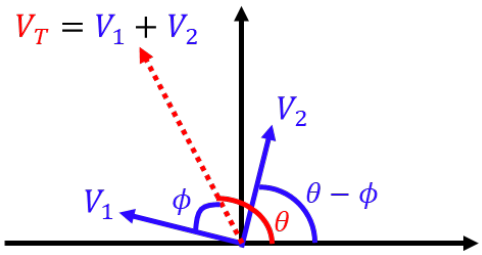


Figure 1.8: Vector sum theory of how outphasing power amplifiers store amplitude and phase data. $V_1 = Ae^{\theta+\phi}$ and $V_2 = Ae^{\theta-\phi}$ where both vectors have a similar constant amplitude and the outphasing angle ϕ is varied between them to control the output amplitude $V_T = 2Ae^{\theta}$. The phase modulation of the input signal is stored in θ and represents a coordinate system rotation.

space. These constant amplitude phase modulated signals are passed through two separate power amplifiers which are amplified and then recombined at the output through a vector sum operation. The in-phase components are added together and output and the out-of-phase components are subtracted and dissipated. This specific implementation of outphasing, which requires an isolated power combining network, is called linear amplification using non-linear components (LINC). Because the two signals going through each of the branch PA's are utilizing a constant amplitude, AMAM linearity of the branch PA isn't theoretically important due to the amplitude data being stored in the relative phase shift.

The isolating power combiner acts as the vector sum operation required to extract the original AM and PM signal at the output of the combiner. The two signals coming out of the two PA branches are:

$$A_1(t) = \frac{A_{MAX}}{2} cos(\theta(t) + \phi(t)) \; and \; A_2(t) = \frac{A_{MAX}}{2} cos(\theta(t) - \phi(t)) \tag{1.5}$$

$$A_{OUT} = A_{MAX} cos(\theta(t)) cos(\phi(t)) \; and \; i_{diss} = -\frac{A_{MAX}}{Z_0} sin(\theta(t)) sin(\phi(t)) \tag{1.6}$$

where i_{diss} is the current through the isolation resistor of a classic Wilkinson combiner. Therefore the dissipated power through the isolation resistor is:

$$P_{diss} = 2i_{diss}^2 Z_0 \tag{1.7}$$

Due to the dissipated power, which is quite large at lower power levels (larger relative phase shift), the PAE of a LINC PA as a function of output power is actually worse than that of a Class B PA and similar to that of a Class A PA. For this reason, a non-isolating power combiner is the standard implementation

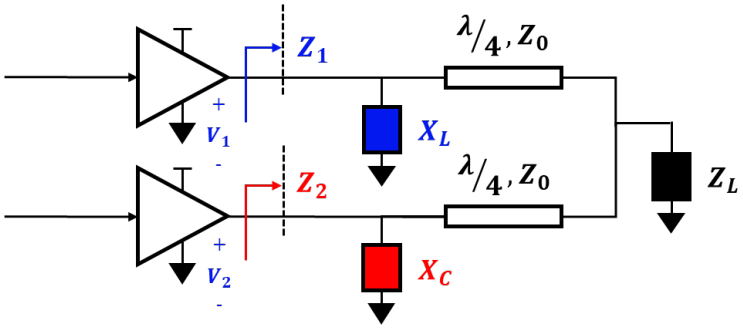


Figure 1.9: Chireix outphasing combiner block diagram.

when utilizing the outphasing architecture. The non-isolating power combiner still allows for a vector sum operation while not dissipating the out-of-phase vector components. The traditional non-isolating outphasing power combiner is the Chireix outphasing combiner.

1.3.1 Chireix Outphasing

Chireix outphasing is an implementation of the outphasing PA architecture which uses a non-isolating power combiner. This allows the architecture to take advantage of the improved efficiency that the branch amplifiers see in OBO operating regions without dissipating the out-of-phase vector components into an isolation resistor. The non-isolating combiner allows for the branch amplifiers to load each other allowing for a load modulation operating mode. This topology is shown in Fig. 1.9. The load impedances seen by each of the branch PA's is a function of the outphasing angle:

$$Z_1 = \frac{Z_L}{2}(1 - jcot(\phi)) \tag{1.8}$$

$$Z_2 = \frac{Z_L}{2}(1 + jcot(\phi)) \tag{1.9}$$

When two PA's are combined in a non-isolating power combiner the PA's will reactively load each other. One branch PA will see an inductive load while the other branch PA will see a capacitive load. The magnitude of the reactive mismatch is a function of the outphsaing angle (phase offset) between the two branches. When sweeping the relative phase between the two branch PA's between 0° and 180° the two branch PA's are only resistively matched at maximum power and at zero output power. There are also massive reactive impedance

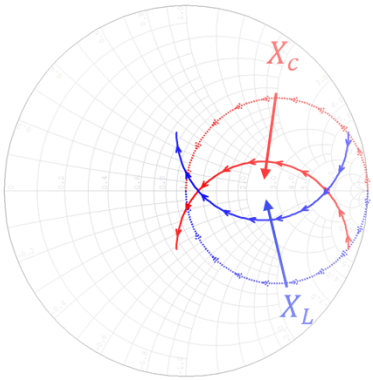


Figure 1.10: Chireix outphasing reactance compensation effect. Dashed lines show un-compensated branch amplifier loading. The solid lines show the branch amplifier loading when using reactance compensation reducing the average reactance seen by each of the branches across the range of outphasing angles that are being used. Blue corresponds to Z_1 and red corresponds to Z_2 in Fig. 1.9.

swings on both branches shown in Fig. 1.10 with the dashed lines. Shunt reactances are added to each of the input ports of the combiner which shifts the load contours towards the real axis of the smith chart. This allows for a resistive match at two outphasing angles (output power levels). These compensatory reactances are shown as X_C and X_L in Fig. 1.9. This allows for a reduced impedance range that the branch amplifiers see both resistive and reactive. The more compensation added allows the curves to move closer to the real axis of the smith chart. The trade-off is as the load contours move closer together the dynamic range of the outphasing PA reduces. The ratio of the the impedance of the first real axis crossing to the second real axis crossing determines the dynamic range of the outphasing PA. This means that a Chireix outphasing PA will start to degrade as relative output power levels reach <-12 dB from max. when attempting to make zero output power the outphasing PA must use two maximum power signals and perfectly cancel the two signals out. This is an extremely inefficient method for producing low output powers. Mixed-mode outphasing is the most common current method of driving outphasing PA's. This gets rid of the issue of needing to perfectly cancel out two high power signals to produce a low or zero output power signal.

1.3.2 Mixed-Mode Outphasing

A problem with the Chireix outphasing architecture is the trade-off that is inherent with branch PA resistive matching and dynamic range of the PA. There is also significant efficiency degradation at lower output power

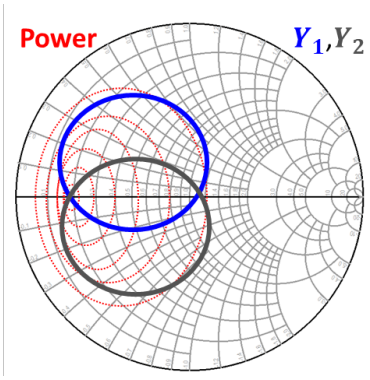


Figure 1.11: Chireix outphasing combiner branch load contours for an idealized combiner (blue corresponds to branch 1 and gray corresponds to branch 2). The dotted red lines show a load contour plot for an idealized transistor. Sweeping the outphasing angle from 0° to 360° produces two circular load trajectories. Due to the combination of the shape of the load contours for the transistor output power and the combiner load trajectories, a limited output power dynamic range is shown.

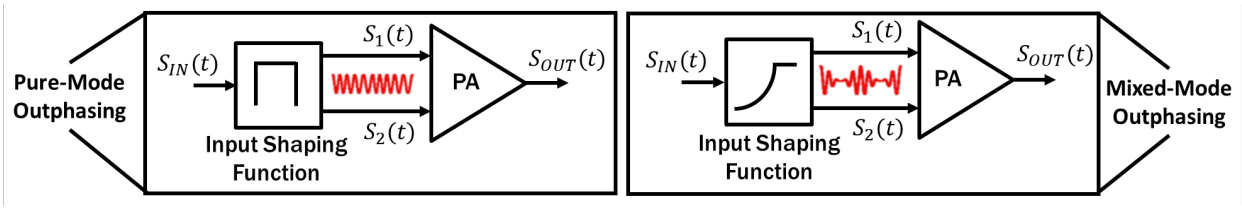


Figure 1.12: Mixed-mode with a shaping function for input power control vs. classical outphasing without input power shaping.

levels due to the fact that the branch amplifiers are constantly running at maximum power while attempting to phase cancel the two signals to produce a small or zero output power signal. To counteract the need to perfectly cancel out the two signals, amplitude control can be introduced back in as shown in Fig. 1.12. This provides a boost in efficiency at extremely low power levels since the power being input into the system is also reduced. The efficiency of the system can still be maintained through coherently controlling both the outphasing angle and the input amplitude in order to get the desired output power. The branch PA's can still maintain saturation if the outphasing angle, which directly corresponds to the load impedance seen by each of the branches, is controlled correctly with the input power to ensure the branches are still operating at peak efficiency at any given output power point.

Reducing the input power into the branch PA's will shift the optimum load for maximum P_{OUT} and PAE to higher load impedances which are within the outphasing combiner load trajectory regions. This

adds a significant performance advantage to the outphasing PA over a classically driven outphasing PA. The back-off efficiency benefit comes at a trade-off of complexity. Now a another dimension must be added to the look-up table (LUT) that is required for the signal decomposition in the digital domain since the amplitude and phase of both input signals must be coherently controlled.

1.4 Thesis Contents

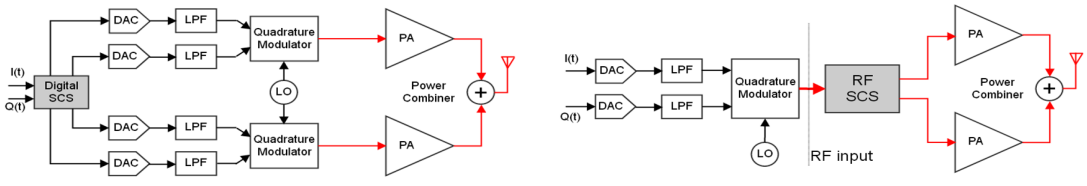
This research work has proposed 2 different PA architectures which resulted in 3 conference publications and 3 journal publications. The work will address the issue of complexity when decomposing the outphasing signal from a desired AM and PM signal into two mixed-mode outphsaing signals. It will also address the issue of implementing outphasing into wide-band/multi-band systems for modern communications and telemetry.

Chapter 2

RF-Input Outphasing

Since the inception of of the first outphasing power amplifier by Chireix in 1935, the strongest limitation of the architecture is the need for multiple coherent input drive signals. The generation of the input signals typically means the implementation of multiple modulator paths to generate the two or four constant-envelope phase-modulated signals. Modern realization of dynamic phase modulation for the generation of the outphasing signals is done through high frequency digital to analog converter (DAC) IQ modulators. These DAC modules take the separated outphasing signals that were generated in a digital baseband signal component seperator as shown in Fig. 2.1a and convert them into an RF signal.

The use of multiple TX up-conversion chains in each of the outphasing PA branches negatively impacts the C-SWaP (Cost Size Weight and Power) considerations of the overall TX module. In addition, it adds to



(a) (b)

Figure 2.1: Outphasing signal decomposition networks in (a) the digital domain and (b) the analog domain. Reduced complexity by moving signal decomposition network into the analog domain. Allows the leveraging of RF fractional bandwidth scaling.

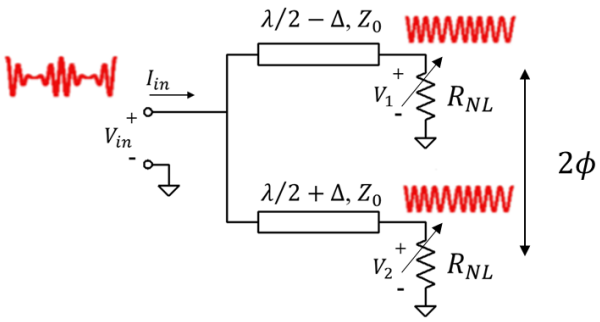


Figure 2.2: Idealized RF input outphasing splitter schematic showing time reversal duality drive to generate a relative phase split from an AMPM signal.

the overall complexity of linearizing the power amplifier through the use of DPD. Recent frequency scaling of RF systems has also posed a problem for traditional multiple input outphasing systems because the baseband computation doesn't scale with frequency. For many current system designs, an easier to implement solution would be to move the signal generation from the digital domain, where processing is costly from a C-SWaP standpoint especially when considering frequency scalability, and move it to the analog domain. This would create a drop-in replacement for a traditional RF power amplifier with a single RF input and and single RF output as shown in Fig. 2.1b.

2.1 RF-Input Outphasing PA Theory

In order to generate the outphasing signals in the RF domain an analog splitting network needs to be developed. It is discovered in [14] that a time reversal duality can be applied to an outphasing combiner network in order to generate the model for how an analog outphasing splitter network (inphasing splitter) needs to behave. A time reversal duality of the combiner shown in Fig. 1.9 would mean that Z_L is replaced with a power source that generates an AM and PM signal and the transistors on the two branches are swapped with loads. In order to properly model the varying impedances at each of the amplifier ports, the loads need to be power dependent loads. The network created is represented by Fig. 2.2. The voltage across the loads is:

$$V_{1,2} = V_{in}\frac{\pm jR_{NL}}{Z_0 sin\sigma \mp jR_{NL}cos\sigma} \tag{2.1}$$

where R_{NL} is a function of $P_{in} = V_{in}i_{in}^{*}$ and

$$\sigma = \frac{2\pi\Delta}{\lambda} \tag{2.2}$$

Then the magnitude and outphasing angle are:

$$|V_1| = |V_2| = \frac{V_{in}R_{NL}}{\sqrt{Z_0^2 sin^2\sigma + R_{NL}^2 cos^2\sigma}} \tag{2.3}$$

$$\phi = arctan\left(\frac{Z_0 tan\sigma}{R_{NL}}\right) \tag{2.4}$$

This gives a direct relationship between output voltage and the non-linear loading of the splitter network:

$$V_{out} = sin\left(tan^{-1}\left(\frac{Z_0 tan\sigma}{R_{NL}}\right)\right) \tag{2.5}$$

To complete the relationship so that $P_{out}(P_{in})$, a non-linear impedance element with a $R_{NL}(P_{IN})$ transfer function optimized for outphasing control of the system needs to be chosen. The ideal transfer function is a non-limiting characteristic at lower power levels, where the outphasing control is predominately amplitude based, with gradually increased limiting as input drive approaches amplifier saturation region. This allows the impedance at the splitter's output ports to vary at an increasing rate modulating the phase shift between the two ports. This allows for mixed-mode outphasing control which maximizes the efficiency that is obtained from the outphasing PA without having to add additional digital processing or complexity.

The default element/circuit with a characteristic that is described above is a limiter circuit. A limiter circuit provides a power clamp on the maximum amount of power that can be output through the limiter. This effect is achieved through the use of anti-parallel diodes and a RF matching circuitry. The limiting transition of a limiter circuit is typically faster than what is desired based on the analytically derived transfer functions above (as will be shown later in this thesis), however, its combination of AMAM and AMPM splitting characteristics fit well for the use of an RF-input outphasing (RFIO) PA splitter (inphasing splitter). This effect has been previously demonstrated at lower frequencies [15]. The scalability of the RFIO architecture will be addressed in the following section showing its capabilities at X-band.

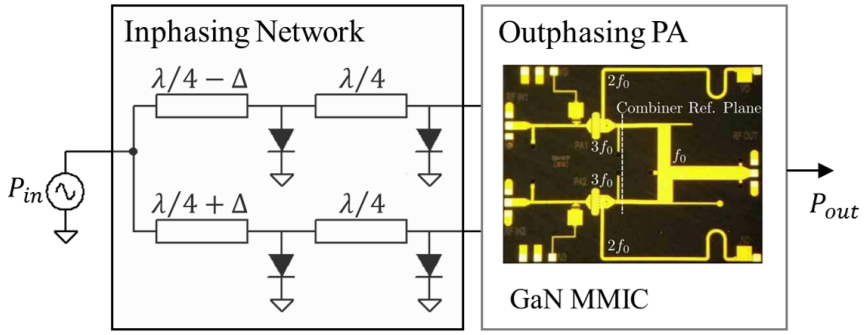
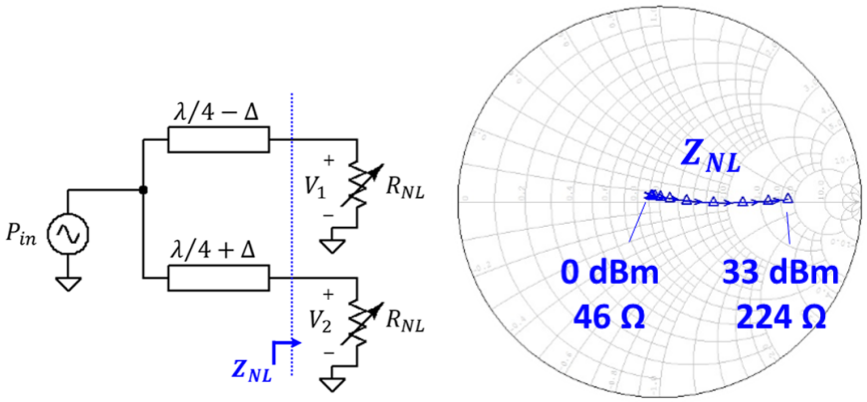


Figure 2.3: Simplified block diagram of the X-band RFIO PA described in this work. The passive inphasing network provides the required phase signals to drive the outphasing PA MMIC.



(a) (b)

Figure 2.4: The inphasing network (a) is based on transmission lines loaded with a non-linear termination. As R_{NL} varies, so does the relative phase of the outputs. Simulated limiter large-signal impedance across input power is shown in (b).

2.2 X-Band Hybrid RFIO PA

The proposed X-band RFIO PA, shown in Fig. 2.3, comprises an outphasing PA MMIC implemented in 0.15 μm GaN [16] and the hybrid inphasing network that is the focus of this work. The inphasing network is based on a non-linear technique that has been previously proposed for L band, but with topology adaptations to enable operation at X-band. Hybrid board fabrication at X-band was a major considering when designing the inphasing splitter as well as selecting non-linear elements.

RF-input outphasing uses a non-linear resistive element to produce a varying termination impedance

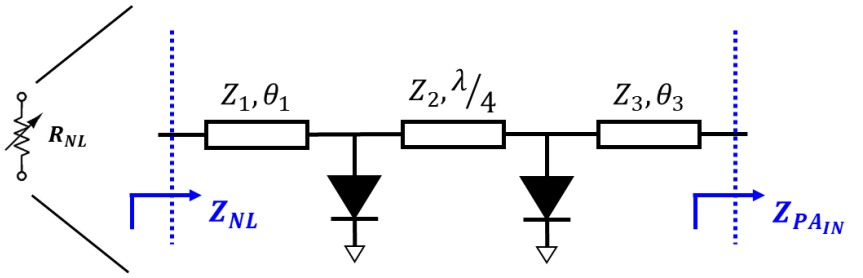
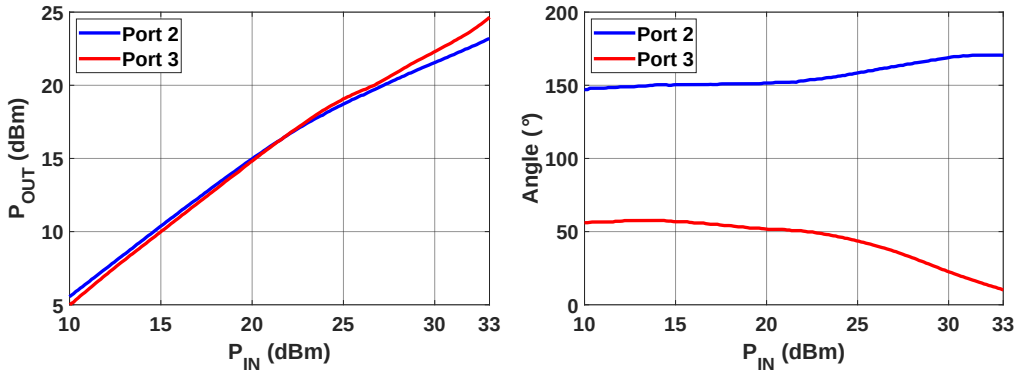


Figure 2.5: Schematic of the limiter design using PIN diodes. Replaces R_{NL} element in Fig. 2.4

at the output ports of a lossless splitter network, as shown schematically in Fig. 2.4. As the resistance R_{NL} varies, the relative phase (and magnitude) of the two outputs of the network will vary. By selecting a power-dependent non-linear element for R_{NL}, the network can be designed such that its output signals vary as an appropriate function of input power. These phase- and amplitude-modulated signals are then used to drive PAs in an outphasing architecture. This approach has been previously described in the previous section as providing a time-reversal dual of the Chireix outphasing combiner, and can be applied to two-way and multi-way power combining system.

The inphasing network must be designed to produce the correct input trajectory (i.e., input power levels and relative phases). The MMIC outphasing PA used in this work [16] is characterized and requires an outphasing angle of 159 degrees and input power at each port of 25 dBm for maximum output power, with the phase decreasing for subsequent lower output power levels. To generate this characteristic, a limiter is first designed to produce a wide-range resistive impedance variation in response to varying input power, and with a maximum output power of 25 dBm. The MACOM MA4L101-134 PIN diode was selected due to its high power handling and availability as a chip diode package. This allows for the lowest package parasitics while allowing for a wire-bond connection to the the top terminal and a soldered ground connection. The limiter architecture shown in Fig. 2.5 employs two cathode-grounded diodes separated by a quarter-wavelength transmission line, with stub lengths tuned to ensure that the impedance variation lies along the resistive axis of the Smith Chart. The input and output transmission lines provide additional system match to both the splitter and the input of the PA. The simulated impedance of the limiter network is shown in Fig. 2.4 as the power applied to the limiter is varied from 0 to 33 dBm.



(a) (b)

Figure 2.6: Simulated performance of the inphasing network, showing the power (a) and relative phase (b) of the two output signals.

The simulated inphasing network performance is shown in Fig. 2.6. The target outphasing angle (phase difference) of 159 degrees with 25 dBm output power at each of the ports is met. The difference in power between the two ports is less than 0.5 dB which will prevent excessive asymmetrical driving of the branch power amplifiers. The asymmetric drive is a result of the parasitic reactances of both the package and the non-linear element itself. The minimum phase difference of the network is 80 degrees, providing an expected power dynamic range of approximately 6 dB in the outphasing operating mode. Below this power level, the relative phases are held constant (due to the limiter diodes remaining off) and only amplitude modulation is applied. This results in mixed-mode operation, an established method in which amplitude modulation is used to extend the output power back-off range [14]. During the outphasing operating regime, amplitude modulation prevents over-driving of the branch PAs.

2.2.1 Measurements

The inphasing network, shown in Fig. 2.7, is fabricated using a Rogers 5880 20 mil thickness substrate. The outphasing angle of the inphasing splitter is measured using a four-port network analyzer with a calibrated power sweep (limited to 28 dBm due to vector network analyzer output power limitation). The resulting outphasing angle, calculated as the difference of phase(S_{21}) and phase(S_{31}), is shown in Fig. 2.8. It can be seen that the phase response matches simulation well in shape, but is offset in terms of absolute value. In

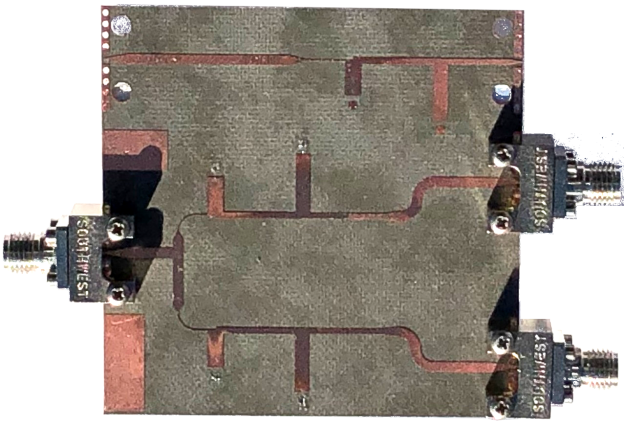


Figure 2.7: Photograph of the fabricated X-band inphasing network. The board, including a limiter drop-out, measures 60 mm by 59.8 mm.

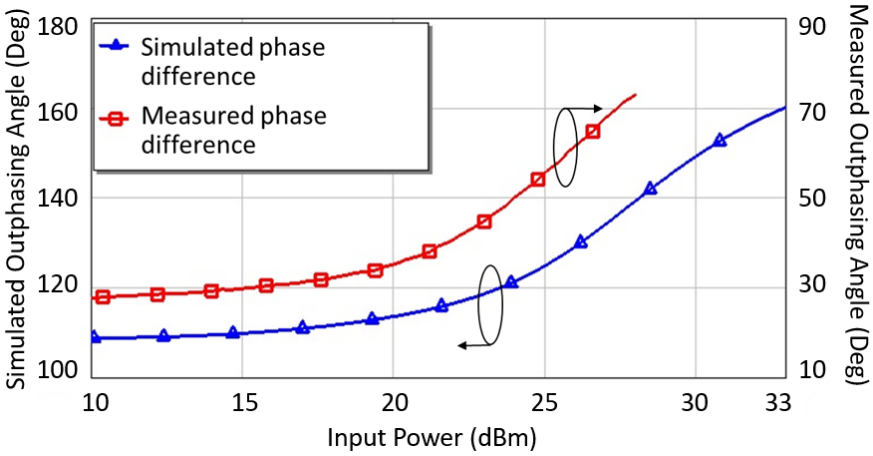


Figure 2.8: Measured and simulated outphasing angle produced by the inphasing network. The calibrated drive power of the VNA setup is limited to 28 dBm.

our experimental setup, this offset is compensated for using static phase shifters. The phase shift tuners are adjusted such that the phase at peak power corresponds to that required for the outphasing MMIC. The phase response of the inphasing network provides the dynamic phase modulation in back-off.

The output power required from the splitter when operating at maximum input drive (33 dBm) is 25 dBm at each port. Although this constraint is met in simulation, when measured the network was found to have approximately 10 dB additional loss: under peak drive conditions, the output powers at ports 2 and 3 are only 14.7 dBm and 14.06 dBm, respectively. This loss is attributed to fabrication issues, in particular relating to modeling of the diode ground return path. To compensate for the unanticipated loss, driver amplifiers are

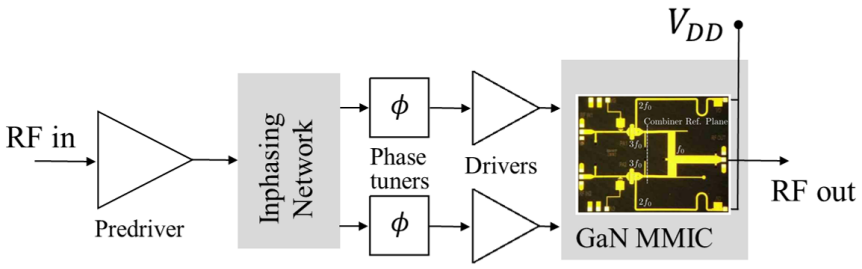


Figure 2.9: Block diagram of the experimental test setup. Driver amplifiers and fixed phase shift tuners are included to compensate for non-idealities in the inphasing network.

used between the inphasing network and outphasing PA to ensure sufficient drive power to saturate the PAs. These bench drivers are set up to provide approximately 10 dB gain.

The block diagram of the characterized RFIO system including phase shift tuners and drivers is shown in Fig. 2.9. Due to the inclusion of the drivers, only drain efficiency is reported in this work. The modulated RF signal is generated and analyzed using a National Instruments PXIe-5645R VST with 80 MHz analog bandwidth. The baseband I/Q signal is up/down converted at 3 GHz within the VST and an external frequency extension at 9.7 GHz is added to the VST and realized by off-the-shelf mixers and image-rejection filters.

The RFIO is characterized using modulated RADAR signals. Measured drain efficiency is shown in Fig. 2.10, with a peak drain efficiency of 63%. The outphasing “banana curve" characteristic is also visible, with the peak efficiency point located below the peak output power level. It is interesting to note that similar efficiency trajectories have been obtained in [2] for the same MMIC by means of digitally-controlled continuous input phase and amplitude modulation. The slightly lower peak efficiency reported in [2] is due to the inclusion of a supply modulator in the efficiency calculation.

Figs. [2.11,2.12] show the drive setup for the RFIO measurement setup as well as the mixed-mode measurement setup for comparison. Fig. 2.13 shows a comparison of the outphasing MMIC when measured in the RFIO setup (blue) vs when measured in a classical dual-input mixed-mode outphasing setup (red). The degradation of the drain efficiency at peak power and the improvement at 1.5 dB back off in the RFIO architecture is attributed to an uneven power split in the inphasing network, which generates unequal drive powers to the two branch PAs. This asymmetry modifies the load trajectories from their design values, and produces an optimum efficiency point further into power back off. The 0.65 dB less peak output power for

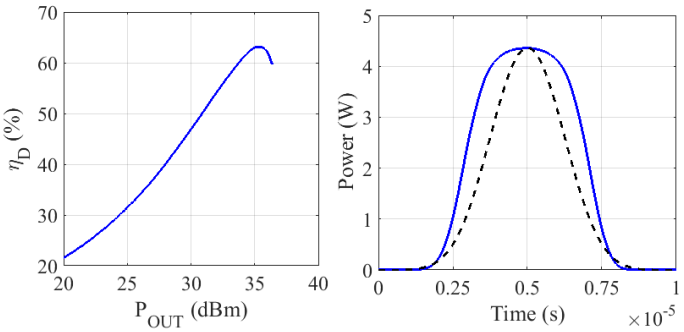


Figure 2.10: Measured drain efficiency vs. output power of the outphasing MMIC in the RFIO architecture, characterized for the pulse shown at right.

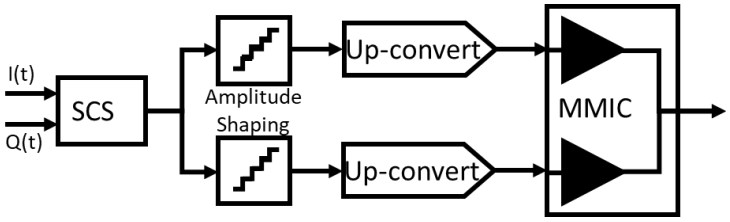


Figure 2.11: Mixed-mode outphasing drive schematic for measurements.

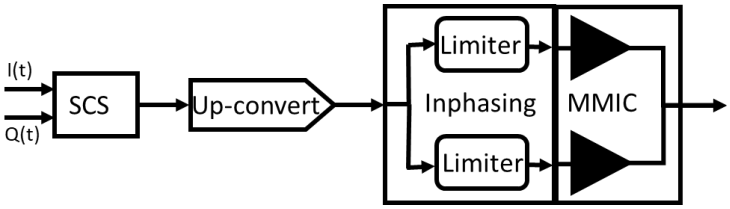


Figure 2.12: RFIO drive schematic for measurements.

the RFIO system is due to the accuracy of the static phase shifters in reaching the optimum outphasing angle for the outphasing MMIC. This comparison shows that the RFIO setup tracks the mixed-mode outphasing deep into power back off. We note that the dual-input measurement employs only a narrow range of input amplitude variation, whereas the RFIO system continuously modulates the PA drive power. The back-off efficiency of the dual-input system could be enhanced by increasing the extent of mixed-mode operation used.

Measured AM/AM and AM/PM characteristics of the PA are shown in Fig. 2.14. A generalized memory polynomial with non-linearity and memory order respectively equal to nine and one is used to model the inverted non-linear behavior with memory of the RFIO PA. The DPD is extracted off-line by characterizing

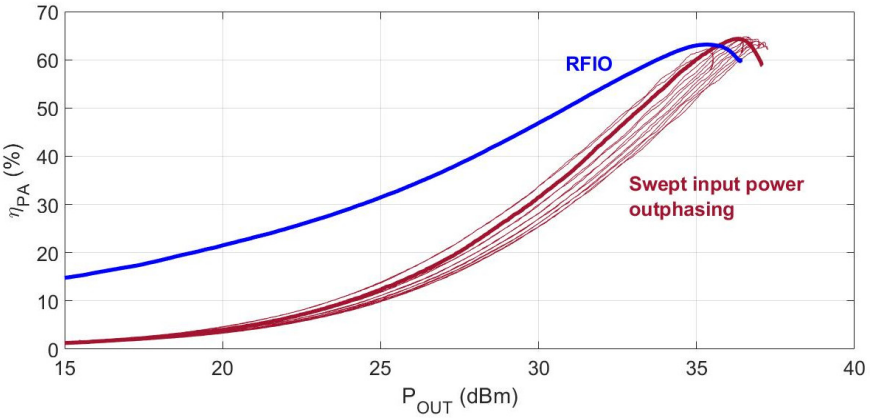


Figure 2.13: Measured drain efficiency vs. output power of the outphasing MMIC in the RFIO architecture (blue) vs. the same MMIC operated in conventional dual-input mixed-mode outphasing (red), with limited variation in PA drive power [2].

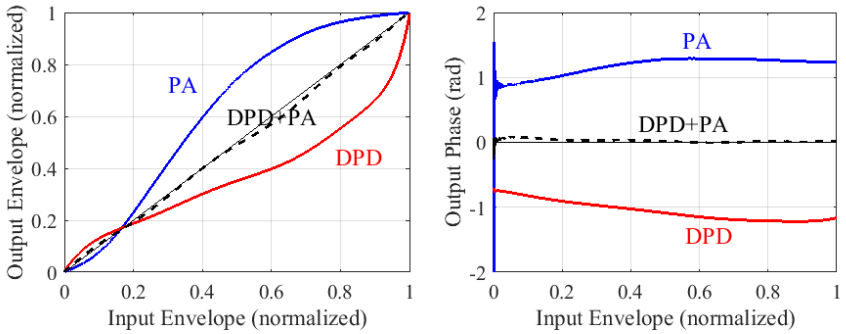


Figure 2.14: Measured AM/AM and AM/PM characteristics of the RFIO PA, characterized for pulsed measurements.

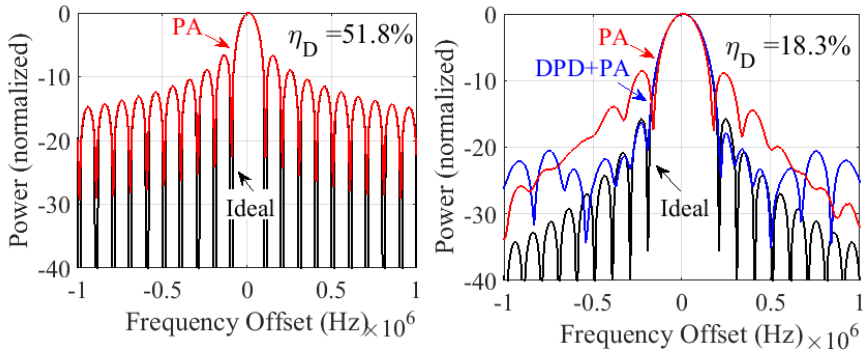


Figure 2.15: Measured output spectrum for a rectangular RF pulse and for an amplitude-modulated pulse with raised-cosine pulse profile. In both cases, the pulse duration is 10μs and the repetition period is 100μs.

the PA with the same sequence used as a test signal. An indirect learning architecture is employed, with the post-inverse model of the PA extracted at first, and then used to predistort the input signal of the PA. Rectangular and raised-cosine AM signals are used to evaluate the spectrum of the system without DPD and with DPD and the resulting spectrums are shown in Fig. 2.15. The system linearity improves by using DPD as shown in Fig. 2.15 where the first side-lobe of the raised-cosine pulse approaches the ideal signal spectrum. Although some distortion is still present, DPD clearly improves the system linearity. The average PA efficiency is 51.8% for the rectangular RF pulse and 18.3% for the raised cosine pulse. We note that in this work we do not employ a drain switch as in most typical radar PAs, therefore the PA continues to draw power during the off part of the period and this penalizes the average efficiency.

This work was successful in showing the scalability of the RFIO PA architecture into mm-wave frequencies. It was able to track the mixed-mode outphasing contours of the outphasing MMIC well giving back-off efficiency benefits equivalent to the complicated drive technique of the dual-input outphasing PA. The splitter ended up having significantly more loss than was initially simulated. This was due to discrepancies in the diode model as well as fabrication inconsistencies that have major performance impacts due to the 10 GHz frequency operation. The AMAM characteristic of the RFIO PA was heavily non-linear and required multiple memory taps to linearize. Utilizing the non-linear element characteristic as a way to linearize the PA is an un-utilized control knob in this design.

2.3 RFIO Analysis

All analysis done for RFIO PAs until this point has been done under the basic assumption that the transistors operating in an outphasing system can be modeled as ideal voltage switches. This assumption heavily over-simplifies all of the fundamental operations of the transistor and how it actively interacts with the active load modulation environment created by the outphasing combiner. A significant understanding of the outphasing system is that the sources are ideal voltage sources. Transistors in their normal amplifier operating condition function as current sources. To get the transistors to operate as close to a dependent voltage source the transistor needs to be driven heavily into saturation. Even in heavy saturation, the transistor doesn't function

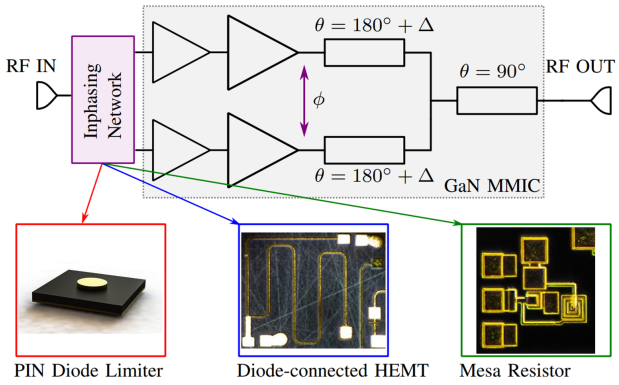


Figure 2.16: Block diagram of the RFIO PA architecture. Inphasing networks based on three different non-linear elements are designed and their performance compared.

as either a full dependent voltage source or a full dependent current source. Most of the limitation on its ability to operate as a dependent voltage source is due to the knee effect of the transistor. A more thorough model of the how a modern transistor operates and functions in an outphasing system will help to provide more accurate outphasing angle and amplitude trajectories for the inputs to the outphasing system.

A simplified model of the RFIO system for analysis is shown in Fig. 2.16. Working backwards from the output stage, this architecture consists of a non-isolating outphasing power combiner, two two-stage branch PAs, and the inphasing network comprising a passive network terminated with a variable impedance. The outphasing combiner presents an impedance to each branch PA that varies as a function of the outphasing angle θ, i.e. the relative angle between the two PA signals. In this work, a transmission-line combiner with asymmetric lengths is used which presents an impedance whose real part varies theoretically as cosine squared of the outphasing angle, and which presents complex conjugate imaginary components to the two branches. If the two branch PAs are assumed to operate as ideal equal-magnitude voltage sources — an assumption which will *not* be used in the subsequent analysis — the output power of the outphasing system will be

$$P_{\text{out}} = \frac{V_0^2}{2Z_L}(1 + \cos 2\theta) \tag{2.6}$$

where V_0 is the amplitude of the PA output voltage. In order to produce an overall response in which output power is linearly related to input power, then, according to this model the outphasing angle must be derived

from the input power as:

$$\theta = \frac{1}{2}\cos^{-1}\left(\frac{2Z_L P_{in}}{V_0^2} - 1\right) \tag{2.7}$$

As originally described in [17], this amplitude-to-phase signal decomposition can be performed in the analog domain through a simple passive network. The network is derived by applying principles of time-reversal duality [18] to the outphasing network to generate a network with the inverse characteristics. Conceptually, when the reversed combining network is loaded with a particular resistance value, the relative phase of the two output voltages will be such that when applied to the branch PAs the impedance seen looking into the combiner will have the same real part. Therefore, if the non-linear element R_{NL} can be designed to present the appropriate impedance as a function of applied power, the desired power-to-phase relationship of (2.7) can be implemented.

As is well-established in the outphasing literature [17, 19, 20], effective outphasing systems use mixed-mode operation, in which both the phase and amplitude of the input signal is modulated. In its simplest form, mixed-mode outphasing describes an approach in which the relative phase of the input drives is held fixed below the outphasing region, and instead amplitude is varied. As seen in the comparison of driving strategies in Fig. 2.17, this approach significantly improves efficiency in deep back-off compared to pure outphasing. In the outphasing operating regime, a fixed input drive means that the PA's gain decreases as the total output power increases, as seen for the "mixed mode limiter" drive case in Fig. 2.17. In practical systems, therefore, the input amplitude is modulated together with phase in the outphasing mode ("flat gain limiter" case in Fig. 2.17), ensuring that the branch PAs operate at a fixed saturation level. An input signal separator, whether digital or in the RF domain, must therefore generate an appropriate function in both amplitude and phase.

This simplified analysis, presented in more detail in [17, 21], provides a qualitative understanding of the RFIO architecture but does not accurately produce a linear RFIO response. In particular, the assumption that the PAs behave as ideal sources produces an inaccurate estimation of the relationship between load impedance and output power.

The actual transistor behavior is expected to deviate significantly from the ideal expression in (2.6), thus invalidating the phase relationship in (2.7), while the required input drive will depend on a detailed

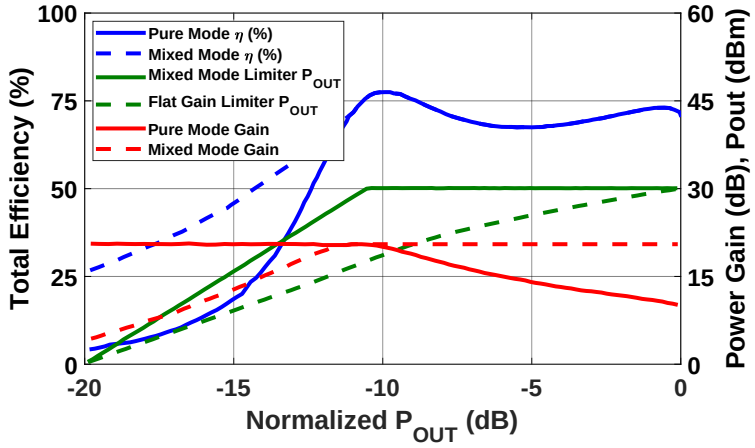


Figure 2.17: Classical outphasing drive vs mixed-mode outphasing drive performance, with the branch amplifiers assumed to be ideal class-B PAs. Ideal limiter performance shown for the ideal AM-AM response for mixed-mode operation.

knee model of the device. A more accurate model of the relationship between outphasing angle (and correspondingly, load impedance) and the output power of the system is therefore needed. In this work, we first use a simplified analytical model to generate a more accurate prediction of the angle and input drive level needed for outphasing operation. Then, based on this relationship an inphasing network and non-linear resistance element can then be designed.

2.3.1 RFIO Model and Design Approach

As a compromise between treating the transistor as ideal voltage-source, or using a full non-linear model, this section establishes a modified clipping model for the 150-nm GaN device used in this work. The goal of this analysis is to predict the output power and efficiency of the technology when operating in an outphasing system at a particular gain compression level.

The typical load-line analysis based on a fixed knee voltage and constant transconductance, although useful for estimating PA performance in a fixed-load system, is not sufficiently detailed for load-modulated PAs. Specifically, the strong knee effect in GaN affects both the desired impedance match at the fundamental frequency (for linearity and efficiency) and the desired harmonic terminations. Additionally, the assumption that the device operates as a current generator is not applicable to architectures where the device is operated in a highly saturated mode. Therefore, clipping behaviors and knee interactions must be well-modeled in

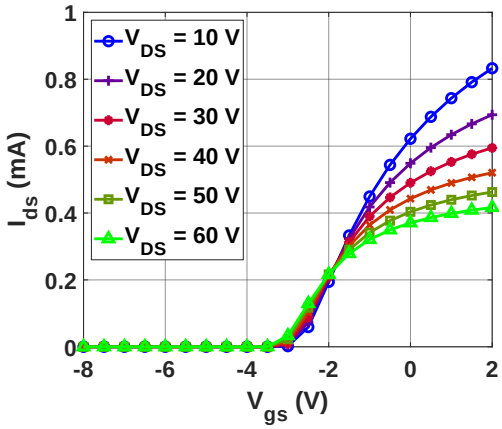


Figure 2.18: Simulated I_{ds} vs. V_{gs} curves for the 8x100μm GaN device used in this design, at different V_{ds} values.

order to predict the device operation in the RFIO architecture.

We apply a modified version of the reappraised load-line method [3] to aid in the design of combining and inphasing networks for the RFIO PA. This model captures the strong knee effect and the knee walk-out effect of GaN technologies.This walk-out occurs due to the dependence of the knee voltage on the transistor bias point, V_{gs}, and is a feature of AlGaN and GaN. This relationship can be seen in Fig. 2.18, which shows simulated dc drain current over swept gate voltage and under different supply voltage conditions for the 8x100 μm GaN device used in this design.

The previously presented knee model describes the I-V curve of the device in terms of a knee non-ideality factor, N, [3]:

$$i_{ds}(\theta) = A(\theta)k(v_{ds}) \tag{2.8}$$

$$k(v_{ds}) = 1 - (1 - v_{ds})^N \tag{2.9}$$

Here, $A(\theta)$ describes the transconductance function applied to the input voltage. Fig. 2.19 reproduces the effect of the parameter N on the I-V characteristics of the model as described in [3]. As $N \rightarrow \infty$ the knee voltage approaches an ideal on-off characteristic, while low values of N correspond to stronger knee effects. Typical values for GaN are on the order of $N \sim 4 - 10$.

We represent the transconductance as a piece-wise function, with a third-order polynomial representing

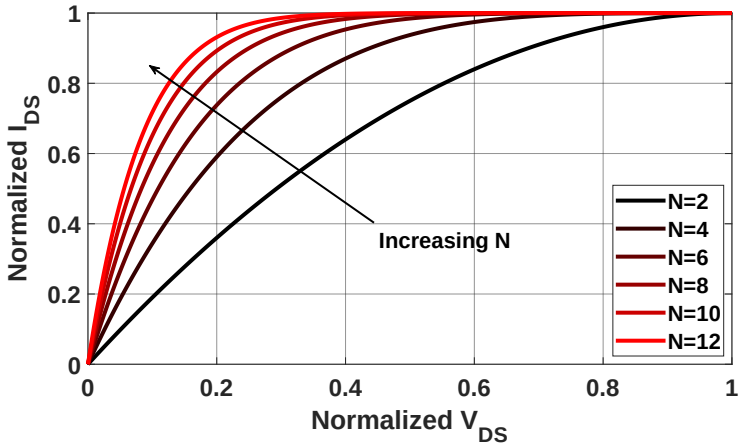
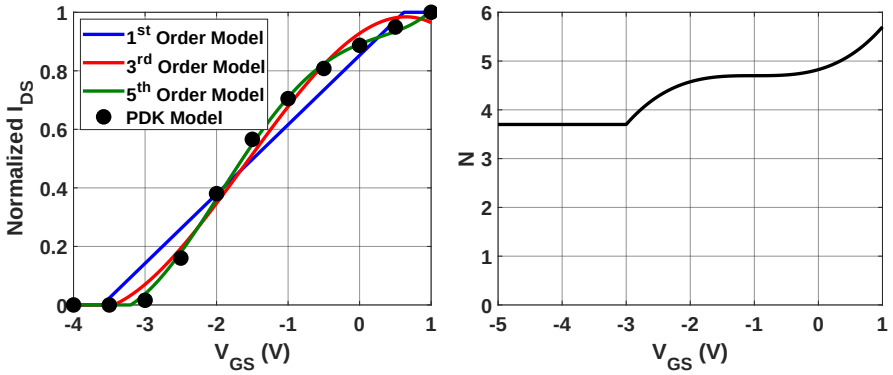


Figure 2.19: Analytical model for I_{DS} vs V_{DS} curves given a knee factor (N) and comparing strong vs. weak knee effect. A strong knee effect corresponds to a smaller N value and a slower transition into saturation. Reproduced based on [3].



(a) (b)

Figure 2.20: Proposed analytical model describing the device saturation characteristics. (a) $A(V_{gs})$ function modeling transconductance as a polynomial, (b) Variation of N with V_{gs}.

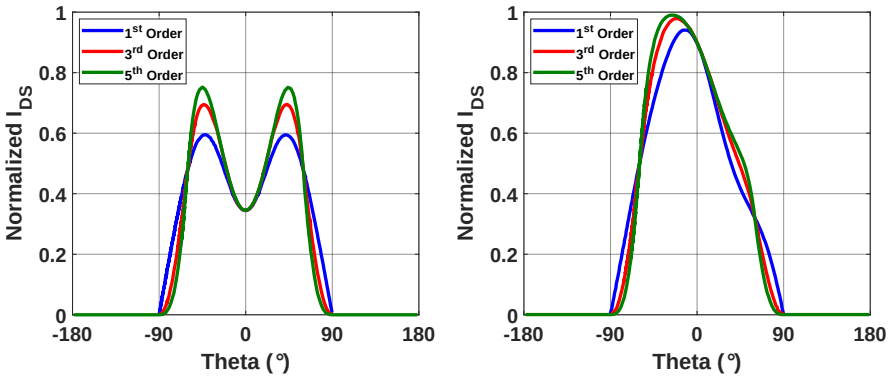
the behavior between pinch-off and saturation:

$$A(V_{gs}) = \alpha_0 + \alpha_1 V_{gs} + \alpha_2 {V_{gs}}^2 + \alpha_3 {V_{gs}}^3 \tag{2.10}$$

$$i_{ds} = A(\theta, V_{gs}) \cdot \left(1 - (1 - V_{ds})^N\right) \tag{2.11}$$

The parameters $\alpha_0, \alpha_1, \alpha_2$, and α_3 are fit to the device's I_{ds} vs. V_{gs} dc characteristic based on simulation using the process design kit (PDK) large-signal, resulting in the functions shown in Fig. 2.20(a).

In this work, the value of N is additionally allowed to vary as a function of V_{gs}, capturing the stronger knee walk-out effect as the quiescent current increases. The factor is modeled as a first-order non-linearity



(a) (b)

Figure 2.21: IDS with clipping effect, Daniel model

with the relationship:

$$N(V_{po}, V_{gs}) = \begin{cases} N_0 + V_{po}, & V_{gs} \leq V_{po}. \\ N_0 + f(V_{gs}), & \text{otherwise} \end{cases} \tag{2.12}$$

where V_{po} is the pinch-off voltage of the device, and assuming that $V_{gs} < 0$ for the GaN HEMT. The function used for the selected device is plotted in Fig. 2.20(b).

Transient waveforms in class-B operation using the model shown in Fig. 2.20 are plotted in Fig. 2.21. The details of clipping effects can be observed, as well as the dependence on the order of the polynomial in (2.10). In this work, the 5th order model is used. Compared to the model in [3], the slope of the transitions near the on-off transitions is better captured, which is important for the load modulation studied here. The modeled dc I-V curves are shown in Fig. 2.22 and are compared to those from the device's large-signal model. Although there is clearly imperfect agreement between the analytical and large-signal models, the analytical model sufficiently captures knee interaction for our initial prediction of the efficiency and output power of the device under different input drive and load modulation conditions, while offering significantly reduced calculation/simulation time.

With the simplified device model established, the waveforms can be analyzed within the outphasing system to understand the relationship between load impedance and output power of the PA. This relationship is used both to design the outphasing combiner, and to determine the optimal inphasing relationship. In the proposed approach, we assume that an outphasing combining network is first designed, and then the

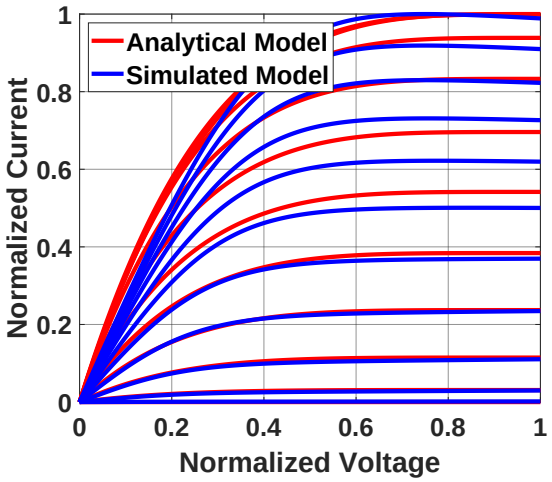


Figure 2.22: PDK Model IV curve (Blue) vs analytical model IV curve (Red).

appropriate inphasing network is developed.

The effects of the transistor knee effect are shown qualitatively in Fig. 2.23, which shows target load-pull contours corresponding to peak output power (solid lines) and peak efficiency (dashed lines) at peak power and at 6-dB back-off. Both output power cases correspond to a fixed compression level and are calculated using the analytical transistor model for $N = 16$ (weak knee effect) and $N = 6$. As can be seen, when the knee effect is properly accounted for, the target impedance for peak power is shifted to the left in the Smith chart, enabling the combiner load trajectory to remain within an efficient region over a wider range of output power. Similarly the region of high efficiency at 6-dB back-off corresponds to a higher impedance than predicted when the PAs are assumed to operate as ideal sources.

The outphasing combiner is designed to present the load impedance trajectories shown in Fig. 2.23 when driven by equal-amplitude inputs, targeting a 6-dB output power dynamic range. The combiner is based on half-wavelength lines with characteristic impedance of 50 ohms and a $\pm\Delta$ electrical length of 180 degrees at the 10-GHz design frequency [22], as shown in Fig. 2.16.

By applying the model developed above, the optimal load trajectories, along the required input amplitude and outphasing angle for a desired output power, can be found that maximize efficiency or linearity of the RFIO PA. We note that the optimal transfer function(s) will be determined by both the device technology and the implementation of the final RF stage of the outphasing PA. The model is used to determine analytically

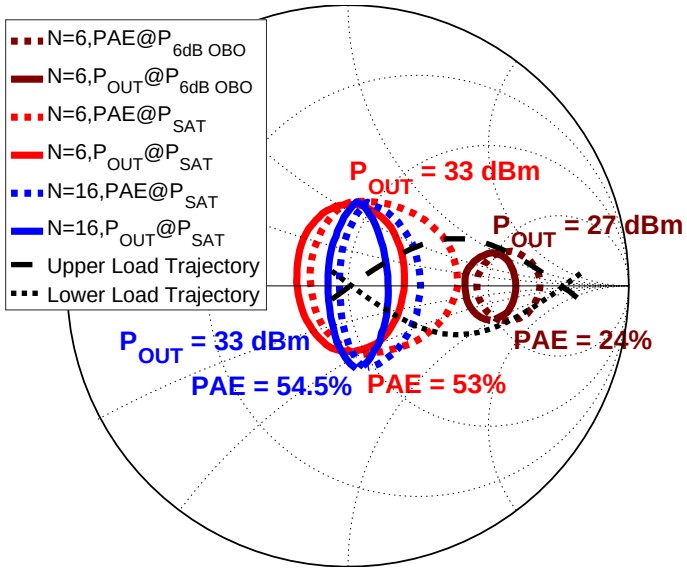


Figure 2.23: Load pull based on analytical model. Ideal outphasing combiner load trajectories (black) overlayed.

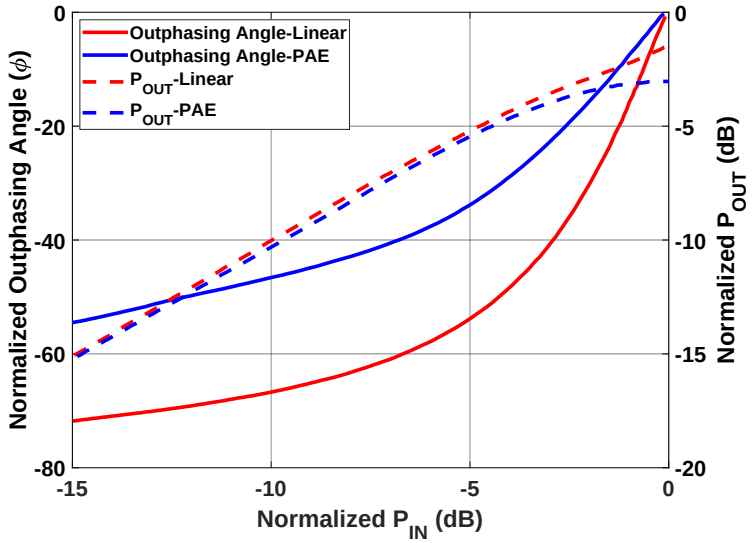
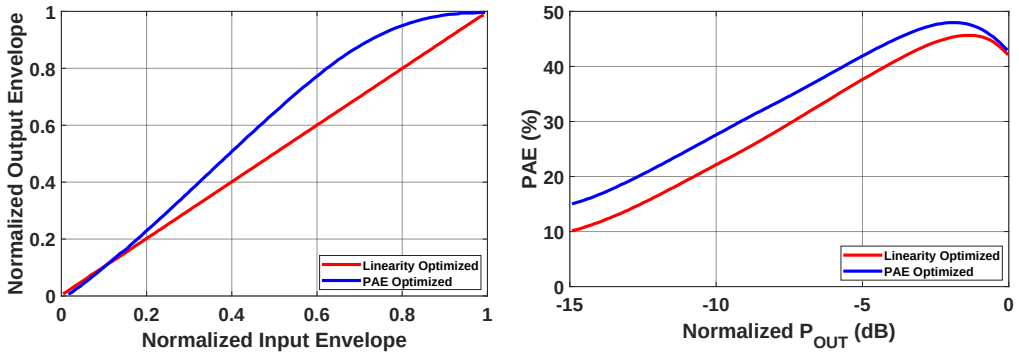


Figure 2.24: Ideal signal decomposition based on non-linear model.

determine the required phase and input amplitude required at each point in order to linearly track the load contours or track the maximum efficiency point at any given output power. This analytical exercise was done under the assumption that the devices themselves looked purely resistive without any non-linear input or output capacitance.

Fig. 2.25 shows the expected output power and efficiency for the two signal decomposition strategies,



(a) (b)

Figure 2.25: Normalized (a) output power and (b) efficiency of the outphasing output stage for the linearity and efficiency optimized signal decompositions.

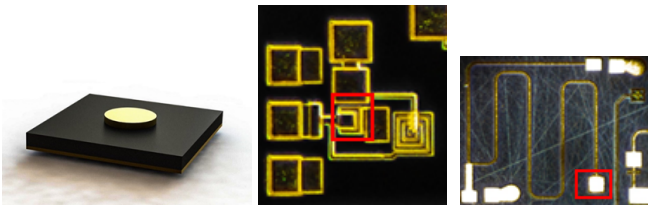
based on the simplified transistor model.

2.4 Non-Linear Elements

The inphasing network must perform a non-linear signal decomposition to implement the desired amplitude and phase response found in the previous section. Previous work [17,23–25] used a diode-based limiter as the non-linear element. in general, The choice of non-linear component and its specific impedance variation as a function of applied power will determine how closely the ideal signal decomposition can be approximated.

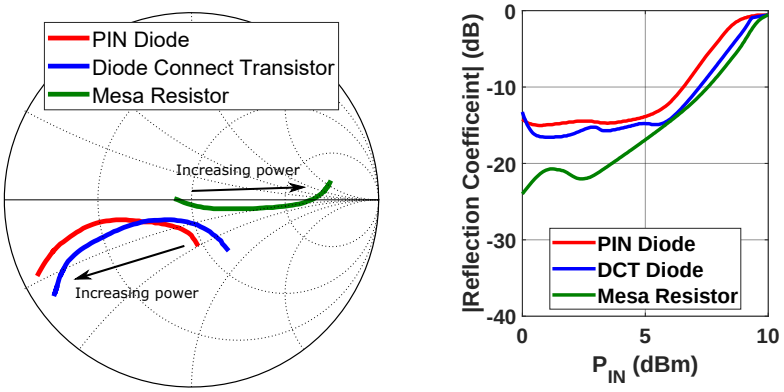
In [17] it is observed that the general characteristics required of the inphasing network's non-linear element are that its impedance decreases with input power, and that its amplitude response has a limiting behavior so that the power applied to the branch PAs remains approximately constant in the outphasing region. In Fig. 2.24, however, it can be seen that for the PA considered in this work only a weakly limiting amplitude response is desired. Additionally, we note that passive network design can be used to compensate for arbitrary complex impedance variation. The key determiner of how closely the outphasing angle decomposition can be synthesized is the rate of change of the (complex) non-linear impedance as a function of applied power.

The ability to synthesize an arbitrary inphasing network characteristic therefore depends on the availability of an appropriate non-linear element. Here, we consider three non-linear elements for use in the inphasing network: a PIN diode, diode-connected GaN HEMT, and mesa resistor. The three components



(a) (b) (c)

Figure 2.26: The three non-linear components used for inphasing signal separation: (a) PIN diode MACOM MA4L101-134, (b) diode-connected GaN HEMT in Wolfspeed 250 nm GaN process. The transistor is single 150 um finger shown in the red box. The surrounding circuitry is a bias tee to enable active biasing of the diode.(c) mesa resistor with on-chip pre-matching network in the Qorvo GaN 150 nm ES process. The resistor is a 35 μm x 15 μm equivalent to 175 Ω shown in the red box.



(a) (b)

Figure 2.27: Simulated power-dependent impedance of the three non-linear elements as the applied power is swept from 0–10 dBm. (a) Smith chart showing large-signal impedance at the fundamental frequency; (b) Magnitude of fundamental-frequency reflection coefficient vs. applied power from large-signal simulation.

are shown in Fig. 2.26, and their large-signal input impedances are plotted in Fig. 2.27 over each device's operating power range.

2.4.1 PIN Diode

The PIN diode was used in [17, 25] as the non-linear element due to its approximation of the properties needed for the inphasing response: its large-signal input impedance decreases as input power increases, and at low input powers the diode remains off, enabling mixed-mode operation. Other advantages of the PIN diode include its relatively low loss as well as the availability of non-linear models. The MACOM MA4L101-134 PIN diode used in this work varies over an approximately 5.4:1 impedance magnitude range at the 10-GHz

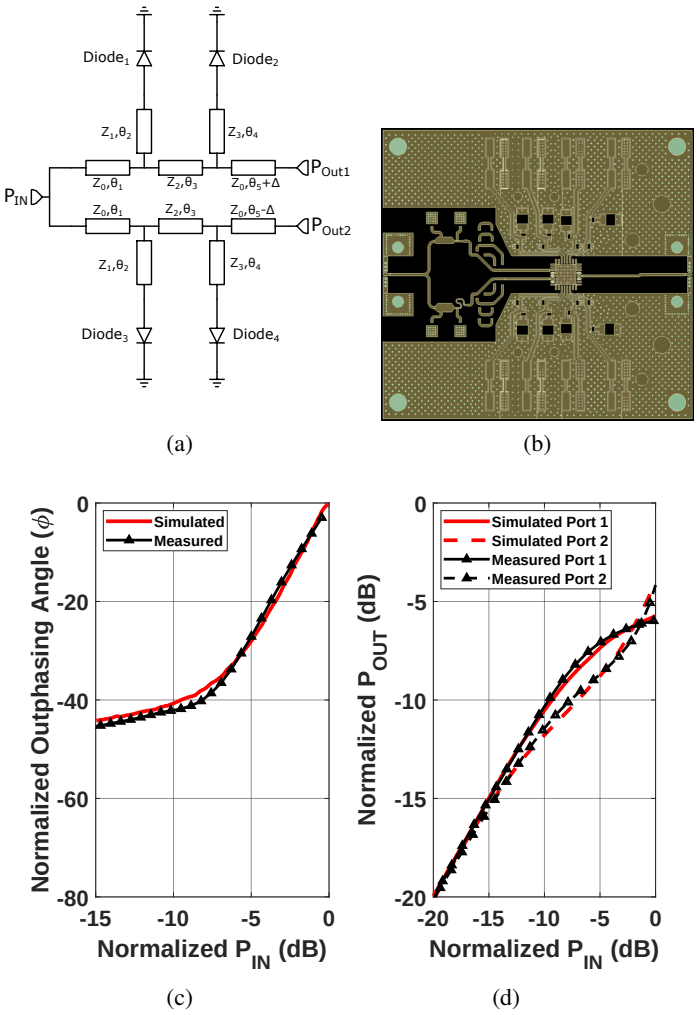


Figure 2.28: Summary of the inphasing network based on the PIN diode: (a) schematic, (b) simulated and measured outphasing angle and (c) normalized power delivered to the two ports.

design frequency as the applied power ranges from 0 to 10 dBm. This impedance variation is used to generate a 45.3 degree variation outphasing angles using the transmission-line structure shown in Fig. 2.28(a). Note that an anti-parallel diode limiter structure is emulated here by using two cathode-grounded diodes separated by a quarter-wavelength transmission line. This structure was selected because the available package for the diode requires wirebonding to the top, anode, pin.

The inphasing network phase and amplitude response is characterized using a test structure printed circuit board (PCB) with connectorized outputs. CW measurements are made using a Rohde & Schwarz ZNA43 vector network analyzer (VNA) in a 50-ohm environment. Because the branch PAs are input matched to

50 ohms and include driver stages, minimizing any input impedance variation due to the output-stage load modulation, it is expected that the connectorized PCB measurement will accurately capture the behavior in the RFIO PA. The measured and simulated outphasing angle and power delivered to the two output ports for this network are shown in Fig. 2.28(b)-(c). The outphasing angle is normalized to the phase at peak input power for best comparison between the three different inphasing networks. For this relatively narrow-band design, a fixed offset in phase can be implemented by unequal feed lengths to the two branch PAs. The output power is normalized such that a lossless network with gain of 1 for all input powers would produce a straight-line response with peak normalized output power of 0dB.

The PIN diode's turn-on behavior is characterized by a long "tail" in which the rate of change of the effective impedance slows as input power increases. As can be seen from the amplitude response in Fig. 2.28(d), the diode must be driven into deep compression to produce the required range of outphasing angles, resulting in lower than desired input power to the branch PAs in the upper $\sim$ 6 dB of operation. The result is a slow compression non-linear behavior in the RFIO PA as was also observed in [17]. Moreover, the diode structure produces only 45.3 degrees of outphasing angle variation compared to the 71.8 degree dynamic range needed for the optimal transfer function for linearity and 54.4 degree range needed for the optimal PAE transfer function response. The difference between measurement and simulation in the AMAM curves for the power split can be attributed to discrepancy in the simulation model and where it is validated as well as the non-linear parasitics in the element. Both of which significantly impact the asymmetric power split between the two branches.

2.4.2 Diode-connected transistor

The Schottky junction of the diode-connected GaN HEMT offers an alternative diode structure to generate the required limiting and non-linear impedance. An advantage of the diode-connected HEMT is that it is available in all MMIC processes, and the device size can be selected for the required input power levels, although the junction is not typically modelled for this specific use. In this work, a 1 x 150 um HEMT in the process is used. A die photograph of the .35 mm x .35 mm die area is shown in Fig. 2.26.

Similar to the PIN diode design, the diode-connected HEMT's source is grounded by the bottom of the

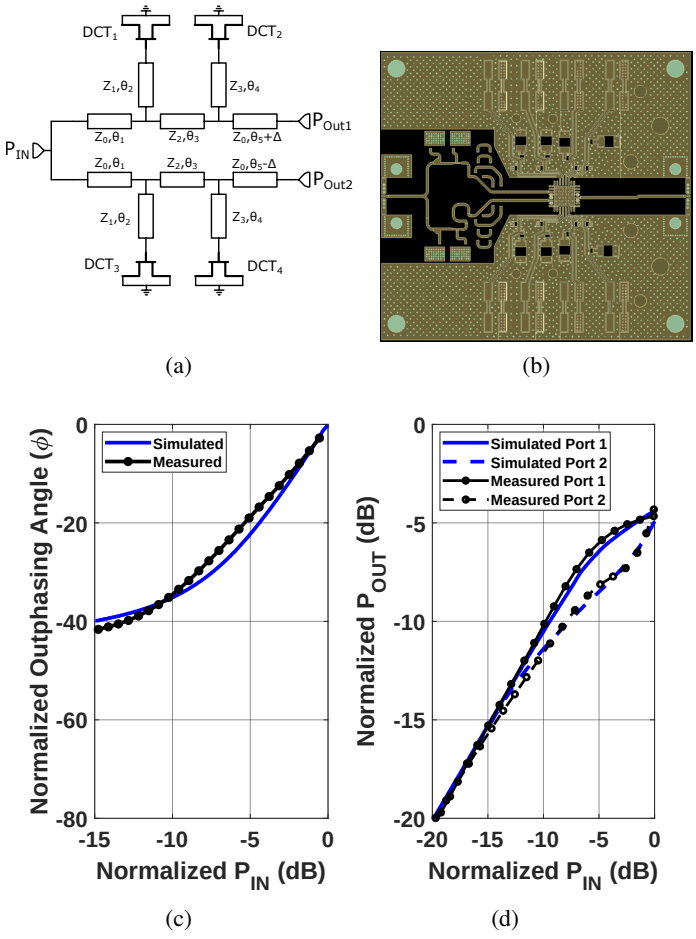


Figure 2.29: Summary of the inphasing network based on the diode-connected HEMT: (a) schematic, (b) simulated and measured outphasing angle and (c) power delivered to the two ports.

MMIC, so it is used in a limiter structure in which two diodes are separated by a quarter-wavelength line to approximate anti-parallel diodes. The transmission line structure is similar to that for the PIN diode, but with higher impedance lines and a longer phase offset to compensate for non-linear gate capcitance effect of the diode-connected transistor. Large mounting pads can be seen on the PCB to accommodate the die size (Fig. 2.29), as the diode-connected HEMT was included as a structure on an unrelated MMIC design.

The simulated and measured signal decomposition is shown in Fig. 2.29(b)-(c). It is clear that the large-signal HEMT model is not designed for operation in this mode, resulting in discrepancies between simulated and measured response. The range of outphasing angles is approximately predicted in simulation. The amplitude response shows that the diode-connected HEMT begins forward conduction at a lower than

predicted input power, leading to a substantially different amplitude response and to increased loss.

2.4.3 Mesa Resistor

The epitaxial mesa resistor in the GaN process was recently demonstrated to function as a limiter due to its saturation current limit [26]. Because this device is integrated with GaN MMIC devices, requires little die area, and can be sized nearly arbitrarily for appropriate power handling, it is an attractive alternative to diode limiters. In addition, its power-limiting characteristic is weaker than those of the conventional limiter, with the implication for mixed-mode outphasing that the power delivered to the branch PAs increases more linearly even as the effective impedance change of the mesa resistor causes outphasing angle variation.

In this work, the mesa resistor is realized in Qorvo GaN15 process and sized as 15 um x 35 um. The sizing was determined to balance the need for proper current handling and output power of the limiter with the compression characteristic and impedance swing as a function of input drive. The large-signal characteristics are modeled in simulation using a non-linear measurement-fit model provided by Qorvo. A T-structure [26] provides the maximum impedance swing obtainable while balancing out the parasitics within the mesa resistor. The MMIC includes a pre-matching network that aligns the large-signal resistance to the real axis at 10 GHz, corresponding to the preferred non-linear element described in [17]. The resulting simulated large-signal impedance over a 0 to 10 dBm input impedance is shown in Fig. 2.27.

The mesa resistor is used with an asymmetric-length transmission line power divider with an offset line length to produce the desired phase range. Similar to the diode-connected HEMT, this element is included on a larger MMIC die which is accounted for in the inphasing network PCB design. The simulated and measured phase and amplitude characteristics in Fig. 2.30 show a relatively low (40 degree) outphasing dynamic range, but with an even and linear power division to the two branch PAs, with the lowest insertion loss of the three non-linear elements.

Fig. 2.31 compares the measured responses of all three non-linear elements to the optimal signal decompositions. For the purposes of comparison, the phases are normalized to that at peak input power, because absolute phase shifts can be easily synthesized. The two diode-based limiters produce similar phase ranges but with different rates of change relative to input power and with different compressive amplitude responses.

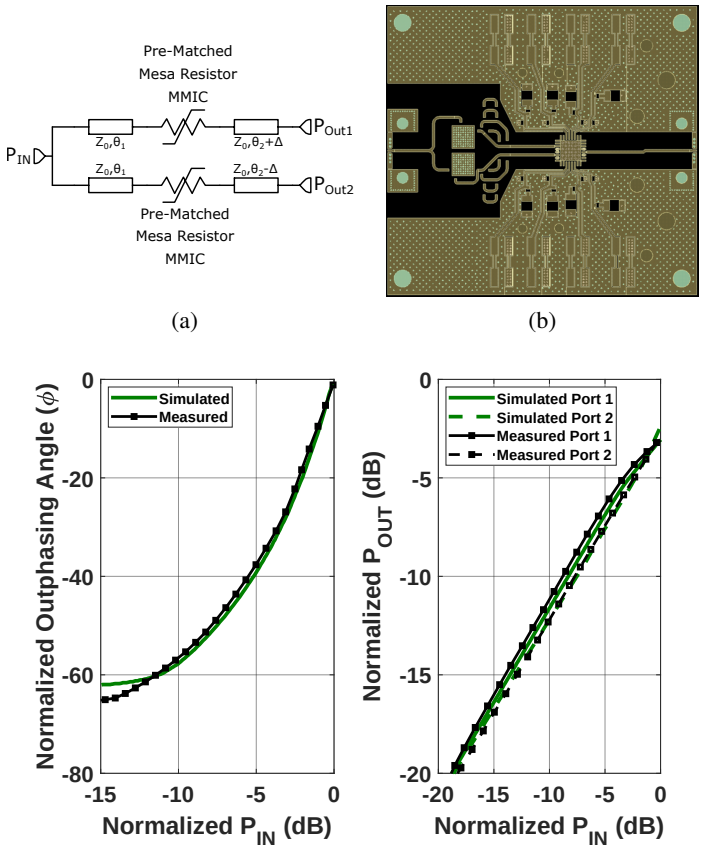


Figure 2.30: Summary of the inphasing network based on the non-linear mesa resistor: (a) schematic, (b) simulated and measured outphasing angle and (c) power delivered to the two ports.

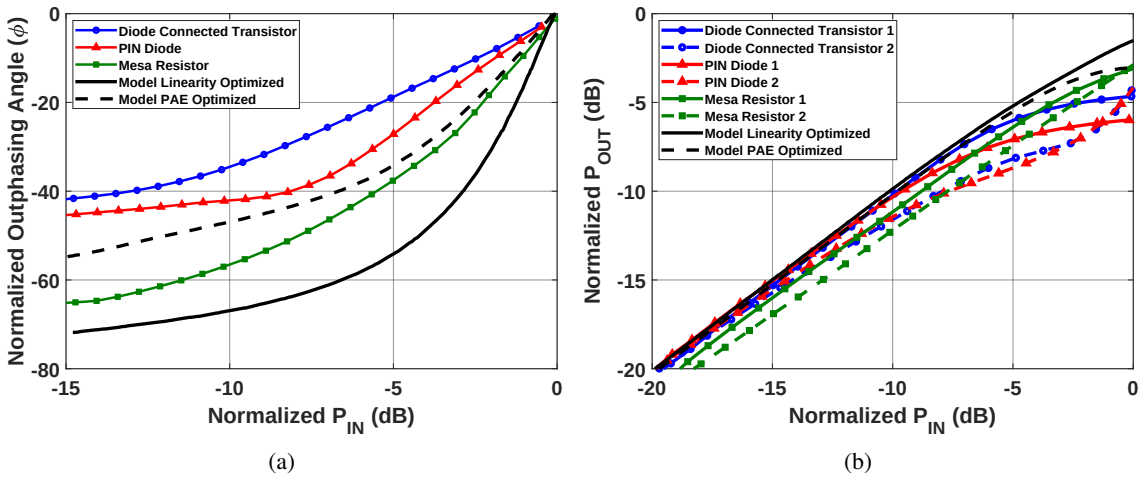


Figure 2.31: Summary of the measured inphasing characteristics for the three non-linear designs, compared to the linearity and efficiency optimized transfer functions.

The mesa resistor produces the greatest outphasing angle variation and offers an efficiency-linearity compromise phase response by lying between the two desired trajectories. In terms of amplitude response, the insertion loss of the two diode-based limiters means that the branch PAs may not be sufficiently driven into saturation in the high-power range. While clearly none of the inphasing networks is lossless, the overall effect of this loss on RFIO gain and PAE is lessened by implementing high 22.1 dB gain branch PAs.

2.4.4 MMIC Design

An X-band dual-input outphasing PA MMIC is fabricated in Qorvo's 150 nm GaN BCB process for demonstration of the different inphasing network strategies. The MMIC is packaged in a 5x5 QFN over-molded package, allowing for straightforward fabrication of the breakout boards and interaction with the hybrid inphasing networks.

As described in Section 2.3, the combining network is based on half-wavelength transmission lines with the reactance compensation asymmetry implemented with a $\pm\Delta$ line length. This transmission line structure occupies a larger die area and presents a higher insertion loss than an equivalent *L*-*C* pi-network structure. Nonetheless, the lumped-element implementation was found to be too sensitive to process variations, specifically the tolerances of the small capacitor values required, to ensure that the correct load trajectories are presented to the branch PAs. To mitigate the insertion loss of the combining network, the transmission lines are raised off the substrate utilizing the air-bridge in process layer. By placing bridges at the maximum allowed spacing it reduces the conduction losses through the substrate. The simulated loss of the network is .178 dB.

The branch amplifiers are designed as two-stage PAs with a 4:1 staging ratio, using 4x50um and 8x100um devices. The simulated gain of the branches is approximately 22 dB across the 9-11 GHz operating band. Including drivers in the branches mitigates the impact of the final-stage load modulation on the input impedance of the PAs by ensuring a unilateral characteristic for the PAs [21, 27]. This unilateral behavior is particularly important in this work because of our goal of comparing the effects of different non-linear devices. In addition, the high branch PA gain in the architecture helps to compensate for losses introduced in the inphasing network, ensuring that the inphasing network operates on low-power signals and therefore

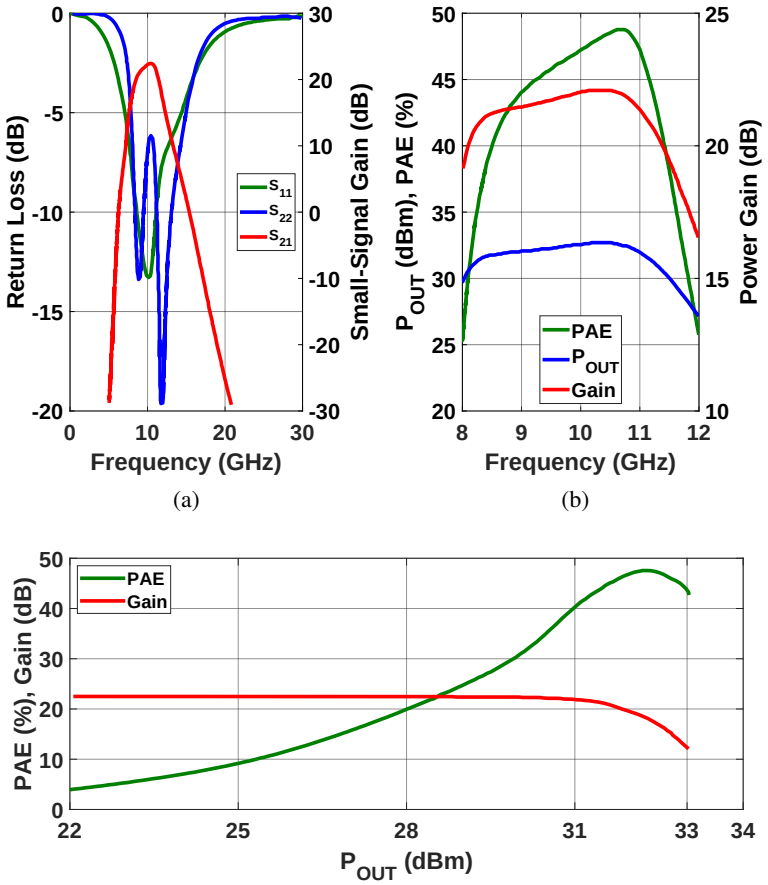


Figure 2.32: Simulated performance of the two-stage branch PAs. (a) – S-parameters, (b) – large-signal performance, (c) – driveup.

has reduced impact on the system PAE. By comparison, previous works [17, 23–25, 27] focused on drain efficiency of the final output stage, neglecting the effects of inphasing network loss. In this design the PAE of the entire RFIO PA is reported.

Stacked CT7 capacitors are used at the bond pads for ESD robustness. In addition ESD diodes were added to the gate pads to improve ESD robustness of the devices. Loop-gain stability analysis is used to verify that the design is stable without off-chip capacitance, and shows an 18 degree worst-chase phase margin. The branch PA simulated performance is shown in Fig. 2.32, and the layout can be seen in the die photograph in Fig. 2.33.

The packaged MMIC is first characterized as a conventional dual-input outphasing PA. CW outphasing

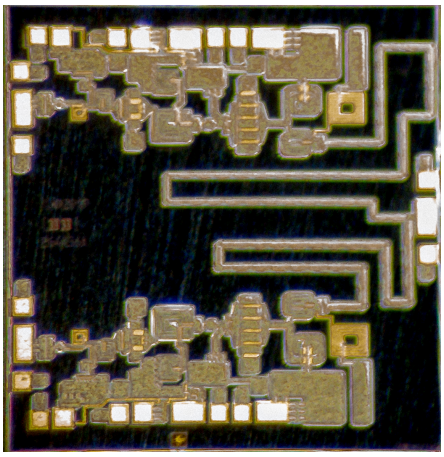


Figure 2.33: Die photograph. The total die area is 2.5 mm × 2.3 mm.

measurements are performed using a Rohde & Schwarz ZVA40 vector network analyzer (VNA), with coherent phase control of the multiple port sources used to control the relative phase applied to the two PA inputs. No pre-driver is required because of the relatively low input power needed to drive the MMIC. For the CW simulation and measurement comparison in Fig. 2.34, a fixed 12.5 dBm input power is applied, and the phase is swept over 24–108 degrees (simulated) and 18–102 degrees (measured) to produce the pure-mode outphasing performance characteristics shown. A good agreement between measurement and simulation can be seen, with both reaching a peak output power of 36 dBm. The slight degradation in PAE at peak power and increase at back-off in measurement is attributed to a shift in load trajectory in the fabricated MMIC. It may be observed that the PAE vs. output power characteristics do not show the characteristic efficiency peak at output back-off that is expected based on ideal outphasing theory. This non-ideal characteristic is commonly observed in load-modulation architectures implemented in technologies with strong knee effect. Nonetheless, the outphasing PA even in pure-mode operation shows improved back-off efficiency compared to the single branch PA (Fig. 2.32(c)).

Due to the non-linear effects occurring at the input of the PA as a result of the inphasing splitter network, non-linear simulations were run to check the impact on the return loss as the input drive varies. The simulation results are shown in Fig. 2.35. Across all three splitter implementations while there is an impact on the return loss as the drive changes, the effects are minimal to the overall performance of PA. The effects are mostly mitigated by the insertion loss through the splitter itself which isolates the input reflection coefficient impact.

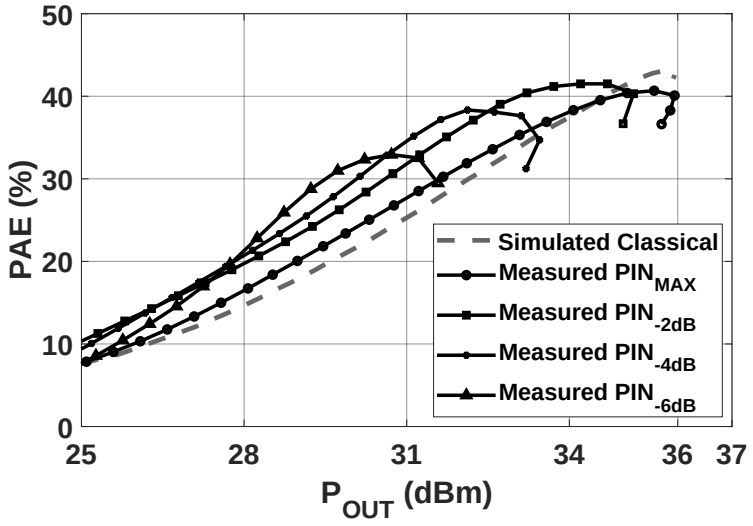
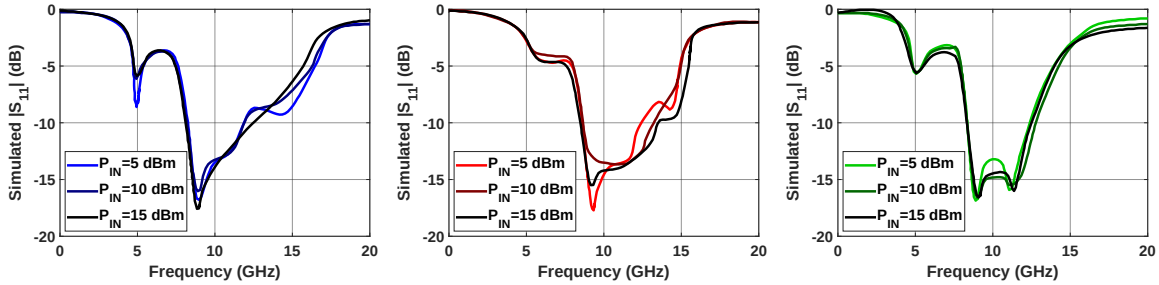


Figure 2.34: Simulation and CW measurements of the dual-input outphasing MMIC operated in pure-mode outphasing at 10 GHz. Mixed mode outphasing curves for measured dual-input outphasing MMIC in 2 dB input power steps.



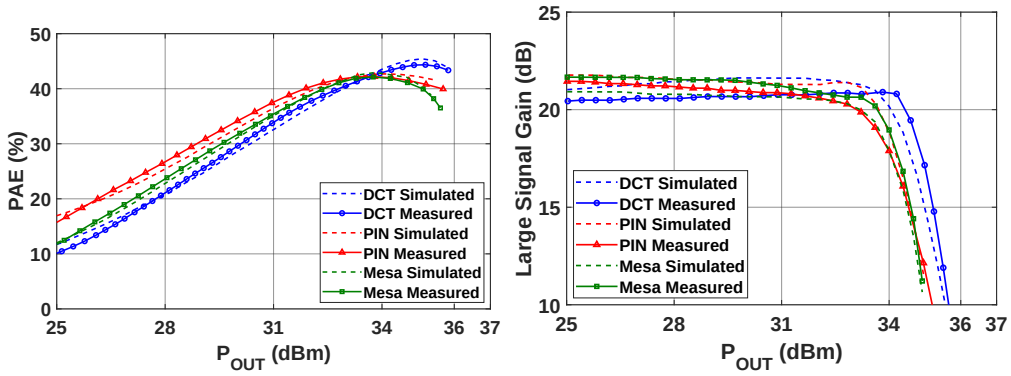
(a) (b) (c)

Figure 2.35: Simulated power-dependent input reflection coefficient at 3 different input drive levels with darker shades as input drive increases for the three different splitter board implementations. (a) DCT diode is shown in blue shades (b) PIN diode is shown in red shades (c) Mesa resistor is shown in green shades.

2.4.5 RFIO System Measurement

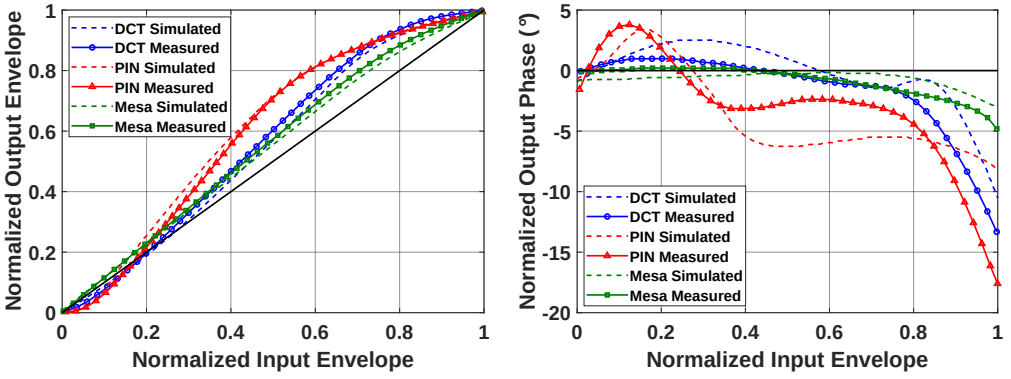
The RFIO system with three different inphasing networks is characterized using the experimental testbench shown in Fig. 4.19. A Rohde & Schwarz SMW200A generates the CW and modulated signals at 10 GHz, and the output signal is analyzed using a Rohde & Schwarz FSW43 vector signal analyzer. The three RFIO test PCBs are shown in Fig. 4.19(b)–(d).

Fig. 2.36 compares the CW drive-up curves for the three different RFIO implementations. All three inphasing variants match closely to the performance expected in simulation. Furthermore, because these



(a) (b)

Figure 2.36: Measured and simulated CW performance of the RFIO PA comparing the three different inphasing networks based on the diode-connected transistor (DCT), PIN diode, and mesa resistor. (a) measured PAE vs output power, (b) measured gain vs. output power.



(a) (b)

Figure 2.37: RFIO: Measured and simulated (a) AMAM and (b) AMPM for the three different splitters.

networks implement mixed-mode outphasing all three show higher PAE in back-off than the pure-mode outphasing (Fig. 2.34) in which a fixed input power is applied. The characteristics of the three variants match the expected behavior from the analysis: the PIN diode version was predicted to be closest to the PAE-optimized optimal input trajectory and indeed has the highest efficiency in back-off, while the mesa resistor shows the expected efficiency-linearity compromise. The Diode-connected HEMT implementation is able to produce the highest output power, likely due to the higher power-handling of this device.

Linearity of the three approaches is compared in Figs. 2.37a and 2.37b, which show the AMAM and AMPM behavior respectively. Again, the measured results match the characteristics predicted in simulation,

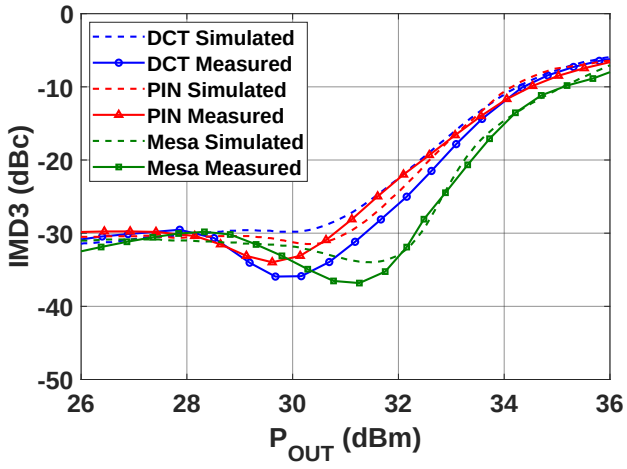
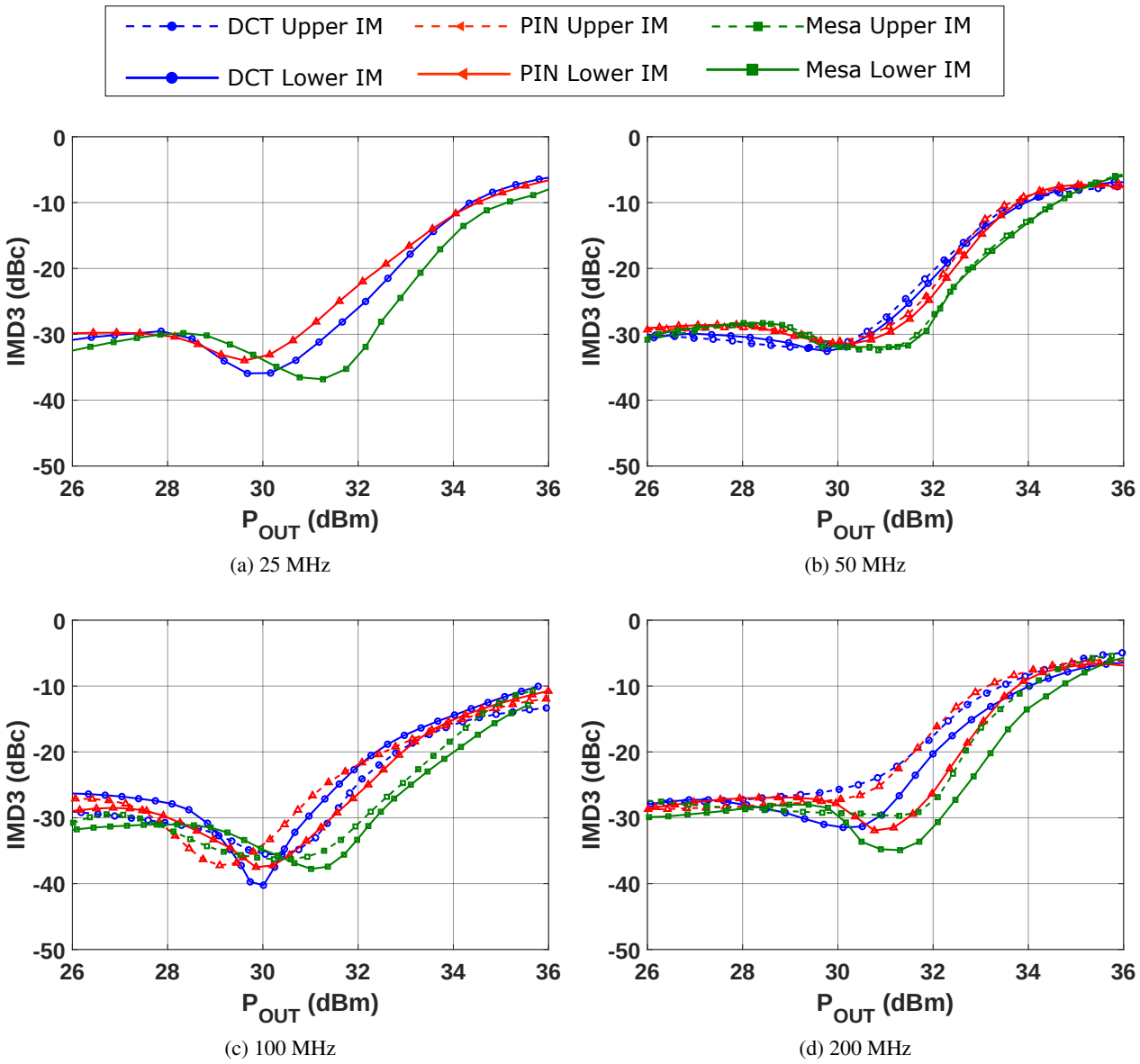


Figure 2.38: IMD3 measurements vs simulation for a 25 MHz tone spacing and averaged power. Upper tones shown, however, no memory effects are present at this tone spacing.

with the PIN diode showing the greatest non-linear response and the mesa resistor the most linear. In particular, in the AMAM response both the PIN and HEMT diodes show an inflection at low power levels. This characteristic is particularly difficult to linearize using DPD compared to the AMAM behavior of the mesa resistor which is more typical of a single-input PA. Similarly, the AMPM response of the mesa resistor RFIO PA shows the lowest phase variation as well as a monotonic behavior.

In order to compare the dynamic performance of the three inphasing networks, the RFIO PAs are characterized using two-tone and LTE modulated signals. Fig. 2.38 compares the IMD3 response over swept power for a 100 MHz tone spacing. As expected, the mesa resistor shows the highest linearity, crossing the -30 dBc threshold at 32.1 dBm power with the upper intermod tone. When driven by an LTE signal with 8.9 dB output PAPR, as shown in Fig. 2.40, the linear mesa resistor response is also seen. The average output powers, efficiency, and ACLR are summarized in Table 2.1. No DPD was applied for signal correction when taking the ACLR spectrum measurements. Interestingly, from this measurement it can also be observed that the diode networks, particularly the diode-connected HEMT, exhibit memory effects. This behavior is attributed to charge relaxation time in these devices which causes memory effects especially for larger instantaneous bandwidth signals. The mesa resistor appears to be best-suited for wide instantaneous bandwidth signals.

The RFIO PAs are compared to related state-of-the-art X-band PAs in Tables 2.2-2.3.



(a) 25 MHz

(b) 50 MHz

(c) 100 MHz

(d) 200 MHz

Figure 2.39: Measured IMD3 response of the three RFIO PAs for two-tone excitation centered at 10 GHz, with 25, 50, 100, and 200 MHz frequency spacings.

Table 2.1: Performance summary for 100-MHz LTE signal.

Tech.	Avg. P_{out}	Output PAPR	Avg. PAE	ACLR$_L$	ACLR$_U$
DCT	28	7.8	27.7	22.2	19.9
PIN	28.1	7.6	33.5	23.1	22.4
Mesa	27.7	7.9	30.2	28.9	27.9

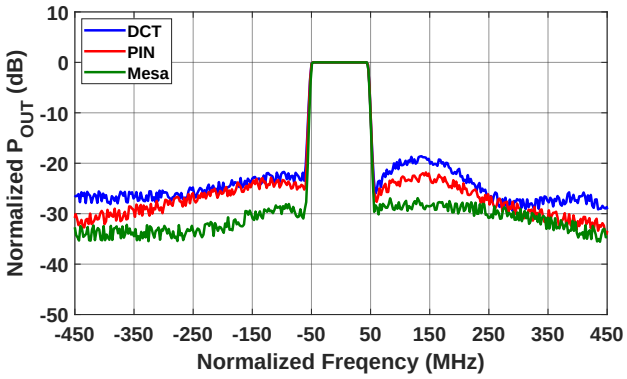


Figure 2.40: Comparison of the three RFIO PAs when characterized with a 100-MHz LTE signal with an 8.9 dB output PAPR. Each spectrum plot is normalized to its peak output power.

Table 2.2: Comparison to state-of-the-art PA MMICs operating near X-band for CW and modulated performance (where reported) PART I.

Ref.	Arch.	Tech.	Freq. (GHz)	Peak P_{out} (dBm)	PAE @ P_{max} (%)	Gain (dB)
[28] 2011	DPA	GaAs	9.5	29	40	7.2
[29] 2013	DPA	0.25μm GaN	6.8–8.5	35	38–50	6–13[a]
[30] 2014	DPA	0.25μm GaN	5.8–8.8	36	30–45[a]	8.5–9
[31] 2015	single-ended	0.15μm GaAs	9.2	40.7	42	29.2
[32] 2015	single-ended	0.25μm GaAs	8–12	40.8–41.8[b]	38–54[b]	27[b]
[33] 2017	single-ended	0.25μm GaAs	6–18	39.6	22	10–16
[34] 2017	DPA	0.25μm GaN	7	38	57	16
[35] 2017	DPA	0.15μmm GaAs	15	26.5	41	17
[36] 2018	LMBA	0.25μm GaN	8–9	41.5	37–48[a]	15–20[a]
[25] 2018	RFIO	0.15μm GaN	9.7	36	63[c]	–
[37] 2018	DPA	0.25μm GaN	5.1–5.9	36.0–38.7	43.2–47.3	14.4–17.3
[38] 2019	DPA	0.25μm GaN	4.5–6.0	35–36	31.8–40.7	7.6–11.6
[39] 2020	supply mod.	0.15μm GaN	9.7	40	50	20
This work	DCT RFIO	0.15μm GaN	9.5–10.5	35.83	43.36	20.5
	PIN RFIO			35.69	39.95	20.9
	Mesa RFIO			35.62	36.51	21

[a]read from graph, [b]pulsed measurements, [c]drain efficiency

Table 2.3: Comparison to state-of-the-art PA MMICs operating near X-band for CW and modulated performance (where reported) PART II.

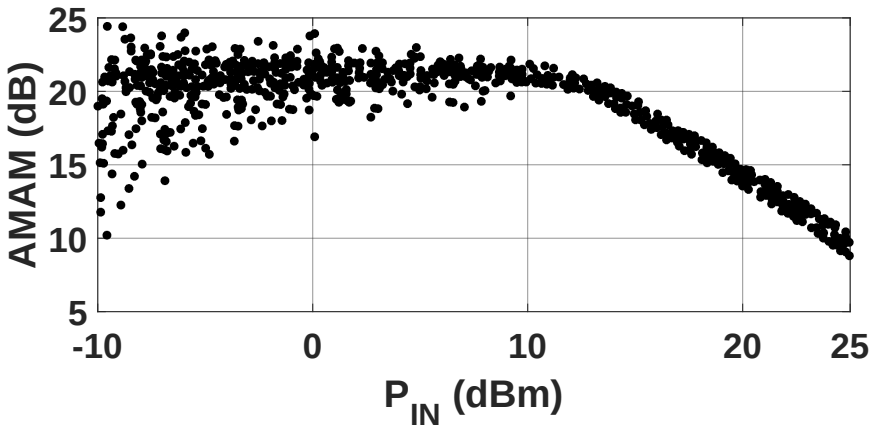
Ref.	Arch.	Tech.	BW (MHz)	Pavg (dBm)	PAPR (dB)	PAE_{avg} (%)	ACLR (dBc)
[29] 2013	DPA	0.25μm GaN	10	27–28	7.8	35–42	-37
[30] 2014	DPA	0.25μm GaN	20	27.6	8.5	35.2	-41
[34] 2017	DPA	0.25μm GaN	56	32	7	40[c]	-36
[35] 2017	DPA	0.15μmm GaAs	20	20	7	–	-23.4
[37] 2018	DPA	0.25μm GaN	80	23.5	–	–	–
[38] 2019	DPA	0.25μm GaN	100	29.3	8	25.7	-34.8
[39] 2020	supply mod.	0.15μm GaN	20	33	7	34[c]	-22[a]
This work	DCT RFIO	0.15μm GaN	100	28	7.8	27.7	-19.9
	PIN RFIO			28.1	7.6	33.5	-22.4
	Mesa RFIO			27.7	7.9	30.2	-27.9

[a]read from graph, [b]pulsed measurements, [c]drain efficiency, *references excluded that data couldn't be obtained for

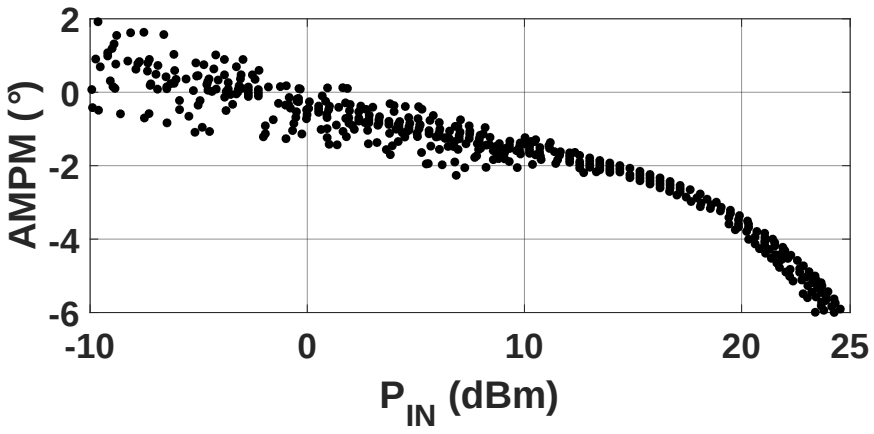
2.5 X-Band MMIC RFIO PA

Being able to fully integrate and RFIO PA into a MMIC would drastically reduce the complexity and size when implementing the architecture into a phased array system. Integrating into a III-V technology also buys the performance benefit of high power density and efficiency. Some of the non-linear elements that were investigated in the previous section are available in several commercial III-V processes. The RFIO PA architecture was designed into the Qorvo GaN 150 nm process.

The outphasing PA design was the same as the one shown in Fig. 2.33. A splitter was designed in the process and integrated in front of the already designed dual-input outphasing PA. The splitter shown in Fig. 2.43 was designed utilizing 4 (2 x 25 um) diode connected transistors. The input split is created by using two half wave-length transmission lines with a $\pm\Delta$ offset. This is a mirror of the outphasing combiner design at the output of the PA. The combiner also utilizes two half-wavelength transmission lines with a $\pm\Delta$ offset. Since diodes were being used as the non-linear elements, bias circuitry was laid out to allow for DC biasing of the diodes used in the splitter. All four diodes in single branch are tied together to one bias. Both branches have separate DC biases for the their respective diodes. This splitter was then laid out with the outphasing MMIC to produce the fully integrated RFIO PA shown in Fig. 2.44



(a)



(b)

Figure 2.41: Dynamic AMAM and AMPM measurements of the mesa resistor RFIO PA with 100-MHz LTE signal.

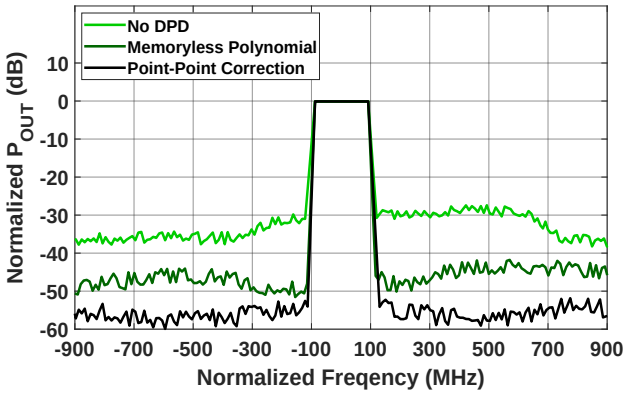
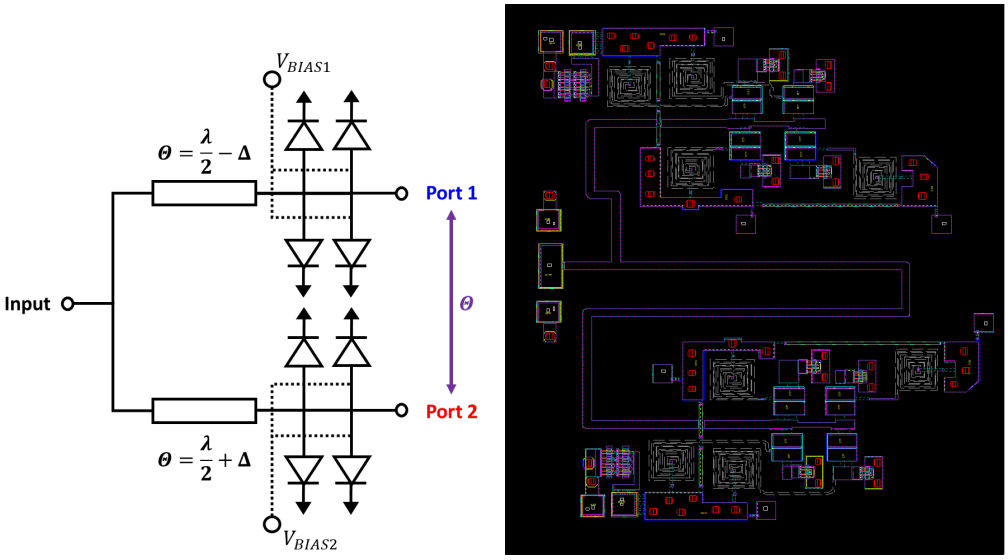


Figure 2.42: Measurements of the RFIO PA with mesa resistor inphasing network driven by a 200-MHz LTE signal, without DPD (light green), with point-by-point DPD (black), and with a 6^{th}-order memoryless polynomial DPD (dark green).



(a) (b)

Figure 2.43: RFIO splitter (a) schematic and (b) layout designed in Qorvo 150 nm GaN es process.

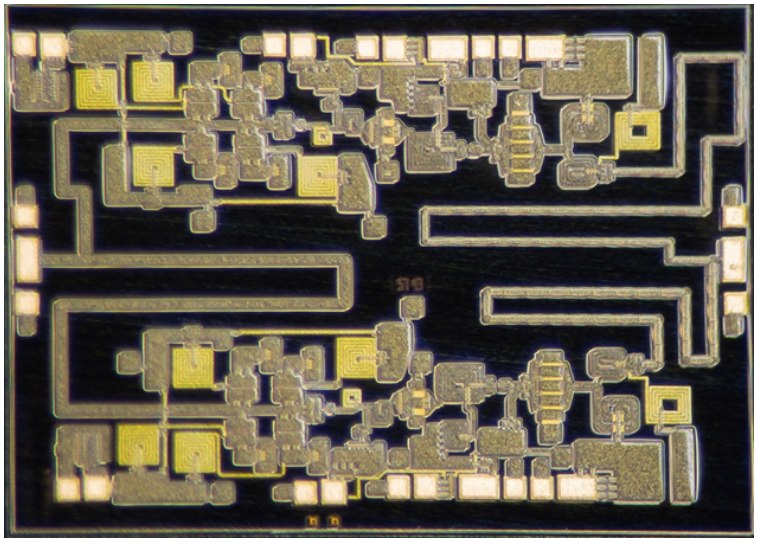


Figure 2.44: RFIO MMIC die photo in Qorvo GaN 150 nm es process. Die is 3.5 mm x 2.3 mm. The outphasing PA is identical to the design shown in the previous section.

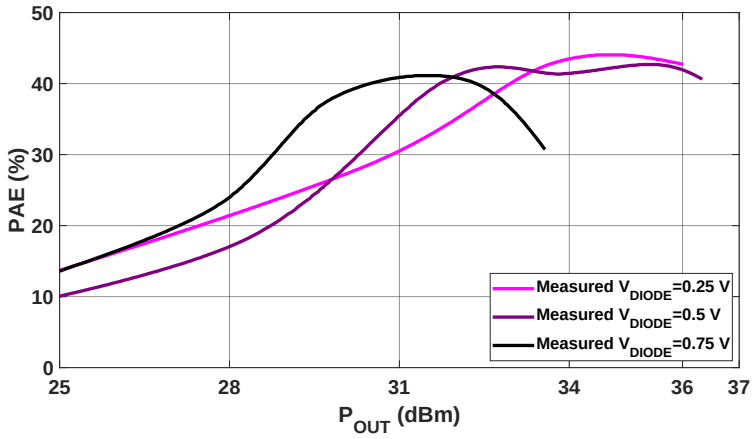


Figure 2.45: Measured RFIO MMIC performance PAE vs P_{OUT} for different bias states for the diodes in the inphasing splitter. Both branches have similar applied biases for this measurement.

The RFIO MMIC PA is 3.5 mm x 2.3 mm and utilizes the same outphasing PA design discussed in the previous chapter that was paired with hybrid inphasing splitter boards. The design was optimized for a 5x5 QFN package in order to allow for easier fabrication. The packaged MMIC was mounted to a PCB and measured utilizing different voltage biases for the non-linear element to achieve different PAE responses. There is improved PAE of greater than 8 points at 8 dB OBO. The MMIC was measured to determine its functionality and the RFIO MMIC performs well. In the future, the MMIC can be measured with numerous different diode bias combinations. Varying both the voltage and the difference of the voltage between the two branches. In addition, a dynamic control scheme can be applied to the diode biases effectively supply modulating the diode bias. This can achieve improved efficiency and linearity characteristics depending on what is optimized but can be implemented more efficiently than a tradition supply modulation architecture since the diode biasing voltage in sub 1 V allowing for significantly more efficient and easy to design supply modulators. This extends the previous work on non-linear element optimization for improved linearity and efficiency by allowing for real-time dynamic control of the non-linear element characteristic. This design specifically utilizes diode-connected transistors as the non-linear element, however, other non-linear elements can also be dynamically change through biasing as well.

2.6 Conclusion

One of the strongest limitations of outphasing power amplifiers is the need for multiple digital processing paths and dedicated processing schemes to achieve the required mixed-mode outphasing signal decomposition. Through the use of the novel RFIO PA architecture the need for the dedicated digital transmitter topology is no longer needed. Looking into how to optimize the design of the inphasing splitter in order to optimize the efficiency and linearity of the RFIO PA showed that there is an optimal design space and the solution is heavily limited by the non-linear element characteristics that are available both in a component form factor and in MMIC processes. The mesa resistor was shown to be the best overall performing implementation of an inphasing splitter providing significantly improved linearity performance while still maintaining improved back-off efficiency performance. The PIN diode had the best overall efficiency performance but suffered more for strong non-linearities and increased memory effects.

The RFIO PA was as successfully implemented completely in a MMIC form factor allowing the topology to be a candidate for phased array systems. The single RF input and single RF output allow for system drop in replacement for traditional linear PA modes. In addition, bias control of the non-linear elements proved to be a promising avenue as a more fine tuning of the more discrete non-linear element characteristics presented from the three different non-linear elements. It also allows for the possibility of active supply modulation of the non-linear elements to dynamically track the signal envelope with a significantly easier implementation than that over classic PA supply modulator implementations.

Chapter 3

Wide-Band Outphasing Combiners

Frequency-reconfigurable transmitters are of interest to many systems due to their operational flexibility. While all-digital transmitters are a natural approach to eliminating the conventional narrowband analog output stage, they are typically implemented in CMOS and are therefore limited in output power and efficiency [40]. Frequency-reconfigurable RF front-ends in III-V technologies are therefore needed to address requirements for efficient, high-power operation over a broad frequency range.

The outphasing architecture is compatible with digital transmitter design due to the multiple phase-controlled input signals, while the load modulation inherent to Chireix outphasing systems provides efficiency enhancement at output power back-off [20]. Conventional non-isolating outphasing PAs, however, are typically narrowband due to the typically used structure comprising a quarter-wavelength combining network with reactive shunt elements [41]. This design addresses this drawback by developing a frequency-reconfigurable outphasing combining network that presents resistive loading to the two branch PAs over a 6–12 GHz range. Although the focus of this design is on the combining network only, the 250-nm GaAs implementation is compatible with watt-level, efficient MMIC front-ends.

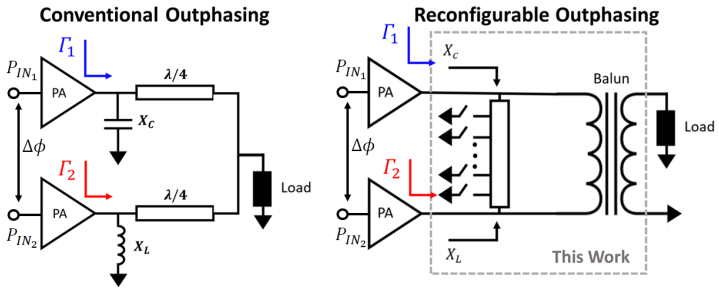


Figure 3.1: (a) Conventional narrowband outphasing structure. (b) Simplified schematic of the reconfigurable outphasing combining network. An octave-bandwidth balun provides single-ended to floating load conversion, while a transmission line with shunt switches provides reconfigurable shunt compensating reactances X_C and X_L.

3.1 Frequency-Reconfigurable Outphasing

A simplified schematic of the prototype is shown compared to the conventional outphasing architecture in Fig. 3.1. In Chireix outphasing systems, the relative phase of the two branch PA output signals controls the input impedances to the two input ports of the combiner. The resulting dynamic load modulation is used for output power control, resulting in efficiency enhancement in output power back-off.

An outphasing combiner comprises two major components: a single-ended to floating load conversion which allows the load to be driven differentially by the two branch PAs, and reactive compensating elements allowing the designer to cancel the reactive variation in the two input impedances at two output power levels. Here, the floating load is implemented using a broadside-coupled transformer in place of the conventional quarter-wavelength transmission lines. This structure, when implemented using broadside coupled lines, can operate over three octaves of bandwidth [42].

The reactance compensation elements are replaced with a reconfigurable shorted stub, enabling near-resistive load trajectories to be presented at the input planes to the combiner over a range of frequencies spanning an octave. In a conventional outphasing PA, where it is assumed that the load trajectory presented to the branch PAs is ideally resistive, reactances X_C and X_L are chosen as complex conjugates [20]. These reactive elements offset the load impedance trajectories presented to the two branch PAs to move them close to the real axis. For broadband operation, fixed shunt reactances pose a challenge because their frequency

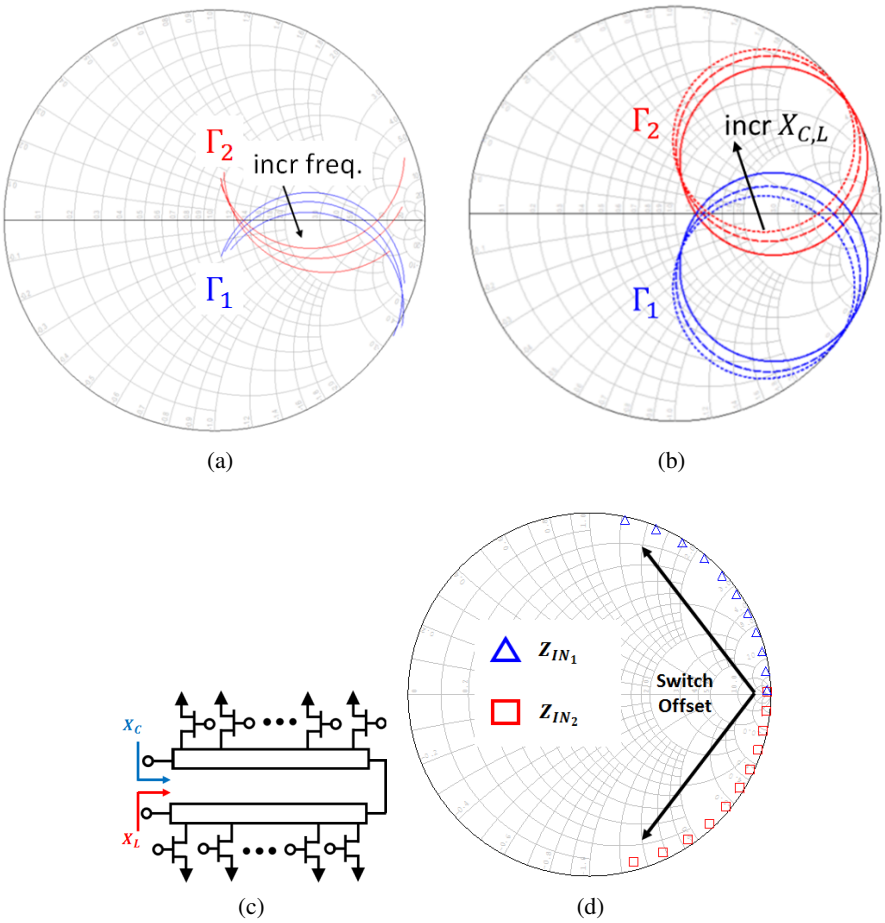


Figure 3.2: Reconfigurable outphasing combiner operation: (a) conventional outphasing combiner input impedances as reactance varies; (b) frequency-dependence (20% total increase in frequency) of outphasing input impedance trajectories for a conventional network; (c) sketch of half-wavelength transmission line with shunt switches (reduced number shown for clarity); (d) complex-conjugate input impedances to the line when a single switch is turned on (starting from the center and moving towards one side).

responses are no longer conjugates. This is illustrated in Fig. 3.2(b), where only a 20% increase in frequency causes the outphasing trajectories to deviate from the resistive axis.

We observe that a half-wavelength transmission line with a shunt short placed arbitrarily along the line will result in complex conjugate impedances looking into the two ends of the line. By placing multiple shunt switches along a half-wavelength line at the nominal design frequency the compensating reactances can be reconfigured, as illustrated in Fig. 3.2. Alternatively, non-conjugate reactances can be used to compensate for non-idealities in the combining structure. Broad frequency reconfigurability is achieved by activating at most two switches along the reactance compensation line. If the line is a half-wavelength at the lower

Figure 3.3: Standard broadside-coupled transformer cross-section (a) and modified transformer cross-section (b).

frequency range, for any higher frequency complex conjugate reactances are achievable using two switches. Here, due to size constraints on the MMIC, simulations were performed to determine the minimum length of line needed to realize the required states which for this design is a guided half-wavelength at 11 GHz.

3.2 MMIC Implementation

In order to implement the broadband transformer, the two different structures with cross sections illustrated in Fig. 3.3 were investigated. The cross section in Fig. 3.3(a) shows a standard broadside coupled line structure where the blue layer corresponds to top metal layer 2, the red layer corresponds to metal layer 1, and the orange layer corresponds to the dielectric passivation layer between them. In Axiem simulation, this structure has 1.5 dB insertion loss and results in undesirable rotation of the outphasing contours with frequency. This causes significant asymmetry between the loading of the two ports. Cross section (b) shows the adjusted broadside coupled structure where the added dark blue layer in the same plane as the orange layer represents a solid via connection. This creates an effectively thick metal layer and reduces the insertion loss of the structure to 0.3 dB. This structure shows simulated performance more closely matching the circuit simulation of broadside coupled lines, due to the increased coupling between the two metals.

From circuit element models in AWR, a transformer unit cell was chosen that produces outphasing performance over the desired bandwidth region. The transformer has a non-unity (1.7x) impedance transformation ratio. In order to achieve the overall unity transformation ratio desired for the outphasing trajectories, two transformer unit cells are placed back to back, as shown in Fig. 3.4. The output section of the combiner is made by constructively stacking two cells to double the transformation ratio increasing the dynamic range of the outphasing load modulation.

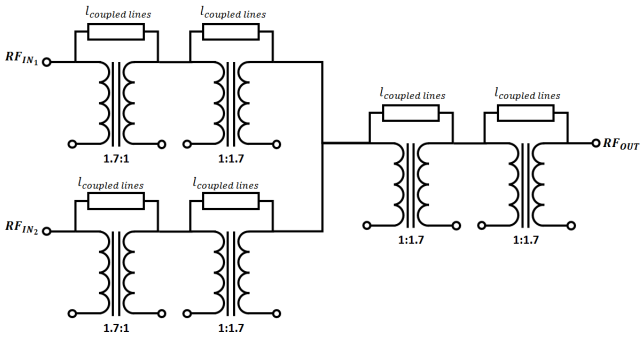
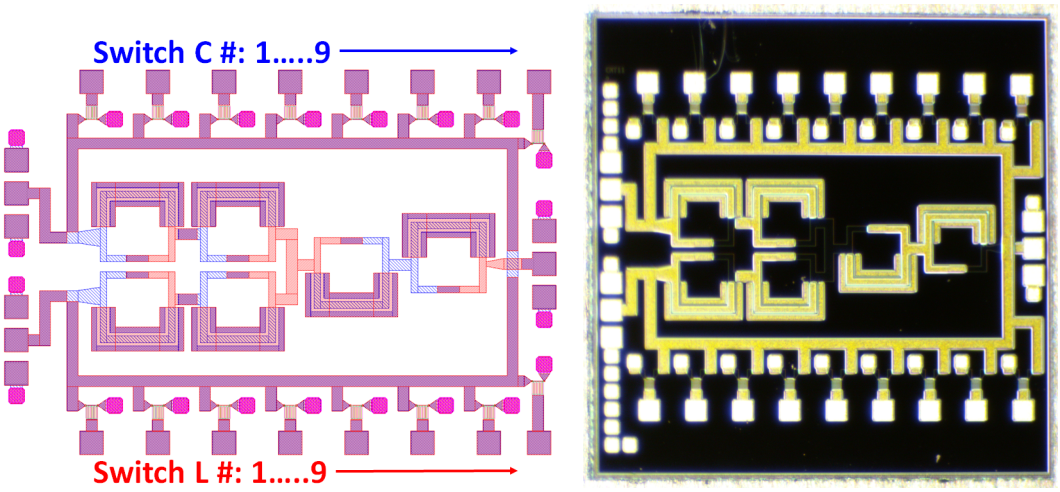


Figure 3.4: Circuit diagram of the overall transformer based combining structure.



(a) (b)

Figure 3.5: Layout and photograph of the 2.5 mm x 2 mm 250-nm Qorvo GaAs MMIC prototype.

The layout and photograph of the fabricated MMIC are shown in Fig. 3.5. The tunable reactance compensation components are implemented using switched shorted stubs that can be reconfigured to a length between 250 μm and 7 mm in intervals of 250 μm. The shunt switches are E-mode 25 μm 8-finger pHEMTs. The transformer structure lies at the center, while the reconfigurable transmission line is wrapped around the edge for access to the switch gates. An airbridge allows the output port to pass under the transmission line.

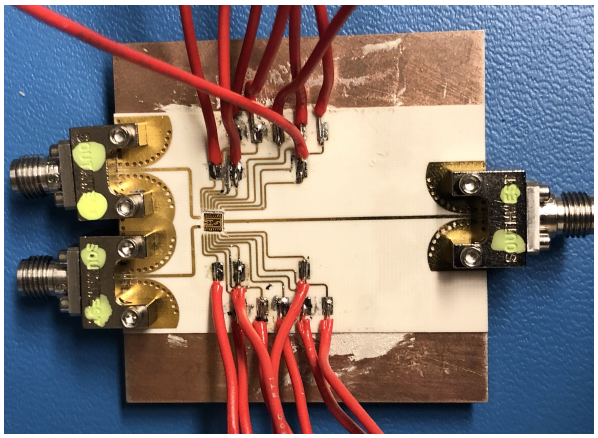


Figure 3.6: Photograph of the experimental break-out board used to characterize the outphasing combiner MMIC.

3.3 Measurements

In order to characterize the combiner performance across frequency, the MMIC is mounted on a test fixture, shown in Fig. 3.6. A standard SOLT calibration is performed at the three connectors, and a loss-less simulated model of the feed line and the bond-wire is used to de-embed the test fixture. Three-port S-parameter measurements are recorded across a 6-14 GHz frequency range for each of the switch state combinations used (note that not all possible combinations are tested because only certain ones have utility). Then, the measured S-parameter files are simulated in AWR using the outphasing test bench shown in simplified schematic form in Fig. 4.19 and the input port reflection coefficients are plotted as a function of the relative outphasing angle. While in previous work we have used the network analyzer's coherent phase mode to directly capture input reflection coefficient [43], we note that the method used here is equivalent and more compatible with the large number of possible states tested.

The input impedance trajectories to the MMIC outphasing combiner based on measured S-parameters are summarized in Fig. 3.8. The corresponding switches ON at each frequency are given in Table 3.1, with all other switches off and with switches numbered as indicated in Fig. 3.5. As can be seen in Fig. 3.8, the combiner presents loading conditions at the input ports that are nearly symmetric about the real axis from 6 GHz up to around 12 GHz where the performance of the transformer starts to break down. Outside of this frequency range, a clockwise rotation with frequency can be observed.

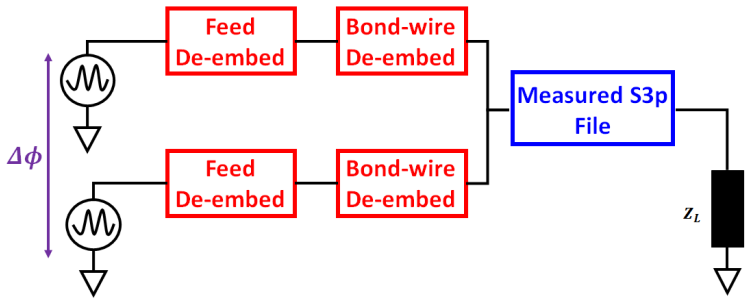


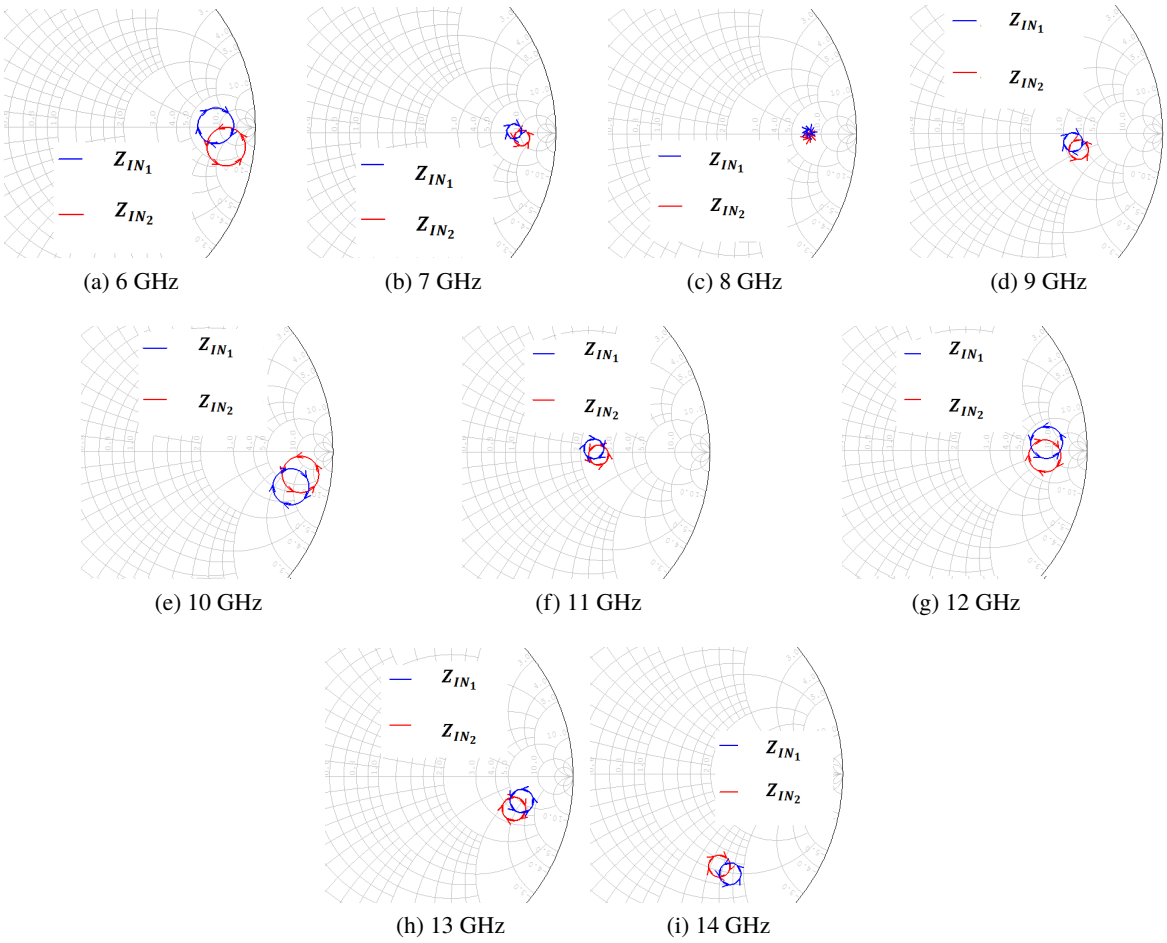
Figure 3.7: Simplified schematic of the simulation test-bench used to determine the port input impedance trajectories as a function of outphasing angle based on measured 3-port S-parameter data.

Table 3.1: Summary of switch states for operation across 6-14 GHz.

Freq.	Switch C	Switch L
6 GHz	-	2
7 GHz	-	2
8 GHz	-	3
9 GHz	8	3
10 GHz	-	5
11 GHz	8	1
12 GHz	7	4
13 GHz	7	3
14 GHz	6	3

The measured outphasing contours are compressed compared to the ideal behavior, although load modulation is still observed over the majority of the band. The contour compression is attributed to additional loss in the network most likely due to greater than anticipated loss in the transformer. The EM simulated loss of the breakout board is shown in Fig. 3.10. This loss includes the connector loss and is aggregated across the input and output. While the loss introduced by the breakout board is significant there is still approximately 6 dB of loss that is not accounted for. The impact of loss on the outphasing contours is illustrated in Fig. 3.9, where the smaller, solid contours represent an ideal outphasing network with each input branch preceded by loss. Here it can be seen that loss alone eliminates overlap between the two input trajectories, which is compensated for in our structure through reconfiguration of the shunt reactances.

Despite the limited outphasing range observed in measurement, the reconfigurable structure demonstrates successful compensation over an octave band. Fig. 3.11 compares the input impedance trajectories at 13 GHz when the shunt reactance elements are controlled to the nominal case in which they are not reconfigured.



(a) 6 GHz (b) 7 GHz (c) 8 GHz (d) 9 GHz

(e) 10 GHz (f) 11 GHz (g) 12 GHz

(h) 13 GHz (i) 14 GHz

Figure 3.8: Measured results summary showing the combiner input impedance trajectories as outphasing angle is swept.

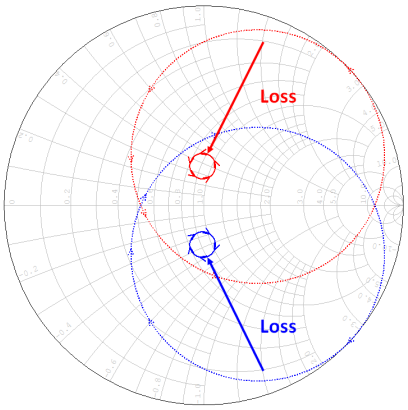


Figure 3.9: Simulated effect of circuit loss on input trajectories, comparing ideal lossless outphasing contours (dashed) to the outphasing contours with 10 dB of loss (solid).

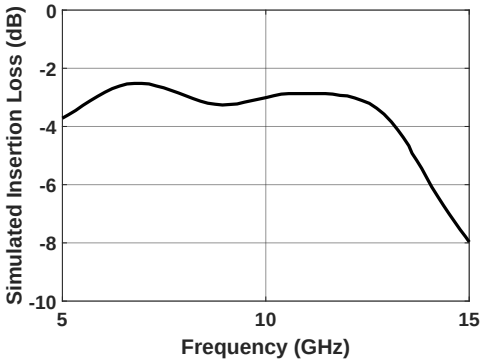


Figure 3.10: EM simulated insertion loss of breakout board including connector loss. Loss is aggregated for both the input and output.

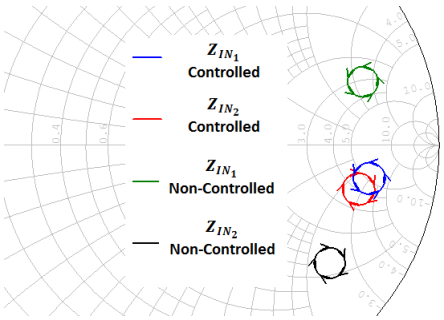


Figure 3.11: Measured outphasing contours at 13 GHz with switch reconfiguration (blue and red) compared to without switch reconfiguration (green and black) for port 1 (blue and green) and 2 (red and black) respectively.Similar behavior is observed at other frequencies.

The controlled case provides a substantially improved loading condition to both branch PAs.

3.4 Conclusion

This MMIC presents a reconfigurable outphasing combiner operating over an octave bandwidth. The switchable shunt reactance line maintains symmetric outphasing operation and resistive loading to the PAs across most of the band. Although a resistive impedance target is assumed here, the technique can be adapted to track the desired load impedance for a realistic broadband PA. Combining this technique with optimally designed branch PAs will allow for ultra-wideband outphasing operation through combiner reconfiguration.

Chapter 4

DIRO PA

Transmitters operating at K- and Ka-band are in demand for a variety of applications relating to high-speed communications and telemetry [44,45]. The 20–40 GHz frequency range contains multiple frequency bands for satellite communications, including telemetry channels over 26.5–32 GHz [44]. Simultaneously, there is increased interest in this frequency range due to emerging 5G wireless communications systems. With rapidly evolving spectrum allocations, frequency-reconfigurable power amplifiers (PAs) are advantageous in enabling multi-function transmitters and new spectrum-management scenarios [46]. The operational and frequency agility allows for reduced time to deployment and redundancy in overall system architecture, saving both cost and size.

Frequency-reconfigurable transmitters are particularly suited to all-digital (CMOS) implementations, for example direct-digital transmitters operating without conventional up-converting paths such as software-defined radios. This highly-digital approach has been particularly effective in sub-6 GHz applications [47–49]. In millimeter-wave (mm-wave) cellular and satellite communications applications, on the other hand, system specifications effectively require III-V compound semiconductor technology for its power density and efficiency capabilities. Operation with high efficiency over a wide range of output power levels is furthermore critical for high-bandwidth communications, and increasingly desired in satellite applications, for example to overcome spectrum access limitations [45]. Therefore, III-V PAs are needed that can be

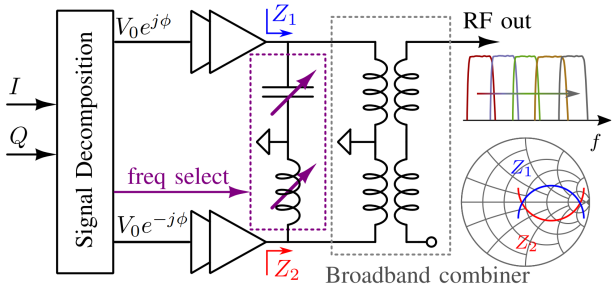


Figure 4.1: Overview block diagram of the frequency-reconfigurable Chireix outphasing architecture.

operated with CMOS-level input powers while providing frequency-reconfigurable efficiency enhancement at mm-wave frequencies. This approach, sketched in Fig. 4.1, employs a relatively high power-density output stage driven and controlled by a low-power digital controller.

The Doherty PA (DPA) has been successfully demonstrated in the literature to provide back-off efficiency enhancement at K- and Ka-band in Gallium Arsenide (GaAs), with the majority of demonstrations using 150-nm GaAs [50–55] or 100-nm GaAs [56]. Power-added efficiency (PAE) as high as 42% at peak output power and 31% at 6-dB output power back-off (OBO) has been reported [51]. While some frequency reconfigurability has been demonstrated, for example using a reconfigurable input matching network to extend the operating frequency to a 3-GHz band [51], and a multi-band DPA in Silicon Germanium (SiGe) BiCMOS [57], the majority of efficiency enhancement literature at K- and Ka-band focuses on single, relatively narrow-band operation. Frequency-reconfigurable K-/Ka-band single-ended PAs have been demonstrated, for example the BiCMOS PA in [58] covering 24.3–35 GHz using varactor tuning.

A SiGe DPA with frequency reconfiguration over 40–60 GHz is reported in [59], in which active impedance synthesis rather than tunable passive elements is used to maintain performance across the band. Unlike in conventional DPAs, in [59] a dual-drive approach is taken, and both the relative amplitude and the relative phase of the two inputs is varied. In effect, this approach is related to that of a combined Doherty-outphasing driving approach such as is described in [60], or the Doherty-outphasing continuum technique for broadband PA operation in [61]. The dual-drive load modulated PA, in particular the outphasing PA [19, 20, 25, 62–65], is attractive for frequency-reconfigurable PAs as the approach can effectively exploit highly-digital signal component generation for input signal generation, independent of the carrier frequency.

This design presents a frequency-reconfigurable dual-input PA operating over 18–38 GHz based on the Chireix outphasing architecture for efficiency enhancement at OBO. The demonstrator MMIC is implemented in a GaAs pHEMT process. The outphasing architecture, which uses phase decomposition of the input signal for active load modulation, is selected based on its potential for high operating efficiency. In particular, because the two branch PAs are both saturated throughout the efficiency-enhancement power range, the Chireix outphasing PA has the theoretical potential to demonstrate higher efficiency compared to the DPA.

This is the highest-frequency III-V Chireix outphasing PA published to date, with prior demonstrations at frequencies up to X-band [25, 62, 63]. One CMOS implementation demonstrates Chireix outphasing at a fixed 28-GHz operating frequency with a 3-GHz operating band (10.7% fractional bandwidth), with 53% peak drain efficiency and 36% drain efficiency at 6-dB OBO [66]. The 71% effective fractional bandwidth with frequency reconfiguration presented in this work is the highest frequency tuning range reported for frequency-reconfigurable Chireix outphasing PAs, compared to the 35% fractional bandwidth tuning range in L-band in [64].

The frequency-reconfigurable K-/Ka-band Chireix outphasing PA presented in this work uses an ultra-wideband combining structure based on a coupled line transformer, and frequency-reconfigurable shunt reactances to maintain the desired load trajectories across the entire frequency range. Compared to our related frequency-reconfigurable outphasing network in [67], this work presents a simplified structure exhibiting lower loss, and demonstrates the full outphasing PA including two-stage branch PAs. The outphasing PA MMIC is measured in CW over a 18–38 GHz range to characterize output power, efficiency, and gain, and with 100-MHz and 200-MHz modulated signals centered at 19.5 GHz.

Section 4.1 briefly reviews outphasing operation and the bandwidth limitations of conventional outphasing structures. The frequency-reconfigurable outphasing architecture used in this work, including the wideband power combining structure and frequency-reconfigurable shunt reactive elements, is described in Section 4.2. Section 4.3 provides details of the MMIC design and implementation. CW and modulated measurements are presented in Section 4.4.

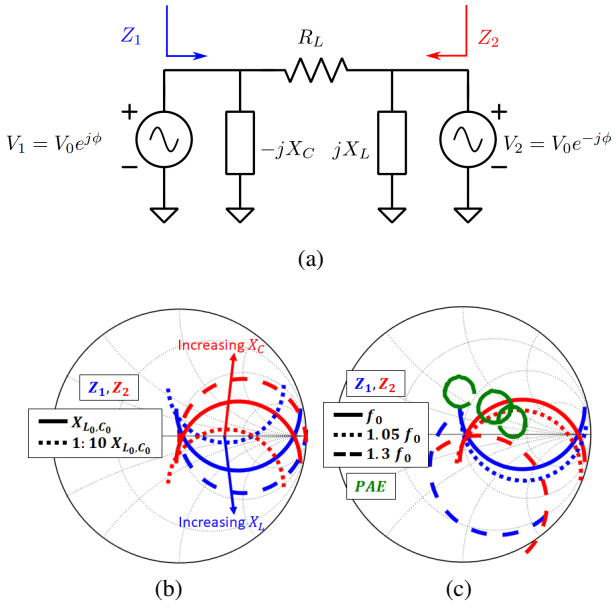


Figure 4.2: Conceptual operation of the Chireix outphasing PA. (a) Simplified schematic. (b) Load trajectory control through manipulation of shunt reactances X_L and X_C, showing a decade increase in the shunt reactances from their nominal values. (c) Load trajectory degradation for an ideal Chireix outphasing combiner when frequency is deviates by 5% and 30% from the nominal design frequency, compared to simulated PAE impedance targets based on the MMIC device.

4.1 Outphasing Theory and Limitations

The generalized outphasing system employs a lossless (non-isolating) power combiner driven by two equal-sized branch PAs. Conceptually, the system is commonly modeled as in Fig. 4.2, in which the branch PAs are treated as voltage sources and drive a floating load. The two inputs are assumed to have equal amplitude and some relative phase 2ϕ, with the input impedance to the combining network controlled by the relative phase. When complementary shunt reactances $|X_L| = |X_C|$ are included, the load trajectories can be designed for a desired dynamic range and peak susceptive loading of the two PAs [20], as illustrated in Fig. 4.2b.

Several considerations must be applied to the conceptual model in Fig. 4.2, including amplitude-modulation of the input signals to maintain gain over output power, and practical implementations of the floating to single-ended load conversion. Furthermore, as described in the next section, for a reconfigurable-frequency outphasing architecture both the shunt compensating reactances and the branch PA design for load modulation must be considered.

While in classical outphasing analysis the combiner input amplitudes V_0 [Fig. 4.2a] are assumed equal and constant, in practical systems mixed-mode operation is used, in which V_0 is varied as a function of the desired output power [19]. In the high-power (outphasing) regime, this amplitude variation serves to maximize gain while keeping the branch PAs in saturation. This adjustment of the drive amplitude to keep the branch PA output approximately constant as the load varies is the reasoning behind treating the branch PAs as voltage sources (as in Fig. 4.2). In a practical system, the branch PAs will not behave as ideal voltage sources but will instead have some equivalent output impedance, modeled as a parallel RC network in the MMIC design. This output impedance is designed so that the branch PAs do not substantially load the combining network, and the combining network can be adjusted to compensate for any loading if necessary.

In output power back-off operation, the outphasing angle is held constant and amplitude control is used to extend the dynamic range of output power [20]. Although the mixed-mode outphasing drive signal generation used in this work is not a novel technique, we note that it is particularly important for mm-wave PAs where device technologies limit the available branch PA gain. Furthermore, although not explored in this work, allowing the two PA amplitudes to vary asymmetrically can improve operating bandwidth [61] and potentially back-off efficiency [60].

While some RF outphasing PAs have used wideband balun combining structures as a means to control harmonic terminations [68], the majority of outphasing PAs in the literature employ a quarter-wavelength transmission line structure to convert the floating load of Fig. 4.2 to single-ended [19,25,63,64]. Alternatively, an all-transmission-line combiners can implement both the floating-to-single-ended conversion and reactance compensation elements [22, 69]. Both of these techniques are well known to limit RF bandwidth; for example, frequency limitations in conventional outphasing structures are studied in [41]. Fig. 4.2c illustrates the frequency degradation that results when a typical quarter-wave line based impedance transformer is used in the power combining structure. The passive combiner produces a clockwise rotation in the Smith chart as frequency increases. This is in opposition to the counter-clockwise rotation with frequency of the target load impedances for efficiency (illustrated here based on simulated load-pull data for the MMIC device). While the combiner can to some extent be co-designed with the PA to mitigate this effect [70], previous outphasing demonstrations have been limited to at most 35% fractional bandwidth.

4.2 Frequency-Reconfigurable Outphasing Architecture

For broadband and frequency-reconfigurable outphasing operation, the two critical modifications to the general outphasing architecture relate to the floating to single-ended load conversion, and to the shunt reactances $\pm jX$. The MMIC-based design approaches to these challenges are described in this section.

4.2.1 Broadband floating to single-ended load conversion

The ideal transformer, while impractical at the sub 6-GHz frequencies where most Chireix outphasing demonstrations are operated, can theoretically convert a floating to single-ended load over an arbitrarily wide bandwidth. In fact, in his original 1935 outphasing work [65], Chireix employed transformer-based structures. At mm-wave frequencies, transformer structures again become attractive candidates.

Balun structures have been integrated in planar structures and can provide ultra-wideband power combining characteristics at mm-wave [42, 71]. For outphasing operation, these structures must be modified to provide the desired load trajectories when operated with arbitrary input phase. In this work, a spiraled coupled line structure with a 1:1 transformation ratio, shown in Fig. 3.1, is employed to operate as a wideband power combining structure. The two secondary transformer lines are combined serially through the coupled output line, while the primary-side lines are terminated in a RF short. In this section, the RF output port is designated as port 3, while the two combiner inputs are ports 1 (IN1) and 2 (IN2).

The main operating mode for a conventional integrated balun is inductive coupling produced by the long electrical length of the coupled lines. As the length of the lines is modified, the dominant coupling effect shifts between inductive and capacitive coupling of the lines. Capacitive coupling reduces isolation between the two input ports, allowing greater load modulation in outphasing operation, but at the expense of bandwidth. This outphasing vs. bandwidth trade-off is illustrated in Figs. 4.3 and 4.4, which compare capacitive-dominant and inductive-dominant combiner implementations. By introducing spiral inductance in the coupler, the frequency range of outphasing operation is increased, even while the conventional balun operation bandwidth is decreased [72].

For simulation accuracy the balun structure is designed using increasingly precise simulation processes.

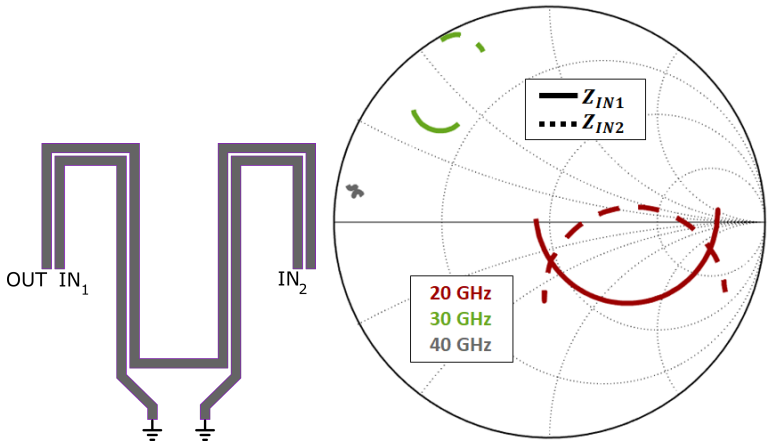


Figure 4.3: Simulated combiner response for edge coupled (capacitive-mode) combiner based on EM extraction. (a) Combiner layout and port definitions. (b) Simulated outphasing operation across frequency when port 3 is is loaded with 50 Ω and ports 1 (IN1) and 2 (IN2) are driven with equal amplitude and swept relative phase.

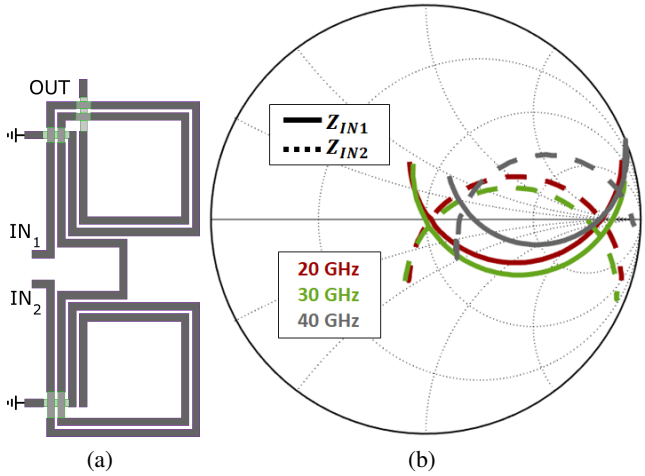


Figure 4.4: Simulated combiner response for implementation of spiral edge coupled (partially inductive mode) combiner. (a) Combiner layout and port definitions. (b) Simulated outphasing operation across frequency when port 3 is loaded with 50 Ω and ports 1 (IN1) and 2 (IN2) are driven with equal amplitude and swept relative phase.

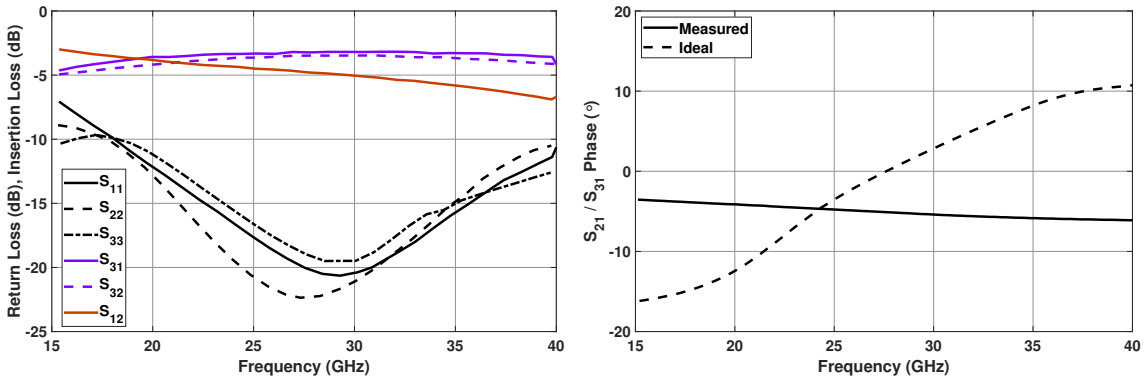
The design begins with a circuit-based model which is designed and simulated in AWR Microwave Office including using the AXIEM EM solver. As the design is refined, it is then simulated in HFSS for validation. The simulated performance of the structures in Figs. 4.3 and 4.4 are based on this HFSS model. In these simulations, the two input ports are driven with equal-amplitude power sources with 50 Ω characteristic impedance, while the relative phase of the two inputs is swept to produce the outphasing load trajectories.

The partially inductive-coupling dominant design of Fig. 4.4 is selected here in order to produce the desired outphasing operation while still maintaining a sufficient bandwidth. (In this work, bandwidth is limited by the input and interstage matching networks of the branch PAs as described in Section 4.3.) The broadband combiner is fabricated as a standalone structure and its S-parameters are measured as shown in Fig. 4.5. The measured performance meets the design goals of providing a better than 10-dB return loss at all ports (we note that the 50-Ω match design goal for the input ports 1 and 2 are specific to the device selected, as described in Section 4.3), while providing an even power ratio at the input ports.

An ideal broadband combining structure for outphasing will maintain a constant phase response across the entire bandwidth for both input ports, so that the combiner input impedance trajectories are maintained as symmetric about the resistive axis. For realistic branch PAs, a negative phase shift with frequency would track the frequency-dependant load impedance targets of the devices, as indicated in Fig. 4.5b. Alternatively, as is done here, a flat phase response is maintained for the combiner and the device target phase response is approximated through selection of the reactive shunt elements to compensate for the output reactance of the device.

4.2.2 Compensating reactances

As the RF carrier is varied over a broad frequency range, the Chireix compensating reactances (whether implemented using lumped or transmission line elements) will no longer present complementary reactance values. Therefore, reconfigurable elements are used as illustrated in Fig. 3.1. These reconfigurable reactances are implemented using shorted stubs, with length controlled through five PIN diode switches to ground on each stub. To avoid shorting the dc supply, dc blocking capacitors are placed at each stub. Single-switch control on each stub is used to select the optimum load trajectory for maximum efficiency over the dynamic



(a) (b)

Figure 4.5: Measured S-parameter magnitudes of standalone power combining structure. (a) Measured magnitude response. (b) Measured phase response, compared to ideal transmission phase based on simulated load-pull of the device. The negative phase shift with frequency of the physical transformer is compensated for using the shunt reactive elements.

range.

The stub design begins with the assumption that the ideal load trajectories to be presented to the branch PAs are resistive, as is assumed in outphasing theory (see Fig. 4.2). Based on an ideal floating-to single-ended combiner with a load resistance $R_L = 50\ \Omega$, the nominal $\pm jX$ reactances values of 80-200 Ω result in the desired load trajectories shown in Fig. 4.2b. When implemented as shorted transmission-line stubs, these reactances correspond to 50 deg and 80 deg electrical lengths, or approximately 0.5-0.9 mm over 20–38 GHz. In practice, as described in Section 4.3, the lengths can be adjusted to also compensate for variations in the optimal branch PA load trajectories as frequency varies.

4.3 MMIC Implementation

The demonstrator MMIC is designed in the WIN semiconductor GaAs PIH-110 process. This process has a 850 mW/mm power density at a 4 V supply voltage, and a load-pull performance of 50% saturated PAE at 29 GHz for a 2×50 μm device [73]. The 18–38 GHz RF frequency range is divided into five overlapping bands, each with at least 2 GHz RF bandwidth. A simplified schematic of the full frequency-reconfigurable outphasing architecture is shown in Fig. 4.7.

A two-stage topology is used for the branch PA in order to improve the gain of the branch amplifier. This

also reduces the amount of input impedance variation to the outphasing PA resulting from load modulation, because the branch PA is more unilateral. If the branch PA gain is low, the input impedance will vary as a function of outphasing angle, producing an input match that varies with output power [74]. The final-stage transistors are 4 x 40 μm devices, biased at a nominal 9.1 mA quiescent current while the drivers are 2 x 25 μm, biased at 2.86 mA. All transistors are operated at a 4 V supply voltage. The input and inter-stage matching networks are implemented as five-element band-pass networks using the decoupling capacitor and bias lines as matching elements.

The input and interstage matching networks are designed to maximize performance across the entire reconfigureable bandwidth while remaining stable. The networks utilize a purely static reactive match, i.e. without any reconfigurable or tunable elements. Performance is traded for simplicity in the design and the number of elements is kept low for both matching networks. The topology and equivalent component values are shown in Fig. 4.6. Overall performance of the amplifier could potentially be improved through the use of tunable networks in the interstage and input matching networks to improve the Q of the match, although at the cost of increased complexity.

The 4 x 40 μm device size selected for the output stage is convenient because the optimal load for peak power is close to 100 Ω, avoiding the need for output matching after the differential to single-ended conversion. We note, however, that for a different device size impedance matching can be implemented in the power combining structure, i.e. by using an $N:1$ conversion. Because the output power combiner bandwidth capabilities greatly exceed those of the input and interstage matching in the branch PAs, the bandwidth degradation associated with a non-unity transformation ratio would not prevent use of this architecture.

Operation in a load-modulated architecture requires branch PAs to be designed for a load trajectory rather than a fixed load impedance. In other words, the target load impedance for the PAs at both peak power and at a desired output back-off (here, 6-dB OBO is used) must match the active load trajectory presented by the combining network in outphasing operation. The combiner (ideally) presents a resistive loading trajectory at its inputs, which is also the desired loading for the transistor at its intrinsic current plane. In a broadband or multi-band MMIC implementation, therefore, the combiner is ideally directly connected to the drain of the device. Including a bias tee between the transistor and outphasing combiner would introduce dispersion,

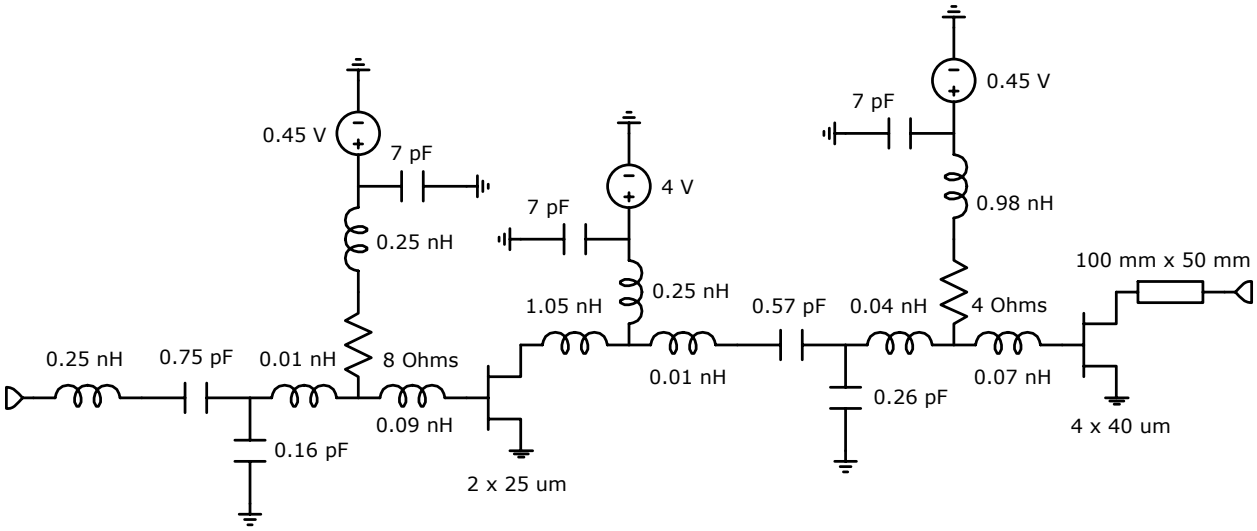


Figure 4.6: Simplified circuit schematic of branch amplifier layout with component values. Input and interstage matching network designed to maximize operation across entire reconfigureable bandwidth while remaining stable.

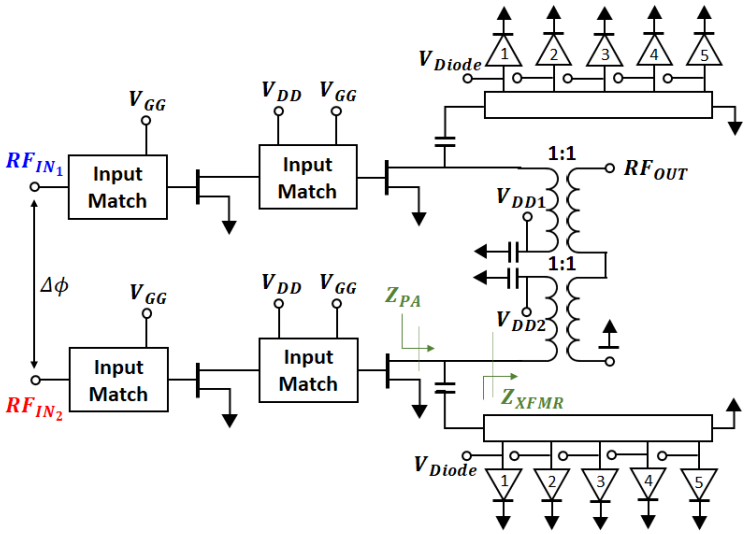


Figure 4.7: Simplified circuit schematic of the frequency-reconfigurable outphasing PA MMIC. The diode switches are numbered as shown.

requiring additional compensation by the reactive shunt elements and/or combiner structure. In this work, we avoid the need for a broadband bias tee by using the RF shorts of the transformer power combining network to feed in the dc supplies, as can be seen in the simplified schematic shown in Fig. 4.7.

The reconfigurable shunt reactances are implemented using 5 PIN diodes spaced approximately evenly along a 1.1 mm short-circuited transmission line. Details of the PIN diode bias structure are shown in

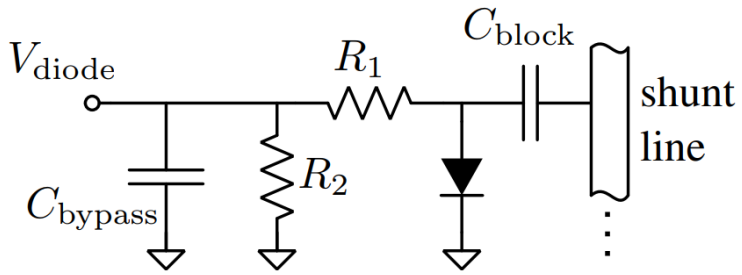


Figure 4.8: Details of the switched-reactance element bias structure.

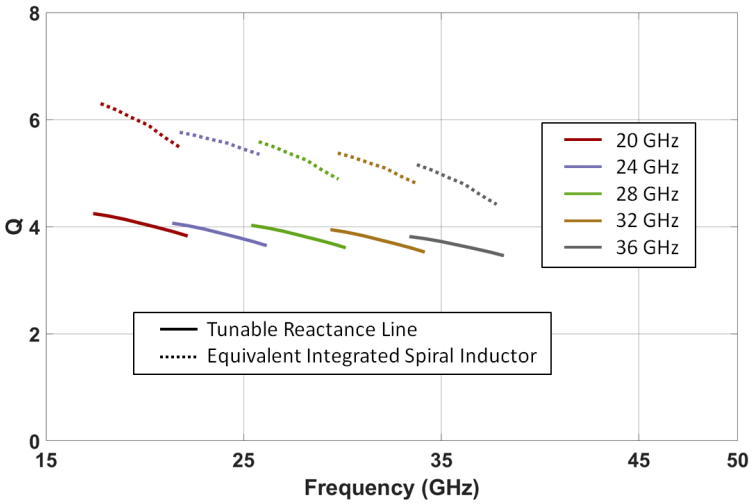


Figure 4.9: Simulated quality factor of the shunt inductive stub when the appropriate switch corresponding to each frequency range is selected (solid lines). Shown for comparison is the Q of a fixed integrated spiral inductor (2 nH) in this process having the same reactance value (dashed lines).

Fig. 4.8. A high-valued ($R_1 = 1\,\text{k}\Omega$) series resistor provides RF isolation to the dc control port. While in principle a choke inductor could also be used, this is not practical in MMIC implementation due to both size limitations and because an inductor with a self-resonant frequency above the 38 GHz upper frequency range will not provide sufficient isolation at 18 GHz. Pull-down resistors ($R_2 = 5\,\text{k}\Omega$) are included on-chip so that the diodes are normally off, for ease of testing with dc probes. The dc power consumption associated with the diode control voltages are included in all PAE measurements reported in Section 4.4.

In Fig. 4.9 we show the quality factor, Q, simulated for the inductive shunt stub (equivalent to a 2 nH inductance) and corresponding to the different switch states used in each operating frequency range [see Table 4.1]. Also shown is the simulated Q of a fixed inductor element in this process having the same reactance value. The reconfigurable line has a Q degraded by approximately 30% compared to the fixed

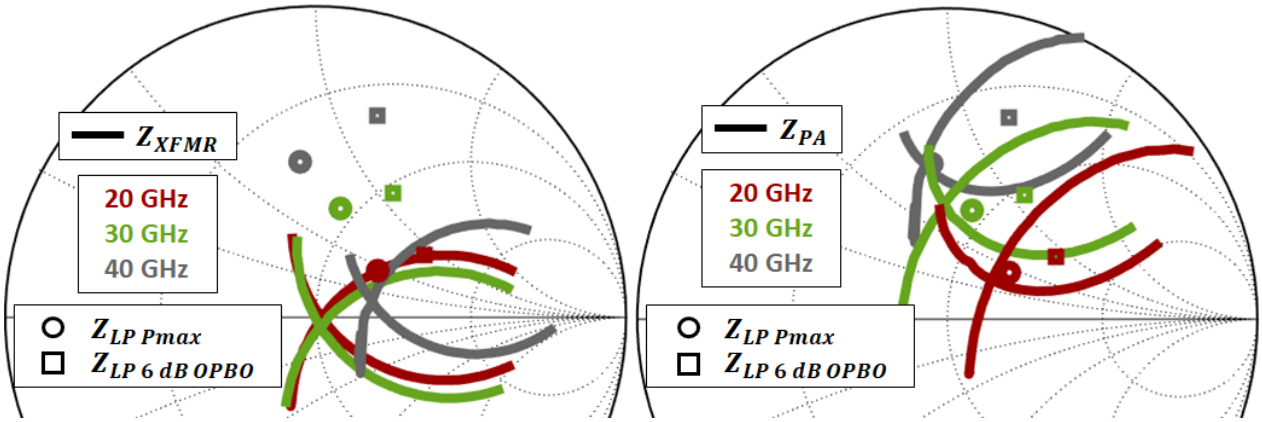
Table 4.1: Summary of switch states for operation across nominal center frequencies 20–36 GHz

Switch	20 GHz	24 GHz	28 GHz	32 GHz	36 GHz
X_C	4	3	2	2	1
X_L	4	2	2	1	1

lumped element at the lower frequency range, the difference is less towards the higher frequencies where the self-resonance of the inductor structure limits its quality factor. Similar behavior is seen in the capacitive stub relative to fixed lumped elements.

Fig. 4.10 shows the simulated target impedances corresponding to the highest-efficiency impedance at peak output power ($Z_{LP\ Pmax}$) and highest efficiency at 6-dB output back-off ($Z_{LP\ 6dBOPBO}$) for 20 GHz, 30 GHz, and 40 GHz center frequencies. These load-pull targets are simulated at the drain manifold of the output stage transistor, i.e. at Z_{PA} in Fig. 4.7. Fig. 4.10(a) shows the load trajectories at the input plane to the power combiner (Z_{XFMR} in Fig. 4.7), when simulated using ideal power sources as described in Section 4.2. Fig. 4.10(b) shows the load trajectories at the Z_{PA} plane, where a single diode in each shunt reactance stub is turned on in each frequency range, setting the operating band to compensate for the frequency-dependent target impedance rotation in the Smith chart. A summary of diode switch states corresponding to each band is given in Table 4.1, with switch numbering beginning with the switch closest to the branch PA as indicated in Fig. 4.7. In the measured system, the output power dynamic range is determined by a combination of the load trajectories seen in Fig. 4.10 and mixed-mode operation, in which the input drive power is backed off once the limit of practical output power control through load modulation is reached.

A die photograph of the 2.5 mm by 2 mm fabricated MMIC is shown in Fig. 4.11, along with an annotated layout diagram indicating the various architecture components. In addition to the outphasing PA, various test structures have been included, such as the drop-out of the power combiner structure used for the characterization in Fig. 4.5.



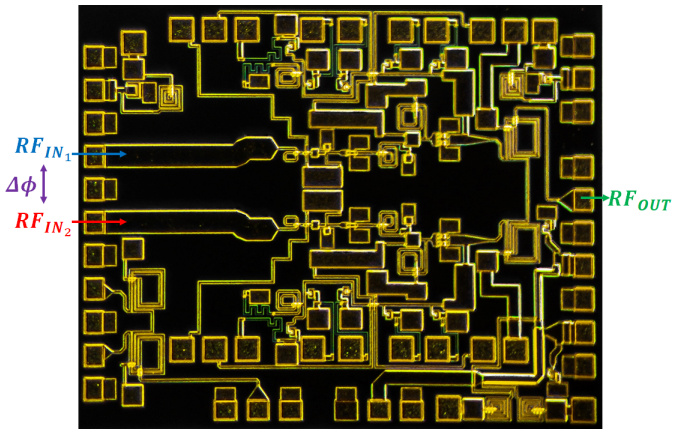
(a) (b)

Figure 4.10: Simulated target impedances for highest PAE at peak power ($Z_{LP\ Pmax}$) and 6-dB back-off ($Z_{LP\ 6dBOPBO}$) across frequency at reference plan Z_{PA} Fig. 4.7. (a) Simulated input impedances to the combiner shown at the transformer plane Z_{XFMR}. (b) Impedance trajectories at Z_{PA} after compensation by the shunt elements.

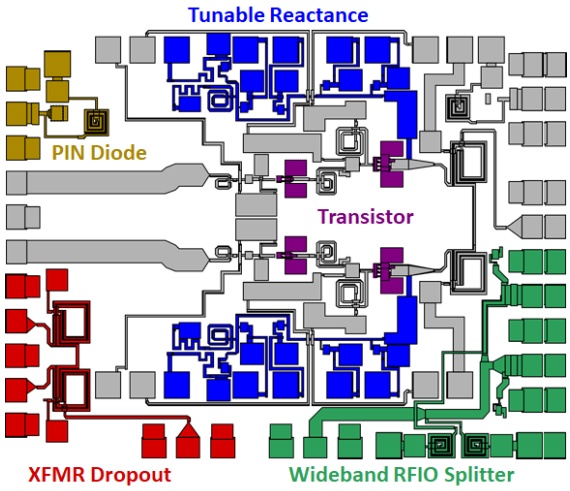
4.4 Measurements

The frequency-reconfigurable outphasing MMIC is characterized on-wafer using a Micromanipulator probe station. For CW measurements, a Rohde & Schwarz ZVA43 four-port vector network analyzer (VNA) is used to drive the input ports. Software options K4 and K6 enable coherent phase control of the internal sources, with the relative phase of the two driving ports swept to produce outphasing measurements.

The PA is first characterized at each nominal center frequency of the five bands. The switch states are selected based on the simulated behavior, i.e. using the values given in Table 4.1. Fig. 4.12 shows a complete set of CW measurements at 28 GHz, in which the outphasing angle is continuously swept and the input power is stepped, resulting in the four outphasing contours shown. This measurement is used to generate a signal separation function that determines how both the outphasing angle and drive amplitude are varied to produce a desired output power, expressed as an 8th order polynomial and plotted in Fig. 4.13. The function is chosen such that the highest-PAE performance is tracked, corresponding to the black curve in Fig. 4.12. Alternatively, other decomposition approaches could be selected, for example to optimize for gain flatness. In this work, for simplicity of operation the same signal separation function is applied at all center frequencies for CW performance measurements. The resulting PAE and gain vs. output power are



(a)



(b)

Figure 4.11: Completed design of the MMIC, with overall dimensions 2.5 mm x 2 mm. (a) Die photograph. (b) Annotated layout diagram.

presented at each band center frequency in Figs. 4.14 and 4.15.

Based on the CW measurements at each center frequency, the outphasing angles and input power levels corresponding to peak output power and 6-dB OBO in each band are identified. With these values held fixed within a given frequency range, the RF input frequency is then swept. The resulting measured peak output power, and PAE at peak and 6-dB OBO are shown in Figs. 4.16–4.18. The comparison to simulation shows excellent agreement between simulated and measured results, with the slight discrepancies attributed to variations in the realized inductive peaking. Over the 18–38 GHz range, the two-stage PA produces 20–24 dBm output power with 23%–30% PAE at peak output power and 17%-23% at 6-dB output back-off.

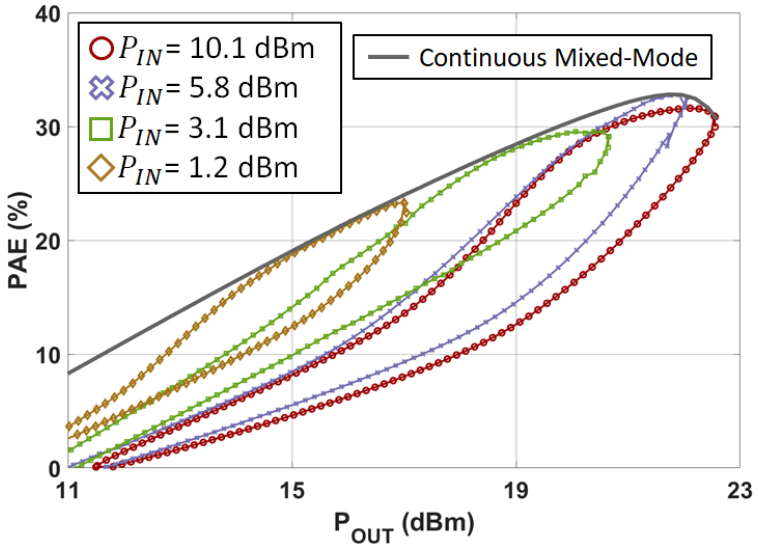


Figure 4.12: Outphasing performance curves at discrete input power levels, measured in CW at 28 GHz. The input power and phase corresponding to the highest PAE is determined, and then a function fit to determine the mixed-mode signal decomposition.

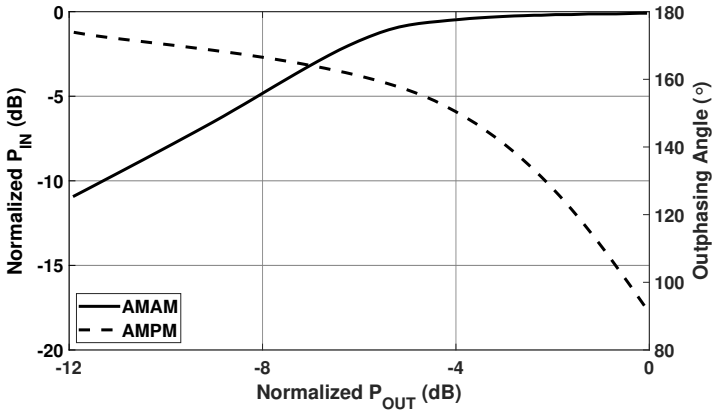


Figure 4.13: Empirically determined amplitude and phase signal separation for CW measurements, based on the measurements shown in Fig. 4.12.

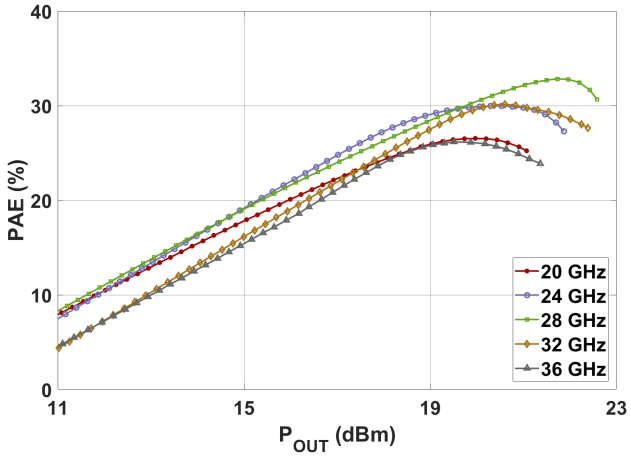


Figure 4.14: Measured PAE vs. P_{OUT} at different center frequencies (different switch state configurations denoted by different color traces). In this and subsequent measurement plots, every 2nd measurement point is indicated with a marker.

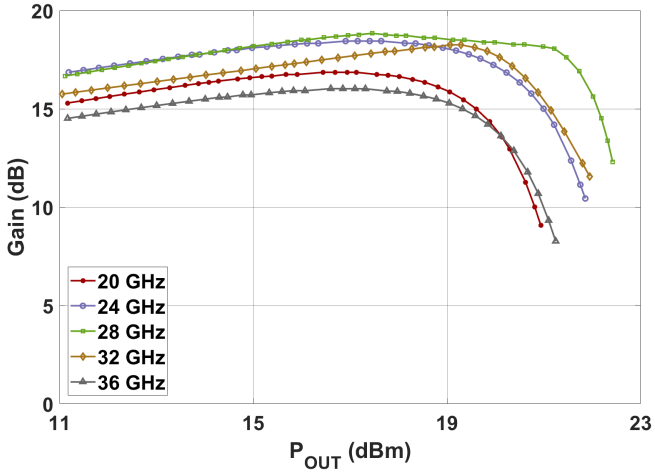


Figure 4.15: Measured gain vs. P_{OUT} at different center frequencies(different switch state configurations denoted by different color traces)

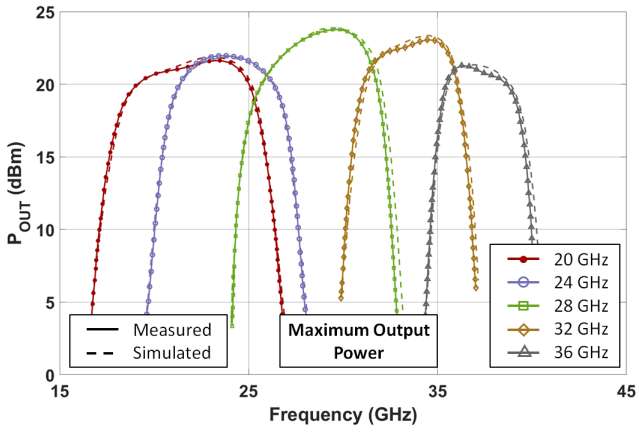


Figure 4.16: Measured peak output power, P_{MAX} (as determined from the CW center-frequency measurements in Fig. 4.14), measured across frequency for different center frequencies (different switch state configurations denoted by different color traces).

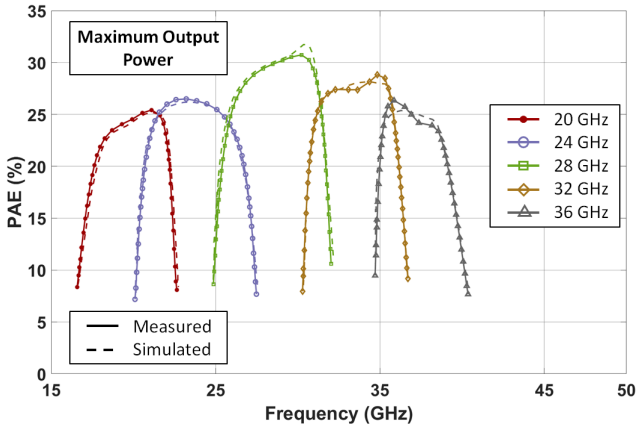


Figure 4.17: Measured (solid line) and simulated (dashed line) PAE at P_{MAX} across frequency for different center frequencies (different switch state configurations denoted by different colors).

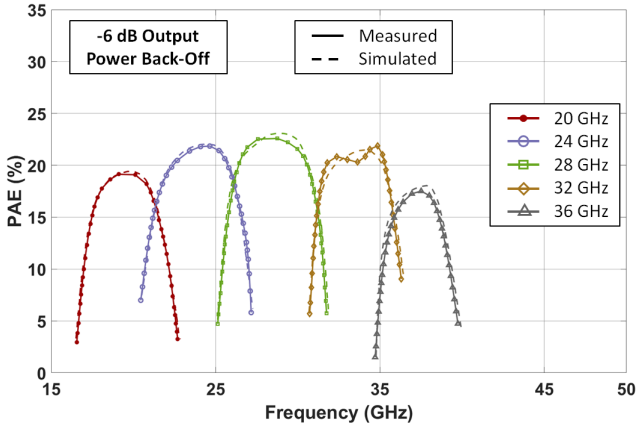


Figure 4.18: Measured (solid line) and simulated (dashed line) PAE at $P_{MAX} - 6$ dB across frequency for different center frequencies (different switch state configurations denoted by different colors).

Table 4.2: Comparison to state-of-the-art broadband, frequency reconfigurable, and efficiency enhanced K/Ka-band PAs.

Ref./Year	Architecture	Freq. (GHz)	RF Bandwidth (GHz)	Gain (dB)	$P_{\max}$ (dBm)
[59] 2017	Freq-reconfig. active load mod.	40–65	25	18.8 @ 55 GHz	23.6 @ 55 GHz
[57] 2019	Multiband Doherty	28 / 37 / 39	–	16.6–18.2	16.8–17.1
[58] 2015	24.3–35	10.7	16	11.1	
[51] 2019	Doherty	28	3	11.8	26.5
[50] 2018	Doherty	28	1.25	14.4	28.5
[52] 2018	Doherty	31.1	2.8	14	26.3
[53] 2016	Doherty	26.5	1	10.5	26.9
[56] 2019	Doherty	40	2	12.7	23.1
[75] 2018	Outphasing	28	–	–	17.1
[76] 2019	Reactive match	25–34	9	20	24
[77] 2019	Reactive match	18–24	6	25	36.5
This work	Freq-reconfig. outphasing	20 / 24 / 28 / 32 / 36	2–6 / band	16–18.5	20–24

† — read from graph. * — includes test structures on chip.

Based on the comparison to other broadband, frequency-reconfigurable, and efficiency enhanced (Doherty) PAs in this frequency range given in Table 4.3, this PA performs with efficiency comparable to that of single-frequency designs but over a 71% effective fractional RF bandwidth.

4.4.1 Modulated Measurements

The frequency-reconfigurable outphasing MMIC is characterized with modulated input signals using the experimental test bench shown in Fig. 4.19. Two Rohde & Schwarz SMW200A signal generators are connected to provide modulated, coherent input signals, while the output is captured using a Rohde & Schwarz FSW43. Time-alignment between the two paths is verified using an oscilloscope. The outphasing signal decomposition is performed offline in Matlab. Due to the 20-GHz carrier frequency limitation of the sources, the PA is characterized in the lowest band only. The nonlinear signal decomposition function generating the outphasing signals results in approximately 10× bandwidth expansion [20]. Therefore, despite the 2-GHz instantaneous bandwidth capability of the SMW200A, modulated measurements are limited to

Table 4.3: Comparison to state-of-the-art broadband, frequency reconfigurable, and efficiency enhanced K/Ka-band PAs.

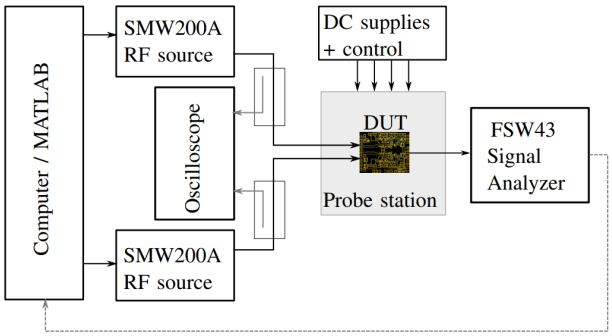
Ref./Year	Technology	Architecture	PAE @ $P_{\max}$ (%)	PAE @ 6 dB OBO (%)	Size (mm^2)
[59] 2017	180 nm SiGe	Freq-reconfig. active load mod.	27.7 @ 55 GHz	17† @ 55 GHz	1.02
[57] 2019	130 nm SiGe	Multiband Doherty	19.5–21.4	12.6–16.6	1.76
[58] 2015	180 nm SiGe	Tunable OMN	55.9	24†	0.72
[51] 2019	150 nm GaAs	Doherty	42	31	2.86
[50] 2018	150 nm GaAs	Doherty	37	27	4.93
[52] 2018	150 nm GaAs	Doherty	35	28 @ 7 dB	3.57
[53] 2016	150 nm GaAs	Doherty	42	32	25
[56] 2019	100 nm GaAs	Doherty	28.5	21.1	2.25
[75] 2018	45-nm CMOS	Outphasing	η_D =56	η_D =38	–
[76] 2019	150 nm GaAs	Reactive match	35	9†	2.8
[77] 2019	150 nm GaN-on-SiC	Reactive match	40	12–22†	8
This work	100 nm GaAs	Freq-reconfig.	23–31	17.5–22.5	5*

† — read from graph. * — includes test structures on chip.

200-MHz instantaneous bandwidth.

The measured output spectrums for 100-MHz and 200-MHz instantaneous bandwidth LTE signals with 7.3 dB PAPR each are shown in Fig. 4.20. A mixed-mode outphasing signal decomposition based on the empirically obtained CW decomposition data in Fig. 4.13 is used. The modulated performance demonstrates 15.4% average efficiency and 24.18 dBc ACLR at an average output power of 14.3 dBm for the 100-MHz signal, and 15.3% average efficiency and 25.22 dBc ACLR at an average output power of 14.3 dBm for the 200-MHz signal.

While no linearization outside of the basic offline signal separation is performed here, other groups have demonstrated the linearizability of dual-input outphasing systems [78–81], including linearization of a 200-MHz instantaneous bandwidth 64-QAM signal with 12.2 dB PAPR to a worst-case ACLR of -40 dBc [82].



(a)

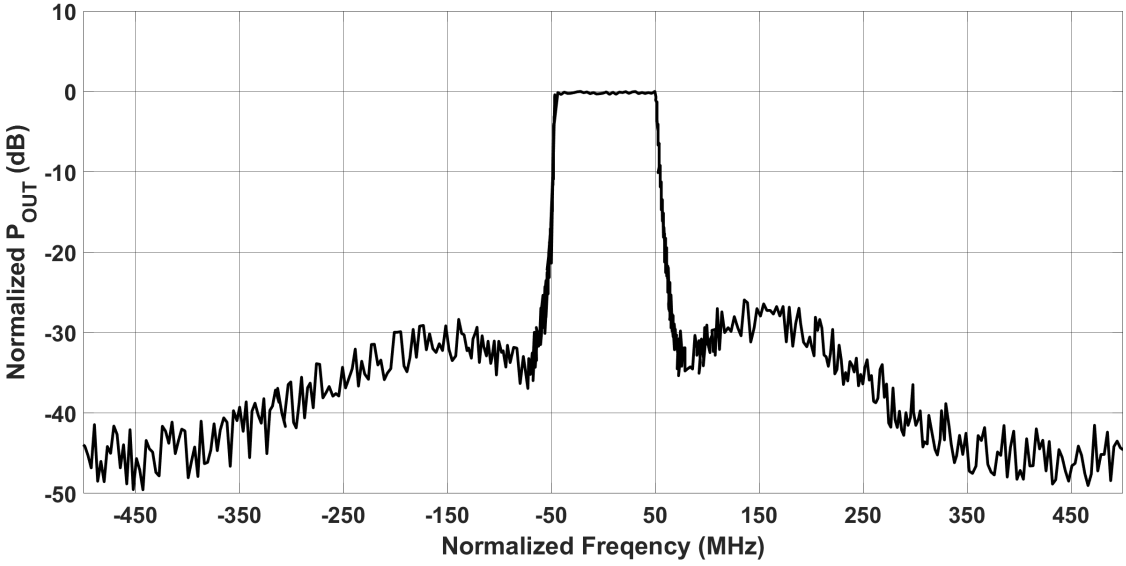
(b)

Figure 4.19: Experimental testbench used to characterize the frequency-reconfigurable outphasing MMIC for modulated signals. (a) Block diagram of the setup. (b) Photograph (probe station, located at front right, not shown).

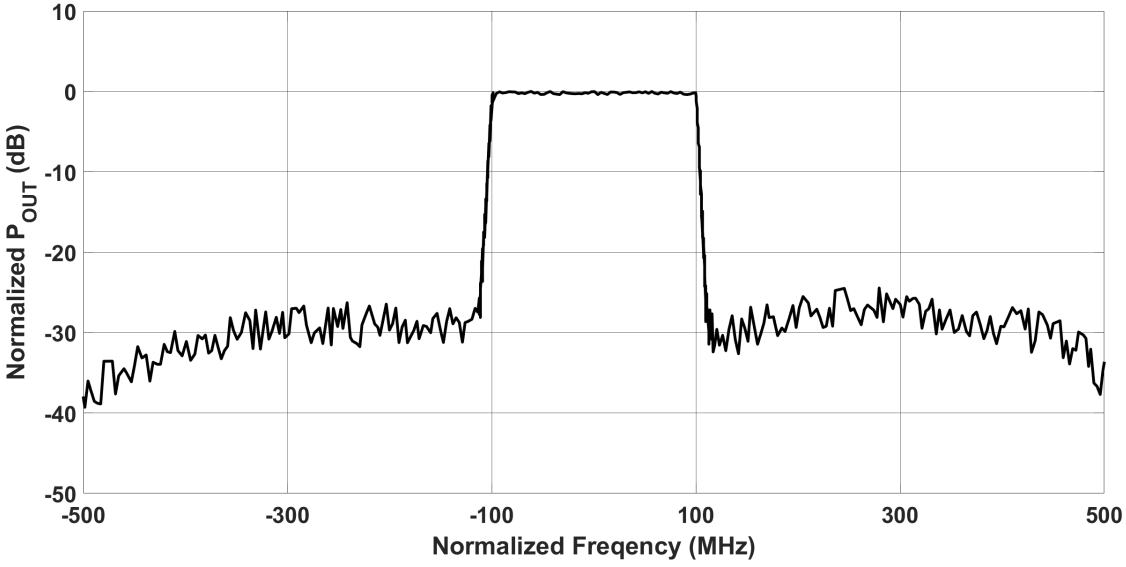
4.5 Conclusion

This design presents for the first time a frequency-reconfigurable outphasing PA, operating over K/Ka-band with a total 71% effective fractional bandwidth and $\geq$ 2 GHz bandwidth in each of the five frequency configurations. The design exploits the MMIC implementation options possible at this frequency range, using a wideband power combining structure, with shunt stubs to set the reconfigurable Chireix compensating reactances. The combining structure additionally performs the function of a bias tee, avoiding the potentially bandwidth-limiting dispersion of a conventional biasing structure.

With its 20–24 dBm peak power and 23–31% peak PAE across 18–38 GHz, efficiency enhancement at 6-dB OBO, and demonstrated performance with 100-MHz and 200-MHz instantaneous bandwidth modulated signals, the presented design demonstrates state-of-the-art performance for a GaAs PA operating in this



(a)



(b)

Figure 4.20: Modulated performance of the PA using mixed-mode signal decomposition centered at 19.5 GHz. (a) Measured 100-MHz LTE signal with 7.3 dB PAPR, average output power 14.3 dBm, average efficiency 15.4%, and ACLR 25.22 dBc. (b) Measured 200-MHz LTE signal with 7.3 dB PAPR, average output power 14.3 dBm, average efficiency 15.3%, and ACLR 24.18 dBc.

frequency range. The performance of this technique is limited by the narrowband performance of the interstage and input matching networks. Adding reconfigurability to the interstage and input matching networks will boost overall performance.

Chapter 5

Summary and Future Work

5.1 Summary

This thesis covered two distinct topologies: X-band RFIO PA utilizing novel non-linear elements for inphasing splitting network and a DIRO PA showing novel reconfigurable outphasing performance in III-V technologies at Ku/K/Ka bands. Both topologies solved pertinent issues with the outphasing PA architecture as it pertains to current needs in modern communication and telemetry systems.

The X-band RFIO PA MMICs proved the scalability of the RFIO architecture. It showed that there is an optimal design space for both linearity and efficiency for an RFIO PA. Through the use of discrete non-linear elements, different efficiency and linearity characteristics were shown in conjunction with a dual input outphasing MMIC designed for an RFIO architecture. The mesa resistor showed to be the best overall with high linearity performance and good efficiency performance while the PIN diode showed the highest efficiency performance while suffering from strong non-linearities as well as large memory effects. This is a similar result that was shown in the previous X-band implementation utilizing PIN diodes as the non-linear elements. In addition, the full RFIO PA was integrated into a single MMIC in Qorvo's 150 nm GaN process utilizing in process diode-connected transistors. The RFIO MMIC works as expected while implementing bias control over the non-linear elements allowing for a finer tuning adjustability of the non-

linear characteristics that determine the linearity and efficiency performance of the RFIO PA. Controlling the bias of the diode-connected transistors showed to improve the efficiency of the RFIO PA in deep back-off upwards of 10 points of PAE.

The K-band DIRO PA showed the first K-band outphasing MMIC in III-V technology that proved reconfigurable operation. The MMIC is able to obtain high average efficiency numbers over large instantaneous bandwidths operating across over an octave worth of bands given different switch state configurations. The PA utilizes a novel power combining structure in conjunction with a novel switchable shunt reactance setup to simultaneously match the output transistor and load the outphasing power combiner with the correct reactive compensation. This technique can be expanded to cover different band configurations as well as be optimized for different forms of operation in different bands.

5.2 Future Work

Continuing with the work done on the integrated RFIO MMIC with bias controlled non-linear elements. Measurements can be done on the MMIC to determine the benefit of asymmetric biasing across the two branches. In addition, measurements can be taken while dynamically controlling the bias of the non-linear elements tracking the signal envelope. This will be easier to implement than traditional supply modulators give the sub-1 V biasing voltage the diodes require.

Continuing with the DIRO, work can be done on optimizing the outphasing drive signal at the different bands to even further expand the operating band performance given different switch states. This works off of the Doherty-outphasing continuum utilizing arbitrary signal drive but could significantly improve performance. Wide-band RFIO signal generation could also be paired with the DIRO. A wide-band inphasing splitter network is taped-out on the DIRO MMIC and can be measured.

Bibliography

[1] B. Manz, "Rf power amplifier efficiency: Big challenges for designers," https://www.mouser.com/publicrelations_techarticle_rf_power_amp_efficiency_2015final/, accessed: 2020-03-20. x, 4, 5

[2] T. Cappello, T. W. Barton, C. Florian, M. Litchfield, and Z. Popovic, "Multilevel supply-modulated Chireix outphasing with continuous input modulation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5231–5243, Dec 2017. xii, 20, 22

[3] R. Quaglia, D. J. Shepphard, and S. Cripps, "A reappraisal of optimum output matching conditions in microwave power transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 3, pp. 838–845, March 2017. xiii, 27, 28, 29

[4] D. N. Martin, "X-band gan mmic inverse-f pa optimized for load modulation," Ph.D. dissertation, 2016, copyright - Database copyright ProQuest LLC; ProQuest does not claim copyright in the individual underlying works; Last updated - 2020-11-09. [Online]. Available: https://colorado.idm.oclc.org/login?url=https://www-proquest-com.colorado.idm.oclc.org/docview/1973329346?accountid=14503 xix, 101, 102

[5] P. E. de Falco, J. Birchall, and L. Smith, "Hitting the sweet spot: A single-ended power amplifier exploiting class ab sweet spots and optimized third harmonic termination," *IEEE Microwave Magazine*, vol. 18, no. 1, pp. 63–70, 2017. 1

[6] S. C. Cripps, *RF Power Amplifiers for Wireless Communications, 2nd ed.* Norwood, MA: Artech House, 2006. 4, 6

[7] P. Enrico De Falco, K. Mimis, S. B. Smida, K. Morris, G. Watkins, A. Yamaoka, and K. Yamaguchi, "Single-ended branch pa characterisation for outphasing amplifiers," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, 2018, pp. 178–181. 6

[8] P. E. de Falco, G. Watkins, K. Mimis, S. Bensmida, and K. Morris, "Analysis of optimal outphasing load trajectories for gan pas," in *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 58–60. 7

[9] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for rf and microwave," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814–826, 2002. 7

[10] D. Fishler, T. Cappello, W. Hallberg, T. W. Barton, and Z. Popovic, "Supply modulation of a linear doherty power amplifier," in *2018 48th European Microwave Conference (EuMC)*, 2018, pp. 519–522. 7

[11] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of a doherty-like rf-input load modulated balanced amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5322–5335, 2018. 7

[12] P. E. de Falco, P. Pednekar, K. Mimis, S. B. Smida, G. Watkins, K. Morris, and T. W. Barton, "Load modulation of harmonically tuned amplifiers and application to outphasing systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 10, pp. 3596–3612, 2017. 7

[13] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935. 7

[14] T. W. Barton and D. J. Perreault, "Theory and implementation of RF-input outphasing power amplification," *IEEE T-MTT*, vol. 63, no. 12, pp. 4273–4283, Dec 2015. 14, 18

[15] N. Faraji and T. W. Barton, "An RF-input Chireix outphasing power amplifier," in *IEEE PAWR*, Jan 2016, pp. 11–14. 15

[16] M. Litchfield and Z. Popovic, "Multi-level Chireix outphasing GaN MMIC PA," in *IEEE CSICS*, Oct 2015, pp. 1–4. 16, 17

[17] T. W. Barton and D. J. Perreault, "Theory and implementation of RF-input outphasing power amplification," vol. 63, no. 12, pp. 4273–4283, Dec 2015. 25, 32, 33, 35, 37, 40

[18] D. J. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1713–1726, 2011. 25

[19] J. H. Qureshi, M. J. Pelk, M. Marchetti, W. C. E. Neo, J. R. Gajadharsing, M. P. van der Heijden, and L. C. N. de Vreede, "A 90-w peak power gan outphasing amplifier with optimum input signal conditioning," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 1925–1935, Aug 2009. 25, 62, 65

[20] T. Barton, "Not just a phase: Outphasing power amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 18–31, Feb 2016. 25, 52, 53, 62, 64, 65, 79

[21] A. Grebennikov, Ed., *Radio Frequency and Microwave Power Amplifiers. Volume 2: Efficiency and Linearity Enhancement Techniques*, ser. Materials, Circuits amp; Devices. Institution of Engineering and Technology, 2019. [Online]. Available: https://digital-library.theiet.org/content/books/cs/pbcs071g 25, 39

[22] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-way lossless outphasing system based on an all-transmission-line combiner," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1313–1326, April 2016. 30, 65

[23] N. Faraji and T. W. Barton, "An rf-input chireix outphasing power amplifier," in *2016 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, Jan 2016, pp. 11–14. 32, 40

[24] H. Q. Nguyen and T. W. Barton, "Linearity characterization of RF-input Chireix outphasing power amplifier," in *2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS)*, Aug 2017, pp. 1–4. 32, 40

[25] D. N. Martin, T. Cappello, M. Litchfield, and T. W. Barton, "An x-band rf-input outphasing power amplifier," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, June 2018, pp. 308–311. 32, 33, 40, 46, 62, 63, 65

[26] S. Schafer and M. Roberg, "Monolithic attenuator/limiter using nonlinear resistors," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Oct 2018, pp. 152–155. 37

[27] H. Jang, R. Wilson, T. Canning, D. Seebacher, C. Schuberth, B. Arigong, F. Trang, and S. Ward, "Rf-input self-outphasing doherty–chireix combined amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4518–4534, Dec 2016. 39, 40

[28] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE T-MTT*, vol. 59, no. 9, pp. 2295–2305, Sept 2011. 46

[29] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A wideband and compact gan mmic doherty amplifier for microwave link applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 2, pp. 922–930, 2013. 46, 47

[30] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A gan mmic modified doherty pa with large bandwidth and reconfigurable efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3006–3016, 2014. 46, 47

[31] H. Yao, T. Yuan, G. Liu, X. Ning, Z. Jin, and X. Liu, "X-band 11.7-w, 29-db gain, 42% pae three-stage phemt mmic power amplifier," in *2015 Asia-Pacific Microwave Conference (APMC)*, vol. 3, 2015, pp. 1–3. 46

[32] Q. Wu, B. Song, Y. Shih, X. Huang, and J. Wu, "A full x-band high-efficiency 12-watt gaas mmic power amplifier with harmonic tuning," in *2015 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, 2015, pp. 1–3. 46

[33] M. Meghdadi and A. Medi, "Design of 6–18-ghz high-power amplifier in gaas phemt technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 7, pp. 2353–2360, 2017. 46

[34] R. Giofré and P. Colantonio, "A high efficiency and low distortion 6 W GaN MMIC Doherty amplifier for 7 GHz radio links," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 70–72, 2017. 46, 47

[35] M. Darwish and A. Pham, "Compact and high efficiency doherty power amplifier using a new modulation load range," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017, pp. 782–784. 46, 47

[36] J. R. Powell, D. J. Shepphard, R. Quaglia, and S. C. Cripps, "A power reconfigurable high-efficiency *x* -band power amplifier mmic using the load modulated balanced amplifier technique," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 6, pp. 527–529, 2018. 46

[37] S. Li, S. S. H. Hsu, J. Zhang, and K. Huang, "Design of a compact gan mmic doherty power amplifier and system level analysis with x-parameters for 5g communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5676–5684, 2018. 46, 47

[38] G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of gan mmic doherty power amplifiers using broadband transformer-based load modulation network," *IEEE Access*, vol. 7, pp. 119 844–119 855, 2019. 46, 47

[39] M. R. Duffy, G. Lasser, T. Cappello, and Z. Popović, "Efficiency and linearity enhancement of a two-stage X-band PA through simultaneous gate and drain supply modulation," *IET Microwaves, Antennas Propagation*, vol. 14, no. 12, pp. 1347–1354, 2020. 46, 47

[40] N. Kuo, B. Yang, A. Wang, L. Kong, C. Wu, V. P. Srini, E. Alon, B. Nikolić, and A. M. Niknejad, "A wideband all-digital CMOS RF transmitter on HDI interposers with high power and efficiency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4724–4743, Nov 2017. 52

[41] A. Piacibello, R. Quaglia, M. Pirolaf, and S. Cripps, "Design of an S-band Chireix outphasing power amplifier based on a systematic bandwidth limitation analysis," in *European Microw. Integ. Circuits Conf.*, Sep. 2018, pp. 186–189. 52, 65

[42] C. F. Campbell, M. D. Roberg, J. Fain, and S. Nayak, "A 1–8 GHz gallium nitride distributed power amplifier MMIC utilizing a trifilar transformer," in *European Microw. Integr. Circuits Conf.*, Oct 2016, pp. 217–220. 53, 66

[43] P. Pednekar, L. Deng, and T. Barton, "Experimental characterization and control of a four-way non-isolating power combiner," in *2016 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, Jan 2016, pp. 8–10. 57

[44] S. Shambayati, "Ka-band telemetry operations concept: A statistical approach," *Proc. IEEE*, vol. 95, no. 11, pp. 2171–2179, Nov 2007. 61

[45] S. Maleki, S. Chatzinotas, B. Evans, K. Liolis, J. Grotz, A. Vanelli-Coralli, and N. Chuberre, "Cognitive spectrum utilization in Ka band multibeam satellite communications," *IEEE Commun. Mag.*, vol. 53, no. 3, pp. 24–29, March 2015. 61

[46] "Telemetry group, range commanders council, "Document 106-15" (June 2015)," [Online] http://www.irig106.org/docs/106-15/. 61

[47] W. Jang, R. Cordeiro, A. Oliveira, and N. B. Carvalho, "A broadband almost-digital RF transmitter with an efficient power amplifier," vol. 64, no. 5, pp. 1526–1534, May 2016. 61

[48] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters," vol. 59, no. 5, pp. 1284–1293, May 2011. 61

[49] Y. Chen, T. Wang, S. Lin, J. Chen, and Y. E. Chen, "A pulse-modulated polar transmitter using direct digital synthesis for 5G NR mobile applications," pp. 1–1, 2019. 61

[50] D. P. Nguyen, T. Pham, and A. Pham, "A 28-GHz symmetrical Doherty power amplifier using stacked-FET cells," vol. 66, no. 6, pp. 2628–2637, June 2018. 62, 79, 80

[51] D. P. Nguyen, B. L. Pham, and A. Pham, "A compact Ka-band integrated Doherty amplifier with reconfigurable input network," vol. 67, no. 1, pp. 205–215, Jan 2019. 62, 79, 80

[52] G. Lv, W. Chen, and Z. Feng, "A compact and broadband Ka-band asymmetrical GaAs Doherty power amplifier MMIC for 5G communications," June 2018, pp. 808–811. 62, 79, 80

[53] J. Curtis, A. Pham, and F. Aryanfar, "Ka-band Doherty power amplifier with 26.9 dBm output power, 42% peak PAE and 32% back-off PAE using GaAs PHEMTS," *IET Microw. Antennas Propag.*, vol. 10, no. 10, pp. 1101–1105, 2016. 62, 79, 80

[54] R. Quaglia, V. Camarchia, T. Jiang, M. Pirola, S. Donati Guerrieri, and B. Loran, "K-band GaAs MMIC Doherty power amplifier for microwave radio with optimized driver," vol. 62, no. 11, pp. 2518–2525, Nov 2014. 62

[55] Y. Lin, J. Ji, T. Chien, H. Chang, and Y. Wang, "A Ka-band 25-dBm output power high efficiency monolithic Doherty power amplifier in 0.15-μm GaAs E-mode pHEMT process," in *IEEE Asia Pacific Microw. Conf.*, Nov 2017, pp. 984–987. 62

[56] Y. Chen, C. Chen, C. Chiong, and H. Wang, "A compact 40-GHz Doherty power amplifier with 21% PAE at 6-dB power back off in 0.1-μ m GaAs pHEMT process," vol. 29, no. 8, pp. 545–547, Aug 2019. 62, 79, 80

[57] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," vol. 54, no. 6, pp. 1586–1599, June 2019. 62, 79, 80

[58] K. Ma, T. B. Kumar, and K. S. Yeo, "A reconfigurable K-/Ka-band power amplifier with high PAE in 0.18-μm SiGe BiCMOS for multi-band applications," vol. 63, no. 12, pp. 4395–4405, Dec 2015. 62, 79, 80

[59] C. R. Chappidi and K. Sengupta, "Frequency reconfigurable mm-wave power amplifier with active impedance synthesis in an asymmetrical non-isolated combiner: Analysis and design," vol. 52, no. 8, pp. 1990–2008, Aug 2017. 62, 79, 80

[60] C. Liang, P. Roblin, Y. Hahn, Z. Popovic, and H. Chang, "Novel outphasing power amplifiers designed with an analytic generalized Doherty–Chireix continuum theory," vol. 66, no. 8, pp. 2935–2948, Aug 2019. 62, 65

[61] C. M. Andersson, D. Gustafsson, J. Chani Cahuana, R. Hellberg, and C. Fager, "A 1–3-GHz digitally controlled dual-RF input power-amplifier design based on a Doherty-outphasing continuum analysis," vol. 61, no. 10, pp. 3743–3752, Oct 2013. 62, 65

[62] M. Litchfield and Z. Popović, "X-band outphasing GaN MMIC PA with power recycling," May 2015, pp. 1–4. 62, 63

[63] C. Xie, D. Cripe, J. Reyland, D. Landt, and A. Walker, "Development of high-efficiency X-band outphasing transmitter," in *IEEE CSICS*, Oct 2014, pp. 1–4. 62, 63, 65

[64] E. Aggrawal and K. Rawat, "Reconfigurable Chireix outphasing power amplifier over multiple frequency bands," pp. 1–1, 2019. 62, 63, 65

[65] H. Chireix, "High power outphasing modulation," *Proceedings of the IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935. 62, 66

[66] S. Li, T. Chi, J. Park, H. T. Nguyen, and H. Wang, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," vol. 54, no. 5, pp. 1243–1253, May 2019. 63

[67] D. Martin, M. Roberg, Z. Popovic, and T. W. Barton, "A 6–12 GHz reconfigurable transformer-based outphasing combiner in 250-nm GaAs," in *IEEE BiCMOS Compound Semicon. Integr. Circuits Tech. Symp.*, November 2019. 63

[68] A. Bogusz, J. Lees, R. Quaglia, G. Watkins, and S. C. Cripps, "A waveform-engineered outphasing RFPA using a broadband balun combiner," June 2018, pp. 301–303. 65

[69] M. El-Asmar, A. Birafane, A. B. Kouki, and A. El-Rafhi, "Optimal combiner design for outphasing RF amplification systems," in *Intl Conf. Advances in Computational Tools for Eng. Appl.*, Dec 2012, pp. 176–181. 65

[70] M. Özen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, "A generalized combiner synthesis technique for class-E outphasing transmitters," vol. 64, no. 5, pp. 1126–1139, May 2017. 65

[71] J. M. Schellenberg, "A broadband, push-pull power MMIC operating at K/Ka-band frequencies," vol. 2, June 2002, pp. 909–912 vol.2. 66

[72] S. Chakraborty, L. E. Milner, A. Parker, and M. Heimlich, "A folded edge-coupled transformer balun in GaAs with excellent balance from 9 to 20 GHz," in *European Microw. Conf.*, Sep. 2018, pp. 1101–1104. 66

[73] D. Danzillio, "Advanced GaAs integration for single chip mmWave front-ends," *Microw. Journal*, May 2018 [Online, accessed March 2020]. 69

[74] H. Jang, R. Wilson, T. Canning, D. Seebacher, C. Schuberth, and B. Arigong, "Self-outphasing Chireix power amplifier using device input impedance variation," May 2016, pp. 1–4. 70

[75] S. Li, T. Chi, H. T. Nguyen, T. Huang, and H. Wang, "A 28GHz packaged Chireix transmitter with direct on-antenna outphasing load modulation achieving 56%/38% PA efficiency at peak/6dB back-off output power," in *IEEE Radio Freq. Integ. Circuits Symp.*, June 2018, pp. 68–71. 79, 80

[76] D. P. Nguyen, X. Tran, N. L. K. Nguyen, P. T. Nguyen, and A. Pham, "A wideband high efficiency Ka-band MMIC power amplifier for 5G wireless communications," in *IEEE Intl. Symp. Circuits Syst.*, May 2019, pp. 1–5. 79, 80

[77] M. R. Duffy, G. Lasser, G. Nevett, M. Roberg, and Z. Popović, "A three-stage 18.5–24-GHz GaN-on-SiC 4 W 40% efficient MMIC PA," vol. 54, no. 9, pp. 2402–2410, Sep. 2019. 79, 80

[78] A. Birafane and A. B. Kouki, "Phase-only predistortion for LINC amplifiers with Chireix-outphasing combiners," vol. 53, no. 6, pp. 2240–2250, June 2005. 80

[79] T. Hwang, K. Azadet, R. S. Wilson, and J. Lin, "Nonlinearity modeling of a Chireix outphasing power amplifier," vol. 62, no. 12, pp. 2898–2907, Dec 2015. 80

[80] ——, "Linearization and imbalance correction techniques for broadband outphasing power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 7, pp. 2185–2198, 2015. 80

[81] P. Afanasyev, P. Ramabadran, S. Mohammady, R. Farrell, and J. Dooley, "Phase-only digital predistortion technique for class-E outphasing power amplifiers," in *European Microw. Conf. Central Europe*, May 2019, pp. 14–17. 80

[82] P. Gilabert, D. Vegas, Z. Ren, G. Montoro, J. Perez-Cisneros, M. Nieves Ruiz, X. Si, and J. Garcia, "Design and digital predistortion linearization of a wideband outphasing amplifier supporting 200 MHz bandwidth," 2020, pp. 46–49. 80

Appendix A

MMIC Process Technology

There are many different competing RF and microwave process technologies. Each foundry has its own advantages from active/passive performance, PDK (process design kit)/model accuracy, and foundry turn around time. Each of these need to weighed appropriately when deciding the best fit foundry for a specific task. In this appendix, three specific foundry experiences will be discussed covering 5 different PDKs. This section is a combination of quantitative and qualitative experiences learned utilizing each of the different processes as well as personal thoughts and experiences.

A.1 Wolfspeed (Cree)

Wolfspeed is the RF and microwave device foundry for the legacy Cree company. It was spun off as a separate company around 2015. Cree is well known for its power electronic and lighting III-V devices. Wolfspeed has long been a strong competitor in the C-band and S-band discrete discrete RF transistor arena. Their MMIC process was heavily limited for high frequency performance due to the lack of backside etching making it unable to obtain a 2-mil substrate thickness as well as limited device size to a 250 nm feature size. Recently Wolfspeed has released a 150 nm feature size GaN process which includes back-side etching for 2-mil substrate thickness. The process performance on paper seems to heavily rival Qorvo and would definitely be worth giving it shot if the chance arises for an X-band or higher PA.

A.1.1 250 nm GaN

Wolfspeed's 250 nm GaN process is a legacy process that has been around for a while. The PDK has all the required fundamentals for the design but doesn't specifically stand out in any area. There are significant device convergence issues present in the PDK specifically in the MWO (AWR) implementation. Improved device convergence in observed in the legacy Keysight ADS software (pre v.11). Due to limitations of the device feature size as well as substrate thickness performance severely degrades past X-band operating region. Below X-band, however, the transistors perform well without any irregularities as do the integrated passives.

A.2 Qorvo

Qorvo is one of the biggest commercial GaN foundries. Its keystone processes include 250 nm GaN HV (High Voltage Breakdown) as well as the 150 nm GaN es. I personally have never used the 250 nm GaN HV process but did get extensive experience on the 150 nm GaN es process which will be discussed. Qorvo has significant experience in the MMIC and especially in the GaN arena and it shows in there PDKs as well as their overall MMIC performance. However, due to being a lone player in many of their arenas they often have slow external fabrication turn around times and delays from original delivery dates can be expected. This should all be taken into consideration when deciding to move forward with a Qorvo tape-out in terms of time frame.

A.2.1 250 nm GaAs

The Qorvo 250 nm GaAs process is an older process. It is a very heavily used and well understood process technology. As such, the transistor models are very accurate as is typical with GaAs processes. The larger feature size of the process limits the higher frequency range of the process but it still performs well up to lower K-band frequencies. In addition, the process has in-process switch FET models for the enhancement and depletion mode switches. This not only drastically increases ease of design for certain RF circuitry but also adds in the possibility of adding in some on chip digital circuitry.

A.2.2 150 nm GaN es

The Qorvo 150 nm GaN es process is one of Qorvo's premiere processes. It comes in both 4-mil and 2-mil substrate thicknesses with a variety of environmental protections. Qorvo's transistors perform well with a reasonable amount of process variation. However, there isn't anything spectacular about the the transistor performance as the trade-off was made for higher yields than most other boutique GaN foundries. Much of the strength of Qorvo MMICs comes in the form of their passive components. It is very easy to design unique structures and circuits that all peform very well. Specifically their CT7 capacitor is a very high performing integrated microwave capacitor with very low leakage current. In addition, their PDK is very streamlined and transistor convergence is faster than any other PDK I have used during my Ph.D. This makes a big difference for quality of life when designing MMICs in the process. Qorvo's PDK is available and functions well in both ADS and MWO, however, it operates smoother in the MWO environment at that was my preferred software for utilizing Qorvo PDKs. This comes with the added benefit of improved support from Qorvo as Qorvo designers typically utilize MWO. Overall, Qorvo's 150 nm GaN es process is my preferred GaN process to design in due to a combination of good circuit performance, consistent PDK performance, and overall usability.

A.3 WIN Semiconductor

WIN Semiconductor is one of the biggest names in the international GaAs foundry business. They produce more GaAs than anyone else in the world. This means that there GaAs offerings are all thoroughly vetted and their turn around times are faster than any other foundry that I was able work with even including the delays. One specific difference with WIN over the other companies mentioned is that WIN Semiconductor doesn't do any designs internally like Qorvo or Wolfspeed. They are purely a fabrication house. This means that sometimes support is a little more difficult to obtain when coupled with a language barrier. However, support will not likely be needed when utilizing their GaAs processes as they are accurate and thoroughly designed.

A.3.1 PIH-110 GaAs

This GaAs process is a widely utilized process. It is the 2-MI with the option to extend to 3 or 4-MI process. There are in-process PIN diodes that perform exceptionally well for switches. They outperform the transistor equivalents on both conduction losses and isolation with the added bonus of no DC current draw that transistor based switches incur. The PDK functions well with a few convergence issues on the FET models when pushed into non-standard operating modes such as deep saturation and class-B bias operations. When simulating with ideal components adding in some loss will assist in faster non-linear harmonic balance simulation times. In addition, a process that greatly improves 2.5 D EM simulation in the Qorvo PDKs through layout simplification of the via structures is absent in the WIN PDKs. This causes exponentially increased simulation time for each additional via. Therefore, manually reshaping the vias for EM simulations during the design phase can save a significant amount of time. Overall, the accuracy of the PDK to measurements for this process is astounding and is my recommended process for GaAs all the way up to upper Ka-band.

A.3.2 Pre-Production 150 nm GaN

WIN semiconductor is mostly known for their GaAs technology, however, they are currently developing a 150 nm GaN process similar to the Qorvo and Wolfspeed offering. At the moment, the process is in pre-production alpha and beta testing. However, their transistors are very well flushed out and all of the standard passives are available. At the moment, not much information is known about what the official offerings will be for substrate thickness and metal layer offerings. The transistor models are still very rough with a large number of convergence issues but there is significant work going into smoothing out the model performance for the GaN transistors using physical based transistor modeling techniques. Currently, Qorvo is definitely still the favorite for 150 nm GaN technology. However, with WIN Semiconductor ramping they may soon become a cheaper and faster alternative. They do have a little ways to go to match Qorvo's passive performance.

A.4 Conclusion

Overall, there is a number of considerations that go into the selection of a process technology. Typically the desired implementation of a circuit and the tools available in the process to do so is the main driving factor in the decision, however, ease of use and accuracy of a PDK is another thing to consider as well as wafer turn around. Overall, there are many options out there and they are continually growing. One key thing is to never take PDK models for granted and knowledge of bad model is ultimately more powerful than utilizing a good model with no understanding of how it was validating and how it is functioning.

Appendix B

MMIC Information

Below is a description of operation for all MMICs designed during this Ph.D.

B.1 X-Band Inverse Class-F PA

This PA was designed in the Wolfspeed 250 nm GaN process and was optimized for operation in a load modulation (outphasing specifically) setup. It is designed to operate with 11.5 dBm input drive and for a 100 mA/mm bias current density at a drain voltage of $V_D = V_{D1} = V_{D2}$=28 V. The gate voltage ($V_G = V_{G1} = V_{G2}$) according to simulation should rest somewhere around V_G=3.5 V reverse bias. The PA had parametric

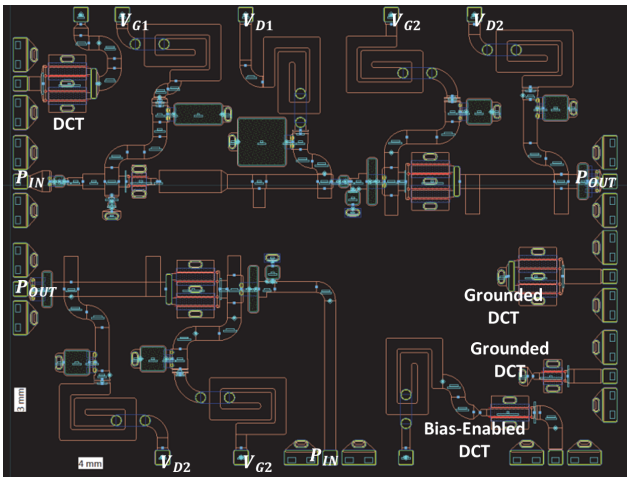
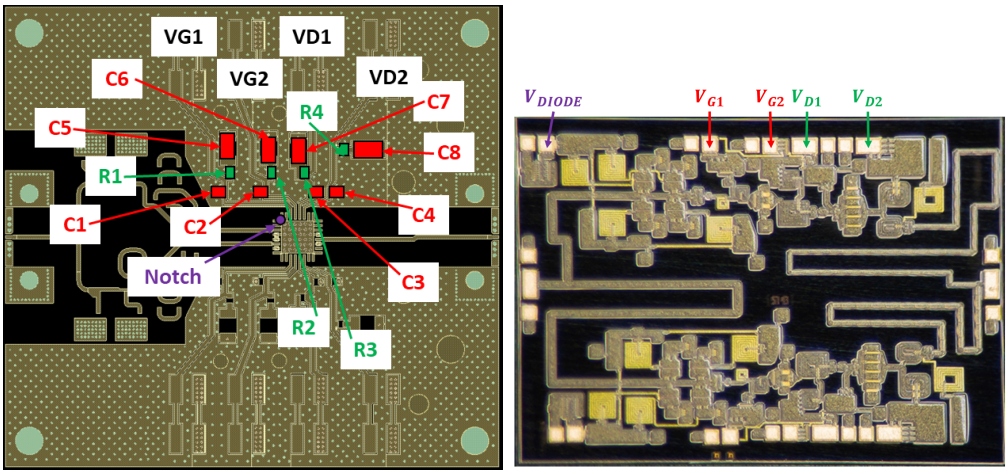


Figure B.1: X-Band inverse class-F PA diagram for bias and mounting setup [4]



(a) (b)

Figure B.2: Measurement diagram for (a) the RFIO splitter PCBs for hybrid implementation and (b) the RFIO MMIC in the case of probing and/or mounting.

oscillation issues at drive levels above 10 dBm for the bias condition. It could be partially stabilized utilizing 100 pF chip capacitors on each of the drain and gate biases, however, it was never able to fully stabilized [4].

B.2 Wideband Outphasing Combiner

This MMIC was designed in the Qorvo 250 nm GaAs process. The MMIC is a reconfigurable outphasing combiner utilizing enhancement mode switches to tune the reactive loading at the two input ports of the combiner. The e-mode switches are naturally in an off-state at 0 volt bias. However, the bias pads have a floating voltage problem and must all be tied to ground in order for the switches to correctly work. In order to bias the switches on a voltage of 1.3 V was used. Do not drive with a power greater than 20 dBm input in order to prevent damage of any of the switches. The order of the switch states is shown in Fig. 3.5 (a) with the inputs to the combiner on the left-hand side. The switch state configurations for different frequency bands are given in Table 3.1

B.3 X-Band Dual Input Outphasing PA

This MMIC was designed in the Qorvo 150 nm GaN es process. It was designed as a two stage branch PA and optimized for RF-input outphasing operation. The PA is designed to receive 12 dBm input power at

Form Factor	Element	Value	
0402	C1	100 pF	
	C2		
	C3		
	C4		
	R1	0 Ohms	
	R2		
	R3		
	R4		
0603	C5	100 nF	
	C6		
	C7		
	C8		
Bias	Vdiode	0 V	
	VG1	-2.55 V	Iq=80 mA/mm
	VG2		
	VD1	20 V	
	VD2		

Figure B.3: Table showing component and bias values for the RFIO PA implementations using the diagrams found in Fig. B.2.

each port so for a single drive with a 3 dB split the power should be 15 dBm. In order to bias the PA each of the gates should be set for an 80 mA/mm current density when the drain voltage is at 22 V. This should be around 2.55 V reverse bias. In order to stabilize the chip for the package implementation a 100 pF and 100 nF capacitor on each of the gate and drains are used. Dual bondwires or a ribbon bond are required at the drain pads in the case of mounting the MMIC to a carrier and breakout board implementation. The passive placements for the PCB as well as package orientation are shown in Fig. B.2 (a) as well as the mounting diagram in (b). The component and bias values are shown in Fig. B.3. The placement is mirrored to the bottom half of the PCB board/MMIC.

B.4 X-Band RFIO PA

This PA was designed in conjunction with the dual-input PA above. All the operating conditions are the same as above. The difference is that there are 2 additional bias pads, one on each side of the chip. These control the non-linear diode elements. A bias of -1 to 1 V can be applied to control the non-linear response without damaging the diodes. It was designed to operate at no bias control voltage. Fig. B.2 shows the PCB diagram as well as the mounting/probing diagram. The component and bias values are shown in Fig. B.3. The placement is mirrored to the bottom half of the PCB board/MMIC.

B.5 DIRO PA

This PA was designed in WIN PIH-110 GaAs process. The Chip is a two stage PA which is biased at 0.45 V gate voltage and 4 V drain voltage for each of the stages. In order to stabilize include 100 pF chip capacitors on each of the gate and drain pads. The addition of PIN diode switches for this design requires that each of the off PIN diode switches be set to -1 V for optimal off state performance and 1 V for optimal on state performance.

B.6 3 stage K-Band PA

This PA was designed in order to operate within a baseband feedback system for PA linearization. It is a 3 stage PA where each of the PAs are designed to operate at 80 mA/mm bias condition for 25 V drain bias. This should give a gate bias of around 2.5 V reverse bias. The input power for the PA is 10 dBm input power. It should be stable as is but 100 pF chip capacitors if feasible wouldn't hurt.