High Frequency DC-DC Power Conversion for Automotive LED Driver Applications

by

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High Frequency DC-DC Power Conversion for Automotive LED Driver Applications

Thesis directed by Professor Dragan Maksimović

This thesis studies high frequency dc-dc power converters for automotive LED driver applications. A high-frequency zero voltage switching (ZVS) integrated-magnetics Ćuk converter is well-suited for automotive LED-driver applications. In this converter, the input and output filter inductors and the transformer are realized on a single magnetic structure, resulting in very low input and output current ripples, thus reducing electromagnetic interference (EMI) and minimizing the required input and output filter capacitances. Active-clamp snubbers are used to mitigate the effects of the transformer leakage inductance. A prototype 1.8 MHz Ćuk converter with integrated magnetics is designed, built and tested. The prototype converter supplies 0.5 A output current to a string of 1-10 LEDs, and achieves 89.6% peak power-stage efficiency.

The use of active-clamp snubbers introduces additional conduction and gate-drive losses. This thesis introduces a planar integrated magnetics structure that is designed to minimize the transformer leakage inductance and therefore eliminates the need for snubbers. The planar integrated magnetics structure is optimized using 3D finite element modeling (FEM) tools. Two 1.8 MHz-to-2.4 MHz Ćuk converter prototypes are constructed: one using Silicon MOSFETs and the other using GaN transistors. The former achieves a peak efficiency of 92.9%, while the latter achieves a peak efficiency of 93.5% and a wider ZVS range. Both prototypes maintain greater than 90% efficiency across their wide output voltage range.

A new control architecture for the ZVS integrated magnetics Ćuk converter is presented. A Spice-based averaged circuit model is employed to model the converter dynamics. The duty-cycle-to-output-inductor-current transfer function is obtained and an integral compensator is designed to precisely regulate the output inductor current (LED current) over the entire output voltage range of the converter (3 V-to-50 V). To achieve high-resolution PWM dimming, new turn-off and

turn-on strategies are proposed. The proposed turn-off strategy reduces the fall time of the LED current by up to 83%, and the turn-on strategy reduces the rise time by up to 43%. The controller is implemented digitally and experimental results are presented.

This work also investigates resonant dc-dc converters as an alternative approach for automotive LED driver applications. The LLC resonant dc-dc converter is studied and is found that this converter suffers from high circulating currents, when designed to operate over a wide input and output voltage range. An LC^3L resonant dc-dc converter is proposed. The converter exhibits minimal circulating currents. Furthermore, it is shown that when appropriately designed, the converter behaves like a current source, with its output current being independent of the output voltage. This property is particularly favorable for automotive LED driver applications. A 10 MHz LC^3L resonant dc-dc converter is designed and simulated. This converter is predicted to achieve greater than 86% efficiency, and be 60% smaller in size compared to the planar integrated magnetics Ćuk converter.

Further increase in the switching frequency of automotive LED drivers demands exploring new design techniques and the use of high performance semiconductor devices. This thesis presents high efficiency dc-dc converters operating at very high frequencies using custom monolithic GaN-based half-bridge power stages with integrated gate drivers. A new gate driver circuitry is introduced, which enables efficient converter operation at very high switching frequencies, while maintaining very low quiescent power consumption. While using only n-type transistors in the GaN process, the proposed gate driver emulates complementary operation commonly employed in CMOS processes. A family of monolithic GaN chips is designed to operate over switching frequencies in the range of 20-400 MHz, at input voltages up to 45 V, while delivering up to 16 W of output power. The performance of the GaN chips is demonstrated in synchronous buck converters, which achieve record power stage efficiencies of 95.0% at 20 MHz, 94.2% at 50 MHz, 93.2% at 100 MHz, 86.5% at 200 MHz, and 72.5% at 400 MHz.

Dedication

To Sadra, my beloved son.

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I am highly grateful and indebted to my advisor Prof. Dragan Maksimović. He has been a mentor, teacher, a role model and a friend throughout the years of my Ph.D program. His deep knowledge and understanding of the various facets of power electronics has been an invaluable resource in my own explorations of the subject. It has always been an honor and a privilege to work under his supervision.

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CHAPTER 1

Introduction

Contents

This thesis is focused on analysis, modeling and design of high frequency and high efficiency switched-mode dc-dc power converters for automotive LED driver applications. This chapter provides a brief introduction to switched-mode power conversion and motivation for increasing the switching frequency, followed by a thesis outline.

1.1 Switched-Mode DC-DC Converters

A basic dc-dc power processing block is shown in Fig. 1.1, where an input DC voltage V_{IN} is converted to a desired dc output voltage V_{OUT}. A simple dc-dc converter that provides the desired voltage conversion while regulating the output voltage can be built using a series pass regulator, as shown in Fig. 1.2. The transistor effectively acts as a variable resistor and its resistance can be controlled using a voltage v_{ref}. The equivalent circuit model of this type of converter is shown in Fig. 1.3. The major drawback of such a dc-dc converter is that it has low efficiency. The efficiency

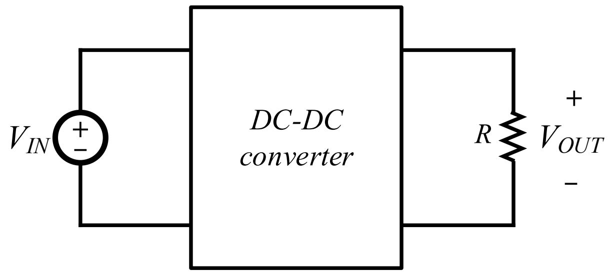


Figure 1.1: A basic power processing block.

is inversely proportional to the voltage conversion ratio. Due to thermal limitations, the output power of such converters is very limited. Another limitation is that this converter can only provide step-down voltage conversion. A simple switched-mode dc-dc converter is shown in Fig. 1.4 [2].

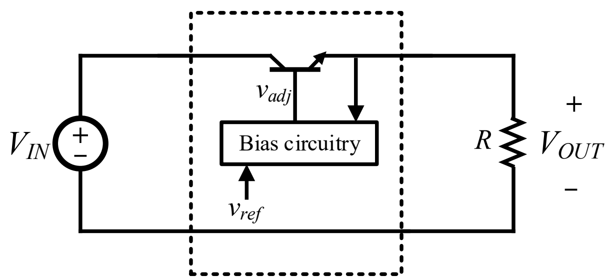


Figure 1.2: Series pass regulator as a dc-dc converter.

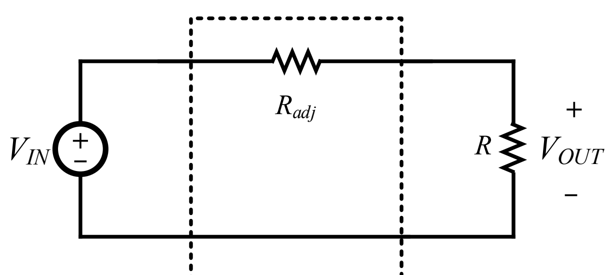


Figure 1.3: Equivalent circuit model of the series pass regulator.

This dc-dc converter comprises a single-pole double-throw (SPDT) switch along with a lossless LC filter at its output. The single-pole double-throw switch connects the switching node to the input

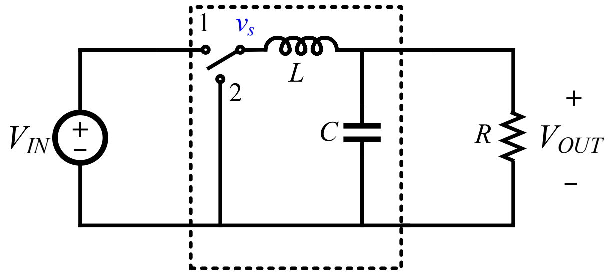


Figure 1.4: A switched-mode dc-dc converter.

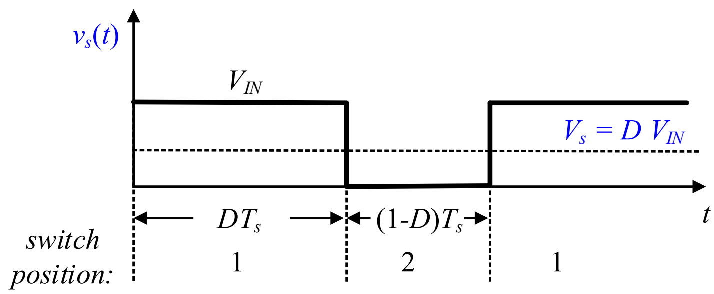


Figure 1.5: Switching node voltage v_s.

voltage source or to ground with a switching frequency $f_s = \frac{1}{T_s}$ and a duty-cycle D. During the first interval (DT_s), the switch is in position 1 and the switching node is connected to the input voltage source (V_{IN}). During the second interval ($(1-D)T_s = D'T_s$), the switch is in position 2 and the switching node is connected to ground. The resultant voltage waveform of the converter switching node, v_s, is shown in Fig. 1.5. The low-pass LC filter attenuates the harmonics present in v_s, providing the load with a dc output voltage V_{OUT}, which equals the average value of v_s ($V_{OUT} =< v_s >_{T_s}= DV_{IN}$). An ideal switched-mode dc-dc converter is 100% efficient. In practice, very high efficiencies can be achieved. In order to regulate the output voltage, a control system is added. A practical implementation of the step-down (buck) converter of Fig. 1.5 along with a feedback control loop to regulate the output voltage is shown in Fig. 1.6 [2]. The SPDT switch is implemented using a MOSFET and a diode. The output voltage of the converter is sensed and

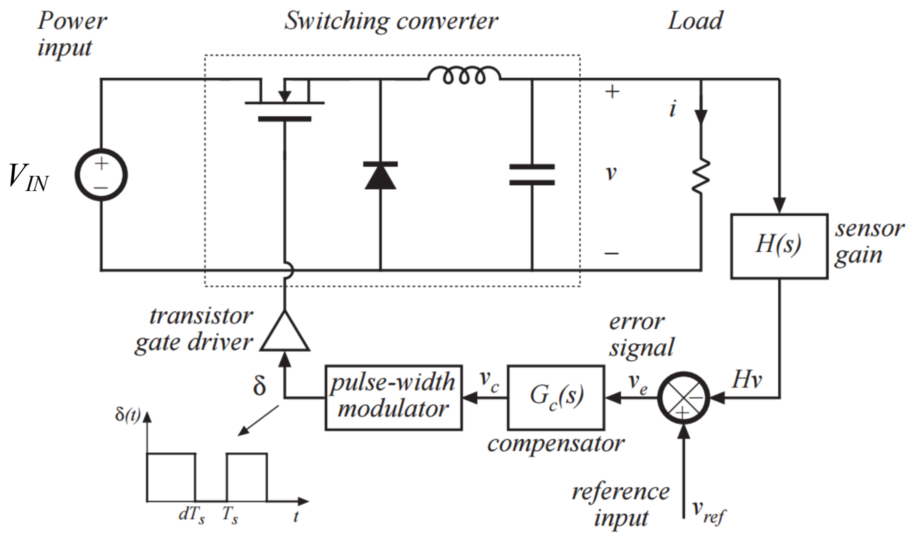


Figure 1.6: Switch-mode dc-dc converter with a control system to regulate the output voltage [2].

compared with a reference. The error is then fed into a compensator followed by a pulse-width modulator (PWM) modulator that generates the required control signal to drive the MOSFET.

1.2 Motivation for Increasing the Switching Frequency

Efficiency, bandwidth and size are important performance metrics for dc-dc power converters. The size and bandwidth of power converters are typically limited by passive energy storage components (inductors and capacitors). Energy storage requirements, and hence the required inductance (L) and capacitance (C) values in a power converter vary inversely with the converter switching frequency, that is, $L, C \propto f^{-1}$. The size versus frequency dependence is complicated due to ac losses in the windings and the magnetic core, which strongly depend on the frequency. The volume of a typical resonant inductor is shown as a function of switching frequency in Fig. 1.7 based on a detailed analysis presented in [1]. Smaller passive components and higher switching frequency also contribute to faster responses and potentials to achieve a higher regulation bandwidth. However, as the switching frequency of the converter is increased, various frequency-dependent loss mechanisms

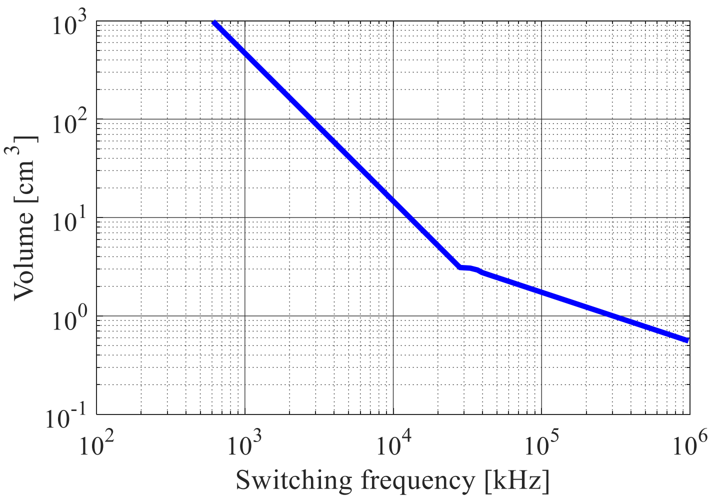


Figure 1.7: Resonant inductor volume vs. operating frequency [1].

are also exacerbated, resulting in reduced efficiency and potentially negating the aforementioned benefits of high frequency operation. For instance, in a semiconductor switching device such as a MOSFET, switching losses resulting from overlaps between the device voltage and current during transients increase linearly with the switching frequency. Another frequency dependent loss mechanism is related to the process of charging and discharging the gate capacitance of the MOSFET. In addition, as already mentioned, high frequency operation also results in increased core and winding losses in magnetic components.

In order to operate efficiently at high switching frequencies, appropriate power converter topologies capable of achieving soft switching, together with new design and optimization techniques and high performance semiconductor devices are required.

1.3 Automotive LED Driver Applications

Light-emitting diodes (LEDs) with dc-dc drivers are increasingly used in automotive lighting applications [3–11]. Compared to conventional incandescent lamps, LED-based lighting solutions result in lower power consumption and longer lifetime, together with additional flexibility. Depending on the specific lighting application, the number of series-connected LEDs (N in Fig. 3.1) can typically be between 1 and 15. As a result, the output voltage range is between about 3 V and about 50 V. The input voltage is nominally 12-14 V, but can be as low as around 4.5 V (during cold-start events) or as high as around 45 V (during "load dump" events). A dc-dc driver is required to efficiently deliver well regulated, low-ripple current to the string of series-connected LEDs, and must be designed to operate over wide ranges of output and input voltages. Fast converter turn on and turn off transitions are required to achieve high resolution dimming using pulse-width modulation of the output current at the rate of 200 Hz to 1 kHz, to avoid flicker. To meet fast turn-on and turn-off times, it is advantageous to minimize the need for large output filter capacitors and internal energy storage. Meeting EMI requirements in automotive applications is also challenging. Conventional LED driver dc-dc converters, which typically operate at hundreds of kHz [3, 4, 8–11], raise issues with AM radio interference. Table 1.1 lists state-of-the-art automotive LED drivers along with their operating frequencies and peak efficiencies.

Table 1.1: Efficiency and switching comparison for conventional state-of-the-art LED drivers.

Ref.	Peak Efficiency	f_{sw}(max)	Output Power
[3]	92%	120 KHz	30 W
[4]	89.7%	500 KHz	40 W
[8]	90%	350 KHz	40 W

The integrated magnetics Ćuk converter provides buck and boost capabilities as well as inherent input and output current filtering [12–20] is an attractive topology for LED driver applications. All three magnetic components in this converter (L_{in}, L_{out} and the transformer) are integrated on a single magnetic structure, which can be designed to minimize the input and output current ripples [12–20]. This reduces the input and output capacitance requirements, improving the converter's dynamic performance. Furthermore, when appropriately designed, the transistors in an integrated magnetics Ćuk converter can be operated with zero voltage switching (ZVS) over wide input and output voltage ranges. This enables the converter to be switched at high frequencies (above AM frequency band), hence relaxing EMI constraints. This thesis investigates and optimizes the integrated magnetics Ćuk converter for automotive LED driver applications, including a new control architecture that maintains precise wide-range regulation and achieves high resolution PWM dimming.

1.4 High frequency Operation of Automotive LED Drivers

Modern automotive LED driver applications demand very high resolution PWM dimming. To achieve higher performance, the switching frequency may be increased even further (>2.4 MHz). At high switching frequencies, PWM dc-dc converters exhibit higher switching losses and may require larger magnetics. Soft-switching resonant converters overcome these limitations and are viable candidates for high performance automotive LED driver applications. This thesis explores resonant converter topologies and proposes an LC^3L resonant dc-dc converter for automotive LED driver applications. The LC^3L resonant dc-dc converter, when appropriately designed, can produce a constant current to a string of LEDs and it maintains ZVS operation with minimal circulating current across wide operating ranges.

Further increases in switching frequency requires advances in circuit design techniques, as well as higher performance semiconductors, such as Gallium Nitride (GaN) based power devices [21–39]. In particular, monolithic integration of GaN switching power devices and gate drivers has enabled high efficiency operation of pulse-width modulated (PWM) converters at up to 200 MHz switching frequencies [22,24–26,39], with 90% power-stage efficiency at 100 MHz switching frequency reported in [22]. In this thesis, the monolithic power stage integration approach is extended to a quasi enhancement-mode GaN-on-SiC process using a new gate-driver circuit with improved switching speed versus power consumption trade-off. A family of monolithic GaN chips is designed for high efficiency operation at 20-400 MHz switching frequencies.

1.5 Thesis Organization

The first part of the thesis investigates various challenges associated with the design and implementation of a high frequency (1.8-2.4 MHz) ZVS integrated magnetics Ćuk converter. An implementation of this converter with active-clap snubbers is presented first. Then, a planar integrated magnetics structure is considered, in order to enhance the converter efficiency. A control methodology is introduced to regulate the output LED current and to perform high resolution PWM dimming. Further performance improvements by utilizing resonant dc-dc converters, such as the proposed LC^3L configuration are considered. The last part of the thesis is focused on opportunities to pursue even higher switching frequencies by means of monolithic integration of the gate-driver and power stage in a GaN process. A family of power stage GaN chips using the proposed gate-driver circuit is described, which optimizes the power consumption and switching speed at 20-400 MHz switching frequencies.

The thesis is organized as follows.

Chapter 2: This chapter studies automotive LED drivers based on a high frequency zero-voltage-switching (ZVS) integrated-magnetics Ćuk converter with active-clamp snubbers. An efficient numerical technique is introduced to analyze ZVS transitions and optimize the converter design, taking into account resonant transitions with active-clamp snubbers and non-linear transistor output capacitances. An experimental 1.8 MHz prototype, featuring very low input and output current ripples, and greater than 80% efficiency over wide output voltage range is demonstrated.

Chapter 3: A planar integrated-magnetics structure is used in the Ćuk converter to minimize the leakage inductance and eliminate the need for snubber circuitry. Based on state-plane analysis, the transformer magnetizing inductance is designed to achieve ZVS operation over a wide operating range. The planar integrated magnetics structure is optimized using a combination of analytical and 3D finite element method (FEM) tools. Experimental prototype converters using Silicon MOSFET and GaN transistors are built and experimental results are presented.

Chapter 4: The dynamics of the ZVS planar integrated magnetics Ćuk converter are analyzed in this chapter. A Spice averaged circuit model is utilized to quickly obtain the converter duty-cycle-to-output-current transfer function. An integral compensator is designed to achieve the desired closed loop performance over entire operation range. To achieve high resolution PWM dimming, new power-on and power-off strategies are proposed. The controller is implemented digitally and experimental results are presented.

Chapter 5: Resonant dc-dc converters for automotive LED driver applications are studied in this chapter. An LLC resonant converter is analyzed first, and designed to operate over a wide operating range. It is found that the converter suffers from high circulating currents. An LC^3L resonant dc-dc converter is proposed. The LC^3L resonant dc-dc converter, when properly designed, behaves as a current source and can provide a constant current to a string of LEDs. Tank design guidelines and simulation results are shown for a prototype operating at 10 MHz.

Chapter 6: The monolithic integrated gate driver GaN power stages are presented in this chapter. A new gate-driver circuit with improved switching speed versus power consumption is proposed. The GaN chip optimization is summarized and experimental results, including switching waveforms and efficiency measurements, are presented for prototyped synchronous buck test converters operating at 20-400 MHz switching frequencies from up to 45 V supply voltage.

Chapter 7: The thesis contributions and opportunities for future work are summarized in Chapter 7.

CHAPTER 2

Automotive LED Driver Based On High Frequency Zero Voltage Switching Integrated Magnetics Ćuk Converter

Contents

This chapter presents an automotive LED driver based on a high frequency zero-voltage-switching (ZVS) integrated-magnetics Ćuk converter with active-clamp snubbers, as shown in Fig 2.1. The prototype converter operates at 1.8 MHz switching frequency, above the AM frequency band. The transformer magnetizing inductance is designed such that the magnetizing current, in combination with the transformer leakage current, can be used to achieve ZVS over a wide operating range. All three magnetic components in this converter (L_{in}, L_{out} and the transformer) are integrated on a single magnetic component, designed to minimize input and output current ripples [12–20]. As a result, the need for additional filtering on the input side is greatly reduced, and no output filter capacitor is required on the output side. The integrated magnetic structure not only reduces the overall size of the magnetics structure but also greatly reduces the self inductance of the input and output inductors, allowing for fast turn-on and turn-off transients. Active-clamp snubbers are used to mitigate the effect of the leakage inductance and limit the volt-

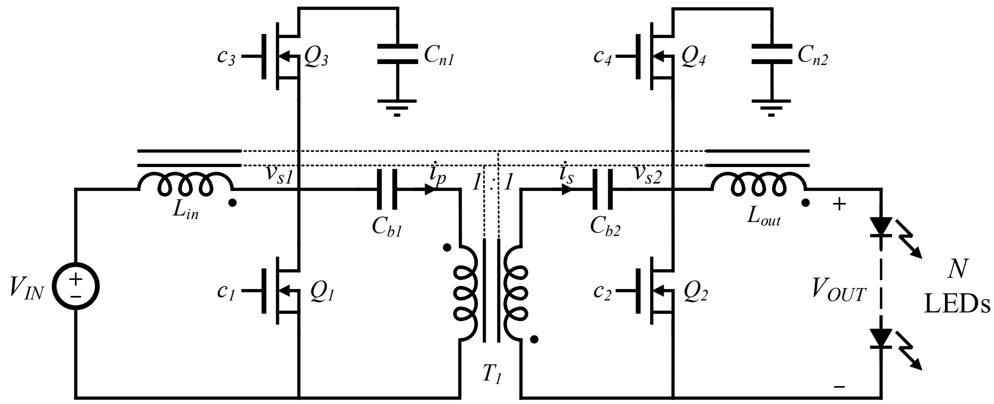


Figure 2.1: Zero voltage switching (ZVS) integrated-magnetics Ćuk converter with active-clamp snubbers.

age stress on the devices [40–42]. However, it is found that the active-clamp snubbers introduce substantial deviations in the steady-state operation of this converter when compared to a conventional Ćuk converter. An efficient numerical technique is introduced to address ZVS transitions and to optimize the design, taking into account resonant transitions with active-clamp snubbers and non-linear transistor output capacitances [43]. Experimental 1.8 MHz prototype features very low input and output current ripples, and greater than 80% efficiency over wide output voltage range.

The chapter is organized as follows. Section 6.2 presents analysis of the converter shown in Fig 2.1. Prototype design and experimental results are presented in Section 4.2. Section 6.4 summarizes the chapter.

2.1 Zero-Voltage Switching Integrated-Magnetics Ćuk Converter with Active-Clamp Snubbers

The power stage of the integrated-magnetics Ćuk converter consists of transistor Q_1 and synchronous rectifier Q_2, energy-transfer capacitors C_{b1} and C_{b2}, input and output filter inductors L_{in} and L_{out}, and transformer T_1, as shown in Fig. 2.1. The integrated magnetics, designed as described in [13, 16] results in very low input and output current ripples so that I_{IN} and I_{OUT} can be considered dc currents in steady-state operation of the converter. The active-clamp snubbers (Q_3 and C_{n1} on the primary side, and Q_4 and C_{n2} on the secondary side mitigate the effects of the transformer leakage inductance, clamp the transistor voltage stresses close to the ideal value ($V_{IN} + V_{OUT}$), and participate in ZVS resonant transitions of all transistors [44–46]. It should be noted, however, that the active-clamp snubbers introduce substantial deviations in the steady-state operation of this converter when compared to a conventional Ćuk converter, which is addressed further in the rest of the chapter.

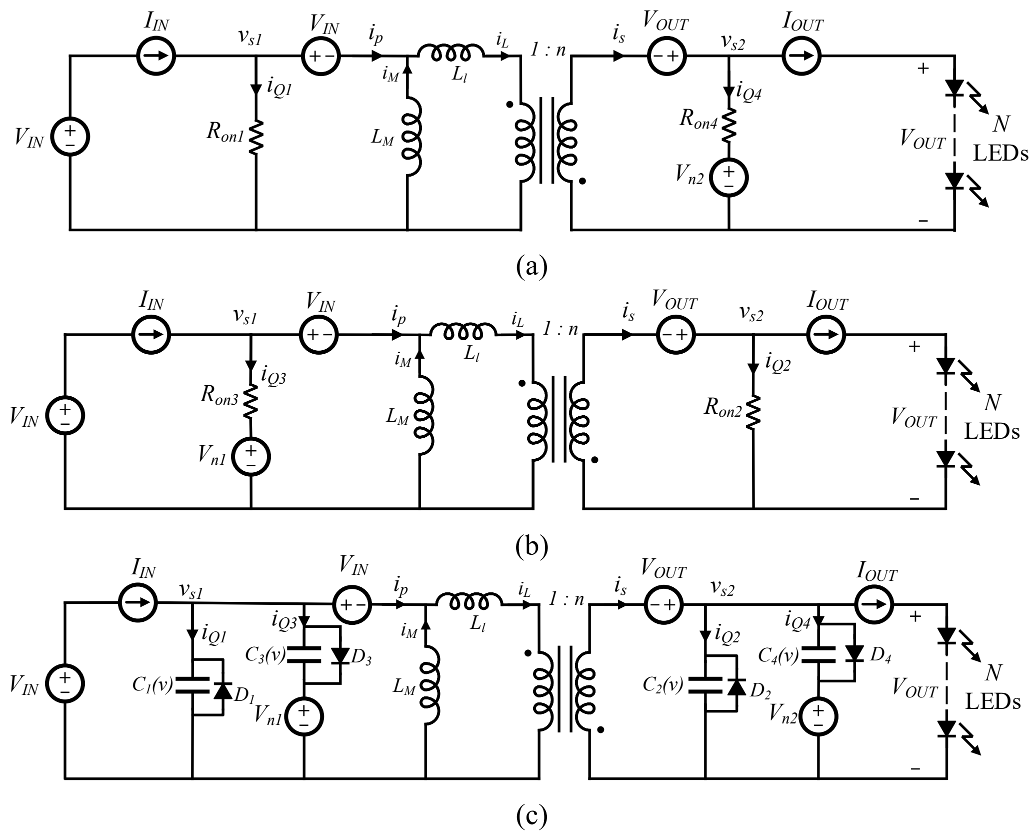


Figure 2.2: Equivalent circuit models of the Ćuk converter with active-clamp snubbers during: (a) DT_s interval, (b) $D'T_s$ interval, and (c) commutation intervals. The transformer is represented using the Cantilever model where L_M is the magnetizing inductance and L_l as the leakage inductance.

Steady-state operation of the Ćuk converter is divided into four subintervals. In the first subinterval, the primary-side power-stage transistor Q_1 and the secondary-side active-clamp transistor Q_4 are on, while Q_2 and Q_3 are off, leading to the equivalent circuit shown in Fig. 2.2(a).

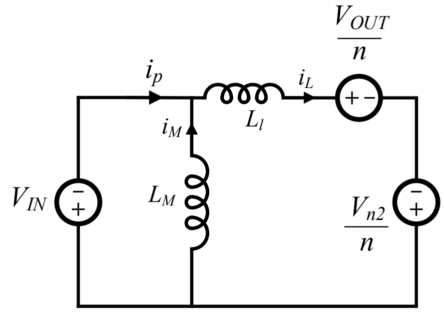


Figure 2.3: Simplified equivalent circuit model during DT_s interval.

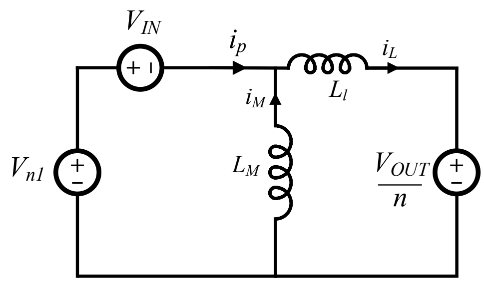


Figure 2.4: Simplified equivalent circuit model during $D'T_s$ interval.

During this interval the current in the active-clamp transistor Q_4 is given by:

$$i_{Q4} = i_s - I_{OUT} = \frac{i_L}{n} - I_{OUT} \, . \tag{2.1}$$

Hence,

$$\Delta i_{Q4} = \frac{\Delta i_L}{n} \, . \tag{2.2}$$

Neglecting the transistor on-resistance and reflecting V_{OUT} and V_{n2} to the transformer's primary side, Fig. 2.2(a) can be reduced to Fig. 2.3. The amplitude of the current ripple in the leakage inductance current during this interval is given by

$$\Delta i_L = \frac{-V_{IN} + \frac{-V_{OUT}+V_{n2}}{n}}{2L_l} DT_s \, , \tag{2.3}$$

where V_{n2} is the DC voltage across capacitor C_{n2} in Fig. 2.1. Since Q_4 is in series with the snubber capacitor C_{n1}, i_{Q4} cannot have a dc component. Therefore, $i_{Q4}(t)$ waveform during the first subinterval can be constructed using (2.1) and (2.2). Rewriting (2.1), the leakage inductance

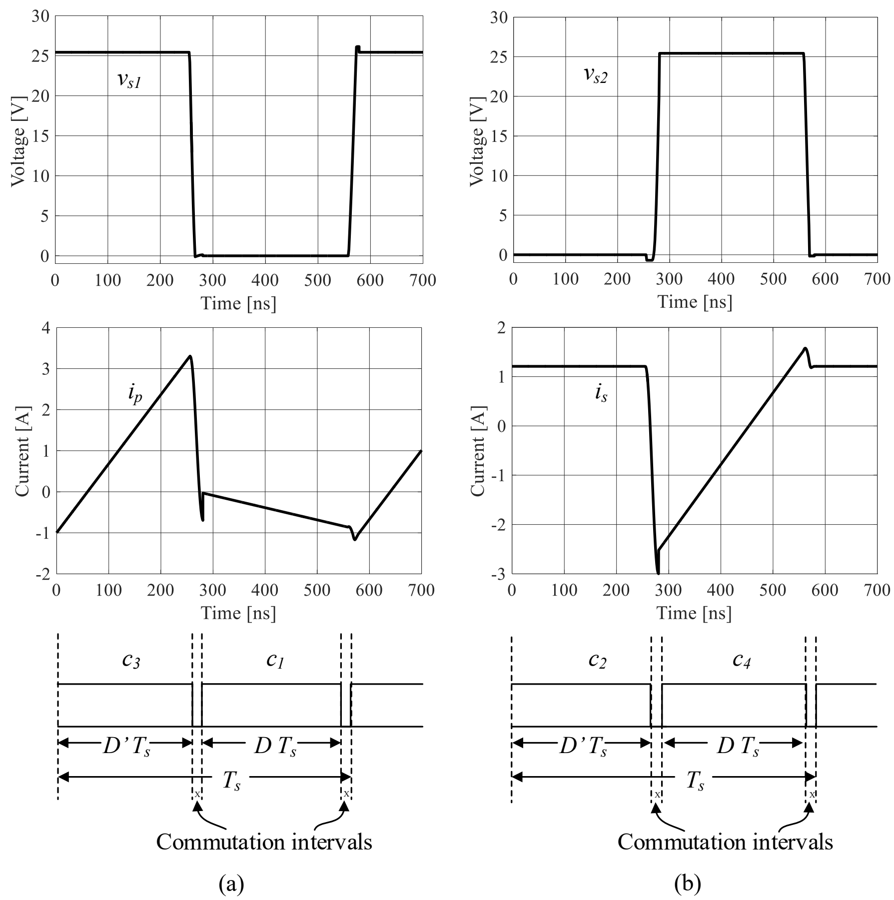


Figure 2.5: (a) Switch-node voltage v_{s1}, transformer primary current i_p and input control signals c_1 and c_3; (b) switch-node voltage v_{s2}, transformer secondary current i_s and input control signals c_2 and c_4. $V_{IN} = 12$ V, $V_{OUT} = 12$ V and $I_{OUT} = 0.5$ A.

current can be expressed as

$$i_L = n(i_{Q4} + I_{OUT})\,. \tag{2.4}$$

As shown in Fig. 2.3 the magnetizing inductance voltage is V_{IN}. Therefore, the magnetizing inductance current ripple Δi_M can be written as

$$\Delta i_M = \frac{V_{IN}}{2L_M} DT_s\,, \tag{2.5}$$

and the magnetizing inductance current $i_M(t)$ can be constructed using

$$i_M = I_{M0} + \frac{\Delta i_M}{DTs} t\,, \tag{2.6}$$

where I_{M0} is the initial condition for the magnetizing inductance current. The transformer primary and secondary currents can be found using

$$i_p = i_L - i_M \,, \tag{2.7}$$

$$i_s = \frac{i_L}{n} \,, \tag{2.8}$$

while the current i_{Q1} in transistor Q_1 is given by

$$i_{Q1} = I_{IN} - i_p \,. \tag{2.9}$$

During this interval the converter switching node voltages, V_{s1} and V_{s2}, can be considered constant and are, neglecting conduction losses, given approximately by

$$v_{s1} \approx 0 \,, \tag{2.10}$$

and

$$v_{s2} \approx V_{n2} \,. \tag{2.11}$$

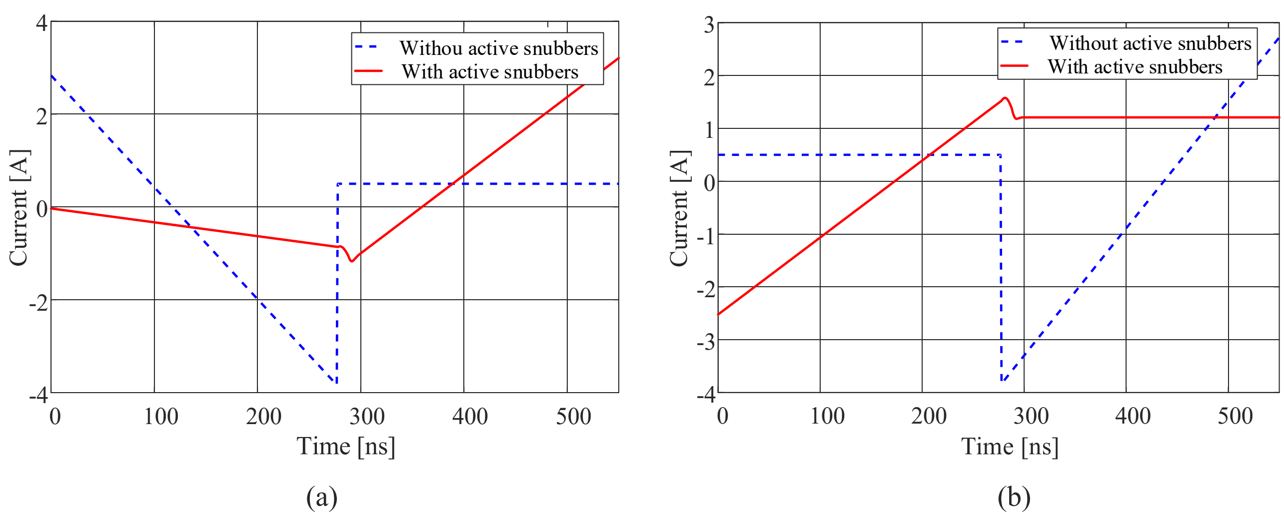


Figure 2.6: The transformer current waveforms for the Ćuk converter with and without active snubbers, (a) primary current i_p and (b) secondary current i_s. $V_{IN} = 12$ V, $V_{OUT} = 12$ V and $I_{OUT} = 0.5$ A.

At the end of this subinterval, Q_1 and Q_4 are turned off, initiating a resonant transition during which the converter assumes the equivalent circuit shown in Fig. 2.2(c). A numerical solution to the resonant transition waveforms is described in Section 2.1.1. Assuming ZVS conditions are met, the resonant transition ends when the secondary-side power stage transistor Q_2 and the primary-side snubber transistor Q_3 are turned on, resulting in the equivalent circuit shown in Fig. 2.2(b). The converter switching node voltages, V_{s1} and V_{s2} are given by:

$$v_{s1} \approx V_{n1}\,, \tag{2.12}$$

and

$$v_{s2} \approx 0\,. \tag{2.13}$$

In this interval, the active clamp transistor current, i_{Q3}, can be written as

$$i_{Q3} = I_{IN} - i_p = I_{IN} - i_L + i_M\,. \tag{2.14}$$

Similar to i_{Q4}, i_{Q3} does not have any dc component, so that an expression for $i_{Q3}(t)$ can be obtained based on the ripple

$$\Delta i_{Q3} = -\Delta i_L + \Delta i_M\,. \tag{2.15}$$

In order to evaluate the current ripples in i_L and i_M, the simplified circuit model of Fig. 2.2b is redrawn in Fig. 2.4 by neglecting the transistor on-resistances and transferring V_{OUT} to the transformer primary side,

$$\Delta i_L = \frac{V_{n1} - V_{IN} - \frac{V_{OUT}}{n}}{2L_l} \times D'T_s\,, \tag{2.16}$$

and

$$\Delta i_M = \frac{V_{n1} - V_{IN}}{2L_M} \times D'T_s\,, \tag{2.17}$$

where V_{n1} is the voltage of the active snubber capacitor C_{n1}, which is considered constant, and the leakage inductance current is

$$i_L = I_{IN} - i_{Q3} + i_M\,. \tag{2.18}$$

During this interval, the magnetizing current i_M is given by:

$$i_M = I_{M0} + \frac{\Delta i_M}{D'T} t\,, \tag{2.19}$$

where I_{M0} is the magnetizing inductance current at the end of the previous transition. Other waveforms in the circuit during this interval can be obtained as follows:

$$i_{Q2} = \frac{i_L}{n} - I_{OUT}\,, \tag{2.20}$$

$$i_p = I_{IN} - i_{Q3}\,, \tag{2.21}$$

$$i_s = \frac{i_L}{n}\,. \tag{2.22}$$

At the end of this subinterval, Q_2 and Q_3 are turned off, and the converter reverts to the equivalent circuit of Fig. 2.2(c) undergoing the second resonant transition, which is solved numerically as described in the next section.

2.1.1 Zero-voltage-switching resonant transitions

The magnetizing inductance of the transformer is selected to ensure ZVS operation at the converter's worst-case operating point, which corresponds to the maximum step-up conversion ratio. The resultant magnetizing inductance is relatively small, and comparable in value to the transformer's leakage inductance. Therefore, in contrast to the conventional Ćuk converter, both the magnetizing and the leakage inductances resonate with transistor output capacitances during ZVS transitions. Furthermore, since no additional capacitors are used in the resonant circuits, the nonlinearity in the device output capacitance plays a significant role, as discussed in [43].

The transistor output capacitance is modeled as a voltage-depended capacitance using polynomial curve fit,

$$C(v) = \alpha_0 + \alpha_1 v^1 + \alpha_2 v^2 + \alpha_3 v^3 + \alpha_4 v^4\,, \tag{2.23}$$

where the coefficients are found from datasheet charts.

During commutation intervals, the state equations of the converter are written in a compact matrix form using the equivalent circuit model of the converter in Fig. 2.2c,

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t)\,. \tag{2.24}$$

Here, the state vector $x(t)$ is a vector containing the inductor currents and the capacitor voltages. The state-space equations (2.24) for the equivalent circuit of Fig. 2.2(c) are derived and solved numerically using a short time step ($\Delta t = 50$ ps),

$$x_n = x_{n-1} + (A_{n-1}x_{n-1} + Bu_n)\Delta t, \quad n = 1, 2, 3..... \tag{2.25}$$

where A_{n-1} contains the values of transistor output capacitances at time $n-1$. The transistor output capacitances are considered constant over time-step Δt and are updated using (2.23) in each time step.

2.1.2 Steady-state waveforms

The converter waveforms are obtained by concatenating the waveforms obtained from the four subintervals as described earlier, including analytical solutions in the DT_s and $D'T_s$ intervals, and the numerical solution to resonant transitions as described in Section 2.1.1. This analysis is numerically iterated until a steady-state solution is obtained. Using this approach, steady state waveforms of the converter can be obtained quickly at any particular operating point, and for any set of parameter values. This allows for choosing the power-stage parameter values, and in particular the transformer magnetizing inductance, to achieve desired ZVS operation, as discussed further in the next section.

As example, Fig. 2.5 shows the steady-state waveforms obtained for $V_{IN} = 12$ V, V_{OUT} =12 V and $I_{OUT} = 0.5$ A, using the parameter values in the experimental prototype described in Section 4.2. The primary-side switch-node voltage and transformer current are shown in Fig. 2.5(a), while the corresponding secondary-side waveforms are shown in Fig. 2.5(b). In Fig. 2.6, the transformer currents $i_p(t)$ and $i_s(t)$ are overlaid with the corresponding transformer currents for a Ćuk converter without active-clamp snubbers (when the leakage inductance is zero). The operating condition is considered the same and waveforms are shown for one switching period. One may note that the transformer currents $i_p(t)$ and $i_s(t)$ in a Ćuk converter with active-clamp snubbers differ significantly from those in a Ćuk converter without active-clamp snubbers. In particular, small voltages across the leakage inductance, as given by (2.3) and (2.16), result in significant current ripples in the transformer leakage inductance, which consequently alter the converter current waveforms, as well as ZVS conditions.

2.2 Prototype Design and Experimental Results

This section describes a prototype design and experimental results obtained when the converter is used to supply current through a string of LEDs.

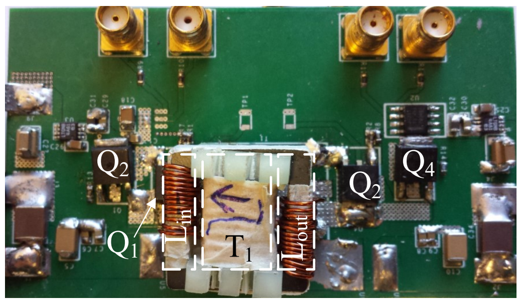


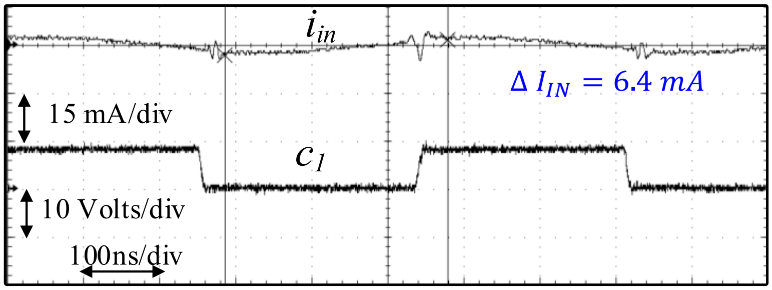
Figure 2.7: Photograph of the 1.8 MHz ZVS integrated-magnetics Ćuk converter.

Table 2.1: Design specifications for the integrated-magnetics Ćuk converter.

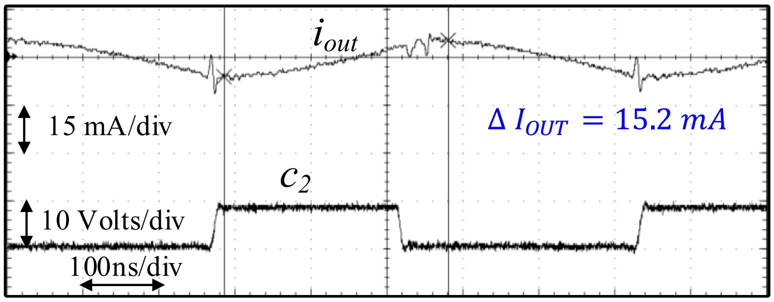
Switching frequency f_{sw}	1.8 MHz
Input voltage V_{IN}	12 V
Output voltage V_{OUT}	3 V to 30 V
Output current I_{OUT}	0.5 A

2.2.1 Prototype design

Using the analysis approach presented in Section 6.2, a prototype of the high-frequency ZVS integrated magnetics 1.8 MHz Ćuk converter is designed based on the specifications listed in Table 5.1. The converter input voltage is 12 V while the output voltage varies from 3 V to 30 V. As stated earlier in Section. 6.2, during resonant transitions, both the leakage inductance and magnetizing inductance of the transformer resonate with the transistor output capacitances. In the



(a)



(b)

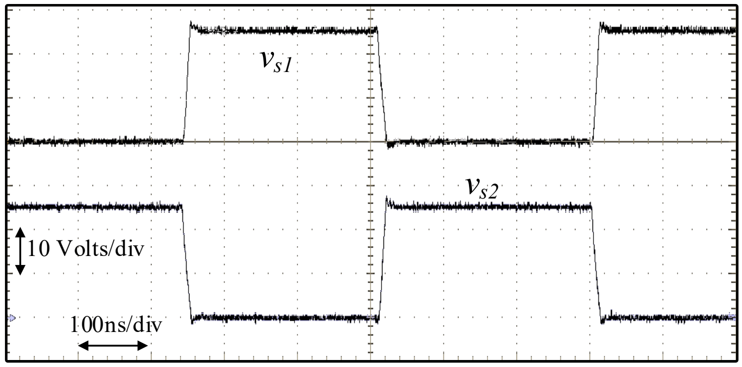
Figure 2.8: (a) Input current ripple, and the control signal c_1. (b) output current ripple, and the control signal c_2. $V_{IN} = 12$ V, V_{OUT} =12 V and $I_{OUT} = 0.5$ A.

magnetics design, leakage inductance is a less controlled parameter compared to the magnetizing inductance of the transformer. The design approach taken to ensure ZVS operation is to select a magnetizing inductance first based on approximate considerations, and then to evaluate and refine the design based on the solution approach described in Section 6.2. In presence of wide variations in input voltage, the converter can be further optimized to achieve ZVS for the minimum input voltage, which also ensures ZVS for higher input voltages. Referring to Fig. 2.2(c), the transistor current i_{Q1} during a resonant transition can be found as

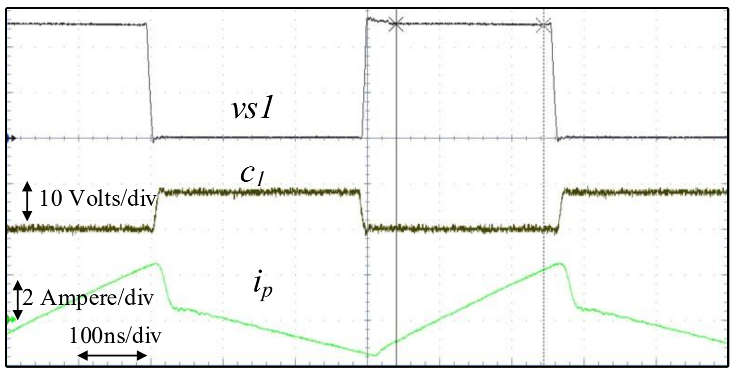
$$i_{Q1} = I_{IN} + nI_{OUT} + i_M\,. \tag{2.26}$$

During the commutation interval, i_{Q1} needs to be negative in order to achieve ZVS of the transistor Q_1. Therefore, the magnetizing current ripple must be larger than the sum of input current and the output current, that is:

$$\Delta i_M > I_{IN} + nI_{OUT}\,, \tag{2.27}$$



(a)



(b)

Figure 2.9: (a) Primary-side switch-node voltage v_{s1}, and the secondary-side switch-node voltage v_{s2}. (b) Primary-side switch-node voltage v_{s1}, the control signal c_1, and the transformer primary current i_p. V_{IN} = 12 V, V_{OUT} =12 V and I_{OUT} = 0.5 A.

where $I_{IN} \approx \frac{D}{D'} I_{OUT}$. Assuming a constant output current I_{OUT}, the worst case scenario occurs when the input current is at its highest DC level. Therefore, if the converter is designed to achieve ZVS at its highest duty cycle, then ZVS is ensured for all lower duty cycles. The secondary side transistor current i_{Q2} is given by:

$$i_{Q2} = \frac{I_{IN}}{n} - nI_{OUT} + i_M \,. \tag{2.28}$$

One may notice that if (2.27) is satisfied, then (2.28) implies that ZVS condition is also satisfied for transistor Q_2.

Referring to Fig. 2.2(a), the required magnetizing inductance can be found as:

$$L_M = \frac{V_{IN} D T_s}{2\Delta i_M} \,. \tag{2.29}$$

This presents a starting point for the design of the integrated magnetics. The selected core is Ferroxcube's E/20/10/5, with the 3F46 ferrite material suitable for MHz switching. The number of turns in the transformer is optimized to minimize the total (core and winding) losses. An air-gap is inserted in the center leg of the core to achieve the desired magnetizing inductance. In addition, the number of turns in the input and the output inductors are adjusted to minimize the ripple in the input and output currents. The leakage inductance of the optimized transformer is measured to be 190 nH.

The analysis approach described in Section 6.2 is employed to optimize the converter design. The energy-transfer capacitors C_{b1} and C_{b2} are designed to ensure small voltage ripples (less than 5%) under the worst-case operating condition (highest duty cycle).

$$C_{b1} = \frac{I_p D T_s}{\Delta V_{b1}} \,. \tag{2.30}$$

Here, I_M is the peak current in the transformer primary. The same approach is employed to calculate the value of C_{b2},

$$C_{b2} = \frac{I_s D T_s}{\Delta V_{b2}} \,. \tag{2.31}$$

Here, I_s is the peak current in the transformer secondary. C_{n1} and C_{n2} are designed using a similar approach, but with more relaxed ripple constraints. Power MOSFETs are selected by a search through a large transistor database, in order to achieve the best trade-off between conduction and switching losses.

The components used in the prototype along with the design parameters are listed in Table 2.2.

2.2.2 Experimental results

A photograph of the experimental prototype is shown in Fig. 6.5. As can be seen from Fig. 6.5, the input and output inductors (L_{IN} and L_{OUT}) of the converter are wound on the outer legs of the transformer core, while the transformer windings are wound on the center leg. The

Table 2.2: Components in the integrated-magnetics Ćuk converter prototype.

Transistors Q_1 to Q_4	Fairchild FDD86252
Energy-transfer capacitors C_{b1}, C_{b2}	4.5 μF
Active-clamp snubber capacitors C_{n1}, C_{n2}	2.2 μF
Input inductor L_{IN} winding	13 turns of #23 AWG
Output inductor L_{OUT} winding	15 turns of #23 AWG
Transformer primary and secondary winding	4 turns of 1000-strand #48 AWG Litz
Magnetic core	Ferroxcube E/20/10/5 core, 3F46 material
Magnetizing inductance L_M	650 nH
Leakage inductance L_l	190 nH
Transformer cantilever model turns-ratio n	0.92
Gate-drivers	Texas instruments UCC27211

ac-coupled input and output currents waveforms of the converter are shown in Fig. 2.8, showing less than 3% ripple.

Measured primary-side switch-node voltage v_{s1} and the secondary-side switch-node voltage v_{s2} are shown in Fig. 2.9(a). One may note smooth transitions of v_{s1} and v_{s2} which indicate ZVS commutations of the transistors. Also, the primary-side switch-node voltage v_{s1}, aligned with the control signal c_1 and the transformer primary-side current i_p are shown in Fig. 2.9(b) for an input voltage of 12 V and output current of 0.5 A. Power stage and overall efficiency (including the

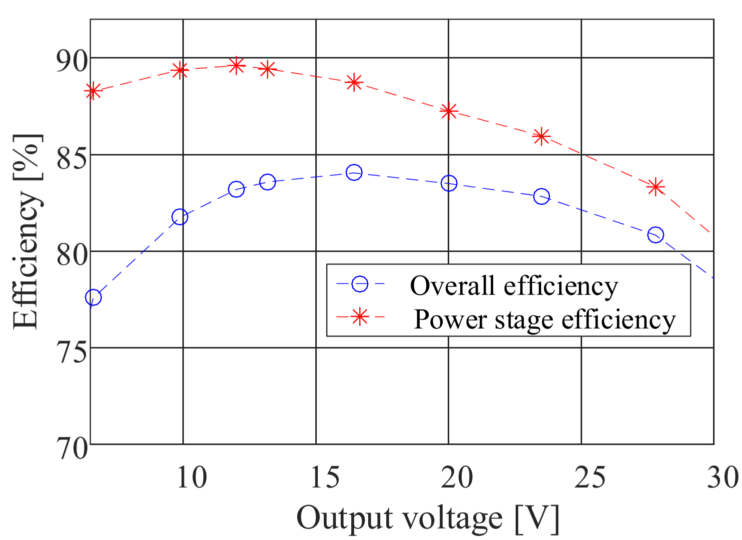


Figure 2.10: Power stage and overall efficiency versus output voltage. $V_{IN} = 12$ V and $I_{OUT} = 0.5$ A.

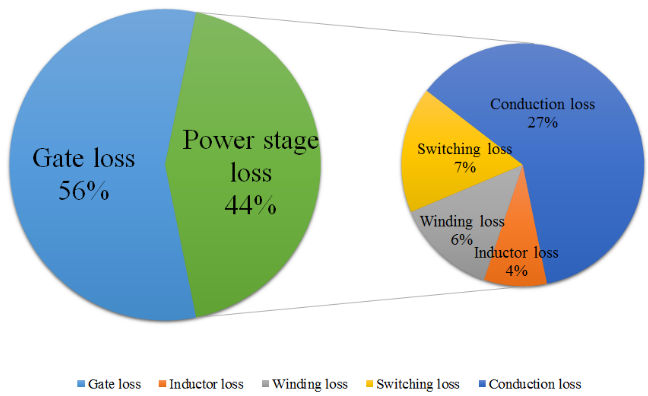


Figure 2.11: The converter loss breakdown. $V_{IN} = 12$ V, $V_{OUT} = 12$ V and $I_{OUT} = 0.5$ A.

gate-driver losses) of the prototype converter are shown in Fig. 2.10 as functions of the output voltage (which correspond to different numbers of LEDs at the output). It can be seen that the converter achieves a peak power-stage efficiency of 89.6% and maintains greater than 80% overall efficiency over a wide range of output voltages. A converter loss breakdown is shown in Fig. 2.11. The effect of gate-drive losses, which are significant at the 1.8 MHz switching frequency, can be observed.

2.3 Summary

This chapter presents a high-frequency zero voltage switching (ZVS) integrated-magnetics Ćuk converter suitable for automotive LED-driver applications. This Ćuk converter utilizes active-clamp snubbers on both the input and the output side to mitigate the effect of the transformer leakage inductance. The magnetic components of the converter are integrated on a single structure, facilitating ripple cancellation in both the input and output currents. Furthermore, an analysis technique is introduced to quickly evaluate the steady state behavior including the effects of non-linear transistor output capacitances on ZVS transitions. A prototype 1.8 MHz Ćuk converter with integrated magnetics is designed, built and tested. The prototype converter achieves 89.6% peak power-stage efficiency and maintains greater than 80% overall efficiency across a wide output voltage range. The use of active-clamp snubbers introduces additional gate-drive and conduction losses.

Efficiency can be improved by reducing the transformer leakage inductance and hence eliminating the need for active snubbers, as discussed further in the next chapter.

CHAPTER 3

High-Frequency ZVS Ćuk Converter for Automotive LED Driver Applications using Planar Integrated Magnetics

Contents

In this chapter, a planar integrated-magnetics structure is used in the ZVS integrated magnetics Ćuk converter of Fig. 3.1 to minimize leakage inductance and eliminate the need for passive or active snubbers. Using state-plane analysis, the transformer magnetizing inductance is designed to achieve ZVS operation over a wide operating range. The planar integrated magnetics structure is optimized using a combination of analytical and 3D finite element method (FEM) tools.

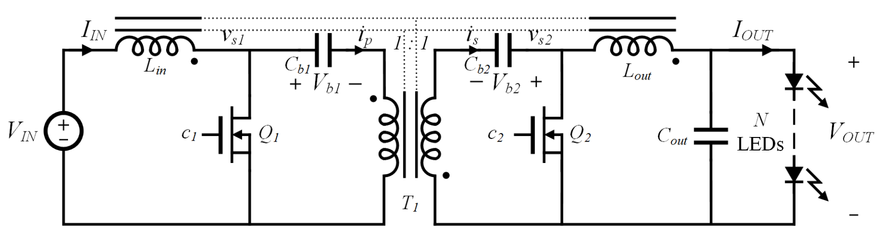


Figure 3.1: Integrated magnetics Ćuk converter for automotive LED driver applications.

Experimental prototype converters are constructed using Silicon MOSFET or GaN transistors. Both prototypes operate at 1.8 MHz-to-2.4 MHz, above the AM frequency band, achieve low input and output current ripples, and maintain greater than 90% efficiency over wide output voltage range. It is shown how GaN transistors result in 93.5% peak efficiency, which is 0.6% higher compared to the peak efficiency of the Silicon MOSFET prototype. The GaN prototype offers up to 5.5% higher efficiency over the full voltage range.

The chapter is organized as follows. Section 3.1 presents operation and analysis of the integrated magnetics Ćuk converter shown in Fig. 3.1. The design of the planar integrated structure is described in Section 3.2. Experimental results are presented in Section 4.2. Section 6.4 summarizes the chapter.

3.1 ZVS Ćuk Converter with Integrated Magnetics

The converter schematic is shown in Fig. 3.1. All magnetic components are realized on the same core, resulting in low input and output ripples as described in [13,16]. A simplified schematic of ZVS Ćuk converter is shown in Fig. 3.2. Input and output filter inductors are modeled as dc current sources and energy transfer capacitors are modeled as dc voltage sources. The transformer leakage inductance is neglected and the circuit elements are transformed to the primary side of the transformer.

Steady-state operation of the Ćuk converter is divided into four subintervals, following the standard zero-voltage-switching quasi-square-wave (ZVS-QSW) approach. During DT_s (where D is the duty cycle), the primary-side transistor Q_1 is on while the synchronous rectifier Q_2 is off. The magnetizing inductance current i_M increases linearly with a slope $\frac{V_{b1}}{L_M} = \frac{V_{IN}}{L_M}$. At the end of this interval, Q_1 is turned off, and the transformer magnetizing inductance L_M resonates with the transistor output capacitances. During the third interval $(1-D)T_s$, transistor Q_2 is turned on, while Q_1 is off. The magnetizing current i_M now decreases with a slope $\frac{V_{b2}}{L_M} = \frac{V_{OUT}}{L_M}$. This interval is followed by a second resonant transition. Typical steady-state switching node voltages v_{s1}, v_{s2}, and the transformer magnetizing current i_M are shown in Fig. 3.3(a). In order to achieve ZVS, the magnetizing current ripple Δi_M must be larger than the sum of the input and the output currents,

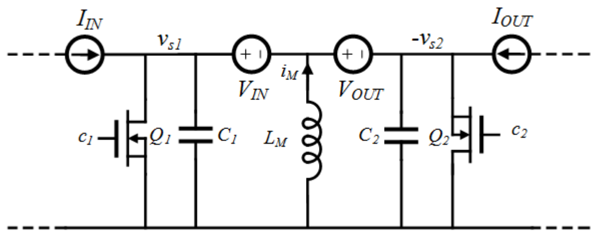


Figure 3.2: Simplified schematic of the ZVS-QSW Ćuk converter.

$\Delta i_M > I_{IN} + I_{OUT}$, where ripples in the input and the output inductor current are neglected. State-plane analysis is used to select the magnetizing inductance and the switching frequency to achieve ZVS operation [47]. Capacitors C_1 and C_2 are charge equivalent capacitors representing the device output capacitances. During commutation intervals t_{d1} and t_{d2}, capacitors C_1, C_2 and the transformer magnetizing inductance L_M are effectively in parallel. A typical steady-state state-plane trajectory is shown in Fig. 3.3(b), where the normalized voltage across resonant capacitor $C_r = C_1 + C_2$ is denoted as $\mathrm{m_C}$ and j denotes the normalized current i defined as:

$$i = i_M + I_{IN} + I_{OUT} \,. \tag{3.1}$$

The state-plane equations are as follows:

$$V_{base} = V_{IN} + V_{OUT} \,, \tag{3.2}$$

$$\omega = \frac{1}{\sqrt{L_M C_r}} \,, \tag{3.3}$$

where C_r is the sum of the transistor output capacitances.

$$R_o = \sqrt{\frac{L_M}{C_r}} \,, \tag{3.4}$$

$$I_{base} = \frac{V_{base}}{R_o} \,, \tag{3.5}$$

$$M = \frac{V_{OUT}}{V_{IN}} \,, \tag{3.6}$$

$$\mu = \frac{M}{1+M} \,, \tag{3.7}$$

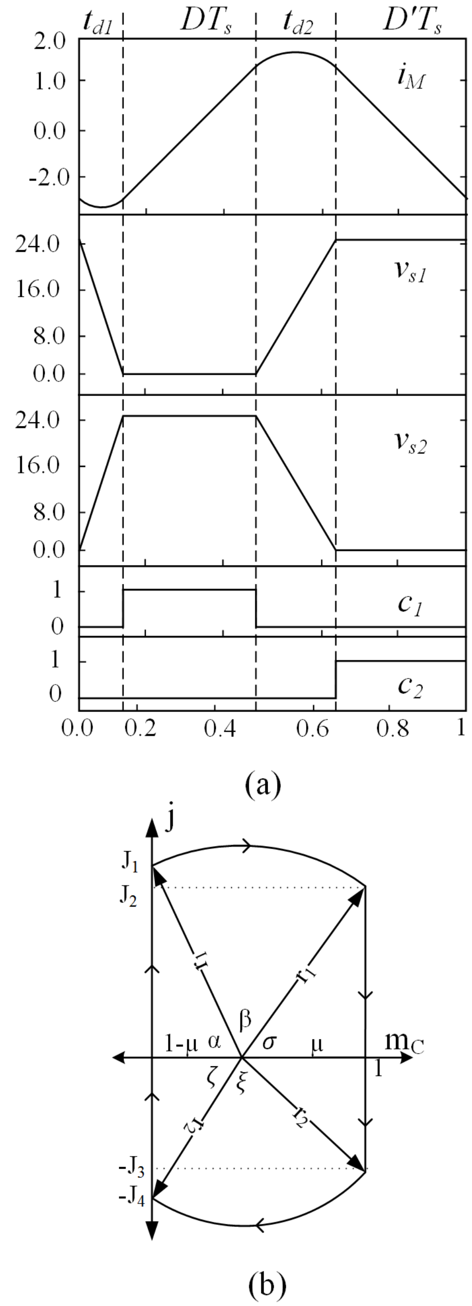


Figure 3.3: (a) Typical steady-state waveforms, and (b) state-plane trajectory in the ZVS-QSW Ćuk converter.

$$J_3 = \sqrt{1 - 2\mu + J_4^2}\,, \tag{3.8}$$

$$J_2 = \sigma\mu - J_3\,, \tag{3.9}$$

$$J_1 = \sqrt{J_2^2 - 1 + 2\mu}\,, \tag{3.10}$$

$$\beta = tan^{-1}(\frac{1-\mu}{J_1}) + tan^{-1}(\frac{\mu}{J_2})\,, \tag{3.11}$$

$$\xi = tan^{-1}(\frac{1-\mu}{J_4}) + tan^{-1}(\frac{\mu}{J_3})\,, \tag{3.12}$$

$$\alpha = \frac{J_1}{1-\mu}\,, \tag{3.13}$$

$$\zeta = \frac{J_4}{1-\mu}\,, \tag{3.14}$$

$$\theta = \alpha + \xi\,, \tag{3.15}$$

$$F_s = \frac{2\pi}{\alpha + \beta + \sigma + \zeta + \xi}\,, \tag{3.16}$$

$$f_{sw} = \frac{F_s}{f_r}\,, \tag{3.17}$$

where $f_r = \frac{w_r}{2\pi}$.

The normalized output current is then given by:

$$J_{OUT} = \frac{1}{1+M}\frac{F_s}{4\pi}[\theta(J_1 - J_4) + \sigma(J_2 - J_3)]\,. \tag{3.18}$$

State-plane equations are solved numerically to select the magnetizing inductance L_M and the switching frequency f_{sw}.

3.2 Planar Integrated-Magnetics Design

The integrated magnetics structure consists of a transformer in which the primary and secondary windings are wound on the middle core leg, while the input and output filter inductors are wound on the outer legs of an EI-core, as shown in Fig. 3.4. As discussed in [48], the leakage inductance can be reduced significantly by using a low profile (planar) transformer. The transformer leakage inductance can be further reduced by interleaving the primary and secondary windings [2].

3.2.1 Transformer design

The transformer turns ratio is 1 : 1 and the magnetizing inductance L_M is selected based on the ZVS requirements, as described in Section 3.1.

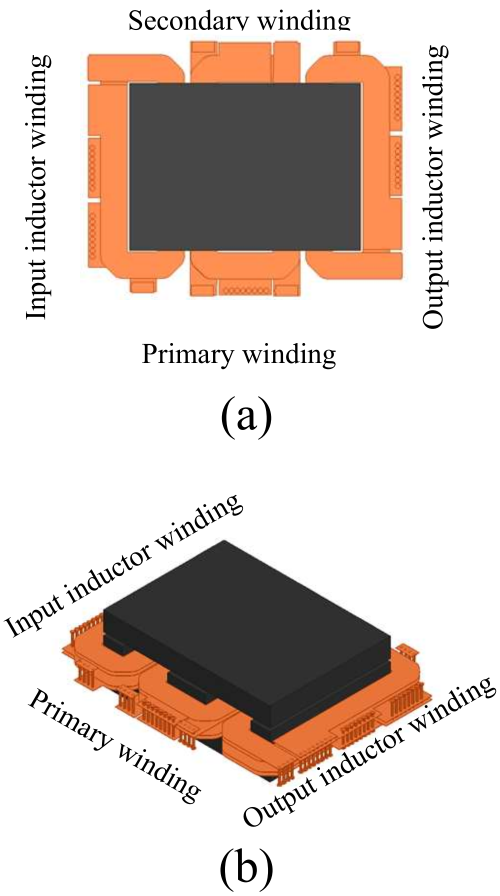


Figure 3.4: Planar integrated magnetics structure: (a) top-view and (b) side view.

Table 3.1: Core and winding losses for various core geometries using Ferroxcube 3F46 material.

Core	Core loss [W]	Winding loss [W]	Total loss [W]	N
EQ13	0.75	3.75	4.5	4
E/18/4/10	0.55	1.62	2.17	3
E/22/6/16	0.6	1.25	1.85	2

Due to the non-sinusoidal nature of the transformer voltages in the Ćuk converter, the improved generalized Steinmetz equation (iGSE) method [49] is used to calculate the core losses. The transformer primary and secondary currents are non-sinusoidal, which complicates calculation of ac losses in the windings. A 3D FEM tool (Ansys HFSS) is used to simulate the planar structure for the fundamental and a number of current harmonics n. The transformer Z-matrix can then be extracted, and the transformer winding losses are then calculated using [50]:

$$P_{winding} = \sum_{1}^{n} \frac{1}{2} R_{11_n} i_{p_n} i_{s_n}^* + \frac{1}{2} R_{22_n} i_{s_n} i_{s_n}^* + \frac{1}{2} R_{12_n} \left(i_{p_n} i_{s_n}^* + i_{p_n}^* i_{s_n} \right), \tag{3.19}$$

where * indicates complex conjugate, R_{11} and R_{22} are the transformer primary and secondary winding resistances, respectively, and R_{12} is a mutual resistance due to eddy current losses.

The design optimization consists of selecting a core, the number of turns, the number of PCB layers, and the geometry of the PCB copper traces. A number of cores with different geometries are examined. The optimization results for a selection of cores are listed in Table. 3.1. The E/22/6/16 core has the lowest total loss, and is selected for the design. The number of turns for the transformer primary and secondary windings is selected as $N = 2$. The width and thickness of the transformer windings are selected to minimize the winding loss and still allow for the input and output inductor windings on the outer legs of the core (Fig. 3.4). The final optimized transformer windings have 2 mm width and a thickness of 0.034 mm (1 oz copper).

3.2.2 Ripple steering in input and output inductors

Once the transformer is designed, the input and output filter inductors are designed to minimize input and output current ripples. Assuming the same number of turns for the input and

Table 3.2: Specifications and parameters of the ZVS Ćuk converter using planar integrated magnetics.

Switching frequency f_{sw}	1.8 – 2.4 MHz
Input voltage V_{IN}	12 V nominal, 5 – 45 V
Output voltage V_{OUT}	3 V to 50 V
Output current I_{OUT}	0.5 A
Output capacitor C_{out}	125 nF
Transistors Q_1 to Q_4	Fairchild FDMS86105, EPC2007C
Energy-transfer capacitors C_{b1}, C_{b2}	4.5 μF
Input and output inductor L_{IN} and L_{OUT} windings	4 turns
Transformer primary and secondary winding	2 turns
Magnetic core	Ferroxcube E/22/10/16 core, 3F46 material
Magnetizing inductance L_M	680 nH
Leakage inductance L_l	22 nH
Gate-drivers	Texas instruments UCC27511A-Q1 and LM5114

output inductors ($N_1 = N_2$), and the same air-gap in all three core legs, an equivalent magnetic circuit model is shown in Fig. 3.5. Flux $\phi_1 = \phi_2 = \frac{1}{2}\phi$ is deduced by solving the magnetic circuit model under ideal zero-ripple conditions [12]. The air gap length x, is given by

$$x = \frac{\mu_o S N^2}{L_M}, \tag{3.20}$$

where S is the cross section area of the core. The leakage length l is defined as the length of a virtual leg representing the transformer leakage inductance [16], and is expressed by:

$$l = \frac{\mu_o S N^2}{L_l}, \tag{3.21}$$

where L_l is the transformer leakage inductance extracted from 3-D FEM simulation, $L_l = 22$ nH. The number of turns in the input and output filter inductors, N_1 and N_2, are given by

$$N_1 = N_2 = 2N(\frac{x}{l} + 1), \tag{3.22}$$

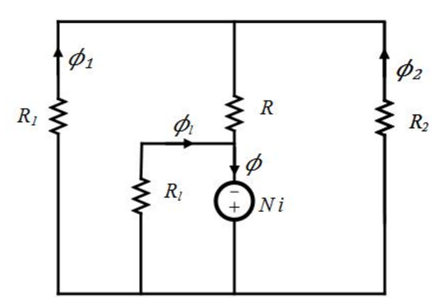


Figure 3.5: Magnetics circuit model of the integrated magnetics.

The number of turns obtained from (3.22), $N_1 = N_2 = 4.12$, is rounded to the nearest integer value $N_1 = N_2 = 4$. It should be noted that it is possible to select the magnetizing inductance such that (3.22) results in an integer value, in order to minimize the input and output current ripples. This choice, however, may result in higher losses because of the loss of zero voltage switching. For example, if the magnetizing inductance were selected so that (3.22) results in $N_1 = N_2 = 4$, this magnetizing inductance would be higher than the optimum value calculated to meet ZVS conditions, as described in Section 3.1. If the magnetizing inductance were selected so that (3.22) results in

$N_1 = N_2 = 5$, this magnetizing inductance would be smaller than the optimum value, which would result in ZVS operation but at the expense of larger current ripple, and larger conduction losses.

In the experimental prototypes described in Section 4.2, the magnetizing inductance is optimized for efficiency, resulting in acceptable increase in input and output current ripples due to the rounding of the number of turns. To ensure that the LED current ripple meets the requirements (less than 10%), a small filter capacitor is added across the output [2],

$$C_{out} = \frac{\Delta I \; T_s}{8 \; \Delta V}\,, \tag{3.23}$$

where ΔI is the inductor current ripple, ΔV is the allowed capacitor voltage ripple and T_s is the switching period.

3.2.3 Simulation results

The resultant integrated magnetics structure is verified using Ansys Q3D FEM tools and the Spice sub-circuit of the integrated magnetics structure is extracted. The sub-circuit includes self inductance, coupling coefficients, self resistance (AC loss model) and mutual resistances (proximity loss model) for the integrated magnetics windings. The Spice netlist is provided in appendix A. The value of the Q3D-extracted parameters are only valid for the applied excitation frequency. The value of the self-inductance and mutual inductances do not vary significantly in the presence of switching frequency harmonics. However, the self and mutual resistances do vary with frequency. In order to accurately predict winding losses, the self and mutual resistances can be obtained for a range of frequencies using Ansys HFSS-based analysis as given in (3.19).

The integrated magnetics Spice model is used to simulate the ZVS planar integrated magnetics structure as shown in Fig. 3.6. A Resistor R_c is placed in parallel with the primary and secondary side of the transformer to model the core losses. The switching node voltage waveforms v_{s1} and v_{s2} are shown in Fig. 3.7 for $V_{IN} = 12$ V, $I_{OUT} = 0.5$ A, $V_{OUT} = 40$ V ($N = 12$) and $f_{sw} = 2.2$ MHz, indicating minimal ringing and the smooth transitions characteristic of ZVS operation.

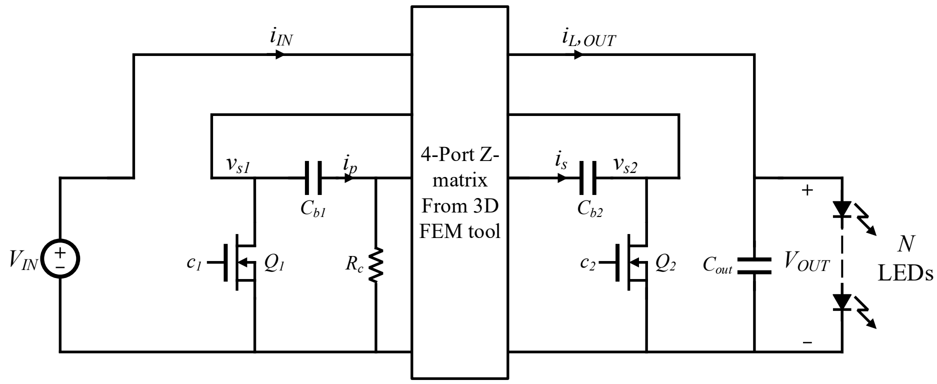


Figure 3.6: Simulation setup for the ZVS planar integrated magnetics Ćuk converter.

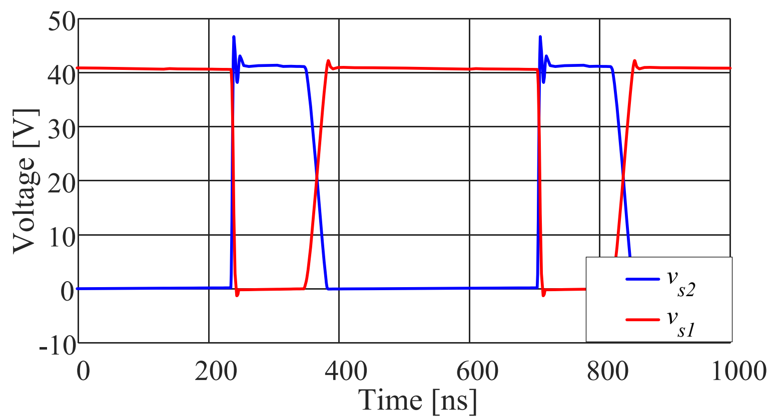


Figure 3.7: Simulated switching node voltage waveforms v_{s1} and v_{s2} of the ZVS planar integrated magnetics Ćuk converter for $V_{IN} = 12$ V, $I_{OUT} = 0.5$ A, $V_{OUT} = 40$ V ($N = 12$) and $f_{sw} = 2.2$ MHz.

3.3 Experimental Results

Using the analysis and design approach presented in Sections 3.1 and 3.2, prototypes of the Ćuk converter have been designed, built and tested, using Silicon MOSFET or GaN transistors. The specifications and parameters are listed in Table 5.1, and a photograph of the prototype with Silicon MOSFETs is shown in Fig. 6.5.

Measured primary-side switch-node voltage v_{s1} and secondary-side switch-node voltage v_{s2}, aligned with input control signals c_1 and c_2 are shown in Fig. 3.9, for an input voltage of 12 V, output

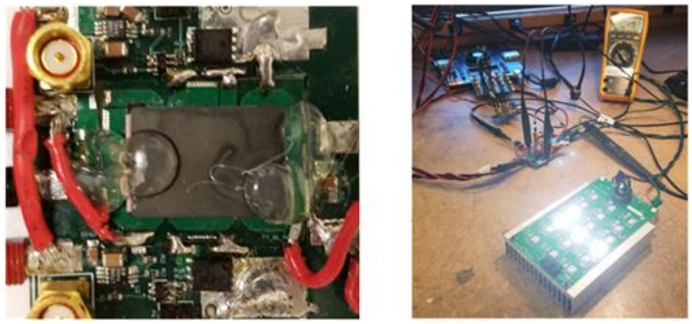
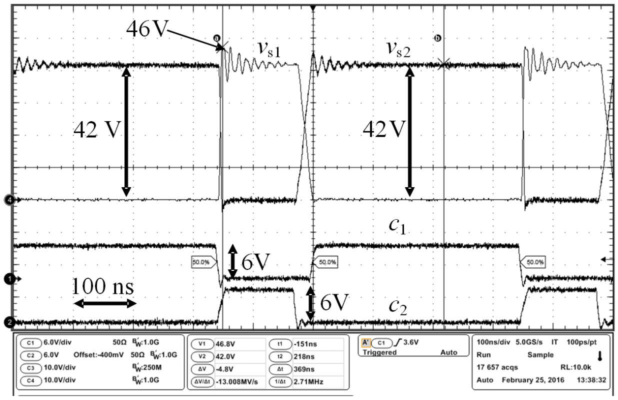


Figure 3.8: Planar integrated magnetics ZVS Ćuk converter prototype, and a test bench with LED's as the load.

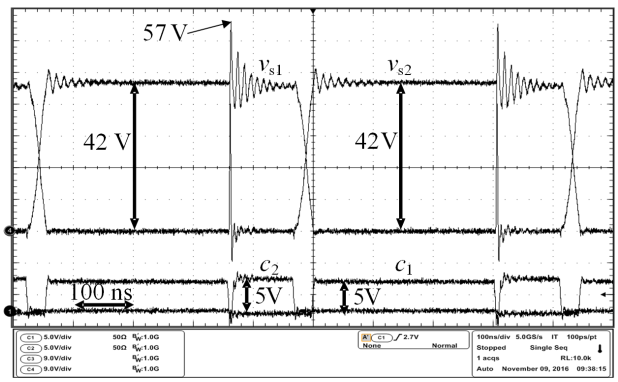
voltage of 30 V and output current of 0.5 A. The results are shown for the Silicon prototype using Fairchild FDMS86105 MOSFET transistors in Fig. 3.9(a), and for the prototype using EPC2007C GaN transistors in Fig. 3.9(b). Smooth transitions in v_{s1} and v_{s2} indicate ZVS commutations of the transistors in both prototypes. Small ringing in the switch-node voltages is indicative of low transformer leakage inductance. A somewhat larger ringing is observed in the GaN prototype, which is due to the smaller device output capacitances compared to the prototype with Silicon devices.

Measured output current and switch-node voltage v_{s1} are shown in Fig. 3.10 aligned with input control signals c_1 and c_2 for an input voltage of 12 V, output voltage of 15 V and output current of 0.5 A. The output current exhibits relatively small but not zero current ripple, which can be attributed to the rounding of the number of turns $N_1 = N_2$ in (3.22), capacitor voltage ripples, and other causes of residual current ripples [16]. A small output filter capacitor $C_{OUT} = 125$ nF is placed across the output. In this case, $L_M = 680$ nH, and the Silicon converter measured peak efficiency is 92.3%.

Fig. 3.11 shows the output current ripples for the case when the magnetizing inductance is reduced to $L_M = 460$ nH so that $N_1 = N_2 = 5$ more closely meet the zero-ripple condition (3.22). The input and output current ripples are reduced, but additional losses and larger ringing are observed in the switching node voltages due to the increased magnetizing current ripple and increased energy in the leakage inductance. In this case, the measured peak efficiency of the Silicon



(a)



(b)

Figure 3.9: Switch-node voltages v_{s1} and v_{s2}, and transistor control signals c_1 and c_2 for $V_{IN} = 12$ V, $V_{OUT} = 30$ V, $I_{OUT} = 0.5$ A, $L_M = 680$ nH and $N_1 = N_2 = 4$ using (a) Silicon MOSFETs, and (b) GaN transistors.

prototype is 89.3%.

Because of the higher efficiency, and because the resulting input and output ripples can be filtered using small filter capacitors, the design with optimized $L_M = 680$ nH and the inductor turns rounded to $N_1 = N_2 = 4$ is selected. The rest of the section presents experimental results for this design choice.

Experimentally measured efficiency using Silicon MOSFETs (Fairchild FDMS86105), or GaN transistors (EPC2007C) are shown in Fig. 3.12 for $V_{IN} = 12$ V, $V_{OUT} = 3$ V-to-35 V, $I_{OUT} = 0.5$ A, with both prototypes operated at constant switching frequency $f_s = 2.2$ MHz. Model based loss breakdowns for the two prototypes are shown in Fig. 3.13 under the same operating condition

(V_{IN} = 12 V, V_{OUT} = 35 V, I_{OUT} = 0.5 A and f_s = 2.2 MHz). One may note how conduction losses in the two prototypes are nearly the same, while the switching and gate-drive losses are smaller in the GaN prototype. Furthermore, with the GaN transistors, which have lower output capacitances, ZVS operation is extended over a wider range of output voltages, which results in more significant efficiency gains at low and high output voltages, as shown in Fig. 3.12. As noted in chapter 3, these prototypes can be further optimized to achieve ZVS over wide input voltage ranges as well.

As the number of LED's at the output changes, the switching frequency f_{sw} can be adjusted so that the converter can achieve ZVS over a wider range of output voltages. For a given output voltage, an optimum switching frequency can be found to minimize the losses. Model predicted and measured efficiencies are shown for the prototype using Silicon MOSFETs (FDMS86105) in Fig. 3.14(a), and for the prototype using GaN transistors (EPC2007C) in Fig. 3.14(b), as functions of the output voltage (which corresponds to different numbers of LEDs). The converter switching frequency f_{sw} varies from 1.8 MHz-to-2.4 MHz. It can be seen that the prototype with Silicon MOSFETs (FDMS86105) achieves a peak power-stage efficiency of 92.9%, while the converter using GaN transistors (EPC2007C) achieves a peak power-stage efficiency of 93.5% and greater

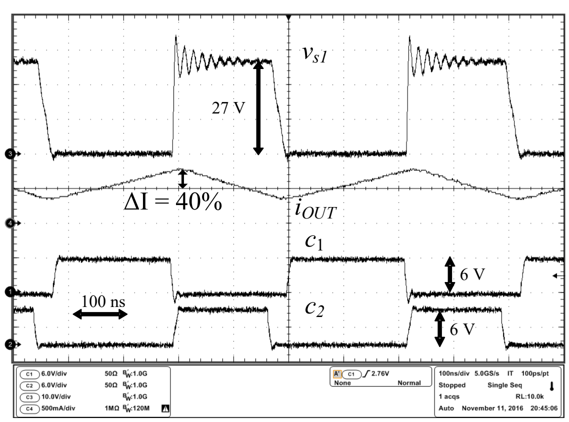


Figure 3.10: Switch-node voltage v_{s1}, output current i_{OUT}, and transistor control signals c_1 and c_2 for V_{IN} = 12 V, V_{OUT} = 15 V, I_{OUT} = 0.5 A, $N_1 = N_2 = 4$, L_M = 680 nH and η = 92.9% in the prototype with Silicon MOSFETs.

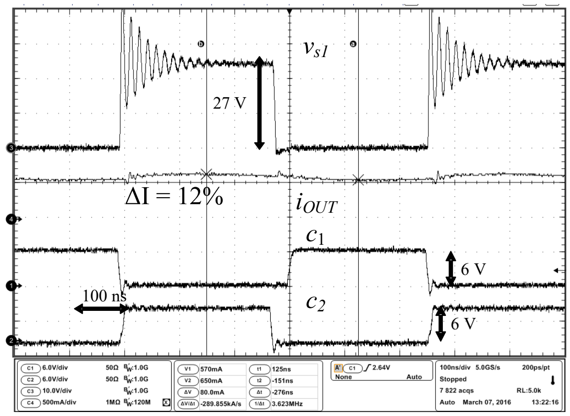


Figure 3.11: Switch-node voltage v_{s1}, output current i_{OUT}, and transistor control signals c_1 and c_2 for $V_{IN} = 12$ V, $V_{OUT} = 15$ V, $I_{OUT} = 0.5$ A, $N_1 = N_2 = 5$, $L_M = 460$ nH and $\eta = 89.3\%$, in the prototype with Silicon MOSFETs.

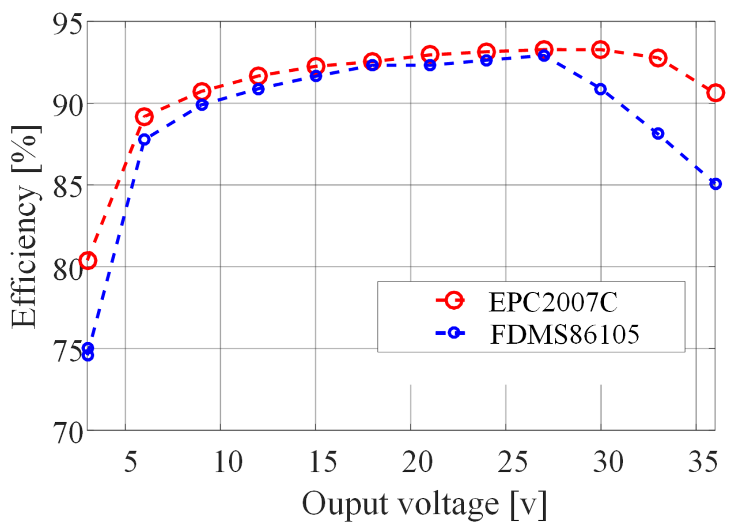


Figure 3.12: Experimentally measured efficiencies for $V_{IN} = 12$ V, $I_{OUT} = 0.5$ A in the prototypes with Silicon MOSFETs (FDMS86105) and GaN transistors (EPC2007C) operated at $f_{sw} = 2.2$ MHz.

than 86% efficiency over the full 3-48 V output voltage range. Both Silicon and GaN prototypes maintain greater than 90% efficiency over a wide range of output voltages (12 V-to-42 V for the Silicon prototype, and 9 V-to-45 V for the GaN prototype). These efficiency results are marked improvements over the design with non-planar wound integrated magnetics and active snubbers where the converter peak efficiency of about 85% was reported [51].

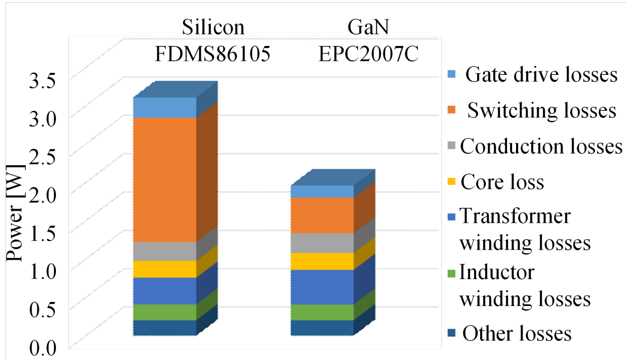


Figure 3.13: Loss break down for the prototypes using Silicon MOSFETs (FDMS86105) or GaN transistors (EPC2007C) for $V_{IN} = 12$ V, $V_{OUT} = 36$ V, $I_{OUT} = 0.5$ A and $f_{sw} = 2.2$ MHz.

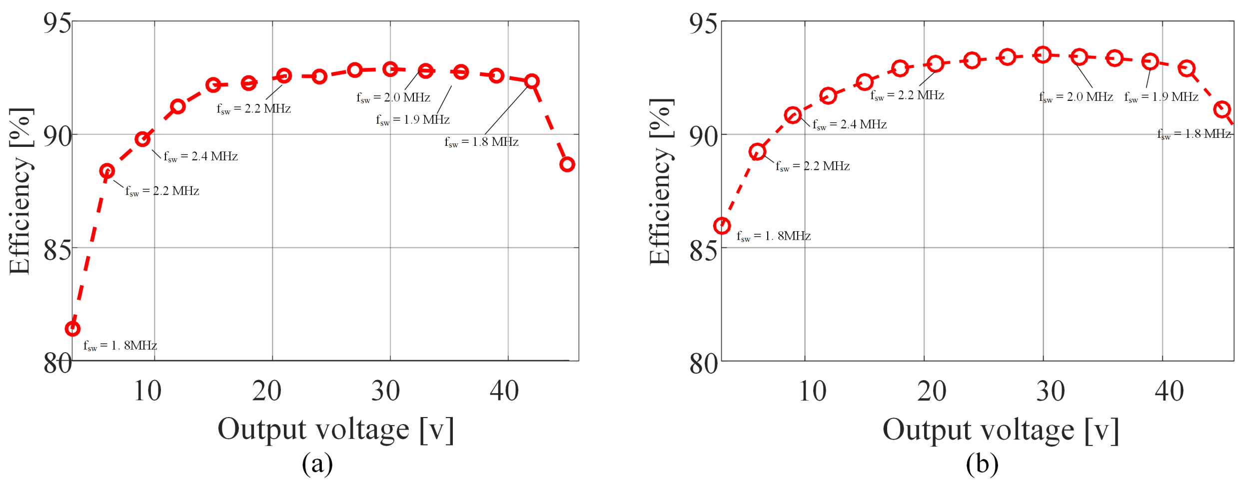


Figure 3.14: Experimentally measured efficiency of the Ćuk converter prototype, for input voltage 12 V, output voltage 3 V-to-46 V, output current 0.5 A and optimized f_{sw} (1.8 MHz-to-2.4 MHz, using (a) the Silicon MOSFETs (FDMS86105) and (b) the GaN transistors (EPC2007C).

Table. 3.3 compares the prototypes in this chapter to similar automotive LED drivers reported earlier [3, 4, 8, 51].

Table 3.3: Efficiency and switching comparison for conventional LED drivers and this work.

Ref.	Peak efficiency	f_{sw}(max)	Output power
[3]	92%	120 KHz	30 W
[4]	89.7%	500 KHz	40 W
[8]	90%	350 KHz	40 W
Prototype using active-clamp (ch. 2)	85%	1.8 MHz	30 W
Prototype using Silicon MOSFETs	**92.9%**	**2.4 MHz**	30 W
Prototype using GaN transistors	**93.5%**	**2.4 MHz**	30 W

3.4 Summary

This chapter presents a high-frequency zero voltage switching (ZVS) Ćuk converter for automotive LED driver applications using planar integrated magnetics. The planar magnetics structure is optimized using a combination of analytical and numerical FEM tools to minimize losses, leakage inductance, and input and output current ripples. Low leakage inductance eliminates the need for passive or active snubbers, while the magnetizing inductance and switching frequency are selected to achieve zero voltage switching over wide range of output voltages. Experimental prototypes operate at switching frequencies between 1.8 MHz and 2.4 MHz (above AM band) over an output voltage range of 3 V to 50 V while supplying a constant 0.5 A output current to a string of 1-to-15 LEDs. Using Silicon MOSFETs, the prototype achieves a peak efficiency of 92.9%. The same prototype, but with Silicon MOSFETs replaced by GaN devices, achieves 93.5% peak efficiency, and up to 5.5% efficiency improvement over the output voltage range. Both Silicon and GaN prototypes maintain greater than 90% efficiency over a wide range of output voltages (12 V-to-42 V for the Silicon prototype, and 9 V-to-45 V for the GaN prototype).

CHAPTER 4

Closed-Loop Control and High-Resolution PWM Dimming in a Planar Integrated Magnetics Ćuk Converter

Contents

Modern automotive LED drivers have two major control requirements: precise regulation of the LED (output) current, and high-resolution dimming in order to vary the LEDs' light intensity without adverse optical effects such as flicker. The dimming functionality is typically implemented using pulse-width modulated (PWM) dimming, in which the converter is turned on and off at frequencies up to 1 kHz. To achieve high-resolution PWM dimming, the converter must be able to quickly turn on or off the output current. The integrated magnetics Ćuk converter presented in this thesis is well suited for high-resolution PWM dimming, since it requires a very small output filter capacitance, resulting in fast transient response capabilities. To better appreciate this advantage, consider the planar integrated magnetics Ćuk converter shown in Fig. 3.1 of Chapter 3.

State-space equations of the integrated magnetics structure are solved under the zero-ripple condition to obtain the effective inductances looking into the input and output inductor ports which can be expressed, respectively, as:

$$L_{in,eff} = -\frac{L_{14}^2 L_{33} + 2L_{14}L_{13}L_{34} + L_{11}L_{34}^2 + L_{13}^2 L_{44} - L_{11}L_{33}L_{44}}{-L_{14}^2 + L_{14}L_{13} + L_{11}L_{34} - L_{14}L_{34} + L_{11}L_{44} - L_{13}L_{44}}, \tag{4.1}$$

$$L_{out,eff} = -\frac{L_{14}^2 L_{33} + 2L_{14}L_{13}L_{34} + L_{11}L_{34}^2 + L_{13}^2 L_{44} - L_{11}L_{33}L_{44}}{L_{14}L_{13} - L_{13}^2 + L_{11}L_{33} - L_{14}L_{33} + L_{11}L_{34} - L_{13}L_{34}}, \tag{4.2}$$

where, L_{11}, L_{22}, L_{33} and L_{44} are the self inductances of the transformer primary, secondary, input filter inductor, and output filter inductor windings, respectively, and L_{ij} is the mutual inductance between windings i and j. The effective inductances given by (4.1) and (4.2) are significantly larger than the self-inductances of the input and output inductors. For instance, for the integrated magnetics Ćuk converter prototype presented in the previous chapter, the 2 μH input inductor appears effectively as a 4.58 μH inductor, while the 2.8 μH output inductor appears effectively as a 7.56 μH inductor. The ripple in the input and output currents can be expressed in terms of the effective input and output inductances as:

$$\Delta I_{in} = \frac{V_{IN} D}{2L_{in,eff} f_{sw}}, \tag{4.3}$$

$$\Delta I_{out} = \frac{V_{OUT} D'}{2L_{out,eff} f_{sw}}, \tag{4.4}$$

It can be seen from (4.3) and (4.4) that since the effective input and output inductances are large, the input and output currents have small ripples. Therefore, the integrated magnetics Ćuk converter requires very small input and output filter capacitances. In particular, the small output capacitances allow the output voltage and current of the converter to be changed at fast rates, enabling the converter to be turned on and off very quickly, as required in high-resolution PWM dimming. The following section presents a new control architecture for the integrated magnetics Ćuk converter that leverages this favorable property to achieve ultra-fast turn-off and turn-on dynamics, while precisely regulating the output current.

4.1 Control Architecture

Automotive LED drivers, like many other converter systems, invariably require feedback. In a typical automotive LED driver application, the input voltage V_{IN} varies from 4.5 V (during cold start) to more than 45 V (during load dump), while the output voltage ranges from 3 V to 60 V (depending on the number of LEDs, N = 1-18).

The feedback controller must precisely regulate the LEDs' current (with less than 10% ripple) over these wide voltage ranges. Furthermore, the output current of an automotive LED driver is typically close to the LEDs' current rating. As a result, a small overshoot in the output current may cause the LEDs to fail. Therefore, extra care needs to be taken to prevent transient overshoots in the output current. As stated earlier, PWM dimming is employed to control the LED brightness: the LEDs are turned on and off with a dimming frequency f_{dim} and a dimming dutycycle D_{dim}. The dimming frequency is selected above noticeable frequencies ($>$ 200 Hz) to avoid flicker, extending up to around 1 kHz.

In this chapter, a closed-loop control architecture is presented for the integrated magnetics Ćuk converter, which enables the converter to achieve the aforementioned regulation and dimming requirements. In order to develop this control architecture, the small-signal dynamics of the converter need to be analyzed. Similar to its conventional counterpart, the integrated magnetics Ćuk converter has non-minimum phase dynamics [52]. Furthermore, in a non-inverting Ćuk converter with a transformer, the magnetizing inductance adds additional conjugate poles and zeros to the converter's transfer functions [53]. The integrated magnetics Ćuk converter explored in this thesis is a sixth-order system. Therefore, developing a reliable and wide-bandwidth regulation scheme using conventional modeling approaches such as state-space averaging involves complicated mathematical expressions [54]. In the following sub-section, an approach is presented based on Spice simulations of converter averaged model, greatly simplifying the analysis of the small-signal dynamics of the integrated magnetics Ćuk converter and design of the control loop.

4.1.1 Small signal modeling of the integrated magnetics Ćuk converter

The small-signal dynamics of the integrated magnetics Ćuk converter are investigated using the averaged switch model [2]. In this model, a general two-switch network, shown in Fig. 4.1(a), is represented using dependent voltage and current sources with the duty cycle d as a control input, as shown in Fig. 4.1(b). The mathematical basis of this modeling approach can be found in [2].

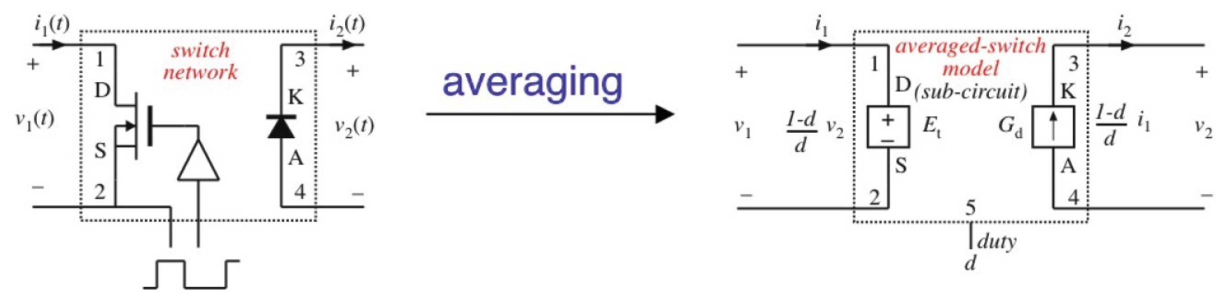


Figure 4.1: Averaged switch modeling (a) the general two-switch network and (b) averaged-switch sub-circuit. [2].

A Spice implementation of the averaged switched model is used to obtain the dynamics and, in particular, the duty-cycle-to-output-inductor-current transfer function of the integrated magnetics Ćuk converter, given by:

$$G_{id}(s) = \frac{i_{L,out}(s)}{d(s)} \tag{4.5}$$

It may be noted that since the converter has a very small output capacitor, the output inductor current is essentially equal to the LED current, and is hence utilized as the control parameter. An advantage of using the Spice-assisted averaged switch model is that the detailed Spice model of the planar integrated magnetics structure presented in chapter. 3 can be directly utilized, resulting in accurate average model of the system. The simulation setup is shown in Fig. 4.2. The converter's switch network (comprising transistors Q_1 and Q_2) is replaced by the averaged switch model, and the magnetic components (L_{in}, L_{out} and the transformer) are represented by the Spice model of the integrated magnetics structure obtained from 3D FEM analysis. An additional resistor R_c is introduced in parallel with the transformer's input port to model its core loss. The value of this resistance depends on the converter's input and output voltages, and can be computed by applying the improved Generalized Steinmetz Equation (iGSE) over the operating range of the converter [55].

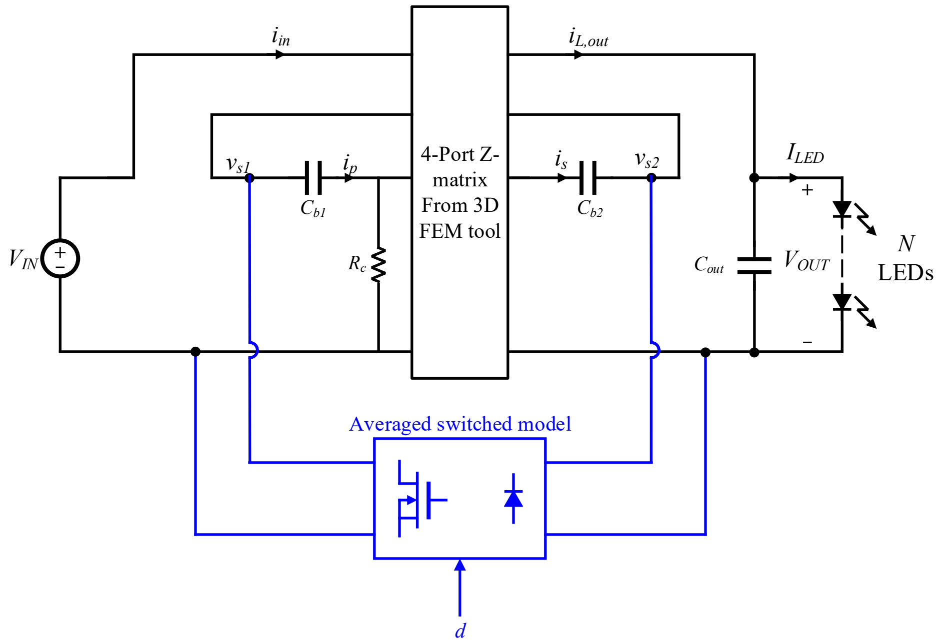


Figure 4.2: Spice averaged circuit model of the converter.

Using .AC simulation in the Spice environment, the converter's duty-cycle-to-output-inductor-current transfer function, as expressed in (4.5), is plotted, for $V_{IN} = 12$ V, $V_{OUT} = 3$ V-to-50 V ($N = 1$-to-12) and output current $I_{LED} = 0.5$A. The results are shown in Fig. 4.3. As can be seen from the magnitude plot, the transfer function consists of a single pole located around 10 kHz, multiple high-frequency poles and zeros due to the magnetizing inductance of the transformer [53], and a right-half plane zero at a very high frequency (> 200 kHz).

One may notice that the low frequency gain of the duty-cycle-to-output-inductor-current transfer function remains approximately constant regardless of changes in the output voltage. Since this approximate gain invariance is observed at a low frequency, it is not associated with the integrated magnetics structure, which predominantly modifies the higher-frequency dynamics of the converter. Therefore, to investigate this property of the transfer function analytically, the small signal model of a conventional Ćuk converter (with an ideal transformer and non-coupled inductors) is developed. The duty-cycle-to-output-inductor-current transfer function of this converter is given

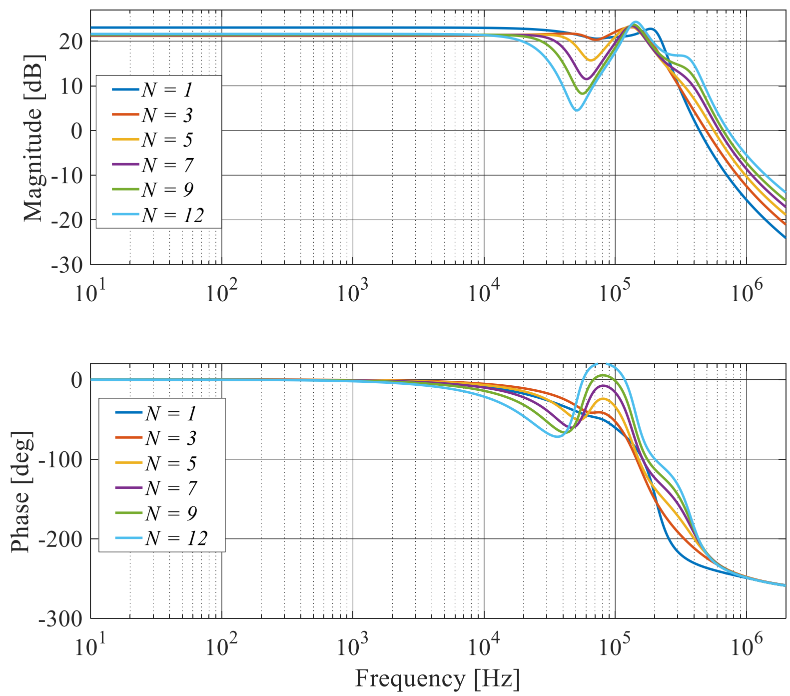


Figure 4.3: Duty-cycle to output inductor current transfer function $G_{id}(s) = \frac{i_{L,out}(s)}{d(s)}$ for V_{IN} = 12 V, V_{OUT} = 3 V-to-50 V (N = 1-to-12) and output current I_{LED} = 0.5A.

by:

$$G_{id}(s) = \frac{G_{id0}(1 - \frac{s}{Q_z w_z} + \frac{s^2}{w_z^2})}{(1 + \frac{s}{Q_p wp} + \frac{s^2}{w_p^2})(1 + \frac{s}{w_{p2}})}, \tag{4.6}$$

where the low frequency (DC) gain is:

$$G_{id0} = \frac{DD'V_c + D'^2 Vc}{D'^2 \frac{V_{OUT}}{I_{LED}}}, \tag{4.7}$$

and $V_c = V_{cb1} + V_{cb2} = V_{IN} + V_{OUT}$. Simplifying (4.7) results in:

$$G_{id,0} = \frac{I_{LED}}{DD'}\,. \tag{4.8}$$

A plot of this low-frequency gain versus duty cycle is shown in Fig. 4.4. It can be seen that as the duty cycle D varies from 20% to 80%, representing a corresponding variation in the converter's output voltage, the low frequency gain changes only by about 4 dB. The transfer function of the integrated magnetics Ćuk converter exhibits a similar low-frequency behavior.

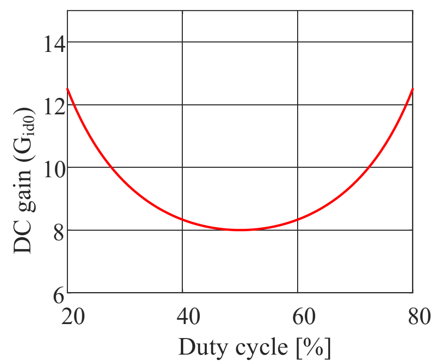


Figure 4.4: Low-frequency gain of the duty-cycle-to-output-inductor-current transfer function versus steady-state duty cycle D for a non-inverted Ćuk converter with ideal transformer and non-coupled inductors.

4.1.2 Compensator design and output current step response

Based on the Spice model presented in the previous section, a closed loop controller is developed to regulate the output current of the integrated magnetics Ćuk converter, as shown in Fig. 4.5. The output inductor current is sensed and compared with a current reference, and the error is processed by an integral compensator. The output of the compensator is fed into a pulse-width modulator (PWM), which provides the modulated duty cycles for the two transistors, Q_1 and Q_2. As can be seen from Fig. 4.5, a test signal source is inserted at the compensator output to measure the loop gain of the system. The integral compensator ensures that the output current reference is tracked accurately in steady state, and is designed such that the loop gain has a crossover frequency of 15 kHz, below the resonant poles and zeros of the open loop transfer function shown in Fig. 4.3, while providing a phase margin of $\phi = 57^o$ at the worst case operating point (V_{OUT}=50 V corresponding to number of LEDs $N = 12$), where the phase of the open loop transfer function is the lowest, as also shown in Fig. 4.3. Designing for this phase margin ensures a fast transient response with minimal overshoot in the LED current. Furthermore, as discussed in the previous section, since the low frequency gain of the open loop transfer function varies over a relatively narrow range in response to changes in the number of LEDs, the crossover frequency also remains approximately constant. The Spice-simulated loop gain is plotted for various numbers of LEDs in Fig. 4.6. The

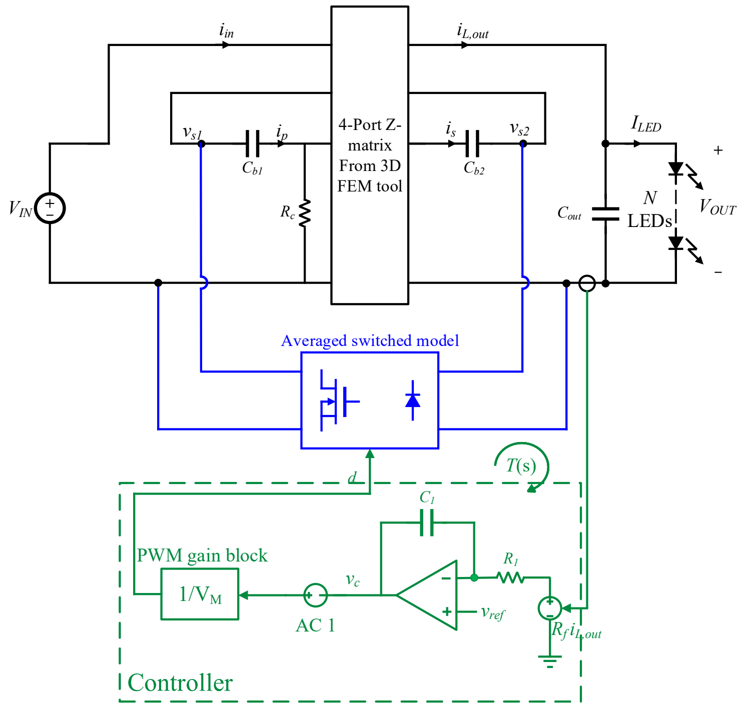


Figure 4.5: Setup to obtain the converter loop gain using Spice .AC simulation.

simulation setup of Fig. 4.5 is also used to perform a transient simulation and obtain the response of the converter's output (LED) current to a 100 mA positive step change in the current reference (from 400 mA to 500 mA), and a symmetric negative step change. This step response is shown for various numbers of LEDs (ranging from $N = 1$ to 12) in Fig. 4.7. It can be seen that for all values of N, the LED current exhibits fast rise and fall times and small overshoots, with the maximum overshoot (less than 10%) occurring for the maximum number of LEDs.

So far the averaged switch model has been used to analyze the converter dynamics. Next, the designed controller is tested using a Spice swithcing circuit model comprising detailed subcircuit models of the switching devices Q_1 and Q_2, as shown in Fig. 4.8. The transient step response using the detailed switch models for different operating points is shown in Fig. 4.9. As expected, switching ripple can now be observed in the LED current. The step response does not show any overshoot even in the worst case scenario ($N = 12$). This is due to the additional damping provided by the on-resistances of the transistors, which were neglected in the averaged switch model, but

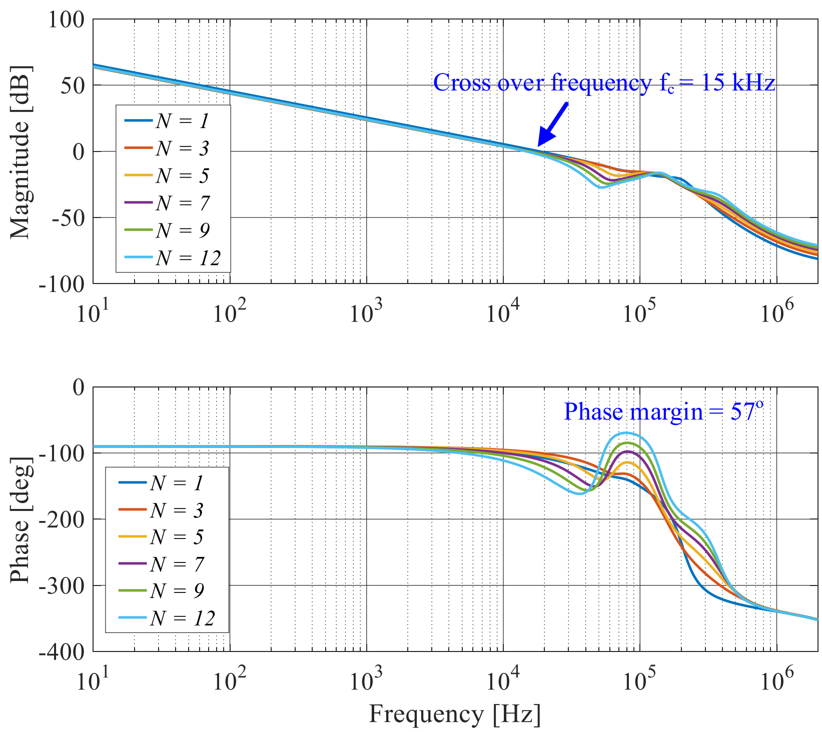


Figure 4.6: The converter loop gain for $V_{IN} = 12$ V, $V_{OUT} = 3$ V-to-50 V ($N = $ 1-to-12) and output current $I_{LED} = 0.5$A.

are now included in the transistor subcircuit definitions. Given this satisfactory transient response, the control architecture is extended to include PWM dimming functionality.

4.1.3 Pulse width modulated dimming

PWM dimming functionality is added to the feedback controller by introducing a new control input, PWM_in, as shown in Fig. 4.10. PWM_in is a pulsating signal with a duty cycle corresponding to the required LED brightness. The converter is turned on when this signal is high, and turned off when it is low. When the signal goes high, the gate drivers are enabled and the compensator reference input is set to $V_{ref} = R_f I_{ref}$. Conversely, when PWM_in goes low, the gate drivers are disabled and consequently the converter is shut down. At this time, the compensator reference input is set to zero and the converter's output voltage drops from its steady state

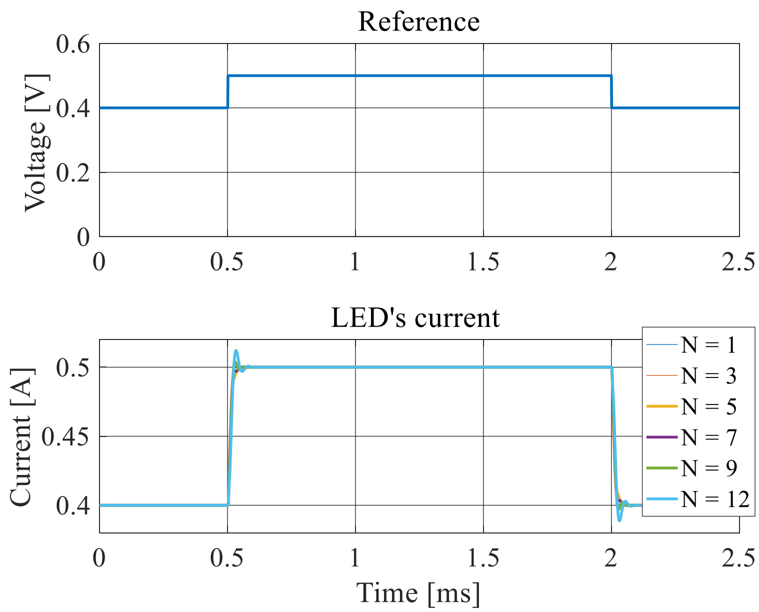


Figure 4.7: The LED's current response to a 100 mA (400 mA-to-500 mA) change in the reference current for V_{IN} = 12 V, V_{OUT} = 3 V-to-50 V (N = 1-to-12).

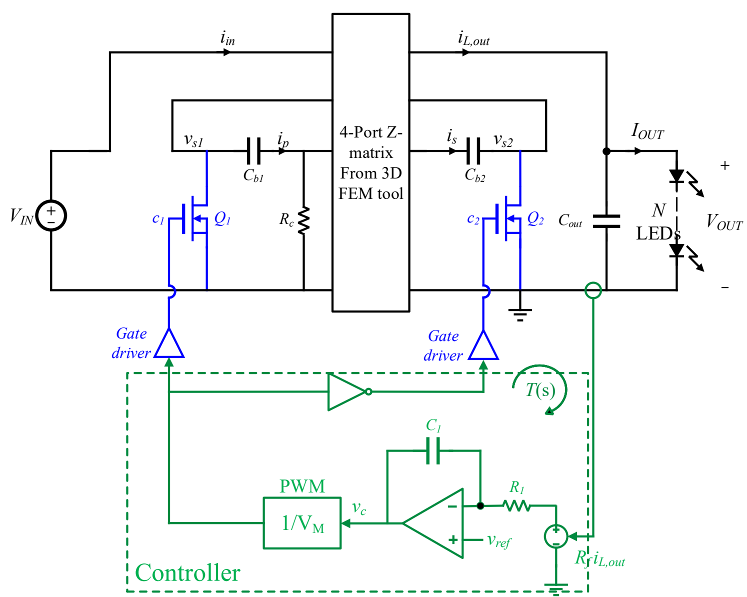


Figure 4.8: Simulation setup to perform transient step responses using a converter switching circuit model.

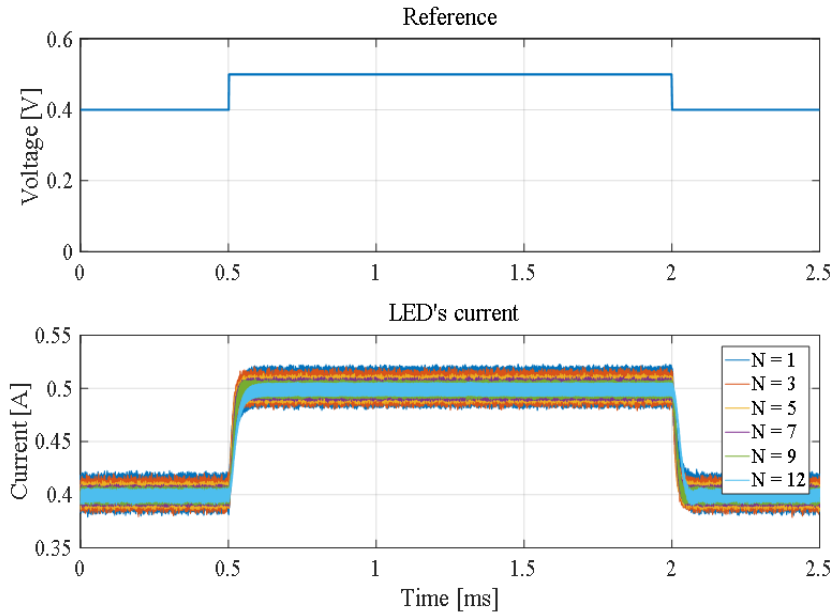


Figure 4.9: The LED's current response to a 100 mA (400 mA-to-500 mA) change in the reference current using the switching circuit model for V_{IN} = 12 V, V_{OUT} = 3 V-to-50 V (N = 1-to-12).

value. This prevents any overshoot from occurring in the LED current in the next PWM dimming cycle when the PWM_in signal goes high again. A transient Spice simulation is performed to verify this PWM dimming operation. The LED current time-aligned with the PWM_in signal is shown in Fig. 4.11. The dimming frequency f_{sw} is 1 kHz, and the dimming duty cycle D_{dim} is 50%. The waveform also demonstrates the start-up behavior of the converter. It can be seen that the converter turns on and off with no overshoots or undershoots in the LED current.

4.1.4 Turn-off strategy

A zoomed-in version of Fig. 4.11 is shown to illustrate the turn-off and the turn-on transitions of the LED current in Fig. 4.12 (a) and (b), respectively. The turn-off time of the LED current is longest when the number of LEDs N is maximum, with a fall time $t_{off} \approx 40$ μs. Similarly, the turn-on time is also longest for the maximum number of LEDs ($t_{on} \approx 40$ μs). In this sub-section, a turn-off strategy is proposed to shorten the turn-off time in order to enable higher-resolution PWM

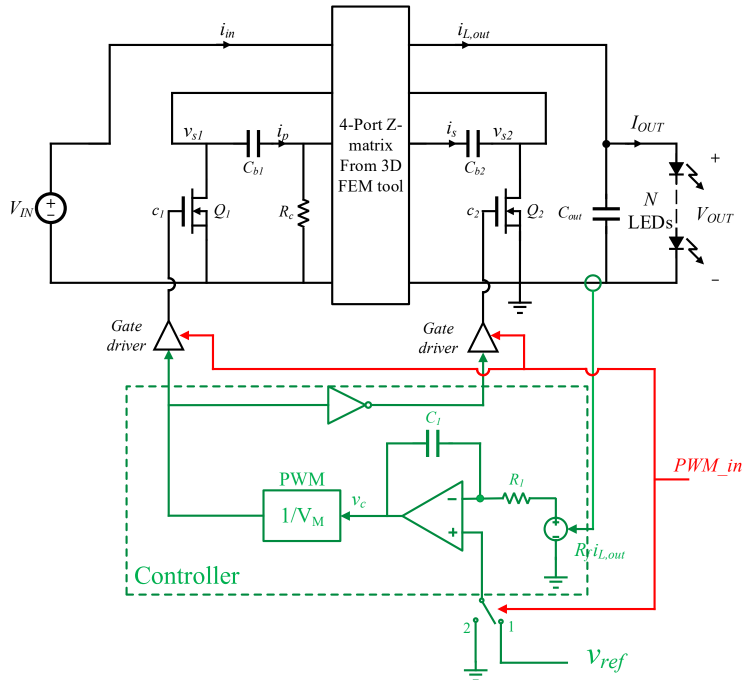


Figure 4.10: The simulation setup to perform PWM dimming.

dimming. This turn-off strategy is implemented in the following steps:

- During the on-time, the steady state value of the duty cycle command is sampled.
- When the PWM_in signal goes low, instead of completely turning off the converter, the converter duty cycle is set to a fraction (90%) of its steady state value to reverse the power flow and to actively discharge the converter's output capacitor. In response, the LED current decays at a fast rate, and reaches zero when the output voltage falls below the forward drop of the LED string.
- The converter is turned off when the LED current reaches zero.

A circuit implementation of the proposed turn-off strategy is shown in Fig. 4.13. In Fig. 4.14, the turn-off time transitions of the LED currents with and without the turn-off strategy are overlaid. It can be seen that with the proposed turn-off technique, the fall time of the LED current is improved by up to 82% (from 39.8μs to 6.6μs) for V_{IN} = 12 V and V_{OUT} = 40 V (N = 12).

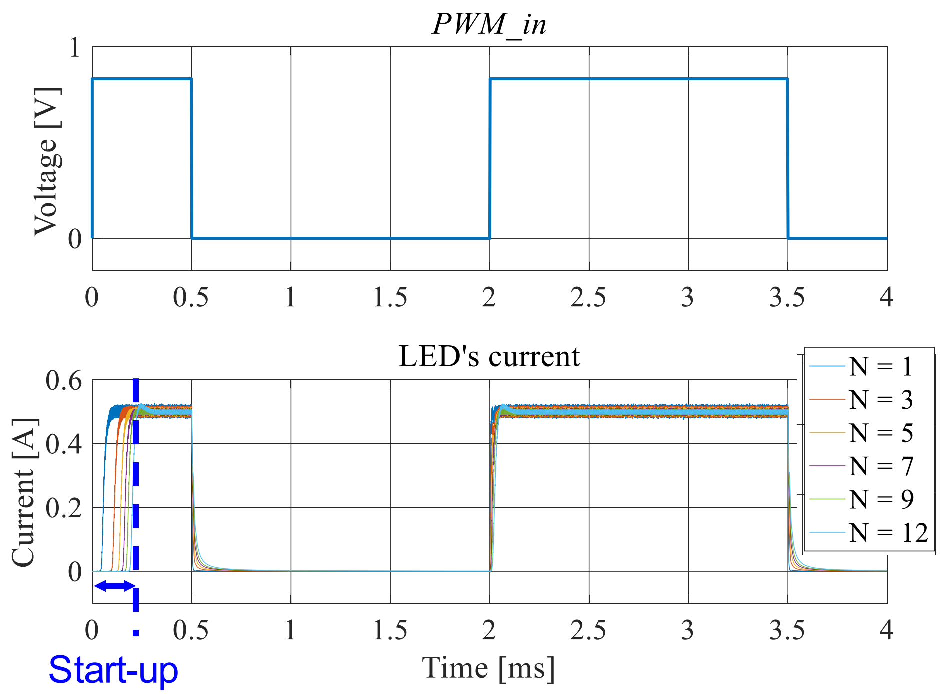


Figure 4.11: The LED's current response to a 100 mA (400 mA-to-500 mA) change in the reference current using the subcircuit models of the switching devices for V_{IN} = 12 V, V_{OUT} = 3 V-to-50 V (N = 1-to-12).

4.1.5 Turn-on strategy

In order to improve the turn-on transition time, the following procedure is proposed:

- When the converter is turned off, the output of the compensator is held to a value slightly below its steady state value, and the controller output v_c is disconnected from the controller switching-frquency modulator.
- When the PWM_in signal goes high, the converter is commanded with the steady-state value of the duty cycle.
- The LED current builds up at a fast rate, and when the current reaches the vicinity of its steady state value, the controller is re-connected to the modulator and current regulation loop is re-established.

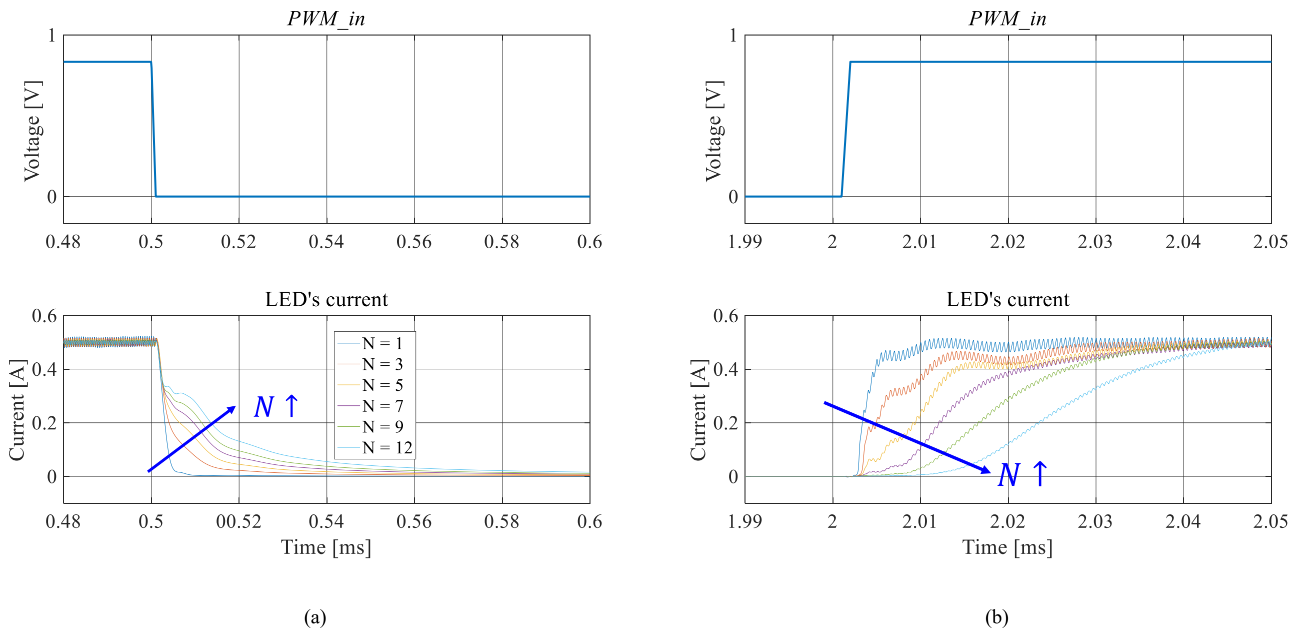


Figure 4.12: PWM dimming performance in LED's current (a) zoomed-in turn-off transition and (b) zoomed-in turn-on transition .

- When the LED current reaches its steady-state value, the duty cycle command v_c is sampled and stored to be used during turn-off.

Fig. 4.15 shows a circuit implementation of the turn-on strategy. Turn-on transitions of the LED current with and without the turn-on strategy are shown in Fig. 4.16. It can be seen in Fig. 4.16(a) that the turn-on time is improved by up to 43% (4.4 μs to 2.2 μs) for V_{IN} = 12 V, V_{OUT} = 3 V (N = 1). Figure Fig. 4.16(b) shows that the turn-on time is improved by up to 32% (38.0 μs to 25.6 μs) for V_{IN} = 12 V, V_{OUT} = 40 V (N = 12).

4.2 Experimental Results

A feedback controller with PWM dimming functionality utilizing the proposed compensator design and turn-off and turn-on strategies is digitally implemented and applied to the prototype 2-MHz ZVS planar integrated magnetics Ćuk converter presented in Chapter 3. The converter, along with the digital controller, is shown in Fig. 4.17. An Altera Stratix IV FPGA is used to provide high-

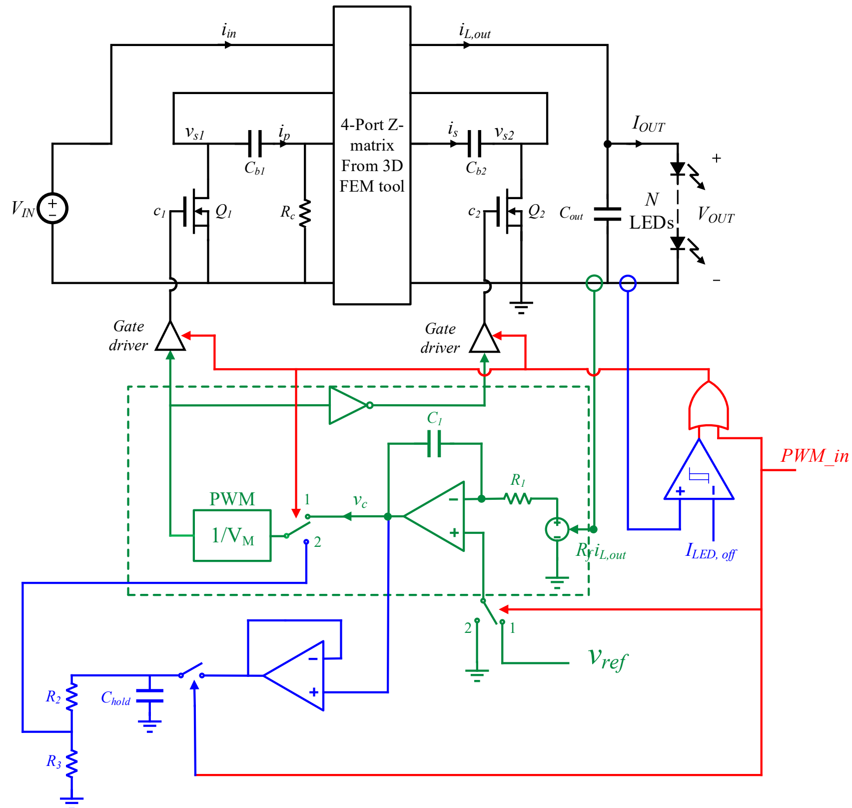


Figure 4.13: Implementation of the proposed turn-off strategy.

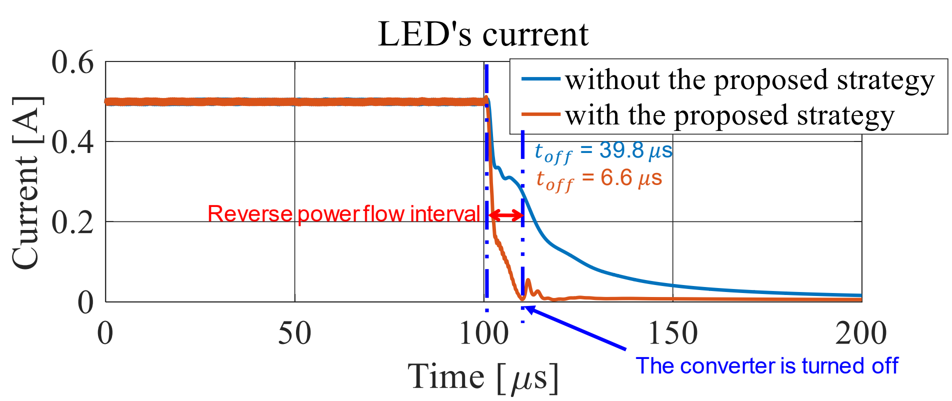


Figure 4.14: Turn-off transition with and without the proposed turn-off strategy.

resolution switching PWM duty cycle signals. The PWM dimming signal, PWM_in, is provided using a signal generator and the current reference I_{ref} is set thorough an interface command to the

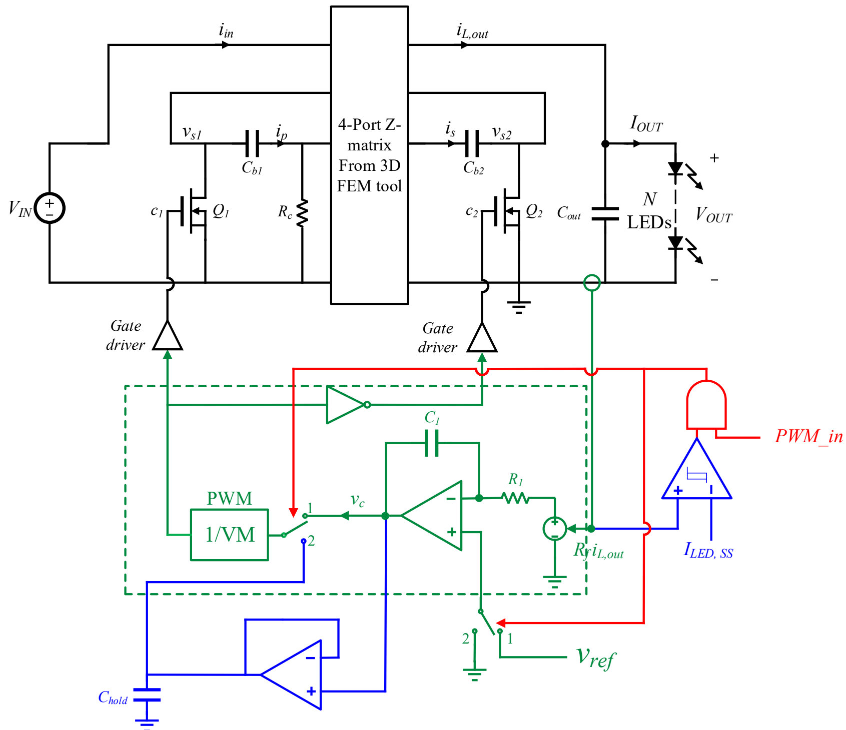


Figure 4.15: Implementation of the proposed turn-on strategy.

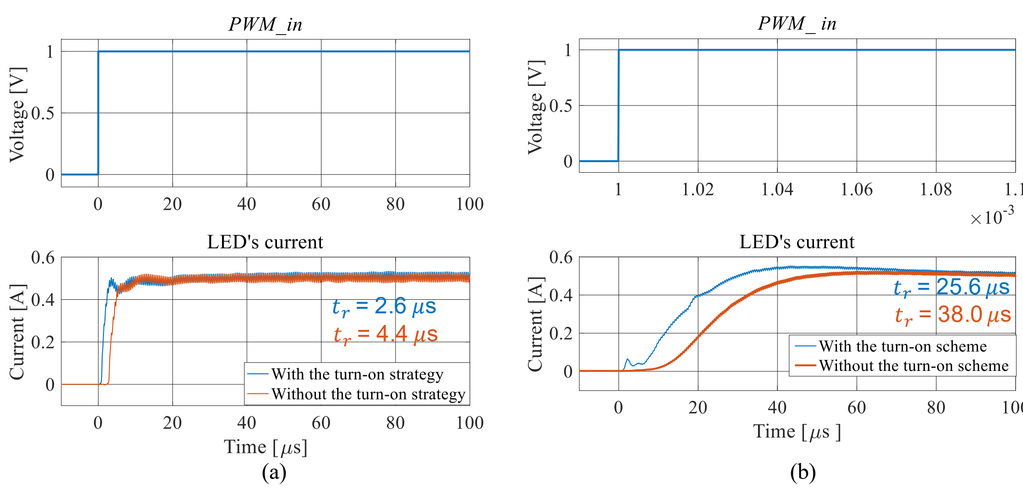


Figure 4.16: Tun-on transition with and without the proposed turn-on strategy for for V_{IN} = 12 V, I_{LED} = 0.5 A (a) V_{OUT} = 3 V (N = 1) and (b) V_{OUT} = 40 V (N = 12).

FPGA console. The output inductor current, $i_{L,out}$, is sensed using a sense resistor R_f. The sensed current is fed into a preamplifier and preconditioned using a low pass filter with a cut-off frequency

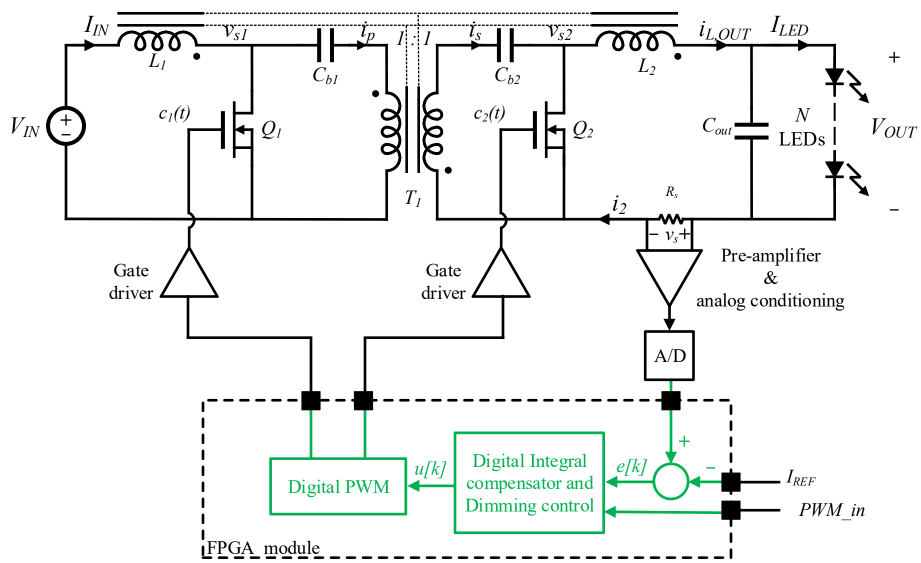


Figure 4.17: Block diagram of the proposed digitally controlled automotive LED driver based on the high-frequency ZVS integrated magnetics Ćuk converter.

set to 1 MHz to attenuate switching noise. A 12-bit differential ADC with a sampling frequency of 50 MHz is used to sample the sensed and filtered current. The sampled current is transfered into the FPGA using GPIO ports. The integral compensator is written in VHDL and implemented on the FPGA. Sample code is provided in Appendix B. A digital pulse-width modulator provides two separate control signals, which are used by the converter gate drivers to generate the two gate control signals $c_1(t)$ and $c_2(t)$, corresponding to the two transistors Q_1 and Q_2, respectively. The LED current response to a 250 mA step change in the reference current is measured and shown for $V_{IN} = 12$ V, $V_{OUT} = 40$ V ($N = 12$) in Fig. 4.18. It can be seen that the LED current rises without any overshoot. Measured PWM dimming performance for a dimming frequency $f_{dim} =$ 1 kHz and for two dimming duty cycles, $D_{dim} = 20\%$ and $D_{dim} = 80\%$, is shown in Fig. 4.19(a) and Fig. 4.19(b) respectively. Turn-on and turn-off transitions of the LED current are shown in Fig. 4.20 for two example operating points. It can be observed from Fig. 4.20(a) that at $V_{IN} = 12$ V and $V_{OUT} = 40$ V ($N = 11$), the LED current rises from 0 to 0.5 A in 35 μs. In Fig. 4.20(b), it is shown that at $V_{IN} = 12$ V and $V_{OUT} = 15$ V ($N = 5$), the LED current drops from its steady state value, 0.5 A, to 0 in less than 4 μs. The experimental results are consistent with the simulation

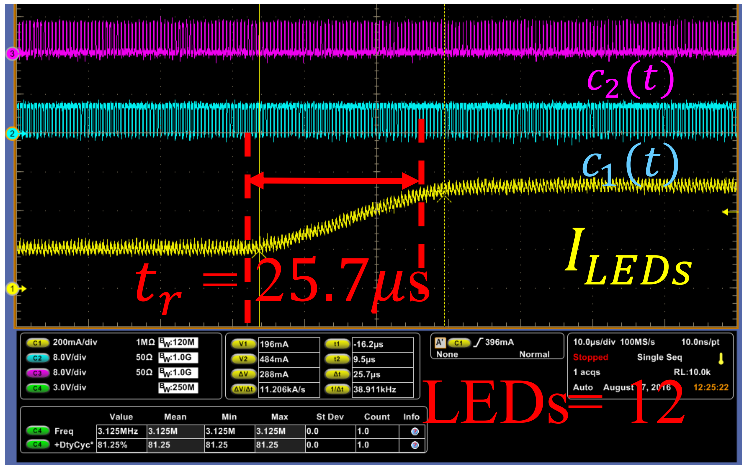
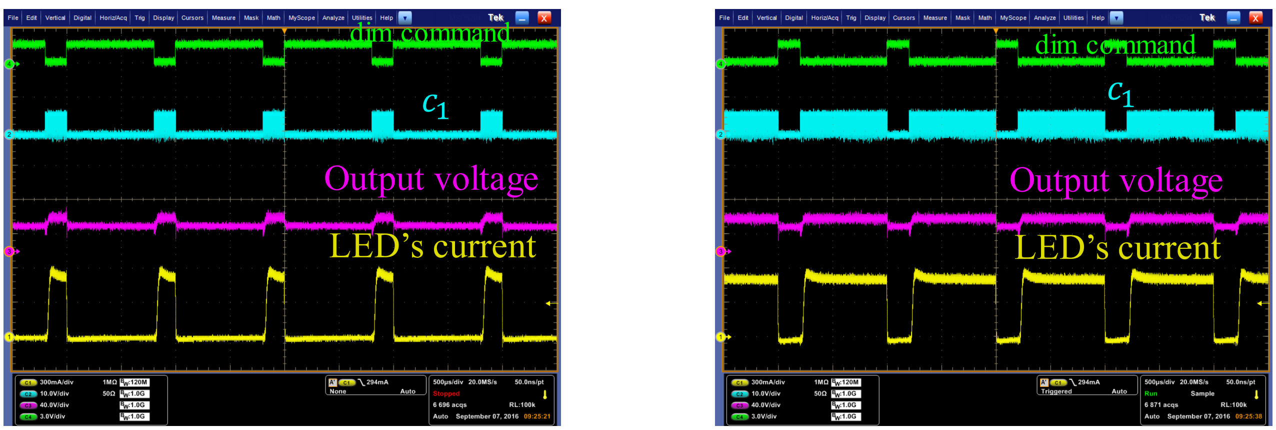


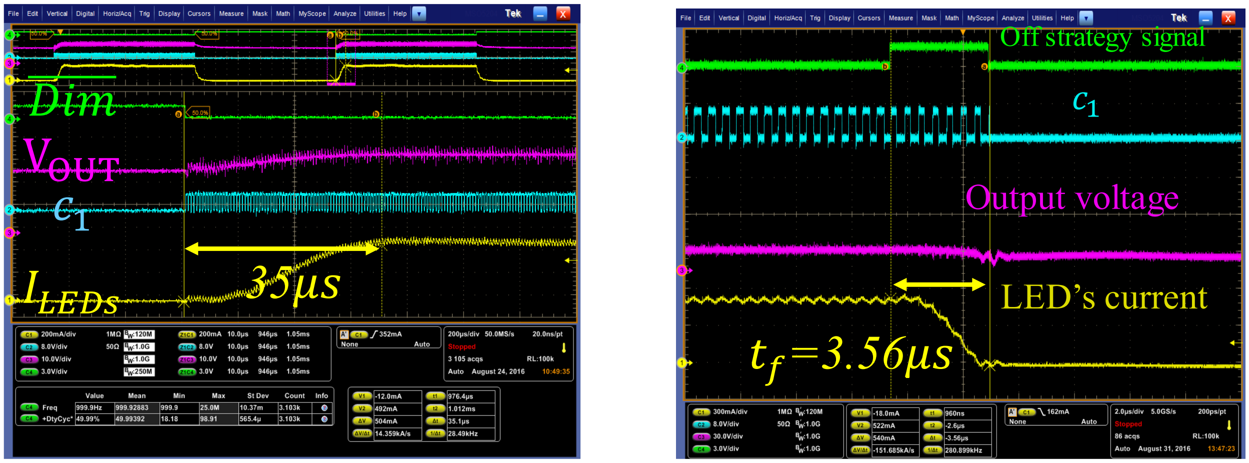
Figure 4.18: LED current response to a 250 mA step change in the reference current is shown for V_{IN} = 12 V, V_{OUT} = 40 V (N = 12).



(a) (b)

Figure 4.19: PWM dimming performance for a dimming frequency f_{dim} = 1 kHz and dimming duty cycle (a) D_{dim} = 20% and (b) D_{dim} = 80%. V_{IN} = 12 V, V_{OUT} = 40 V (N = 12), I_{LED} = 0.5 A.

results.



(a) (b)

Figure 4.20: Turn-on and turn-off transitions: (a) turn-on transition for $V_{IN} = 12$ V, $V_{OUT} = 40$ V ($N = 11$) and (b) turn-off transition for $V_{IN} = 12$ V, $V_{OUT} = 15$ V ($N = 5$).

4.3 Summary

This chapter describes output current regulation and a PWM dimming architecture for the high-frequency ZVS planar integrated magnetics Ćuk converter for automotive LED driver applications. The converter's small-signal dynamics are analyzed using Spice simulations of an averaged circuit model comprising a 3D-FEM based model of the integrated magnetics and an averaged-switch model. Based on the Spice-simulated duty-cycle-to-output-inductor-current transfer function, the loop gain of the system is obtained, and an integral compensator is designed to achieve a bandwidth of 15 kHz and a worst-case phase margin of 57^o. This compensator precisely regulates the average output inductor current, and hence the LED current, over the entire output voltage range of the converter (3 V to 50 V). The control architecture is enhanced to include fast PWM dimming functionality. To enable high-resolution PWM dimming, new turn-off and turn-on strategies are proposed. The proposed turn-off strategy reduces the fall time of the LED current by up to 83%, while the turn-on strategy reduces the rise time by up to 40%. The controller and the turn-off and turn-on schemes are implemented in a digital fashion using an FPGA. Experimental results on the 2 MHz, 30 W, 0.5 A prototype demonstrate overshoot-free regulation of the LED current, as well as fast turn-on and turn-off dimming performance.

CHAPTER 5

High Frequency LC^3L Resonant DC-DC converter for Automotive Applications

Contents

To achieve even higher performance in automotive LED driver applications, the switching frequency of the automotive LED drivers may be increased further. At these higher frequencies (> 2.4 MHz) the integrated magnetics Cuk converter may not be a suitable candidate due to higher losses in the magnetics. The converter may also exhibit a relatively narrow ZVS range at higher frequencies. Furthermore, the size of the integrated magnetics structure limits the achievable power density of this converter.

This chapter studies high frequency resonant dc-dc converters as an alternative approach for automotive LED driver applications. A block diagram of a resonant dc-dc converter is shown in Fig. 5.1. The converter consists of an inverter, a transformation stage (resonant tank) and a rectifier. Resonant dc-dc converters are capable of achieving zero-voltage switching (ZVS) and near zero-current switching (ZCS). To achieve soft switching the converter switching frequency is selected such that the resonant tank input current is slightly inductive relative to the inverter output voltage. However, as the operating point varies, the resonant tank input impedance might

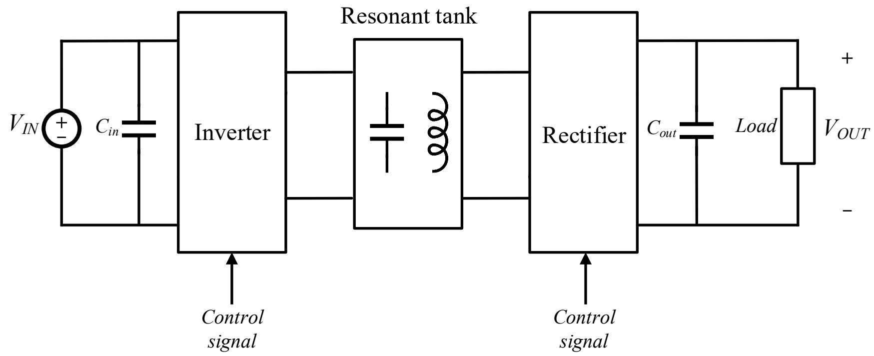


Figure 5.1: Block diagram for a resonant dc-dc converter.

become capacitive, resulting in lose of ZVS, or become too inductive, leading to loss of ZCS and high circulating currents. In a high frequency, high efficiency automotive LED driver, it is desired to maintain soft switching over wide input and output voltage ranges.

This chapter is organized as follows. Section. 5.1 studies the LLC resonant dc-dc converter for automotive LED driver applications and discusses its drawbacks. Section 5.2 proposes an LC^3L resonant converter with current source characteristics, well-suited for automotive LED driver applications. Section 5.3 discusses the design of the LC^3L resonant dc-dc converter and provides simulation results. Finally Section. 5.4 summarizes the chapter.

5.1 LLC Resonant DC-DC Converter

The schematic of an LLC resonant dc-dc converter for automotive LED driver applications is shown in Fig. 5.2 [56,57]. The inverter stage consists of transistors Q_1 and Q_2, switching alternately at 50% duty ratio. The resonant tank comprises L_r, C_r and L_M, designed to provide the required voltage transformation. The output of the tank is fed into a synchronous rectifier, consisting of transistors Q_3 and Q_4. A dc-blocking capacitor C_b prevents saturation of the inductor L_M. A string of N LEDs is connected at the output of the converter. The converter is analyzed using sinusoidal approximation, where only the first harmonic of the waveforms are considered [2]. Under this approximation the inverter stage is modeled as a sinusoidal voltage source with an amplitude

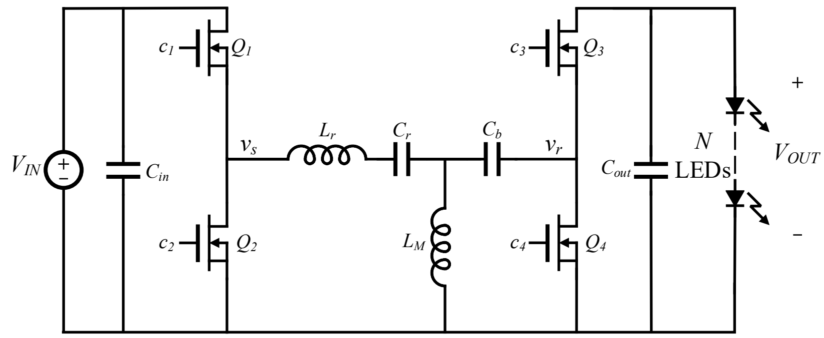


Figure 5.2: Schematic of LLC resonant dc-dc converter.

$v_s = \frac{2V_{IN}}{\pi}$. The rectifier is modeled as an effective resistor, given by:

$$R_{eff} = \frac{2\ V_{OUT}}{\pi^2\ I_{OUT}}. \tag{5.1}$$

The equivalent fundamental-frequency circuit model is shown in Fig. 5.3. The input impedance of

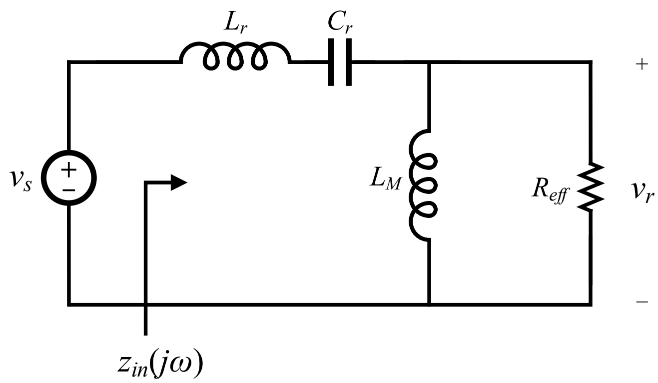


Figure 5.3: The equivalent circuit model of the LLC resonant dc-dc converter under sinusoidal approximation.

the resonant tank $z_{in}(j\omega)$ can be expressed as:

$$z_{in}(j\omega) = L_r j\omega + \frac{1}{C_r j\omega} + R_{eff}||L_M j\omega. \tag{5.2}$$

The normalized voltage conversion ratio $M = \frac{v_r}{v_s}$ is expressed as:

$$M(f_n, \lambda, Q) = \frac{R_{eff}||L_M j\omega}{z_{in}(j\omega)} \tag{5.3}$$

$$M(f_n, \lambda, Q) = \frac{1}{1 + \lambda + \frac{\lambda}{f_n} + jQ(f_n - \frac{1}{f_n})}. \tag{5.4}$$

where $Z_o = \sqrt{\frac{L_r}{C_r}}$ and $Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{eff}}$ are the characteristic impedance and the quality factor of the series resonance tank (L_r and C_r) respectively. $\lambda = \frac{L_r}{L_M}$ and $f_n = \frac{f_s}{f_r}$ is the normalized switching frequency with $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$.

The normalized voltage conversion ratio of the LLC resonant dc-dc converter M is shown as a function of the normalized frequency f_n, for various values of Q (corresponding to different numbers of LEDs) in Fig. 5.4 . The converter input voltage V_{IN} = 8 V-to-40 V and the output current is set at I_{OUT} = 0.5 A. The output voltage of the converter varies from 3 V-to-60 V (N = 1-18). The ratio of L_r to L_M, λ, is selected such the required maximum and minimum gain are guaranteed in the specified normalized frequency range, f_n = 0.9 to 1.2 (f_s = 1.8-to-2.4 MHz). As the number of LEDs varies, N = 1 to 18, the converter switching frequency needs to be adjusted across a wide range to provide the required gain, as also shown in Fig. 5.4. The operating points are selected in the inductive region to ensure ZVS of the inverter transistors. The phase of the resonant tank input impedance is plotted versus normalized switching frequency f_n in Fig. 5.5. The operating points of the converter are overlaid on the phase plot. It can be seen that across the operating range, the phase remains positive, indicating that the inverter is inductively loaded. However, since the phase is always greater than 50^o, the converter suffers from high circulating currents. This can be better understood by evaluating the magnitude of the input impedance of the LLC converter's resonant tank $|z_{in}|$ which is shown for various numbers of LEDs in Fig. 5.6. As the number of LEDs N decreases, corresponding to a decrease in the effective load resistance R_{eff} (indicating less output power is required), the magnitude of the tank input impedance decreases monotonically [2]. Therefore, as the number of LEDs increases, the magnitude of the tank input current is higher, and hence higher circulating currents are generated. This results in reduced efficiency, making the LLC resonant dc-dc converter ill-suited for an automotive LED driver application with wide input and output voltage ranges.

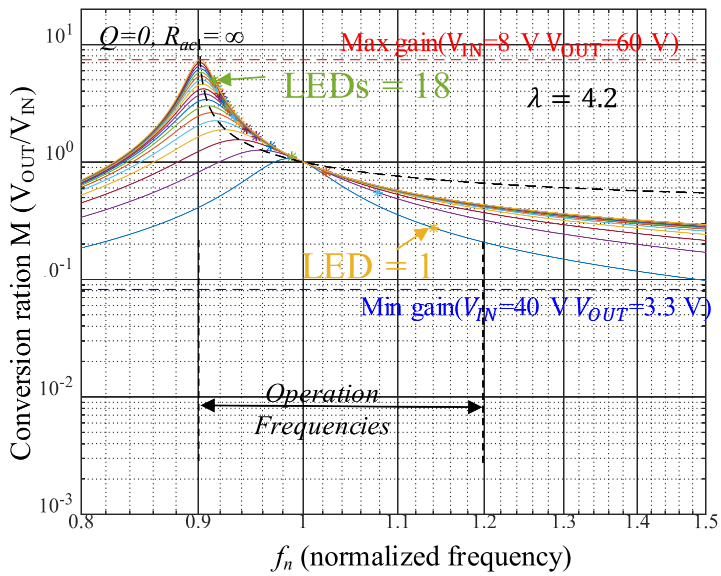


Figure 5.4: Voltage conversion ration M vs normalized switching frequency f_n.

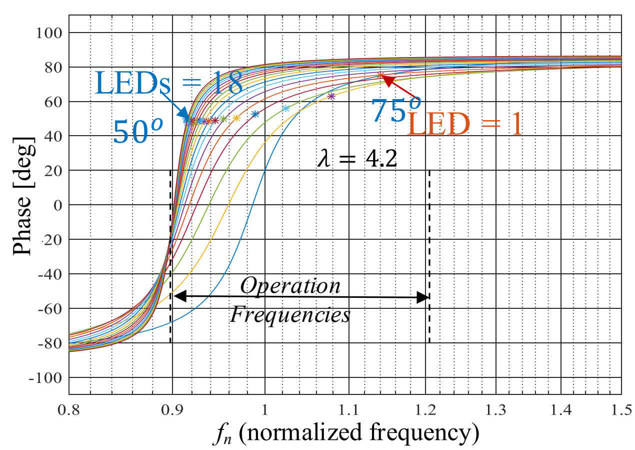


Figure 5.5: Phase of the tank input impedance z_{in} vs normalized switching frequency f_n.

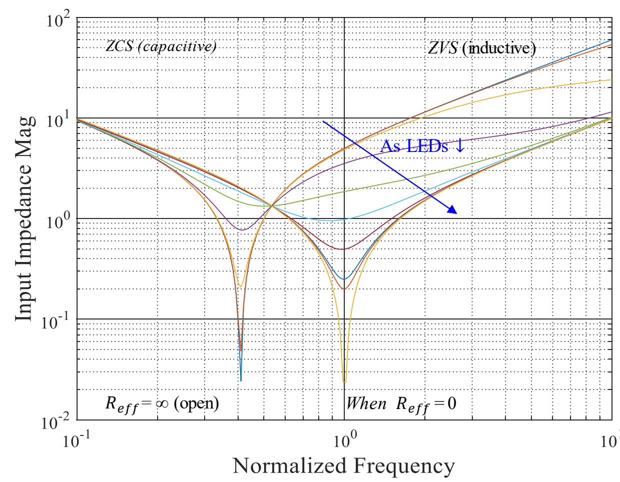


Figure 5.6: Magnitude of the tank input impedance $|z_{in}|$ vs normalized switching frequency f_n.

5.2 Proposed LC^{3}L Resonant DC-DC converter

To overcome the limitations of the LLC converter described above, it is desired to utilize a converter topology in which the magnitude of the resonant tank input impedance increases, and hence the tank input current decreases, as the number of LEDs decreases. In this thesis an LC^{3}L resonant dc-dc converter with such properties is proposed, and shown in Fig. 5.7. The converter

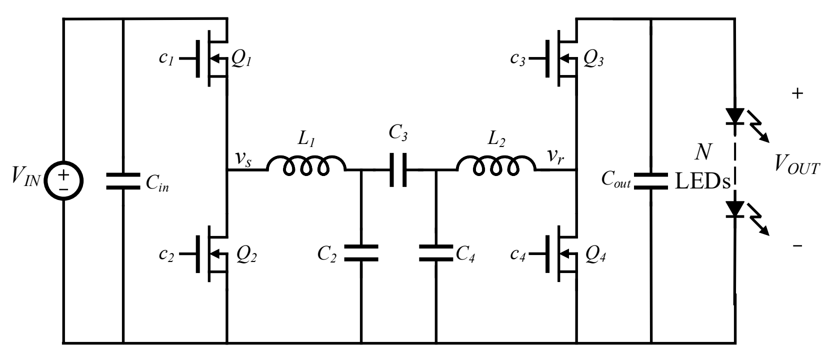


Figure 5.7: Schematic of LC^{3}L resonant dc-dc converter.

uses a half-bridge inverter, a two-inductor, three-capacitor resonant tank, and a half-bridge rectifier. The converter is analyzed using sinusoidal approximation and the resonant tank equivalent circuit is shown Fig. 5.8. The tank input impedance $z_{in}(j\omega)$ is given by:

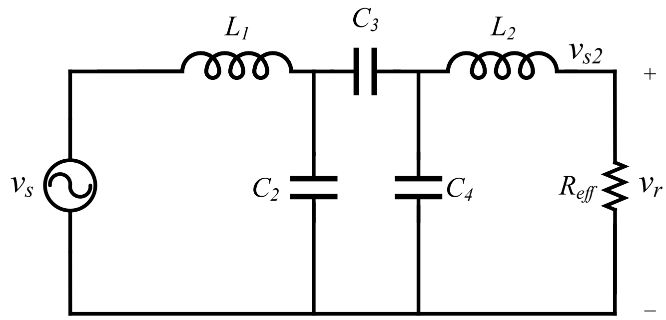


Figure 5.8: The resonant tank equivalent model under sinusoidal approximation.

$$z_{in}(j\omega) = a + jb = L_1 j\omega + \frac{1}{C_2 j\omega}||(\frac{1}{C_3 j\omega} + (\frac{1}{C_4 j\omega}||(L_2 j\omega + R_{eff}))). \tag{5.5}$$

To ensure minimal circulating currents, it is desired to to design the resonant tank such the imaginary part b of the tank input impedance is close to zero. A design that ensures this is found by setting $b = 0$ in (5.5) resulting the following relationships:

$$C_2 = \frac{2(L_1 - 2L_2)}{L_1(L_1 - 4L_2)\omega^2}, \tag{5.6}$$

$$C_3 = \frac{2}{(4L_2 - L_1)\omega^2}, \tag{5.7}$$

$$C_4 = C3. \tag{5.8}$$

It is interesting to note that these design equations have no dependence on the converter's output voltage or power, hence ensuring that circulating currents are minimized regardless of the number of LEDs. Under the design constraints given by (5.6 - 5.8), the real part of the tank input impedance is given by:

$$a = \frac{L_1^2 \omega^2}{4\ R_{eff}}. \tag{5.9}$$

The magnitude of the tank input current is given by:

$$I_{in} = \frac{2V_{IN}}{\pi\ a} = \frac{2V_{IN}}{\pi\ \frac{L_1^2\omega^2}{4\ R_{eff}}} = \frac{16 V_{IN} V_{OUT}}{\pi^3 \omega^2 L_1^2 I_{OUT}}. \tag{5.10}$$

Equation (5.10) indicates that for a constant output current I_{OUT}, as the number of LEDs (corresponding to V_{OUT}) decreases, the magnitude of the tank input current also decreases. This is in contrast to the LLC converter analyzed earlier, and makes the proposed LC^{3}L converter well-suited for automotive LED driver applications. The behavior of the proposed LC^{3}L converter is encapsulated by Fig. 5.9, wherein the design frequency is 10 MHz. Depending on the number of LEDs, the converter switching frequency may be selected slightly higher or slightly lower than the design frequency to ensure the tank input impedance has positive phase, as can be seen from the phase plot in Fig. 5.9.

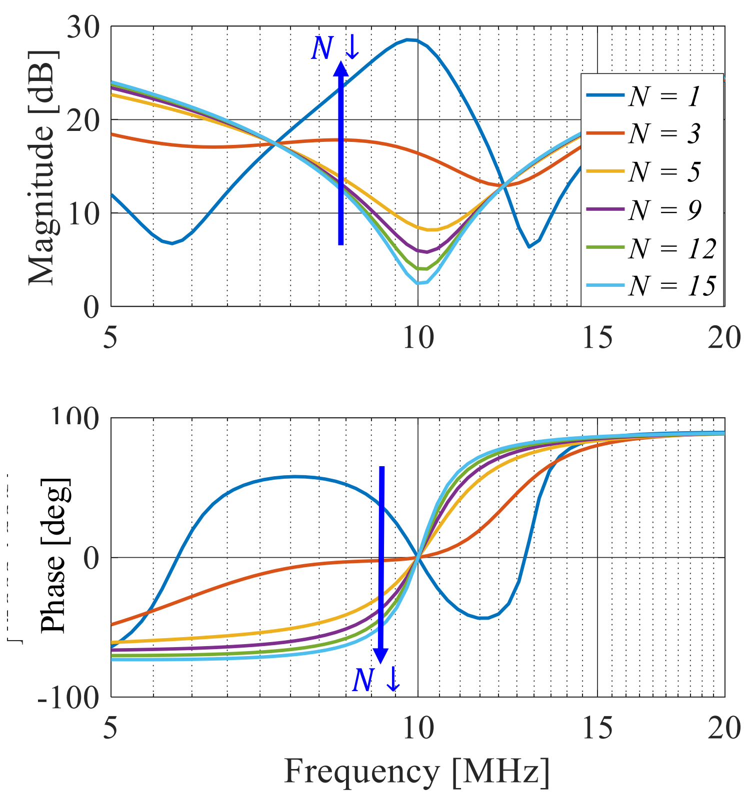


Figure 5.9: The magnitude and phase of the tank input impedance of LC^{3}L versus the switching frequency.

Assuming lossless conversion, the converter output current I_{OUT} is given by:

$$I_{OUT} = \frac{2\sqrt{2}V_{IN}}{\pi L_1 \omega}. \tag{5.11}$$

It can be seen that the converter output current does not depend on the output voltage and hence the number of LEDs. Therefore, this converter behaves like a current source, and is capable of supplying a constant current to a string of variable numbers of LEDs. With variations in the input voltage, the output current can be controlled by modifying the phase-shift between the inverter and the rectifier, or using narrowband frequency variations.

5.3 Simulation Results

The proposed LC^{3}L converter is simulated in a Spice tool, and the switching node voltage v_s and the tank input current i_{L_1} are shown in Fig. 5.10. It can be seen that the converter achieves

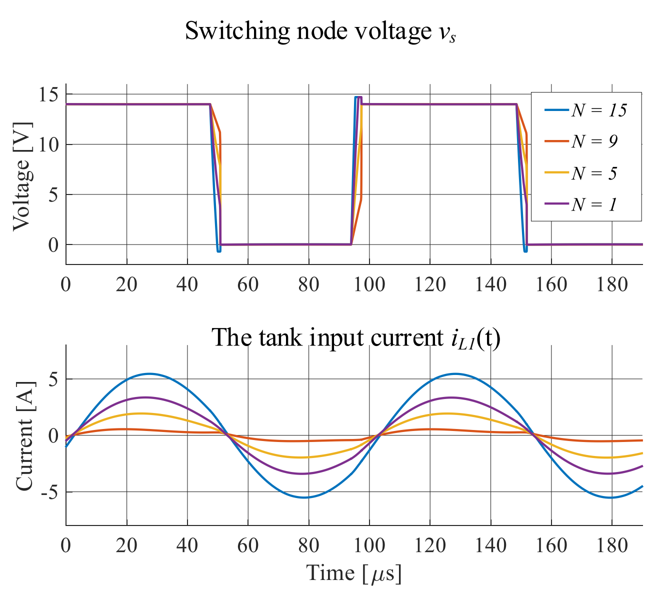


Figure 5.10: Simulation waveform for switching node voltage v_s and the tank input current i_{L_1}.

ZVS over a wide range of operating conditions. As predicted by (5.10), the magnitude of the tank input current decreases as the number of LEDs decreases, while its phase remains slightly inductive with minimal circulating currents.

The converter's power-on and power-off times are depicted in Fig. 5.11(a) and (b) respectively for $V_{IN} = 14$ V, $I_{OUT} = 0.5$ A, $N = 1$ and $C_{out} = 1$ μF. Also, in Fig. 5.12 the power-on and power-off times are presented for V_{IN} = 14 V, I_{OUT} = 0.5 A, N = 12 and C_{out} = 50 nF. The converter output capacitor is selected such that the LEDs current ripple is less than 10%. Compared to the turn-on time of the ZVS integrated magnetics Ćuk converter presented in chapter 4, the proposed LC^{3}L converter has 80% faster power-on time. The power-off time of the proposed converter is also 20% smaller. This enhanced performance is due to higher switching frequency and reduced energy storage requirements.

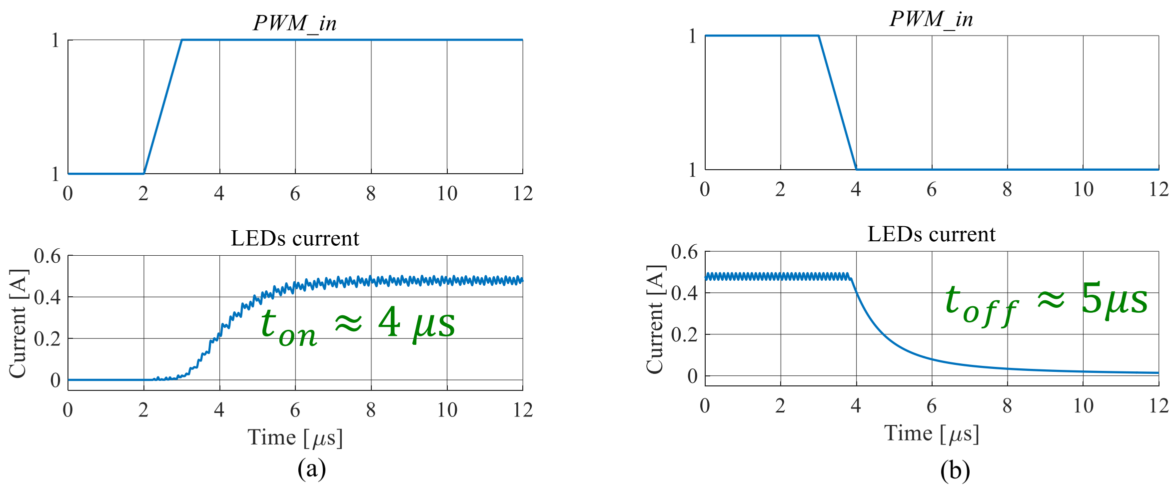


Figure 5.11: The proposed LC^{3}L resonant dc-dc converter (a) power-on and (b) power-off transients for V_{IN} = 14 V, I_{OUT} = 0.5 A, N = 1 and C_{out} = 1 μF.

A prototype of proposed converter is designed for the specifications shown in Table 5.1, using off-the-shelf components.

A loss model is developed for the proposed converter, which includes transistor conduction losses, winding losses in the air-core inductors and gate-drive losses. The inductor winding losses are computed based on the ac resistance provided in the inductor datasheets. Since the converter achieves ZVS and near-ZCS, switching losses are negligible. Based on this loss analysis, the converter efficiency is predicted to be 86.7% for V_{IN} = 14 V, I_{OUT} = 0.5 A, N = 9 and a switching frequency f_s of 10 MHz. The loss break down of the converter at this operating point is shown in Fig. 5.13. It can be seen that greater than 65% of the losses owe their origin to winding losses

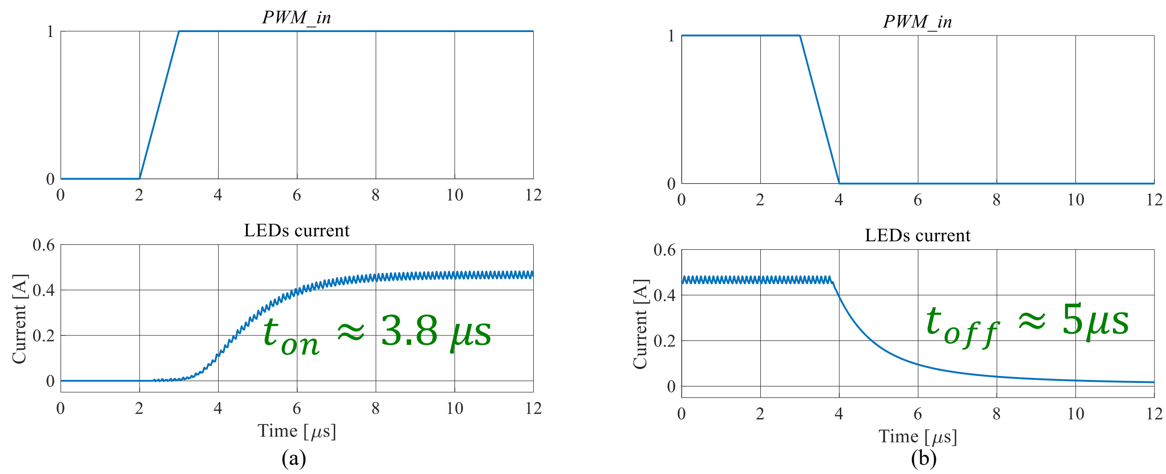


Figure 5.12: The proposed LC^{3}L resonant dc-dc converter (a) power-on and (b) power-off transients for V_{IN} = 14 V, I_{OUT} = 0.5 A, N = 12 and C_{out} = 50 nF

Table 5.1: Design details for the LC^{3}L resonant dc-dc converter.

Switching frequency f_{sw}	10 MHz
Input voltage V_{IN}	14 V
Output voltage V_{OUT}	3 V to 50 V (N = *1 to 15*)
Output current I_{OUT}	0.5 A
Inductor L_1	180 nH Coilcraft 2222SQ series
Inductor L_2	100 nH Coilcraft 2222SQ series
Capacitors C_2	0.25 nF
Capacitors $C_3 = C_4$	2.3 nF
Inverter and rectifier	Texas Instruments LMG5200 (TI's 80 V GaN HB power stage)

of the inductors, indicating that significant efficiency improvement is achievable through custom magnetics design. A PCB layout of the proposed LC^{3}L resonant dc-dc converter is performed to compare its size to the ZVS integrated magnetics Ćuk converter discussed in previous chapters. The dimensions of the two converters are illustrated in Fig. 5.14. It can be seen that the area of the proposed LC^{3}L converter is approximately 65% less than the Ćuk converter. The volume of the magnetics in the proposed LC^{3}L resonant dc-dc converter is 92% smaller than the volume of the integrated magnetics structure of the Ćuk converter.

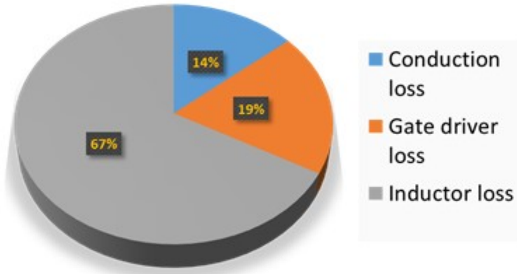


Figure 5.13: Loss breakdown for $V_{IN} = 14$, $I_{OUT} = 0.5$ A, $N = 9$ and the switching frequency $f_s = 10$ MHz.

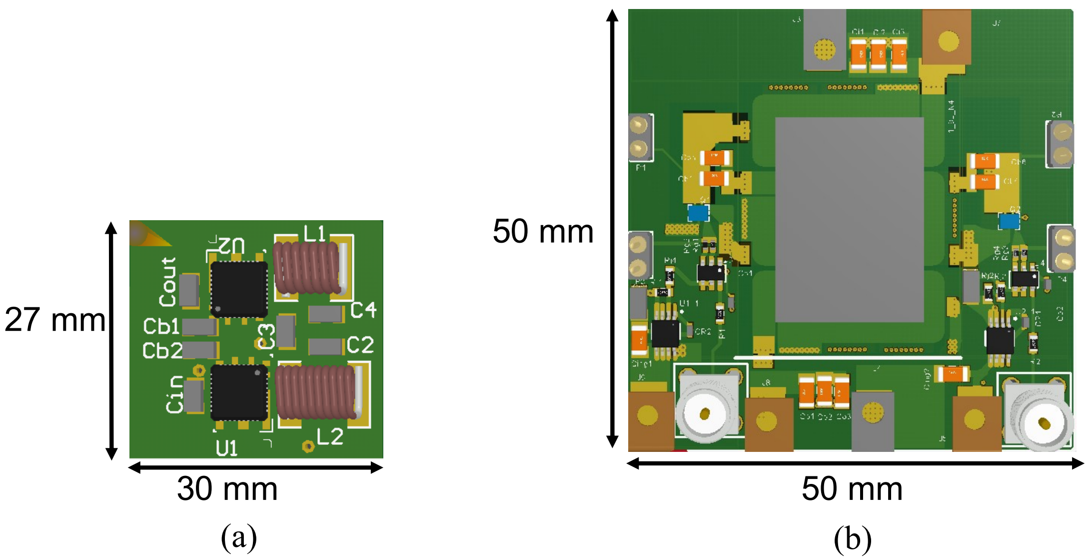


Figure 5.14: Size comparison of the LC^{3}L resonant dc-dc converter and integrated magnetics ZVS Ćuk in chapter (3).

5.4 Summary

In this chapter, resonant dc-dc converters are studied as an alternative approach for automotive LED driver applications. First, the LLC resonant dc-dc converter is analyzed. The analysis reveals that the LLC converter suffers from high circulating currents when designed to operate over a wide range of input and output voltages. A novel LC^{3}L resonant dc-dc converter is proposed. The proposed topology achieves soft-switching and maintains minimal circulating currents across wide operating ranges. This converter also features current source characteristics, making it particularly suitable for automotive LED driver applications. The converter performance is verified using simulations, indicating grater than 80% faster power-on and 20% faster power-off transitions even without any turn-on or turn-off strategy applied. The converter is predicted to achieve an efficiency of 86.7% for a string of 9 LEDs. A 10 MHz prototype of the proposed converter is designed and shown to be 65% smaller than the ZVS planar integrated magnetics Ćuk converter.

CHAPTER 6

High Frequency Monolithic Power Stages in a Normally-Off GaN Process

Contents

Resonant converters presented in chapter. 5, enable automotive LED driver to operate at high switching frequency (up to 10 MHz). However, increasing the switching frequency to very high frequency (VHF) and ultra high frequency (UHF) levels requires advances in circuit topologies and design techniques, high-Q passive components, as well as higher performance semiconductors, such as GaN devices [21–39]. In particular, monolithic integration of GaN switching power devices and gate drivers has enabled high efficiency operation of pulse-width modulated (PWM) converters at up to 200 MHz switching frequencies [22, 24–26, 39], with 90% power-stage efficiency at 100 MHz switching frequency reported in [22].

These results have been reported for a depletion-mode (normally-on) GaN-on-SiC process, which raises practical concerns related to system start-up issues. Furthermore, pull-up techniques employed in the integrated gate drivers introduce challenging trade-offs between switching speed of power devices, power-stage switching losses, and driver power consumption.

In this chapter, the monolithic power stage integration approach is advanced for an enhancement-mode (normally-off) GaN-on-SiC process using a new gate-driver circuit with improved switching speed versus power consumption trade-off. A synchronous buck converter using the monolithic normally-off GaN half-bridge with the new integrated gate driver circuitry is shown in Fig. 6.1(a), and a photograph of the GaN chip die is shown in Fig. 6.1(b). A family of monolithic GaN chips has been designed, targeting operation from up to 50 V, delivering up to 16 W of output power, and operating at 20-400 MHz switching frequencies.

The chapter is organized as follows: the monolithic normally-off GaN power stages including half-bridge power switches and integrated gate drivers are described in Section 6.1. The GaN chip optimization is summarized in Section 6.2. Experimental results, including efficiency measurements and switching waveforms, are presented in Section 6.3 for synchronous buck converter prototypes operating at 20-400 MHz switching frequencies from up to 45 V supply voltage. Finally, Section 6.4 concludes the chapter.

6.1 Monolithic Normally-off GaN Half-Bridge Power Stage with Integrated Gate Drivers

A circuit diagram of the monolithic GaN power stage chip is shown in Fig. 6.1(a). This chip includes two power stage transistors in a half-bridge configuration (Q_H and Q_L), with two gate drive circuits, 'HS driver' and 'LS driver', employed for the high-side and the low-side transistors, respectively. The chip is realized in a normally-off GaN process with a threshold voltage $V_{th} \approx +0.1$ V [32]. The positive threshold voltage ensures the leakage current is sufficiently low at zero gate-to-source bias. As a result, the GaN power chip converter can be safely powered up as a normally off power stage. However, since V_{th} is close to zero, the gate driver must be able to supply a positive gate-to-source voltage to turn the power device fully on, and a negative gate-to-source voltage to turn the power device off during normal operation. Using $V_{dd} > 0$ and $V_{ss} < 0$, the gate drivers described in this chapter are capable of producing such bipolar gate-to-source drive voltages. Simply by adjusting the gate-driver supply voltages V_{dd} and V_{ss}, the same circuits can also be applied to produce positive or negative unipolar drive voltages to accommodate normally-off (enhancement-mode) or normally-on (depletion mode) processes, respectively.

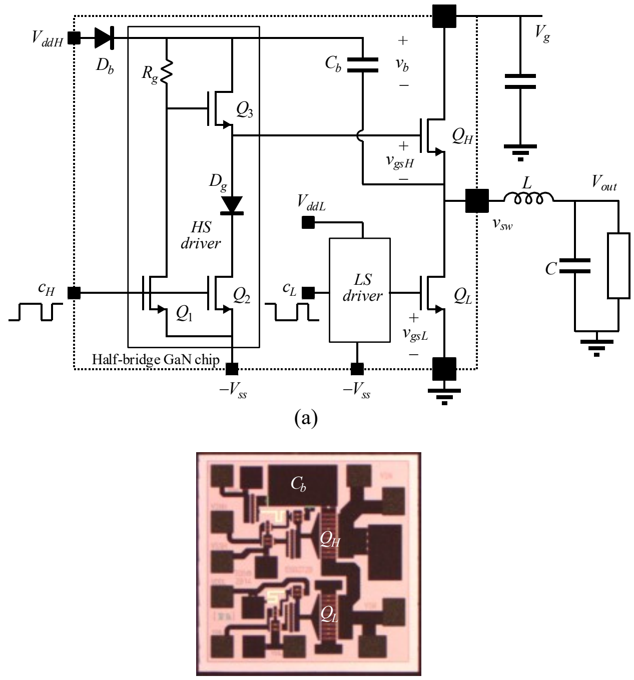


Figure 6.1: (a) Circuit diagram of the synchronous buck converter using the monolithic GaN half-bridge power stage chip with integrated gate drivers; (b) die photo of the (2mm × 2mm) GaN chip optimized for 100 MHz switching frequency.

[!h]

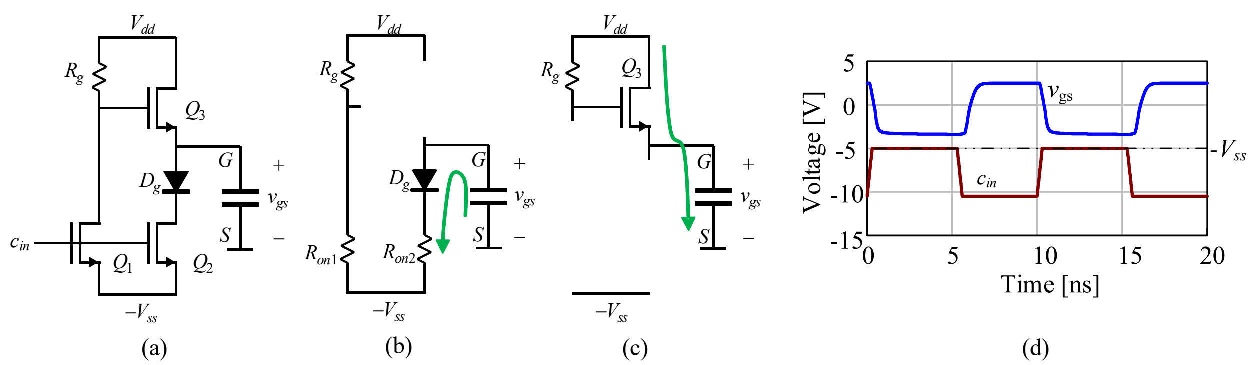


Figure 6.2: (a) Proposed gate driver circuit with the power-device gate-to-source capacitive load; (b) the driver circuit when the input PWM signal (c_{in}) is high, and (c) when the input PWM signal (c_{in}) is low; (d) simulation waveforms illustrating the gate driver operation at 100 MHz.

The logic inputs to the two gate drive circuits are complementary PWM signals with associated dead-times, shown as c_H and c_L in Fig. 6.1(a). The high-side and the low-side gate driver circuits have identical configurations. Details are shown only for the high-side driver, which further includes a level shifting circuit consisting of the bootstrap capacitor C_b and the bootstrap diode D_b. Note that the bootstrap components are integrated on the same chip. Diodes D_b and D_g are Schottky diodes realized in the same GaN process, hence eliminating losses related to reverse recovery, which would otherwise adversely affect efficiency at very high switching frequencies. The new gate driver circuit is constructed so as to minimize static power consumption while at the same time improving current source and current sink capabilities.

The driver circuit operation is explained with reference to Fig. 6.2. When the input PWM signal (c_{in}) is logic high, transistors Q_1 and Q_2 are turned on. As Q_1 turns on, the gate of Q_3 is pulled to the negative gate-driver rail ($-V_{ss}$). Furthermore, as Q_2 turns on, a low-impedance path is formed through diode D_g and Q_2 to discharge the power-device gate-to-source capacitance. As a result, v_{gs} is pulled down to

$$v_{gs} = -V_{ss} + V_{Dg} \approx -2.5 \text{ V}, \tag{6.1}$$

which is sufficient to fully turn off the power device. Due to the voltage drop V_{Dg} across the forward biased diode D_g, the gate-to-source voltage of Q_3 is negative, and Q_3 is off, as shown in Fig. 6.2(b). In this state, static power consumption in the driver is determined by the power dissipated predominantly in the pull-up resistor R_g taking into account that the on-resistance R_{on1} of the transistor Q_1 is much smaller than R_g. In the half-bridge configuration, neglecting dead times, one of the two gate drivers is in this state. Hence, assuming the same R_g is employed in the high-side and the low-side driver, (6.3) approximates the total static power consumption in the on-chip integrated gate drivers.

When the input PWM signal (c_{in}) is logic low, the transistors Q_1 and Q_2 are off. The gate of transistor Q_3 is pulled to V_{dd} by R_g. The equivalent circuit of the gate driver in this state is shown in Fig. 6.2(c). The source-follower Q_3 quickly charges the power device gate-to-source capacitance to

$$v_{gs} \approx V_{dd} - V_{th} \approx 2.5 \text{ V}, \tag{6.2}$$

where $V_{th} \approx +0.1$ V is the device threshold voltage. As a result, the power switch turns on. In this state the static power consumption is zero. It is important to note that the driver current sourcing is greatly enhanced by the source-follower Q_3. As a result, a large R_g can be employed, minimizing the driver static power consumption. Fig. 6.2(d) shows the waveform of the input PWM signal (c) and the driver output voltage (v_{gs}) for the GaN chip optimized for operation at 100 MHz. One may note that the driver propagation delay, the rise time, and the fall time are all less than 1 ns.

Compared to the previously reported integrated GaN gate drivers [22,25], the main advantage of the new gate driver is that the pull-up resistor R_g is neither in the source nor in the sink path at the output of the driver. In contrast, Q_3 and Q_2 act as active, low-impedance source and sink paths, respectively, while R_g can be increased in value, thus reducing the quiescent power consumption given by (6.3 without affecting the driver switching speed. This property resembles the operation of standard complementary gate drivers commonly employed in CMOS processes, even though only n-type devices are available in the considered GaN process.

$$P_{driver} = \frac{(V_{dd} + V_{ss})^2}{R_g}\,, \tag{6.3}$$

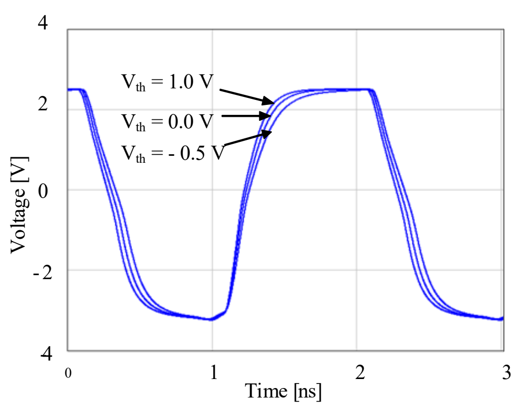


Figure 6.3: Simulated output voltage of the proposed gate driver at 500 MHz switching frequency, as the threshold voltage of the transistors is changing from $-0.5V$ to $1V$.

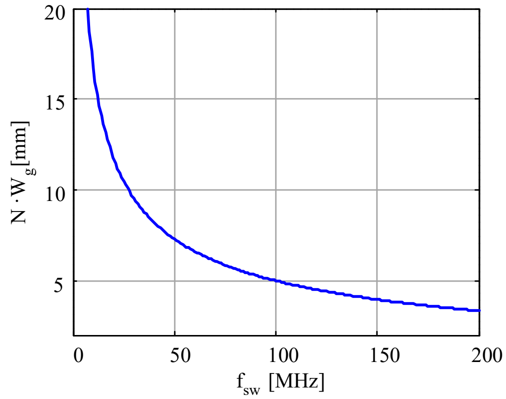


Figure 6.4: The optimum power-stage device size as a function of switching frequency for a 25 V, 5 W ZVS-QSW synchronous buck converter.

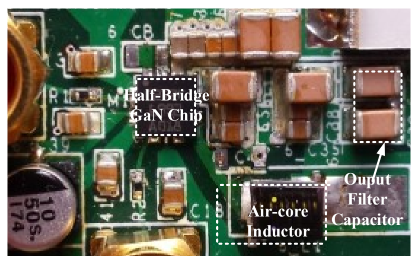


Figure 6.5: Photograph of the 100 MHz synchronous buck converter prototype using the GaN chip in the 20-pin 4mm × 4mm QFN package and 47 nH air-core inductor.

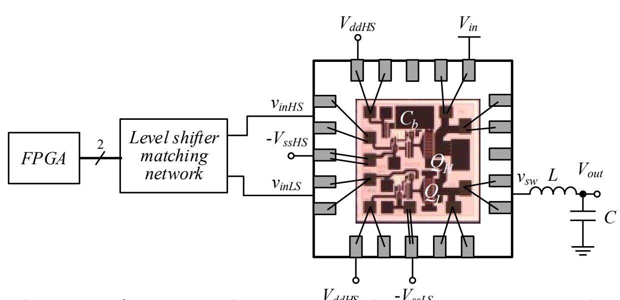


Figure 6.6: The test setup diagram for a synchronous buck converter using the monolithic GaN power chip.

6.2 GaN Power Chip and Converter Design Optimization

Another advantage of the proposed gate driver is that the circuit operation is relatively independent of the threshold voltage, which is beneficial as the threshold voltage changes with process variations or with temperature. Simulations have been performed to examine the sensitivity to threshold voltage variations. Fig. 6.3 shows the output voltage of the proposed gate driver as the

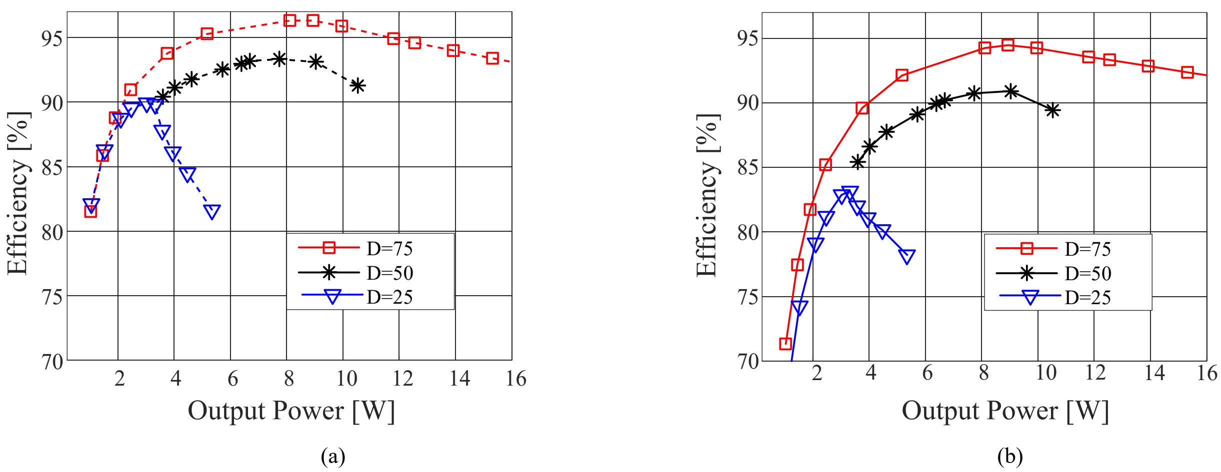


Figure 6.7: (a) Power stage efficiency and (b) overall efficiency for different duty cycles as functions of output power for the synchronous buck converter operating at 20 MHz from 25 V supply voltage.

threshold voltage of the transistors varies from -0.5 V to 1 V. As the threshold voltage varies, only slight changes in the rise and fall times can be observed. It may be noted that even at a switching frequency as high as 500 MHz, the effect of threshold voltage variation is minimal. The monolithic half-bridge GaN power chips presented in the previous section are used to construct synchronous buck converters operated with resonant transitions in the zero-voltage switching quasi-square-wave (ZVS-QSW) mode [47]. The converter circuit utilizing the GaN power chip is shown in Fig. 6.1(a). Using state-plane analysis, the filter inductance is selected to maintain ZVS operation of the power stage transistors across wide operating ranges in terms of output voltages and power levels. In the GaN power chip, the half-bridge power-stage transistors and the gate-driver circuits are sized to maximize efficiency for a given power level and a target switching frequency, following a loss modeling and optimization approach similar to what has been described in [21]. As an example, Fig. 6.4 shows the optimum power-stage device size as a function of the switching frequency, for a 25 V, 5 W ZVS-QSW synchronous buck converter operating at 50% duty cycle.

A photograph of one of the GaN power chips, optimized for 100 MHz switching frequency and up to 5 W power, is shown in Fig. 6.1(b). The size of the chip die is 2mm $\times$ 2mm. Depending on intended power level, the fabricated GaN chips have been packaged in 20-pin 4mm $\times$ 4mm or

5mm × 5mm QFN packages.

6.3 Experimental Results

Based on the operation and design approaches presented in Sections II and III, a family of monolithic GaN half-bridge power stage chips has been designed, fabricated, and tested in ZVS-QSW synchronous buck converters at switching frequencies between 20 MHz and 400 MHz, input voltage levels ranging from 20 V up to 45 V, and output power levels up to 16 W. The power converters use high-Q RF-compatible air-core inductors from Coilcraft (1812SMS and 2222SQ series). Low-ESR ceramic capacitors from American Technical Ceramics are used as input voltage decoupling and output filter capacitors. A photograph of one of the tested buck converter prototypes, using the 100 MHz optimized GaN chip, a 47 nH Coilcraft air-core inductor (1812SMS series), and a 1 µF American Technical Ceramics low-ESR ceramic capacitor is shown in Fig. 6.5.

The PWM control signals (c_H and c_L in Fig. 6.1(a)) for the half-bridge GaN chips are obtained from an Altera Stratix IV FPGA, which provides PWM control signals with 125 ps resolution. A simple level-shifter interfaces the FPGA with the GaN chip gate driver inputs. A diagram of the test setup for the buck converters is shown in Fig. 6.6. A summary of the power stage and overall efficiency of the converter prototypes is provided in Table 6.1.

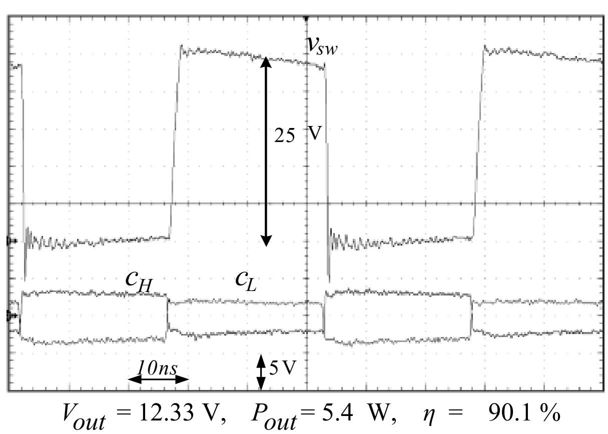


Figure 6.8: Switching node (v_{sw}) and the input control signals (c_H and c_L) at 50% duty cycle for the 20 MHz, 25 V ZVS-QSW synchronous buck converter.

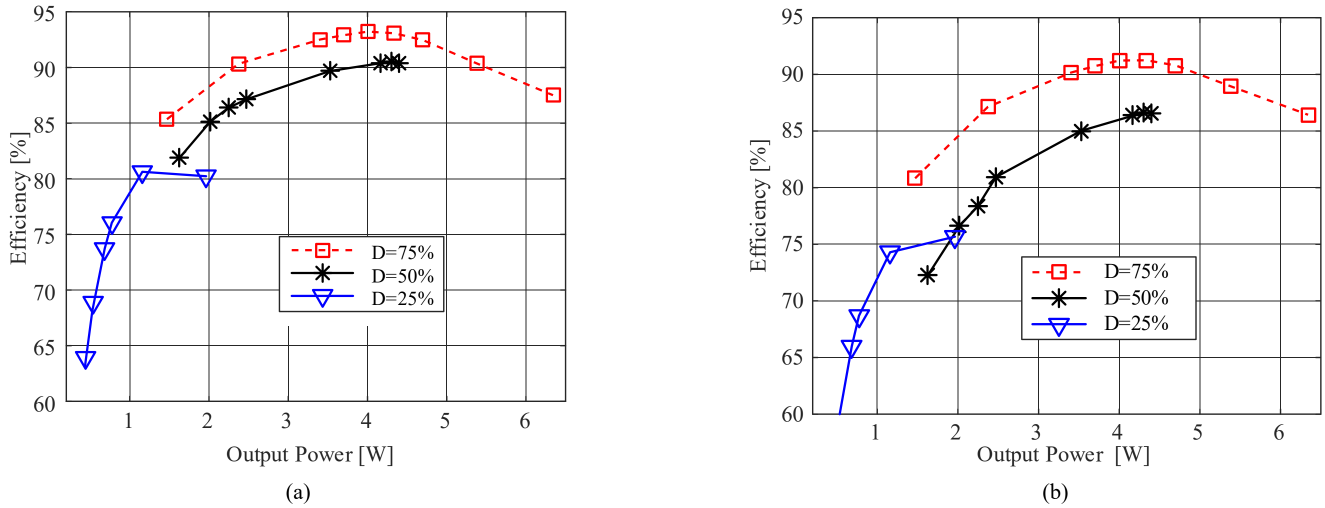


Figure 6.9: (a) Power stage efficiency and (b) overall efficiency for different duty cycles as functions of output power for the synchronous buck converter operating at 100 MHz from 25 V supply voltage.

Next, measured operation waveforms and efficiency curves are presented for selected converter prototypes.

6.3.1 ZVS-QSW buck converter operating at 20 MHz from 25 V input voltage

Power stage efficiency as well as overall efficiency (including the gate drive losses) of the ZVS-QSW synchronous buck converter prototype operating at 20 MHz from 25 V input voltage are shown in Fig. 6.7(a) and Fig. 6.7(b) respectively. In this case, the size of the power stage transistors gate periphery (Q_H and Q_L) is 6 mm, and the gate-drive resistor R_g is 950 Ω. A peak power stage efficiency of 95.1% is obtained at 75% duty cycle. The converter maintains greater than 90% power efficiency and greater than 85% overall efficiency over a wide range of output power (4 to 16 W), at 50% and 75% duty cycles. Switching node voltage (v_{sw}) and PWM control signals (c_H and c_L) for 50% duty cycle operation are shown in Fig. 6.8. Smooth low-to-high and high-to-low transitions typical for ZVS-QSW operation can be observed.

Table 6.1: Experimental results for synchronous buck converter prototypes using monolithic GaN power chips with integrated gate drivers

Switching frequency, f_s [MHz]	20	50	100	200	400	100
Input voltage [V]	25	25	25	25	20	45
Maximum output power [W]	16.0	10.1	7.1	3.4	5.0	6.0
Peak power stage efficiency [%]	95.0	94.2	93.2	86.5	72.5	91.7
Peak total efficiency [%]	92.5	91.7	89.2	82.0	67.0	90.2
Inductance (L) [nH]	160	90	47	22	12.5	90
Duty cycle (D) [%]	75	75	75	75	50	50

6.3.2 ZVS-QSW buck converter operating at 100 MHz from 25 V input voltage

Power stage and overall efficiency for the 100 MHz, 25 V ZVS-QSW synchronous buck converter prototype are shown in Fig. 6.9. The size of the power stage transistors gate periphery (Q_H and Q_L) is 2.6 mm, and R_g is 950 Ω. This converter achieves a peak efficiency of 93.2% at 75% duty cycle. Switching node voltage and PWM control signals for this prototype, at 50% duty cycle, are shown in Fig. 6.10, illustrating ZVS operation.

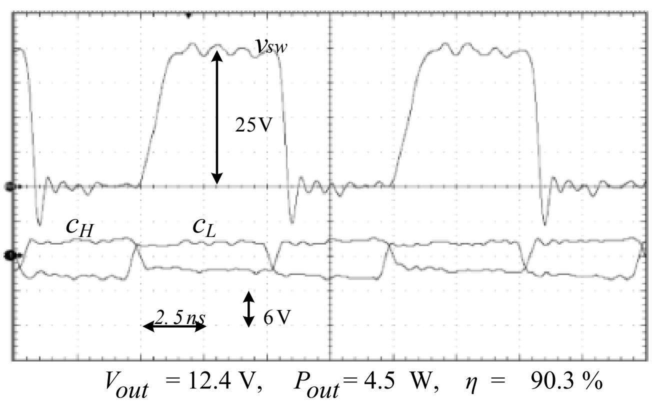


Figure 6.10: Switching node voltage (v_{sw}) and the input control signals (c_H and c_L) at 50% duty cycle for the 100 MHz, 25 V ZVS-QSW synchronous buck converter.

6.3.3 ZVS-QSW buck converter operating at 200 MHz from 25 V input voltage

Efficiency plots for the 200 MHz, 25 V ZVS-QSW buck converter prototype are shown in Fig. 6.11, for operation at 50% duty cycle. The prototype uses the GaN power chip optimized for 100 MHz operation. Peak power stage efficiency greater than 86% is recorded at high output power levels (> 3 W). The switching node voltage and PWM control signals for this converter at 50% duty cycle are shown in Fig. 6.12.

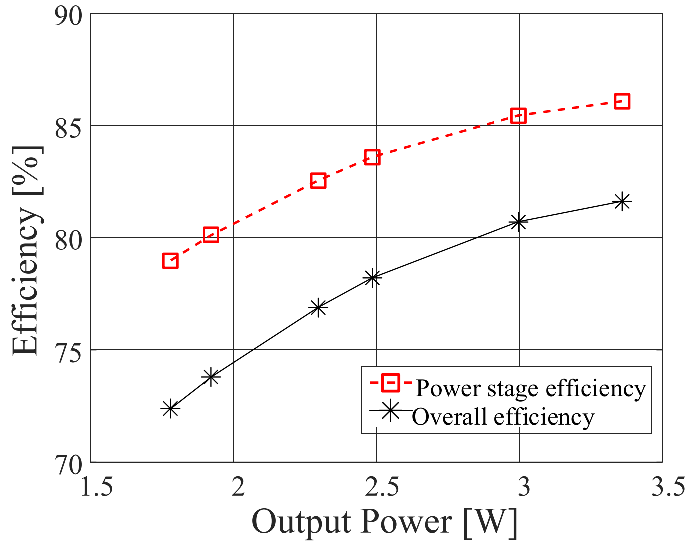


Figure 6.11: Power stage and overall efficiency (at 50% duty cycle) vs output power for the 200 MHz, 25 V ZVS-QSW synchronous buck converter.

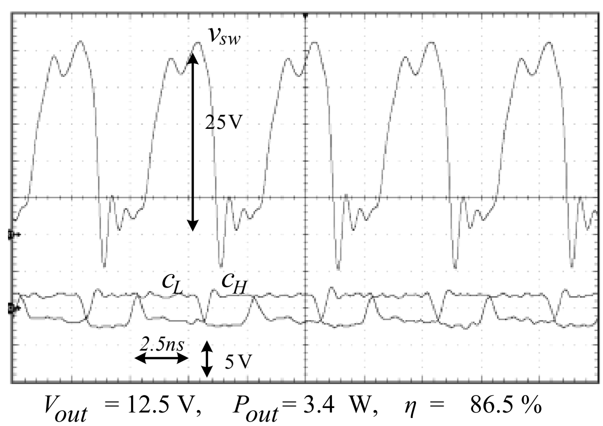


Figure 6.12: Switching node voltage (v_{sw}) and the input control signals (c_H and c_L) at 50% duty cycle for the 200 MHz, 25 V ZVS-QSW synchronous buck converter.

6.3.4 ZVS-QSW Buck converter operating at 400 MHz from 20 V input voltage

Power stage efficiency results for the 400 MHz, 20 V ZVS-QSW buck converter prototype are shown in Fig. 6.13. In this case, the size of the power stage transistors gate periphery (Q_H and Q_L) is 1.6 mm, and R_g is 150 Ω. Due to practical difficulties of generating complementary input control signals at ultra high switching frequencies, the 400 MHz prototype was operated in the non-synchronous mode. The low side transistor was turned off, and operated as a rectifier in the reverse conduction mode. The reverse conduction behavior of the low-side transistor can be observed in Fig. 6.14, wherein the switching node (v_{sw}) shows a larger excursion to negative voltages. Nevertheless, a greater than 72% peak power stage efficiency has been obtained.

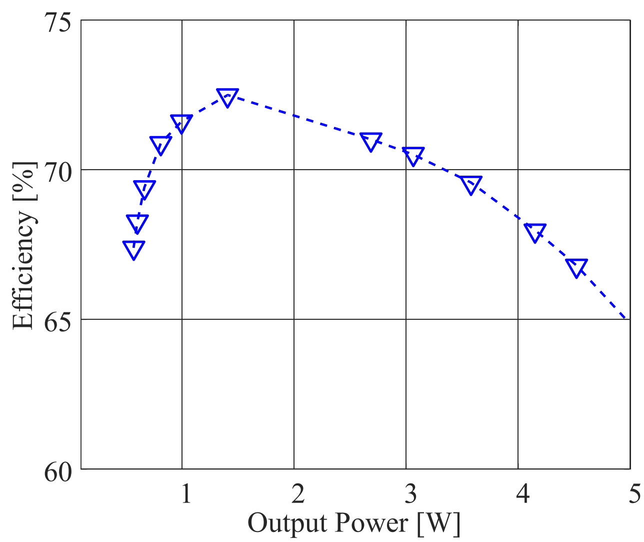


Figure 6.13: Power stage efficiency (at 50% duty cycle) for the buck converter operating at 400 MHz from 20 V input voltage.

6.3.5 ZVS-QSW buck converter operating at 100 MHz from 45 V input voltage

The power stage and the overall efficiency for the 100 MHz, 45 V ZVS-QSW synchronous buck converter are shown in Fig. 6.15 as functions of the output power. The size of the power stage transistors gate periphery (Q_H and Q_L) is 1.6 mm, and R_g is 1 kΩ. Note that a larger R_g is employed to support higher-voltage operation. The peak efficiency of 91.7% is obtained at high

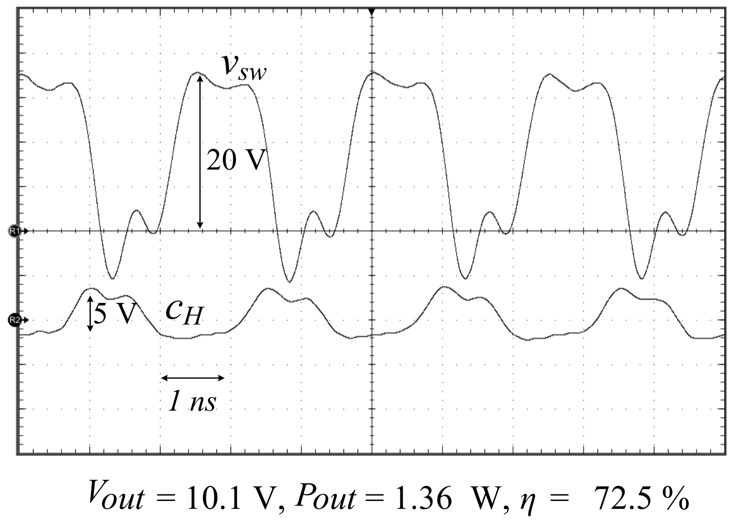


Figure 6.14: Switching node (v_{sw}) and the input control signal (c_H) at 50% duty cycle for the 400 MHz, 20 V buck converter.

output power levels ($\approx$ 6 W). Fig. 6.16 shows the switching node voltage and the control signals for this converter operating at 50% duty ratio.

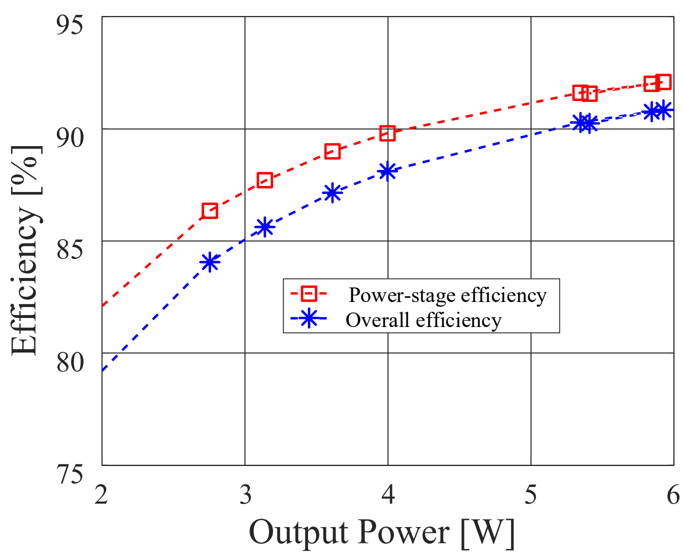


Figure 6.15: Power stage and overall efficiency vs output power at 50% duty cycle for a 100 MHz and 45 V QSW synchronous buck converter.

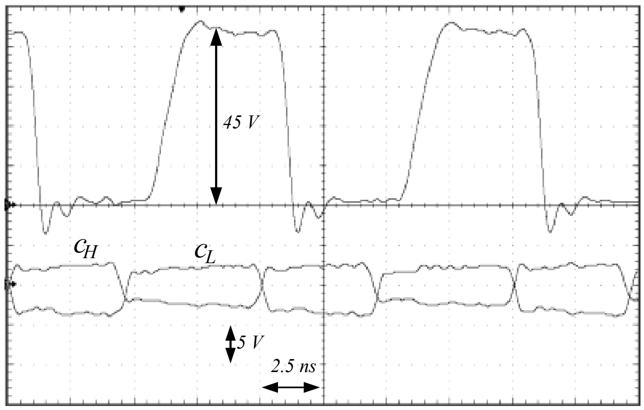


Figure 6.16: Switching node (v_{sw}) and the input control signals (c_H and c_L) at 50% duty cycle for a 100 MHz and 45 V QSW synchronous buck converter.

6.4 Summary

In search of new design techniques and architectures for high performance automotive LED drivers, this chapter studies high efficiency dc-dc converters operating at very-to-ultra high frequencies, ranging from the 20 MHz to 400 MHz. The high performance is achieved using monolithic GaN half-bridge power chips with integrated gate drivers in an enhancement-mode (normally-off) GaN-on-SiC process. While using only n-type transistors available in the GaN process, a novel gate driver circuit has been developed to maintain low static power consumption while enabling fast switching by emulating complementary operation similar to approaches commonly employed in processes such as CMOS where complementary devices are available. Level shifting is accomplished using a bootstrap technique, with the bootstrap capacitor and the bootstrap diode integrated on the same GaN power chip. A family of monolithic GaN chips has been designed, targeting operation from up to 45 V, delivering up to 16 W of output power, and operating at 20-400 MHz switching frequencies. The GaN chips are verified in synchronous buck converters, demonstrating record peak power stage efficiencies of 95.0% at 20 MHz, 94.2% at 50 MHz, 93.2% at 100 MHz, 86.5% at 200 MHz, and 72.5% at 400 MHz.

CHAPTER 7

Conclusions and Future work

Contents

7.1 Summary of Contributions

The thesis is focused on high frequency techniques applied to dc-dc converters operating as drivers for automotive lighting applications based on light emitting diodes (LED). The design of dc-dc LED drivers is challenging because the required input voltage range and the output voltage range can be very wide. The input voltage is nominally around $12 - 14$ V, set by the automotive low-voltage battery, but can be as low as 4.5 V (during cold-start events) or as high as around 45 V (during âĂIJload dumpâĂİ events). The output voltage, which depends on the number N of LED's in series, can be between 3 V ($N = 1$), and about 50 V ($N = 18$). Furthermore, stringent EMI requirements impose the need for substantial input and output filtering. Switching frequency above the AM radio band is preferred to avoid interference, but is difficult to achieve because of switching losses. Controller design is also challenging because the output dc current through the LED string must be precisely regulated, while high-resolution pulse with modulation (PWM) dimming requires short current turn on and turn off times. Conventional state-of-the-art solutions are based on buck-boost or boost followed by buck stages operating at up to hundreds of kilohertz, with bulky magnetics and efficiency well below 90%.

To overcome limitations of the conventional LED driver solutions, two approaches are proposed and developed in this thesis: a ZVS integrated-magnetics Ćuk converter suitable for operation around 2 MHz, and an LC^3L resonant converter, which is a promising configuration for operation at even higher frequencies.

The high frequency ZVS integrated magnetics Ćuk converter is found to be very well suited for automotive LED driver applications, as described in Chapter 2 of this thesis. The input and output filter inductors and the transformer are coupled and wound on a single magnetics structure. The input and output current ripples are steered to the transformer magnetizing inductor. Therefore very low input and output current ripples are obtained, thus mitigating EMI filtering requirements. As a result, small input or output filter capacitors are sufficient. ZVS operation makes it possible to achieve relatively high efficiency at frequency above the AM band (1.8 Mhz). However, with conventionally wound magnetics, leakage inductances result in significant voltage spikes across the transistors. In order to mitigate the effects of transformer leakage inductance, two active-clamp snubbers are used. Unfortunately, this results in additional gate-drive and conduction losses. With silicon MOSFETs, a prototype ZVS Ćuk converter with conventionally wound magnetics achieves 84% peak efficiency for V_{IN} = 12, V_{OUT}= 16 V, I_{OUT} = 0.5 A and f_{sw} = 1.8 MHz.

Efficiency can be improved by reducing the transformer leakage inductance and hence eliminating the need for active snubbers, as discussed in Chapter 3. A planar integrated magnetics structure is proposed to minimize the leakage inductance of the transformer. The strucure features a low profile and small number of turns. The transformer primary and secondary windings are interleaved to further reduce the leakage inductance. The input and output filter inductor number of turns are adjusted to achieve the ripple steering effect. The integrated magnetics structure is simulated using 3D-FEM tools, which is employed to obtain a Spice model. The Spice model of the integrated magnetics is then used in a Spice simulator to predict the converter behavior, including ZVS conditions and losses, and to design a controller. Two power stage prototypes using Silicon MOSFETs or GaN transistors are designed, built and tested. ZVS operation over wide range of output voltages is verified by experiments. A variable frequency method is proposed to maximize the efficiency over a range of output voltages, i.e. for different number of LEDs connected at the output. The prototype with Silicon MOSFETs (FDMS86105) achieves a peak efficiency of 92.9%, while the converter using GaN transistors (EPC2007C) achieves a peak efficiency of 93.5% and greater than greater than 90% efficiency over a wide range of output voltages (12 V-to-42 V).

In Chapter 4, the converter dynamics are studied analytically, as well as using the Spice model of the integrated magnetics, and the averaged-switch modeling technique. It is found that the duty-cycle control signal to output inductor current transfer function features a low-frequency gain weakly dependent on the output voltage. Based on this property, a simple integral compensator is designed to regulate the output inductor current over the entire operating range.

PWM dimming is performed by turning the converter on and off based on the PWM dimming control signal at up to around 1 kHz frequency. Turn-on and turn-off strategies are developed to achieve fast turn-on and turn-off transitions within 30 μs and 4 μs, respectively. The fast transients enable high resolution PWM dimming. The controller is implemented in a digital fashion using an Altera IV FPGA. Experimental results verify steady state regulation and PWM dimming.

The second approach pursued, which is potentially suitable for even higher frequency operation, is based on resonant dc-dc conversion techniques. In Chapter 5 it is found that an LLC resonant converter exhibits high circulating currents when designed for a wide output voltage range. Therefore, the LLC converter is not best suited for automotive LED driver applications. A novel LC^{3}L resonant dc-dc converter is proposed. With a properly designed resonant tank, which consists of two inductors and three capacitors, the converter average output current is independent of the output voltage. This current-source property is very well suited for the intended application. A prototype converter is designed and verified by simulations. The converter exhibits ZVS transitions over almost the entire output voltage range, and its predicted efficiency is above 86% at 10 MHz switching frequency. The prototype converter is expected to be approximately 65% smaller in area than the ZVS planar integrated magnetics Ćuk converter.

Resonant converters operating at 10 MHz or even higher switching frequencies rely on capabilities of GaN power devices with superior figures of merit. Furthermore, it is found that efficiency gains and switching frequency capabilities can be extended further by means of integration of the power stage transistors and gate-drivers. In Chapter 6 of the thesis, it is shown how high performance can be achieved using monolithic GaN half-bridge power chips with integrated gate drivers in an enhancement-mode (normally-off) GaN-on-SiC process. While using only n-type transistors available in the GaN process, a novel gate driver circuit has been developed to maintain low static power consumption while enabling fast switching by emulating complementary operation similar to approaches commonly employed in CMOS processes. Level shifting is accomplished using a bootstrap technique, with the bootstrap capacitor and the bootstrap diode integrated on the same GaN power chip. A family of monolithic GaN chips has been designed, targeting operation from up to 45 V, delivering up to 16 W of output power, and operating at 20-400 MHz switching frequencies.

7.2 Future Work

A number of directions can be pursued starting from the work reported in this thesis.

Custom controller chip design for ZVS IM Ćuk LED drivers.

The control techniques developed in Chapter 4 of this thesis are well suited for implementation in a custom controller chip using analog, digital, or mixed-signal approaches.

Analysis of the LC^{3}L converter using non-sinusoidal techniques.

The work presented in Chapter 5 is based on standard sinusoidal approximation. However, the tank port currents may contain substantial harmonics, which is an opportunity for application of analysis techniques that do not rely on sinusoidal approximation, such as those presented in [58, 59]

Prototyping LC^{3}L resonant dc-dc converter.

Design techniques for the LC^{3}L resonant dc-dc converter suitable for automotive LED driver applications are verified by simulations. Prototyping and experimental evaluation are the necessary follow-up steps. It is expected that custom inductor design could yield significant efficiency improvements.

Closed loop control of the LC^{3}L converter.

The simulation results shown in Chapter 5 are done with the converter operating in open loop. A closed-loop control scheme needs to be developed to precisely control the output current in the presence of input and output voltage variations. Phase-shift or variable-frequency control techniques are promising.

Automotive LED drivers using GaN chips. The monolithic integrated gate driver GaN chips enable high frequency and high efficiency power conversion at very high switching frequencies. Further developments and practical applications of monolithic GaN power chips for automotive LED and many other applications is a promising direction for future work.

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APPENDIX A

Spice Netlist

This appendix includes the Spice model for the inteerated mangetics structure mentioned in Chapter 3.

```
.subckt E22_N5_Tx_L_Rac 1 2 3 4 5 6 7 8
    X1 1 2 3 4 5 6 7 8 E22_N5_Tx_L_Rac_series
    .subckt E22_N5_Tx_L_Rac_series 1 2 3 4 5 6 7 8
        V1 1 9 dc 0.0
        V2 2 10 dc 0.0
        V3 3 11 dc 0.0
        V4 4 12 dc 0.0
        R1 9 13 0.111997764025
        R2 10 14 0.417801049651
        R3 11 15 0.481999906272
        R4 12 16 0.0859181616104
        F1_2 13 9 V2 0.166558
        F1_3 13 9 V3 -0.284281
        F1_4 13 9 V4 -0.738547
        F2_1 14 10 V1 0.0446483
        F2_3 14 10 V3 0.207544
        F2_4 14 10 V4 -0.0216015
```

```
        F3_1 15 11 V1 -0.0660556
        F3_2 15 11 V2 0.179901
        F3_4 15 11 V4 0.0453416
        F4_1 16 12 V1 -0.962725
        F4_2 16 12 V2 -0.105043
        F4_3 16 12 V3 0.254366
        L1 13 5 5.72190379151e-007
        L2 14 6 2.69351157506e-006
        L3 15 7 2.69284252617e-006
        L4 16 8 5.66040905421e-007
        K1_2 L1 L2 0.483024
        K1_3 L1 L3 -0.481614
        K1_4 L1 L4 -0.987883
        K2_3 L2 L3 0.279938
        K2_4 L2 L4 -0.48208
        K3_4 L3 L4 0.483584
    .ends E22_N5_Tx_L_Rac_series
.ends E22_N5_Tx_L_Rac
```

APPENDIX B

VHDL Scripts

This appendix includes example VHDL code implementing the digital controller described in Chapter 4.

```
library ieee;                                  -- tell which library
USE ieee.std_logic_1164.ALL;                   -- used standard logic variables, binary variables
use IEEE.STD_LOGIC_UNSIGNED.ALL;               -- the library again from ieee
use ieee.numeric_std.all;                      -- It is needed for data type conversion
--use ieee.std_logic_arith.all;

entity I is
GENERIC (
LengthCounterPWM : INTEGER := 14;
KID: INTEGER := 1;
NbitSD : INTEGER := 1;
NbitADC : INTEGER :=12
);
```

```
Port (
     clk: in std_logic;  --SWITCHING
     dim_ctrl: in std_logic;
     reference: in std_logic_vector(NbitADC-1 downto 0);
     y_mis: in std_logic_vector(NbitADC-1 downto 0);
     y_I: out std_logic_vector(LengthCounterPWM+NbitSD-1 downto 0)
     );
end I;
architecture Behavioral of I is

component saturated_adder is                                              --saturated_adder
generic (
n    :    integer
);
port (
     a,b  :    in std_logic_vector(n-1 downto 0);
     s         :    out std_logic_vector(n-1 downto 0);
     OV        :    out std_logic;
     op        :    in std_logic
);
end component;

component saturated_multiplier is                                         --saturated_multiplier
```

```
generic (
n, p, m   :    integer        --   m<=n+p
);

port (
     x         :    in std_logic_vector(n-1 downto 0);
     y         :    in std_logic_vector(p-1 downto 0);
     z         :    out std_logic_vector(m-1 downto 0);
     OV        :    out std_logic
     );
end component;



signal u_k: std_logic_vector(LengthCounterPWM+NbitSD-1 downto 0);  --
   ↪   signal  u[k]
signal u_k_1: std_logic_vector(LengthCounterPWM+NbitSD-1 downto 0);  --
   ↪  delayed  signal  u[k-1]
signal u_k_ss: std_logic_vector(LengthCounterPWM+NbitSD-1 downto 0);
   ↪ -- steady state value of u[k]
signal e_k     : std_logic_vector(NbitADC-1 downto 0);  -- error signal
   ↪  e[k]
signal e_k_1: std_logic_vector(NbitADC-1 downto 0);  -- delayed error
   ↪ signal e[k-1]
signal e_add: std_logic_vector(NbitADC-1 downto 0);  -- for output of
   ↪ e[k] + e[k-1]
signal e_mult: std_logic_vector(LengthCounterPWM+NbitSD-1 downto 0);
```

```
    ↪ -- for output of  KID(e[k] + e[k-1])
signal y_mis_k: std_logic_vector(NbitADC-1 downto 0);  -- for latching
    ↪ the input from ADC
signal fake_sig: std_logic:='0';

constant KIDDstd: std_logic_vector (LengthCounterPWM+NbitSD-NbitADC-1
    ↪ downto 0) := std_logic_vector(to_unsigned(KID, LengthCounterPWM+
    ↪ NbitSD-NbitADC));
constant saturation_INT: std_logic_vector (LengthCounterPWM+NbitSD-1
    ↪ downto 0) := "001101101011000";



begin

     diff_ref_ymis : saturated_adder
         ↪                                                   --
         ↪ diff_ref_ymis
     generic map(
     n => 12
     )
     port map(
          a => reference,
          b => y_mis_k,
          s => e_k,           -- error signal e[k]
          op => '0'  --       sx   <=   ax+bx when op='1' else   ax-bx;
     );

```

```
e_k_add : saturated_adder                                                --e[k]+e[k-1]
generic map(
n => 12
)
port map(
     a => e_k,
     b => e_k_1,
     s => e_add,              -- error signal e[k]+e[k-1]
     op => '1'  --       sx    <=    ax+bx when op='1' else   ax-bx;
);
-- Here we divide by 6
e_mult <= "11111111" & "11" & e_add(NbitADC-2 downto 6) when e_add (NbitADC-1) = '1' else "00000000"&"00" & e_add(NbitADC-2 downto 6);

k_1_proc : process(clk)  -- A proccess to generate e[k-1] and u[k -1]
begin
if dim_ctrl ='1' then
     --u_k <= std_logic_vector(to_signed(5300,LengthCounterPWM+ NbitSD)); -- Duty cycle equivalent for 500mA
     --u_k_1 <= std_logic_vector(to_signed(5300,LengthCounterPWM+ NbitSD)); -- Duty cycle equivalent for 500mA
     u_k <= u_k_ss-std_logic_vector(to_signed(1000, LengthCounterPWM+NbitSD)); -- Duty cycle equivalent for  500mA
```

```
            u_k_1 <= u_k_ss-std_logic_vector(to_signed(1000, LengthCounterPWM+NbitSD)); -- Duty cycle equivalent for 500mA
            y_mis_k <= (others => '0');
            e_k_1 <= (others => '0');
      else
            if (clk'event AND clk='1') then
                  e_k_1 <= e_k;
                  u_k_1 <= u_k;
                  y_mis_k <= y_mis;
                  u_k_ss <= u_k;
                  if( signed(e_mult)+signed(u_k_1) > signed(saturation_INT )) OR ( signed(e_mult) >0 AND signed(u_k_1) >0 AND (signed(e_mult)+signed(u_k_1) <0))then
                        u_k <= saturation_INT;
                  elsif ( (signed(e_mult) + signed(u_k_1))  < 0  ) then
                        u_k <= (others => '0');
            else
                  u_k <= u_k_1+e_mult;
                  end if;
            end if;
      end if;
      end process;

      y_I <= u_k;
end architecture;
```

VHDL script for digital pulse width modulator.

```
library ieee;
USE ieee.std_logic_1164.ALL;
use ieee.numeric_std.all;
-- simple control block for the PWM based in transceivers
-- input:
--        -> duty cycle
--        -> clock
--        -> reset

-- output:
--        -> address for the memory block, at a clk clock rate
--        LOW SIDE DATA = data_tx_LS1 NAND data_tx_LS2) AND data_tx_LS1
-- designed for a 400 MHz clock driving the transceivers, which gives 8
   ↪  Gbps and 125 ps resolution

entity duty_control_B is
     port
     (
          -- Input ports
          reset     : in  std_logic;
          clk  : in  std_logic;
          enable: in std_logic;
          phase_shift: in std_logic_vector(13 downto 0); -- 13 bit
             ↪ resolution,
          duty_cycle: in std_logic_vector(13 downto 0);  -- 13 bit
```

```
        ↪ resolution,
        td1: in std_logic_vector(13 downto 0);             -- dead
        ↪ times
        td2: in std_logic_vector(13 downto 0);
        td3: in std_logic_vector(13 downto 0);
        td4: in std_logic_vector(13 downto 0);
        tx_pll_locked: in std_logic_vector(0 downto 0); -- tx pll is
        ↪ locked, we can start operating
        -- Output ports
        clk_2M_out      : out std_logic;
        adc_sync        : out std_logic;
        address_HS      : out std_logic_vector(39 downto 0);
        address_LS      : out std_logic_vector(39 downto 0);
        address_HSn     : out std_logic_vector(39 downto 0);
        address_LSn     : out std_logic_vector(39 downto 0)
    );
end duty_control_B;


architecture rtl of duty_control_B is

-- Declarations (optional)
signal delayed_enable : std_logic:='0';
signal count_integer:integer range 0 to 111:=0;  -- This one tells what
↪  is the frequency. by deciding how many sections to be sent
signal count:std_logic_vector(4 downto 0):= (others => '0');
signal duty_cycle_sampled: std_logic_vector(13 downto 0):=(others =>
```

```
    '0');
signal phi_sampled: std_logic_vector(13 downto 0):=(others => '0');
signal td1_sampled: std_logic_vector(13 downto 0):=(others => '0');
signal td2_sampled: std_logic_vector(13 downto 0):=(others => '0');
signal td3_sampled: std_logic_vector(13 downto 0):=(others => '0');
signal td4_sampled: std_logic_vector(13 downto 0):=(others => '0');

-- TX signals
signal tx_pll_locked_latched:std_logic_vector(0 downto 0):="0";
signal locked_and_wait: std_logic:='0';

begin
    -- this process limits the and duty cycle and dead times
    process(reset,clk)
    begin
        if (reset = '0') then
            duty_cycle_sampled <= (others => '0');
        elsif (rising_edge(clk)) then
            -- phase shift
            phi_sampled <= phase_shift;
            --duty cycle
            if (signed(duty_cycle) > 3500) then   -- This is the max number for 2 MHz frequency
                duty_cycle_sampled <= std_logic_vector(to_signed(3500, 14));
            elsif (signed(duty_cycle) < 0) then
                duty_cycle_sampled <= std_logic_vector(to_signed(0,
```

```
                            14));
                else
                    duty_cycle_sampled <= duty_cycle;
                end if;
                ---td1
                if (signed(td1) >= 1000) then
                    td1_sampled <= std_logic_vector(to_signed(1000, 14));
                    elsif (signed(td1)+100 <= 0) then
                td1_sampled <= std_logic_vector(to_signed(-100, 14));
                else
                    td1_sampled <= td1;
                end if;
                ------td2
                if (signed(td2) >= 1000) then
                    td2_sampled <= std_logic_vector(to_signed(1000, 14));
                elsif (signed(td2)+100 <= 0) then
                    td2_sampled <= std_logic_vector(to_signed(-100, 14));
                else
                    td2_sampled <= td2;
                end if;
                ---td3
                if (signed(td3) >= 1000) then
                    td3_sampled <= std_logic_vector(to_signed(1000, 14));
```

```
            elsif (signed(td3)+100 <= 0) then
                td3_sampled <= std_logic_vector(to_signed(-100, 14));
            else
                td3_sampled <= td3;
            end if;
            ---td4
            if (signed(td4) >= 111) then
                td4_sampled <= std_logic_vector(to_signed(111, 14));
            elsif (signed(td4) <= 80) then
                td4_sampled <= std_logic_vector(to_signed(80, 14));
            else
                td4_sampled <= td4;
            end if;
        end if;
    end process;

    -- watches the transceivers pll lock signal.
    --latch the tx pll
    process(clk,reset)
    begin
        if (reset = '0') then
            tx_pll_locked_latched <="0";
        elsif (rising_edge(clk)) then
            tx_pll_locked_latched <= tx_pll_locked;
        end if;
```

```
end process;


-- process to wait after the pll is locked, to help stabilize the
   ↪ sequences
process(reset,clk)
variable count:integer range 0 to 255:=0;
begin
     if (reset = '0') then
          locked_and_wait <='0';
          count :=0;
     elsif (rising_edge(clk)) then
          if (tx_pll_locked_latched = "1") then
               if (count < 250 ) then
                    count:=count+1;
               else
                    locked_and_wait <= '1';
               end if;
          end if;
     end if;
end process;
-- a clock indicating where to sample
clk_2M_out_gen:process(reset,clk)
begin
     if (reset = '0') then
          clk_2M_out <= '0';
          --             adc_sync <= '0';
     elsif (rising_edge(clk)) then
```

```
                -- we have a synchronous reset here if the tx pll is not
                   ↪  good
                if (locked_and_wait = '1') then
                     -- Here the High side generating part will start.
                     for i in 39 downto 0 loop
                          if(i + count_integer * 40 < signed(td4_sampled
                             ↪ )*20) then
                               clk_2M_out <= '1';
                               --
                                  ↪ adc_sync <= '1';
                          else
                               clk_2M_out <= '0';
                          --                                  adc_sync <=
                             ↪  '0';
                          end if;
                     end loop;
                end if;
           end if;
      end process;

      compare_HS:process(reset,clk)
      begin
           if (reset = '0') then
                     address_HS <= (others=>'0');
                     adc_sync <= '0';
                elsif (rising_edge(clk)) then
                     -- we have a synchronous reset here if the tx pll
```

```
                    ↪ is not good
            if (locked_and_wait = '1') then
                -- Here the High side generating part will start.
            for i in 39 downto 0 loop
                if(i + count_integer * 40 <= signed(duty_cycle_sampled)) then
                    address_HS(i) <= '1';
                    adc_sync <= '0';
                else
                    address_HS(i) <= '0';
                    adc_sync <= '1';
                end if;
            end loop;
            end if;
        end if;
    end process;

    compare_LS:process(reset,clk)
        begin
        if (reset = '0' OR signed(duty_cycle_sampled) < 50) then
            address_LS <= (others=>'0');
        elsif (rising_edge(clk)) then
            -- we have a synchronous reset here if the tx pll is not good
            if (locked_and_wait = '1') then
            -- Here the High side generating part will start.
                for i in 39 downto 0 loop
```

```
                    if ((i + count_integer * 40 >= signed(duty_cycle_sampled) + signed(td1_sampled)) AND (i + count_integer * 40 <= (signed(td4_sampled)*40-1) - signed(td2_sampled))) then
                        address_LS(i) <= '1';
                    else
                        address_LS(i) <= '0';
                    end if;
                end loop;
            end if;
        end if;
    end process;

    counting:process(reset,clk)
        begin
            if (reset = '0') then
                count_integer <= 0;
            elsif (rising_edge(clk)) then
                count_integer <= count_integer + 1;
                if (count_integer = signed(td4_sampled)) then  -- this coresponds to 1.8 MHz (T=555ns) frequency. or  * 5ns. OR  40bits*1/8Mbps=5ns hence we need 100 frames to generate 555ns
                    count_integer <= 0;
            end if;
        end if;
```

```
    end process;


end rtl;
```