HIGH-PERFORMANCE POWER CONVERTERS FOR TELECOM AND DATACENTER APPLICATIONS

by

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ABSTRACT

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High-Performance Power Converters for Telecom And Datacenter Applications

Thesis directed by Prof. Khurram Afridi

Telecommunication systems and datacenters require compact isolated power converters that maintain high efficiencies across wide operating ranges. This thesis introduces high-efficiency high-power-density isolated dc-dc converters suitable for such applications. These converters are based on the impedance control network (ICN) resonant converter architecture, which enables high performance by achieving soft-switching across wide variations in operating conditions. First, an ICN-based telecom bus converter is developed. The design of this ICN converter is optimized using an enhanced augmented state-space analysis approach. A 1-MHz 550-W prototype of this ICN converter achieves a peak efficiency of 97.6%, maintains >95.3% full-power efficiency across 2:1 ranges of input voltage and output voltage, and >93.6% efficiency across a 10:1 range of output power. Next, an approach to reduce the size of this ICN converter is developed, in which the three inductors of the converter are combined into a single integrated magnetic structure utilizing two coupled windings. The integrated magnetic structure is designed and optimized using 3D finite element analysis. This results in a very high performance 550-W quarter-brick ICN converter prototype, which maintains efficiencies comparable to those described above, while achieving a much higher power density of 462 W/in^3. The ICN converter architecture is then applied to a large step-down conversion application – a single-stage isolated 48V-to-1.8V point-of-load (PoL) converter for datacenters. Three generations of this PoL ICN converter are developed, progressively achieving higher efficiencies and reduced size through innovations in the design of magnetically integrated matching networks and transformers, and through the utilization of transformer and rectifier architectures suitable for providing large voltage step-down. The final 1-

MHz 90-W PoL ICN converter prototype provides up to 33:1 voltage step-down while achieving a peak efficiency of 92.6% and a power density of 314 W/in^3. This thesis also describes an improved approach to optimizing the design of high-efficiency high-gain matching networks, with applications in large-conversion-ratio resonant converters and in wireless power transfer (WPT) systems. Finally, a high-frequency inverter architecture building upon the concepts of the ICN is developed, which compensates for coupling variations in WPT systems while maintaining high power transfer and high efficiency.

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Chapter 1
Introduction

1.1 MOTIVATION

Information and communication technology, which includes telecommunication systems and datacenters, accounts for a large and growing fraction of electricity consumption in the United States (U.S.). For instance, the electricity usage of datacenters was estimated at 70 billion kilowatt-hours (kWh) in 2014 – nearly 1.8% of the total U.S. electricity consumption – and is projected to grow to 73 billion kWh by 2020 [1]. Power conversion losses typically account for more than 10% of a datacenter's electricity consumption, with cooling infrastructure (a significant fraction of which is associated with power converters) accounting for a further 50% [2]. Therefore, efficient power conversion in telecom and datacenter applications is key to saving costs and reducing energy footprint. Furthermore, since most of the physical space in telecommunication systems and datacenters is allocated to the primary objective of data processing, power converters in these applications also need to be compact.

The compactness of a power converter is quantified by its power density, which is defined as the power processed by a converter per unit of the volume it occupies. The volume of a switched-mode power converter, which is a more efficient and flexible alternative to other means of power conversion such as a linear regulator [3], is typically dominated by its energy storage components – inductors and capacitors [4], [5]. For the same amount of power being processed, the size of these components can be reduced (and hence, power density increased) by increasing the converter's switching frequency [6]. However, as the size of a power converter is reduced, it becomes increasingly important to maintain high efficiencies in order to ensure thermal stability and minimize cooling requirements [7]. This challenge is exacerbated by non-ideal switching transitions of the converter's transistors, wherein an overlap between transistor voltage and current causes power dissipation, as illustrated in Figs. 1.1(a) and 1.1(c). These switching losses occur every switching period, and hence, increase proportionally with frequency. Therefore, to

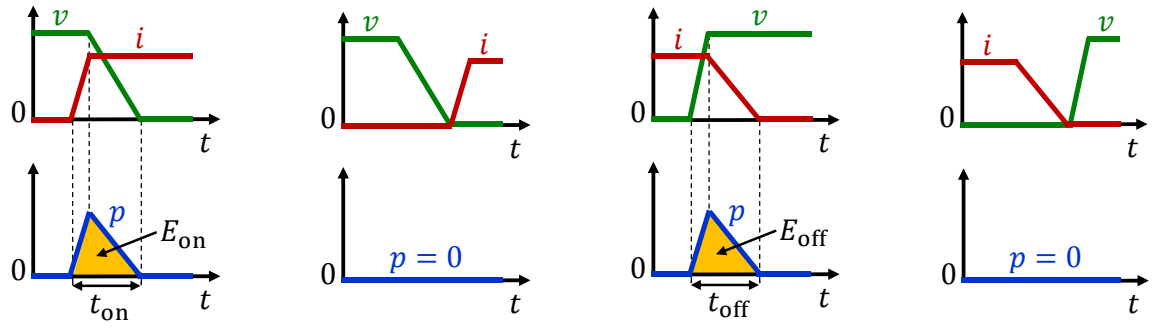
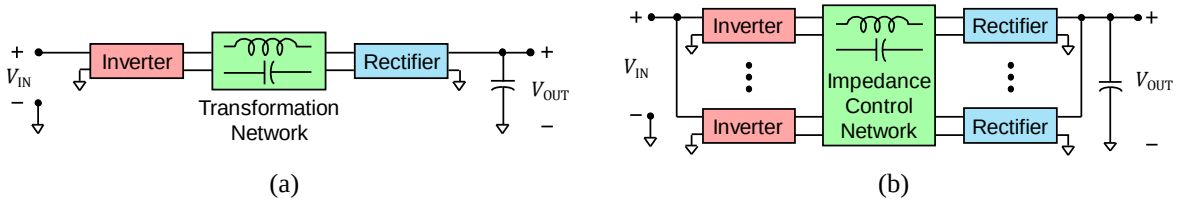


Figure 1.1: Switching transitions of a transistor in a power converter: (a) hard turn on, (b) zero-voltage turn on, (c) hard turn off, and (d) zero-current turn off. Here, v is the voltage across the transistor, i is the current flowing through the transistor, p is the instantaneous power loss in the transistor, E_{on} is the energy lost during the turn-on transition, and E_{off} is the energy lost during the turn-off transition. For simplicity, the transistor is assumed to have zero on-resistance.

simultaneously achieve high power density and high efficiency, increases in switching frequency must be accompanied by techniques that reduce switching losses. Such techniques, broadly termed soft-switching, can be categorized into zero-voltage switching (ZVS) and zero-current switching (ZCS). The ZVS approach ensures that the voltage across a transistor drops to zero before the transistor is turned on and begins to carry current, as shown in Fig. 1.1(b). Similarly, the ZCS approach ensures that the transistor's current drops to zero before it is turned off and begins to block voltage, as shown in Fig. 1.1(d).

In telecom and datacenter applications, power converters also need to maintain high efficiencies across wide operating ranges. For example, typical telecom and datacenter dc-dc converters need to operate across 2:1 or higher ranges of input voltage (as dictated by the state of charge of the backup battery connected at the converter's input), and across 10:1 or higher ranges of output power (as required by the varying power consumption of digital loads) [8]. Unfortunately, conventional soft-switching converters, including resonant converters [9]-[15] and quasi-resonant converters [16]-[22], generally lose ZVS and/or ZCS when operating conditions vary widely. As a result, their efficiency drops rapidly with variations in input voltage, output voltage and/or output power. Therefore, there is a need for soft-switching converter architectures for telecom and datacenter applications that enable high power densities while maintaining high wide-range efficiencies.



(a) (b)

Figure 1.2: Architecture of: (a) a conventional resonant dc-dc converter, and (b) an impedance control network resonant dc-dc converter.

1.2 State of the Art

A recently introduced converter architecture that addresses the challenge of maintaining high efficiencies across wide operating ranges is the impedance control network (ICN) resonant dc-dc converter [23]-[29]. The architectures of a conventional resonant dc-dc converter and that of the ICN dc-dc converter are shown in Fig. 1.2. The conventional resonant dc-dc converter (Fig. 1.2(a)) comprises a high-frequency inverter, a transformation stage containing a resonant network with inductors, capacitors and possibly a transformer, and a high-frequency rectifier. On the other hand, the ICN converter (Fig. 1.2(b)) has multiple inverters, a transformation stage containing a specifically designed resonant network called the impedance control network and possibly a transformer, and one or more rectifiers. The impedance control network is inspired by the concepts of lossless power combiners and resistance compression networks [30]-[32]. Through the specific design of its impedance control network and by utilizing appropriate phase-shifts between its inverters, the ICN converter is able to maintain ZVS and near-ZCS operation across wide ranges of input voltage and output voltage. The converter can also maintain ZVS and near-ZCS across wide ranges of output power, either using burst-mode control [23], [24] or using rectifier phase-shift control [25]-[27]. Hence, this converter architecture enables a high and flat efficiency across wide operating ranges in terms of input voltage, output voltage and power.

A common aspect of the ICN converters presented in [23]-[29] is that they contain at least three discrete magnetic structures (inductors and transformers). This results in a large fraction of their volume being occupied by magnetic components, and limits their power density even at relatively high switching frequencies (500 kHz – 1 MHz). Furthermore, burst-mode controlled ICN converters require bulky input

and output capacitors, further limiting their power density.

1.3 Contributions of the Thesis

This thesis introduces ICN converter topologies and associated design and control techniques that enable high power density while maintaining high efficiencies across wide operating ranges. An important prerequisite to designing a power converter is the ability to model and analyze its steady-state behavior. This is commonly done using circuit simulators such as SPICE. However, when the design of the power converter needs to be optimized for operation across wide ranges of voltage and power, the simulation-based approach becomes time-consuming. In the case of resonant converters, a faster approach to steady-state modeling is fundamental-frequency analysis [10], [33], [34]. In this approach, the resonant network waveforms are approximated by their fundamental components, and switching frequency harmonics are neglected. This modeling method simplifies the design of resonant converters as it converts the nonlinear power converter into an equivalent linear circuit. However, this approach becomes inaccurate when the resonant network waveforms are significantly non-sinusoidal. More accurate modeling approaches that consider higher-order harmonics in the resonant network waveforms have also been proposed [35]; however, these approaches are limited in their accuracy by the number of harmonics considered, and become analytically intractable and computationally intensive when a large number of harmonics are included. A more accurate approach to steady-state modeling of resonant converters is state-plane analysis [36]-[45], which converts the time-domain analysis of resonant converters to geometrical analysis, with network waveforms being described using segments of circles, lines or ellipses. Through such graphical representations, state plane analysis simplifies the exact analysis of complicated resonant network behavior. However, its application is practically limited to simple resonant converters (e.g., with up to two or three elements in the resonant network). To analyze high-order resonant converters with multiple network elements, this method needs to employ complicated higher-dimensional or multiple two-dimensional state planes [43], and becomes difficult to use. A related approach to exact analysis of resonant converters is state-space analysis [9], [46]-[50]. State space analysis identifies the

operating modes of a resonant converter over one switching cycle, and solves the state vectors recursively from one mode to the next. This approach is highly systematic and accurate, and can be generalized to any converter. However, conventional state-space modeling techniques involve solving nonlinear transcendental equations and integration, which require substantial computational effort. An improved state-space based modeling approach, termed augmented state-space analysis, was introduced in [51]. This approach preserves the accuracy and generality of state-space analysis, while enabling steady-state converter waveforms to be obtained with minimal computational effort. A drawback of this approach is that the switching instant of each transistor of the resonant converter must be known in advance. This knowledge is often not available for the rectifier transistors of a resonant converter, which may be implemented as diodes whose switching instants depend on the converter voltages/currents, or as active devices whose switching instants need to be determined to achieve ZVS and near-ZCS. This thesis introduces an enhanced augmented state-space analysis approach that determines such unknown switching instants through an optimized numerical algorithm. The fast convergence of this numerical algorithm ensures that the computational efficiency of augmented state-space analysis is maintained. Furthermore, modeling accuracy is enhanced by incorporating circuit non-idealities such as diode parasitic capacitances. Though general in scope, this enhanced augmented state-space analysis approach is particularly suitable for the modeling and design optimization of topologically advanced resonant converters with high-order resonant networks, an example of which is the ICN converter.

Next, this thesis introduces an ICN dc-dc converter topology ideal for use as an isolated telecom power supply with both step-up and step-down voltage conversion capability. A comprehensive design optimization methodology for this ICN converter is developed. This methodology utilizes the above-described enhanced augmented state-space analysis to accurately determine the impact of circuit parameters such as inductance and capacitance values on the converter's performance over wide ranges of operation, hence, allowing these values to be optimally selected. A prototype 1-MHz, 550-W ICN converter operating over an input voltage range of 36 V to 60 V and producing a regulated output voltage in the range of 34 V to 55 V, suitable as a telecom bus converter, is designed, built and tested. The

prototyped ICN converter achieves a peak efficiency of 97.6% and maintains full-power efficiencies above 95.3% across its full range of input and output voltages. It also maintains greater than 93.6% efficiency across its 10:1 output power range, for the entire range of input and output voltages.

The above ICN converter prototype achieves very high and flat efficiencies, but is limited in its power density due to the use of four discrete magnetic structures. This thesis develops a methodology to reduce the size of the magnetics in an ICN converter by combining its three inductors into a single integrated magnetic structure utilizing two coupled windings. This magnetics integration is conceptualized using a circuit-theoretic modeling approach. The integrated magnetic structure is realized on a custom-designed planar core, and its winding and core are minimized using a 3D finite element analysis (FEA) based design optimization procedure. This results in a very-high-power-density high-efficiency ICN converter. A prototype 1-MHz, 550-W isolated ICN converter with its three inductors implemented as a single planar integrated magnetic structure is designed, built and tested. This converter is designed for the same input and output specifications as those described above. The prototype ICN converter achieves a peak full-power efficiency of 96.7% and maintains greater than 94.8% efficiency at full-power across its nearly 2:1 ranges of input voltage and output voltage. It also maintains above 93.2% efficiency over a 10:1 output power range across its full input and output voltage range. This 550-W prototype conforms to the dimensions of a quarter brick [52] and achieves a power density of 462 W/in^3.

The output voltage and power of most ICN converters, including the ones described above, is regulated using burst-mode (on/off) control [53]-[55], in which the converter is turned on and off at a frequency much lower than its switching frequency. Burst-mode control enables the ICN converter to maintain soft-switching operation across power levels. However, the use of burst-mode control introduces several challenges. For instance, the low-frequency on/off modulation of burst-mode control results in a low-frequency ripple in the output voltage of the ICN converter. Therefore, a large output capacitance is required to regulate the voltage, limiting the converter's power density. Furthermore, the repeated startup and shutdown transients resulting from burst-mode operation lead to reduced partial-power efficiencies. To further improve the power density and efficiency of ICN converters, this thesis introduces a

multimode topology morphing control approach for output voltage and power regulation, in which the rectifier of the ICN converter dynamically alternates between full-bridge and half-bridge topologies. This control approach allows the ICN converter to maintain soft-switching across power levels, while substantially reducing the output capacitance requirement and improving partial-power efficiencies compared to the conventional burst-mode control. These performance enhancements are analytically evaluated and quantified for an example ICN converter design. A closed-loop control architecture for the proposed multimode topology morphing is also introduced, which ensures smooth mode transitions while regulating output voltage across input voltage and load transients. A prototype 1-MHz, 120-W step-down ICN resonant converter designed for an input voltage range of 18 V to 36 V, an output voltage of 12 V, and a 10:1 output power range, suitable as an intermediate bus converter [8] in a telecommunication power distribution system, is built and tested. Compared to burst-mode control, the topology morphing control reduces the output capacitance requirement in the prototype ICN converter by 57% and reduces converter losses at partial power levels by up to 46.5%, validating the analytical predictions. The prototype converter is also tested under closed-loop control, and is shown to successfully regulate its output voltage with smooth mode transitions in the face of input voltage and load variations.

Following the development of high-power-density high-efficiency ICN converters in telecom applications, this thesis targets a datacenter application. Conventionally, server racks in datacenters employ a three-stage power conversion architecture, shown in Fig. 1.3(a). This architecture comprises a front-end ac-dc converter that steps the ac line voltage (single-phase or three-phase depending on the required power level) down to a dc voltage with a nominal value of 48 V. DC-DC converters then step this voltage down to an intermediate bus voltage (typically 12 V), followed by point-of-load (PoL) converters that step the intermediate bus voltage further down to the levels required by digital loads (typically in the range of 0.8 V to 3.3 V). This three-stage architecture allows the power converters in each stage to be individually optimized (for example, the intermediate bus converter may be optimized to provide a fixed step-down conversion ratio, and the PoL converter to provide regulation [56]); however, with increasing power demands and associated power losses, the efficiencies achievable with this

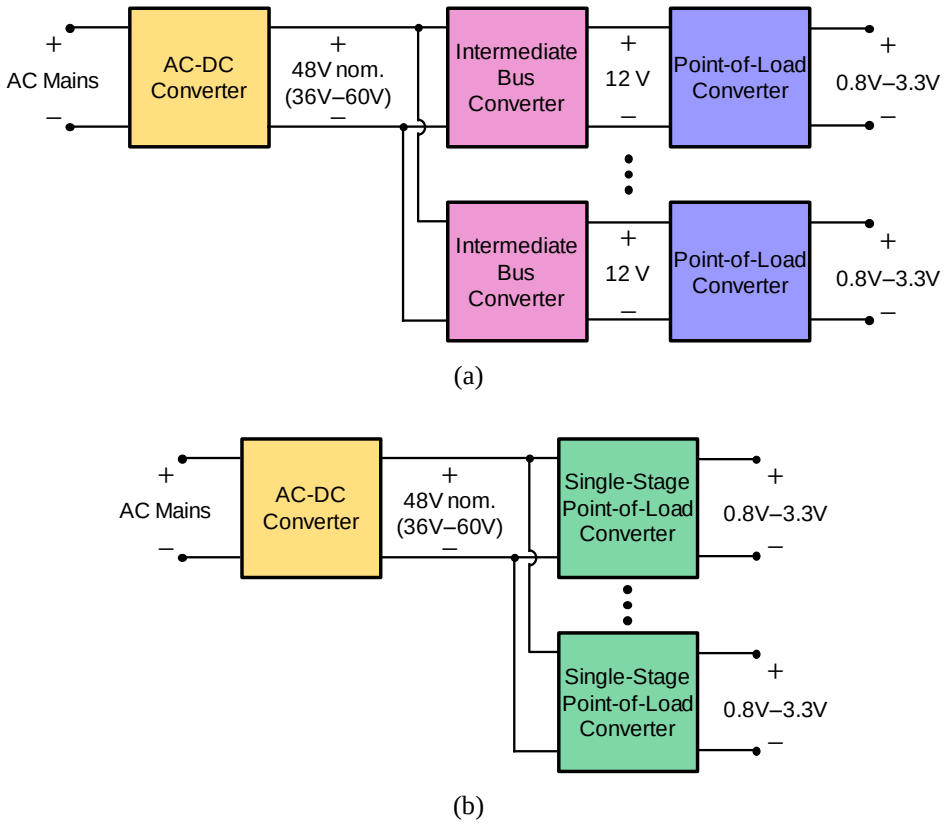


Figure 1.3: Datacenter power distribution architectures: (a) conventional architecture with three power conversion stages in each path from source to load, and (b) modern architecture with one power conversion stage eliminated by replacing intermediate bus converters and point-of-load converters by single-stage point-of-load converters.

architecture are proving to be insufficient. This has driven efforts towards an alternate architecture, shown in Fig. 1.3(b). In this architecture, the intermediate bus converter is eliminated and the 48 V dc voltage is converted directly to the required load voltage using a single-stage PoL converter [57]-[59]. Isolated variants of this single-stage PoL solution have been presented in [60]-[64]. These converters achieve relatively high peak efficiencies; however, their efficiency drops considerably with variations in input voltage and/or output power. The ICN architecture is a natural candidate to address this challenge. To this end, this thesis develops several ICN-based converter topologies suitable for this large step-down datacenter application.

First, an ICN converter that efficiently achieves large step-down using a combination of stacked inverters, a transformer and a current-doubler rectifier is developed. The power density of this converter is enhanced by combining the three inductors of the ICN into a single integrated magnetic structure, as

described earlier. A prototype 250-kHz, 90-W PoL ICN converter utilizing planar PCB-integrated magnetics, designed to operate over an input voltage range of 36 V to 60 V and an output voltage of 1.8 V is built and tested. The prototyped converter achieves a peak efficiency of 88.7%, maintains full-power efficiencies above 87.6% across its nearly 2:1 input voltage range, and above 86.6% efficiency across a 10:1 output power range at its nominal input voltage of 48 V.

Based on the learnings from this converter, a second ICN converter is developed. This converter avoids voltage unbalance issues that arise from stacking inverters, and instead achieves a portion of its large step-down using a resonant immittance network. The inductance of this immittance network is realized using the magnetizing inductance of the transformer, hence, not requiring any additional magnetic component. The power density of this converter is enhanced by combining its magnetic components into two integrated magnetic structures: one implementing the three inductors of the ICN using two coupled windings, and the other implementing the immittance network transformer and current-doubler magnetics on a common core. A systematic methodology is introduced to design and optimize the proposed ICN converter. A prototype 500-kHz, 90-W, 36V-to-60V input, 1.8-V output PoL ICN converter utilizing planar PCB-integrated magnetics is built and tested. The prototype ICN converter achieves a peak efficiency of nearly 90%, maintains greater than 87.9% full-power efficiency across its nearly 2:1 input voltage range, and greater than 86.8% efficiency across its 10:1 power range at its nominal input voltage of 48 V.

To further improve performance, a power loss breakdown of the above ICN converter is performed, and two major sources of loss are identified. The first source, the transformer core losses, are found to be increased by the use of the transformer magnetizing inductance as the inductance of the immittance network. This issue is resolved by utilizing an alternative implementation of the immittance network, one that is functionally equivalent to the original implementation but does not utilize the magnetizing inductance. On the flip side, this immittance network requires two inductors; however, one of these are obtained from the coupling of the ICN inductors, and the other from the leakage inductance of the transformer. Hence, this two-inductance immittance network is realized without the need for any

additional magnetic component. The second major source of loss, the transformer winding losses, are found to be high due to ac (skin- and proximity-effect [3]) losses in the interconnects of the paralleled secondary windings of the transformer. These losses are reduced by employing a distributed transformer structure in which the secondary windings are paralleled after rectification, hence, avoiding ac losses in the interconnects. The resultant ICN converter utilizes only two magnetic structures: one for the coupled inductors and the other for the distributed transformer. To maximize power density, both these magnetic structures are realized using custom core geometries, and designed and optimized using 3D FEA. Power density is further enhanced by regulating the converter's output voltage using rectifier phase-shift control [25]-[27], which eliminates the need for bulky input and output capacitors. These improvements culminate in a high-power-density high-efficiency 48V-to-1.8V PoL ICN converter. A prototype 1-MHz, 90-W, 36V-to-60V input, 1.8-V output PoL ICN converter is built and tested. The prototyped converter achieves a peak efficiency of 92.6%, maintains full-power efficiencies above 91.3% across its nearly 2:1 input voltage range, and greater than 83.9% efficiency across its 10:1 power range at its nominal input voltage of 48 V. The prototyped converter also achieves a power density of 314 W/in^3.

Large-conversion-ratio power converters such as the single-stage PoL ICN converters described above, as well as wireless power transfer (WPT) systems, often require circuit stages that provide voltage/current gain. In systems where isolation is not required (or provided by a transformer) and the switching frequency is relatively narrowband, matching networks can be an efficient means of providing these gains [65]-[87]. When the required voltage/current gains are large, multistage matching networks can be more efficient than their single-stage counterparts. In the conventional approach to designing multistage matching networks [88], each stage is designed to have a purely resistive input impedance and assumed to be loaded by a purely resistive load. This thesis introduces an improved design approach for multistage matching networks comprising L-section stages. The proposed design approach explores the possibility of improvement in efficiency of the network by allowing the L-section stages to have complex input and load impedances. A new analytical framework is developed to determine the effective transformation ratio and efficiency of each stage for the case when input and load impedances may be complex. The

method of Lagrange multipliers [89], [90] is used to determine the gain and impedance characteristics of each stage in the matching network that maximize overall efficiency. Compared with the conventional design approach for matching networks, the proposed approach achieves higher efficiency, resulting in loss reduction of up to 35% for a three-stage L-section matching network. The theoretical predictions are validated experimentally using a three-stage matching network designed for 1-MHz and 100-W operation.

Finally, this thesis introduces a new high-frequency inverter architecture that can compensate for coupling variations in WPT systems while maintaining high power transfer and high efficiency. WPT can reduce the need for energy storage and enhance consumer convenience by enabling autonomous charging in applications ranging from electric vehicles (EVs) [66], [68], [70]-[75], [91]-[95] to portable electronics [96]-[100]. WPT approaches can be categorized into inductive WPT systems, which utilize a pair of magnetically coupled coils, and capacitive WPT systems, which utilize two pairs of electrically coupled plates as their coupler. Both inductive and capacitive WPT systems require circuit components that can compensate for the reactance of their coupler. To achieve effective power transfer, WPT systems need to operate at frequencies close to the resonance frequency of the resonant tank formed by the coupler and the compensation components. When the coupling reactance changes, either due to coupler misalignments or due to variations in the air-gap, so does the resonance frequency. A typically used approach to maintain effective power transfer in this scenario is to track the varying resonance frequency by changing the operating frequency of the system [101]. While this variable-frequency approach is effective, it makes the design of magnetics and gate driver circuitry challenging, as these are difficult to optimize for a wide range of frequencies, particularly when operating in the high-frequency (MHz) regime. Furthermore, in multi-MHz WPT systems, the operating frequency must stay within one of the designated industrial, scientific and medical (ISM) bands (e.g., 6.78 MHz, 13.56 MHz and 27.12 MHz), which have very restrictive bandwidths [102]. Alternative approaches to dealing with coupling variations include the use of banks of switchable capacitors [103], [104], or variable inductors [105] in the compensating network, which allow the resonance frequency to remain roughly unchanged in the event of coupling variations. These approaches also have significant demerits, including additional size, weight and losses, particularly

in high-power WPT systems. The recently introduced active variable reactance (AVR) rectifier [106] mitigates these disadvantages through an innovative rectifier structure that can provide variable compensation at fixed frequency while maintaining high efficiency. However, the AVR rectifier requires several circuit components to be incorporated on the receiving side of the WPT system, where space and weight are at a premium (for instance, on-board an EV or inside a smartphone). To address this challenge, this thesis introduces a high-frequency inverter architecture termed the variable compensation inverter (VCI). This architecture comprises multiple high-frequency inverters feeding a lossless resonant network, with the inputs of the inverters fed by controllable voltages. By appropriately controlling the input voltages of the individual inverters and their relative phase-shift, the VCI can maintain near-resistive, and slightly inductive, loading of the inverters even as the reactance of the WPT coupler changes; hence, providing compensation while maintaining zero-voltage and near-zero-current switching. The VCI also ensures that the output power of the WPT system is maintained at a fixed level even during coupling variations. A prototype VCI is designed, built and tested with a 1.5-MHz 65-W capacitive WPT system for laptop charging applications. The system is able to fully compensate for up to 50% lateral misalignments in the capacitive coupler while maintaining a fixed output power level of 65 W and achieving high efficiency.

1.4 Thesis Organization

The remainder of this thesis is organized as follows: Chapter 2 describes the enhanced augmented state-space analysis approach to modeling resonant converters. Chapter 3 presents the topology and design optimization methodology of the ICN-based telecom bus converter. This chapter also presents experimental results from the 550-W ICN converter prototype. Chapter 4 describes the magnetics integration approach that enables the ICN converter to achieve very high power density, and presents experimental results from the prototype 550-W quarter-brick ICN converter prototype. Chapter 5 describes the multimode topology morphing control approach for power density and efficiency enhancement in ICN converters, and presents experimental results from a step-down ICN converter that

validate the analytical predictions. Chapter 6 describes the development, design and implementation of the first two single-stage isolated 48V-to-1.8V PoL ICN converters. Chapter 7 describes the topology, design and control of the third PoL ICN converter, and presents experimental results from the high-performance prototype of this converter. Chapter 8 describes the improved design optimization approach for high-efficiency matching networks, and provides analytical and experimental comparisons of the matching network efficiencies achieved with this approach as compared to the conventional approach. Chapter 9 describes the architecture and implementation of the variable compensation inverter, and presents experimental results demonstrating the performance of this inverter in a capacitive WPT system. Finally, the conclusions of this thesis are presented in Chapter 10. This thesis also contains seven Appendices. Appendix A describes a generalized procedure to the obtain output power and inverter phase-shift expressions for various ICN converter topologies. Appendix B describes the methodology employed to design the step-down ICN converter presented in Chapter 5. Appendix C derives expressions for the low-frequency output voltage ripple generated by the conventional burst-mode control and the topology morphing control introduced in Chapter 5. Appendix D derives expressions for power losses in the ICN converter under these two control approaches. Appendix E provides derivations for the efficiency of L-section matching network stages as expressed in Chapter 8. Appendix F derives an expression for the asymptotic maximum efficiency of multistage L-section matching networks. Appendix G provides a mathematical basis for the conclusion drawn in Chapter 8 that for certain narrow ranges of gain, single-stage L-section matching networks are more efficient than multistage matching networks.

Chapter 2
Enhanced Augmented State-Space Approach to Steady-State Modeling of Resonant Converters

This chapter presents a highly accurate method to model resonant converters operating in periodic steady-state. This method is applicable to all resonant dc-dc converters, and is particularly well-suited to converters with high-order resonant networks, multiple inverters and/or rectifiers. The proposed approach involves an optimized numerical algorithm that predicts the steady-state converter waveforms with accuracy and computational efficiency. Modeling accuracy is further enhanced through the inclusion of rectifier non-idealities. For validation, the approach is applied to the recently proposed ICN converter [23], which contains a high-order resonant network and multiple inverters. Excellent agreement is shown to exist between the modeled and experimental waveforms.

2.1 Proposed Modeling Approach

The architecture of a typical resonant dc-dc converter is shown in Fig. 2.1. It comprises an inversion stage, a transformation stage that includes a resonant network, and a rectification stage. Within each switching period, the resonant converter operates in multiple modes, each corresponding to a particular configuration of the conduction states (on/off) of the inverter and rectifier switches. In each such mode, the converter can be modeled as a linear circuit excited by dc sources; these modes are henceforth referred to as linear operating modes. For the simple case of a series resonant converter (SRC) with a half-bridge inverter and rectifier, shown in Fig. 2.2(a), the equivalent circuits for each linear operating mode are shown in Fig. 2.2(b). These operating modes apply when the SRC operates above resonance, with the two inverter

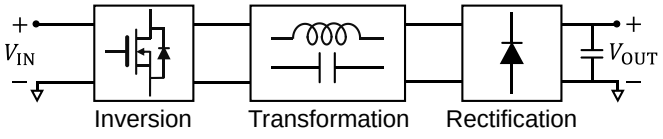


Figure 2.1: Architecture of a typical resonant dc-dc converter.

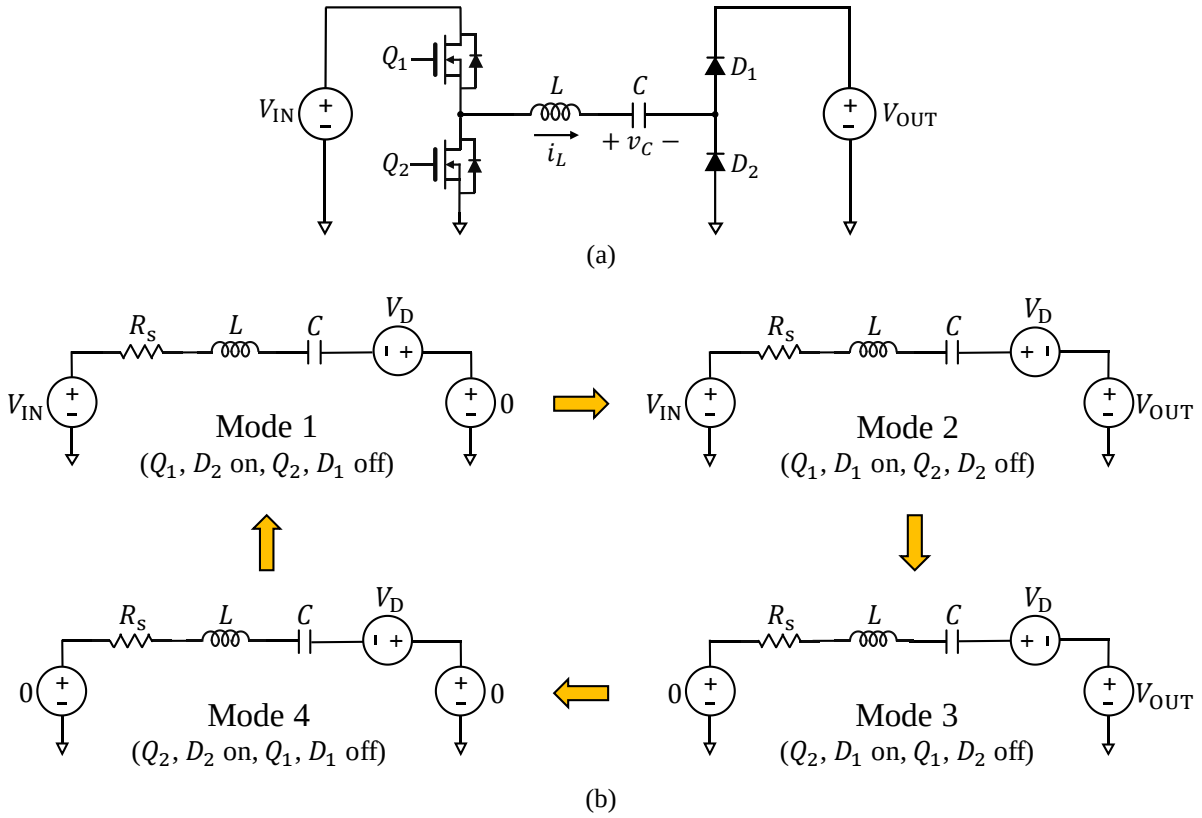


Figure 2.2: A half-bridge input, half-bridge output series resonant converter: (a) topology and (b) equivalent circuit in each linear operating mode.

switches driven alternately at 50% duty ratio. Note that the equivalent circuits incorporate conduction losses modeled as a series resistance, R_s, and the diode forward drop, V_D. It may also be observed from Fig. 2.2(a) that the converter is fed and loaded by voltage sources. The modeling approach described here is not restricted to such a configuration, and remains applicable to converters that are current-fed or current-loaded.

Once the linear operating modes of the resonant converter are identified, the state variables need to be determined. The most meaningful choice for state variables in resonant converters are the resonant network inductor currents and capacitor voltages. In each linear operating mode, the resonant converter can be modeled by the following state equation:

$$\dot{x}(t) = A_k x(t) + b_k \,. \tag{2.1}$$

Here, x is the state vector, k is the linear mode number (i.e., k-th linear mode), A_{k} is the system matrix of the converter in the k-th linear mode, and b_{k} is the input vector of the converter in the k-th mode. To the extent that the circuit elements are considered time-invariant, the state trajectory in the k-th linear mode is given by:

$$x(t) = e^{A_{\mathrm{k}}(t-t_{\mathrm{k}-1})}x_{\mathrm{k}-1} + \int_{t_{\mathrm{k}-1}}^{t} e^{A_{\mathrm{k}}(t-\tau)}b_{\mathrm{k}}\,d\tau\,. \tag{2.2}$$

Here, $t_{\mathrm{k}-1}$ is the time at the end of the $(k-1)$-th linear mode. $x_{\mathrm{k}-1}$ is the state vector at the end of the $(k-1)$-th mode, and hence, the initial state vector for the k-th mode. Using (2.2), the state vector at the end of each linear mode can be expressed as:

$$x_{\mathrm{k}} = e^{A_{\mathrm{k}}d_{\mathrm{k}}T_{\mathrm{s}}}x_{\mathrm{k}-1} + \int_{t_{\mathrm{k}-1}}^{t_{\mathrm{k}}} e^{A_{\mathrm{k}}(t_{\mathrm{k}}-\tau)}b_{\mathrm{k}}\,d\tau \triangleq \Phi_{\mathrm{k}}x_{\mathrm{k}-1} + \Gamma_{\mathrm{k}}\,, \tag{2.3}$$

where d_{k} is the duty ratio of the k-th mode, T_{s} is the converter's switching period, t_{k} is the time at the end of the k-th mode, $\Phi_{\mathrm{k}} = e^{A_{\mathrm{k}}d_{\mathrm{k}}T_{\mathrm{s}}}$ is the state-transition matrix for the k-th mode, and Γ_{k} is the term with the integral that accounts for the effect of the input vector on the evolution of the states. The state trajectories for the full switching period in periodic steady-state operation can be calculated through a recursive application of (2.3) and (2.2), provided the state vector at the beginning of the first linear mode is known.

The preceding analysis is mathematically sound, but requires the time-intensive operation of integration to compute the Γ_{k}'s in (2.3) and the state trajectories in (2.2). An alternative approach is to resolve (2.2) and (2.3) into closed-form expressions involving the inverse of the system matrix (A_{k}^{-1}). However, depending on the converter topology, the system matrix may be singular or ill-conditioned, in which case significant numerical errors may result from inversion. These issues can be mitigated using the augmented state-space technique presented in [51]. In this technique, the state vector and system matrix are augmented as follows:

$$\tilde{x}(t) \triangleq \begin{bmatrix} x \\ 1 \end{bmatrix}, \tag{2.4a}$$

$$\tilde{A}_{\mathrm{k}} \triangleq \begin{bmatrix} A_{\mathrm{k}} & b_{\mathrm{k}} \\ \Theta & 0 \end{bmatrix}. \tag{2.4b}$$

Here, Θ is the zero row-vector of length equal to the size of the system matrix. A new state equation can now be written for the augmented system, and the solution be obtained as under:

$$\dot{\tilde{x}} = \tilde{A}_{\mathrm{k}}\tilde{x}\,, \tag{2.5}$$

$$\tilde{x}(t) = e^{\tilde{A}_{\mathrm{k}}(t-t_{\mathrm{k-1}})}\tilde{x}_{\mathrm{k-1}}\,. \tag{2.6}$$

Here, $\tilde{x}_{\mathrm{k-1}}$ is the augmented state vector at the end of the $(k-1)$-th linear mode. The augmented state vector at the end of the k-th mode is given by:

$$\tilde{x}_{\mathrm{k}} = \tilde{\Phi}_{\mathrm{k}}\tilde{x}_{\mathrm{k-1}}\,, \tag{2.7}$$

where $\tilde{\Phi}_{\mathrm{k}} = e^{\tilde{A}_{\mathrm{k}}d_{\mathrm{k}}T_{\mathrm{s}}}$ is the augmented state-transition matrix for the k-th mode. Equations (2.6) and (2.7) allow the state trajectory to be computed without any integration or system matrix inversion. This technique is very efficient, with the most computationally intensive aspect being the calculation of matrix exponentials, which matrix-based software such as MATLAB can perform in a highly optimized fashion. Further details on this augmented state-space modeling technique, including the computation of the state vector at the beginning of the first linear mode in steady-state operation, can be found in [51].

The augmented state-space modeling technique described above requires that the linear operating mode durations ($d_{\mathrm{k}}T_{\mathrm{s}}$) of the converter be known in advance. This is only possible if the switching instants of all devices (transistors and diodes) in the converter are known before the converter is modeled, which is often not the case. For instance, in the SRC of Fig. 2.2, the switching instants of the rectifier diodes are dependent on the zero-crossings of the resonant tank current. Therefore, the mode durations corresponding to the diode switching transitions are not known in advance. Even in resonant converters that employ synchronous rectification, the switching instants of the rectifier transistors are not known in advance, and in fact, these transistors often emulate diodes in order to achieve soft-switching. The augmented state-space technique cannot be directly applied to such converters. However, the computational advantages that this technique offers are highly desirable. To exploit these advantages, we propose an enhanced augmented state-space approach that can accurately predict converter waveforms without *a priori* knowledge of the

converter's mode durations. The proposed approach involves a numerical algorithm that determines the mode durations of the converter through iterative application of the augmented state-space technique. In principle, such iterations could be performed in an exhaustive, brute-force manner. However, the proposed approach focuses on maintaining high computational efficiency, and utilizes an optimized search to determine the converter's mode durations. The first step in this procedure is to determine the absolute lower and upper bounds for the duration of each mode, based on physical insights into the converter's operation. For instance, referring again to the SRC of Fig. 2.2, the duration of mode 1 must be less than quarter the switching period ($T_s/4$). Any duration of mode 1 greater than $T_s/4$ implies that the average power flow in the converter is in the negative direction (from the output to the input), which is prohibited due to the presence of the rectifier diodes. Therefore, the absolute upper bound on mode 1 duration of the SRC is $T_s/4$ (and the lower bound is 0). Other mode duration bounds can be similarly determined. The next step in the procedure is to obtain the converter waveforms using the augmented state-space technique, with the initial estimate for the mode durations being the average of the absolute upper and lower bounds determined as described above. Based on the polarity of the resonant tank current at the diode switching instants, these mode duration estimates are updated using an optimized search algorithm. The choice of search algorithm depends on the characteristics of the converter. For instance, in the example SRC, it was found that the resonant tank current at the switching instant of the rectifier is a monotonically increasing function of the duration of mode 1. Therefore, a bisection search algorithm is ideally suited for updating the mode durations in this converter. The bisection search algorithm halves the search interval in each iteration, resulting in a significant computational advantage. Furthermore, the greater the required modeling accuracy, the better the bisection search performs relative to an exhaustive search. The search terminates when a solution is found such that the transition times of the rectifier diodes coincide with the zero-crossings of the resonant tank current, within a pre-determined error bound. It may be noted that such an application of an optimized numerical search algorithm for determining converter mode durations is a general approach, and can be easily extended to resonant converters with multiple inverters and/or

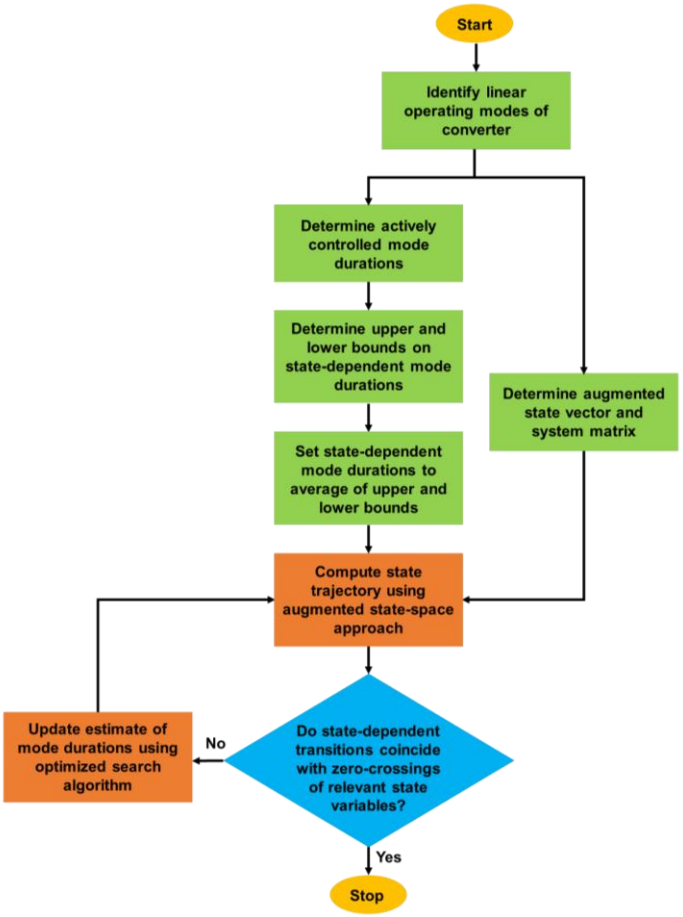


Figure 2.3: Flowchart detailing the proposed modeling approach.

rectifiers and higher-order resonant networks. A flowchart summarizing the steps involved in the proposed modeling approach is shown in Fig. 2.3.

The computational efficiency of the proposed enhanced augmented state-space approach is further improved in cases where converters exhibit half-period symmetry. For instance, in the example SRC, the resonant tank current in the second half of the switching period is equal in magnitude and opposite in polarity to that in the first half. Therefore, the converter waveforms need only be obtained for half the switching period.

This proposed modeling approach is applied to the SRC of Fig. 2.2, operating with 200 V input voltage, 100 V output voltage, and 500 kHz switching frequency. The values of the resonant tank components are $L = 3.84\ \mu\text{H}$ and $C = 37.4\ \text{nF}$. A comparison between the modeled and simulated waveforms of the

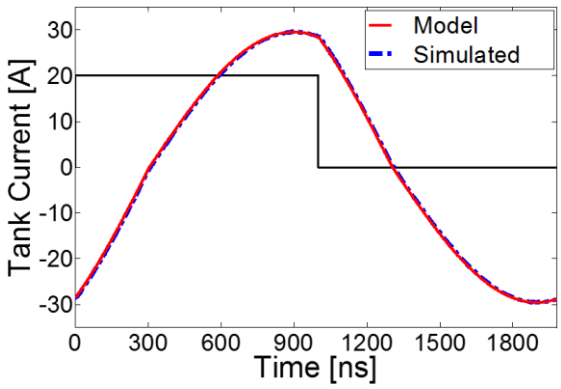
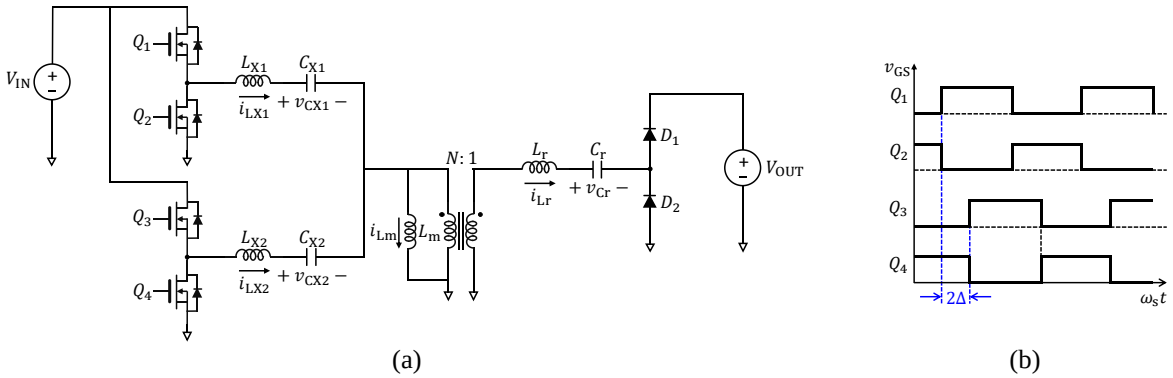


Figure 2.4: Comparison between modeled and simulated tank currents of a half-bridge series resonant converter operating in steady state with 200 V input voltage, 100 V output voltage and 500 kHz switching frequency. Also shown for reference is a scaled version of the inverter output voltage (in black).

resonant tank current is shown in Fig. 2.4. It can be seen that the enhanced augmented state-space approach predicts the resonant tank current to a very high degree of accuracy.

2.2 Application to the Impedance Control Network (ICN) Resonant Converter

As stated earlier, the proposed modeling approach is applicable to multi-inverter, multi-rectifier resonant converters with high-order resonant networks. An example of such a converter is the recently proposed impedance control network (ICN) resonant converter [23]-[29]. The ICN converter utilizes multiple phase-shifted inverters and an impedance control network to maintain high efficiencies across wide operating ranges. The ICN converter introduced in [23] is shown in Fig. 2.5(a). This converter comprises two phase-shifted inverters and a resonant network with three tanks: two at the outputs of the inverters, and the third



(a) (b)

Figure 2.5: The impedance control network (ICN) converter of [23]: (a) topology, and (b), switch gating signals demonstrating the phase-shift between the top and bottom inverters.

on the secondary side of the transformer. The converter is operated at a fixed switching frequency. The gating signals for the inverter switches of this ICN converter are shown in Fig. 2.5(b). As can be seen, all the inverter switches are driven at a fixed (~50%) duty ratio, and the two inverters are driven with a phase-shift of 2Δ between them. In this section, the proposed modeling approach is applied to this ICN converter, and a further enhancement is presented to improve modeling accuracy.

The ICN converter, operated as described above, has six linear operating modes. These modes are identified in Fig. 2.6. An augmented state vector and the corresponding augmented system matrix for the converter are given by (2.8), shown at the top of the next page. In (2.8), the inductor currents and capacitor voltages, and the inductances and capacitances correspond to those shown in Fig. 2.5(a), $\Sigma\mathcal{P}_{\mathrm{L}} = L_{\mathrm{X1}}L_{\mathrm{X2}} + L_{\mathrm{X2}}N^2L_{\mathrm{r}} + N^2L_{\mathrm{r}}L_{\mathrm{X1}}$, $V_{1\mathrm{k}}$ and $V_{2\mathrm{k}}$ correspond to the input-side dc sources and $V_{3\mathrm{k}}$ corresponds to the output-side dc sources in the k-th linear mode, as shown in the circuits of Fig. 2.6. R_{s1}, R_{s2} and R_{s3} represent the parasitic series resistances in the converter circuit, including FET on-resistances, inductor ac winding resistances and capacitor ESRs. Note that the current in the magnetizing inductance of the transformer (i_{Lm}) is included in the state vector. The magnetizing inductance must be included in the

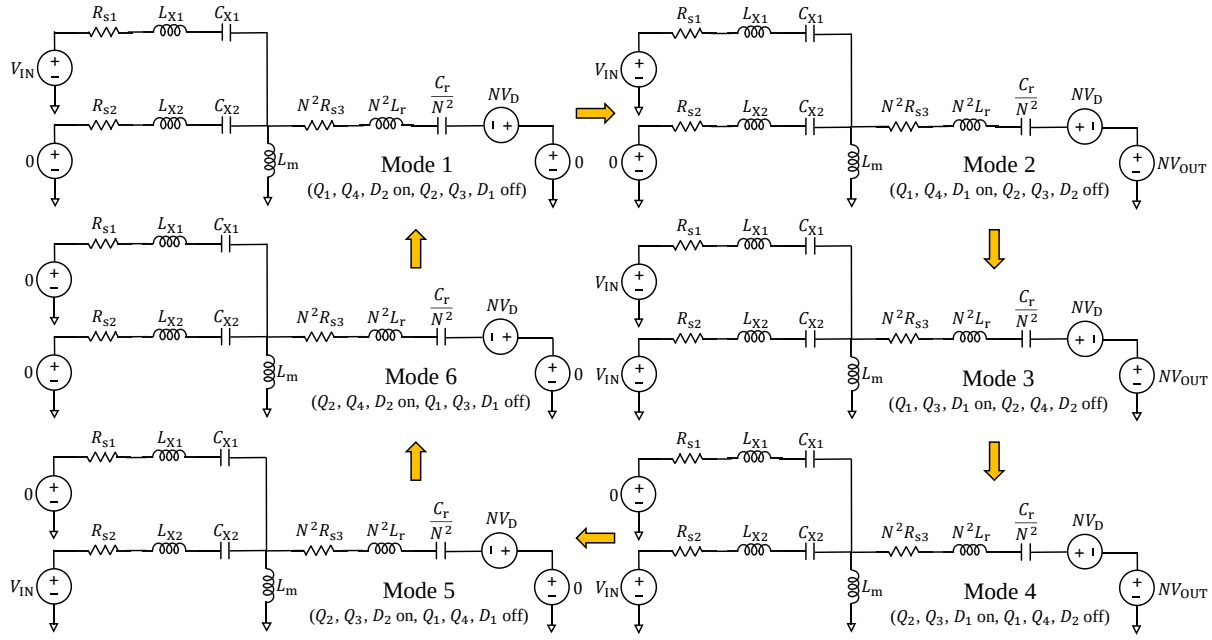


Figure 2.6: The six linear operating modes of the impedance control network (ICN) converter of [23].

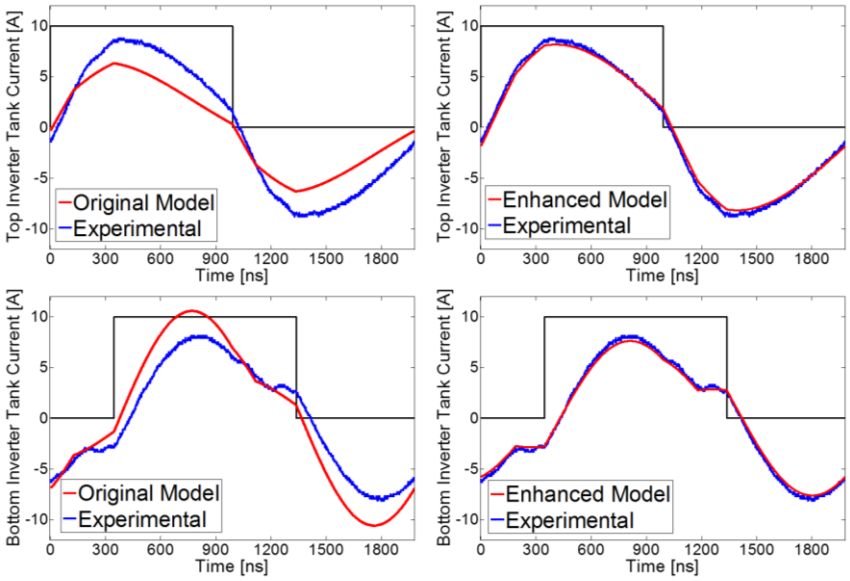
$$\tilde{x} = \begin{bmatrix} i_{\mathrm{LX1}} \\ i_{\mathrm{LX2}} \\ v_{\mathrm{CX1}} \\ v_{\mathrm{CX2}} \\ \frac{v_{\mathrm{Cr}}}{N} \\ i_{\mathrm{Lm}} \\ 1 \end{bmatrix}, \tag{2.8a}$$

$$\tilde{A}_{\mathrm{k}} = \begin{bmatrix} \frac{-(L_{\mathrm{X2}}+N^2L_{\mathrm{r}})R_{\mathrm{s1}}-L_{\mathrm{X2}}R_{\mathrm{s3}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{N^2L_{\mathrm{r}}R_{\mathrm{s2}}-L_{\mathrm{X2}}R_{\mathrm{s3}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-(L_{\mathrm{X2}}+N^2L_{\mathrm{r}})}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{N^2L_{\mathrm{r}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-L_{\mathrm{X2}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & 0 & \frac{(L_{\mathrm{X2}}+N^2L_{\mathrm{r}})V_{1\mathrm{k}}-N^2L_{\mathrm{r}}V_{2\mathrm{k}}-L_{\mathrm{X2}}V_{3\mathrm{k}}}{\Sigma\mathcal{P}_{\mathrm{L}}} \\ \frac{N^2L_{\mathrm{r}}R_{\mathrm{s1}}-L_{\mathrm{X1}}R_{\mathrm{s3}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-(L_{\mathrm{X1}}+N^2L_{\mathrm{r}})R_{\mathrm{s2}}-L_{\mathrm{X1}}R_{\mathrm{s3}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{N^2L_{\mathrm{r}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-(L_{\mathrm{X1}}+N^2L_{\mathrm{r}})}{\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-L_{\mathrm{X1}}}{\Sigma\mathcal{P}_{\mathrm{L}}} & 0 & \frac{-N^2L_{\mathrm{r}}V_{1\mathrm{k}}+(L_{\mathrm{X1}}+N^2L_{\mathrm{r}})V_{2\mathrm{k}}-L_{X1}V_{3\mathrm{k}}}{\Sigma\mathcal{P}_{\mathrm{L}}} \\ \frac{1}{C_{\mathrm{X1}}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_{\mathrm{X2}}} & 0 & 0 & 0 & 0 & 0 \\ \frac{N^2}{C_{\mathrm{r}}} & \frac{N^2}{C_{\mathrm{r}}} & 0 & 0 & 0 & \frac{-N^2}{C_{\mathrm{r}}} & 0 \\ \frac{L_{\mathrm{X1}}L_{\mathrm{X2}}R_{\mathrm{s3}}-L_{\mathrm{X2}}N^2L_{\mathrm{r}}R_{\mathrm{s1}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{L_{\mathrm{X1}}L_{\mathrm{X2}}R_{\mathrm{s3}}-L_{\mathrm{X1}}N^2L_{\mathrm{r}}R_{\mathrm{s2}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-L_{\mathrm{X2}}N^2L_{\mathrm{r}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{-L_{\mathrm{X1}}N^2L_{\mathrm{r}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} & \frac{L_{\mathrm{X1}}L_{\mathrm{X2}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} & 0 & \frac{L_{\mathrm{X2}}N^2L_{\mathrm{r}}V_{1\mathrm{k}}+L_{\mathrm{X1}}N^2L_{\mathrm{r}}V_{2\mathrm{k}}+L_{\mathrm{X1}}L_{\mathrm{X2}}V_{3\mathrm{k}}}{L_{\mathrm{m}}\Sigma\mathcal{P}_{\mathrm{L}}} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{2.8b}$$

modeling procedure in order to correctly predict the dc biases of the capacitor voltages. This is important for the converter's design, as it allows the capacitor voltage ratings to be correctly determined.

The durations of modes 1 and 2 of the ICN converter depend on the zero-crossings of the current in the secondary-side resonant tank, and the absolute lower and upper bounds on these are deduced as follows: with a phase-shift of 2Δ between the two inverters (see Fig. 2.5(b)), the duration of mode 1 is bound between 0 and $\frac{2\Delta}{2\pi}T_{\mathrm{s}}$, where T_{s} is the switching period of the converter. The duration of mode 2 is correspondingly bound between $\frac{2\Delta}{2\pi}T_{\mathrm{s}}$ and 0. Mode 3 has an actively controlled duration of $\frac{T_{\mathrm{s}}}{2} - \frac{2\Delta}{2\pi}T_{\mathrm{s}}$. Owing to half-period symmetry, modes 4 to 6 have the same mode durations and bounds as modes 1 to 3, respectively. With the linear mode durations and bounds identified, the waveforms of the ICN converter are predicted using the enhanced augmented state-space modeling approach outlined in the previous section.

An ICN converter prototype, designed for an input voltage range of 25 V to 40 V and an output voltage range of 250 V to 400 V is built and tested in [23]. The component values used in this prototype are: $N = 0.187$, $L_{\mathrm{X1}} = 1.38\ \mu\mathrm{H}$, $C_{\mathrm{X1}} = 141\ \mathrm{nF}$, $L_{\mathrm{X2}} = 0.84\ \mu\mathrm{H}$, $C_{\mathrm{X2}} = 68\ \mathrm{nF}$, $L_{\mathrm{r}} = 18.8\ \mu\mathrm{H}$ and $C_{\mathrm{r}} = 4.66\ \mathrm{nF}$. Experimental waveforms from this prototype are used to validate the proposed modeling approach. A comparison between modeled and experimental waveforms is shown in Fig. 2.7(a). It can be seen that the



(a) (b)

Figure 2.7: Comparison of modeled and experimental inverter tank currents of the ICN converter operating at an input voltage of 40 V and output voltage of 250 V: (a) with ideal model, and (b) with model including diode non-ideality. Also shown (in black) are scaled versions of the inverter output voltages.

shapes of the model-predicted tank current waveforms are similar to their experimental counterparts; however, there is a significant difference in magnitude between the two. Upon closer examination, this was revealed to be an artifact of the parasitic capacitances of the diodes used in the prototype. The charging and discharging of these capacitances introduces a delay in the switching transitions of the rectifier diodes. Therefore, the mode durations computed using the bisection search algorithm discussed earlier deviate from the experimental values. To improve modeling accuracy, the proposed modeling approach is modified to include the effect of the diode parasitic capacitances. The delay induced by these capacitances can be approximated by:

$$C_{\text{diode}} V_{\text{OUT}} = \int_{t_r}^{t_r+\Delta t_r} N(i_{\text{LX1}} + i_{\text{LX2}})\, dt\,. \tag{2.9}$$

Here, C_{diode} is the diode parasitic capacitance, V_{OUT} is the output voltage of the converter, N is the transformer turns ratio, t_r is the duration of mode 1 of the ICN converter assuming ideal diodes, Δt_r is the delay in the mode duration induced by the diode parasitic capacitance, i_{LX1} and i_{LX2} are the currents in the top and bottom inverter tanks assuming ideal diodes. The currents i_{LX1} and i_{LX2} and the mode duration t_r

are obtained using the numerical algorithm described earlier. A delay of Δt_r is then added to the duration of mode 1, and the other mode durations are correspondingly modified. The converter is solved an additional time with the modified mode durations using the augmented state-space technique. The resulting waveforms for tank currents are shown in Fig. 2.7(b), superimposed on the experimental waveforms. It can be seen that the enhanced model including the effect of the diode parasitic capacitances achieves excellent agreement with the experimental results. This inclusion of rectifier non-ideality in the modeling procedure is applicable to other resonant converters as well. This technique is particularly effective for converters with high output voltage and low output current, in which case the charging and discharging of the diode parasitic capacitances induces significant changes in the converter mode durations.

2.3 Chapter Summary and Conclusions

This chapter presents a highly accurate approach to model the steady-state operation of resonant converters based on an enhanced augmented state-space technique. The proposed modeling approach is applicable broadly but especially suited to resonant converters with high-order resonant networks, multiple inverters and/or rectifiers. The approach involves an optimized numerical algorithm that leverages the computational benefits of augmented state-space modeling to accurately predict converter voltage and current waveforms. Further enhancement in modeling accuracy is achieved through the inclusion of rectifier non-idealities. For validation, this approach is applied to the multi-inverter, multi-element impedance control network (ICN) converter. It is shown that this enhanced augmented state-space model achieves excellent agreement with experimental results. The next chapter will demonstrate how this approach is useful for the comprehensive design optimization of an ICN converter.

Chapter 3
High-Efficiency Impedance Control Network Resonant DC-DC Converter

This chapter introduces a new resonant dc-dc converter topology based on the impedance control network (ICN) converter architecture. This converter maintains very high efficiency by achieving ZVS and near-ZCS across a wide operating range, and is ideal for use as an isolated power supply with both step-up and step-down voltage conversion capability. The performance of this converter is further enhanced through a comprehensive design optimization methodology based on the enhanced augmented state-space analysis approach presented in Chapter 2. A prototype 1-MHz, 550-W ICN converter operating over an input voltage range of 36 V to 60 V and producing a regulated output voltage in the range of 34 V to 55 V, suitable as an isolated bus converter in a telecommunication power distribution system, is designed, built and tested. The prototyped ICN converter achieves a peak efficiency of 97.6% and maintains full power efficiencies above 95.3% across its full range of input and output voltages. It also maintains efficiency above 93.6% across its 10:1 output power range, for the entire range of input and output voltages.

3.1 ICN Converter Topology and Operation

The ICN converter topology proposed here is shown in Fig. 3.1. It comprises two half-bridge inverters, a transformation stage incorporating the impedance control network and a transformer, and a full-bridge synchronous rectifier. The converter is operated at a fixed switching frequency, and all inverter and rectifier transistors are switched at a fixed duty ratio (~50%). The converter's operation can be understood using fundamental frequency analysis. The impedance control network is realized by two series resonant tanks placed at the outputs of the half-bridge inverters, and designed to have equal and opposite reactances, represented by $+jX$ and $-jX$, at the switching frequency. The inverters are operated with a phase-shift between them. When the switching frequency equals the resonant frequency of the series resonant tank

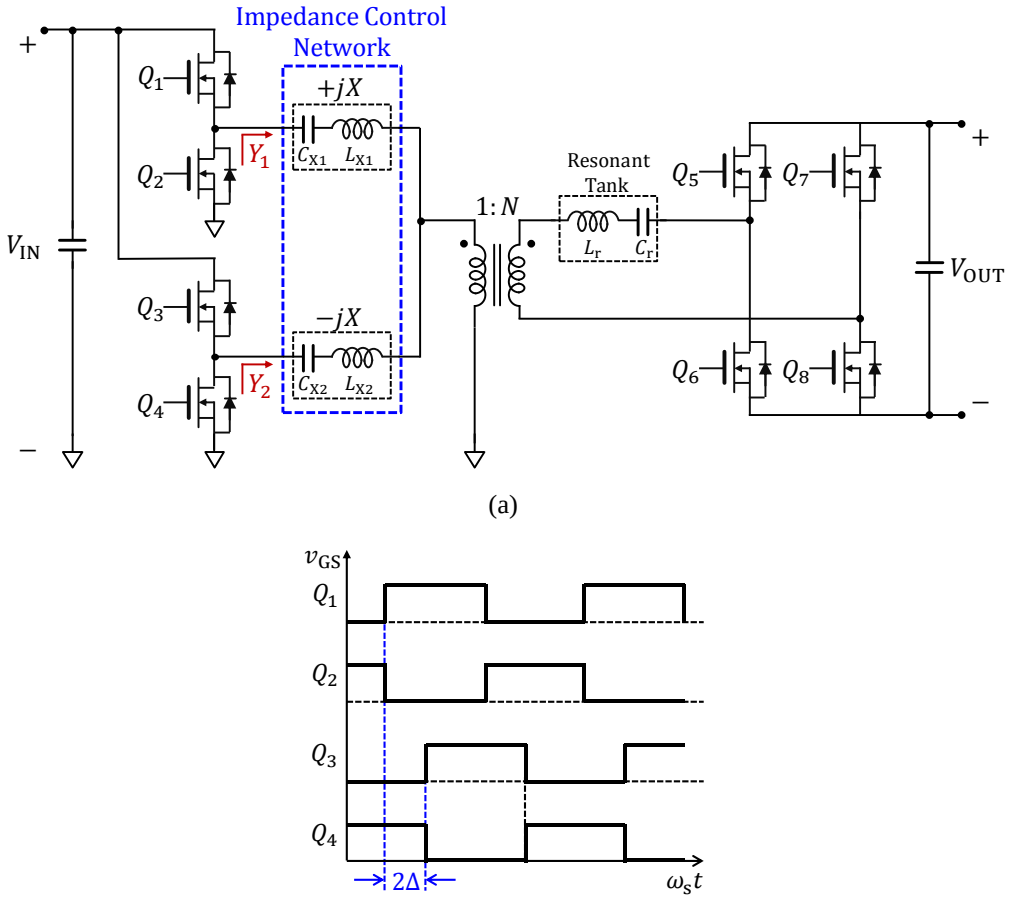


Figure 3.1: Impedance control network (ICN) resonant dc-dc converter: (a) topology, and (b) inverter gating signals.

(shown in Fig. 3.1 on the secondary side of the transformer), and the rectifier transistors are switched at the zero crossings of the resonant tank current (emulating diodes), the admittances seen by the two inverters (Y_1 and Y_2 in Fig. 3.1) are given by:

$$Y_1 = Y_2^* = \frac{2V_{\mathrm{OUT}} \sin \Delta}{NV_{\mathrm{IN}}X} + j\left(\frac{2V_{\mathrm{OUT}} \cos \Delta}{NV_{\mathrm{IN}}X} - \frac{1}{X}\right). \tag{3.1}$$

Here, V_{IN} is the input voltage, V_{OUT} is the output voltage, N is the transformer turns ratio and 2Δ is the phase-shift between the two inverters. The admittance expression in (3.1) is derived in Appendix A. It can be seen from this expression that the imaginary part of the admittances (susceptances) can be made zero or arbitrarily small through proper choice of the inverter phase-shift. This is illustrated in Fig. 3.2. For both

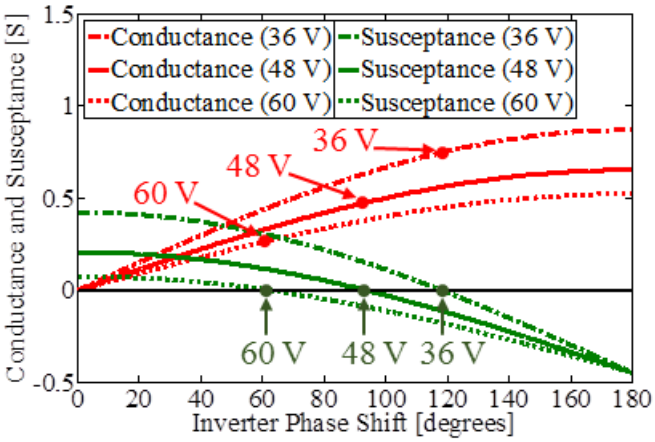


Figure 3.2: Effective conductance and susceptance seen by the two inverters of the ICN converter of Fig. 3.1 as a function of the inverter phase-shift, for three input voltage values: 36 V, 48 V and 60 V, and for an output voltage of 34 V.

inverters to see zero susceptance, the required inverter phase-shift is a function of the input and output voltages, and is given by:

$$2\Delta = 2\cos^{-1}\left(\frac{NV_{\text{IN}}}{2V_{\text{OUT}}}\right). \tag{3.2}$$

This expression for inverter phase-shift also derived in Appendix A.

Thus, as the input and/or output voltages of the converter change, the phase-shift between the inverters is controlled to satisfy (3.2), allowing the admittances seen by the two inverters to be purely conductive across the entire input and output voltage range of the converter. This facilitates zero-current switching of the inverter transistors. In practice, these transistors are implemented as power MOSFETs, which have non-negligible output capacitances, hence, creating the need for zero-voltage switching as well. This is achieved by operating the converter at a switching frequency marginally higher than the design value, so that the impedances seen by the inverters are slightly inductive. Under these conditions, the inverter transistors operate with zero-voltage and near-zero-current switching. Furthermore, since synchronous rectification is used in this topology, the rectifier transistors must also be actively soft-switched. As stated earlier, these are ideally switched at the zero crossings of the resonant tank current, which automatically guarantees zero-current switching. Zero-voltage switching of the rectifier transistors is achieved by delaying the switching of the rectifier slightly to create the necessary phase lag between the resonant tank current and rectifier switch

node voltages. This enables both zero-voltage and near-zero-current switching of the rectifier transistors over the entire operating range. Thus, this ICN converter maintains zero-voltage and near-zero-current switching of all devices over the entire range of input and output voltages, with very low switching losses and minimal circulating energy.

Figure 3.2 demonstrates another desirable characteristic of the proposed ICN converter: the conductance seen by the inverters decreases with increase in input voltage. As a result, in contrast to conventional converter designs where output power is a monotonic function of input voltage, the output power of the ICN converter, operated with the inverters phase-shifted as described above, is inherently a concave function of input voltage, as illustrated in in Fig. 3.3, and mathematically expressed as:

$$P_{\mathrm{OUT,max}} = \frac{4}{\pi^2}\frac{V_{\mathrm{IN}}}{NX}\sqrt{4V_{\mathrm{OUT}}^2 - N^2V_{\mathrm{IN}}^2}\,. \tag{3.3}$$

Operating across an optimal regime of this concave function allows for a relatively flat output power profile, which in turn enables better component sizing.

Figure 3.3 describes the maximum output power capability of the ICN converter. For operation at partial loads, burst-mode (on/off) control [53] is used, in which power is regulated by turning the converter on and off at a frequency much lower than the switching frequency. On/off control allows desirable switching characteristics to be maintained at light loads, and conduction losses back off proportionally to the power

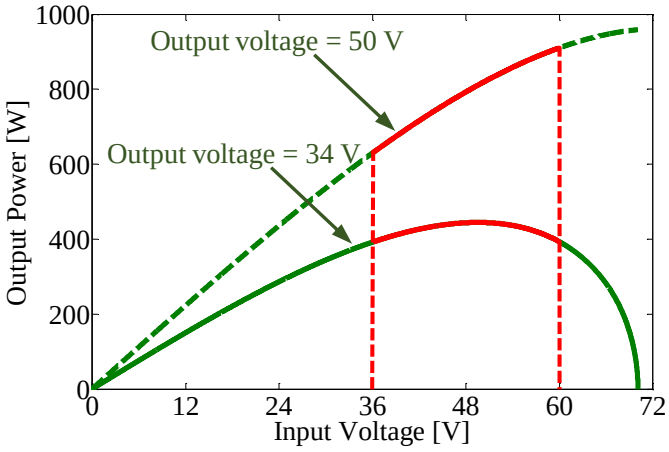


Figure 3.3: Variation in output power as a function of input voltage for the ICN converter of Fig. 3.1 operated with the phase-shift between the two inverters controlled to provide zero effective susceptance of the inverters.

delivered, enabling high efficiency operation over a wide power range. In summary, with the proposed topology we are able to achieve fixed-frequency wide voltage and power range operation at high efficiency.

3.2 Design and Optimization Methodology

The design methodology developed here for the proposed ICN converter is a two-step process. In the first step, two circuit parameters, the transformer turns ratio, N, and the differential reactance of the impedance control network, X, are selected to meet the output power specifications. Given the variation in output power with input voltage (see Fig. 3.3), the need for burst-mode control can be minimized if the converter is designed to deliver the same amount of power at the minimum input voltage $V_{\mathrm{IN,min}}$ and the maximum input voltage $V_{\mathrm{IN,max}}$. Referring again to Fig. 3.3, the output power of the ICN converter increases with output voltage. Therefore, if the converter is designed to provide its rated output power $P_{\mathrm{OUT,rated}}$ at the minimum output voltage $V_{\mathrm{OUT,min}}$, it can meet its power specifications for all input and output voltages. Applying these two design constraints to the output power expression given in (3.3) results in the following closed-form expressions for the transformer turns ratio and the ICN differential reactance:

$$N = \frac{2V_{\mathrm{OUT,min}}}{\sqrt{V_{\mathrm{IN,min}}^2 + V_{\mathrm{IN,max}}^2}}, \tag{3.4}$$

$$X = \frac{4}{\pi^2} \frac{V_{\mathrm{IN,min}} V_{\mathrm{IN,max}}}{P_{\mathrm{OUT,rated}}\big|_{V_{\mathrm{OUT}}=V_{\mathrm{OUT,min}}}}. \tag{3.5}$$

In the second step of the design methodology, the individual elements of the three resonant tanks in the ICN converter (L_{X1}, C_{X1}, L_{X2}, C_{X2}, L_{r} and C_{r}) are determined. L_{X1} and C_{X1} must together realize the impedance $+jX$, L_{X2} and C_{X2} must realize $-jX$, and L_{r} and C_{r} must resonate (that is, together have zero impedance) at the switching frequency. These constraints can be satisfied by infinitely many L-C combinations. One approach to judiciously choosing these combinations, outlined in [23], is to design the tanks to have low loaded quality (Q) factors. Such a low-Q design is highly desirable in that it reduces the inductances required in the resonant tanks, hence, potentially reducing conduction losses; however, the low

quality factors may lead to significantly non-sinusoidal tank currents under some operating conditions, with increased turn-off switching losses. This tradeoff presents an opportunity to select the inductance and capacitance values of the proposed ICN converter in a manner that minimizes overall converter losses. Such a design optimization procedure is presented below.

The non-sinusoidal tanks currents in low-Q designs cannot be predicted using fundamental frequency analysis. Therefore, a more rigorous modeling approach, one that accounts for all harmonics of the switching frequency and is able to exactly predict circuit behavior under all operating conditions is called for. The enhanced augmented state-space analysis presented in Chapter 2 is one such modeling approach. Modeling the converter using this approach allows circuit waveforms of the ICN converter to be obtained for each converter operating condition very quickly and with great accuracy. In the proposed design approach, this technique is exploited in various powerful ways for comprehensive optimization over the wide operating range of the ICN converter. To begin with, it is used to evaluate how turn-off currents in the inverters and rectifier vary as the design of the tanks is changed. Illustrative waveforms obtained from the model are shown in Fig. 3.4, for an operating condition (V_{IN} = 60 V, V_{OUT} = 34 V) at which the inverters and the rectifier carry significantly non-sinusoidal currents. The analytical waveforms of Figs. 3.4(a)-(c) show the variation in the inverter and rectifier turn-off currents as the inductance in the bottom inverter tank (L_{X2}) is changed (along with its series capacitance, C_{X2}, while maintaining the impedance $-jX$), for fixed values of the other inductances and capacitances. It can be seen from Fig. 3.4(b) that the turn-off current in the transistors of the bottom inverter increases sharply as L_{X2} decreases, and from Figs. 3.4(a) and (c) that the top inverter and rectifier turn-off currents also increase. To evaluate the effect of these turn-off currents, turn-off switching losses are calculated as a function of L_{X2} (using the loss model given in [23]), and shown in Fig. 3.4(d). As can be seen, the total turn-off losses decrease as L_{X2} is increased. Similar analyses of all major source of loss (including the inductor and transformer winding and core losses) are performed iteratively for a range of inductance values in all three tanks, and over the entire span of operating conditions. The inductance-capacitance combinations that result in the lowest total converter losses are then selected. In effect, this

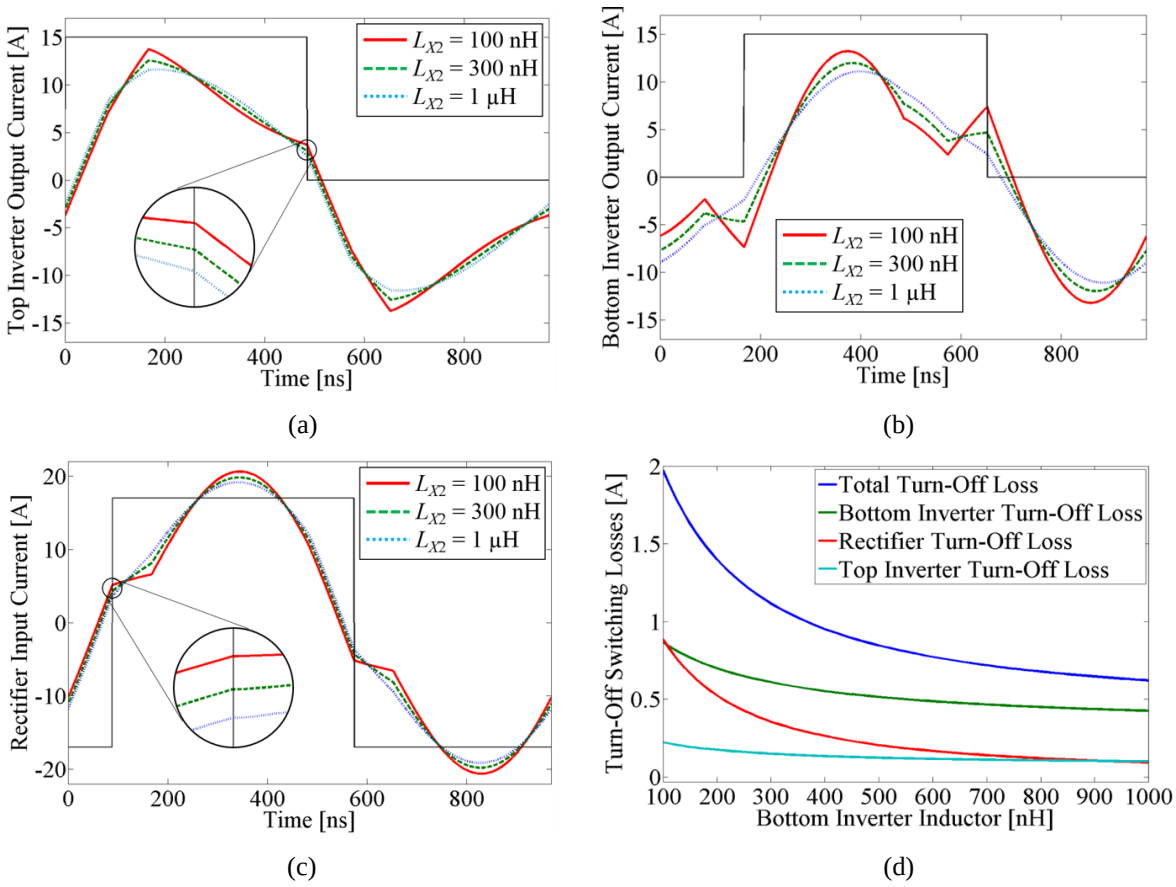


Figure 3.4: Analytical waveforms illustrating the variation in turn-off currents in: (a) the top inverter, (b) the bottom inverter, and (c) the rectifier; and (d) the variation in turn-off switching losses, as the inductance in the bottom inverter tank (L_{X2}) is increased, with the converter operating at 60 V input voltage and 34 V output voltage. Other circuit elements are held constant at: L_{X1} = 450 nH, C_{X1} = 200 nF, L_r = 300 nH, C_r = 81.2 nF. The capacitance C_{X2} is varied along with $L_{X2}$to maintain impedance $-jX$ in the bottom inverter tank. The switching frequency is 1.02 MHz.

approach implements an optimal low-Q design of the ICN converter that further enhances its high-performance potential.

In addition to design benefits, the enhanced augmented state-space analysis based modeling approach has several advantages with regard to the operation of the ICN converter. For instance, it enables us to calculate the exact timing required for the soft-switching of the synchronous rectifier. As mentioned earlier, the transistors of the rectifier must be switched near the zero-crossings of the resonant tank current (with a slight delay) in order to maintain near-ZCS and ZVS operation. Therefore, accurately determining the timing of the zero-crossings of the resonant tank current is critical to the converter's performance. Our analysis has revealed that these zero-crossing times are considerably different from those predicted by the fundamental

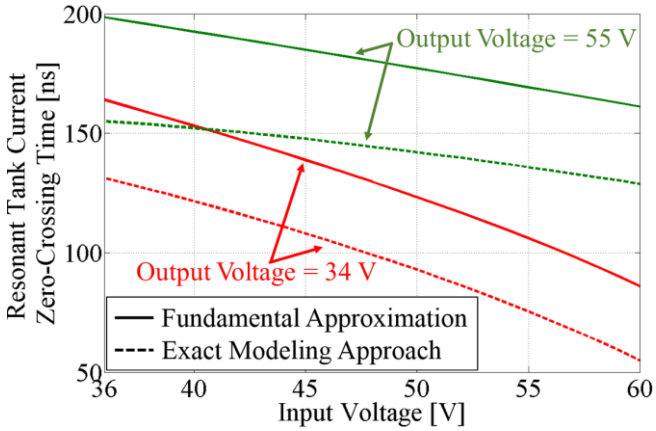


Figure 3.5: Zero-crossing time of resonant tank current (with respect to switching-time of top inverter), as predicted by the fundamental approximation (solid lines), and by the exact modeling technique (dashed lines), for an output voltage of 55 V (green) and 34 V (red).

frequency analysis, and are highly dependent on the operating conditions and tank design. A comparison between the resonant tank zero-crossing times as predicted by the fundamental frequency analysis, and those obtained from our exact modeling approach, is shown in Fig. 3.5 as a function of input voltage, for two output voltage levels. It can be seen that the fundamental-frequency predicted zero-crossing times deviate considerably from their exact counterparts.

Another advantage of the detailed modeling approach is that it allows us to compute the optimum switching dead times to minimize the reverse conduction periods of the transistors. A fourth significant benefit of this approach is the easy evaluation of peak currents and voltages for the full operating range of the converter, allowing us to select appropriate component ratings. These multifaceted performance enhancements demonstrate that the enhanced augmented state-space analysis based methodology is well-suited for the design and optimization of the ICN converter.

3.3 Prototype Design and Experimental Results

A prototype of the ICN resonant converter of Fig. 3.1 has been designed with the following specifications: an unregulated input voltage range of 36 V to 60 V, a regulated output voltage range of 34 V to 55 V, and a maximum output power of 550 W. The converter is designed for a switching frequency of 1 MHz. The circuit element values for the prototype are selected using the design methods detailed in the previous section, and

are listed here: N = 0.97, X = 2.08 Ω, L_{X1} = 450 nH, C_{X1} = 200 nF, L_{X2} = 480 nH, C_{X2} = 30.1 nF, L_r = 300 nH, and C_r = 81.2 nF. The actual components used in the fabrication of the prototype ICN resonant converter are listed in Table 3.1. The core material chosen for the magnetic elements (inductors and transformer) is DMR51W from DMEGC [107]; this material is optimized for low core-loss operation around 1 MHz. The resonant capacitors are 630-V low-ESR ceramic capacitors. For the inverters and the rectifier, EPC 100-V/25-A enhancement-mode gallium nitride (GaN) transistors (EPC2001) are used. These are driven by half-bridge bootstrap drivers designed for enhancement-mode GaN transistors (TI LM5113). The control signals for the converter are generated using a Microchip dsPIC33FJ64GS610, a 16-bit digital signal controller with high-speed PWM outputs. Figure 3.6 shows a photograph of the prototype ICN converter.

TABLE 3.1
COMPONENTS USED IN THE PROTOTYPE ICN RESONANT CONVERTER

Component	Designed Value	Actual Value	Description
$Q_1 - Q_8$	–	–	EPC2001 100-V/25-A eGaN FETs
L_{X1}	450 nH	456 nH	RM14 DMEGC DMR51 (2 turns 6000/48AWG)
C_{X1}	200 nF	227 nF	630-V NP0
L_{X2}	480 nH	481 nH	RM14 DMEGC DMR51 (2 turns 6000/48AWG)
C_{X2}	30.1 nF	29.6 nF	630-V NP0
L_r	300 nH	281 nH	RM14 DMEGC DMR51 (2 turns 6000/48AWG)
C_r	81.2 nF	64.7 nF	630-V NP0
Transformer	1:0.97	1:0.96	RM14 DMEGC DMR51 (Primary 2 turns 6000/48AWG Secondary 2 turns 6000/48AWG Leakage inductance referred to the secondary side: 80 nH)
C_{IN}	2.2 mF × 2	2.2 mF × 2	100-V electrolytic capacitors
C_{OUT}	2.2 mF × 2	2.2 mF × 2	100-V electrolytic capacitors

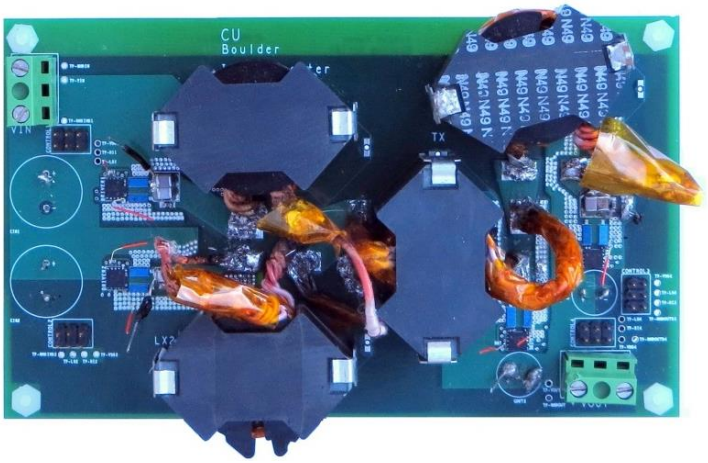


Figure 3.6: Photograph of the prototype ICN resonant converter.

The 1-MHz, 550-W prototype ICN converter has been built and tested. The converter is operated at a switching frequency of 1.02 MHz, slightly higher than the designed value, to ensure slightly inductive loading of the inverters for ZVS. The converter is required to deliver maximum power of 390 W at 34 V output voltage, and the power requirement increases with output voltage, with a maximum power of 550 W required at 55 V output voltage. Figure 3.7 shows the measured waveforms of the ICN converter operating at full power (390 W) at its minimum input voltage (V_{IN} = 36 V) and minimum output voltage (V_{OUT} = 34 V). It is clear from the waveforms of Fig. 3.7 that all the inverter and rectifier transistors operate with ZVS and near-ZCS; in particular, it may be observed that the switching of the rectifier transistors is delayed slightly with respect to the zero crossing of the resonant tank current (labeled as rectifier input current in Fig. 3.7), enabling them to operate with ZVS. Figure 3.8 shows ZVS and near-ZCS turn-off operation for the top and bottom inverters with the ICN converter operating at full power (390 W) at its minimum input voltage of 36 V and maximum input voltage of 60 V, and its minimum output voltage of 34 V. Figure 3.9 further expands upon these waveforms, confirming ZVS operation of the inverters at V_{IN} = 36 V and V_{IN} = 60 V, with V_{OUT} = 34 V. At these two operating points, the rectifier soft-switches with voltage and current waveforms similar to the ones shown in Fig. 3.7. This is because the output power of the converter is identical at the two extreme input voltages at the minimum output voltage level. The converter also achieves soft-

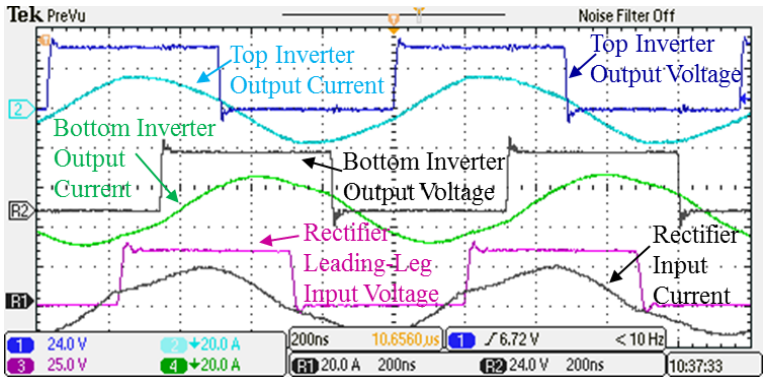


Figure 3.7: Measured waveforms for the ICN resonant converter operating at full power (390 W) at 36 V input voltage and 34 V output voltage. Waveforms shown are the output voltage and output current of both (top and bottom) half-bridge inverters, and the input voltage and input current of the leading leg of the rectifier.

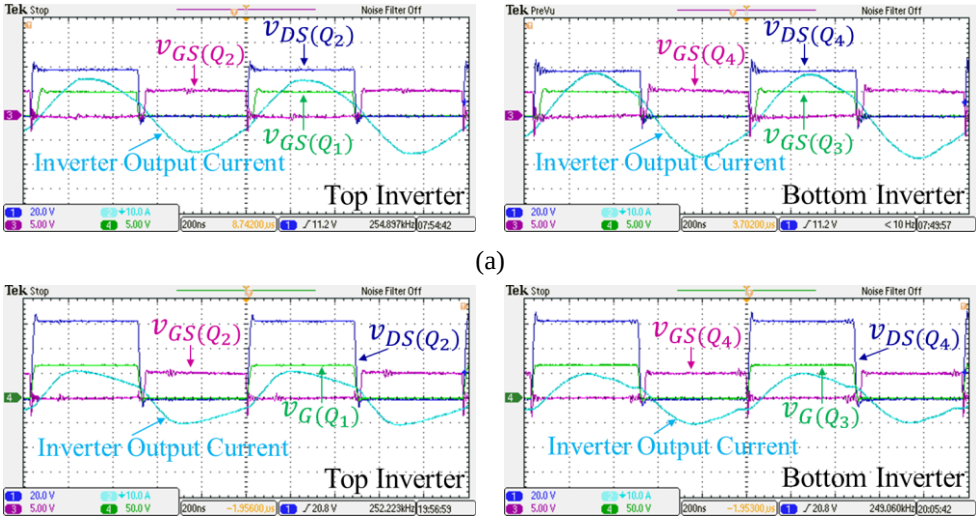
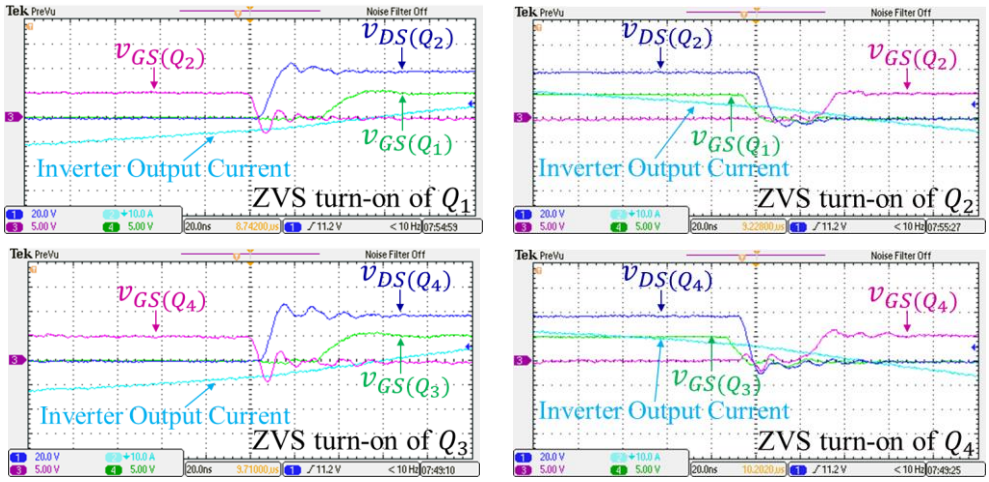


Figure 3.8: Measured waveforms confirming ZVS and near-ZCS operation of the inverters of the ICN resonant converter operating at full power (390 W) at: (a) 36 V input voltage and 34 V output voltage, and (b) 60 V input voltage and 34 V output voltage. Waveforms shown are the output voltage, output current, and gate signals of the two half-bridge inverters.

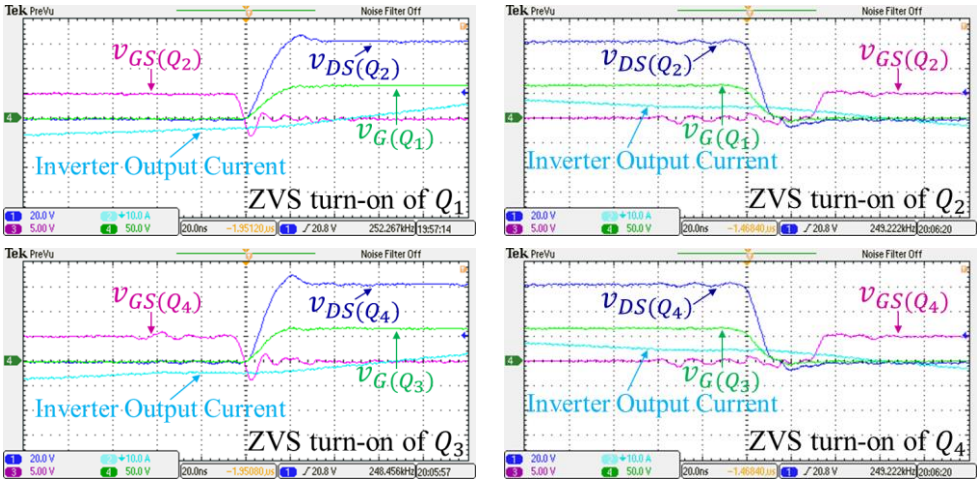
switching at higher output voltage levels. Waveforms confirming ZVS operation of all inverter and rectifier transistors at the maximum output voltage of 55 V, for an input voltage of 36 V, are shown in Figure 3.10.

As mentioned earlier, when the output power of the ICN converter is required to be reduced below its rated level, burst-mode control is used. Figure 3.11 shows an example of converter waveforms under burst-mode control, with the converter operating at its minimum input and output voltages, and delivering 25% of its rated power at this output voltage (nearly 100 W). Magnified views of the top inverter's output voltage and output current waveforms during converter startup and shutdown are also shown in Fig. 3.11. The burst-mode on/off modulation frequency is 1 kHz.

The efficiency of the prototyped converter has been measured across its entire operating range. The measured efficiency is very high and stays fairly flat under variations in input voltage, output voltage and output power. The measured efficiency results of the ICN converter are summarized in Fig. 3.12. The peak efficiency of the converter is 97.6%, and the full power efficiency stays above 96.5% as input voltage is varied across its full range (36 V to 60 V), with the output voltage maintained at its minimum value of 34 V. With the output voltage at its maximum value of 55 V, the full power efficiency stays above 95.3% as the



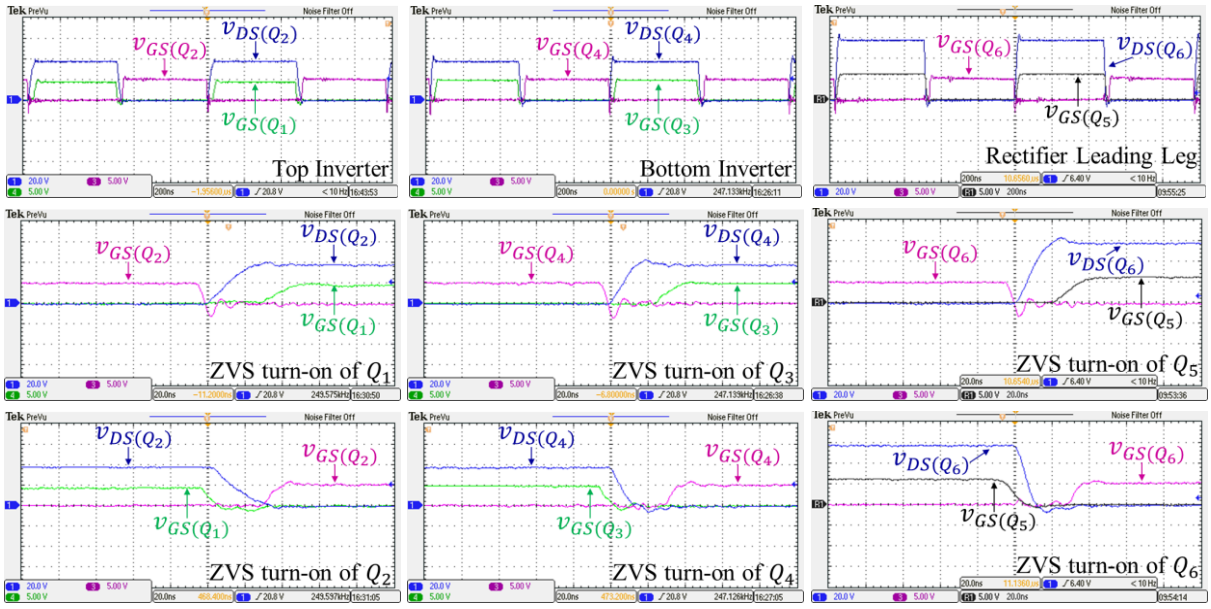
(a)



(b)

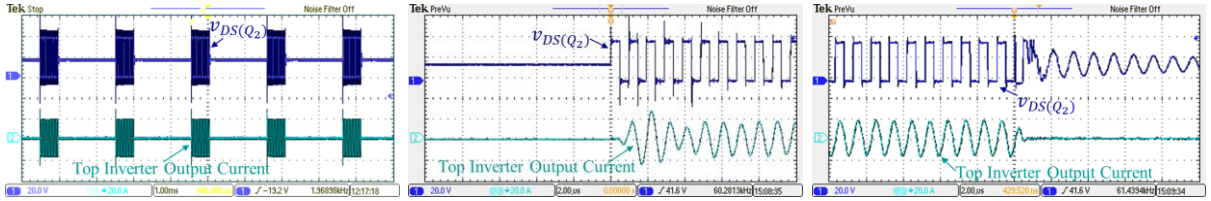
Figure 3.9: Measured waveforms confirming ZVS turn-on operation of the ICN resonant converter operating at full power (390 W) at: (a) 36 V input voltage and 34 V output voltage, and (b) 60 V input voltage and 34 V output voltage. Waveforms shown are the output voltage, output current, and gate signals of the two half-bridge inverters.

input voltage varies. High efficiencies are also achieved with output voltage variation; the converter maintains greater than 96.8% full power efficiency as output voltage is varied between 34 V and 55 V at the maximum input voltage of 60 V, and above 95.3% at the minimum input voltage of 36 V. Under output power variations, the converter records an efficiency of 95% at as low as 55 W (10% of full power), at 60 V input voltage and 50 V output voltage. The prototype ICN converter maintains greater than 93.6% efficiency across its nearly 2:1 range of input and output voltages, and 10:1 range of output power.



(a) (b) (c)

Figure 3.10: Measured waveforms confirming ZVS turn-on operation of the ICN resonant converter operating at full power (550 W) at 36 V input voltage and 55 V output voltage. Waveforms shown are the output voltage, output current, and gate signals of: (a) the top inverter, (b) the bottom inverter, and (c) the leading leg of the rectifier.



(a) (b) (c)

Figure 3.11: Burst-mode operation of the ICN converter delivering 25% of the full power at 36 V input voltage and 34 V output voltage. Waveforms shown are the output voltage and output current of the top half-bridge inverter: (a) long timescale showing multiple startup and shutdown sequences, (b) magnified timescale to show the startup dynamics, and (c) magnified timescale to show the shutdown dynamics.

3.4 Chapter Summary and Conclusions

This chapter presents a new resonant converter topology that utilizes an impedance control network (ICN) to maintain zero-voltage switching (ZVS) and near zero-current switching (ZCS) across wide operating ranges in terms of input and output voltages and output power. A design optimization methodology based on enhanced augment state-space analysis is developed for wide-range efficiency optimization of this ICN converter. A prototype 1-MHz, 550-W ICN resonant converter designed to operate over an unregulated input

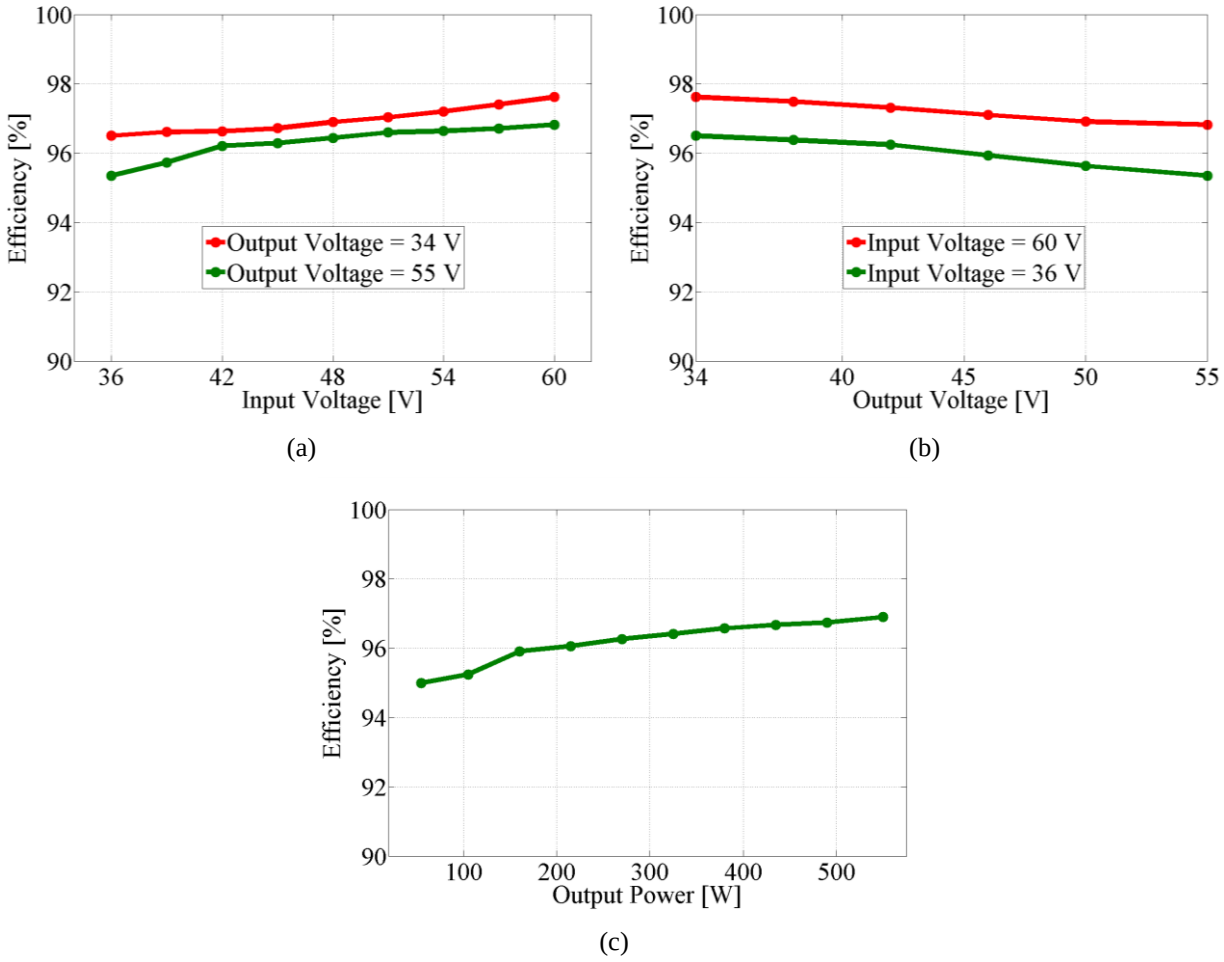


Figure 3.12: Measured efficiency of the ICN resonant converter across variations in: (a) input voltage at output voltages of 34 V and 55V at full power; (b) output voltage with input voltages of 36 V and 60 V at full power; and (c) output power with input voltage of 60 V and output voltage of 50 V.

voltage range of 36 V to 60 V and regulated output voltage range of 34 V to 55 V, suitable as an isolated telecom bus converter, is built and tested. It is shown that the converter achieves a peak efficiency of 97.6% and maintains full-power efficiency above 95% across its entire input and output voltage range. Furthermore, the converter maintains greater than 93.6% efficiency over a 10:1 range of output power across its full range of input and output voltages. These results demonstrate the capability of this ICN converter to maintain high efficiencies over wide ranges of operation. However, the power density of the prototype ICN converter presented in this chapter is limited to 21 W/in^3 due its use of four discrete magnetic components. The next chapter describes an approach to substantially increasing the power density of this ICN converter while maintaining high efficiency.

Chapter 4
High-Power-Density High-Efficiency Impedance Control Network Resonant DC-DC Converter

This chapter introduces a high-power-density high-efficiency ICN resonant dc-dc converter. Similar to the ICN converter presented in Chapter 3, this ICN converter maintains very high efficiency by achieving ZVS and near-ZCS across a wide range of input voltages, output voltages and output power. High power density is achieved by combining the three inductors of the ICN converter into a single integrated magnetic structure with two coupled windings, and by realizing this integrated magnetic structure and the converter's transformer as planar structures. Power losses in the integrated magnetic structure and transformer are minimized using a finite element analysis (FEA) based design optimization approach. A prototype 550-W, 1-MHz ICN converter incorporating a planar integrated magnetic structure and a planar transformer, both having printed circuit board (PCB) windings, designed to operate over an input voltage range of 36 V to 60 V and an output voltage range of 34 V to 55 V is built and tested. The prototyped ICN converter achieves a power density of 462 W/in^3, a peak efficiency of 96.7% and maintains efficiencies above 93.2% across its entire operating range.

4.1 Magnetics Integration Approach for ICN Converter

The series resonant tank (comprising L_r and C_r) on the transformer's secondary side in the ICN converter of Fig. 3.1 can be moved to the transformer's primary side, as shown in Fig. 4.1. The ICN converter of Fig. 4.1 is electrically equivalent to the ICN converter of Fig. 3.1 provided the magnetizing inductance of the transformer is large, and the inductance and capacitance values of the series resonant tank are scaled by the square of the transformer turns ratio (that is, $L_\mathrm{rp} = L_\mathrm{r}/N^2$ and $C_\mathrm{rp} = N^2 C_\mathrm{r}$). It can be seen that the three

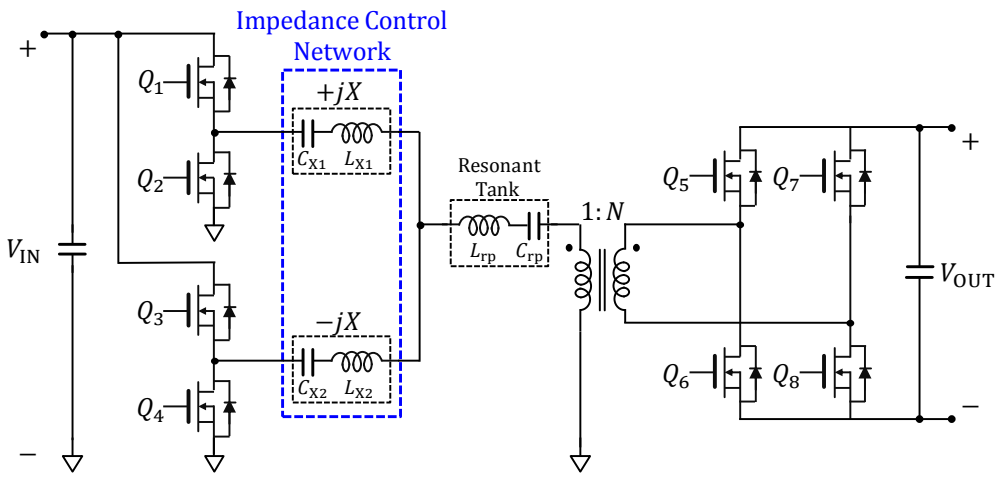


Figure 4.1: Impedance control network (ICN) resonant dc-dc converter with its three inductors connected at a common node, forming a T- network.

inductors L_{X1}, L_{X2} and L_{rp} in the ICN converter of Fig. 4.1 are connected at a common node, forming a T-network. A T-network of inductors is an equivalent circuit representation for a pair of coupled windings [108], [109], as shown in Fig. 4.2. The pair of coupled windings can be modeled as a two-port network with the following inductance matrix:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & M \\ M & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{4.1}$$

Here v_1, i_1 and v_2, i_2 are the terminal voltages and currents of the two-port network (as illustrated in Fig. 4.2), L_{11} and L_{22} are the self inductances of the two coupled windings, and M is their mutual inductance. The three inductors of the equivalent T-network in Fig. 4.2 can be expressed in terms of these self- and mutual inductances as:

$$L_1 = L_{11} - M. \tag{4.2a}$$

$$L_2 = L_{22} - M. \tag{4.2b}$$

$$L_3 = M. \tag{4.2c}$$

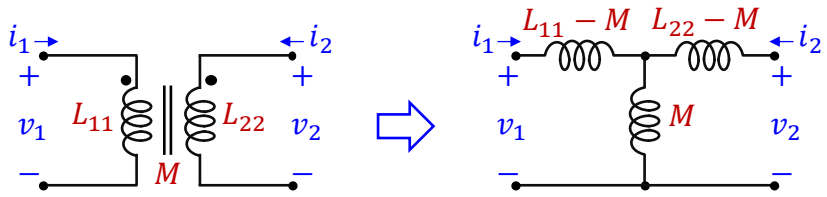


Figure 4.2. Modeling of two coupled windings by a T-network of inductors.

Reversing the equivalent circuit representation shown in Fig. 4.2, the T-network of inductors in the ICN converter of Fig. 4.1 (formed by L_{X1}, L_{X2} and L_{rp}) can be realized using two coupled windings, as shown in Fig. 4.3. As can be seen from Fig. 4.3(a)-(c), there are three topologically distinct ways of implementing the two coupled windings. Using (4.2), the self and mutual inductances of the coupled windings in these three configurations can be expressed in terms of the inductances L_{X1}, L_{X2} and L_{rp}, as:

$$\left.\begin{aligned} L_{11} &= L_{X1} + L_{rp} \\ L_{22} &= L_{X2} + L_{rp} \\ M &= L_{rp} \end{aligned}\right\} \text{ for Fig. 4.3(a),} \tag{4.3a}$$

$$\left.\begin{aligned} L_{11} &= L_{X1} + L_{X2} \\ L_{22} &= L_{rp} + L_{X2} \\ M &= L_{X2} \end{aligned}\right\} \text{ for Fig. 4.3(b),} \tag{4.3b}$$

$$\left.\begin{aligned} L_{11} &= L_{X2} + L_{X1} \\ L_{22} &= L_{rp} + L_{X1} \\ M &= L_{X1} \end{aligned}\right\} \text{ for Fig. 4.3(c).} \tag{4.3c}$$

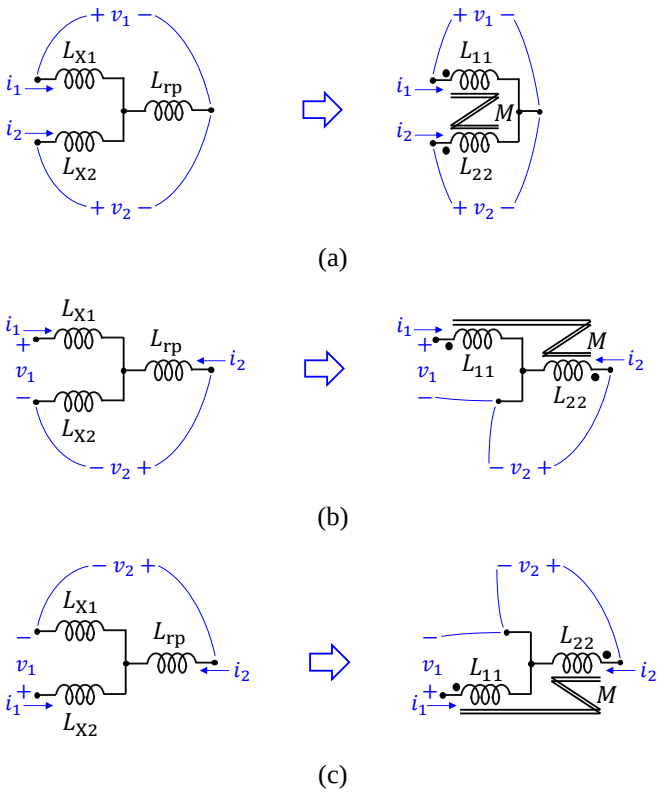


Figure 4.3: Realization of the three inductors of the ICN converter using two coupled windings in three topologically distinct ways. In (a), $L_{X1} = L_{11} - M$, $L_{X2} = L_{22} - M$ and $L_{rp} = M$; in (b), $L_{X1} = L_{11} - M$, $L_{X2} = M$ and $L_{rp} = L_{22} - M$; and in (c), $L_{X1} = M$, $L_{X2} = L_{11} - M$ and $L_{rp} = L_{22} - M$.

The three coupling configurations of Fig. 4.3 result in the three ICN converter topologies shown in Fig. 4.4. In each of these converters, the coupled windings can be implemented in a single integrated magnetic structure. Therefore, compared to the ICN converter of Chapter 3 that requires three discrete inductors, each ICN converter in Fig. 4.4 requires two fewer magnetic components, enabling significant size reduction.

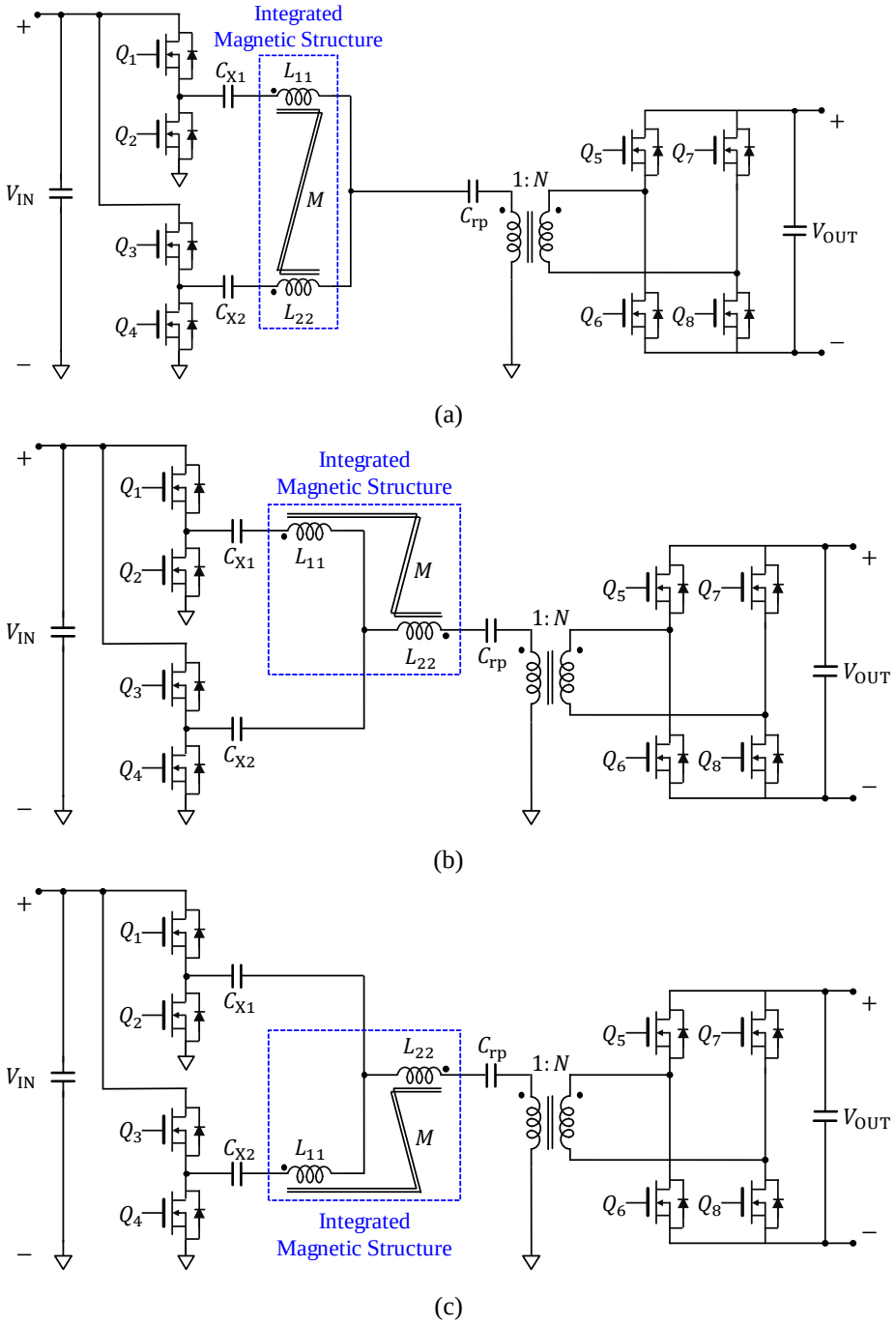


Figure 4.4: The three ICN converter topologies resulting from the coupling configurations of Fig. 4.3.

Depending on the ICN converter's operating regime in terms of input voltage, output voltage and power, one of the three topologies of Fig. 4.4 may be more efficient than the others. In each topology, the two coupled windings carry phase-shifted currents. The magnitude of these currents and the phase-shift between them depends on the topology. For example, in the topology of Fig.4.4(a), the two windings carry the two inverter output currents, whose magnitudes are ideally equal, and whose phase-shift is approximately equal to the inverter phase-shift 2Δ (assuming near-resistive loading of the inverters). On the other hand, in the topologies of Figs. 4.4(b) and (c), one winding carries an inverter output current, while the other winding carries the transformer primary current. Depending on the converter's operating point, the inverter output current may be higher or lower than the transformer primary current. Also, assuming the two inverter output currents are equal in magnitude and phase-shifted by 2Δ, the phase-shift between an inverter output current and the transformer primary current (which is the sum of the two inverter output currents) is equal to half the inverter phase-shift (i.e., Δ). These differing current magnitudes and phase-shifts can lead to different winding and core losses in the integrated magnetic structure of the three ICN converter topologies of Fig. 4.4. Therefore, the optimal topology may change based on the specifications of the converter. All three topologies were designed for the voltage and power specifications considered here (using the methodology described in the following two sections), and the worst-case total (winding + core) losses were found to be minimum for the topology of Fig. 4.4(b).

4.2 Integrated Magnetic Structure Design

To facilitate the design of the single integrated magnetic structure used to realize the three inductors of the ICN converter, a magnetic circuit representation of the structure is developed, as shown in Fig. 4.5(a). In this magnetic circuit model, the two coupled windings are modeled as mmf sources: $\mathcal{F}_1$ and $\mathcal{F}_2$. This magnetic circuit has three flux paths: two primary flux paths that carry the flux generated by each winding (Φ_1 and Φ_2), and a differential flux path that carries the difference in the flux of the two windings ($\Phi_1 - \Phi_2$). The self and mutual inductances of the integrated magnetic structure are related to the physical parameters of the structure as follows:

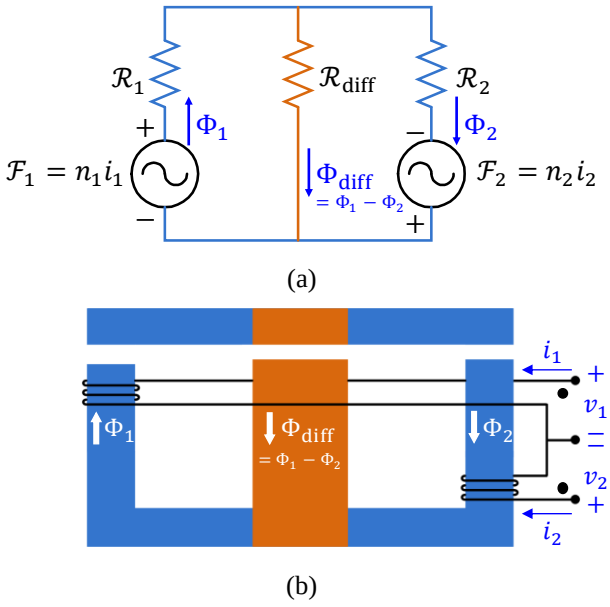


Figure 4.5: Proposed approach for realization of the integrated magnetic structure: (a) magnetic circuit, and (b) implementation. The primary flux paths are shown in blue, and the differential flux path is shown in orange.

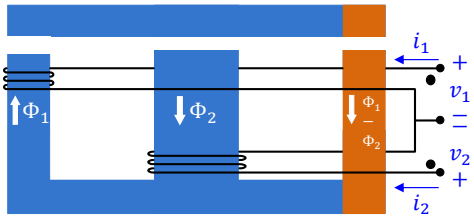
$$L_{11} = \frac{n_1^2}{\mathcal{R}_1 + (\mathcal{R}_2 \| \mathcal{R}_{\text{diff}})}, \tag{4.4a}$$

$$L_{22} = \frac{n_2^2}{\mathcal{R}_2 + (\mathcal{R}_1 \| \mathcal{R}_{\text{diff}})}, \tag{4.4b}$$

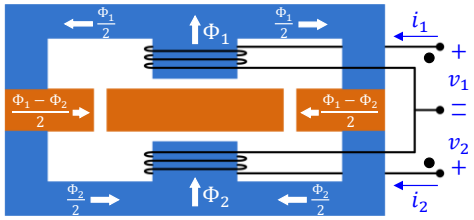
$$M = \frac{n_1 n_2}{\left(\mathcal{R}_1 + \mathcal{R}_2 + \frac{\mathcal{R}_1 \mathcal{R}_2}{\mathcal{R}_{\text{diff}}}\right)}. \tag{4.4c}$$

Here $\mathcal{R}_1$ and $\mathcal{R}_2$ are the reluctances of the primary flux paths, $\mathcal{R}_{\text{diff}}$ is the reluctance of the differential flux path, and n_1 and n_2 are the number of turns in the two windings. Multiple combinations of these five physical parameters can be used to realize the required self and mutual inductances, as will be discussed in the next section.

The magnetic circuit of Fig. 4.5(a) can be implemented using the integrated magnetic structure shown in Fig. 4.5(b). The reluctances of the three flux paths in this structure are controlled by inserting air-gaps in the three core legs. The two windings are wound on the outer legs of the core, which serve as the primary flux paths, while the center leg serves as the differential flux path. Note that one of the windings can also be wound on the center leg, in which case one of the outer legs would serve as the differential flux path, as shown in Fig. 4.6(a). Such an implementation is more volume-efficient, since the two windings share one



(a)



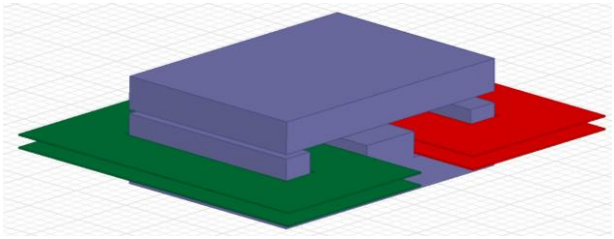
(b)

Figure 4.6: Alternative implementations of the integrated magnetic structure with: (a) differential flux path on side leg of E core, and (b) horizontally layered flux paths.

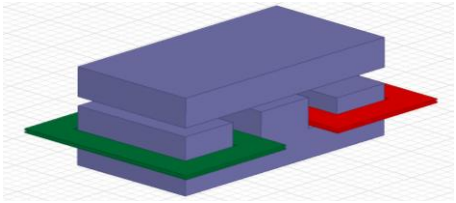
of the core windows. However, due to the closer proximity between the two windings, this implementation is also likely to suffer from higher ac winding losses. Another candidate implementation of the integrated magnetic structure is shown in Fig. 4.6(b). Here, the flux paths are layered horizontally. This implementation – on similar lines to those explored in [110] – allows the core to carry smaller flux than in the implementation of Fig. 4.5(b), hence, resulting in lower core losses. However, the implementation of Fig. 4.6(b) is difficult to fabricate and assemble, and is not suited for a planar implementation where the two windings are constructed from traces on the same printed circuit board (PCB). Owing to its lower winding losses than the implementation of Fig. 4.6(a), and easier planar PCB realization than the implementation of Fig. 4.6(b), the implementation of Fig. 4.5(b) is selected here. The geometry of this integrated magnetic structure is optimized using 3D finite element analysis, as described in the following section.

4.3 Design Optimization Using Finite Element Analysis

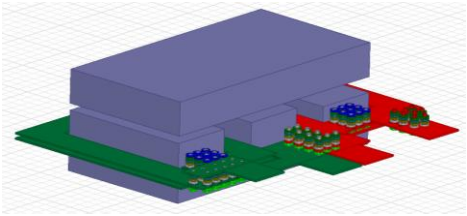
A planar PCB implementation of the integrated magnetic structure is used in the proposed ICN converter, which is designed for the same specifications as those described in Chapter 3: an input voltage range of 36 V to 60 V, an output voltage range of 34 V to 55 V, and a maximum output power of 550 W. To achieve a



(a)



(b)



(c)

Figure 4.7: 3D finite element analysis based design optimization of the integrated magnetic structure: (a) initial core and winding geometry, (b) optimized geometry and (c) optimized geometry as implemented in a printed circuit board, including vias and winding terminals.

high power density, upper limits are imposed on the magnetic structure's height and the board area it occupies. The design of the core and the windings is then optimized to minimize the magnetic structure's size while remaining within prescribed temperature limits. The converter operating point where the winding and core losses are expected to be maximum – the minimum input voltage and maximum output voltage of the ICN converter (where the inverter output currents are the highest) – is used in the optimization process. Finite element analysis (FEA) using Ansys Maxwell 3D is employed to determine field and current distributions and accurately predict winding and core losses. First, a baseline core and winding geometry is selected with area and height equal to the chosen upper limits. Initial values for the number of turns (n_1, n_2) are also chosen and appropriate air-gap lengths are determined to achieve the reluctance values ($\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_{\text{diff}}$) needed to realize the required self and mutual inductances, as given by (4.4). Such an initial integrated magnetic structure having an EI geometry is shown in Fig. 4.7(a). Next, the winding and core

losses as well as the temperature rise in this structure are computed. The design is iterated by varying the number of turns in each winding and the core core-sectional area until further reduction in winding and core losses is not achievable. If the resultant temperature of this design is below the specified limit, then the size of the magnetic structure is reduced and the procedure repeated until no further reduction in size is possible. The final optimized magnetic structure design obtained from this procedure is shown in Fig. 4.7(b). The optimized structure has a length of 23 mm, a width of 12 mm and a height of 8.6 mm (including air-gaps), and all three legs of the E-half of the structure have an equal width of 5.5 mm. Both the windings have two turns in this optimized design.

The total losses in the optimized magnetic structure of Fig. 4.7(b) are 4.2 W, compared to 7.1 W in the initial configuration of Fig. 4.7(a), representing a 41% reduction in losses. To predict the losses in the optimized structure with greater accuracy, the windings are laid out in a PCB design tool and imported into Maxwell using Ansys ALinks for EDA. This PCB-extracted winding and core configuration is shown in Fig. 4.7(c). Simulating the structure at the layout level enables additional modes of loss, such as the effect of PCB vias and terminal connections, to be captured. It is found that these higher-order effects have a non-negligible impact on the performance of the integrated magnetic structure. The total losses in the PCB-extracted structure are 5.1 W, around 20% higher than the simpler version without vias and terminations.

4.4 Prototype Design and Experimental Results

A prototype isolated ICN converter with its three inductors combined into a single planar integrated magnetic structure is designed, built and tested. This ICN converter is identical in its specifications to the converter described in Chapter 3: it switches at 1 MHz, operates over an input voltage range of 36 V to 60

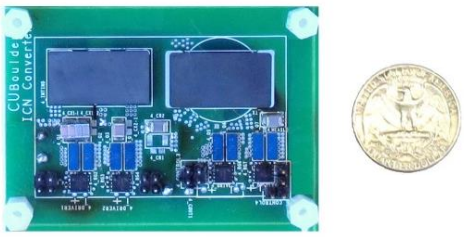
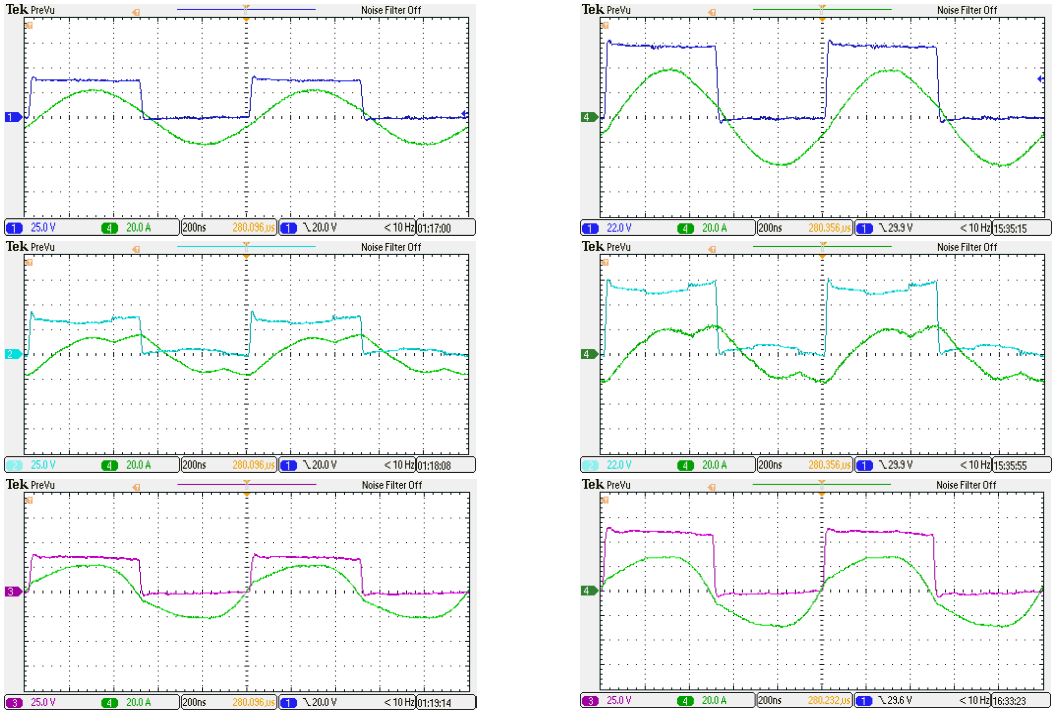


Figure 4.8: Photograph of the prototype ICN converter. Also shown for size comparison is a U.S. quarter.

V and an output voltage range of 34 V to 55 V, and delivers a maximum of 550 W. A photograph of the prototype ICN converter is shown in Fig. 5. The three inductances in the prototype ICN converter are: $L_{X1} = 342$ nH, $L_{X2} = 164$ nH and $L_r = 187$ nH. These are realized by a two-winding integrated magnetic structure with the following self and mutual inductances: $L_{11} = 506$ nH, $L_{22} = 351$ nH and $M = 164$ nH. To provide isolation, this prototype has a planar PCB transformer with a turns ratio of 1:1. The geometry of this transformer is also optimized using a procedure similar to that described in the previous section. The ferrite core material used in both the integrated magnetic structure and the transformer is DMEGC's DMR51W. The inverters and rectifier in this prototype converter use EPC2021 80-V/60-A enhancement-mode GaN transistors, with TI LM5113 half-bridge gate drivers.

The prototype ICN converter has been tested across its entire range of input and output voltages and output power. All inverter and rectifier transistors achieve ZVS and near-ZCS across its operating range. Switching waveforms demonstrating ZVS and near-ZCS operation of the inverter and rectifier transistors



(a) (b)

Figure 4.9: Inverter and rectifier switching waveforms of the prototype ICN converter while delivering full power at: (a) $V_{\mathrm{IN}} = 36$ V, $V_{\mathrm{OUT}} = 34$ V and (b) $V_{\mathrm{IN}} = 60$ V, $V_{\mathrm{OUT}} = 55$ V. The waveforms shown in (a) and (b) are, from top to bottom, the output voltage and current of the top inverter, the output voltage and current of the bottom inverter and the input voltage and current of the leading leg of the rectifier.

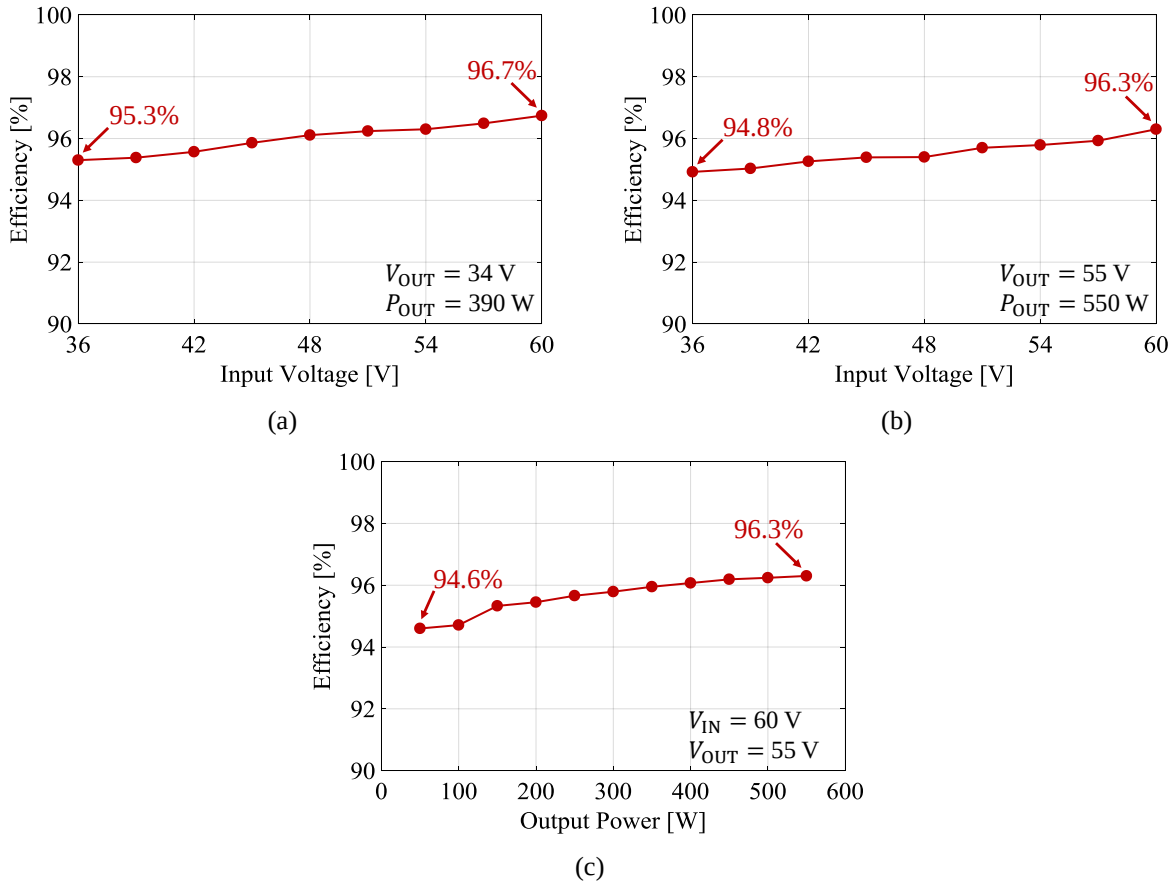


Figure 4.10: Measured efficiency of the prototype ICN converter across variations in: (a) input voltage at its minimum output voltage of 34 V; (b) input voltage at its maximum output voltage of 55 V; and (c) output power with an input voltage of 60 V and output voltage of 55 V.

at two of the corner operating points of the converter are shown in Fig. 4.9. The efficiency of the prototype ICN converter has also been measured across its entire operating range, and shown in Fig. 4.10. The prototype converter achieves a peak full-power efficiency of 96.7%, and a minimum full-power efficiency of 94.8%. The converter also maintains greater than 93.2% efficiency across a 10:1 range of output power across its entire range of input and output voltages. While maintaining these high efficiencies across wide operating ranges, this 550-W prototype ICN converter conforms to quarter-brick dimensions and achieves a power density of 462 W/in^3.

4.5 Chapter Summary and Conclusions

This chapter presents a high-power-density and high-efficiency isolated dc-dc converter based on the

impedance control network (ICN) resonant converter architecture. The ICN converter maintains very high efficiency by achieving ZVS and near-ZCS across wide operating ranges. High power density is achieved by combining the three inductors of the ICN converter into a single integrated magnetic structure with two coupled windings. A 3D FEA based design optimization approach is employed to minimize winding and core losses in this integrated magnetic structure. A prototype 1-MHz, 550-W ICN converter incorporating a planar PCB implementation of the integrated magnetic structure, designed to operate over an input voltage range of 36 V to 60 V and a regulated output voltage range of 34 V to 55 V is designed, built and tested. This ICN converter prototype is suitable as an isolated telecom bus converter. The prototyped converter achieves a power density of 462 W/in^3, a peak full-power efficiency of 96.7% and maintains full-power efficiencies above 93.2% across its entire operating range.

Compared to the high-efficiency ICN converter prototype presented in Chapter 3, the ICN converter prototype presented in this chapter maintains comparable efficiencies (~1% lower on average), but achieves more than 20 times higher power density. This dramatic increase in power density is made possible by combination of: 1) greatly reduced height achieved by replacing discrete magnetic components with planar components, and 2) further reduced height and footprint achieved by integrating the ICN inductors into a single optimized magnetic structure. While these improvements in magnetics design enable the ICN converter to be substantially reduced in size, this converter still requires large input and output capacitors due to the use of burst-mode control to regulate its output voltage and power. The next chapter describes an alternative to burst-mode control, termed multimode topology morphing control, that substantially reduces the input and output capacitance requirements in ICN converters, and also improves their partial-power efficiencies.

Chapter 5
Multimode Topology Morphing Control of Impedance Control Network DC-DC Converters

This chapter introduces a multimode topology morphing control approach for output voltage regulation in ICN resonant dc-dc converters, in which the rectifier of the ICN converter dynamically alternates between full-bridge and half-bridge topologies. The proposed control approach allows the ICN converter to maintain soft-switching across power levels, while substantially reducing input and output capacitance requirements and improving partial-power efficiencies compared to the conventional burst mode (on/off) control. These performance enhancements are analytically evaluated and quantified for an example ICN converter design. A closed-loop control architecture for the proposed multimode topology morphing is also introduced, which ensures smooth mode transitions while regulating output voltage across input voltage and load transients. A prototype 1-MHz, 120-W step-down ICN resonant converter designed for an input voltage range of 18 V to 36 V, an output voltage of 12 V and a 10:1 output power range, suitable as an intermediate bus converter in a telecommunication power distribution system, is built and tested. Compared to burst-mode control, the topology morphing control reduces the output capacitance requirement in the prototype ICN converter by 57% and reduces converter losses at partial power levels by up to 46.5%, validating the analytical predictions. The prototype converter is also tested under closed-loop control, and is shown to successfully regulate its output voltage with smooth mode transitions in the face of input voltage and load variations.

5.1 Background on Topology Morphing

Resonant converters typically achieve a significant portion of their voltage conversion ratio using resonant networks that provide voltage or current gain. For a converter operating over wide ranges of input voltage, output voltage and/or output power, the gain required from the resonant network also varies over

a wide range. To achieve this widely varying gain, wide variations in operating parameters such as switching frequency are required, making it difficult to optimize the design of the resonant network, and hence, achieve high efficiencies. Conventional topology morphing approaches address this issue by modifying the topology of the converter's inverter and/or rectifier based on the operating conditions, such that even as the operating conditions vary over a wide range, the gain required from the resonant network is restricted to a narrower range. For instance, [111]-[114] describe resonant converters having full-bridge inverters, which are operated in full-bridge mode when the converter's input voltage is lower than a threshold value, and in half-bridge mode when the input voltage is higher. Resonant converters with multilevel inverters performing a similar function have been presented in [115]-[117]. Similar approaches involving rectifiers are presented in [118]-[122], and an approach involving both inverters and rectifiers is presented in [123]. In all the above approaches, the converter's operating range is divided into portions based on the input voltage, output voltage or power, and each portion is served by the inverter/rectifier topology that results in the best efficiency. Furthermore, in each portion of the operating range, the output voltage and power are regulated using other techniques such as frequency or phase-shift control. The proposed multimode topology morphing control approach is fundamentally different from these conventional topology morphing approaches, because in addition to enhancing the converter's performance, the proposed approach also serves as a means for regulating the converter's output voltage and power. Another point of difference between the conventional and proposed approaches is that the proposed approach specifically targets resonant converters that are otherwise operated under burst-mode control. As demonstrated here in the context of the ICN resonant converter, this multimode topology morphing control serves as a higher-performance alternative to burst-mode control.

5.2 Multimode Topology Morphing Control of ICN Converter

Consider the ICN converter of Fig. 5.1, whose topology is identical to the converter described at the beginning of Chapter 4. Now consider the ICN converter of Fig. 5.2. This converter differs from the ICN converter of Fig. 5.1 in one respect: the resonant capacitor C_{r} is moved to the secondary side of the

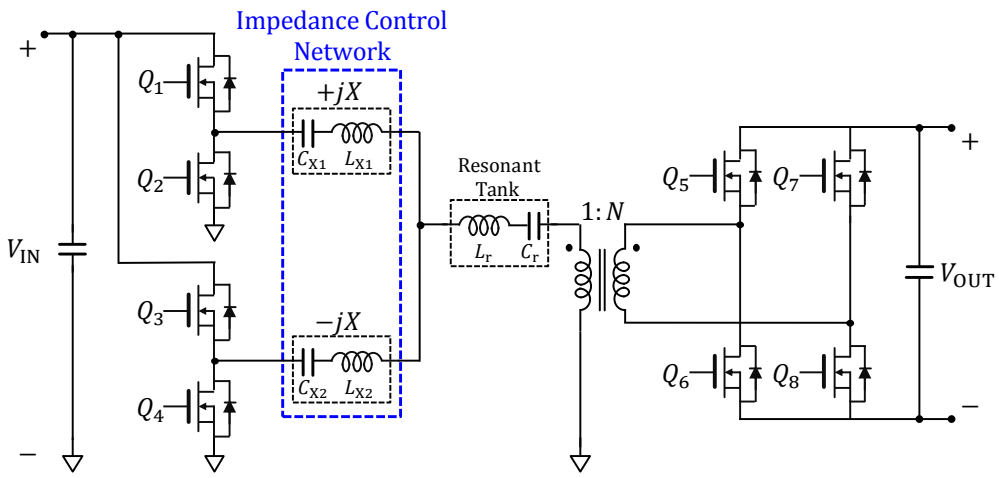


Figure 5.1: Impedance control network (ICN) dc-dc converter with a full-bridge synchronous rectifier.

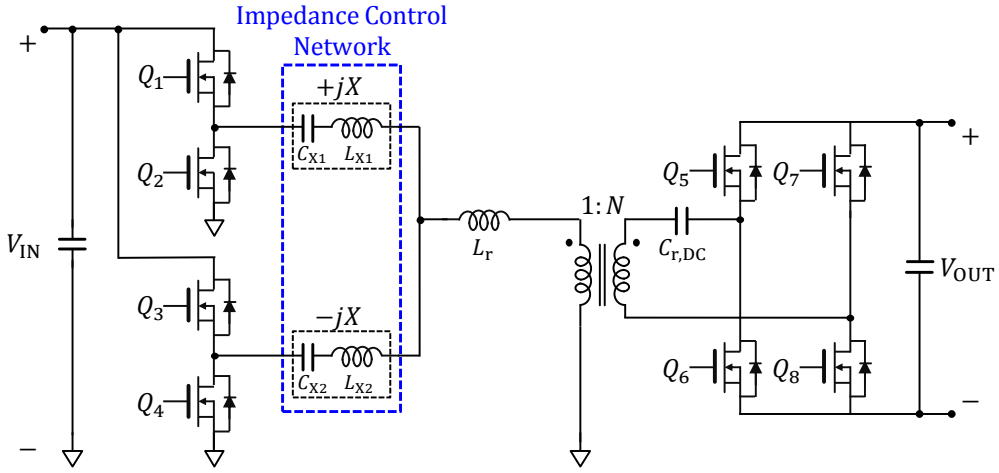


Figure 5.2: Impedance control network (ICN) dc-dc converter with its resonant capacitor C_r moved to the secondary side of the transformer to enable dc blocking.

transformer (labeled as $C_{r,DC}$ in Fig. 5.2). Provided that the magnetizing inductance of the transformer is large, and with C_r scaled by the square of the transformer turns ratio (that is, $C_{r,DC} = \frac{C_r}{N^2}$), the series resonant tank formed by L_r and C_r in Fig. 5.1 is functionally equivalent to the one formed by L_r and $C_{r,DC}$ in Fig. 5.2. However, this modification enables the resonant capacitor to also serve as a dc blocking capacitor. As a result, the rectifier of the ICN converter of Fig. 5.2 can be operated either as a full-bridge or as a half-bridge. When operated in full-bridge mode, all four rectifier transistors ($Q_5 - Q_8$ in Fig. 5.2) are switched with ~50% duty ratio, and the two rectifier legs are phase-shifted with respect to one another by 180°. In

the half-bridge mode, one of the rectifier legs (for instance, Q_5 and Q_6) continues to switch with ~50% duty ratio, while the bottom transistor of the other leg (Q_8) is kept turned on and its top transistor (Q_7) is kept turned off.

The maximum output power that the ICN converter of Fig. 5.2 can deliver in full-bridge rectifier mode is given by:

$$P_{\mathrm{OUT,max,FB}} = \frac{4V_{\mathrm{IN}}}{\pi^2 NX}\sqrt{4V_{\mathrm{OUT}}^2 - N^2 V_{\mathrm{IN}}^2}. \tag{5.1}$$

Similarly, the maximum power delivered by the converter in the half-bridge rectifier mode ($K_{\mathrm{rec}} = \frac{2}{\pi^2}$) is given by:

$$P_{\mathrm{OUT,max,HB}} = \frac{4V_{\mathrm{IN}}}{\pi^2 NX}\sqrt{V_{\mathrm{OUT}}^2 - N^2 V_{\mathrm{IN}}^2}. \tag{5.2}$$

The expressions in (5.1) and (5.2) are derived in Appendix A. It can be seen from (5.1) and (5.2) that the maximum power capability of the converter in the full-bridge rectifier mode is higher than that in the half-bridge rectifier mode.

The output power of the converter is regulated below the full-bridge maximum level given in (5.1) using the proposed multimode topology morphing control, as illustrated in Fig. 5.3 for a range of input voltages and a fixed output voltage. When the output power requirement equals the full-bridge maximum power

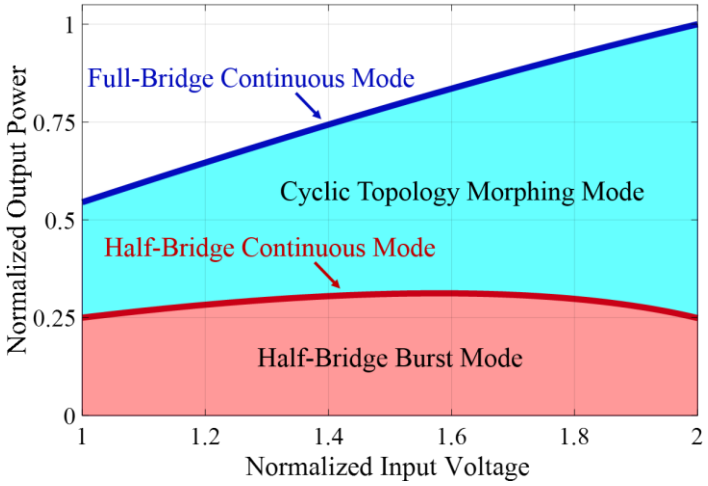


Figure 5.3: The four modes of the proposed topology morphing control scheme. Here the output power of the ICN converter (the y-axis) is normalized with respect to the maximum power the converter can deliver with a full-bridge rectifier, and the input voltage (the x-axis) is normalized with respect to the minimum input voltage of the converter.

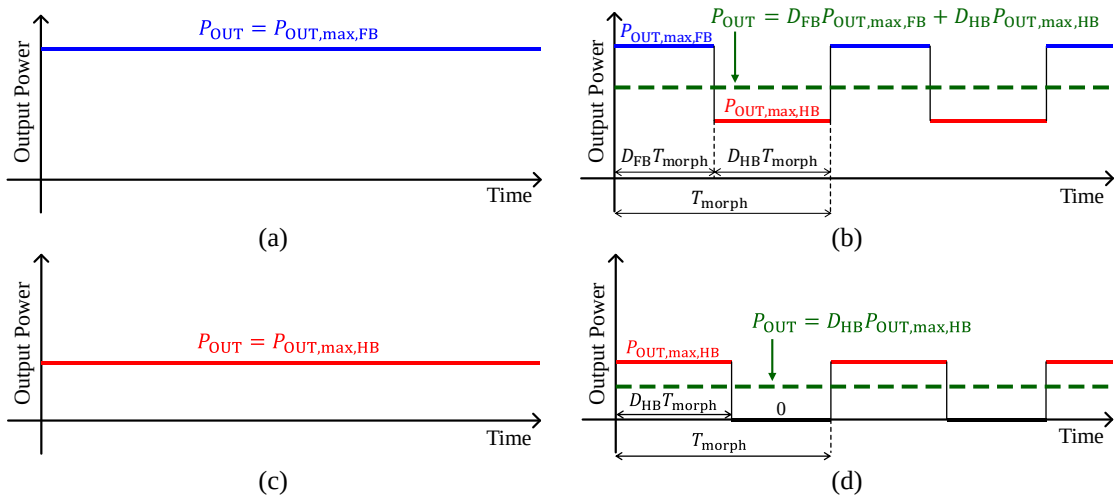


Figure 5.4: The four modes of output power regulation in the proposed topology morphing control scheme: (a) full-bridge continuous mode, (b) cyclic topology morphing mode, (c) half-bridge continuous mode, and (d) half-bridge burst-mode.

level (the dark blue curve in Fig. 5.3), the rectifier operates continuously in full-bridge mode. The output power delivered by the converter during this mode is illustrated as a function of time in Fig. 5.4(a). For power levels below the full-bridge maximum but higher than the half-bridge maximum (the blue-shaded region in Fig. 5.3) the rectifier of the ICN converter periodically cycles between its full-bridge and half-bridge topologies, at a frequency f_{morph} substantially lower than the switching frequency. This cyclic topology morphing mode is illustrated in Fig. 5.4(b). When the output power requirement equals the half-bridge maximum (the dark red curve in Fig. 5.3), the rectifier operates continuously as a half-bridge, as depicted in Fig. 5.4(c). Power levels below the half-bridge maximum (the red-shaded region in Fig. 5.3) are delivered using the half-bridge burst-mode, in which the rectifier operates as a half-bridge and the converter is periodically turned on and off at the same frequency as that used in the cyclic topology morphing mode. This is illustrated in Fig. 5.4(d).

The output power delivered by the ICN converter in the above-described topology morphing control scheme is given by:

$$P_{\text{OUT}} = D_{\text{FB}}P_{\text{OUT,max,FB}} + D_{\text{HB}}P_{\text{OUT,max,HB}}. \tag{5.3}$$

Here, D_{FB} and D_{HB} are the duty ratios for which the rectifier of the ICN converter operates as a full-bridge and as a half-bridge, respectively, in each of the four modes of the proposed topology morphing control

scheme (see Fig. 5.4). Given a required output power P_{OUT}, the full-bridge and half-bridge duty ratios can be computed using:

$$D_{\mathrm{FB}} = \min\left[1, \max\left\{\frac{P_{\mathrm{OUT}} - P_{\mathrm{OUT,max,HB}}}{P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT,max,HB}}}, 0\right\}\right]. \tag{5.4}$$

$$D_{\mathrm{HB}} = \max\left[0, \min\left\{\frac{P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT,max,HB}}}, \frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,HB}}}\right\}\right]. \tag{5.5}$$

Figure 5.5 illustrates the full-bridge and half-bridge duty ratios for an ICN converter operating at a particular input and output voltage as a function of the required output power P_{OUT}, across the four modes of the proposed topology morphing control scheme. As can be seen, in the half-bridge burst-mode, as the required output power increases, the half-bridge duty ratio D_{HB} is ramped up linearly while the full-bridge duty ratio D_{FB} is maintained at 0. When the required power equals the half-bridge maximum level $P_{\mathrm{OUT,max,HB}}$, the rectifier operates continuously as a half-bridge, corresponding to a half-bridge duty ratio of 1. Beyond this power level, the half-bridge duty ratio is decreased linearly, and the full-bridge duty ratio is increased linearly. Finally, when the required output power equals the full-bridge maximum level, the half-bridge duty ratio D_{HB} is 0 and the full-bridge duty ratio D_{FB} is 1.

As described in Chapter 3, the phase-shift between the inverters of an ICN converter is controlled to achieve ZVS and near-ZCS operation. In the proposed topology morphing control scheme, when the

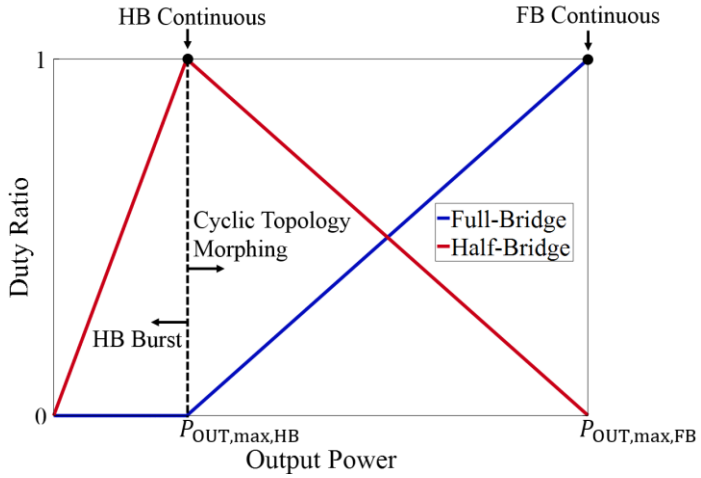


Figure 5.5: Duty ratios of full-bridge and half-bridge rectifier operation of the ICN converter across the four modes of the proposed topology morphing control scheme. The half-bridge duty ratio D_{HB} is shown in red, and the full-bridge duty ratio D_{FB} in blue.

rectifier is operated as a full-bridge, the inverter phase-shift is controlled to be:

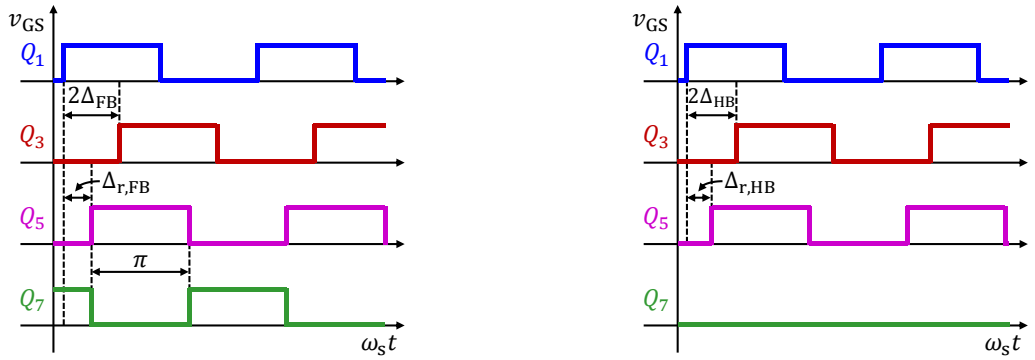
$$2\Delta_{\mathrm{FB}} = 2\cos^{-1}\left(\frac{N\mathrm{V_{IN}}}{2\mathrm{V_{OUT}}}\right), \tag{5.6}$$

while during half-bridge operation, the inverter phase-shift is controlled to be:

$$2\Delta_{\mathrm{HB}} = 2\cos^{-1}\left(\frac{N\mathrm{V_{IN}}}{\mathrm{V_{OUT}}}\right). \tag{5.7}$$

Depending on the rectifier's mode of operation (full-bridge or half-bridge), the inverter phase-shift is controlled either according to (5.6) or (5.7), and in both cases the rectifier is switched slightly later than the zero-crossings of the rectifier input current, enabling the ICN converter to maintain soft-switching and high-efficiency in all the modes of the proposed topology morphing control approach. Gating signals for the inverter and rectifier transistors under the proposed control approach are shown in Fig. 5.6.

A potential challenge in the proposed topology morphing control scheme is the transition between the full-bridge and half-bridge modes. During the full-bridge-to-half-bridge transition, the dc blocking capacitor ($C_{\mathrm{r,DC}}$ in Fig. 5.2) needs to charge from an average voltage of 0 in the full-bridge mode to an average voltage of $-\frac{V_{\mathrm{OUT}}}{2}$ in the half-bridge mode; the reverse transition then needs to occur during the next half-bridge-to-full-bridge transition. The cyclic topology morphing mode of the proposed control scheme requires these transitions to occur repeatedly at a topology morphing frequency f_{morph}, which is



(a) (b)

Figure 5.6: Gating signals for the high-side transistors of the inverter and rectifier of the ICN converter of Fig. 5.2 with the rectifier operating as a: (a) full-bridge, and (b) half-bridge. Gating signals for the low-side transistors are complementary to the signals shown above, with short dead times. The inverter phase-shifts $2\Delta_{\mathrm{FB}}$ and $2\Delta_{\mathrm{HB}}$ are given by (5.6) and (5.7), respectively, and the corresponding rectifier phase-shifts $\Delta_{\mathrm{r,FB}}$ and $\Delta_{\mathrm{r,HB}}$ are selected such that the rectifier transistors switch slightly later than the zero-crossings of the rectifier input current (to enable ZVS and near-ZCS of the rectifier).

typically of the order of kilohertz to tens of kilohertz (for a switching frequency of the order of 500 kHz to a few MHz). If the dc blocking capacitor is large, these transitions consume a prohibitively large fraction of the topology morphing period (T_{morph} in Fig. 5.4). This degrades the converter's efficiency because during these transitions, the inverter and rectifier transistors are not guaranteed to operate with ZVS and near-ZCS, and the converter currents are likely to experience large-amplitude low-frequency oscillations owing to the resonance between the dc blocking capacitor and the magnetizing inductance of the transformer. Furthermore, the large dc blocking capacitor increases the converter's size. These issues are resolved to a significant extent by utilizing a resonant capacitor to perform the dc blocking function. Compared to a large dc-blocking capacitor, this resonant capacitor is much smaller in size, and being small valued, enables the full-bridge-half-bridge transitions to consume a much smaller number of switching cycles. While these faster transitions are not completely free of hard-switching events and current oscillations, they take up a much smaller fraction of the topology morphing period; hence, allowing the converter's efficiency to be less impacted than it would be with a large dc-blocking capacitor. Utilizing a resonant capacitor for dc-blocking also reduces the converter's component count, since this capacitor is already a part of the harmonic-mitigating series resonant tank in ICN converters. One disadvantage of having this capacitor on the secondary side in step-down ICN converters is that it needs to carry $1/N$ times higher current than that carried by the primary-side resonant capacitor in conventional step-down ICN converters, where $N(<1)$ is the transformer turns ratio (compare the current carried by $C_{\mathrm{r,DC}}$ in Fig. 2 to that carried by C_{r} in Fig. 5.1). However, since this capacitor $C_{\mathrm{r,DC}}$ is small-valued (for example, in the range of 100's of nF for a switching frequency of 1 MHz), it can be implemented using ceramic capacitors with very low ESR, resulting in acceptably low losses.

5.3 Performance Enhancement With Topology Morphing Control

Compared to the conventional burst-mode control, the proposed topology morphing control enhances the performance of the ICN converter both in terms of its power density and its efficiency, as described below in subsections A and B, respectively. In these subsections, the performance of the ICN converter under the

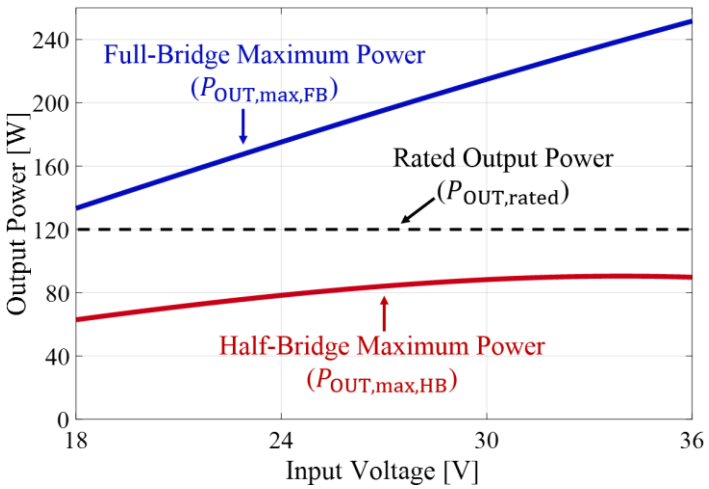


Figure 5.7: The full-bridge and half-bridge maximum power levels of an ICN converter designed for an input voltage range of 18 V to 36 V, output voltage of 12 V and rated output power of 120 W.

two control schemes is first compared in a general analytical manner applicable to all ICN converter designs. The performance improvement brought about by topology morphing control is then quantified for an example ICN converter, designed for an input voltage range of 18 V to 36 V, an output voltage of 12 V and a rated output power of 120 W. This ICN converter has a transformer turns ratio of 4:1, an ICN differential reactance X of 5.2 Ω, and a switching frequency of 1 MHz. The full-bridge and half-bridge maximum power curves of this ICN converter are shown in Fig. 5.7. Additional design details of this converter are provided in Table 5.1, and its design methodology is provided in Appendix B.

A. Power Density Comparison

In the conventional burst-mode control, the ICN converter is turned on and off at a frequency substantially lower than its switching frequency, resulting in a low-frequency ripple in the converter's output voltage. A large output capacitor is required to limit this ripple, adversely impacting the converter's power density. In the proposed topology morphing control, the ICN converter either cycles between half- and full-bridge rectifiers (in the cyclic topology morphing mode), or is turned on and off (in the half-bridge burst-mode), at a similarly low frequency. Therefore, the proposed control scheme also introduces a low-frequency ripple in the ICN converter's output voltage. However, the magnitudes of this output voltage ripple are significantly different in the two control schemes. At a given operating point (input voltage V_{IN}, output

TABLE 5.1

DESIGN OF STEP-DOWN ICN CONVERTER

Component	Design	Loss Parameters
Inverter transistors ($Q_1 - Q_4$)	EPC2001C, 100-V, 36-A eGaN FETs	$R_{\mathrm{DS,on}\mid T_\mathrm{J}=100°\mathrm{C}} =$ 10 mΩ
Rectifier transistors ($Q_5 - Q_8$)	EPC2023, 30-V, 60-A eGaN FETs	$R_{\mathrm{DS,on}\mid T_\mathrm{J}=100°\mathrm{C}} = 2$ mΩ
L_{X1}	1.45 µH Winding: 4 turns of 2000-strand AWG-48 Litz wire Core: RM10, Ferroxcube 3F46	$R_{\mathrm{ac}} = 5.3$ mΩ $K_{\mathrm{fe}} = 5.25\times10^{-4}$ $\alpha = 2, \beta = 2.73$
$C_{\mathrm{X1}}\left(=\frac{1}{\omega_\mathrm{s}(\omega_\mathrm{s}L_{\mathrm{X1}} - X)}\right)$	40.2 nF 4 × 10-nF TDK C3225C0G2E103J160AA, 250-V NP0	ESR = 0.5 mΩ
L_{X2}	700 nH Winding: 3 turns of 2000-strand AWG-48 Litz wire Core: RM10, Ferroxcube 3F46	$R_{\mathrm{ac}} = 3.1$ mΩ $K_{\mathrm{fe}} = 5.25\times10^{-4}$ $\alpha = 2, \beta = 2.73$
$C_{\mathrm{X2}}\left(=\frac{1}{\omega_s(\omega_s L_{X2} + X)}\right)$	16.7nF 1 × 10-nF TDK C3225C0G2E103J160AA, 250-V NP0 1 × 6.8-nF TDK C3225C0G2J682J200AA, 630-V NP0	ESR = 1.3 mΩ
L_r	650 nH Winding: 3 turns of 2000-strand AWG-48 Litz wire Core: RM10, Ferroxcube 3F46	$R_{\mathrm{ac}} = 3.1$ mΩ $K_{\mathrm{fe}} = 5.25\times10^{-4}$ $\alpha = 2, \beta = 2.73$
$C_{\mathrm{r,DC}}\left(=\frac{1}{N^2\omega_\mathrm{s}^2 L_\mathrm{r}}\right)$	623.5 nF 6 × 100-nF TDK C3225C0G1H104J250AA, 50-V NP0 1 × 22-nF TDK C3225NP01H223J125AA, 50-V NP0	ESR = 0.25 mΩ
Transformer	4:1 Winding: 4 primary turns of 1000-strand AWG-48 Litz wire 1 secondary turn of 3000-strand AWG-48 Litz wire Core: RM10, Ferroxcube 3F46	$R_{\mathrm{ac,primary}} = 6.4$ mΩ $R_{\mathrm{ac,secondary}} = 0.5$ mΩ $K_{\mathrm{fe}} = 5.25\times10^{-4}$ $\alpha = 2, \beta = 2.73$

voltage V_{OUT} and output power P_{OUT}), the low-frequency output voltage ripple in conventional burst-mode control can be expressed as:

$$\delta v_{\mathrm{out,burst}} = \frac{\left(P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT}}\right) P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,FB}}} \frac{1}{C_{\mathrm{OUT}} V_{\mathrm{OUT}} f_{\mathrm{burst}}}. \tag{5.8}$$

Here, C_{OUT} is the output capacitance of the converter and f_{burst} is the frequency at which the converter is turned on and off during burst-mode operation. In comparison, the output voltage ripple at the same operating point in the proposed topology morphing control is given by:

$$\delta v_{\mathrm{out,morph}} = \begin{cases} \frac{\left(P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT}}\right)\left(P_{\mathrm{OUT}} - P_{\mathrm{OUT,max,HB}}\right)}{P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT,max,HB}}} \frac{1}{C_{\mathrm{OUT}} V_{\mathrm{OUT}} f_{\mathrm{morph}}} & \text{in FBC and CTM} \\ \frac{\left(P_{\mathrm{OUT,max,HB}} - P_{\mathrm{OUT}}\right) P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,HB}}} \frac{1}{C_{\mathrm{OUT}} V_{\mathrm{OUT}} f_{\mathrm{morph}}} & \text{in HBC and HBB} \end{cases}. \tag{5.9}$$

Here, the acronyms FBC, CTM, HBC and HBB correspond to the full-bridge continuous, cyclic topology

morphing, half-bridge continuous and half-bridge burst-modes of the proposed topology morphing control scheme, respectively. The expressions in (5.8) and (5.9) are derived in Appendix C. Assuming that the conventional burst-mode frequency f_{burst} is the same as the topology morphing frequency f_{morph}, and that the same output capacitance C_{OUT} is used in both control schemes, (5.8) and (5.9) can be used to show that topology morphing control reduces the output voltage ripple relative to burst-mode control by:

$$\frac{\delta v_{\text{out,burst}} - \delta v_{\text{out,morph}}}{\delta v_{\text{out,burst}}} = \begin{cases} \frac{\left(\frac{P_{\text{OUT,max,FB}}}{P_{\text{OUT}}} - 1\right)}{\left(\frac{P_{\text{OUT,max,FB}}}{P_{\text{OUT,max,HB}}} - 1\right)} & \text{in FBC and CTM} \\ \frac{\left(\frac{P_{\text{OUT,max,FB}}}{P_{\text{OUT,max,HB}}} - 1\right)}{\left(\frac{P_{\text{OUT,max,FB}}}{P_{\text{OUT}}} - 1\right)} & \text{in HBC and HBB} \end{cases} . \tag{5.10}$$

Since the full-bridge maximum power level $P_{\text{OUT,max,FB}}$ of the ICN converter is always greater than the half-bridge maximum power level $P_{\text{OUT,max,HB}}$ (see Figs. 5.3 and 5.7), the right-hand side of (5.10) is positive for all operating points where the converter delivers less output power P_{OUT} than the full-bridge maximum power level $P_{\text{OUT,max,FB}}$ (i.e., the entire area under the dark blue curve in Fig. 5.3). Therefore, the output voltage ripple under topology morphing control is smaller than that under burst-mode control at all these operating points. This ripple reduction is quantified for the step-down ICN converter design described above, as a function of the input voltage and output power of the converter, in Fig. 5.8. As can be seen, at every input voltage, when the output power P_{OUT} equals the half-bridge maximum power level $P_{\text{OUT,max,HB}}$, the output voltage ripple is reduced by 100%. This is because in the proposed control scheme, the rectifier operates continuously in half-bridge mode at this operating point, resulting in zero low-frequency output voltage ripple.

Given a maximum limit on the output voltage ripple of the ICN converter, the above-described ripple reduction translates to a smaller required output capacitance. For instance, to limit the output voltage ripple within 5% across the operating range of the example step-down ICN converter, burst-mode control requires a capacitance of 8.75 mF (according to (5.8)), while topology morphing control requires a capacitance of 3.45 mF (according to (5.9)), corresponding to a capacitance reduction of nearly 61%. This results in a proportionally large reduction in the size of the output capacitor, and hence, a substantially improved power

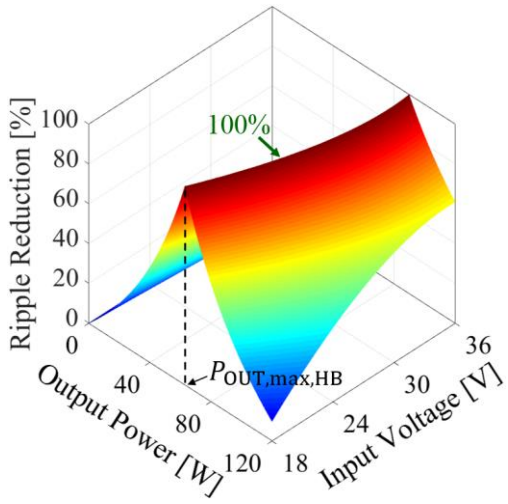


Figure 5.8: Reduction in output voltage ripple brought about by the proposed topology morphing control relative to the conventional burst-mode control for the step-down ICN converter design of Table 5.1.

density. The reason for this capacitance reduction can be intuitively understood by noting that in the proposed control scheme, the output voltage ripple is largest in the cyclic topology morphing mode (as shown in Appendix C). However, in contrast to conventional burst-mode control where the converter is periodically turned off, under the proposed control scheme the converter always delivers some power in the cyclic topology morphing mode, resulting in a smaller output voltage ripple. Hence, the proposed control scheme requires a smaller capacitance to maintain the same voltage ripple.

B. Efficiency Comparison

The losses in the ICN converter under the two control schemes are also compared. For this comparison, all major contributors to the converter's losses are considered: conduction losses in the inverter and rectifier transistors, winding and core losses in the inductors and the transformer, and conduction losses in the capacitors. Since the ICN converter achieves ZVS and near-ZCS both under the conventional burst-mode control and the proposed topology morphing control, switching losses in both the control schemes can be neglected in comparison to the above-mentioned modes of loss. Other losses not considered in this comparison include burst-mode startup and shutdown losses, and losses during the full-bridge-half-bridge transitions of the proposed topology morphing control approach. The impact of these losses is discussed in detail in Section 5.5 of this chapter.

Consider the ICN converter of Fig. 5.2. The conduction losses in the inverter transistors $Q_1 - Q_4$ and the ICN capacitors C_{X1} and C_{X2}, and the winding and core losses in the ICN inductors L_{X1} and L_{X2}, all depend on the output currents of the two inverters. Using fundamental frequency analysis, the inverter output currents in burst-mode control and in topology morphing control can be expressed as functions of the output power P_{OUT}, the full-bridge maximum power $P_{\mathrm{OUT,max,FB}}$ and, in the case of topology morphing control, the half-bridge maximum power $P_{\mathrm{OUT,max,HB}}$ of the ICN converter. It can then be shown that the reductions in the above losses under topology morphing control relative to burst-mode control are given by:

$$\frac{P_{\mathrm{cond,inv,X1,X2,b}} - P_{\mathrm{cond,inv,X1,X2,m}}}{P_{\mathrm{cond,inv,X1,X2,b}}} = \begin{cases} P_{\mathrm{OUT,max,HB}} \left(\frac{1}{P_{\mathrm{OUT}}} - \frac{1}{P_{\mathrm{OUT,max,FB}}} \right) & \text{in FBC and CTM} \\ 1 - \frac{P_{\mathrm{OUT,max,HB}}}{P_{\mathrm{OUT,max,FB}}} & \text{in HBC and HBB} \end{cases}, \quad (5.11)$$

$$\frac{P_{\mathrm{core},L_{\mathrm{X1}},L_{\mathrm{X2}},\mathrm{b}} - P_{\mathrm{core},L_{\mathrm{X1}},L_{\mathrm{X2}},\mathrm{m}}}{P_{\mathrm{core},L_{\mathrm{X1}},L_{\mathrm{X2}},\mathrm{b}}} = \begin{cases} \frac{\left(\frac{P_{\mathrm{OUT,max,FB}}}{P_{\mathrm{OUT}}} - 1 \right) \left(1 - \left(\frac{P_{\mathrm{OUT,max,HB}}}{P_{\mathrm{OUT,max,FB}}} \right)^{\beta - 1} \right)}{\frac{P_{\mathrm{OUT,max,FB}}}{P_{\mathrm{OUT,max,HB}}} - 1} & \text{in FBC and CTM} \\ 1 - \left(\frac{P_{\mathrm{OUT,max,HB}}}{P_{\mathrm{OUT,max,HB}}} \right)^{\beta - 1} & \text{in HBC and HBB} \end{cases}. \quad (5.12)$$

Here, $P_{\mathrm{cond,inv,X1,X2,b}}$ and $P_{\mathrm{cond,inv,X1,X2,m}}$ are the sum of the conduction losses in the inverter transistors and the capacitors C_{X1} and C_{X2}, and the winding losses in the inductors L_{X1} and L_{X2} under the conventional burst-mode control and the proposed topology morphing control, respectively. Similarly, $P_{\mathrm{core},L_{\mathrm{X1}},L_{\mathrm{X2}},\mathrm{b}}$ and $P_{\mathrm{core},L_{\mathrm{X1}},L_{\mathrm{X2}},\mathrm{m}}$ are the sum of the core losses of L_{X1} and L_{X2} under burst-mode control and topology morphing control, respectively. The parameter β in (5.12) is the flux-associated Steinmetz parameter [124] of the core material used to construct the two inductors. Derivations of the expressions in (5.11) and (5.12) are provided in Appendix D.

It can be inferred from the right-hand side of (5.11) that the proposed topology morphing control reduces the conduction losses in the inverter transistors and the capacitors C_{X1} and C_{X2}, and the winding losses in the inductors L_{X1} and L_{X2}, at all operating points where the output power P_{OUT} is less than the full-bridge maximum power $P_{\mathrm{OUT,max,FB}}$. Similarly, the core losses of the inductors L_{X1} and L_{X2} evaluated in (5.12) are also reduced at all these operating points, provided the Steinmetz parameter β is greater than 1, which

holds true for most magnetic materials suitable for high-frequency power conversion [125]. The loss reductions predicted by (5.11) and (5.12) are plotted for the step-down ICN converter design described earlier, as a function of the input voltage and output power of the converter, in Figs. 5.9(a) and 5.9(b), respectively. As can be seen from Fig. 5.9(a), the proposed topology morphing control reduces the conduction and winding losses considered in (5.11) by up to over 64%, with an average loss reduction of over 51% over the converter's operating range. Figure 5.9(b) shows that the core losses in L_{X1} and L_{X2} (built using Ferroxcube's 3F46 ferrite material with $\beta = 2.73$, as computed using the manufacturer's datasheet [126]) are reduced by even larger amounts, with a maximum reduction of over 83% and an average reduction of nearly 69%.

The reduction in the above losses can be understood using Fig. 5.5, which indicates that in the proposed topology morphing control scheme, the rectifier of the ICN converter operates in half-bridge mode for a larger fraction of the operating range than in full-bridge mode (in contrast to the conventional burst-mode control, in which the rectifier always operates in full-bridge mode). Since the ICN converter generates less power with a half-bridge rectifier than with a full-bridge rectifier, at a given input voltage, the inverter output currents in the half-bridge rectifier mode are smaller than those in the full-bridge rectifier mode. Therefore, the losses in (5.11) and (5.12), which depend directly on the inverter output currents, are reduced under the proposed control scheme.

A similar comparison is performed for the winding and core losses of the resonant inductor L_{r}, the winding losses of the transformer, and the conduction losses of the resonant capacitor $C_{\mathrm{r,DC}}$ and the rectifier transistors $Q_5 - Q_8$. All these losses directly depend on the input current of the rectifier. Expressing the rectifier input current in terms of the output power P_{OUT} and the full-bridge and half-bridge maximum power levels $P_{\mathrm{OUT,max,FB}}$ and $P_{\mathrm{OUT,max,HB}}$ using fundamental frequency analysis, it can be shown that the reductions in these losses under the proposed topology morphing control relative to the conventional burst-mode control are given by:

$$\frac{P_{\text{cond},L_r,Tx,C_r,rec,b}-P_{\text{cond},L_r,Tx,C_r,rec,m}}{P_{\text{cond},L_r,Tx,C_r,rec,b}} = \begin{cases} \frac{\left(1-\frac{4P_{OUT,max,HB}}{P_{OUT,max,FB}}\right)\left(\frac{P_{OUT,max,FB}}{P_{OUT}}-1\right)}{\frac{P_{OUT,max,FB}}{P_{OUT,max,HB}}-1} & \text{in FBC and CTM} \\ 1-\frac{4P_{OUT,max,HB}}{P_{OUT,max,FB}} & \text{in HBC and HBB} \end{cases}, \quad (5.13)$$

$$\frac{P_{\text{core},L_r,b}-P_{\text{core},L_r,m}}{P_{\text{core},L_r,b}} = \begin{cases} \frac{\left(\frac{P_{OUT,max,FB}}{P_{OUT}}-1\right)\left(1-2^{\beta}\left(\frac{P_{OUT,max,HB}}{P_{OUT,max,FB}}\right)^{\beta-1}\right)}{\frac{P_{OUT,max,FB}}{P_{OUT,max,HB}}-1} & \text{in FBC and CTM} \\ 1-2^{\beta}\left(\frac{P_{OUT,max,HB}}{P_{OUT,max,HB}}\right)^{\beta-1} & \text{in HBC and HBB} \end{cases}. \quad (5.14)$$

Here $P_{\text{cond},L_r,Tx,C_r,rec,b}$ and $P_{\text{cond},L_r,Tx,C_r,rec,m}$ represent the sum of the winding losses of the inductor L_r and the transformer, and the conduction losses of the capacitor $C_{r,DC}$ and the rectifier transistors under burst-mode control and topology morphing control, respectively; and $P_{\text{core},L_r,b}$ and $P_{\text{core},L_r,m}$ represent the core losses of L_r under burst-mode control and topology morphing control, respectively. The expressions in (5.13) and (5.14) are also derived in Appendix D. It can be seen that the losses considered in (5.13) are reduced under the proposed topology morphing control at all the operating points of the ICN converter where the half-bridge maximum power level $P_{OUT,max,HB}$ is less than a quarter of the full-bridge maximum power level $P_{OUT,max,FB}$. In the example step-down ICN converter designed earlier, the half-bridge maximum power level $P_{OUT,max,HB}$ is greater than a quarter of the full-bridge maximum power level $P_{OUT,max,FB}$ at all input voltages (see Fig. 5.7). Therefore, the losses considered in (5.13) are actually higher in this design under the proposed control scheme. This is illustrated in Fig. 5.9(c), which indicates that these losses increase on an average by nearly 62%. A similar analysis of (5.14) shows that the core losses in the inductor L_r are reduced at all operating points where the half-bridge maximum power $P_{OUT,max,HB}$ is less than the full-bridge maximum power $P_{OUT,max,FB}$ by a factor of $\frac{1}{\frac{\beta}{2^{\beta-1}}}$ (that is, $P_{OUT,max,HB} < \frac{1}{\frac{\beta}{2^{\beta-1}}} P_{OUT,max,FB}$). This factor comes out to be 0.33 for the example step-down ICN converter design (with $\beta = 2.73$ for the 3F46 material). However, the maximum power curves of this converter, shown in Fig. 5.7, indicate that the half-bridge maximum power level $P_{OUT,max,HB}$ is greater than 0.36 times the full-bridge maximum power $P_{OUT,max,FB}$ at all input voltages. Therefore, the core losses of the inductor L_r in this

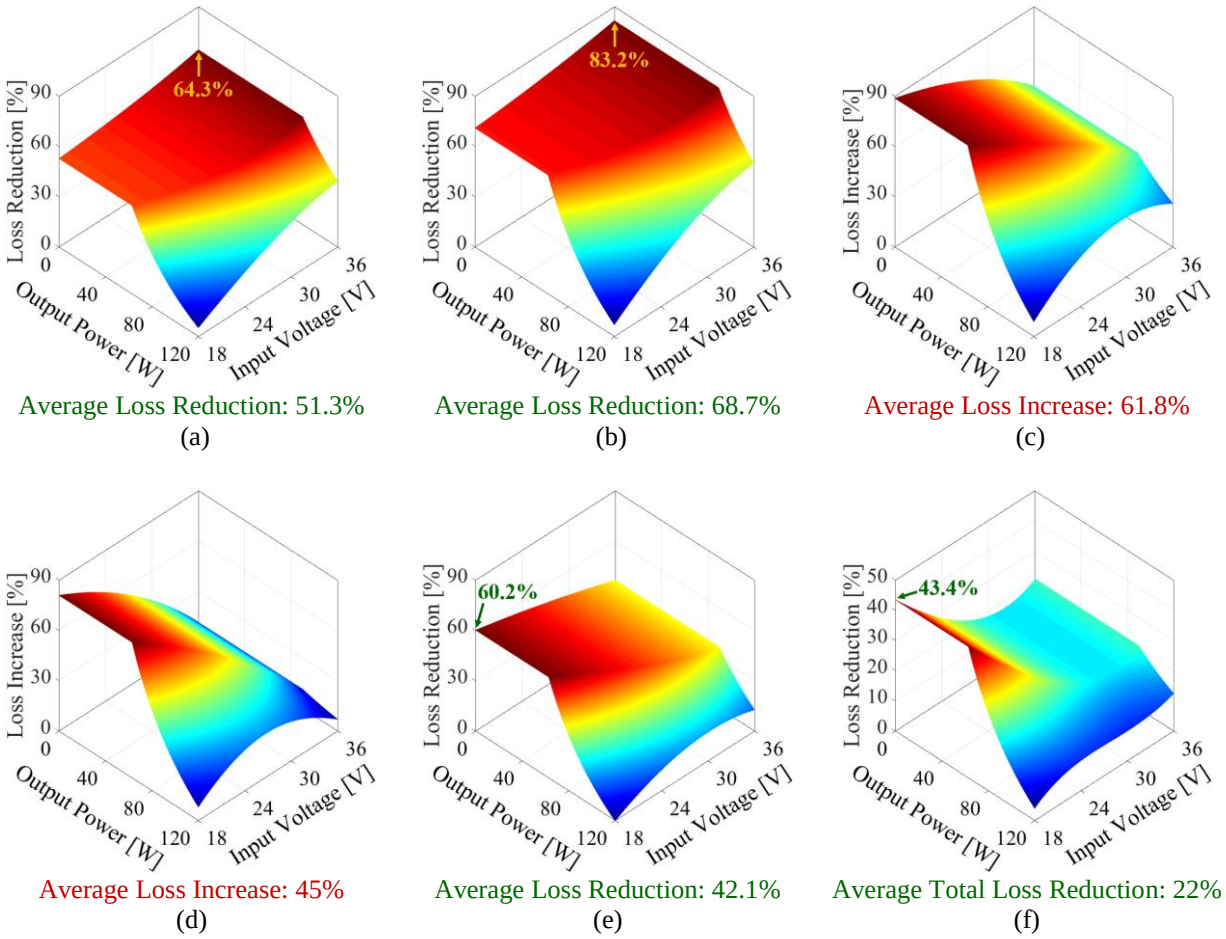
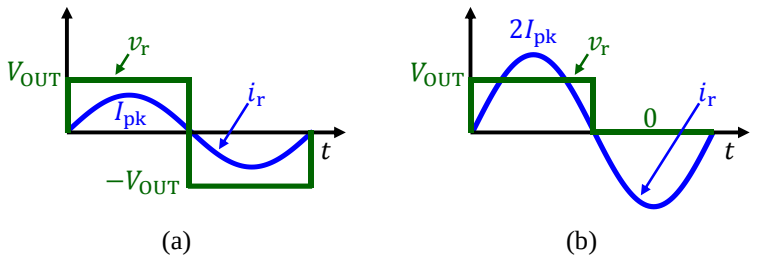


Figure 5.9: Percentage change in losses in the proposed topology morphing control relative to conventional burst-mode control in an ICN converter designed for an input voltage range of 18 V to 36 V, an output voltage of 12 V, and a rated output power of 120 W: (a) reduction in conduction losses of inverter transistors, capacitors C_{X1} and C_{X2}, and winding losses of inductors L_{X1} and L_{X2}; (b) reduction in core losses of inductors L_{X1} and L_{X2}; (c) increase in winding losses of inductor L_r and transformer, and conduction losses of capacitor C_r and rectifier transistors; (d) increase in core losses of inductor L_r; (e) reduction in core losses of transformer, and (f) reduction in total losses.

design also undergo an increase, as illustrated in Fig. 5.9(d). The increase in these core losses is smaller than that in the winding and conduction losses considered in (5.13), with an average loss increase of around 45%.

The above-described loss increase also has an intuitive basis: since a half-bridge rectifier transmits its input current to the converter output only during half the switching period (as illustrated in Fig. 5.10), at operating points where the half-bridge maximum power level $P_{OUT,max,HB}$ is sufficiently high, the rectifier input current is higher in half-bridge mode than in full-bridge mode. Therefore, the losses in (5.13) and (5.14) that depend on the rectifier input currents are also higher at these operating points under the proposed



(a) (b)

Figure 5.10: Fundamental-frequency rectifier input voltage v_r and current i_r for a: (a) full-bridge rectifier, and (b) half-bridge rectifier, with both rectifiers operating at the same output power (averaged over one switching period). As can be seen, the half-bridge rectifier in (b) transmits zero power during the second half of the switching period (since its input voltage is 0), resulting in twice the peak current compared to the full-bridge rectifier in (a).

control scheme relative to the conventional burst-mode control, wherein the rectifier always operates as a full-bridge.

The remaining major loss mechanism are the core losses of the transformer, which depend on the voltages impressed across the transformer windings. The voltage across the secondary winding of the transformer under the conventional burst-mode control and under the proposed topology morphing control are illustrated in Fig. 5.11. Since burst-mode control with a full-bridge rectifier does not require a dc blocking capacitor on the transformer's secondary side (as in the ICN converter of Fig. 5.1), the voltage across the transformer secondary under this control scheme is the same as the rectifier input voltage, and can be modeled as a square wave with an amplitude equal to the converter's output voltage V_{OUT} (= 12 V in the

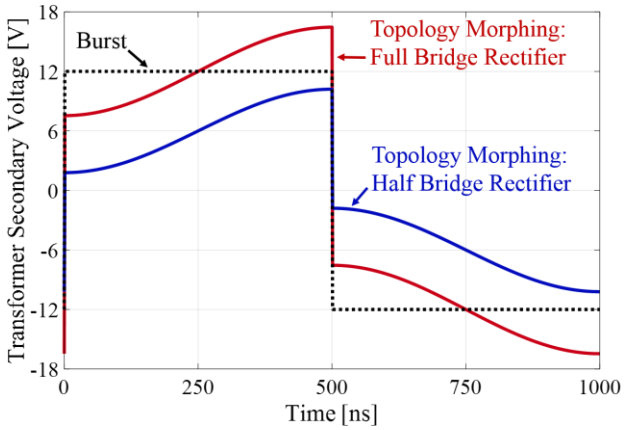


Figure 5.11: Voltage across the secondary winding of the transformer in the conventional burst-mode control (black), with the resonant capacitor C_r on the transformer's primary side, and in the proposed topology morphing control with a full-bridge rectifier (red) and a half-bridge rectifier (blue), both with the resonant capacitor moved to the transformer's secondary side to enable dc blocking. These curves are shown for an ICN converter operating at an input voltage V_{IN} of 18 V and an output voltage V_{OUT} of 12 V.

example shown in Fig. 5.11). In comparison, as discussed earlier, the proposed topology morphing control does require a dc-blocking capacitor, and a resonant capacitor is utilized for this purpose, as in the ICN converter of Fig. 5.2. Therefore, the voltage impressed across the transformer secondary in this control scheme is the sum of the rectifier input voltage – a square wave – and the voltage across the resonant/dc-blocking capacitor $C_{r,\mathrm{DC}}$, which can be modeled as a sine wave with a dc bias, resulting in the waveforms shown in Fig. 5.11. Figure 5.11 demonstrates that under both the conventional burst-mode and the proposed topology morphing control schemes, the transformer secondary voltage is not well-approximated by a sinusoid. Therefore, unlike the inductor core losses evaluated above, the basic Steinmetz equation cannot provide an accurate prediction of the transformer's core losses. Here, the transformer core losses are evaluated using the more accurate improved generalized Steinmetz equation (iGSE) [127]. Unlike the basic Steinmetz equation which requires only the peak flux density in the core, the iGSE requires an additional integral involving the instantaneous slope of the flux density; as a result, concise analytical expressions for loss comparison similar to (5.11)-(5.14) are difficult to derive. Nonetheless, Appendix D provides a straightforward iGSE-based procedure to numerically compare the transformer core losses under the two control schemes. The procedure of Appendix D is applied to the transformer of the example step-down ICN converter design, and the results are plotted in Fig. 5.9(e). As can be seen, the proposed topology morphing control scheme reduces the transformer core losses over the entire operating range of this ICN converter, with a maximum reduction of over 60% and an average reduction of over 42%.

The reduction in transformer core losses also owes its origin to the rectifier being operated as a half-bridge for a substantial fraction of the operating range under the proposed control scheme. As evident from Fig. 5.11, the transformer secondary voltage is lower with a half-bridge rectifier than with a full-bridge rectifier (under both the proposed and the conventional control schemes). Therefore, the transformer core losses are also reduced in the proposed control scheme. The total losses in the example step-down ICN converter design including all the losses considered above are also computed under the two control schemes. It is found that the proposed topology morphing control scheme reduces the total losses in this ICN converter design, as shown in Fig. 5.9(e), with a peak loss reduction of over 43% and an average loss

reduction of 22%.

5.4 Closed-Loop Control Architecture

This chapter also introduces a closed-loop control architecture for ICN converters operated under the proposed multimode topology morphing control, as shown in Fig. 5.12. This architecture employs linear feedback control to drive the ICN converter with the full-bridge and half-bridge rectifier duty ratios (d_{FB} and d_{HB} in Fig. 5.12) that facilitate output voltage and power regulation, and the inverter and rectifier phase-shifts ($2\Delta_{\mathrm{FB}}$, $2\Delta_{\mathrm{HB}}$, $\Delta_{\mathrm{r,FB}}$ and $\Delta_{\mathrm{r,HB}}$ in Fig. 5.12) that facilitate soft-switching. In this architecture, the ICN converter's output voltage v_{OUT} is sensed and compared to its reference value $V_{\mathrm{OUT,ref}}$, and the error v_{e} is processed by a linear compensator (for example, a PI compensator). The output of the compensator v_{C} is then used to identify the required operating mode (full-bridge continuous, cyclic topology morphing, half-bridge continuous, half-bridge burst or shutdown), and to compute the corresponding full-bridge and half-bridge duty ratios d_{FB} and d_{HB}, as follows:

$$\text{If } v_{\mathrm{C}} = v_{\mathrm{C,max}} = 1 \rightarrow \text{Mode} = \text{Full Bridge Continuous} \rightarrow d_{\mathrm{FB}} = 1, d_{\mathrm{HB}} = 0. \tag{5.15}$$

$$\text{If } 0 \leq v_{\mathrm{C}} \leq 1 \rightarrow \text{Mode} = \text{Cyclic Topology Morphing} \rightarrow d_{\mathrm{FB}} = v_{\mathrm{C}}, d_{\mathrm{HB}} = 1 - v_{\mathrm{C}}. \tag{5.16}$$

$$\text{If } v_{\mathrm{C}} = 0 \rightarrow \text{Mode} = \text{Half Bridge Continuous} \rightarrow d_{\mathrm{FB}} = 0, d_{\mathrm{HB}} = 1. \tag{5.17}$$

$$\text{If } -1 \leq v_{\mathrm{C}} \leq 0 \rightarrow \text{Mode} = \text{Half Bridge Burst} \rightarrow d_{\mathrm{FB}} = 0, d_{\mathrm{HB}} = 1 + v_{\mathrm{C}}. \tag{5.18}$$

$$\text{If } v_{\mathrm{C}} = v_{\mathrm{C,min}} = -1 \rightarrow \text{Mode} = \text{Converter Shutdown} \rightarrow d_{\mathrm{FB}} = 0, d_{\mathrm{HB}} = 0. \tag{5.19}$$

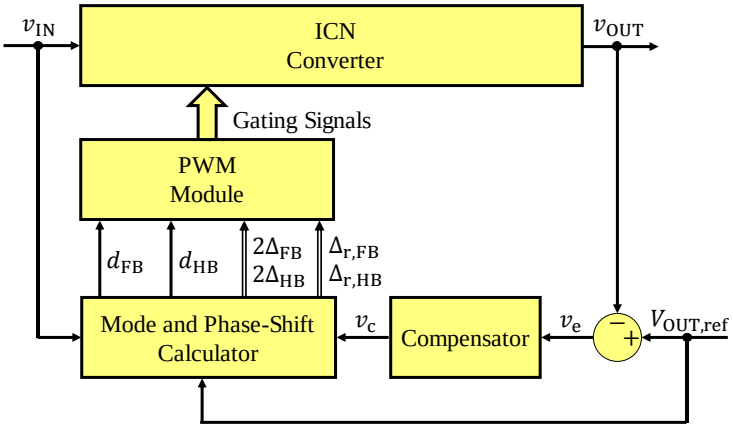


Figure 5.12: Closed-loop control architecture for multimode topology morphing control of ICN converter.

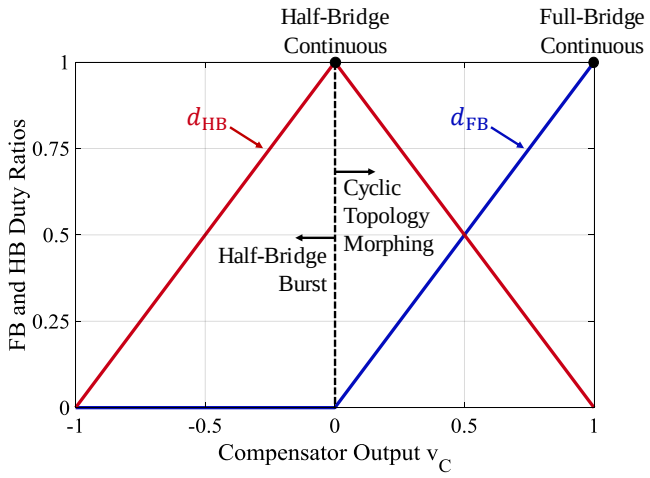


Figure 5.13: The full-bridge and half-bridge duty ratios (d_{FB} and d_{HB}) of the proposed topology morphing control as a function of the compensator output v_{C}.

The full-bridge and half-bridge duty ratios d_{FB} and d_{HB} computed using (5.15)-(5.19) are plotted as a function of the compensator output v_{C} in Fig. 5.13. As can be seen, the full-bridge and half-bridge duty ratios d_{FB} and d_{HB} are continuous functions of the compensator output v_{C}. In particular, there are no discontinues at the mode boundaries. This ensures that the transitions between the operating modes of the proposed topology morphing control are performed smoothly.

The inverter phase-shifts $2\Delta_{\mathrm{FB}}$ and $2\Delta_{\mathrm{HB}}$ in the control architecture of Fig. 5.12 are computed using (5.6) and (5.7), with the dc input voltage V_{IN} replaced by its sensed value v_{IN} and the dc output voltage V_{OUT} replaced by its reference value $V_{\mathrm{OUT,ref}}$. These inverter phase-shifts ensure ZVS and near-ZCS operation of the inverter transistors under steady-state operation. The rectifier phase-shifts $\Delta_{\mathrm{r,FB}}$ and $\Delta_{\mathrm{r,HB}}$ are selected to ensure that the rectifier transistors switch slightly later than the zero-crossings of the rectifier input current, hence, enabling ZVS and near-ZCS of the rectifier transistors. It is found that utilizing a rectifier phase-shift equal to half the inverter phase-shift (that is, $\Delta_{\mathrm{r,FB}} = \Delta_{\mathrm{FB}}$ and $\Delta_{\mathrm{r,HB}} = \Delta_{\mathrm{HB}}$) results in this desired behavior under steady-state operation without needing to sense the rectifier input current.

To evaluate the transient performance of the ICN converter under this closed-loop control architecture, a switching model of the converter and a controller are developed in the simulation tool PLECS [128]. The compensator is implemented as a PI compensator, and the proportional and integral constants are tuned to achieve the desired transient performance. The control functions including the PI compensator are then

experimentally implemented on a prototype ICN converter, as discussed in the next section.

5.5 Prototype Design and Experimental Results

A 1-MHz step-down isolated ICN resonant converter having the topology shown in Fig. 5.2 and a design similar to the example evaluated in Section 5.3 has been built and tested for the following specifications: an input voltage of 18 V to 36 V, an output voltage of 12 V, and a rated output power of 120 W. The prototype ICN converter is suitable as an intermediate bus converter in a power distribution system for telecommunications equipment, as shown in Fig. 5.14. Figure 5.15 shows a photograph of this prototype ICN converter. Details of the components used in the prototype converter are shown in Table 5.2. Note that the component values of the prototype ICN converter are similar to those of the design analyzed in Section 5.3 (see Table 5.1), with slight differences resulting from tuning of the resonant tank components to maximize the prototype converter's efficiency.

The prototype ICN converter is first operated under topology morphing control, with a topology morphing frequency f_{morph} of 1 kHz. Figure 5.16(a) shows the measured periodic steady-state switching waveforms for the inverters and rectifier of the ICN converter operating with 18 V input voltage and delivering 120 W output power. At this operating point the converter operates continuously in full-bridge

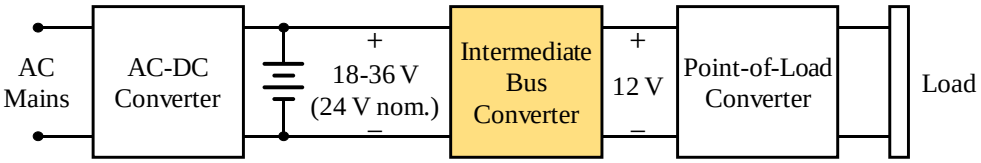


Figure 5.14: Application of the proposed ICN converter as an intermediate bus converter in a power distribution system for telecommunications equipment.

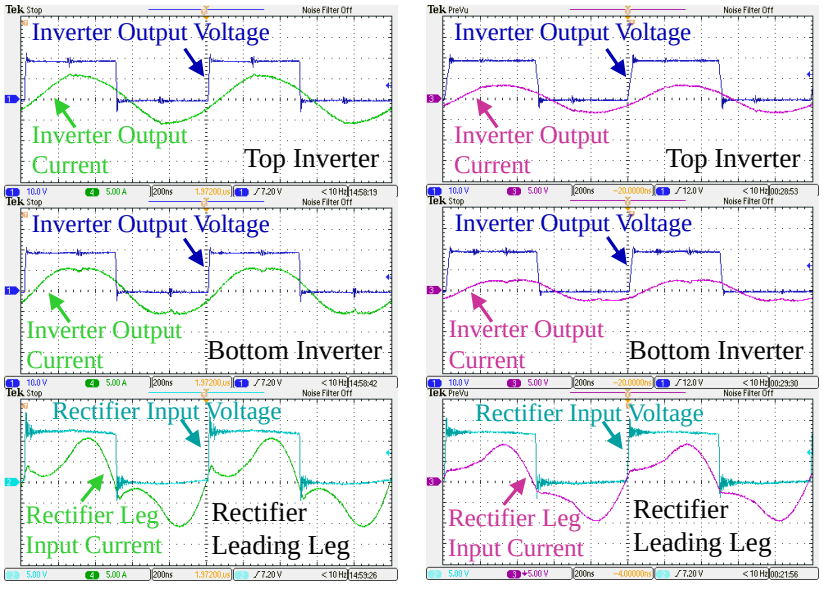
Figure 5.15: Photograph of the prototype ICN converter.

TABLE 5.2

COMPONENTS USED IN THE PROTOTYPE ICN RESONANT CONVERTER

Component	Value	Description
$Q_1 - Q_4$	–	EPC2001C 100-V/36-A eGaN FETs
$Q_5 - Q_8$	–	EPC2023 30-V/60-A eGaN FETs
L_{X1}	1.43 µH	4 turns of 2000-strand AWG-48 Litz wire RM10 Ferroxcube 3F46
C_{X1}	44 nF	NP0
L_{X2}	695 nH	3 turns of 2000-strand AWG-48 Litz wire RM10 Ferroxcube 3F46
C_{X2}	17.8 nF	NP0
Transformer	4:1	4 primary turns of 1000-strand AWG-48 Litz wire 1 secondary turn of 3000-strand AWG-48 Litz wire RM10 Ferroxcube 3F46 Leakage inductance used as L_r (646 nH).
$C_{r,DC}$	416 nF	NP0
C_{OUT}	5.1 mF	Electrolytic

mode. As can be seen from Fig. 5.16(a), all the inverter and rectifier transistors achieve ZVS and near ZCS operation. Figure 5.16(b) shows the measured waveforms of the ICN converter at an input voltage of 18 V and output power of 60 W; here, the ICN converter operates continuously in the half-bridge mode. Again all transistors operate with ZVS and near-ZCS. In the cyclic topology morphing mode, the converter



(a) (b)

Figure 5.16: Steady-state switching waveforms of the ICN converter when operating at $V_{IN} = 18$ V and $V_{OUT} = 12$ V with the rectifier operating in (a) full-bridge mode, and (b) half-bridge mode.

alternates between the waveforms of Figs. 5.16(a) and 5.16(b), and therefore maintains ZVS and near-ZCS operation. ZVS and near-ZCS operation is also maintained in the half-bridge burst-mode, and the converter waveforms are identical to those of Fig. 5.16(b) during its on time, except during a relatively short startup transient. The prototype converter is also operated under the conventional burst-mode control (with a burst frequency f_{burst} of 1 kHz), and its steady-state waveforms are identical to those in Fig. 5.16(a) during its on time.

The cyclic topology morphing mode of the proposed control scheme is illustrated by experimental waveforms at two example operating points in Fig. 5.17. The operating mode of the rectifier can be inferred in Fig. 5.17 from the switch-node voltage of the rectifier leg whose bottom transistor is kept turned on during the half-bridge mode (that is, $v_{\text{DS,Q8}} = 0$ indicates the half-bridge mode). As can be seen, the full-bridge-half-bridge transitions occur in a very small fraction of the topology morphing period, and the

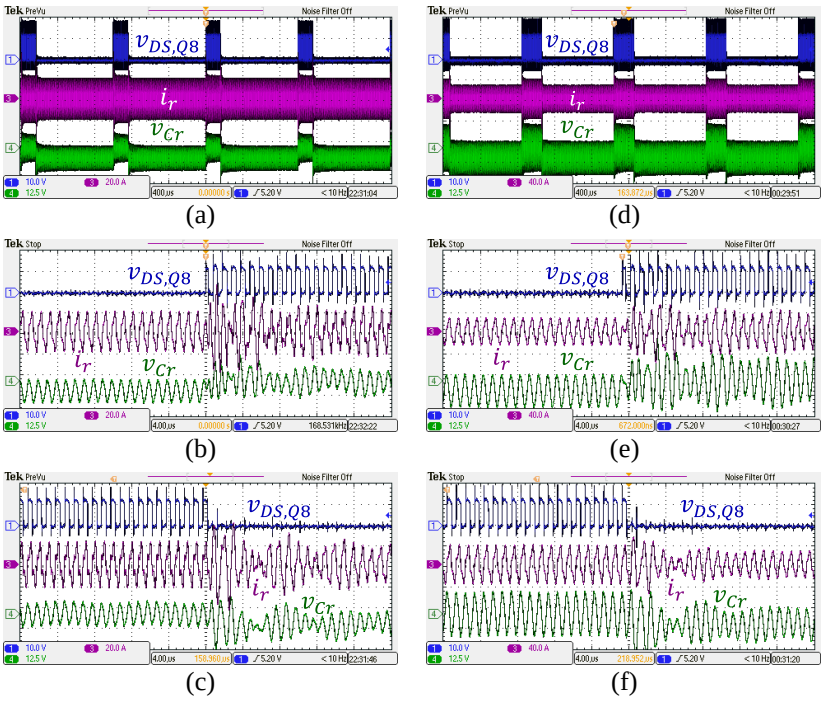


Figure 5.17: Cyclic topology morphing operation of the ICN converter at: (a)-(c) $V_{\text{IN}} = 18$ V, $V_{\text{OUT}} = 12$ V, $P_{\text{OUT}} = 72$ W, and (d)-(f) $V_{\text{IN}} = 36$ V, $V_{\text{OUT}} = 12$ V, $P_{\text{OUT}} = 108$ W. Here, (a) and (d) are long-timescale waveforms demonstrating several full-bridge-half-bridge transitions of the rectifier, (b) and (e) show one half-bridge-to-full-bridge transition, and (c) and (f) show one full-bridge-to-half-bridge transition. Waveforms shown are the switch-node voltage of the rectifier leg that is actively switched only in the full-bridge mode ($v_{\text{DS,Q8}}$), the input current of the other rectifier leg (i_{r}), and the voltage across the resonant/dc-blocking capacitor (v_{Cr}).

voltage across the dc blocking capacitor (v_{Cr}) quickly transitions from its average value of 0 in full-bridge mode to $-\frac{V_{\mathrm{OUT}}}{2}$ ($= -6$ V) in the half-bridge mode and vice versa, with the resonant ripple superimposed.

To demonstrate the improvement in power density that the proposed control scheme brings to the prototype ICN converter, the low-frequency component of the output voltage ripple is measured across the converter's operating range under both burst-mode control and topology morphing control. The measured output voltage ripple under the two control schemes is shown for two example operating points of the converter in Fig. 5.18. At an input voltage of 18 V and output power of 72 W (Figs. 5.18(a) and 5.18(b)), the measured output voltage ripple is 70.6% smaller in the proposed control scheme, which correlates well with the 76.2% ripple reduction predicted by (5.10). At an input voltage of 36 V and output power of 108 W (Figs. 5.18(c) and 5.18(d)), the measured ripple is 68.3% smaller in the proposed control scheme, which is also a good match with its analytical counterpart of 73.9%. Similarly substantial ripple reductions are observed across the entire operating range of the prototype ICN converter. Under burst-mode control, the maximum measured output voltage ripple is found to be 956 mV, while that under topology morphing control is found to be 410 mV (in both cases, at an input voltage of 36 V and output power of 120 W). This

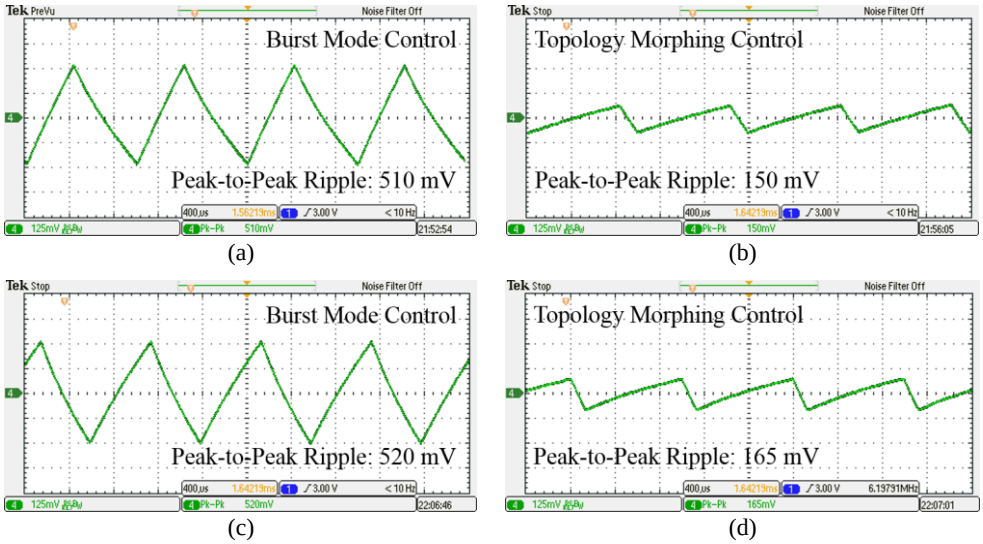


Figure 5.18: Output voltage ripple in the prototype ICN converter under the conventional burst-mode control and the proposed topology morphing control at two example operating points: (a), (b) $V_{\mathrm{IN}} = 18$ V, $V_{\mathrm{OUT}} = 12$ V, $P_{\mathrm{OUT}} = 72$ W, and (c), (d) $V_{\mathrm{IN}} = 36$ V, $V_{\mathrm{OUT}} = 12$ V, $P_{\mathrm{OUT}} = 108$ W. These waveforms show the low-frequency ac component $-\delta v_{\mathrm{OUT}}$ of the converter's output voltage.

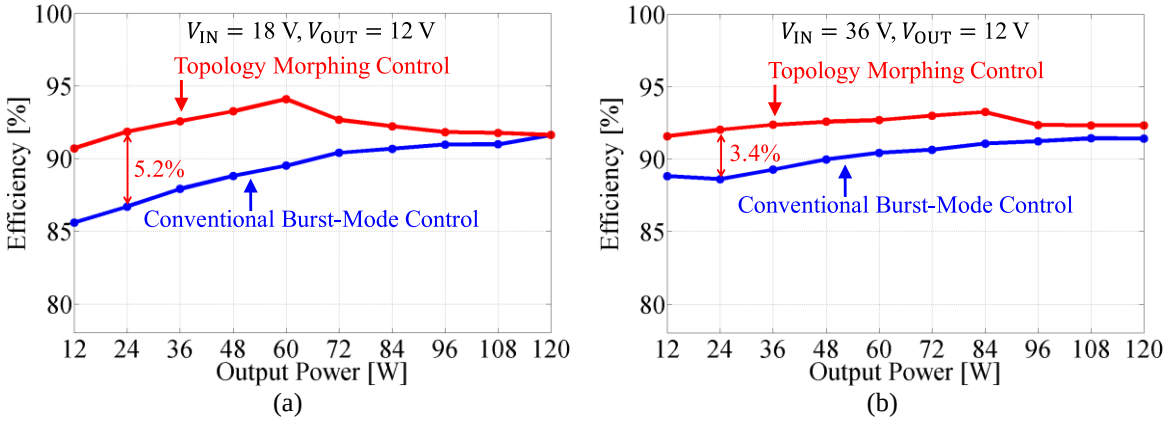
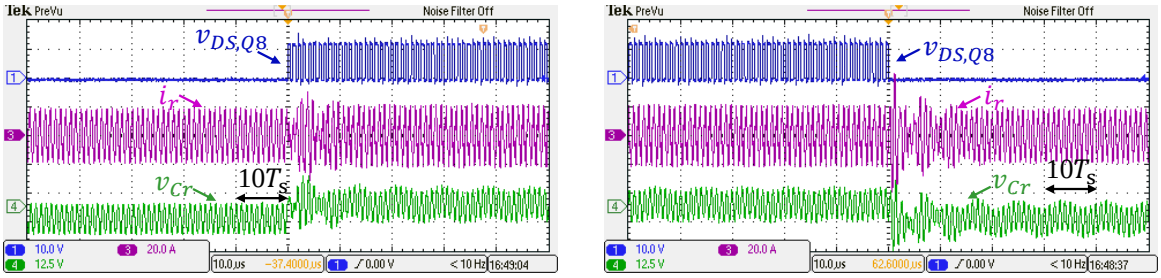


Figure 5.19: Measured efficiency of the ICN converter under topology morphing control and conventional burst-mode control across variations in output power at: (a) input voltage of 18 V, and (b) input voltage of 36 V.

corresponds to a reduction in maximum ripple, and hence, the required output capacitance, of 57%, which matches well with the analytically predicted capacitance reduction of 61%.

The efficiency of the prototyped converter has also been measured across its entire operating range under topology morphing and under conventional burst-mode control. A comparison between the measured efficiencies under the two control methods for the minimum and maximum input voltages of the converter, as a function of the output power, is shown in Fig. 5.19. It can be seen that the proposed control scheme improves the partial-power efficiency of the converter by up to 5.2% at the minimum input voltage, and up to 3.4% at the maximum input voltage. This corresponds to a loss reduction of up to 46.5% at the minimum input voltage, and up to 33% at the maximum input voltage, which compares well with the analytically predicted maximum loss reductions of 43.4% and 20.9% at the corresponding input voltages. The thermal benefits resulting from this loss reduction enable this ICN converter to be further reduced in size while maintaining lower operating temperatures and cooling requirements than those achievable with conventional burst-mode control.

Note that the topology morphing frequency of 1 kHz utilized in the prototype ICN converter is relatively low compared to its switching frequency of 1 MHz. As described earlier and further illustrated in Fig. 5.20, at this topology morphing frequency, the full-bridge-half-bridge transitions in the cyclic topology morphing mode of the proposed control approach consume a very small fraction of the topology morphing period.



(a) (b)

Figure 5.20: Full-bridge-half-bridge rectifier transitions in prototype 1-MHz ICN converter operating in the cyclic topology morphing mode of the proposed control approach with a topology morphing frequency of 1 kHz, at $V_{\mathrm{IN}} = 18$ V, $V_{\mathrm{OUT}} = 12$ V, $P_{\mathrm{OUT}} = 72$ W: (a) from half-bridge to full-bridge, and (b) from full-bridge to half-bridge. These waveforms demonstrate that at this operating point, the full-bridge-half-bridge transitions take up a total of less than 40 switching cycles (T_{s}), and hence, less than 4% of the topology morphing period ($T_{\mathrm{morph}} = 1000\ T_{\mathrm{s}}$).

Hence, the current oscillations and hard-switching events during these transitions minimally impact the converter's efficiency. On the other hand, higher topology morphing frequencies have the benefit of requiring smaller output capacitances (due to smaller output voltage ripples) and allowing higher control bandwidths. To investigate the impact of increasing the topology morphing frequency, the prototype ICN converter is tested in the cyclic topology morphing mode across a wide range of topology morphing frequencies (from 1 kHz to 20 kHz). The measured efficiency of the prototype converter as a function of the topology morphing frequency is shown for an example operating point in Fig. 5.21(a). It can be seen that as the topology morphing frequency increases, the efficiency decreases, falling by 1.6% across the 1 kHz – 20 kHz range. Figure 5.21(b) shows that the losses in the converter increase by up to ~24% over the same range. Depending on the cost and thermal management constraints of the application, such efficiency reductions and loss increases may be tolerable. In such cases, the topology morphing frequency can be appropriately increased to reduce output capacitor size and increase control bandwidth. In cases where such efficiency reductions are not desirable and high topology morphing frequencies are still required, it may be possible to reduce the losses associated with the full-bridge-half-bridge transitions using techniques similar to those utilized to reduce startup losses in the conventional burst-mode control [24].

The prototype ICN converter is also tested under closed-loop topology morphing control. The control functions, including a feedback PI compensator having a transfer function $G_c = K_{\mathrm{p}} + \frac{K_{\mathrm{i}}}{s}$ (with $K_{\mathrm{p}} = 0.25$

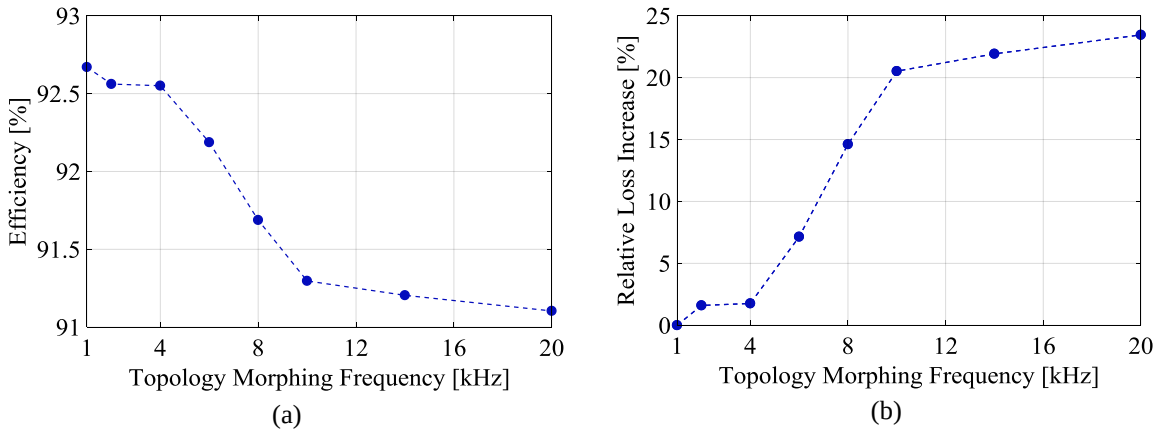


Figure 5.21: Performance of prototype ICN converter as a function of topology morphing frequency when operating in the cyclic topology morphing mode of the proposed control approach, at $V_{\mathrm{IN}} = 18$ V, $V_{\mathrm{OUT}} = 12$ V and $P_{\mathrm{OUT}} = 72$ W: (a) efficiency, and (b) percentage increase in losses relative to the losses at 1-kHz topology morphing frequency.

and $K_{\mathrm{i}} = 7.85$ selected based on the PLECS simulation), are implemented in a Texas Instruments Delfino TMS320F28379D microcontroller, and the control commands are updated once every topology morphing period. The microcontroller is on the primary side of the converter, and the rectifier gating signals are transmitted using NVE Corporation IL711 digital isolators. Figure 5.22 shows that the closed-loop controller successfully regulates the converter's output voltage under input voltage and load transients. In particular, Fig. 5.22(b) shows that even under a relatively large load transient (12% to 68% rated load), the controller is able to regulate the output voltage while maintaining smooth mode transitions.

5.6 Chapter Summary and Conclusions

This chapter introduces a new output voltage regulation scheme for impedance control network (ICN) resonant dc-dc converters in which the rectifier of the ICN converter dynamically alternates between full-bridge and half-bridge topologies. Compared to the conventional burst-mode control, this topology morphing control scheme enhances power density by reducing the output capacitance requirement in ICN converters, and substantially improves partial-power efficiencies. This chapter also introduces a closed-loop control architecture for the ICN converter, which ensures that the output voltage of the ICN converter stays well-regulated with smooth topology morphing mode transitions under input voltage and load variations. A prototype 1-MHz, 120-W step-down ICN resonant converter designed for an input voltage

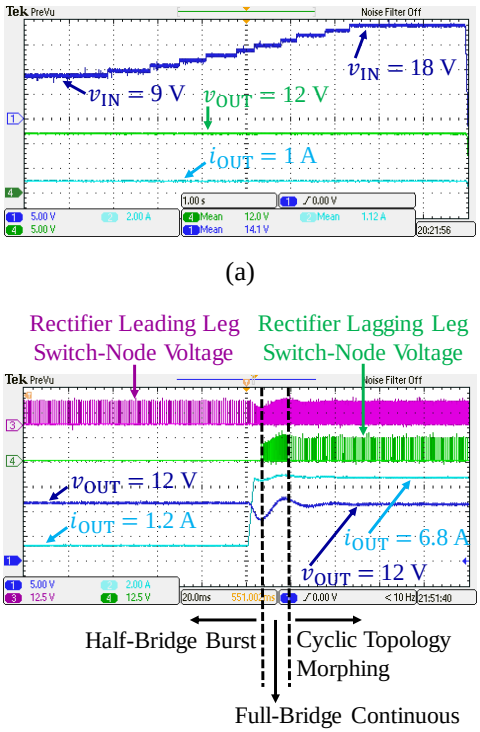


Figure 5.22: Output voltage regulation in the prototype ICN converter under: (a) input voltage ramp-up, and (b) large load transient at $V_{IN} = 18$ V.

range of 18 V to 36 V, an output voltage of 12 V, and a 10:1 output power range has been tested with both burst-mode control and the proposed topology morphing control. The topology morphing control reduces the output capacitance requirement in the prototype converter by over 57%, and reduces converter losses at partial power levels by up to 46.5%. The prototype ICN converter is also tested under closed-loop control using a digitally implemented controller, which is shown to regulate the converter's output voltage with smooth mode transitions under input voltage and load variations.

Chapter 6
ICN-Based Single-Stage Isolated 48V-to-1.8V Point-of-Load Converters

This chapter introduces single-stage isolated 48V-to-1.8V point-of-load (PoL) converters based on the ICN resonant converter architecture. These PoL ICN converters achieve large step-down while maintaining high efficiency across a wide range of input voltage and output power. Two PoL ICN converter topologies are developed. In the first converter topology, large step-down is achieved through a combination of stacked inverters, a transformer and a resonant current-doubler rectifier. The power density of this converter is enhanced by combining the three inductors of the ICN into a single integrated magnetic structure. In the second converter topology, stacked inverter are not employed, and a portion of the large step-down is instead achieved using an immittance network. The shunt inductance of this immittance network is realized using the magnetizing inductance of the converter's transformer, hence, not requiring any additional magnetic component. Furthermore, this transformer and the 1:1 transformer of the current-doubler rectifier are realized on a common core, resulting in an ICN converter with two magnetic structures. For both ICN converters, a design methodology based on 3D FEA analysis is employed to minimize winding and core losses in the magnetic components. Prototypes of both ICN converters are designed to operate over an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a rated output power of 90 W. The first ICN converter switches at 250 kHz, while the second ICN converter switches at 500 kHz. The first ICN converter prototype achieves a peak efficiency of 88.7% and maintains full-efficiencies above 87.6% across its nearly 2:1 input voltage range, and above 86.6% efficiency across a 10:1 output power range. The second ICN converter prototype achieves a peak efficiency of nearly 90%, maintains greater than 87.9% full-power efficiency across its nearly 2:1 input voltage range, and above 86.8% efficiency across its 10:1 output power range.

6.1 First Point-of-Load ICN Converter

A. Topology

The ICN converter topology presented in Chapter 3 can be utilized as a single-stage PoL converter. However, in a large step-down PoL application, this ICN converter will require a large turns-ratio transformer with high currents in its secondary winding. For instance, in a 90-W PoL application with 48 V input voltage and 1.8 V output voltage, this ICN converter requires a 20:1 transformer, with nearly 90 A peak current in its secondary winding. Designing such a transformer within reasonable size limits while maintaining low winding losses is very challenging. Furthermore, the ICN converter of Chapter 3 has a full-bridge rectifier, in which two rectifier transistors are always in series in the conduction path. In a PoL application with large output currents, this can result in unacceptably high conduction losses in the rectifier. Therefore, it is desirable to modify the ICN converter topology of Chapter 3, such that the burden of providing the large step-down is shared between multiple circuit components, and the transformer winding and rectifier conduction losses are reduced. One step in this direction is to utilize stacked inverters, as shown in the ICN converter of Fig. 6.1. Stacking the inverters in this manner halves the voltage at the inverter inputs, thus providing a step-down of a factor of two. As a result, the required transformer turns ratio is halved, enabling it to be designed more efficiently. The ICN converter of Fig. 2 can be further tailored for a large step-down PoL application by employing a current-doubler rectifier [130]. However, a conventional

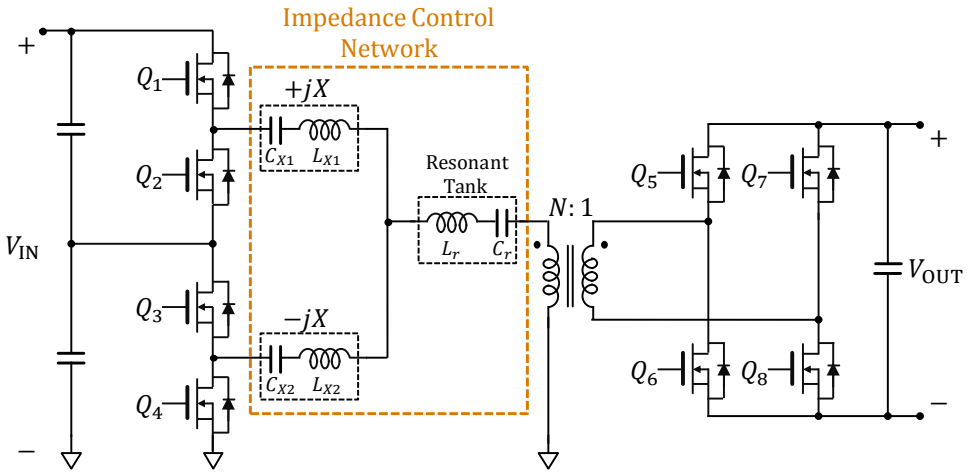


Figure 6.1: ICN resonant converter with stacked inverters.

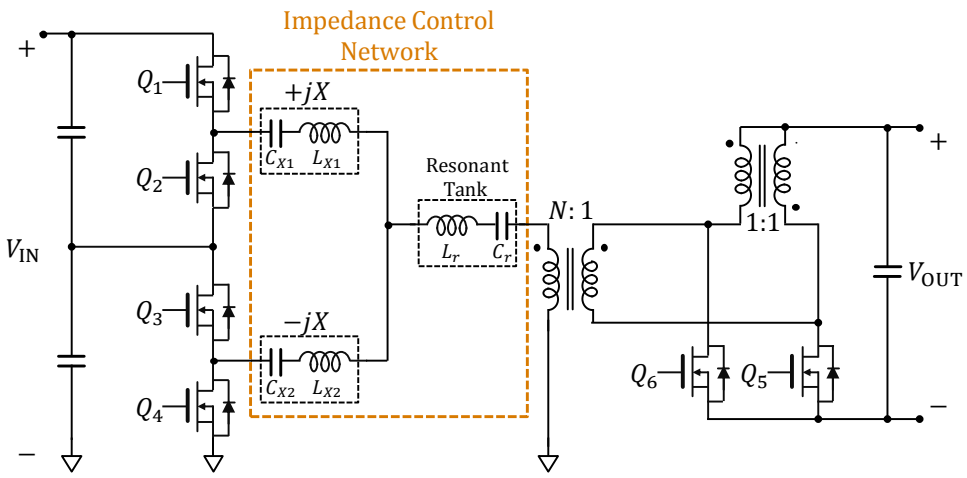


Figure 6.2: ICN resonant converter with stacked inverters and a resonant current-doubler rectifier.

current-doubler rectifier utilizes two relatively large-valued filter inductors carrying low-ripple current. Hence, it cannot be interfaced with the transformer of the ICN converter, in which the currents are of a sinusoidal nature. A resonant version of the current-doubler rectifier, presented in [131], is a suitable alternative. An ICN converter incorporating a resonant current-doubler rectifier is shown in Fig. 6.2. The resonant current-doubler rectifier comprises a 1:1 transformer and two transistors (shown as Q_5 and Q_6 in Fig. 6.2) that switch alternately with ~50% duty ratio. The converter's output current flows through the rectifier transistor that is switched on, and then splits equally between the secondary winding of the main transformer and one of the windings of the 1:1 transformer. Therefore, as opposed to carrying the full output current as in the case of a full-bridge rectifier, the secondary winding of the main transformer now carries half the output current, as illustrated in Fig. 6.3. Furthermore, this 1:2 step-up in current going from the transformer secondary to the converter output corresponds to a 2:1 step-down in voltage (also evident in Fig. 6.3), which corresponds to a further two-fold reduction in the required transformer turns ratio. Through this reduction in transformer secondary current and turns ratio, the resonant current-doubler rectifier enables a significant reduction in the transformer winding losses. Additionally, since only one transistor conducts at a time in this rectifier structure, it enables lower transistor conduction losses.

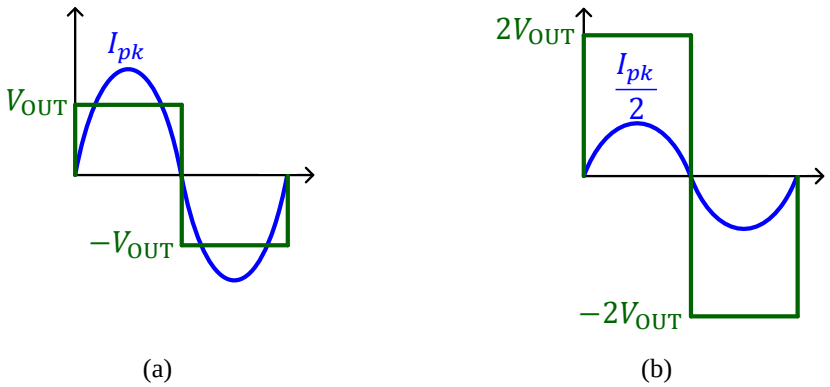


Figure 6.3: Transformer secondary voltage and fundamental-frequency current with: (a) full-bridge rectifier, and (b) resonant current-doubler rectifier, with both rectifier operating at the same output power level. Compared to the full-bridge rectifier, the current-doubler rectifier doubles the transformer secondary voltage by providing a voltage step-down of 2:1, and halves the transformer secondary current.

The ICN converter of Fig. 6.2 is well-suited for a large step-down PoL application; however, this converter requires five magnetic components, which may undesirably increase the converter's size. An effective way to reduce the size of this ICN converter is to combine the three ICN inductors into a single integrated magnetic structure utilizing two coupled windings, as described in Chapter 4. Utilizing this integrated magnetic structure, the ICN converter of Fig. 6.2 is further enhanced to the converter shown in Fig. 6.4. Note that the integrated magnetic structure shown in Fig. 6.4 has the coupling configuration shown previously in Fig. 4.3(a). The reasoning behind selecting this configuration is that for this large step-down

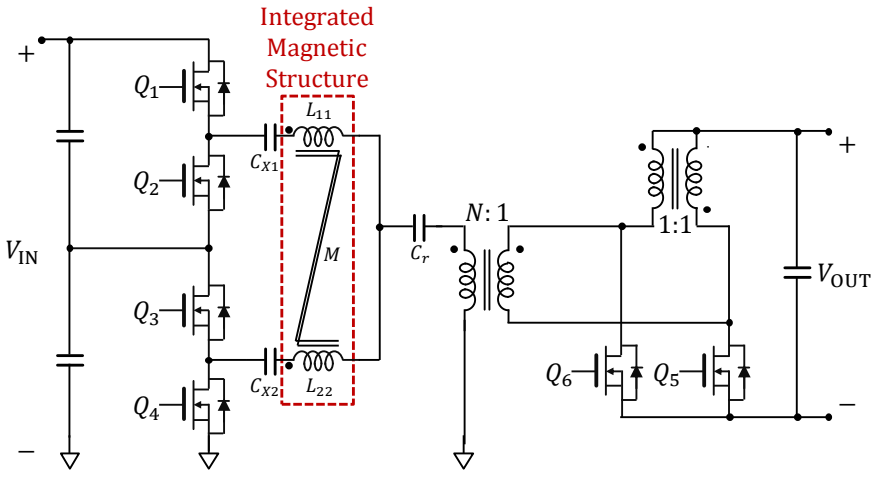


Figure 6.4: First PoL ICN converter topology, comprising stacked inverters, a resonant current-doubler rectifier, and a single integrated magnetic structure realizing the three ICN inductances.

ICN converter, the inverter output currents are relatively low, and come out to be lower at all operating points compared to the transformer primary current. Therefore, from a winding loss point of view, it is beneficial to utilize the coupling configuration shown in Fig. 6.4, which eliminates the discrete inductor L_{r} that carries the higher transformer primary current, as opposed to the inductors L_{X1} and L_{X2} that carry the lower inverter output currents.

B. Design Methodology

As with the ICN converters described earlier in this thesis, the two inverters of the proposed PoL ICN converter of Fig. 6.4 are also driven with a specific phase-shift between them, to enable ZVS and near-ZCS of the inverter transistors across wide operating ranges. For the proposed ICN converter, the required inverter phase-shift is given by:

$$2\Delta = 2\cos^{-1}\left(\frac{V_{\mathrm{IN}}}{8NV_{\mathrm{OUT}}}\right). \tag{6.1}$$

This expression is derived in Appendix A. When the inverters are controlled with the above phase-shift, the maximum output power that this ICN converter can deliver is given by:

$$P_{\mathrm{OUT,max}} = \frac{1}{\pi^2}\frac{V_{\mathrm{IN}}}{X}\sqrt{64N^2V_{\mathrm{OUT}}^2 - V_{\mathrm{IN}}^2}\,. \tag{6.2}$$

A derivation of this expression is also provided in Appendix A. The converter's output power is regulated below the maximum level given in (6.2) using burst-mode control.

The PoL ICN converter of Fig. 6.4 is designed in a manner similar to that described in Chapter 3. First, the transformer turns ratio N and the ICN differential reactance X are selected to satisfy two design objectives: 1) maintaining a flat output power profile by ensuring that the maximum power delivered by the ICN converter at its minimum and maximum input voltages is equal, and 2) ensuring that the converter is able to deliver its rated output power at its minimum input voltage, and hence, at all input voltages. Applying these design objectives to (6.2) results in the following expressions for the transformer turns ratio N and ICN differential reactance X:

$$N = \frac{\sqrt{V_{\mathrm{IN,min}}^2 + V_{\mathrm{IN,max}}^2}}{8V_{\mathrm{OUT}}}, \tag{6.3}$$

$$X = \frac{1}{\pi^2}\frac{V_{\mathrm{IN,min}}V_{\mathrm{IN,max}}}{P_{\mathrm{OUT,rated}}}. \tag{6.4}$$

Here, $V_{\mathrm{IN,min}}$ and $V_{\mathrm{IN,max}}$ are the minimum and maximum input voltages of the converter, respectively, and $P_{\mathrm{OUT,rated}}$ is the rated output power of the converter. Given values for N and X, the next step is to select the inductance and capacitance values for the three resonant tanks of the ICN converter. These are optimally selected using the enhanced augmented state-space analysis based design approach described in Chapter 3.

The inductance values of the three resonant tanks (L_{X1}, L_{X2} and L_{r}) are then used to determine the self and mutual inductances of the integrated magnetic structure that realizes the three inductors in the ICN converter of Fig. 6.4, in accordance with the relationships given in (4.3a), which are reproduced here for notational consistency:

$$L_{11} = L_{\mathrm{X1}} + L_{\mathrm{r}}\,, \tag{6.5a}$$

$$L_{22} = L_{\mathrm{X2}} + L_{\mathrm{r}}\,, \tag{6.5b}$$

$$M = L_{\mathrm{r}}\,. \tag{6.5c}$$

Here L_{11} and L_{22} are the self-inductances, and M is the mutual inductance of the two windings of the integrated magnetic structure.

The three magnetic components of the PoL ICN converter of Fig. 6.4 are implemented as planar PCB structures. Finite element analysis using Ansys Maxwell 3D is employed to determine field and current distributions and accurately predict winding and core losses. Models of the three magnetic components developed in Maxwell 3D are shown in Fig. 6.5. As can be seen in Fig. 6.5(a), an EI core geometry is employed for the integrated magnetic structure. Several commercially available planar EI core sizes smaller than a pre-specified maximum size are evaluated. For each core size, the number of turns in the two windings and the air-gaps in the core legs are selected to realize the required self and mutual inductances as given by (6.5). Winding and core losses are then computed for various degrees of paralleling of the turns.

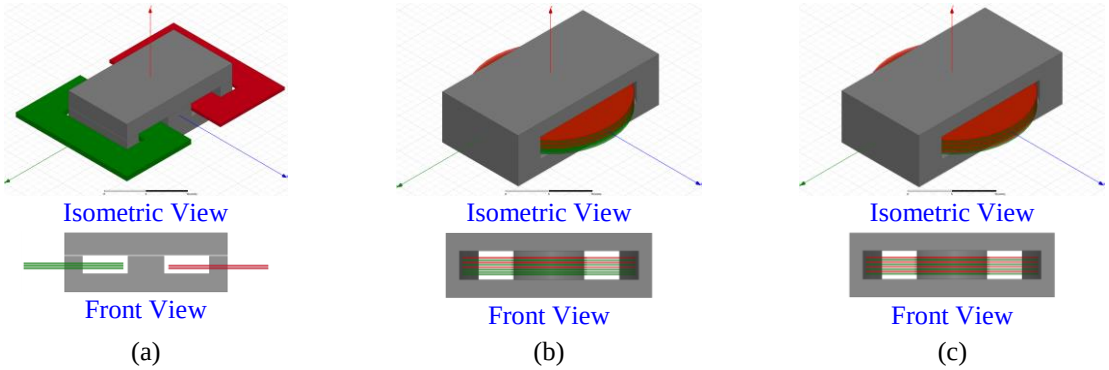


Figure 6.5: Models of the three magnetic components of the PoL ICN converter of Fig. 6.4 implemented in Maxwell 3D: (a) integrated magnetic structure, (b) main transformer, and (c) 1:1 resonant current-doubler transformer.

The core size and paralleling configuration that result in the lowest total losses are then selected. A similar optimization procedure is employed for the main transformer and the current-doubler transformer, for both of which planar ER core geometries are used, as shown in Figs. 6.5(b) and (c). To minimize winding losses, the main transformer is designed with a single-turn secondary winding, paralleled across multiple PCB layers. All possible configurations of interleaving the primary and secondary windings of this transformer are evaluated to select the configuration that results in the lowest winding losses. The two windings of the current-doubler transformer are also implemented as paralleled single turns. Since this transformer has a 1:1 turns ratio, its two windings are fully interleaved to minimize winding losses.

Once the three magnetic components are designed, a PCB layout for the proposed ICN converter incorporating the optimized winding configurations is created. The PCB windings are then exported to Maxwell 3D using Ansys SIwave. The PCB-exported models of the three magnetic components are shown in Fig. 6.6. As discussed in Chapter 4, simulating the structures at the layout level enables additional modes of losses to be captured, including the effect of vias and terminal connections.

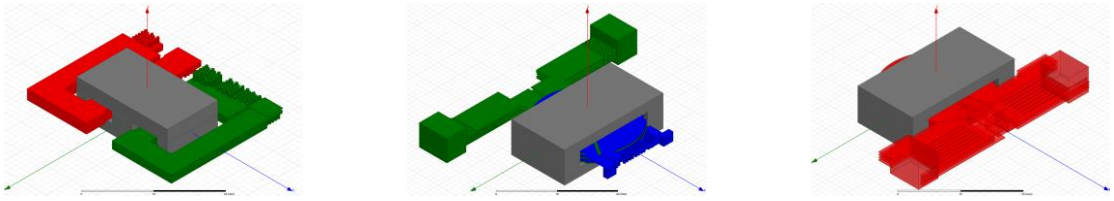


Figure 6.6: Maxwell 3D models of the three magnetic components of the PoL ICN converter of Fig. 6.4, with PCB-exported windings including vias and terminal connections: (a) integrated magnetic structure, (b) main transformer, and (c) 1:1 resonant current-doubler transformer.

C. Prototype Design and Experimental Results

A prototype ICN converter with stacked inverters and a resonant current-doubler rectifier, designed using the procedure outlined in the previous section is built and tested. This ICN converter is designed for an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a maximum output power of 90 W, suitable for a datacenter point-of-load application. The switching frequency of the prototype converter is 250 kHz. A photograph of the prototype converter is shown in Fig. 6.7. The prototype converter is implemented on an 8-layer PCB with 2 oz. copper in the top layer and 4 oz. copper in all other layers. This prototype has three planar PCB magnetic components: an integrated magnetic structure that realizes the three ICN inductances, a 5:1 main transformer, and a 1:1 current-doubler transformer. The designs of these magnetic components, optimized as described in the previous section, are summarized in Table 6.1. The stacked inverters in this prototype converter use EPC2016C 100-V/18-A enhancement-mode GaN

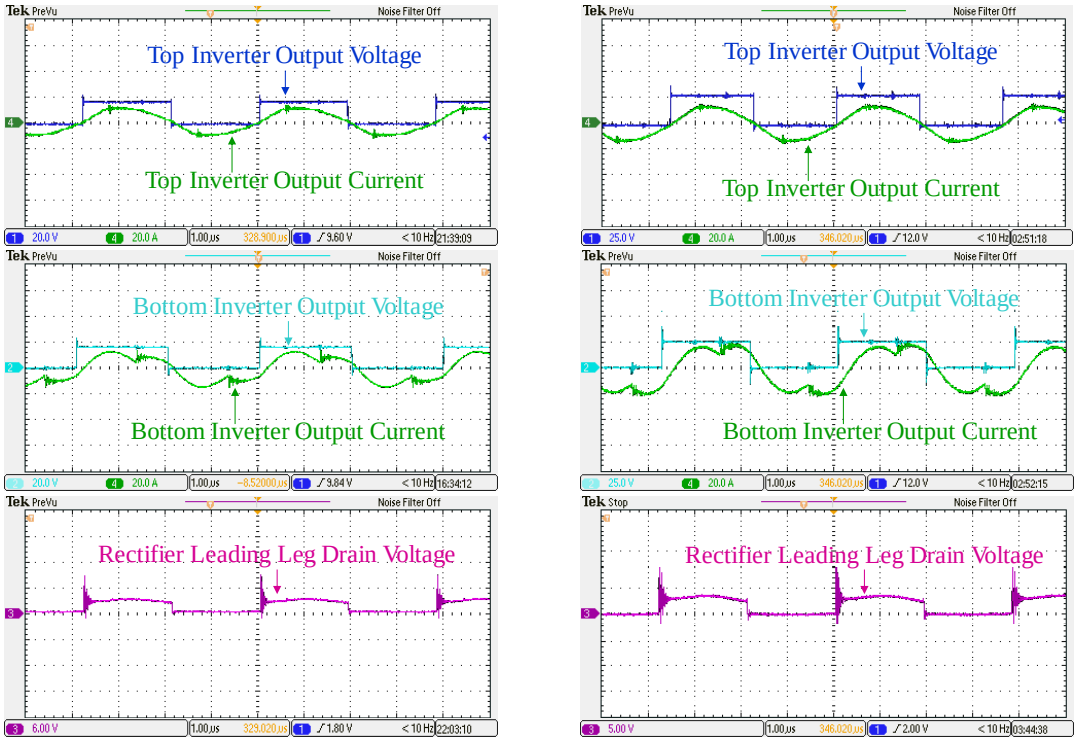
Figure 6.7: Photograph of the first 90-W PoL ICN converter prototype. Also shown for size comparison is a U.S. quarter.

TABLE 6.1
DESIGN DETAILS OF MAGNETIC COMPONENTS OF FIRST POINT-OF-LOAD ICN CONVERTER PROTOTYPE

Component	Core Geometry and Material	Details
Integrated Magnetic Structure	Ferroxcube E 18/4/10 with I 18/10/2, 3F36 material	Winding 1: 3 turns, in layers 3-8, adjacent layers in parallel Winding 2: 2 turns, in layers 1-8, adjacent layers in parallel Air-gap: 0.075 mm in all legs $L_{11} = 2.17$ µH, $L_{22} = 955$ nH, $M = 453$ nH
Main Transformer	Ferroxcube ER 23/3.6/13, 3F36 material	Primary: 5 turns, in layers 1, 3, 4, 6 and 7 Secondary: 1 turn, in layers 2, 5 and 8 (in parallel) Zero air-gap
Current-Doubler Transformer	Ferroxcube ER 23/3.6/13, 3F36 material	Primary: 1 turn, in layers 1, 3, 5 and 7 (in parallel) Secondary: 1 turn, in layers 2, 4, 6 and 8 (in parallel) Zero air-gap

transistors, with TI LM5113 half-bridge gate drivers. The two switches of the current-doubler rectifier are each realized using four EPC2023 30-V/60-A GaN transistors in parallel, and driven using two TI UCC27611 low-side gate drivers.

The prototype ICN converter has been tested across its entire operating range. All inverter and rectifier transistors achieve ZVS and near-ZCS across this operating range. Example switching waveforms demonstrating ZVS and near-ZCS operation with the converter delivering full power (90 W) at its minimum input voltage of 36 V and nominal input voltage of 48 V are shown in Fig. 6.8. The efficiency of the prototype ICN converter has also been measured across its full operating range, and shown in Fig. 6.9. As can be seen from Fig. 6.9(a), the converter maintains a high and flat full-power efficiency across its nearly 2:1 input voltage range, achieving a peak efficiency of 88.7% and a worst-case efficiency of 87.6%. Figure 6.9(b) shows that prototype converter also maintains greater than 86.6% efficiency across a 10:1 range of



(a) (b)

Figure 6.8: Inverter and rectifier switching waveforms of the first PoL ICN converter prototype while delivering 90-W output power at: (a) $V_{\mathrm{IN}} = 36$ V and $V_{\mathrm{OUT}} = 1.8$ V, and (b) $V_{\mathrm{IN}} = 48$ V and $V_{\mathrm{OUT}} = 1.8$ V.

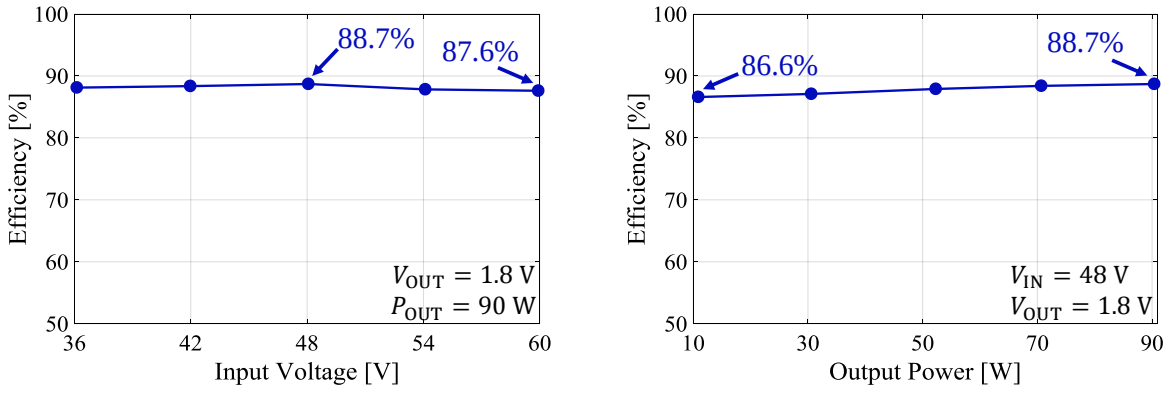


Figure 6.9: Measured efficiency of the first PoL ICN converter prototype: (a) as a function of its input voltage at full power ($P_{\mathrm{OUT}} = 90$ W), and (b) as a function of its output power at its nominal input voltage ($V_{\mathrm{IN}} = 48$ V). In both (a) and (b), the output voltage $V_{\mathrm{OUT}} = 1.8$ V.

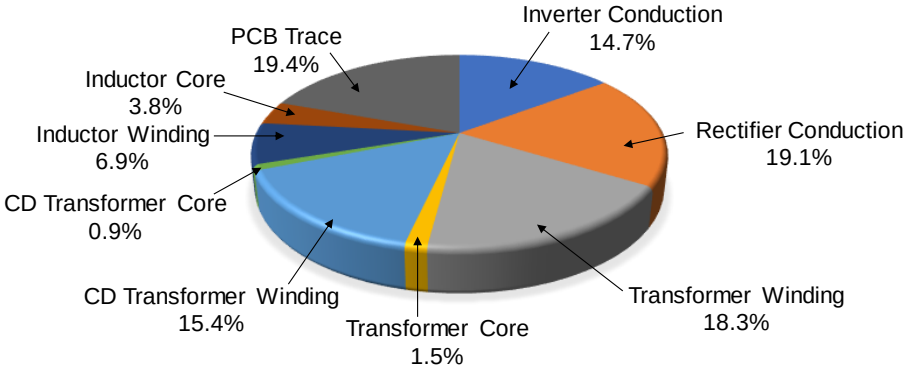


Figure 6.10: Theoretically predicted loss breakdown of the first PoL ICN converter prototype, operating at $V_{\mathrm{IN}} = 36$ V, $V_{\mathrm{OUT}} = 1.8$ V and $P_{\mathrm{OUT}} = 90$ W. Here, "IN" is an abbreviation for immittance network, and "CD" is an abbreviation for current-doubler.

output power. A theoretical loss breakdown of the prototype converter operating at an input voltage of 36 V, an output voltage of 1.8 V, and an output power of 90 W is shown in Fig. 6.10. As can be seen, the dominant portion of losses is contributed by winding losses in the two transformers, and by conduction losses in the current-doubler rectifier. PCB trace losses also account for a significant fraction of the total losses; most of these losses are in the high-current terminations and interconnects on the secondary side of the transformer.

One observation from the testing of this ICN converter prototype is that the input voltages of the two stacked inverters become unbalanced at some operating points. This is due to a slight mismatch between the loading impedances of the two inverters, which arises from deviations in the actual component values

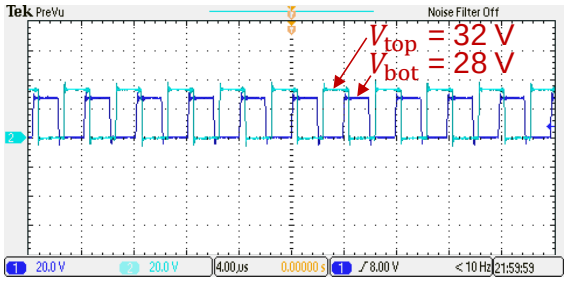


Figure 6.11: Output voltages of the two stacked inverters of the first PoL ICN converter prototype, with the converter operating at $V_{\mathrm{IN}} = 48$ V, $V_{\mathrm{OUT}} = 1.8$ V and $P_{\mathrm{OUT}} = 90$ W, demonstrating a mismatch between the two input voltages of the two inverters. The waveform labeled V_{top} is the output voltage of the top inverter, and the waveform labeled V_{bot} is the output voltage of the bottom inverter.

used in the prototype as compared to their ideal designed values. For example, the output voltages of the two stacked inverters are shown in Fig. 6.11, with the prototype converter operating at an input voltage of 60 V, output voltage of 1.8 V and output power of 90 W. As can be seen, there is a significant difference between the two inverter output voltages, and hence, the two inverter input voltages. This results in unbalanced inverter output currents, and hence, reduced efficiencies at higher input voltages, as noticeable in Fig. 6.9(a).

6.2 Second Point-of-Load ICN Converter

A. Topology

It is possible that the voltage imbalance between the stacked inverters of the ICN converter can be reduced using active voltage balancing techniques, at the cost of increased control complexity. This thesis presents an alternative approach, one that forgoes stacked inverters and instead obtains their 2:1 step-down using a matching network, as illustrated in Fig. 6.12. Since the current-doubler rectifier appears near-resistive under fundamental frequency analysis, the matching network in Fig. 6.12 is loaded near-resistively. For the ICN to function as desired (that is, to maintain near-resistive loading of the inverters), the input impedance of the matching network must also be near-resistive, regardless of the converter's operating conditions. A class of matching networks that satisfies this criterion is that of immittance networks [132]. An ICN converter incorporating a three-element immittance network is shown in Fig. 6.13. This immittance network comprises two capacitors having an impedance $-jX_{\mathrm{imt}}$, and a shunt inductor having equal but opposite

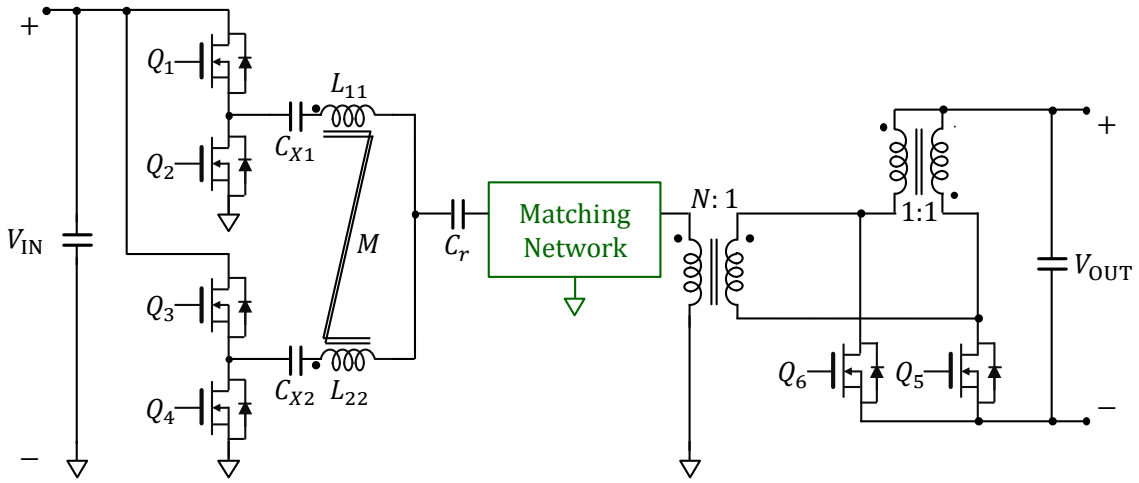


Figure 6.12: Impedance control network (ICN) resonant converter utilizing a matching network to provide voltage step-down.

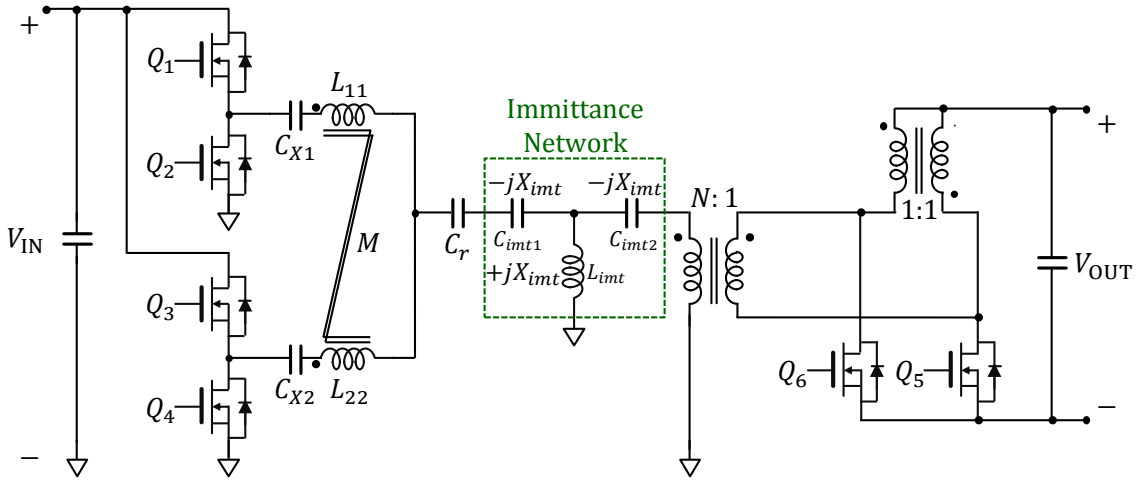


Figure 6.13: Impedance control network (ICN) resonant converter utilizing an immittance network to provide voltage step-down.

impedance $+jX_{\text{imt}}$ at the converter's switching frequency. When the reactance X_{imt} is appropriately selected, this immittance network can provide a greater than 2:1 voltage step-down over the entire operating range of the ICN converter, as shown in Fig. 6.14.

The ICN converter implementation of Fig. 6.13 requires four discrete magnetic components. The size of this ICN converter can be significantly reduced by combining three of these discrete magnetic components into a single integrated magnetic structure. First, the immittance network inductance L_{imt} in the ICN converter of Fig. 6.13 can be realized using the magnetizing inductance of the main transformer, resulting in the immittance network transformer shown in Fig. 6.15. Next, this immittance network transformer and

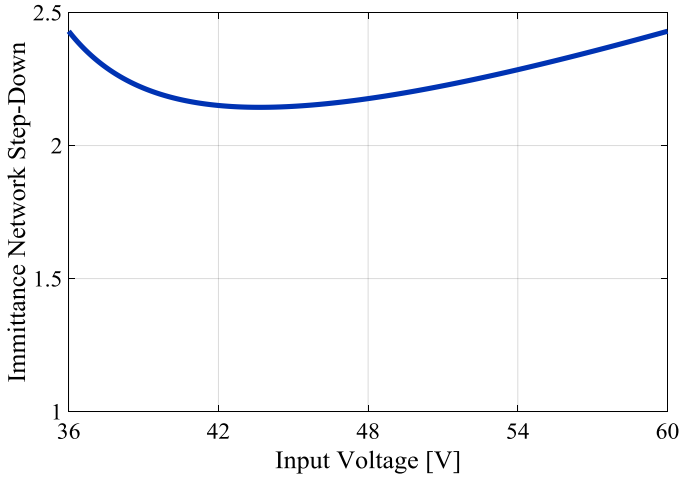


Figure 6.14: Voltage step-down provided by an immittance network in a 90-W POL ICN converter with an input voltage range of 36 V–60 V and an output voltage of 1.8 V. Here, the immittance network reactance X_{imt} is chosen to be 4 Ω.

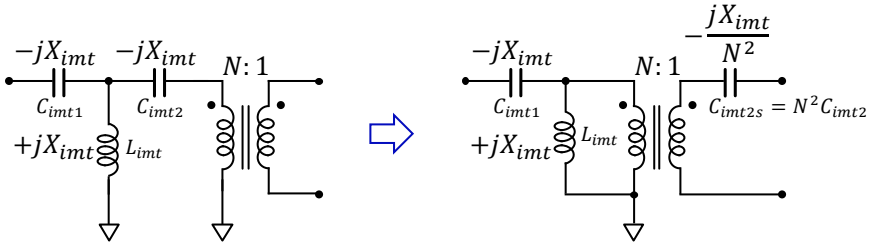


Figure 6.15: Magnetics integration in the proposed ICN converter: (a) the three ICN inductors realized using two coupled windings, and (b) the immittance network and transformer combined, with the immittance network inductance realized using the transformer's magnetizing inductance.

the 1:1 current-doubler transformer of the ICN converter can be implemented as a single integrated magnetic structure, as will be described in the next section. These enhancements result in the ICN converter of Fig. 6.16, which requires only two integrated magnetic components.

B. Design Methodology

To achieve ZVS and near-ZCS, the two inverters of the PoL ICN converter of Fig. 6.16 are also driven with a specific phase-shift between them. Due to the impedance inversion characteristic of the immittance network [132], the expression for this inverter phase-shift is markedly different from the ICN converters considered earlier, and is given by:

$$2\Delta = \cos^{-1}\left(1 - \frac{8X^2N^2V_{\text{OUT}}^2}{X_{imt}^2 V_{\text{IN}}^2}\right). \tag{6.6}$$

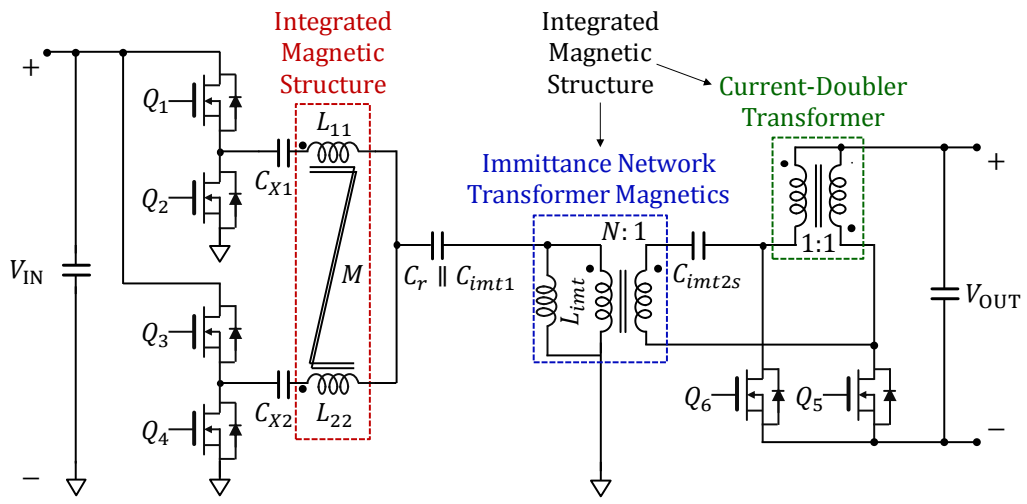


Figure 6.16: Second PoL ICN converter topology, comprising an immittance network transformer and a resonant current-doubler rectifier, with all magnetic components combined into two integrated magnetic structures. Note that one of the capacitances of the immittance network, C_{imt1}, is series combined with the resonant capacitor C_{r} and implemented as a single capacitor.

With this inverter phase-shift, the maximum output power that the PoL ICN converter of Fig. 6.16 can deliver is given by:

$$P_{\text{OUT,max}} = \frac{8}{\pi^2}\left(\frac{N}{X_{imt}}\right)\frac{V_{\text{IN}}^2}{X}\frac{V_{\text{OUT}}}{\sqrt{\frac{V_{\text{IN}}^2}{X^2} - 4\left(\frac{N}{X_{imt}}\right)^2 V_{\text{OUT}}^2}}. \tag{6.7}$$

Derivations of (6.6) and (6.7) are provided in Appendix A.

The design objectives for the PoL ICN converter of Fig. 6.16 are the same as those described in Section 6.1.B for the first PoL ICN converter, i.e., maintaining a flat output power profile and ensuring that the converter can deliver its rated power across its full operating range. The flat output power profile can be achieved again by designing the converter to deliver equal power at its minimum and maximum input voltages. However, ensuring the converter's ability to deliver its rated power across its full operating range requires additional analysis. Owing to the abovementioned impedance inversion characteristic of the immittance network, the maximum output profile of an ICN converter with an immittance network is a convex function of the input voltage, unlike all the ICN converters described earlier in this thesis, for which the maximum output power is a concave funtion of the input voltage. Therefore, for such an ICN converter,

the input voltage at which the maximum output power reaches its minimum value needs to be found. This can be done by setting the derivative of (6.7) with respect to the input voltage V_{IN} equal to zero, resulting in the following expression:

$$V_{\mathrm{IN}}|_{\min(P_{\mathrm{OUT,max}})} = \frac{2\sqrt{2}XNV_{\mathrm{OUT}}}{X_{\mathrm{imt}}}. \tag{6.8}$$

Based on the this analysis, the second design objective for the PoL ICN converter of Fig. 6.16 is to ensure that its maximum output power at the input voltage given by (6.8) equals its rated output power. These objectives can be satisfied by the following design relationships:

$$\frac{N}{X_{\mathrm{imt}}} = \frac{\pi^2}{16}\frac{P_{\mathrm{OUT,rated}}}{V_{\mathrm{OUT}}}\frac{\sqrt{V_{\mathrm{IN,min}}^2 + V_{\mathrm{IN,max}}^2}}{V_{\mathrm{IN,min}}V_{\mathrm{IN,max}}}, \tag{6.9}$$

$$X = \frac{8}{\pi^2}\frac{V_{\mathrm{IN,min}}^2 V_{\mathrm{IN,max}}^2}{(V_{\mathrm{IN,min}}^2 + V_{\mathrm{IN,max}}^2)P_{\mathrm{OUT,rated}}}. \tag{6.10}$$

The maximum output of the PoL ICN converter of Fig. 6.16, designed using the above relationships for the same voltage and power specifications as those discussed in Section 6.1, is shown in Fig. 6.17. It can be seen that the converter's output power remains fairly flat across its entire input voltage range, and that it can deliver the rated output power of 90 W over this range. The next step in the design methodology is to

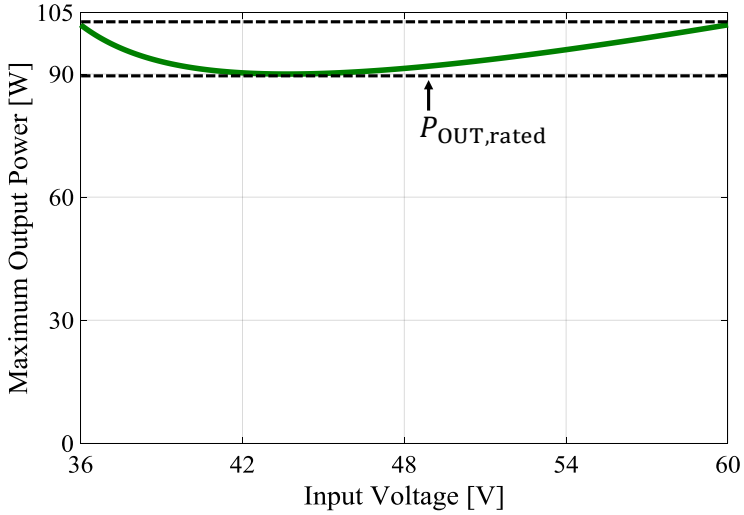
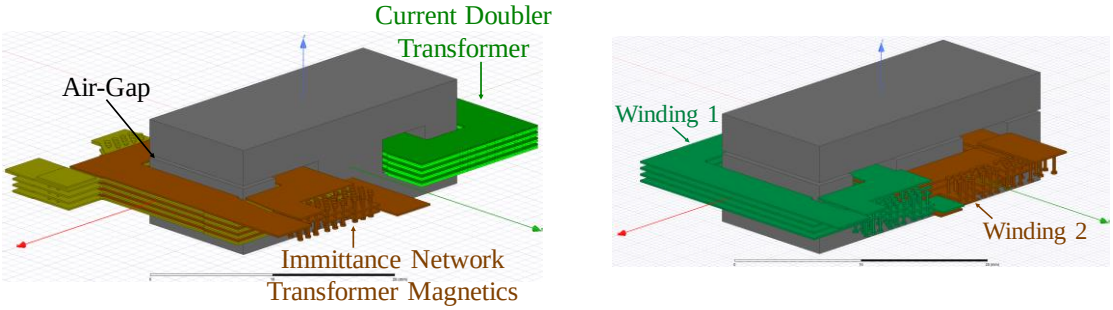


Figure 6.17: Maximum output power delivered by the PoL ICN converter of Fig. 6.16 over its input voltage range in a 36V-to-60V input, 1.8-V output, 90-W PoL application.

select the inductance and capacitance values for the three series resonant tanks of the ICN converter, which is done again using the enhanced augmented state-space analysis based design approach. These inductance values are then used to determine the required self and mutual inductances of the integrated magnetic structure that realizes the three ICN inductors in the converter of Fig. 6.16.

As described in the Section 6.2.A., the magnetic components of the PoL ICN converter of Fig. 6.16 are implemented using two integrated magnetic structures. Finite element analysis using Ansys Maxwell 3D is again employed to design and optimize these magnetic structures. A Maxwell 3D model of the integrated magnetic structure that implements the magnetics of the immittance network transformer and the 1:1 current doubler transformer is shown in Fig. 6.18(a). As can be seen, the core is selected to have an EI geometry, and the windings are realized as PCB traces. The two transformers are wound on the side legs of the core, and the center leg has zero air-gap to magnetically decouple the transformers from one another. To help realize the required transformer magnetizing inductance L_{imt} (and hence, the immittance network reactance X_{imt}), an air-gap is inserted in the core leg that implements the immittance network transformer, as shown in Fig. 6.18(a).

Note that the transformer turns ratio N and the immittance reactance X_{imt} only need to satisfy a particular ratio as given by (6.9); hence, presenting an opportunity to optimally select their values. In the design methodology presented here, the turns ratio N is varied over a wide range (from 1:1 to 10:1), and for each value of N, the air-gap in the immittance network transformer core leg (see Fig. 6.18(a)) is modified to



(a) (b)

Figure 6.18: Maxwell 3D models of the two integrated magnetic structures of the PoL ICN converter of Fig. 6.16: (a) immittance network and current-doubler transformers, (b) ICN inductors.

realize the required reactance X_{imt} such that the ratio $\frac{N}{X_{\text{imt}}}$ satisfies (6.9). Higher values of the turns ratio N correspond to a higher number of primary turns, resulting in higher winding losses. However, since the ratio $\frac{N}{X_{\text{imt}}}$ is fixed by (6.9), higher values of N also result in higher values of the immittance network reactance X_{imt}, which in turn leads to a larger magnetizing inductance L_{imt}, and hence, lower magnetizing currents and lower core losses. The combination of the turns ratio and reactance that results in the minimum total (winding and core) losses is then selected. A similar loss minimization strategy is employed for the 1:1 current doubler transformer, whose core leg has zero air-gap to maximize its magnetizing inductance (sse Fig. 6.18(a)). The second integrated magnetic structure that implements the three ICN inductors also utilizes an EI core geometry, as shown in Fig. 6.18(b). Here, the combination of the number of turns in the two windings and the air-gaps in the three core legs that results in the lowest total losses, while realizing the self and mutual inductances as given by (6.5), is selected.

C. Prototype Design and Experimental Results

A prototype PoL ICN converter utilizing the topology shown in Fig. 6.16, designed and optimized using the methodology outlined in the previous section, has been built and tested. Similar to the converter of Section 6.1, this converter is also designed to operate over an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a rated output power of 90 W. The switching frequency of the prototype converter is 500 kHz. A photograph of the prototype PoL ICN converter is shown in Fig. 6.19. The prototype converter utilizes two PCB-integrated magnetic structures; the design details of which are listed in Table 6.2. The inverters in the prototype converter use TI's LMG5200 GaN half-bridges with integrated gate drivers. The

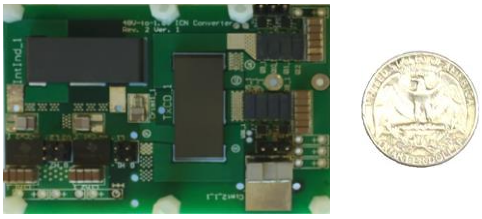


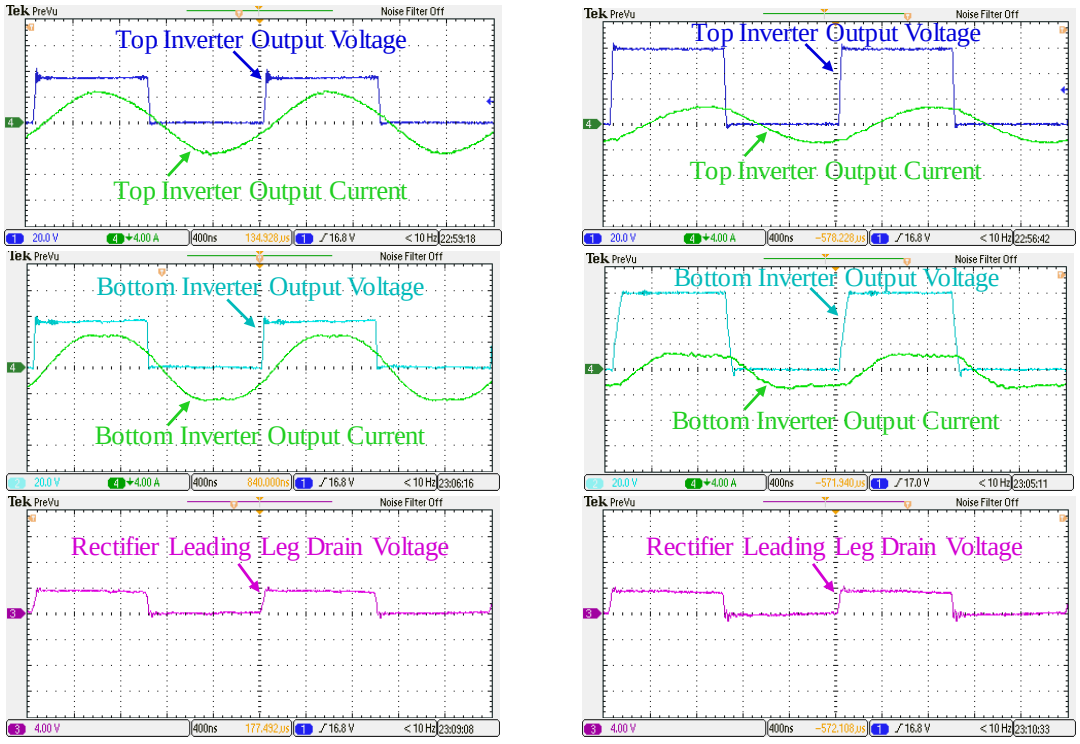
Figure 6.19: Photograph of the second 90-W PoL ICN converter prototype. Also shown for size comparison is a U.S. quarter.

TABLE 6.2
DESIGN DETAILS OF MAGNETIC COMPONENTS OF SECOND POINT-OF-LOAD ICN CONVERTER PROTOTYPE

Component	Core Geometry and Material	Details
Integrated ICN Inductors	Ferroxcube E 25/13/11 3F36 material	Winding 1: 3 turns, in layers 3-8, adjacent layers in parallel Winding 2: 2 turns, in layers 1-8, adjacent layers in parallel Air-gap: 0.1 mm in all legs $L_{11} = 5.02$ µH, $L_{22} = 3.64$ µH, $M = 2.29$ µH
Integrated Immittance Network Transformer and Current-Doubler Transformer	Ferroxcube E 25/13/11 3F36 material	Immittance Network Transformer Primary: 4 turns, in layers 1, 3, 5 and 7 Secondary: 1 turn, in layers 2, 4, 6 and 8 (in parallel) Air-gap: 3 mm
		Current-Doubler Transformer Primary: 1 turn, in layers 1, 3, 5 and 7 (in parallel) Secondary: 1 turn, in layers 2, 4, 6 and 8 (in parallel) Zero air-gap

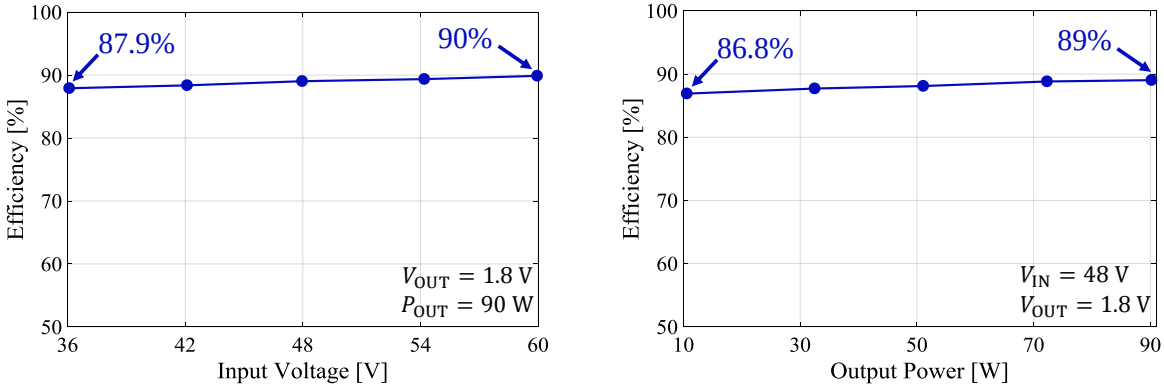
two switches of the current-doubler rectifier are each realized using four EPC2023 30-V/60-A GaN transistors in parallel, and driven using two UCC27611 low-side gate drivers.

Switching waveforms demonstrating soft-switching operation of the prototype converter while delivering full power at its minimum and maximum input voltages are shown in Fig 6.20. The efficiency of the prototype converter has also been measured across its entire input voltage range, as shown in Fig. 6.21. It can be seen from Fig. 6.21(a) that this second PoL ICN converter prototype achieves a high and flat full-power efficiency across its nearly 2:1 range of input voltage, with a worst-case efficiency of 87.9% and a peak efficiency of 90%. Figure 6.21(b) shows that the prototype converter also maintains a flat efficiency across output power variations, with greater than 86.8% efficiency across a 10:1 range of power. A theoretical loss breakdown of the prototype converter operating at an input voltage of 36 V, an output voltage of 1.8 V, and an output power of 90 W is shown in Fig. 6.22. Similar to the first prototype, winding losses in the two transformers and by conduction losses in the current-doubler rectifier again account for the major portion of the total losses.



(a) (b)

Figure 6.20: Inverter and rectifier switching waveforms of the second PoL ICN converter prototype while delivering 90-W output power at: (a) V_{IN} = 36 V and V_{OUT} =1.8 V, and (b) V_{IN} = 60 V and V_{OUT} =1.8 V.



(a) (b)

Figure 6.21: Measured efficiency of the second PoL ICN converter prototype: (a) as a function of its input voltage at full power (P_{OUT} = 90 W), and (b) as a function of its output power at its nominal input voltage (V_{IN} = 48 V). In both (a) and (b), the output voltage V_{OUT} = 1.8 V.

6.3 CHAPTER SUMMARY AND CONCLUSIONS

This chapter introduces two single-stage isolated 48V-to-1.8V point-of-load (PoL) converter topologies based on the ICN resonant converter architecture. The first ICN converter achieves large step-down using

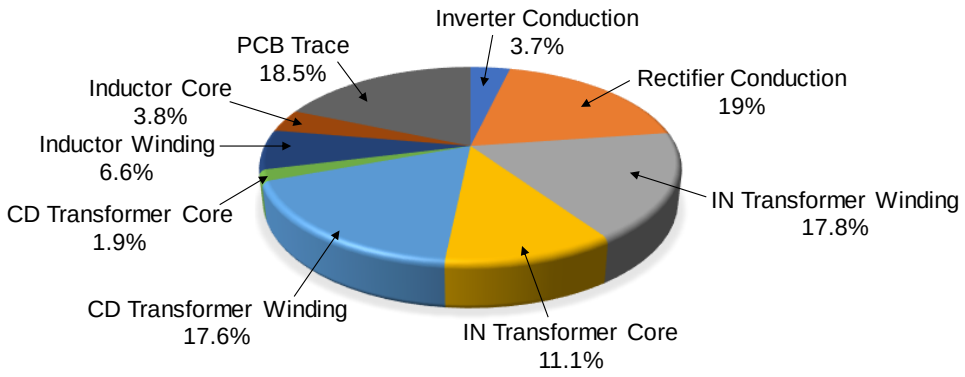


Figure 6.22: Theoretically predicted loss breakdown of the first PoL ICN converter prototype, operating at $V_{\mathrm{IN}} = 36$ V, $V_{\mathrm{OUT}} = 1.8$ V and $P_{\mathrm{OUT}} = 90$ W. Here, "IN" is an abbreviation for immittance network, and "CD" is an abbreviation for current-doubler.

a combination of stacked inverters, a transformer and a resonant current-doubler rectifier. The second ICN converter forgoes inverter stacking due to voltage balancing issues, and instead achieves a portion of its large step-down using an immittance network. To enhance power density, all the magnetic components of this converter are combined into two integrated magnetic structures. For both ICN converters, a design methodology based on 3D FEA analysis is employed to minimize winding and core losses in their magnetic components. Prototypes of both ICN converters are designed to operate over an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a rated output power of 90 W. The first ICN converter prototype achieves a peak efficiency of 88.7% and maintains full-efficiencies above 87.6% across the 2:1 input voltage range, and above 86.6% efficiency across a 10:1 output power range. The second ICN converter prototype achieves higher efficiencies, with a peak efficiency of 90%, greater than 87.9% full-power efficiency across the 2:1 input voltage range, and above 86.8% efficiency across the 10:1 output power range. The second prototype also has 25% smaller footprint than the first prototype. Based on the learnings from these converters, the next chapter develops a new PoL ICN converter with substantially higher efficiency and reduced size.

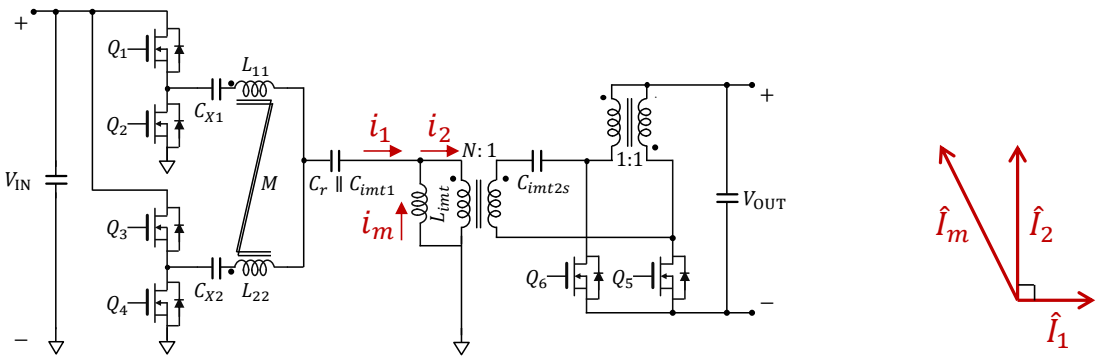
Chapter 7
High-Performance Single-Stage Isolated 48V-to-1.8V Point-of-Load Converter

This chapter presents a high-power-density high-efficiency single-stage isolated 48V-to-1.8V PoL converter based on the ICN resonant converter architecture. This converter achieves large step-down using a distributed transformer and an immittance network, and maintains high efficiency across wide operating ranges using the ICN architecture. To achieve high power density, the proposed converter utilizes rectifier phase-shift control that eliminates the need for bulky electrolytic capacitors, which are otherwise required in conventional ICN-based converters that utilize burst-mode (on/off) control. The converter's power density is further enhanced by implementing its inductors and transformer as planar integrated magnetic structures. These magnetic structures are designed and optimized using 3D finite-element analysis. A prototype single-stage PoL converter utilizing planar PCB-integrated magnetics is designed, built and tested for an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a maximum output power of 90 W. The prototype converter achieves a power density of 314 W/in^3, a peak efficiency of 92.6%, and maintains full-power efficiencies above 91.3% across its entire input voltage range.

7.1 Proposed Point-of-Load ICN Converter

A. Topology

It can be observed from the loss breakdown of the second PoL ICN converter prototype, shown in Fig. 6.22 of Chapter 6, that the core losses of the immittance network transformer account for more than 10% of the total converter losses. For a conventional transformer in this low-output-voltage (1.8-V) application, the core losses would be expected to be substantially lower. However, in the case of the immittance network transformer, the core losses are higher due to the mechanism by which the immittance network provides its voltage step-down (or current step-up). Consider Fig. 7.1, which illustrates the relationship between the



(a) (b)

Figure 7.1: Reason behind relatively large core losses in the immittance network transformer of the second PoL ICN converter: (a) converter topology illustrating the input, output and shunt-branch (magnetizing) currents of the immittance network transformer, and (b) phasor representation of these currents.

input, output and shunt-branch currents of the immittance network. The input and output currents of the immittance network are phase-shifted by 90° (see Fig. 7.1(b)). Assuming that the immittance network is designed to provide a voltage step-down of 2:1 (that is, a current step-up of 1:2), its output current has twice in magnitude of its input current. Owing to this 90° phase-shift and magnitude doubling, the current flowing in the shunt inductance of the immittance network has more than twice the magnitude of the input current, as shown in Fig. 7.1(b). Since this shunt inductance is actually the magnetizing inductance of the transformer, the result is a relatively high magnetizing current, and hence, relatively large core losses.

To mitigate this issue while maintaining the benefits of the step-down provided by the immittance network, an alternative implementation of the immittance network can be employed, as shown in the ICN converter of Fig. 7.2. This immittance network comprises two inductors having equal impedance $+jX_{\text{imt}}$ and a shunt capacitor having equal but opposite impedance $-jX_{\text{imt}}$ at the converter's switching frequency. The shunt-branch current of the immittance network no longer flows through the transformer's magnetizing inductance, hence, lowering core losses. However, it appears that this immittance network requires two additional inductors (L_{imt1} and L_{imt2}), which introduce their own penalties in efficiency and size. A closer examination reveals that one of these inductances, L_{imt1}, can simply be obtained from the third inductance resulting from the coupling of the ICN inductors, and the other inductance, L_{imt2}, can be obtained from the

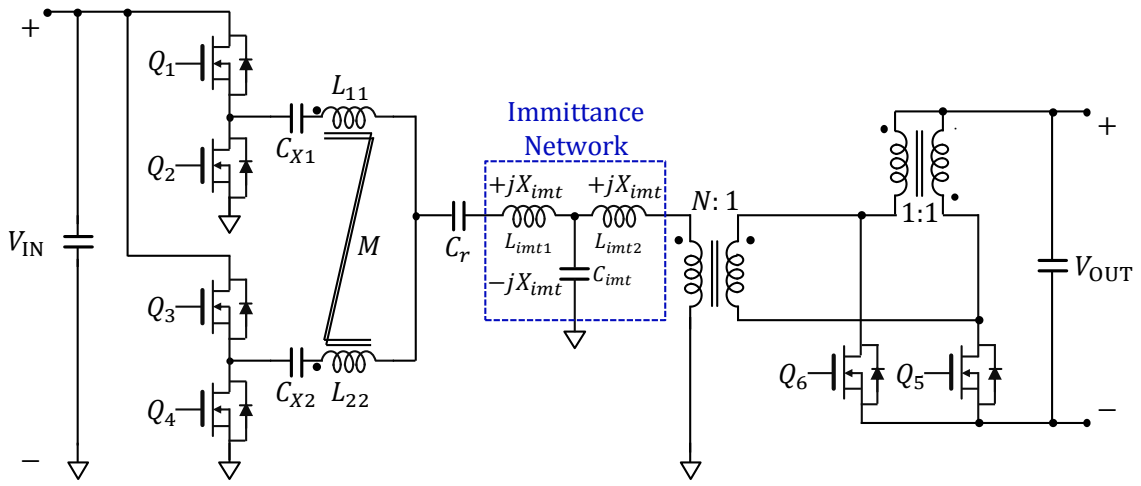


Figure 7.2: ICN converter with an alternative implementation of the immittance network.

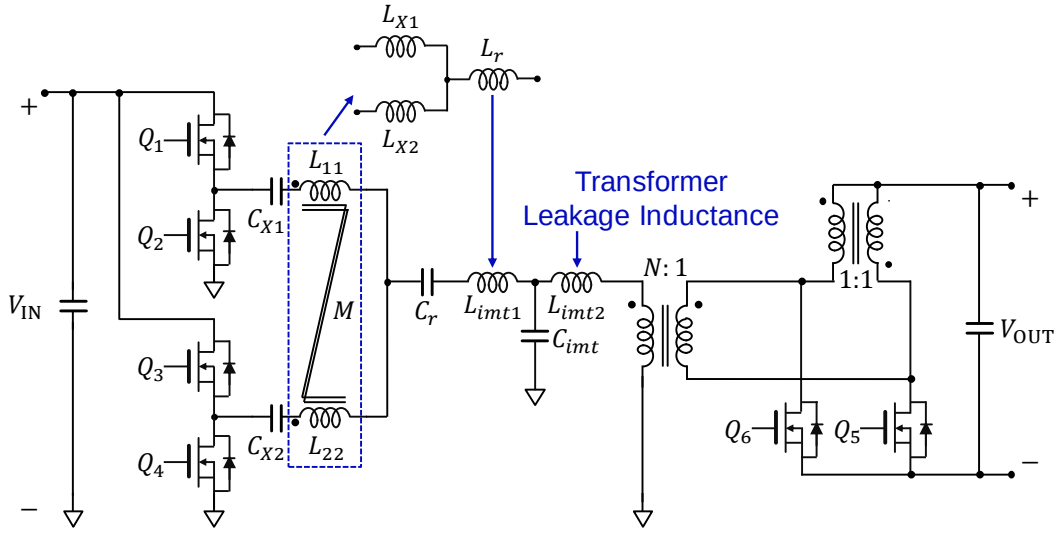


Figure 7.3: Realization of immittance network inductances using the coupling of the ICN inductances and the leakage inductance of the transformer.

leakage inductance of the transformer, as shown in Fig. 7.3. Hence, this immittance network does not require any additional magnetic components, resulting in the ICN converter topology shown in Fig. 7.4.

Other major sources of loss in the second PoL ICN converter prototype include winding losses in the immittance network transformer and PCB trace losses, which together account for more than 35% of the total converter losses. These losses exist primarily on the high-current secondary side of the transformer, and are substantially increased by skin and proximity effect losses in the interconnects and terminations of the paralleled secondary winding. An effective approach to reducing these losses is to utilize a distributed

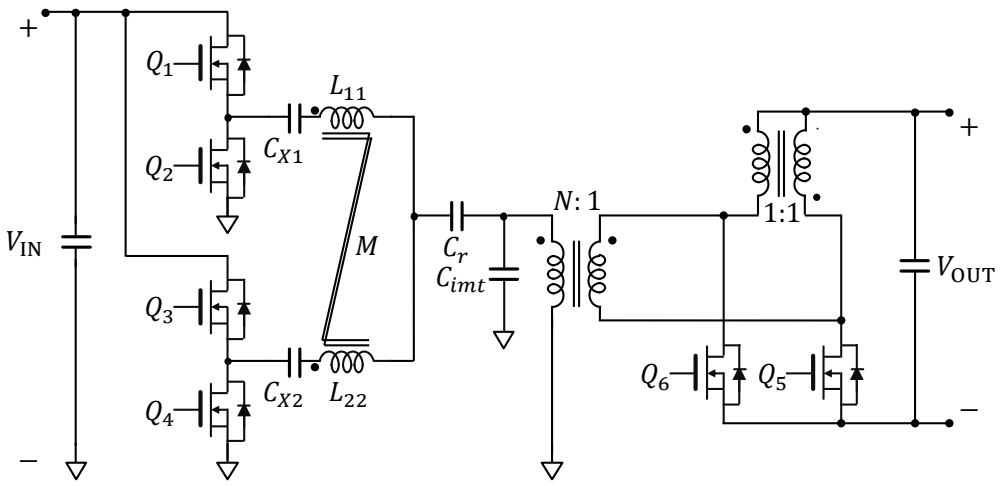


Figure 7.4: ICN converter with the inductances of its immittance network realized using the coupling of the ICN inductances and the leakage inductance of the transformer.

transformer structure, wherein multiple primary turns in series are each individually coupled to a secondary turn, and each secondary turn is individually connected to a rectifier. The outputs of the multiple rectifiers are then paralleled. A PoL ICN converter with this distributed transformer structure is shown in Fig. 7.5. As can be seen, in this converter the secondary-side currents are paralleled after rectification, hence, reducing the ac losses associated with the secondary-side winding interconnects and terminations.

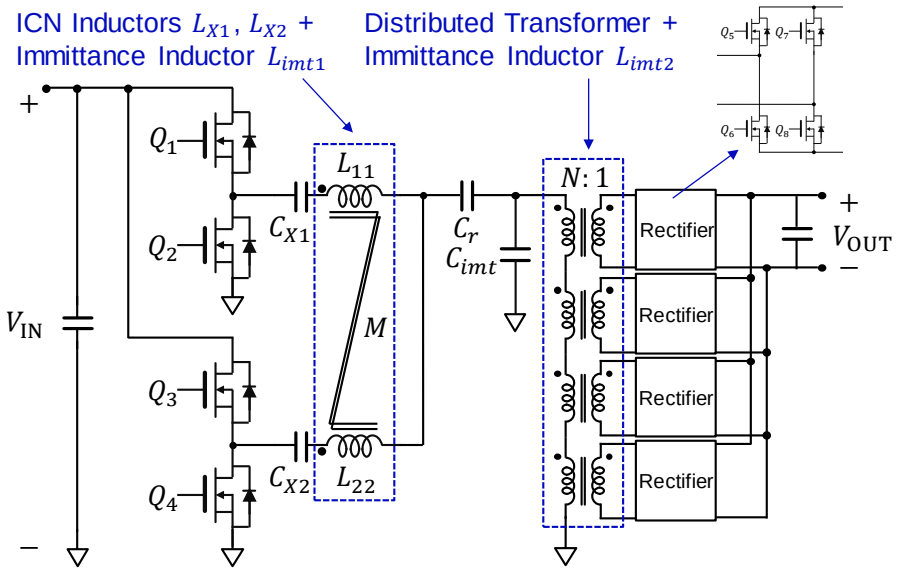


Figure 7.5: PoL ICN converter topology with two integrated magnetic structures, one realizing the ICN inductances L_{X1}, L_{X2} and the immittance network inductance L_{imt1}, and the other realizing a distributed transformer whose leakage inductance is utilized as the immittance network inductance L_{imt2}.

Another distinguishing feature of this PoL ICN converter as compared to the converters described in Chapter 6 is that this converter utilizes full-bridge rectifiers instead of a current-doubler rectifier. Since the transformer secondary currents are now distributed, each rectifier carries smaller currents and full-bridge rectifiers can provide acceptable efficiencies. Furthermore, full-bridge rectifiers allow the use of rectifier phase-shift control, which eliminates the need for bulky input and output capacitors, as described later in Section 7.1.C. The switching of the full-bridge rectifiers in the PoL ICN converter of Fig. 7.5 is synchronized, that is, the high- and low-side transistors of each rectifier switch at the same time as the corresponding transistors of the other rectifiers.

B. Design Methodology

To achieve ZVS and near-ZCS, the inverters in the PoL ICN converter of Fig. 7.5 are operated with a phase-shift of:

$$2\Delta = \cos^{-1}\left(1 - \frac{2N^2X^2V_{\mathrm{OUT}}^2}{X_{imt}^2V_{\mathrm{IN}}^2}\right). \tag{7.1}$$

With this inverter phase-shift, the maximum output power that this converter can deliver is given by:

$$P_{\mathrm{OUT,max}} = \frac{4}{\pi^2}\frac{N}{X_{\mathrm{imt}}}\frac{V_{\mathrm{IN}}^2}{X}\frac{V_{\mathrm{OUT}}}{\sqrt{\frac{V_{\mathrm{IN}}^2}{X^2} - \left(\frac{N}{X_{\mathrm{imt}}}\right)^2 V_{\mathrm{OUT}}^2}}. \tag{7.2}$$

The PoL ICN converter of Fig. 7.5 is designed in the same manner as the second PoL ICN converter of Chapter 6. First, the maximum output power delivered by the converter, as given by (7.2), is made equal at the minimum and maximum input voltages of the converter. Next, the input voltage at which the maximum output power reaches its minimum value is found by setting the derivative of (7.2) with respect to the input voltage V_{IN} to zero. For the PoL ICN converter of Fig. 7.5, this input voltage is given by:

$$V_{\mathrm{IN}}|_{\min(P_{\mathrm{OUT,max}})} = \frac{\sqrt{2}XNV_{\mathrm{OUT}}}{X_{\mathrm{imt}}}. \tag{7.3}$$

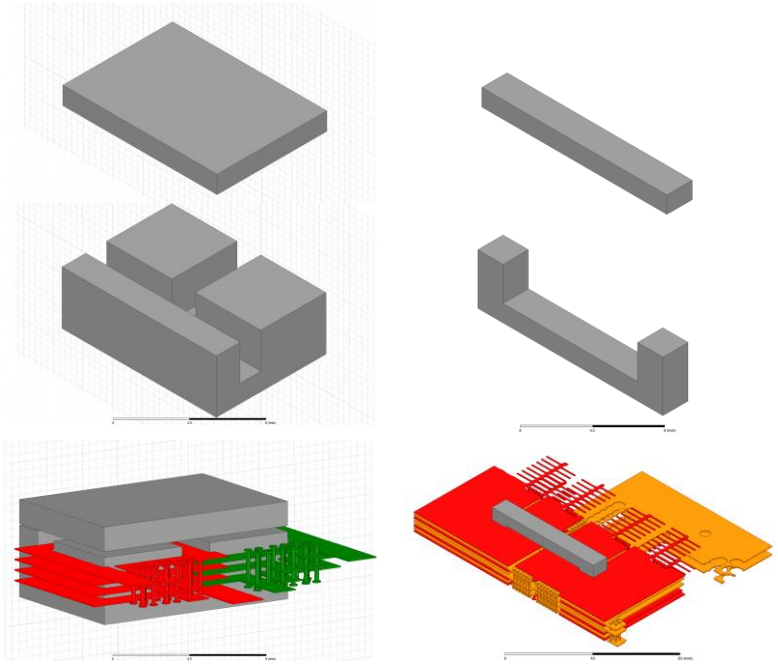
Finally, the maximum output power delivered by the converter at the input voltage given by (7.2) is set equal to its rated output power. This methodology results in the following design relationships for the PoL ICN converter of Fig. 7.5:

$$\frac{N}{X_{\text{imt}}} = \frac{\pi^2}{8}\frac{P_{\text{OUT,rated}}}{V_{\text{OUT}}}\frac{\sqrt{V_{\text{IN,min}}^2 + V_{\text{IN,max}}^2}}{V_{\text{IN,min}}V_{\text{IN,max}}}, \tag{7.4}$$

$$X = \frac{8}{\pi^2}\frac{V_{\text{IN,min}}^2 V_{\text{IN,max}}^2}{(V_{\text{IN,min}}^2 + V_{\text{IN,max}}^2)P_{\text{OUT,rated}}}. \tag{7.5}$$

The inductances and capacitances of the resonant tanks of the converter are then optimally selected using the enhanced augmented state-space analysis based procedure described in Chapter 4.

Various combinations of the transformer turns ratio N and immittance reactance X_{imt} can satisfy the design relationship given in (7.4) (similar to the case of the second PoL ICN converter of Chapter 6, which also utilized an immittance network). For the PoL ICN converter of Fig. 7.5, the optimal combination of N and X_{imt} can be selected based on the following arguments: higher values of N require a greater number of primary turns in the transformer, which may result in higher winding losses, and hence, reduced efficiency. At the same time, with a higher value of N, a proportionally higher value of X_{imt} is required to satisfy (7.4), which corresponds to a higher value of the immittance network inductances L_{imt1} and L_{imt2} (see Fig. 7.2). Since one of these inductances, L_{imt2}, is realized using the transformer's leakage inductance, larger L_{imt2} also requires the transformer to have a larger leakage inductance, which can further increase its winding losses [133]. Hence, to minimize the transformer's losses, it is beneficial to utilize as low a value of N as feasible. In the distributed transformer of Fig. 7.5 with four series-connected primary windings, the lowest feasible value of N, corresponding to one primary turn for each secondary turn, is four. With $N = 4$, the value of X_{imt} can be determined from (7.4). Note that the value of N can be further reduced by reducing the degree of distribution of the transformer, that is, by utilizing fewer windings and rectifiers. This comes at the cost of having each secondary winding process larger high-frequency ac currents, which can degrade efficiency and thermal performance. The optimal degree of distribution of the transformer for given converter specifications can be obtained through a detailed loss analysis, and for the application considered here, was found to be four.



(a) (b)

Figure 7.6: Ansys HFSS models of the integrated magnetic structures employed in the PoL ICN converter of Fig. 7.5: (a) integrated inductors, and (b) distributed transformer.

The integrated magnetic structures of the PoL ICN converter of Fig. 7.5 are realized as custom-shaped planar structures with PCB-integrated windings. These magnetic structures are designed and optimized using 3D finite-element analysis performed in Ansys HFSS. HFSS models of the magnetic structures are shown in Fig. 7.6. The integrated magnetic structure that realizes the three inductors L_{X1}, L_{X2} and L_{imt1} of the converter using two coupled windings (see Fig. 7.5) is shown in Fig. 7.6(a). As can be seen, this structure has two halves: an I-shaped top half and a custom-shaped bottom half with two parallel square-shaped legs and one orthogonal rectangular leg. The windings are wound on the square legs, and the number of turns in each winding as well as the air-gaps in the three legs are selected using an iterative procedure that minimizes the overall (winding + core) losses in the structure while ensuring that the required self and mutual inductances are obtained. This optimization procedure also captures the effect of vias and terminal connections by importing the inductor windings from the converter's PCB layout. A similar design and optimization procedure is utilized for the distributed transformer, which is implemented on a custom U-shaped core, as shown in Fig. 7.6(b). Two primary turns and their corresponding secondary turns are

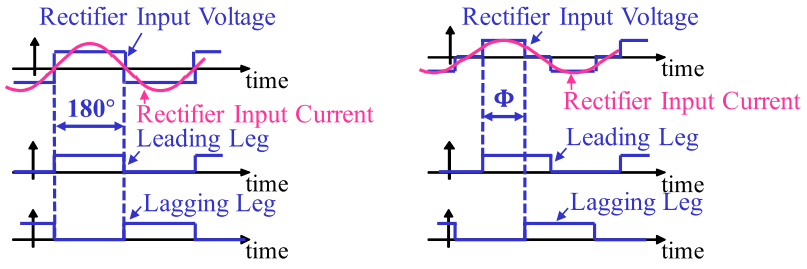
realized on each of the two legs of the U core. Each secondary turn comprises two paralleled turns, and the primary and secondary windings are interleaved to reduced proximity effect losses. Much of the leakage inductance required from the distributed transformer is obtained from traces that connect the bottom end of the primary winding to the input-side ground.

C. Control

The PoL ICN converters described in Chapter 6 utilize burst-mode control to regulate their output voltage and power. Burst-mode control allows these converters to maintain their soft-switching behavior across power levels. However, since the burst-mode (on/off) frequency is typically 1-2 orders of magnitude lower than the converter's switching frequency, large input and output capacitances are required to buffer the low-frequency ripple. The PoL ICN converter of Fig. 7.5 resolves this issue by utilizing an alternative regulation approach, introduced in [25]-[27]. In this approach, output voltage and power are regulated by allowing the phase-shift between the two legs of a full-bridge rectifier to change from a fixed 180° (as in a conventional full-bridge rectifier) to a variable Φ, as shown in Fig. 7.7. The output power delivered by the PoL ICN converter of Fig. 7.5 with a phase-shift of Φ between the two legs of each of its full-bridge rectifiers is given by:

$$P_{\mathrm{OUT}} = \frac{4}{\pi^2}\frac{N}{X_{\mathrm{imt}}}\frac{V_{\mathrm{IN}}^2}{X}\frac{V_{\mathrm{OUT}}\sin\frac{\Phi}{2}}{\sqrt{\frac{V_{\mathrm{IN}}^2}{X^2}-\left(\frac{N}{X_{\mathrm{imt}}}\right)^2 V_{\mathrm{OUT}}^2\sin^2\frac{\Phi}{2}}}. \tag{7.6}$$

A procedure to derive this expression for rectifier phase-shift controlled output power is provided in Appendix A. As can be seen from (7.6), as the rectifier phase-shift is increased from 0° to 180°, the output



(a) (b)

Figure 7.7: Rectifier phase-shift control of the PoL ICN converter of Fig. 7.5: (a) full-power operation, and (b) partial-power operation.

power monotonically increases from zero to its maximum value $P_{\mathrm{OUT,max}}$, as expressed in (7.2). In this control approach the converter's input and output capacitors only have to buffer the switching frequency ripple; hence, dramatically reducing the converter's input and output capacitance requirements and enhancing its power density. This rectifier phase-shift control also allows soft-switching of the inverter transistors to be maintained at partial power levels, provided the inverter phase-shift is modified to:

$$2\Delta = \cos^{-1}\left(1 - \frac{2N^2X^2V_{\mathrm{OUT}}^2\sin^2\frac{\Phi}{2}}{X_{imt}^2V_{\mathrm{IN}}^2}\right). \tag{7.6}$$

The procedure to derive this inverter phase-shift expression is also provided in Appendix A.

7.2 Prototype Design and Experimental Results

A prototype PoL ICN converter having the topology shown in Fig. 7.5, designed using the procedure outlined in the Section 7.1.B is built and tested. This converter is designed for an input voltage range of 36 V to 60 V, an output voltage of 1.8 V, and a maximum output power of 90 W, suitable for a datacenter point-of-load application. The switching frequency of the prototype converter is 1 MHz. A photograph of the prototype converter is shown in Fig. 7.8. This prototype has two planar PCB magnetic components: an integrated magnetic structure that realizes three of the converter's inductors, and a 4:1 distributed transformer with controlled leakage inductance. The ferrite core material used in the two magnetic components is Ferroxcube's 3F46. The inverters in the prototype converter are constructed using TI's LMG5200 half-bridge ICs with integrated gate drivers. For the full-bridge rectifiers, EPC2023 30-V/90-A enhancement-mode GaN transistors are utilized, with each half-bridge driven using TI's LM5113 gate drivers.

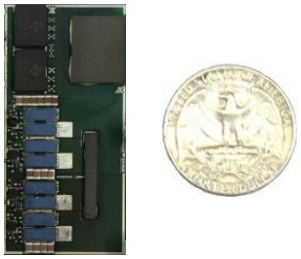
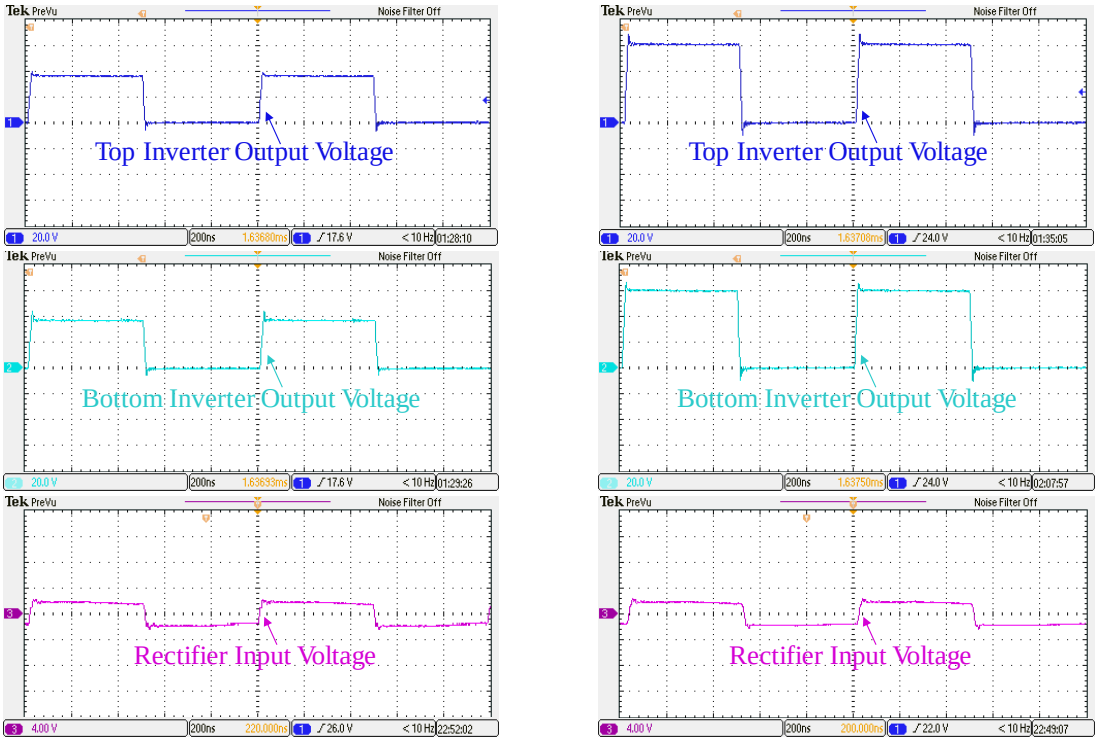


Figure 7.8: Photograph of the final 90-W PoL ICN converter prototype. Also shown for size comparison is a U.S. quarter.



(a) (b)

Figure 7.9: Inverter and rectifier switching waveforms of the final PoL ICN converter prototype while operating at: (a) V_{IN} =36 V and V_{OUT} =1.8 V, and (b) V_{IN} = 60 V and V_{OUT} =1.8 V.

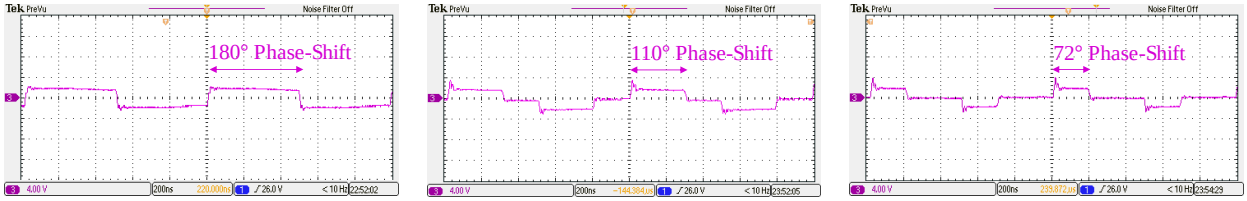
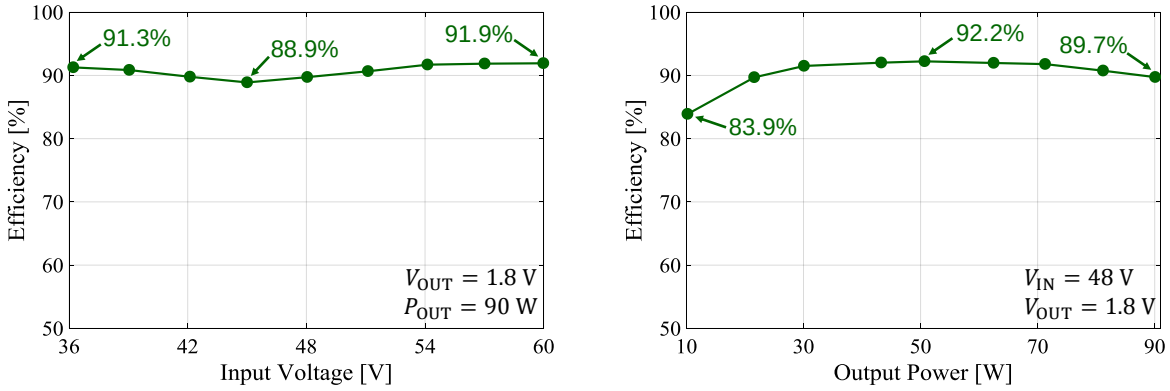


Figure 7.10: Rectifier input voltage under rectifier phase-shift control of the final PoL ICN converter prototype.

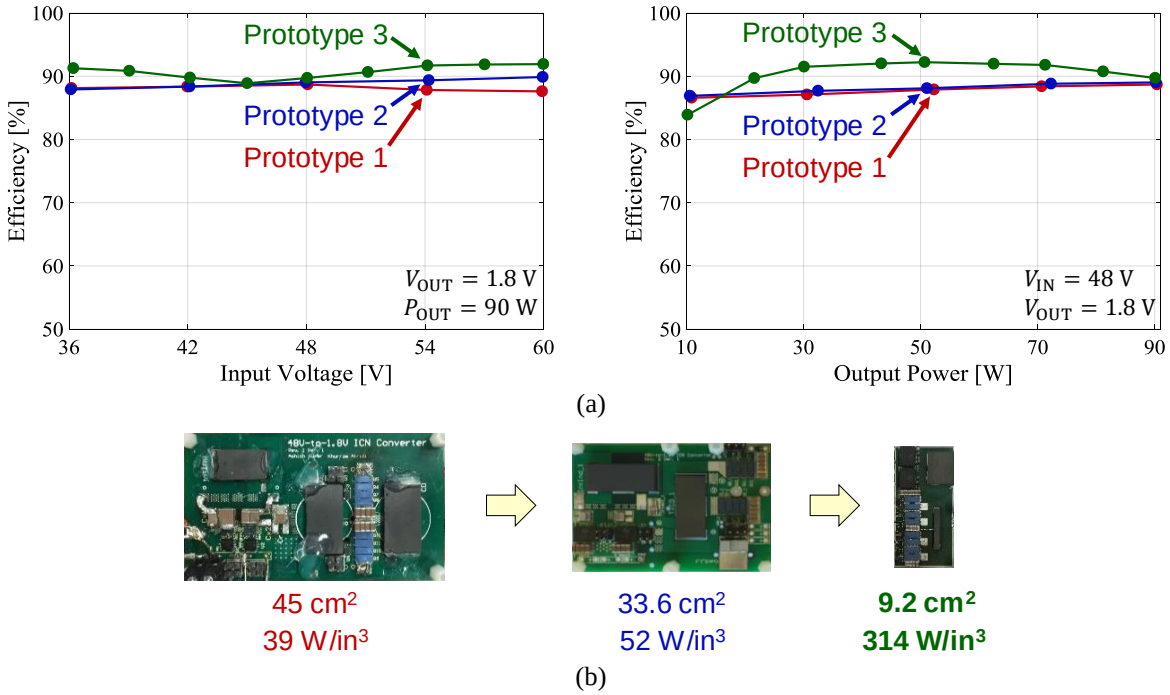
The prototype PoL converter has been tested across its entire input voltage range. All inverter and rectifier transistors achieve soft-switching, as shown in Fig. 7.9 for two corner operating points. To deliver partial power levels, the prototype converter is operated under rectifier phase-shift control, as shown in Fig. 7.10. The efficiency of the prototype converter has also been measured across its full operating range, and shown in Fig. 7.11. This converter prototype achieves greater than 92% peak efficiency. In addition, this converter achieves a power density of 314 W/in^3.

A performance comparison of the converter developed in this chapter with the two converters developed in Chapter 6 is shown in Fig. 7.12. As can be seen, this final PoL ICN converter prototype maintains higher



(a) (b)

Figure 7.11: Measured efficiency of the final PoL ICN converter prototype: (a) as a function of its input voltage at full power (P_{OUT} = 90 W), and (b) as a function of its output power at its nominal input voltage (V_{IN} = 48 V). In both (a) and (b), the output voltage V_{OUT} = 1.8 V.



(a)

(b)

Figure 7.12: Performance comparison of the three PoL ICN converter prototypes developed in this thesis: (a) efficiency comparison, and (b) power density comparison.

efficiencies across most of the operating range, and achieves a substantially higher power density. The performance of this PoL ICN converter is also compared with state-of-the-art (SoA) single-stage isolated 48V-to-1.8V converters, as shown in Fig. 7.13. It can be seen the PoL ICN converter maintains peak efficiencies comparable to the SoA solutions, while achieving a substantially higher power density.

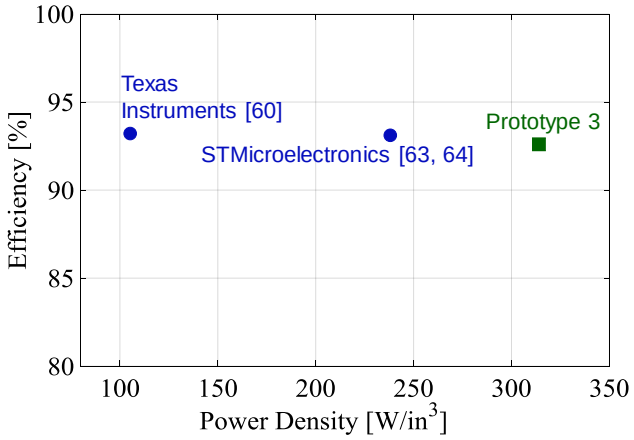


Figure 7.13: Performance comparison of the final PoL ICN converter prototype with state-of-the-art single-stage isolated 48V-to-1.8V point-of-load converters. For the efficiency comparison, the peak efficiency of each converter is considered. For the power density comparison, only the power stage of each converter is considered.

7.3 Chapter Summary and Conclusions

This chapter presents a high-efficiency high-power density single-stage isolated 48V-to-1.8V point-of-load converter for datacenter applications. This converter achieves large step-down while maintaining high efficiency across a wide range of input voltage and output power. The large step-down is achieved by utilizing an immittance network and a distributed transformer. The high efficiency is achieved using the ICN converter architecture, which enables zero-voltage and near-zero-current switching across wide operating ranges. The converter's power density is enhanced by utilizing rectifier phase-shift control to regulate its output voltage, and by implementing its magnetic components as planar PCB-integrated structures. The magnetic components are designed and optimized using 3D finite-element analysis. A prototype 90-W ICN converter utilizing planar magnetics, designed to operate over an input voltage range of 36 V to 60 V and an output voltage of 1.8 V is built and tested. The prototype ICN converter achieves a peak efficiency of 92.6% and a power density of 314 W/in^3.

Chapter 8
Improved Design Optimization for High-Efficiency Matching Networks

Matching networks find application as circuit stages that provide voltage/current gain in large-conversion-ratio resonant converters and wireless power transfer (WPT) systems. The analysis and design of high-efficiency matching networks was explored at a fundamental level in [88], with several important results being reported. It was shown that for a given required gain, using multistage matching networks may be a more efficient solution than a single-stage network. Furthermore, expressions were derived for the optimum number of stages and the maximum efficiency achievable in such a multistage matching network. The design approach presented in [88] is of significant practical interest; however, it constrains the input and load impedances of each stage of a multistage matching network to be purely resistive.

This chapter introduces a new analytical framework for optimization of high-efficiency matching networks. This framework relaxes the resistive constraint on the input and load impedances of the intermediate stages of a multistage matching network and allows them to be complex. Based on this framework, the design of multistage matching networks is optimized using the method of Lagrange multipliers. This design optimization approach predicts the optimum distribution of gains and impedance characteristics among the stages of a multistage matching network. The efficiency of matching networks designed using the proposed approach is compared with the conventional design approach of [88], and it is shown that significant efficiency improvements are possible. These improvements are validated through extensive simulations as well as experiments. An approach to multistage matching network design that also considers relaxing the resistive constraint for efficiency improvement was independently developed at the same time as this work in [134]. However, the optimization approach in [134] is purely numerical. Compared to this approach, the proposed analytical approach provides much richer insights into the design of multistage matching networks.

8.1 MATCHING NETWORKS WITH COMPLEX INPUT AND LOAD IMPEDANCES

Among the basic matching network topologies, L-section matching networks are typically the most efficient for a given gain [88], [135]. Four L-section matching network stages are shown in Fig. 8.1, and multistage matching networks constructed by cascading these stages are shown in Fig. 8.2. Typically, multistage L-section matching networks are designed under a "resistive" design framework, wherein each stage has resistive input and load impedances. This framework was utilized in [88] to optimize the design of multistage matching networks. In this chapter, we propose a new framework for matching network design. This framework relaxes the resistive constraint on the L-section stages of a multistage matching network. Consider a multistage L-section matching network with complex input and load impedances at each stage. To characterize each L-section stage of such a network, we introduce three quantities: G_i, which is the current gain provided by the L-section stage, defined as $G_i = \frac{|\hat{I}_{out}|}{|\hat{I}_{in}|}$, where $|\hat{I}_{out}|$ and $|\hat{I}_{in}|$ are the amplitudes of the output and input currents of the stage, respectively, as shown in Fig. 8.1; Q_{load}, which is a measure of the load impedance characteristic, defined as $Q_{load} = \frac{X_{load}}{R_{load}}$, where X_{load} and R_{load} are the imaginary and real parts of the load impedance, respectively, as shown in Fig. 8.1; and Q_{in},

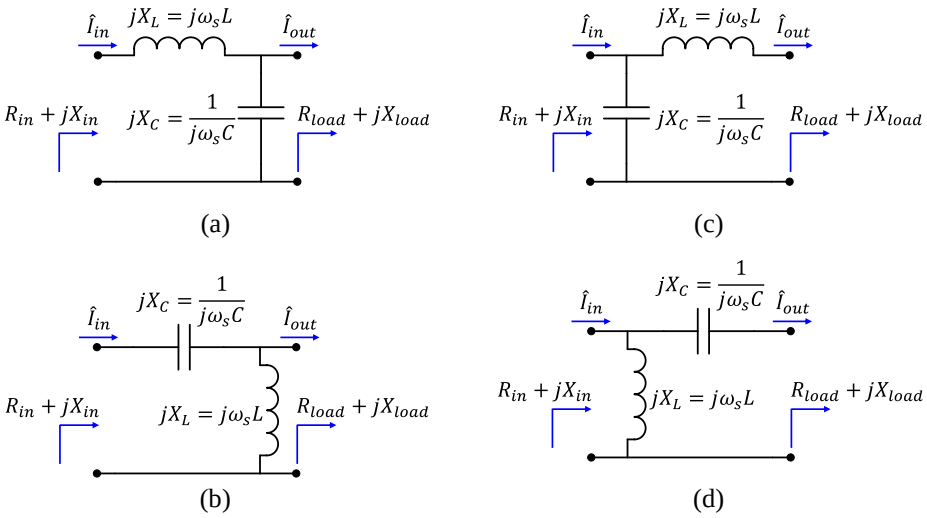


Figure 8.1: Four different types of L-section stages. Under the conventional design approach, the input and load reactances (X_{in} and X_{load}) of all such stages in a multistage matching network are constrained to be zero, while the proposed approach allows X_{in} and X_{load} to have non-zero values.

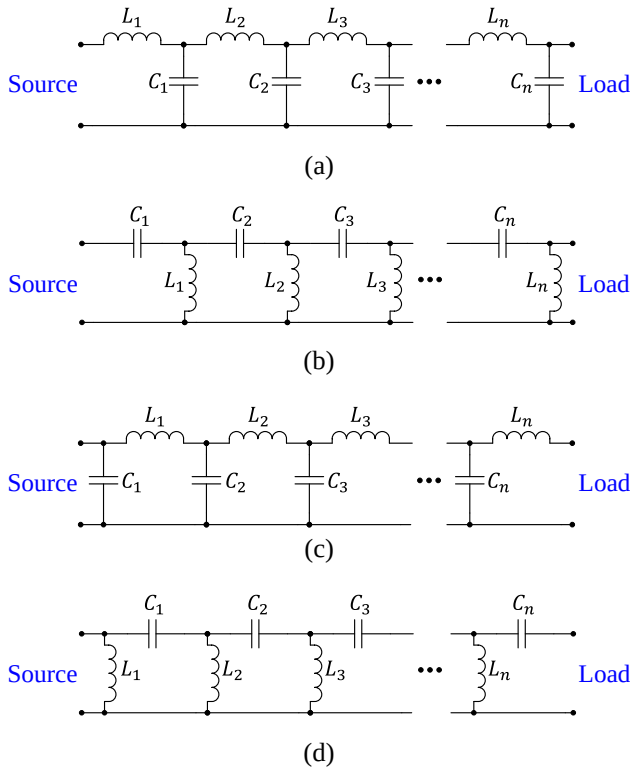


Figure 8.2: Four types of multistage matching networks constructed by cascading the corresponding L-section stages of Fig.1. The multistage networks shown in (a) and (b) are appropriate for stepping-up voltage (that is, for total current gains $G_{i,tot} \leq 1$), while those in (c) and (d) are suitable for stepping-up current ($G_{i,tot} \geq 1$).

which is a measure of the input impedance characteristic, defined as $Q_{in} = \frac{X_{in}}{R_{in}}$, where X_{in} and R_{in} are the imaginary and real parts of the input impedance, respectively, also shown in Fig. 8.1.

Given values of the current gain G_i, the impedance characteristics Q_{load} and Q_{in}, and the load resistance R_{load} for an L-section stage, the inductance and capacitance values of that stage can be determined from closed-form expressions by relating the current gain and input impedance of the stage to the reactances in its series and shunt branches, and the load impedance. For instance, for the L-section stage shown in Fig. 8.1(a), the inductance and capacitance values can be determined from:

$$L = \frac{\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}+G_i^2 Q_{in}\right)R_{load}}{2\pi f_s}, \tag{8.1a}$$

$$C = \frac{1-G_i^2}{2\pi f_s\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}-G_i^2\, Q_{load}\right)R_{load}}. \tag{8.1b}$$

Here f_s is the operating frequency. Similar expressions for the other L-section stages shown in Fig. 8.1

TABLE 8.1
EXPRESSIONS FOR THE INDUCTANCE AND CAPACITANCE OF THE FOUR L-SECTION STAGES OF FIG. 8.1

L-section Stage	Expressions for L and C
Fig. 8.1(a)	$L = \frac{\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}+G_i^2Q_{in}\right)R_{load}}{2\pi f_s}$ $C = \frac{1-G_i^2}{2\pi f_s\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}-G_i^2\,Q_{load}\right)R_{load}}$
Fig. 8.1(b)	$L = \frac{\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}+G_i^2Q_{load}\right)R_{load}}{2\pi f_s(1-G_i^2)}$ $C = \frac{1}{2\pi f_s\left(G_i\sqrt{(1-G_i^2)+Q_{load}^2}-G_i^2\,Q_{in}\right)R_{load}}$
Fig. 8.1(c)	$L = \frac{\left(\sqrt{(G_i^2-1)+G_i^2Q_{in}^2}-Q_{load}\right)R_{load}}{2\pi f_s}$ $C = \frac{1-\frac{1}{G_i^2}}{2\pi f_s\left(\sqrt{(G_i^2-1)+G_i^2Q_{in}^2}+Q_{in}\right)R_{load}}$
Fig. 8.1(d)	$L = \frac{\left(\sqrt{(G_i^2-1)+G_i^2Q_{in}^2}-Q_{in}\right)R_{load}}{2\pi f_s\left(1-\frac{1}{G_i^2}\right)}$ $C = \frac{1}{2\pi f_s\left(\sqrt{(G_i^2-1)+G_i^2Q_{in}^2}+Q_{load}\right)R_{load}}$

are listed in Table 8.1. It should be noted that the framework described above reduces to the conventional resistive framework of [88] when Q_{in} and Q_{load} of each L-section stage of a multistage matching network are set to zero. This new analytical framework enables a substantially larger design space to be explored for the optimization of multistage L-section matching networks.

8.2 PROPOSED MULTISTAGE MATCHING NETWORK DESIGN APPROACH

The analytical framework presented in the previous section is used to develop a new approach for the optimization of multistage matching networks. The primary objective of this approach is to determine the optimal distribution of current gains (G_i's) and impedance characteristics (Q_{in}'s and Q_{load}'s) among the different stages of a multistage matching network in a manner that maximizes its efficiency. The first step in this approach is to express the efficiency of an L-section stage in terms of its current gain and

impedance characteristics. The losses in an L-section stage owe their origin to winding and core losses in the inductor, and conduction and dielectric losses in the capacitor. These losses can be represented at the operating frequency by the unloaded quality factors: $Q_L = \frac{X_L}{R_L}$ for the inductor and $Q_C = \frac{|X_C|}{R_C}$ for the capacitor, where $X_L = 2\pi f_s L$ and $X_C = -\frac{1}{2\pi f_s C}$ are the reactances, and R_L and R_C are the equivalent series resistances of the inductor and the capacitor, respectively. In most cases, losses in the inductor far exceed those in the capacitor, i.e., $Q_C \gg Q_L$. Furthermore, in high-efficiency matching networks, the total losses are low; therefore, capacitor losses can be neglected. In this case, the efficiency of the k-th L-section stage in a multistage matching network can be approximated as:

$$\eta_k \approx 1 - \frac{Q_{eff,k}}{Q_L}. \tag{8.2}$$

Here $Q_{eff,k}$ is an effective transformation factor associated with the k-th L-section stage. Its value depends on the type of the L-section stage, and the stage's current gain and impedance characteristics. Expressions for this transformation factor for the four L-section stages of Fig. 8.1 are listed in Table 8.2. It can be seen from Table 8.2 that the effective transformation factor captures the gain as well as the reactance conversion provided by an L-section stage. In the limiting case when both the input impedance characteristic, Q_{in}, and the load impedance characteristic, Q_{load}, of an L-section stage are zero, the effective transformation factor Q_{eff} quantifies the current gain G_i provided by the stage, and reduces to the quality factor Q of the stage as defined in the conventional design approach of [88]. Derivations of the efficiency expression given in (8.2) for the four L-section stages shown in Fig. 8.1 are provided in Appendix E.

Using (8.2), the efficiency of a multistage matching network with n cascaded L-section stages can be expressed as:

$$\eta_{multistage} \approx \left(1 - \frac{Q_{eff,1}}{Q_L}\right)\left(1 - \frac{Q_{eff,2}}{Q_L}\right) \ldots \left(1 - \frac{Q_{eff,n}}{Q_L}\right), \tag{8.3}$$

TABLE 8.2
EXPRESSIONS FOR THE EFFECTIVE TRANSFORMATION FACTOR Q_{eff} FOR THE FOUR L-SECTION STAGES OF FIG. 8.1

L-section Stage	Expressions for Q_{eff}
Fig. 1(a)	$\frac{1}{G_i}\sqrt{(1-G_i^2)+Q_{load}^2}+Q_{in}$
Fig. 1(b)	$\frac{1}{G_i}\sqrt{(1-G_i^2)+Q_{load}^2}-Q_{load}$
Fig. 1(c)	$G_i\sqrt{\left(1-\frac{1}{G_i^2}\right)+Q_{in}^2}-Q_{load}$
Fig. 1(d)	$G_i\sqrt{\left(1-\frac{1}{G_i^2}\right)+Q_{in}^2}+Q_{in}$

where it is assumed that the inductors of each L-section stage have the same quality factor. Under the high-efficiency assumption (i.e., $Q_{eff,k} \ll Q_L \ \ \forall\, k \in \{1,2,\dots,n\}$), the efficiency of the multistage network is well-approximated by:

$$\eta_{multistage} \approx 1 - \frac{\sum_{k=1}^{n} Q_{eff,k}}{Q_L}. \tag{8.4}$$

The design optimization approach presented here aims to maximize the multistage network efficiency $\eta_{multistage}$ by optimally distributing the gains and impedance characteristics among the L-section stages of the network. It is apparent from the form of (8.4) that maximizing $\eta_{multistage}$ is equivalent to minimizing the sum of the effective transformation factors of the L-section stages, $\sum_{k=1}^{n} Q_{eff,k}$. This minimization problem is constrained by the specification of the total current gain of the multistage matching network, denoted by $G_{i,tot}$. The total current gain is calculated by multiplying the current gains of all the stages of the network. With the source and load positions as indicated in Fig. 8.2, the multistage networks of Figs. 8.2(a) and 8.2(b) are suitable for stepping-up voltage; therefore, the total current gain $G_{i,tot}$ for these networks is constrained to be less than 1. Similarly, the multistage networks of Figs. 8.2(c) and 8.2(d) are suitable for stepping-up current; hence, $G_{i,tot}$ for these networks is constrained to be greater than 1. In this work, two additional design constraints are imposed: the input and load impedances seen at the input and output ports of the overall multistage matching network are purely resistive.

Imposing these resistive constraints is appropriate for many applications, such as when the matching network is loaded by a class-D rectifier (which looks resistive under fundamental frequency approximation [10]), and driven by an inverter requiring near-resistive impedance for zero voltage and near-zero current switching.

With these constraints, the design optimization problem can be formally expressed as:

$$\min \sum_{k=1}^{n} Q_{eff,k} \tag{8.5a}$$

subject to:

$$\prod_{k=1}^{n} G_{i,k} = G_{i,tot},\ Q_{in,1} = 0, \text{ and } Q_{load,n} = 0. \tag{8.5b}$$

Here $G_{i,k}$ is the current gain provided by the k-th L-section stage of the multistage network, $Q_{in,1}$ is the input impedance characteristic of the first stage, and $Q_{load,n}$ is the load impedance characteristic of the last (n-th) stage. To solve this optimization problem, the method of Lagrange multipliers [89], [90] is employed, utilizing the following Lagrangian:

$$\mathcal{L} = \sum_{k=1}^{n} Q_{eff,k} + \lambda_1\left(\prod_{k=1}^{n} G_{i,k} - G_{i,tot}\right) + \lambda_2\, Q_{in,1} + \lambda_3\, Q_{load,n}. \tag{8.6}$$

Here, λ_1, λ_2 and λ_3 are Lagrange multipliers. The first term of the Lagrangian represents the expression to be minimized, while the other terms represent the constraints. The sum of the effective transformation factors of all the L-section stages, $\sum_{k=1}^{n} Q_{eff,k}$, is minimized subject to the given constraints by setting the partial derivatives of the Lagrangian with respect to the gain and impedance characteristics of each L-section stage to zero. Noting that the input impedance characteristic of each stage equals the load impedance characteristic of the previous stage, that is, $Q_{in,k} = Q_{load,k-1}$, the following partial differential equations need to be solved:

$$\begin{aligned} \frac{\partial \mathcal{L}}{\partial G_{i,k}} &= 0, \forall k \in \{1, 2, \dots, n\}, \\ \frac{\partial \mathcal{L}}{\partial Q_{in,k}} &= 0, \forall k \in \{1, 2, \dots, n\}, \end{aligned} \tag{8.7}$$

$$\frac{\partial \mathcal{L}}{\partial \lambda_i} = 0, \forall i \in \{1, 2, 3\}.$$

Solving (8.7) results in the distribution of current gains and impedance characteristics that maximize the efficiency of the multistage matching network. The nature of this optimal distribution depends on the type of multistage matching network and the value of the required total current gain. For the multistage network shown in Fig. 8.2(a), with total current gain $G_{i,tot}$ less than $\frac{1}{\sqrt{2}}$, the optimal current gains G_i of each stage are related as:

$$G_{i,1} = G_{i,2} = \cdots = G_{i,n-1} \stackrel{\text{def}}{=} G_{i,eq}, \tag{8.8a}$$

$$G_{i,n} = \frac{G_{i,tot}}{G_{i,eq}^{n-1}}. \tag{8.8b}$$

It is evident from (8.8a) that in the optimized design, the current gains of the first $n-1$ stages are equal, while the last stage provides the remaining current gain, as given by (8.8b). This is in contrast to all the stages having equal gains when the stages are constrained to have resistive input and output impedances, as in [88]. The optimal equal current gain of the first $n-1$ stages, $G_{i,eq}$ as defined in (8.8a), can be computed from the following equation:

$$\frac{G_{i,eq}^{2\,(n-1)}}{G_{i,tot}\sqrt{G_{i,eq}^{2(n-1)} - G_{i,tot}^2}} = G_{i,eq} + \frac{1}{G_{i,eq}}. \tag{8.9}$$

The optimal impedance characteristics of each stage of the multistage network, Q_{in} and Q_{load}, are related to the optimal current gains as:

$$Q_{in,k} = Q_{load,k-1} = -G_{i,k-1} \forall\, k \in \{2, 3, \ldots, n\}. \tag{8.10}$$

It can be observed from (8.10) that in the optimized design, the input impedance characteristics, Q_{in} (which is the ratio of the imaginary to the real part of the input impedance), of all stages except the first stage are non-zero, since the current gains G_i's must be non-zero. This indicates that higher efficiencies are achievable when the input impedances of the stages of a multistage matching network are allowed to be complex. Equation (8.10) also implies that for the multistage network of Fig. 8.2(a), these input impedances are capacitive (since the current gains G_i's are positive).

Using the design relationships of (8.8) and (8.10), the optimal efficiency of the multistage network of Fig. 8.2(a) can be expressed as:

$$\eta_{multistage,opt} = 1 - \frac{(n-1)\left(\frac{1}{G_{i,eq}} - G_{i,eq}\right) + \frac{1}{G_{i,tot}^2}\left(\frac{G_{i,eq}^{2n-1}}{1+G_{i,eq}^2}\right)}{Q_L}. \tag{8.11}$$

This optimal multistage network efficiency is plotted as a function of the number of stages n for various values of the total current gain, $G_{i,tot} \leq \frac{1}{\sqrt{2}}$, for an inductor quality factor Q_L of 100, in Fig. 8.3. Note that the efficiencies of single-stage designs ($n = 1$) are also shown in Fig. 8.3. The single-stage efficiency can be computed using (8.2) and the expression for the effective transformation factor Q_{eff} of the L-section stage of Fig. 8.1(a) provided in Table II, setting the stage's current gain G_i equal to the total current gain $G_{i,tot}$, and its impedance characteristics, Q_{in} and Q_{load}, both to zero. This results in the following expression for the efficiency of a single-stage network:

$$\eta_{single} = 1 - \frac{\frac{1}{G_{i,tot}}\sqrt{1-G_{i,tot}^2}}{Q_L}. \tag{8.12}$$

It can be seen from Fig. 8.3 that for a given number of stages, the higher the value of the total current gain $G_{i,tot}$, the higher the optimal efficiency. Recalling that the multistage network of Fig. 8.2(a) is designed for stepping-up voltage ($G_{i,tot} \leq 1$), higher values of total current gain correspond to lower voltage step-

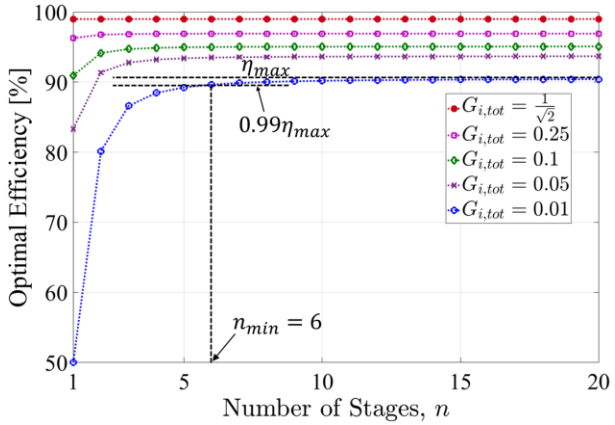


Figure 8.3: Optimal efficiency of the multistage network of Fig. 2(a) as a function of the number of stages for various total current gains $G_{i,tot} \leq \frac{1}{\sqrt{2}}$, as predicted by the proposed design approach. It can be seen that for this range of total current gains, the optimal efficiency increases monotonically with the number of stages, approaching an asymptotic maximum for each value of $G_{i,tot}$.

up ratios. This validates the intuitive conclusion that multistage matching networks providing lower voltage step-up can be designed more efficiently.

It can also be observed from Fig. 8.3 that for each value of total current gain $G_{i,tot}$, the optimal efficiency increases monotonically with the number of stages, indicating that for any required total current gain less than $\frac{1}{\sqrt{2}}$, higher efficiencies can always be obtained by increasing the number of stages. Furthermore, Fig. 8.3 shows that as the number of stages increases, the multistage network efficiency asymptotically converges to a maximum value. It can be shown that this asymptotic maximum efficiency is given by:

$$\eta_{max} = \lim_{n\to\infty} \eta_{multistage,opt} = 1 - \frac{1-\ln\left(2G_{i,tot}^2\right)}{Q_L}. \tag{8.13}$$

This expression, and the corresponding expressions for the other multistage networks of Fig. 8.2, are derived in Appendix F.

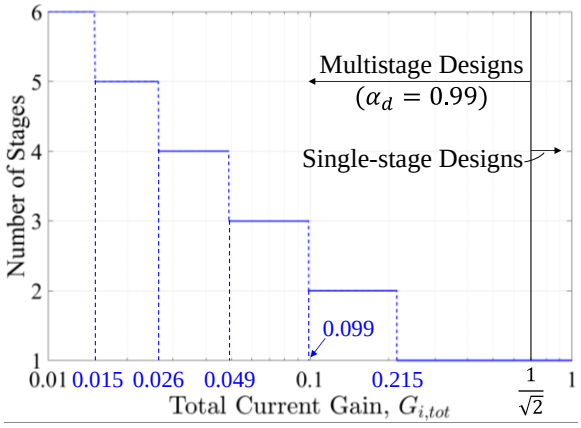
Figure 8.3 reveals another useful insight: for each total current gain less than $\frac{1}{\sqrt{2}}$, although a greater number of stages results in higher optimal efficiencies, the efficiency improvement diminishes with each additional stage. Therefore, for a given total current gain, adding stages to the multistage network is substantially beneficial only up to a certain number of stages. Furthermore, implementing a multistage network with a very high number of stages may introduce additional power losses due to interconnects, and undesirably increase the overall size of the system. To achieve a sufficiently favorable engineering tradeoff in this scenario, a minimum number of stages n_{min} can be defined, for which the efficiency is higher than a pre-defined fraction of the asymptotic maximum efficiency value given by (8.13). This can be mathematically expressed as:

$$n_{min} = \min\{n\} \text{ s.t. } \eta_{multistage,opt} \mid_{n=n_{min}} \geq \alpha_d \eta_{max}. \tag{8.14}$$

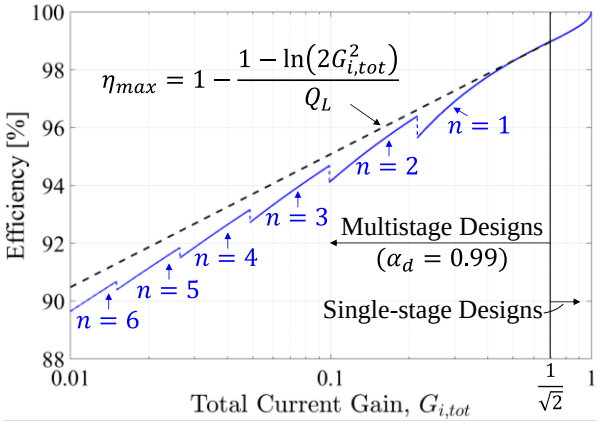
Here, α_d (< 1) is a design choice that quantifies how close the multistage network efficiency is to its asymptotic maximum value η_{max}. The value of α_d is the circuit designer's prerogative and may be decided based on the required total current gain. An example is provided for $G_{i,tot} = 0.01$ (corresponding

to a voltage step-up ratio, $1/G_{i,tot}$, of 100) in Fig. 8.3. Assuming an inductor quality factor of 100, the asymptotic maximum efficiency for $G_{i,tot} = 0.01$ is about 90.5%. As can be seen from Fig. 8.3, if α_d is chosen to be 0.99 (that is, the design objective is to achieve efficiencies within 1% of the asymptotic maximum), then the minimum number of stages required is 6. Marginally higher efficiency can be achieved by choosing a higher value of α_d, at the cost of using more stages.

Figure 8.4(a) shows the minimum number of stages n_{min} required for the same design choice, $\alpha_d = 0.99$, as a function of the total current gain $G_{i,tot}$, for an inductor quality factor Q_L of 100. The corresponding multistage network efficiency is shown in Fig. 8.4(b), along with the asymptotic maximum



(a)



(b)

Figure 8.4: (a) Minimum number of stages in the multistage network of Fig. 2(a) that achieves >99% of the asymptotic maximum efficiency given by (13) for each value of $G_{i,tot} \leq \frac{1}{\sqrt{2}}$, and (b) the efficiencies achieved with this design choice, with an inductor quality factor of 100. The asymptotic maximum efficiency is shown as the dashed curve in (b). (a) and (b) also show that for $G_{i,tot} \geq \frac{1}{\sqrt{2}}$, single-stage designs are the optimal choice.

efficiency for reference. It can be seen from Fig. 8.4 that as the total current gain $G_{i,tot}$ increases (that is, the required voltage step-up decreases), a progressively smaller number of stages can achieve efficiencies within 1% of the maximum efficiency.

Figure 8.4 also presents the results for total current gains $G_{i,tot}$ greater than $\frac{1}{\sqrt{2}}$. For this range of total current gain, the optimal current gains of each stage of the multistage network of Fig. 8.2(a), determined by solving (8.7), are related as:

$$G_{i,1} = G_{i,2} = \cdots = G_{i,n-1} = 1, \tag{8.15a}$$

$$G_{i,n} = G_{i,tot}. \tag{8.15b}$$

It can be seen from (8.15a) that for total current gains greater than $\frac{1}{\sqrt{2}}$, the first $n-1$ stages of a multistage network each provide current gains of 1. Consider the multistage network of Fig. 8.2(a). If an L-section stage in this network provides a current gain of 1, then for an efficiency-optimized network it translates to that stage having zero inductance and zero capacitance, as shown in Appendix G. Therefore, in the optimized design, the first $n-1$ stages are eliminated, and the multistage network is reduced to a single-stage network that provides the total current gain $G_{i,tot}$, as given by (8.15b). The results in (8.15) hold irrespective of the number of stages. Therefore, when the network of Fig. 8.2(a) is designed to provide total current gains greater than $\frac{1}{\sqrt{2}}$ (or, voltage step-up ratios less than $\sqrt{2}$), a single-stage design has the highest efficiency. The efficiency of a single-stage design is given by (8.12), and is also shown in Fig. 8.4(b). It is evident from Fig. 8.4(b) that the single-stage efficiency is a monotonically increasing function of the total current gain $G_{i,tot}$, indicating again that for lower voltage step-up ratios, higher optimal efficiencies are achievable.

For multistage designs, the optimal inductance and capacitance values for the L-section stages can be determined using (8.1) and (8.8)-(8.10). First, (8.9) can be solved either analytically or numerically (depending on the number of stages n) to obtain the optimal equal current gains of the first $n-1$ stages, $G_{i,eq}$. Then, (8.8b) can be used to obtain the current gain of the last stage, $G_{i,n}$. Following this, the

TABLE 8.3
DESIGN OPTIMIZATION RESULTS FOR THE MULTISTAGE MATCHING NETWORKS OF FIG. 8.2

Multistage L-section Network	Range of Total Current Gain $G_{i,tot}$	Optimal Design Relationships	Summary of Optimization Results
Fig. 2(a) and 2(b) ($G_{i,tot} \leq 1$)	$0 < G_{i,tot} \leq \frac{1}{\sqrt{2}}$	$G_{i,1} = G_{i,2} = \cdots = G_{i,n-1} \stackrel{\text{def}}{=} G_{i,eq}$, $G_{i,n} = \frac{G_{i,tot}}{G_{i,eq}^{n-1}}$, $\frac{G_{i,eq}^{2\,(n-1)}}{G_{i,tot}\sqrt{G_{i,eq}^{2(n-1)} - G_{i,tot}^2}} = G_{i,eq} + \frac{1}{G_{i,eq}}$. Fig. 2(a): $Q_{in,k} = -G_{i,k-1} \forall\, k \in \{2,3,\ldots,n\}$, Fig. 2(b): $Q_{in,k} = G_{i,k-1} \forall\, k \in \{2,3,\ldots,n\}$,	• Current gains of first $n-1$ stages are equal. • Fig. 2(a): All stages except first have complex (capacitive) input impedances. • Fig. 2(b): All stages except first have complex (inductive) input impedances. • Optimal efficiency increases with number of stages, asymptotically converging, as $n \to \infty$, to: $\eta_{max} = 1 - \frac{1 - \ln(2G_{i,tot}^2)}{Q_L}$.
	$\frac{1}{\sqrt{2}} \leq G_{i,tot} \leq 1$	$G_{i,1} = G_{i,2} = \cdots = G_{i,n-1} = 1$, $G_{i,n} = G_{i,tot}$.	Single-stage designs have highest efficiency, given by: $\eta_{single} = 1 - \frac{\frac{1}{G_{i,tot}}\sqrt{1 - G_{i,tot}^2}}{Q_L}$.
Fig. 2(c) and 2(d) ($G_{i,tot} \geq 1$)	$1 \leq G_{i,tot} \leq \sqrt{2}$	$G_{i,2} = G_{i,3} = \cdots = G_{i,n} = 1$, $G_{i,1} = G_{i,tot}$.	Single-stage designs have highest efficiency, given by: $\eta_{single} = 1 - \frac{G_{i,tot}\sqrt{1 - \frac{1}{G_{i,tot}^2}}}{Q_L}$.
	$G_{i,tot} \geq \sqrt{2}$	$G_{i,2} = G_{i,3} = \cdots = G_{i,n} \stackrel{\text{def}}{=} G_{i,eq}$, $G_{i,1} = \frac{G_{i,tot}}{G_{i,eq}^{n-1}}$, $\frac{G_{i,tot}^2}{G_{i,eq}^{(n-1)}\sqrt{G_{i,tot}^2 - G_{i,eq}^{2(n-1)}}} = G_{i,eq} + \frac{1}{G_{i,eq}}$. Fig. 2(c): $Q_{in,k} = \frac{1}{G_{i,k}} \forall\, k \in \{2,3,\ldots,n\}$, Fig. 2(d): $Q_{in,k} = -\frac{1}{G_{i,k}} \forall\, k \in \{2,3,\ldots,n\}$,	• Current gains of all but first stage are equal. • Fig. 2(c): All stages except first have complex (inductive) input impedances. • Fig. 2(d): All stages except first have complex (capacitive) input impedances. • Optimal efficiency increases with number of stages, asymptotically converging, as $n \to \infty$, to: $\eta_{max} = 1 - \frac{1 + \ln\left(\frac{G_{i,tot}^2}{2}\right)}{Q_L}$.

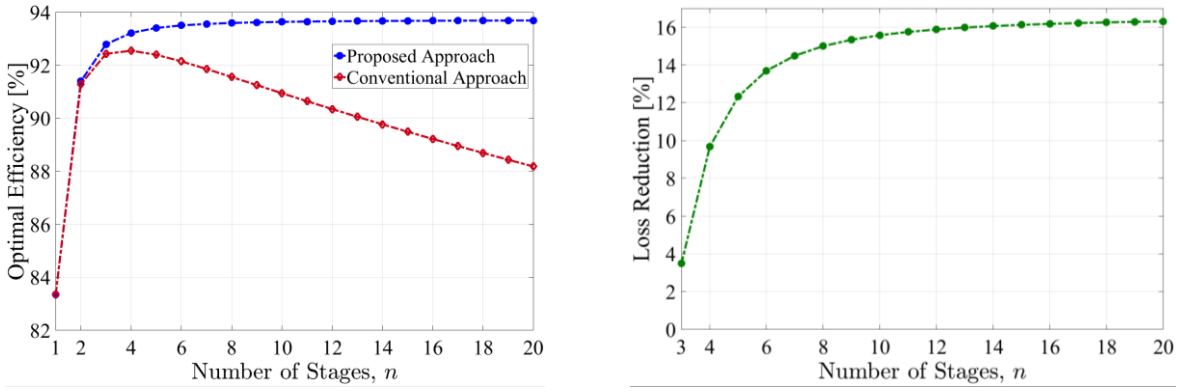
impedance characteristics (Q_{in} and Q_{load}) of each stage can be computed using (8.10). Finally, given these current gains and impedance characteristics, the optimal inductance and capacitance values for each stage can be obtained using (8.1a) and (8.1b). For single-stage designs, the inductance and capacitance values can be obtained directly using the expressions in Table 8.1, with $G_i = G_{i,tot}$, $Q_{in} = 0$ and $Q_{load} = 0$.

Relationships similar to (8.8)-(8.15) can be obtained for the other three multistage matching networks shown in Fig. 8.2, enabling similar insights to be drawn. These relationships are summarized for the four different types of multistage networks in Table 8.3. The optimal inductance and capacitance values for the

networks of Fig. 8.2(b), (c) and (d) can be obtained in a manner similar to that described for the network of Fig. 8.2(a) above, using the corresponding design relationships given in Table 8.3, and the inductance and capacitance expressions provided in Table 8.1. The above presented optimization approach results in new designs of multistage matching networks, ones that will be shown to compare favorably with conventional designs.

8.3 Comparison between Proposed and Conventional Approaches

To determine the advantages of the proposed optimization approach, its results are compared with those of the conventional approach given in [88]. The conventional approach optimally designs multistage matching networks under the constraint that each stage has resistive input and load impedances. The proposed approach relaxes this constraint, resulting in substantially different designs. For instance, under the conventional approach, for any total gain requirement, there is an optimal number of stages for which the multistage network efficiency is maximized. In comparison, as discussed earlier, the proposed design approach predicts that for a broad range of total gain requirement, utilizing a higher number of stages always results in higher efficiencies. For this range of gains, the efficiencies achievable using the proposed approach are consistently higher than those under the conventional approach. This is exemplified for the matching network of Fig. 8.2(a) in Fig. 8.5, for a total current gain of 0.05 (equivalently, a voltage step-up ratio of 20) and an inductor quality factor of 100. Figure 8.5(a) plots the optimal efficiencies predicted by the conventional and the proposed approach as a function of the number of stages. For this total current gain, the conventional approach predicts that using 4 stages is the optimal choice, resulting in an efficiency of 92.5%. In comparison, a 4-stage network designed using the proposed approach is predicted to achieve an efficiency of 93.2%, corresponding to a reduction in losses of nearly 10%. The loss reduction increases if a higher number of stages is used. Figure 8.5(b) shows the loss reduction achievable using the proposed approach over the optimal 4-stage design of the conventional approach, for the same total current gain of 0.05. As can be seen, losses are reduced by greater than 14% if 6 or more stages are utilized. Also notable in Fig. 8.5(b) is that for this total current gain, a 3-stage



(a) (b)

Figure 8.5: Comparison of the proposed and the conventional design approach for the multistage matching network of Fig. 2(a) for a total current gain $G_{i,tot}$ of 0.05, with an inductor quality factor Q_L of 100: (a) Optimal efficiency as predicted by the proposed and the conventional approach as a function of the number of stages, and (b) Loss reduction achievable with the proposed approach as compared to the optimal 4-stage design of the conventional approach.

network designed using the proposed approach is more efficient than the optimal 4-stage design of the conventional approach. Similar performance enhancements are achievable for all the other multistage network types shown in Fig. 8.2.

Substantial improvements are also achieved using the proposed approach for other values of total current gain than the one discussed above, including the range of total current gains for which the conventional approach predicts a single-stage design to be the most efficient. For example, for the network of Fig. 8.2(a), the conventional design approach predicts that single-stage networks are optimal for total current gains greater than 0.33, and up to 1. In comparison, under the proposed approach, single-stage designs are optimal for a much narrower range of total current gain: from $\frac{1}{\sqrt{2}}$ (= 0.707) to 1. Therefore, for total current gains between 0.33 and $\frac{1}{\sqrt{2}}$, while the conventional approach recommends using a single-stage design, the proposed approach suggests that higher efficiencies are achievable if more stages are used. This advantage over the conventional design approach is also maintained for all the other multistage matching networks of Fig. 8.2.

The efficiencies predicted by the conventional and proposed approaches are also compared for a fixed number of stages. A two-stage matching network of the type shown in Fig. 8.2(a) is designed using both

the proposed and the conventional approach. The predicted efficiencies for this two-stage matching network designed using the two approaches are shown as a function of the total current gain, and for three different values of inductor quality factors, in Fig. 8.6(a). It can be seen that designs resulting from the proposed approach have higher efficiency than the conventional approach. Figure 8.6(b) shows the percentage loss reduction due to the proposed approach relative to the conventional approach. The percentage reduction in loss increases with total current gain, but is independent of the inductor quality factor. For a two-stage network, loss reductions in excess of 20% are achievable using the proposed approach. A similar comparison for a three-stage matching network of the type in Fig. 8.2(a) is shown in Figs. 8.6(c) and 8.6(d). For this network, loss reductions approaching 35% are achievable. The operation

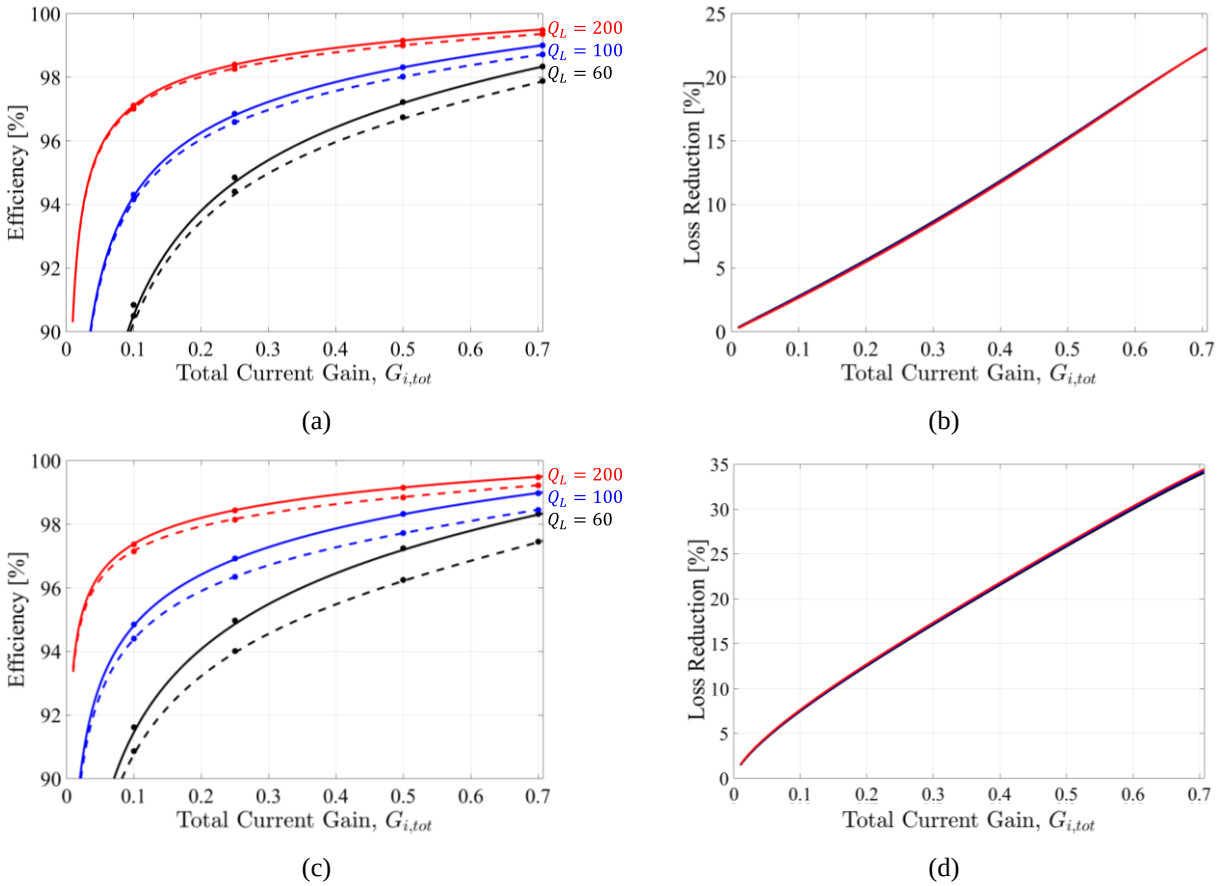


Figure 8.6: Comparison of the proposed and conventional design approaches for two-stage and three-stage matching networks of the type shown in Fig. 2(a): (a) Optimized two-stage efficiency over a range of overall current gains, as predicted by proposed approach (solid lines) and by the conventional approach (dashed lines). Solid markers on the curves indicate LTSpice-simulated efficiencies. (b) Percentage loss reduction achievable using proposed approach. (c) and (d): Optimized efficiency and percentage loss reduction for a three-stage network.

and predicted efficiencies of the two-stage and three-stage designs using the proposed and conventional approaches are validated in LTSpice. The LTSpice predicted efficiencies are superimposed as solid circular markers in Figs. 8.6(a) and 8.6(c).

8.4 EXPERIMENTAL VALIDATION

To validate the analytical and simulated results, an experimental comparison is performed between the proposed and conventional design approaches. Two three-stage matching networks of the type shown in Fig. 8.2(a) are designed: one based on the conventional approach of [88], and the other using the optimization approach presented in this chapter. Both networks are designed for an operating frequency of 1 MHz, output power of 100 W, and total current gain $G_{i,tot}$ of 0.4. Single-layer solenoidal air-core inductors of quality factor $Q_L \approx 35$ and low-ESR NP0 ceramic capacitors are utilized to realize the matching network inductances and capacitances. The inductance and capacitance values for the two networks are listed in Table 8.4. The matching networks are driven by a full-bridge inverter with a 75 V dc input voltage, as shown in Fig. 8.7. The inverter is realized using GaN Systems GS66504B 650-V, 15-A enhancement-mode GaN transistors. The matching networks are loaded by a 250 Ω RF resistor. A photograph of the prototype test circuit is shown in Fig. 8.8.

The measured inverter output voltage, and the matching network input current and output voltage for

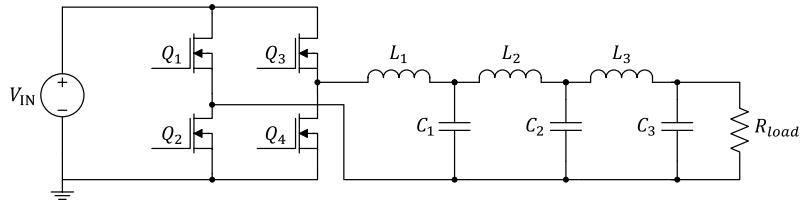


Figure 8.7: Prototype circuit to test matching network efficiency. A full-bridge inverter converts a dc voltage into high-frequency ac, which is fed into a three-stage L-section matching network loaded by a 250 Ω resistance.

TABLE 8.4
INDUCTANCE AND CAPACITANCE VALUES FOR THE THREE-STAGE MATCHING NETWORKS DESIGNED USING THE PROPOSED AND THE CONVENTIONAL APPROACH

Design Approach	L_1	L_2	L_3	C_1	C_2	C_3
Proposed	7.96 µH	4.49 µH	6.98 µH	0.71 nF	0.45 nF	0.8 nF
Conventional	5.83 µH	10.76 µH	19.82 µH	2 nF	1.07 nF	0.58 nF

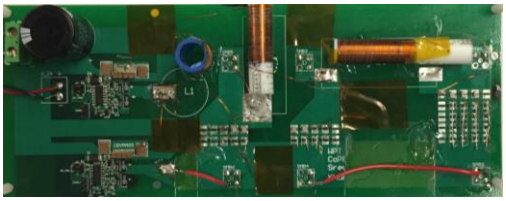
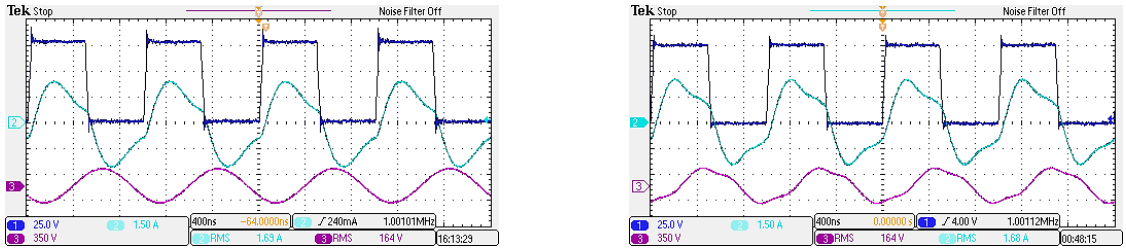


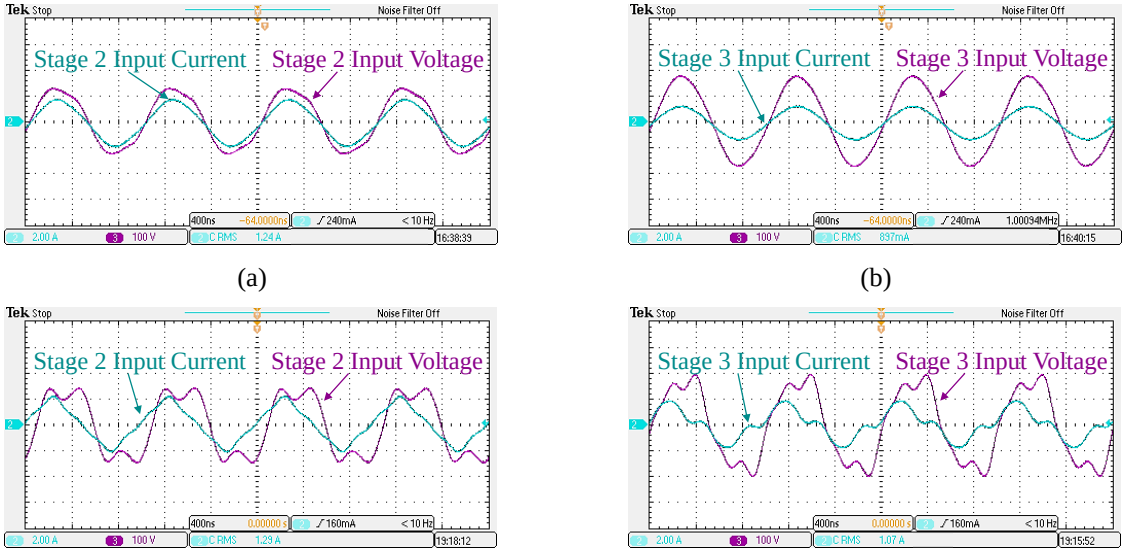
Figure 8.8: Photograph of the prototype test circuit comprising a full-bridge inverter, a three-stage L-section matching network, and a 250 Ω RF load resistor.

the conventional and proposed designs, operating at an output power of 100 W, are shown in Figs. 8.9(a) and 8.9(b), respectively. As can be seen, both the matching networks appear near-resistive to the inverter.



(a) (b)

Figure 8.9: The inverter output voltage, matching network input current (top waveforms, in blue) and load voltage (bottom waveforms, in pink) for the two matching network designs operating at an output power of 100 W: (a) conventional approach and (b) proposed approach.



(a) (b)

(c) (d)

Figure 8.10: The voltage and currents at the inputs of the second and third stages of the two matching network designs: (a) and (b) show these waveforms for the conventionally-designed network, and (c) and (d) for the network designed using the proposed approach. It can be seen that the voltage and currents are in phase in the conventional design, indicating that the second and third stages have resistive input impedances. In contrast, the currents lead the voltages in the proposed design, validating that the input impedances of the second and third stages are capacitive.

The voltages and currents at the inputs of the second and third stages of the two networks are shown in Fig. 8.10. It can be seen from Figs. 8.10(a) and 8.10(b) that the input voltages and currents of the second and third stages are in phase, in accordance with the resistive constraint imposed in the conventional approach. This is illustrated graphically using a Smith chart in Fig. 8.11(a). In comparison, Figs. 8.10(c) and 8.10(d) show that in the network designed using the proposed approach, the second- and third-stage input voltages and currents are not in phase. The currents lead the voltages, indicating that the input impedances of the second and third stages are capacitive, as predicted by the optimization results for the matching network of Fig. 8.2(a) in Section 8.2, and illustrated in the Smith chart of Fig. 8.11(b).

The input and output powers of the matching networks are also measured to determine their efficiency and the difference in their losses. The network designed using the proposed approach has an efficiency of 93.9%, which matches well with the analytically predicted efficiency of 94.1% for $G_{i,tot} = 0.4$ and Q_L = 35. The conventionally-designed network has an efficiency of 92.1%, which is also a good match with its analytical prediction of 92.5%. Based on these measurements, the matching network designed using the proposed approach has 24.8% lower losses than the matching network designed using the conventional approach. This correlates well with the 22.5% predicted reduction in losses.

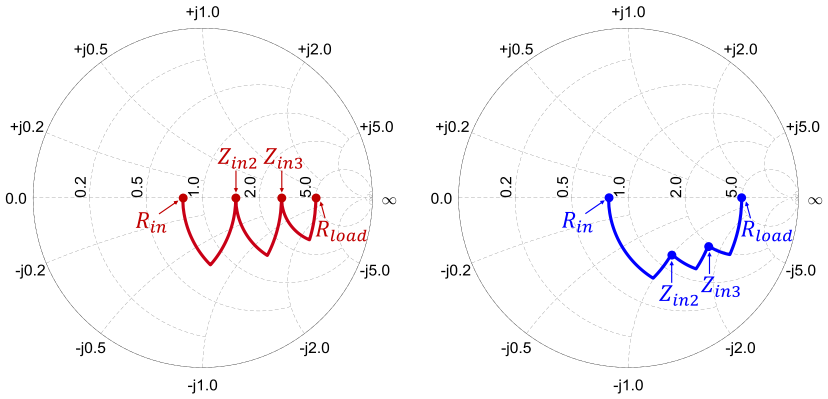


Figure 8.11: Smith charts illustrating the impedance transformation provided by the two three-stage networks designed using: (a) conventional approach and (b) proposed approach. R_{load} denotes the load impedance of the last stage, Z_{in3} and Z_{in2} denote the input impedances of the third and second stages, respectively, and R_{in} denotes the input impedance of the first stage. All impedances are normalized with respect to 50 Ω.

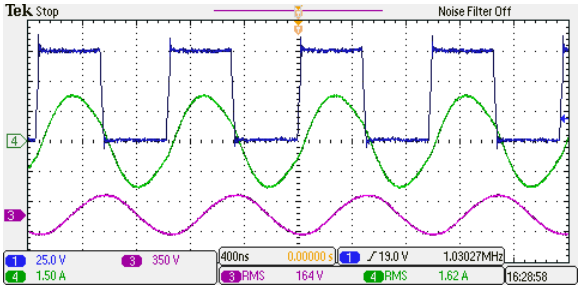


Figure 8.12: The inverter output voltage, matching network input current (top waveforms, in blue and green) and load voltage (bottom waveform, in pink) for a single-stage matching network providing a total current gain $G_{i,tot}$ of 0.4, and operating at an output power of 100 W.

It may be noted that for a total current gain $G_{i,tot}$ of 0.4, a single-stage network is optimal under the conventional design approach. To further demonstrate the advantages of the proposed design approach, a single-stage L-section network providing a total current gain of 0.4 is built and compared with the three-stage network designed using the proposed approach. This network has an inductance of 14.59 μH, which is realized using a solenoidal air-core inductor with a quality factor $Q_L \approx 35$, and a capacitance of 1.46 nF, which is implemented using an NP0 ceramic capacitor. The network is driven by the same 1-MHz full-bridge inverter and loaded by the same 250 Ω RF resistor as the three-stage network. The operating waveforms of the single-stage system at an output power of 100 W are shown in Fig. 8.12. The single-stage network has a measured efficiency of 93.1%, which corresponds well with its analytically predicted efficiency of 93.4%. This validates the predictions of both the conventional and proposed design approaches: the single-stage network is more efficient than the conventional three-stage network (92.1%), but less efficient than the proposed three-stage network (93.9%). The proposed three-stage network has 11.6% lower losses than the single-stage network.

8.5 Chapter Summary and Conclusions

This chapter introduces an improved design optimization approach for multistage matching networks comprising L-section stages. This approach differs from the conventional approach in which each stage of a multistage matching network is designed to have a purely resistive input impedance and assumed to be loaded by a purely resistive load. The proposed design optimization approach explores the possibility of

improvement in efficiency of the network by allowing the L-section stages to have complex input and load impedances. A new analytical framework is developed to determine the effective transformation ratio and efficiency of each stage for which input and load impedances can be complex. The method of Lagrange multipliers is used to determine the gain and impedance characteristics of each stage in the matching network that maximize overall efficiency. Compared with the conventional design approach for matching networks, the proposed approach achieves higher efficiency, resulting in loss reduction of up to 35% for a three-stage L-section matching network. The theoretical predictions are validated experimentally using a three-stage matching network designed for 1 MHz and 100 W operation.

Chapter 9
A High-Frequency Inverter Architecture for Providing Variable Compensation in Wireless Power Transfer Systems

This chapter introduces a new high-frequency inverter architecture, termed the variable compensation inverter (VCI), which can compensate for coupling variations in WPT systems while operating at a fixed frequency and maintaining high efficiency. This architecture incorporates two or more phase-shifted inverters fed by controllable input voltages, and a lossless resonant network, all on the transmitting side of the WPT system. By appropriately controlling the input voltages of the inverters, the VCI can also maintain a fixed output power level during coupling variations. A prototype VCI is designed, built and tested with a 1.5-MHz 65-W capacitive WPT system, and it is shown that the VCI can compensate for up to 50% lateral misalignments in the capacitive coupler, while maintaining the system output power at a fixed level of 65 W and achieving 82% efficiency.

9.1 Proposed Variable Compensation Inverter

The architecture of the proposed VCI is shown in Fig. 9.1. At the front end of the VCI is a power splitting circuit that is fed by a dc voltage (V_{IN} in Fig. 9.1). This power splitting circuit generates multiple controllable

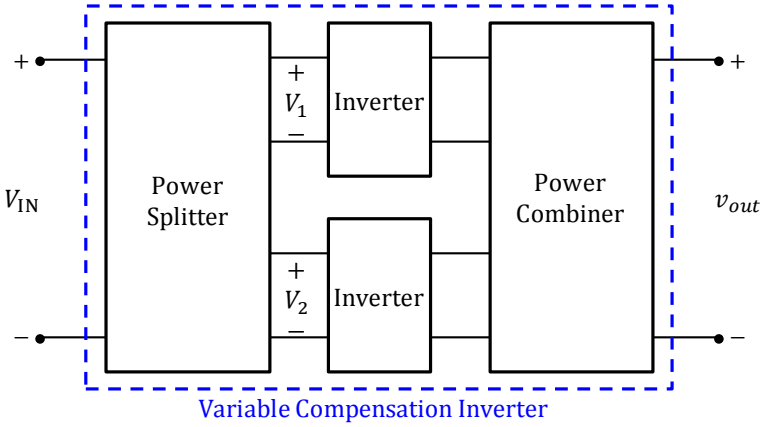


Figure 9.1: Architecture of the proposed variable compensation inverter (VCI).

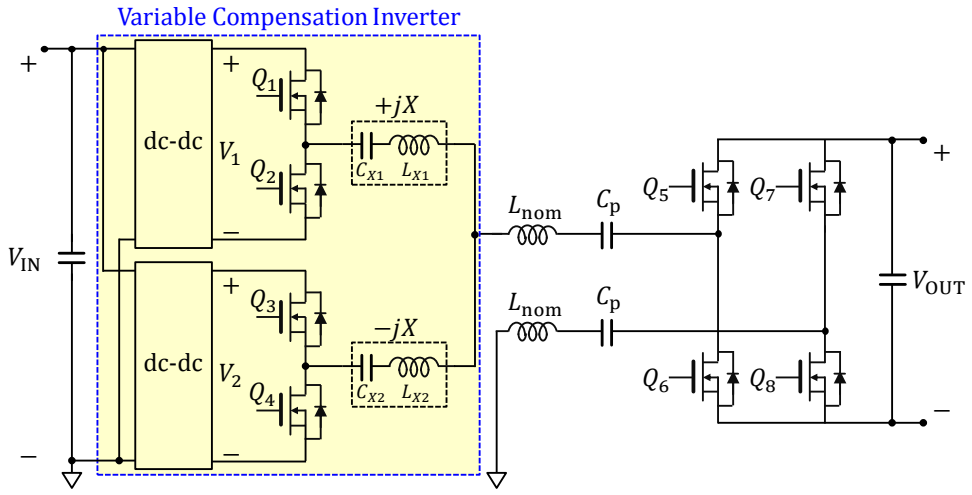


Figure 9.2: Example implementation of the variable compensation inverter (VCI) in a capacitive WPT system.

dc voltages (V_1 and V_2 in Fig. 9.1), which are supplied to high-frequency inverters. The outputs of the inverters feed a power combining circuit, which interfaces the VCI with the remainder of the WPT system. An example implementation of the VCI architecture in a capacitive WPT system is shown in Fig. 9.2. This system operates at a fixed frequency, and the inductors L_{nom} compensate for the reactance of the capacitive coupler (labeled as C_{p} in Fig. 9.2) under the nominal operating conditions; for example, when the transmitting and receiving sides of the coupler are perfectly aligned. The VCI shown in Fig. 9.2 comprises two dc-dc converters (which form the power splitting circuit) feeding two half-bridge inverters. The output power of the two bridge inverters is then combined using a lossless resonant network comprising two branches having equal but opposite reactances ($+X$ and $-X$). This implementation of the VCI builds upon the concepts of the ICN; however, through its use of the dc-dc converters, the VCI differs both topologically and functionally from an ICN. When the coupling reactance X_{C} $\left(= -\frac{1}{\omega_{\mathrm{s}} C_{\mathrm{p}}}\right)$ is at its nominal value, the two dc-dc converters operate in pass-through mode, and the input voltages of the two bridge inverters (V_1 and V_2 in Fig. 9.2), both equal the dc input voltage V_{IN}. The phase-shift between the two inverters under this nominal operating condition is given by:

$$2\Delta = \cos^{-1}\sqrt{1 - \frac{X^2}{\left(\frac{K_{\mathrm{rec}}^2 V_{\mathrm{OUT}}^4}{P_{\mathrm{OUT}}^2}\right)}}. \tag{9.1}$$

Here, V_{OUT} and P_{OUT} are the dc output voltage and rated output power of the WPT system, respectively, and K_{rec} is a constant associated with the topology of the rectifier ($K_{\mathrm{rec}} = \frac{8}{\pi^2}$ for the full-bridge rectifier shown in Fig. 9.2). When the coupling reactance X_{C} changes from its nominal value by an amount δX_{C}, the phase-shift between the two bridge inverters of the VCI is modified to:

$$2\Delta = \cos^{-1}\sqrt{1 - \frac{X^2}{\left(\frac{K_{\mathrm{rec}}^2 V_{\mathrm{OUT}}^4}{P_{\mathrm{OUT}}^2} + \delta X_{\mathrm{C}}^2\right)}}, \tag{9.2}$$

and the input voltages of the bridge inverters, V_1 and V_2, are simultaneously controlled using the dc-dc converters to satisfy the ratio:

$$\frac{V_2}{V_1} = \frac{X - \delta X_{\mathrm{C}}}{\frac{K_{\mathrm{rec}} V_{\mathrm{OUT}}^2}{P_{\mathrm{OUT}}}\sin 2\Delta - \delta X_{\mathrm{C}} \cos 2\Delta}. \tag{9.3}$$

With the inverter phase-shift and input voltage ratio controlled according to (9.2) and (9.3), the impedances seen at the outputs of the two bridge inverters are purely resistive, as illustrated for a wide range of coupling variation in an example WPT application in Fig. 9.3(a)-(c). Therefore, the bridge inverters process purely real power, and the VCI fully compensates for coupling variations. Furthermore, the purely resistive impedances enable ZCS of the inverter transistors. By operating at a frequency slightly higher than the designed frequency, the inverter impedances become slightly inductive, facilitating ZVS and near-ZCS. This enables the VCI to fully compensate for coupling variations while maintaining soft-switching.

The VCI of Fig. 9.2 is also capable of maintaining a fixed output power level during coupling variations. This can be achieved by imposing an additional constraint on the input voltages of the two bridge rectifiers, given by:

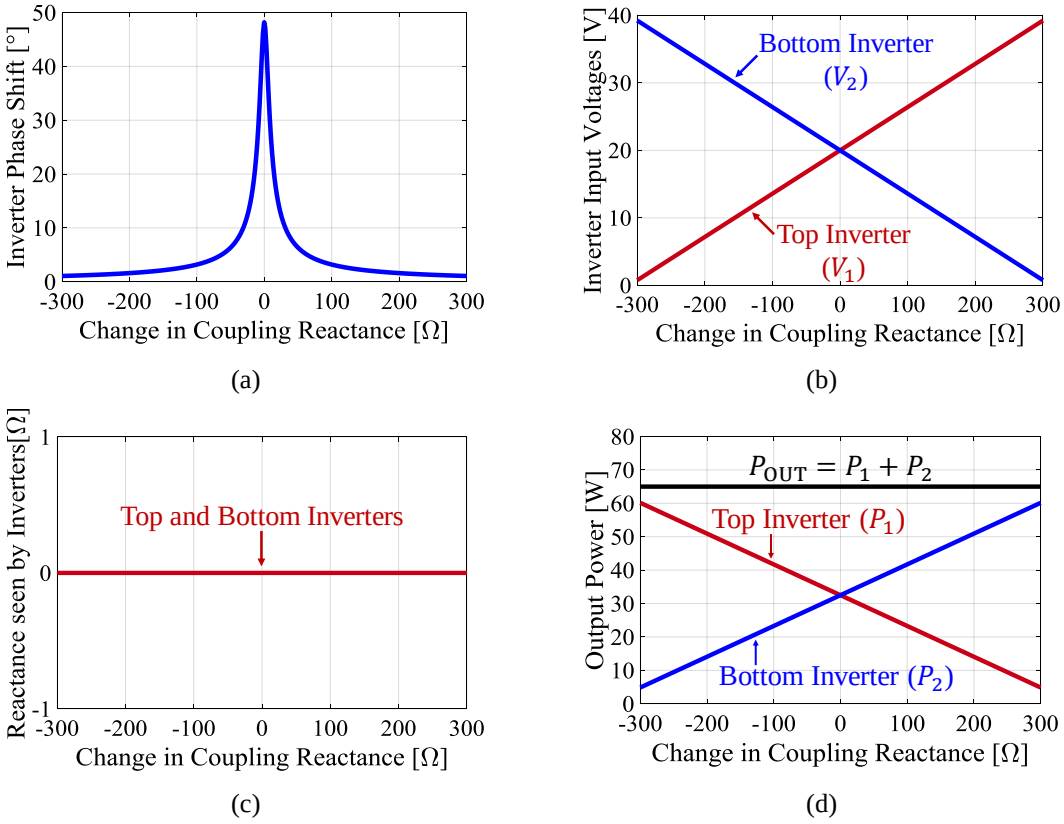


Figure 9.3: Variation in operating parameters of the proposed variable compensation inverter (VCI) as the coupling reactance changes: (a) inverter relative phase-shift, (b) input voltages of top and bottom inverters, (c) resultant reactance seen at the outputs of the two inverters, and (d) output power of the two inverters and the total output power.

$$V_1^2 + V_2^2 - 2V_1V_2\cos 2\Delta = \frac{2X^2P_{\text{OUT}}^2}{K_{\text{inv}}^2K_{\text{rec}}V_{\text{OUT}}^2}. \tag{9.4}$$

Here, K_{inv} is a voltage gain associated with the two bridge inverters, and equals $\frac{2}{\pi}$ for the half-bridge inverters of the VCI of Fig. 9.2. The output power processed by the two bridge inverters of the VCI, and the total output power of the WPT system with the inverter input voltages and phase-shift controlled according to (9.2)-(9.4), are shown as a function of the change in coupling reactance δX_{C} in Fig. 9.3(d). As can be seen, as the coupling reactance varies over a wide range, the power processed by the one of the inverters decreases, while that processed by the other inverter increases, in a manner that the total output power remains constant. This specific power combining mechanism of the VCI enables it to maintain a fixed output power level even under coupling variations.

9.2 Design Methodology

The value of the differential reactance X in the VCI of Fig. 9.2 is selected to ensure that the WPT system delivers the required output power P_{OUT} under nominal operating conditions. This can be ensured by choosing the differential reactance to be:

$$X = \frac{K_{\mathrm{inv}} V_{\mathrm{IN}}}{P_{\mathrm{OUT}}} \sqrt{2K_{\mathrm{rec}} V_{\mathrm{OUT}}^2 - K_{\mathrm{inv}}^2 V_{\mathrm{IN}}^2}\,. \tag{9.5}$$

Various combinations of the inductances and capacitances of the two inverter tanks ($L_{\mathrm{X1}}, C_{\mathrm{X1}}$ and $L_{\mathrm{X2}}, C_{\mathrm{X2}}$ in Fig. 9.2) can realize this value of X, but with different tradeoffs. For instance, designs with relatively large inductance values may suffer from high inductor losses, but also exhibit highly sinusoidal currents that result in relatively low turn-off switching losses. On the other hand, designs with very small inductance values may have low inductor losses, but exhibit highly distorted currents that lead to high turn-off losses. To achieve a favorable tradeoff in this scenario, the circuit waveforms of the WPT system of Fig. 9.2 can be evaluated across a range of inductance and capacitance values using the enhanced augmented state-space analysis approach of Chapter 2, and the inductance-capacitance combinations that result in the lowest total losses can be selected.

9.3 Alternative Applications

The proposed VCI can be utilized in a wide variety of WPT systems, both inductive and capacitive. Examples of inductive and capacitive WPT systems incorporating the VCI are shown in Fig. 9.4. These WPT systems utilize resonant networks that provide voltage and/or current gain as well as compensation for the reactance of the WPT coupler under nominal conditions. When the coupling reactance changes from its nominal value, the VCI provides the required additional compensation. The gain and compensation networks in these WPT systems can have various topologies, including L-section matching networks such as those shown in Fig. 9.5. When appropriately designed, these matching networks can enhance the compensation provided by the VCI.

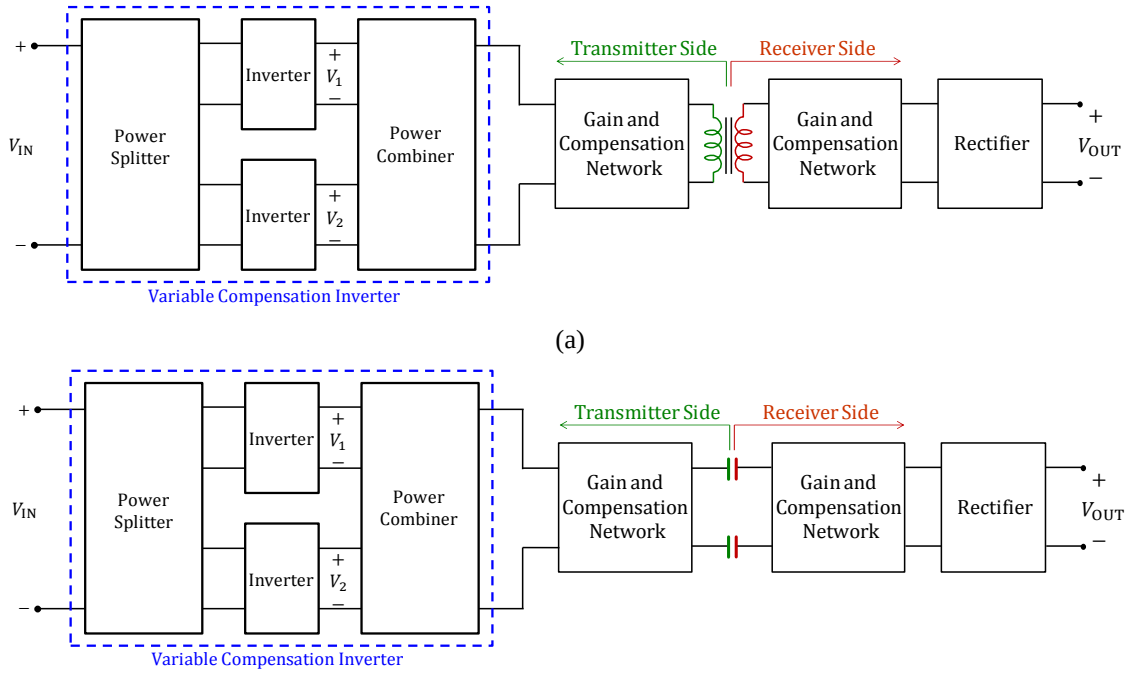


Figure 9.4: Utilization of the proposed VCI in: (a) an inductive WPT system and (b) a capacitive WPT system comprising gain and compensation networks.

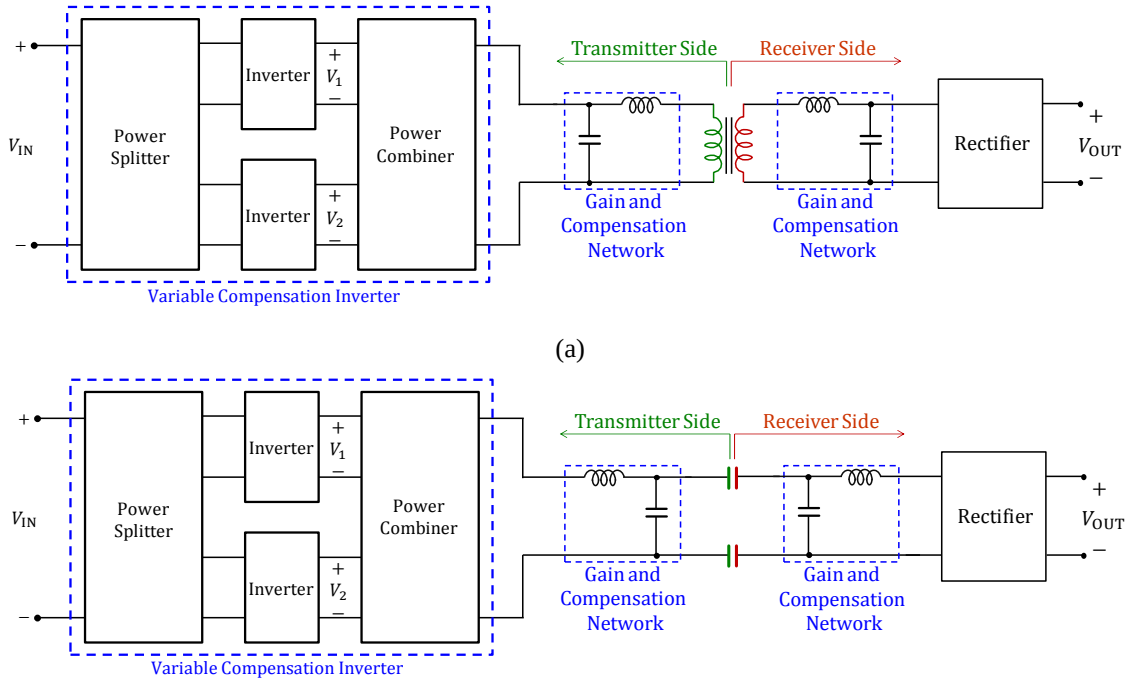


Figure 9.5: Utilization of the proposed VCI in: (a) an inductive WPT system and (b) a capacitive WPT system comprising gain and compensation networks implemented as L-section matching networks.

9.4 PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

A prototype VCI similar to the one shown in Fig. 9.2 is designed, built and tested with a 1.5-MHz, 65-W capacitive WPT system with dc input and output voltages of 20 V, suitable for a laptop charging application. A photograph of the prototype system is shown in Fig. 9.6. The capacitive coupler in the prototype system is implemented using two pairs of 10 cm × 10 cm plates separated by a 1-mm air-gap. The dc-dc converters of the VCI are emulated using two independent power supplies, and the rectifier and laptop battery are emulated using an equivalent load resistor. The inductors in the prototype system are realized using AWG-48, 1000-strand Litz wire wound on RM14 cores of Ferroxcube's 3F46 material. The two inverters of the VCI are constructed using 80-V, 90-A EPC2021 enhancement-mode GaN transistors driven by TI LM5113 half-bridge gate drivers. The system is first tested under nominal operating conditions, that is, with the coupling plates perfectly aligned, and with the input voltages of the two bridge rectifiers set equal to the dc input voltage V_{IN} of 20 V. The corresponding waveforms of the inverter switch-node voltages and the voltage across the load resistor are shown in Fig. 9.7(a). The system transfers the rated power of 65 W at an efficiency of 82% under these conditions. The plates are then misaligned by 50% along a lateral dimension, and the resultant waveforms are shown in Fig. 9.7(b). It can be seen that the load voltage decreases; the output power falls by 35% to 42 W, and the efficiency falls to 74%. The VCI then decreases the inverter phase-shift, increases the input voltage of the bottom inverter, and decreases the input voltage of the top inverter in accordance with (9.2)-(9.4). The resultant waveforms are shown in Fig. 9.7(c). As can be seen, the load

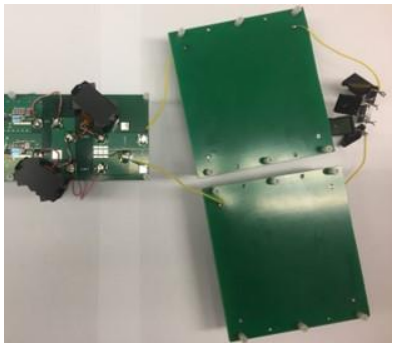


Figure 9.6: Photograph of the prototype capacitive WPT system incorporating a variable compensation inverter.

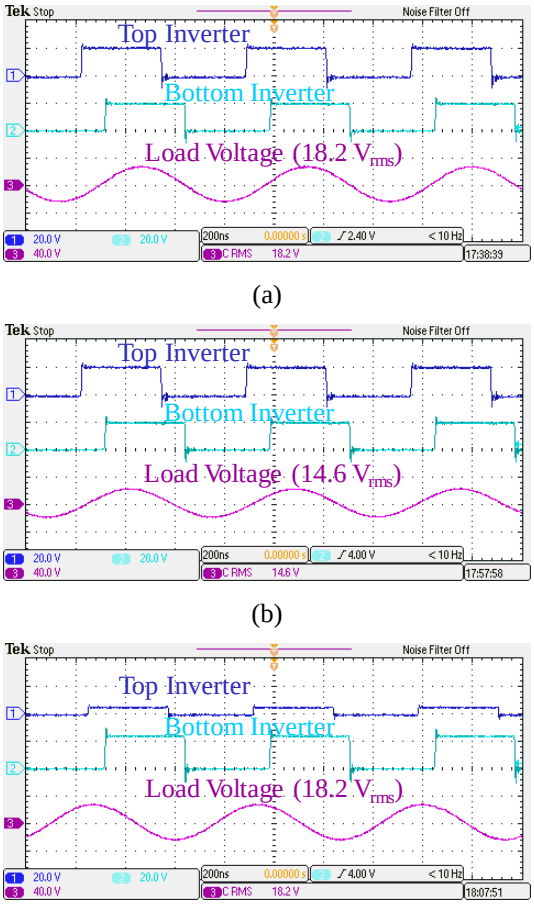


Figure 9.7: Measured switch-node voltages of the two bridge inverters of the prototype variable compensation inverter (VCI) and the voltage across the resistive load for: (a) nominal operating condition with no misalignment, (b) 50% misalignment with no compensation, and (c) 50% misalignment fully compensated by the VCI.

voltage is restored to the original level shown shown in Fig. 9.7(a); the output power is restored to 65 W, and the efficiency increases back to 82%. Hence, the prototype VCI successfully compensates for coupling variations while maintaining fixed output power and high efficiency.

9.5 Chapter Summary and Conclusions

This chapter introduces a new high-frequency inverter architecture that fully compensates for coupling variations in wireless power transfer (WPT) systems while operating at a fixed frequency and maintaining high efficiency. This architecture, termed the variable compensation inverter (VCI), comprises multiple high-frequency inverters fed by controllable voltages, and feeding a lossless resonant network. By appropriately controlling the relative phase-shift and the input voltages of the inverters, the VCI can provide

variable compensation while maintaining zero-voltage and near-zero-current switching. The VCI also ensures that the output power of the WPT system is maintained at a fixed level even during coupling variations. A prototype VCI is designed, built and tested, and its performance validated, with a 1.5-MHz, 65-W capacitive WPT system for laptop charging applications.

Chapter 10
Conclusions

10.1 Thesis Summary and Conclusions

Power converters for telecommunication and datacenter applications need to achieve high power density and maintain high efficiency across wide ranges of operation. Achieving high power density necessitates increasing the power converter's switching frequency. To maintain high efficiency at high switching frequencies, soft-switching in the form of zero-voltage switching (ZVS) and/or zero-current switching (ZCS) is required. Unfortunately, conventional soft-switching converters lose soft-switching as operating conditions change. This challenge is addressed by the recently introduced impedance control network (ICN) converter architecture, which is capable of maintaining ZVS and near-ZCS operation, and hence, a high and flat efficiency, across wide operating ranges. However, conventional ICN converters suffer from power density limitations due to their use of three or more magnetic structures, and due to the use of burst-mode control that requires bulky input and output capacitors. This thesis introduces new ICN converter topologies and associated design methodologies and control techniques, which enable high power density to be achieved while maintaining high wide-range efficiencies.

Chapter 2 of this thesis introduces an enhanced augmented state-space analysis approach for steady-state modeling of resonant converters (now also published in [136]). This approach allows the behavior of resonant converters, even those with high-order resonant networks such as the ICN converter, to be predicted in an accurate and computationally efficient manner. High computational efficiency is achieved by combining conventional augmented state-space analysis with an optimized numerical algorithm that allows initially unknown switching instants to be quickly determined. Modeling accuracy is enhanced by incorporating circuit non-idealities such as diode parasitic capacitances. In conjunction with accurate loss models, this modeling approach can enable comprehensive design optimization of resonant converters.

Chapter 3 of this thesis introduces an ICN dc-dc converter suitable as an isolated telecom power supply

with both step-up and step-down voltage conversion capability (now also published in [137]). The switching instants of the synchronous rectifier of this converter are predicted, and the inductance and capacitance values of its resonant tanks are optimally selected, using the enhanced augmented state-space analysis approach described in Chapter 1. A prototype 1-MHz, 550-W ICN converter operating over an input voltage range of 36 V to 60 V, and a regulated output voltage in the range of 34 V to 55 V is designed, built and tested. The prototyped ICN converter achieves a peak efficiency of 97.6% and maintains full-power efficiencies above 95.3% across its full range of input and output voltages. It also maintains greater than 93.6% efficiency across its 10:1 output power range, for the entire range of input and output voltages.

Chapter 4 of this thesis introduces a magnetics integration approach that allows the power density of ICN converters to be substantially increased while maintaining high efficiency (now also published in [138]). In this approach, the three inductors of the ICN converter are combined into a single integrated magnetic structure using two coupled windings. This integrated magnetic structure is realized on a custom-designed planar core, and its winding and core losses are minimized using 3D finite-element analysis (FEA). A prototype 1-MHz ICN converter with its three inductors implemented as a single planar integrated magnetic structure is designed, built and tested. This converter is designed for the same input voltage, output voltage and power specifications as those utilized for the ICN converter of Chapter 3. The prototype ICN converter achieves a peak full-power efficiency of 96.7% and maintains greater than 94.8% efficiency at full-power across its nearly 2:1 ranges of input voltage and output voltage. It also maintains above 93.2% efficiency over a 10:1 output power range across its full input and output voltage range. This 550-W prototype conforms to the dimensions of a quarter brick and achieves a power density of 462 W/in^3.

Chapter 5 of this thesis introduces a new approach to regulating the output voltage and power of ICN converters, which that can further enhance their power density and efficiency (now also published in [139] and accepted for publication in [140]). In this approach, termed multimode topology morphing control, the rectifier of the ICN converter dynamically alternates between full-bridge and half-bridge

topologies. Compared to burst-mode control, which is conventionally utilized in ICN converters to regulate output voltage and power, this multimode topology morphing control reduces output capacitance requirement, hence, improving power density, and improves partial-power efficiencies. These performance enhancements are analytically evaluated and quantified for a step-down ICN converter design. A closed-loop control architecture for the proposed multimode topology morphing is also introduced, which ensures smooth mode transitions while regulating output voltage across input voltage and load transients. A prototype 1-MHz, 120-W step-down ICN resonant converter designed for an input voltage range of 18 V to 36 V, an output voltage of 12 V, and a 10:1 output power range, suitable as an intermediate bus converter in a telecommunication power distribution system, is built and tested. Compared to burst-mode control, the topology morphing control reduces the output capacitance requirement in the prototype ICN converter by 57% and reduces converter losses at partial power levels by up to 46.5%, validating the analytical predictions. The prototype ICN converter is also tested under closed-loop control using a digitally implemented controller, and is shown to successfully regulate its output voltage with smooth mode transitions under input voltage and load variations.

Chapter 6 of this thesis introduces two ICN-based dc-dc converter topologies suitable as a single-stage isolated 48V-to-1.8V point-of-load (PoL) converter for datacenters (now also published in [141] and [142]). The first ICN converter achieves large step-down while maintaining high efficiency using stacked inverters, a transformer, and a resonant current-doubler rectifier. The power density of this converter is enhanced by combining the three inductors of the ICN into a single integrated magnetic structure, as described in Chapter 4. A prototype 250-kHz, 90-W PoL ICN converter utilizing planar PCB-integrated magnetics, designed to operate over an input voltage range of 36 V to 60 V and an output voltage of 1.8 V is built and tested. The prototyped converter achieves a peak efficiency of 88.7%, maintains full-power efficiencies above 87.6% across its nearly 2:1 input voltage range, and above 86.6% efficiency across a 10:1 output power range at its nominal input voltage of 48 V. Based on the learnings from this converter, a second ICN converter is developed. This converter avoids voltage unbalance issues that arise from stacking inverters, and instead achieves a portion of its large step-down using an immittance network. The

inductance of this immittance network is realized using the magnetizing inductance of the transformer, hence, not requiring any additional magnetic component. The power density of this converter is enhanced by combining its magnetic components into two integrated magnetic structures: one implementing the three inductors of the ICN using two coupled windings, and the other implementing the immittance network transformer and current-doubler magnetics on a common core. A systematic methodology is introduced to design and optimize the proposed ICN converter. A prototype 500-kHz, 90-W, 36V-to-60V input, 1.8-V output PoL ICN converter utilizing planar PCB-integrated magnetics is built and tested. The prototype ICN converter achieves a peak efficiency of nearly 90%, maintains greater than 87.9% full-power efficiency across its nearly 2:1 input voltage range, and greater than 86.8% efficiency across its 10:1 power range at its nominal input voltage of 48 V.

Chapter 7 of this thesis introduces a third PoL ICN converter topology that enables substantially improved efficiency and power density compared to the converters developed in Chapter 6 (now also accepted for publication in [143]). Higher efficiency is achieved using an alternative implementation of the immittance network, one that is functionally equivalent to the one utilized in the second ICN converter in Chapter 6, but reduces core losses by not utilizing the transformer magnetizing inductance. Furthermore, the two inductors required in this implementation of the immittance network are obtained from the coupling of the ICN inductors, and the other from the leakage inductance of the transformer; hence, not requiring any additional magnetic component. Further efficiency improvement is achieved by employing a distributed transformer structure, in which the transformer's secondary windings are paralleled after rectification; hence, avoiding ac losses in the winding interconnects. The resultant ICN converter utilizes only two magnetic structures: one for the coupled inductors and the other for the distributed transformer. To increase power density, both these magnetic structures are realized using custom core geometries, and designed and optimized using 3D FEA. Power density is further enhanced by regulating the converter's output voltage using rectifier phase-shift control, which eliminates the need for bulky input and output capacitors. These improvements culminate in a high-power-density high-efficiency 48V-to-1.8V ICN converter. A prototype 1-MHz, 90-W, 36V-to-60V input, 1.8-V output PoL

ICN converter is built and tested. The prototyped converter achieves a peak efficiency of 92.6%, maintains full-power efficiencies above 91.3% across its nearly 2:1 input voltage range, and greater than 83.9% efficiency across its 10:1 power range at its nominal input voltage of 48 V. The prototyped converter also achieves a power density of 314 W/in^3.

Chapter 8 of this thesis introduces a new approach to designing multistage matching networks, which find application in large-conversion-ratio resonant converters and in wireless power transfer (WPT) systems (now also published in [144], [145]). In the conventional approach to designing multistage matching networks, each stage is constrained to have resistive input and load impedances. In the proposed approach, this constraint is relaxed, and each intermediate stage of a multistage matching network is allowed to have complex input and load impedances, enabling a substantially larger design space to be explored. The method of Lagrange multipliers is used to determine the gain and impedance characteristics of each stage in the matching network that maximize overall efficiency. Compared with the conventional design approach, the proposed approach achieves higher efficiency, resulting in loss reduction of up to 35% for a three-stage L-section matching network. The theoretical predictions are validated experimentally using a three-stage matching network designed for 1-MHz and 100-W operation.

Finally, Chapter 9 of this thesis introduces a new high-frequency inverter architecture to compensate for coupling variations in WPT systems (now also published in [146]). This architecture, termed the variable compensation inverter (VCI), comprises multiple high-frequency inverters feeding a lossless resonant network, with the inputs of the inverters fed by controllable voltages. By appropriately controlling the input voltages of the individual inverters and their relative phase-shift, the VCI can maintain near-resistive, and slightly inductive, loading of the inverters even as the reactance of the WPT coupler changes; hence, providing compensation while maintaining zero-voltage and near-zero-current switching. The VCI also ensures that the output power of the WPT system is maintained at a fixed level even during coupling variations. A prototype VCI is designed, built and tested with a 1.5-MHz 65-W capacitive WPT system for laptop charging applications. The system is able to fully compensate for up to 50% lateral misalignments in the capacitive coupler while maintaining a fixed output power level of 65 W

and achieving high efficiency.

10.2 Recommendations for Future Work

This thesis introduces ICN converter topologies and associated design and control approaches that enable high power density and high efficiency. There are numerous opportunities to build upon this work, three of which are identified below.

The power consumption of digital loads, including central processing units (CPUs), graphics processing units (GPUs) and application-specific integrated circuits (ASICs), can often change abruptly and by large amounts. To cope with such load transients while preventing equipment failure, PoL power converters need to exhibit fast and yet well-damped transient responses. The high-performance PoL ICN converter described in Chapter 7 is operated under open-loop control. For this converter to be successfully deployed in PoL application, its load transient response needs to be investigated. This would require dynamic modeling of this ICN converter. One pathway to obtaining this model is to improve upon the low-frequency dynamic model for ICN converters introduced in [25], [27], such that it is able to capture the high-frequency characteristics of the ICN converter. Such a model can then be utilized to explore the response of the PoL ICN converter of Chapter 7 to fast and large load transients.

The high-performance ICN converters presented in Chapters 4 and 7 both employ two magnetic structures: a coupled inductor structure and a transformer. To further enhance the power density of these ICN converters, it would be valuable to explore methods to integrate these magnetic components further into one structure. A baseline approach to doing this would be to realize the coupled inductors and the transformer on a common core, while keeping the two components magnetically decoupled using a zero-air-gap core leg (which acts as the magnetic equivalent of a short-circuit). This approach can reduce the overall magnetic footprint, and reduce core losses due to a smaller overall core volume. However, a more exciting opportunity is to truly integrate the coupled inductors and the transformer, that is, to employ a common set of coupled windings on a single magnetic structure that performs the functions of both the coupled inductors and the transformer.

Chapters 6 and 7 of this thesis present ICN converters suitable for a large step-down (48V-to-1.8V) PoL application. As discussed in Chapter 1, such large step-down PoL converters embody a move towards reducing the number of power conversion stages in datacenters, with the objectives of reducing losses and saving space. The resultant power distribution architecture, shown in Fig. 1.3(b), has two power conversion stages. However, in most datacenters, the front-end ac-dc converter itself comprises two stages: a power factor correction (PFC) stage that converts the ac line voltage to a dc voltage in the vicinity of 400 V, and an isolated dc-dc conversion stage that steps this voltage down to 48 V. It is envisioned that further advances in efficiency and power density can be made by eliminating this 400-V to 48-V conversion stage, and instead utilize a single-stage power converter that directly steps down the 400-V dc voltage to the required point-of-load voltages. The PoL ICN converter architecture developed in Chapter 7 can be a candidate for this extreme step-down application. However, to keep the transformer turns ratio from becoming prohibitively large, it may be best to connect multiple such PoL ICN converters in an input-series output-parallel (ISOP) configuration. This approach may require sophisticated control techniques to ensure that the converters have balanced input voltages and power, and new magnetics integration approaches to reduce the total number of magnetic components.

The work on design optimization of high-efficiency matching networks presented in Chapter 8 could also be built upon in several ways. For instance, the approach of Chapter 8 can be augmented to perform a multi-objective optimization of matching networks, wherein other desirable objectives, such as size, are also incorporated in addition to efficiency. The approach can also be extended to cases where both voltage/current gain and reactive compensation are required, such as in WPT systems. Some work in this direction has already been carried out for capacitive WPT systems [70], [76], and application to inductive WPT systems can be explored. Finally, the approach of Chapter 8 considers lumped-element (inductor and capacitor) based matching networks. It is possible to extend this approach to optimize matching networks implemented using transmission lines, such as in microwave communication systems.

It is hoped that this thesis will motivate the exploration of these exciting research opportunities.

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Appendix A
Generalized Expressions for Output Power and Inverter Phase-Shift in ICN Converters

This appendix derives generalized expressions for the maximum output power and inverter phase-shift in ICN converters. These expressions are applicable to all ICN converter topologies described in this thesis, and the derivation approach is applicable to all ICN converters previously presented in the literature [23]-[29]. Using fundamental frequency analysis, the ICN converter can be modeled as shown in Fig. A.1. In this model, the phasors $\hat{V}_1$ and $\hat{V}_2$ represent the output voltages of the two inverters, $\hat{I}_1$ and $\hat{I}_2$ represent the output currents of the inverters, and R_{X} is the equivalent resistance of the rectifier referred to the primary side of the transformer. Expressions for the voltages $\hat{V}_1$ and $\hat{V}_2$ and the resistance R_{X} are given by:

$$\hat{V}_1 = K_{\mathrm{inv}} V_{\mathrm{IN}} e^{j\Delta}\,. \tag{A.1}$$

$$\hat{V}_2 = K_{\mathrm{inv}} V_{\mathrm{IN}} e^{-j\Delta}\,. \tag{A.2}$$

$$R_{\mathrm{X}} = \frac{K_{\mathrm{rec}} V_{\mathrm{OUT}}^2}{N^2 P_{\mathrm{OUT}}}\,. \tag{A.3}$$

Here, the transformer has a turns ratio of $1:N$, K_{inv} is a constant associated with the topology of the

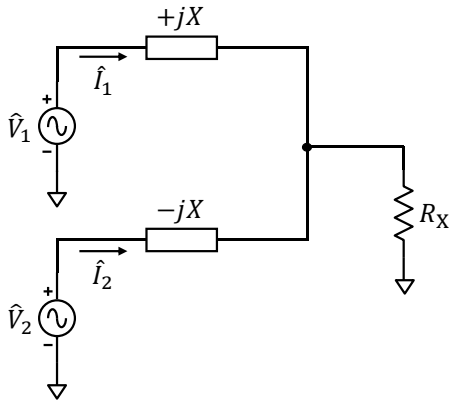

Figure A.1: Fundamental-frequency model of the ICN converter.

inverters, with $K_{\text{inv}} = \frac{2}{\pi}$ for half-bridge inverters and $K_{\text{inv}} = \frac{4}{\pi}$ for full-bridge inverters. Similarly, K_{rec} is a constant associated with the topology of the rectifier, with $K_{\text{rec}} = \frac{2}{\pi^2}$ for a half-bridge rectifier, $K_{\text{rec}} = \frac{8}{\pi^2}$ for a full-bridge rectifier, and $K_{\text{rec}} = \frac{32}{\pi^2}$ for a current-doubler rectifier. Expressions for the inverter output currents $\hat{I}_1$ and $\hat{I}_2$ can be obtained by applying superposition to the circuit model of Fig. A.1, and are given by:

$$\hat{I}_1 = \frac{R_{\text{X}} - jX}{X^2}\hat{V}_1 - \frac{R_{\text{X}}}{X^2}\hat{V}_2\,, \tag{A.4}$$

$$\hat{I}_2 = \frac{R_{\text{X}} + jX}{X^2}\hat{V}_2 - \frac{R_{\text{X}}}{X^2}\hat{V}_1\,. \tag{A.5}$$

Hence, the effective admittances seen by the two inverters can be expressed as:

$$\hat{Y}_1 \equiv \frac{\hat{I}_1}{\hat{V}_1} = \frac{R_{\text{X}} - jX}{X^2} - \frac{R_{\text{X}}}{X^2}e^{-2j\Delta} = \frac{R_{\text{X}}}{X^2}(1 - \cos 2\Delta) + j\frac{1}{X}\left(\frac{R_{\text{X}}}{X}\sin 2\Delta - 1\right), \tag{A.6}$$

$$\hat{Y}_2 \equiv \frac{\hat{I}_2}{\hat{V}_2} = \frac{R_{\text{X}} + jX}{X^2} - \frac{R_{\text{X}}}{X^2}e^{2j\Delta} = \frac{R_{\text{X}}}{X^2}(1 - \cos 2\Delta) - j\frac{1}{X}\left(\frac{R_{\text{X}}}{X}\sin 2\Delta - 1\right). \tag{A.7}$$

It can be seen from (A.6) and (A.7) that the admittances seen by the two inverters are complex conjugates of one another. Therefore, to achieve zero-current switching of the inverter transistors, the imaginary part of both the admittances can be simultaneously made zero by utilizing the following inverter phase-shift:

$$2\Delta = \sin^{-1}\frac{X}{R_{\text{X}}}. \tag{A.8}$$

Next, assuming lossless power conversion, the converter's output power equals its input power, that is:

$$P_{\text{OUT}} = P_{\text{IN}} = \text{Re}\left\{\frac{1}{2}\hat{V}_1\hat{V}_1^*Y_1^* + \frac{1}{2}\hat{V}_2\hat{V}_2^*Y_2^*\right\} = (K_{\text{inv}}V_{\text{IN}})^2\frac{R_{\text{X}}(1 - \cos 2\Delta)}{X^2}. \tag{A.9}$$

Replacing R_{X} and 2Δ in (A.9) by their expressions given in (A.3) and (A.8), respectively, and simplifying, the maximum output power delivered by an ICN converter with a $1{:}\,N$ transformer (and no immittance network) can be expressed as:

$$P_{\text{OUT,max}} = \frac{K_{\text{inv}}V_{\text{IN}}}{NX}\sqrt{2K_{\text{rec}}V_{\text{OUT}}^2 - K_{\text{inv}}^2N^2V_{\text{IN}}^2}\,. \tag{A.10}$$

Power levels below the maximum power level given by (A.10) can be delivered either using burst-

mode control, topology morphing control or rectifier phase-shift control. With appropriate inverter and rectifier constants (K_{inv} and K_{rec}), (A.10) yields the maximum output power expressions for the ICN converters of Chapters 3-5. For the ICN converters of Chapter 6 and 7, the following modifications need to be made: first, since the transformer turns ratio is specified as $N\colon 1$ in these chapters (unlike $1\colon N$ for the earlier chapters), N should be replaced by $1/N$ in (A.10). This directly results in the maximum output power expression for ICN converters with a $N\colon 1$ transformer and no immittance network:

$$P_{\text{OUT,max}} = \frac{K_{\text{inv}} V_{\text{IN}}}{X} \sqrt{2K_{\text{rec}} N^2 V_{\text{OUT}}^2 - K_{\text{inv}}^2 V_{\text{IN}}^2}\,. \tag{A.11}$$

For the second ICN converter of Chapter 6, and the ICN converter of Chapter 7, both of which utilize immittance networks, the expression for the equivalent resistance R_{X} in the fundamental-frequency model of Fig. A.1 is modified to:

$$R_{\text{X}} = \frac{X_{\text{imt}}^2}{\left(\frac{N^2 K_{\text{rec}} V_{\text{OUT}}^2}{P_{\text{OUT}}}\right)}. \tag{A.12}$$

Here, X_{imt} is the reactance of the immittance network. This new expression for R_{X} can now to utilized in (A.8) and (A.9) to yield the following maximum output power expression for ICN converters with a $N\colon 1$ transformer and an immittance network with reactance X_{imt}:

$$P_{\text{OUT,max}} = K_{\text{inv}}^2 \sqrt{K_{\text{rec}}} \left(\frac{N}{X_{\text{imt}}}\right) \frac{V_{\text{IN}}^2}{X} \frac{V_{\text{OUT}}}{\sqrt{\frac{2K_{\text{inv}}^2 V_{\text{IN}}^2}{X^2} - \left(\frac{N}{X_{\text{imt}}}\right)^2 K_{\text{rec}} V_{\text{OUT}}^2}}. \tag{A.13}$$

The inverter phase-shift 2Δ can be determined from (A.8) by replacing R_{X} with its expression given in (A.3) or (A.12), and P_{OUT} with the corresponding expressions for maximum output power given in (A.10), (A.11) or (A.13). For ICN converters having a $1\colon N$ transformer and no immittance network, the inverter phase-shift is given by:

$$2\Delta = 2\cos^{-1}\left(\frac{K_{\text{inv}}}{\sqrt{2K_{\text{rec}}}} \frac{N V_{\text{IN}}}{V_{\text{OUT}}}\right). \tag{A.14}$$

For ICN converters having a $N\colon 1$ transformer and no immittance network, the inverter phase-shift is

given by:

$$2\Delta = 2\cos^{-1}\left(\frac{K_{\text{inv}}}{\sqrt{2K_{\text{rec}}}}\frac{V_{\text{IN}}}{NV_{\text{OUT}}}\right). \tag{A.15}$$

Finally, for ICN converters having a $N{:}\,1$ transformer and an immittance network with reactance X_{imt}, the inverter phase-shift is given by:

$$2\Delta = \cos^{-1}\left(1 - \frac{X^2 K_{\text{rec}} N^2 V_{\text{OUT}}^2}{X_{\text{imt}}^2 K_{\text{inv}}^2 V_{\text{IN}}^2}\right). \tag{A.16}$$

The above-described procedure can also be applied to rectifier phase-shift controlled ICN converters such as the ICN converter of Chapter 7, with one modification: the equivalent resistance of the rectifier computed using (A.3) or (A.12) needs to be multiplied by a factor of $\sin^2\frac{\Phi}{2}$, where Φ is the phase-shift between the two legs of the full-bridge rectifier.

Appendix B
Design Methodology for Topology Morphing Controlled Step-Down ICN Converter

This appendix presents the methodology used to design the step-down ICN converter employed in Chapter 5 to quantify the performance benefits of the proposed topology morphing control. This converter has the topology shown in Fig. 5.2, and is designed for an input voltage range, $V_{\mathrm{IN,min}}$ to $V_{\mathrm{IN,max}}$, of 18 V to 36 V, an output voltage V_{OUT} of 12 V, and a rated output power $P_{\mathrm{OUT,rated}}$ of 120 W. The switching frequency of the converter is chosen to be 1 MHz. The converter is designed to be able to deliver its rated output power $P_{\mathrm{OUT,rated}}$ at all input voltages when operating with a full-bridge rectifier. It can be seen from Fig. 5.3 that the full-bridge maximum output power of the ICN converter $P_{\mathrm{OUT,max,FB}}$ is the lowest at its minimum input voltage. Therefore, if the converter is designed to deliver its rated output power with a full-bridge rectifier at its minimum input voltage, it can deliver the rated power at all input voltages. This results in the first design constraint:

$$P_{\mathrm{OUT,max,FB}} \mid_{V_{\mathrm{IN}}=V_{\mathrm{IN,min}}} = P_{\mathrm{OUT,rated}} \,. \tag{B.1}$$

In the topology morphing control scheme, at some output power levels, the rectifier input current is higher with a half-bridge rectifier than with a full-bridge rectifier. High rectifier input currents result in increased losses in the components on the secondary side of the transformer. An effective approach to reducing these losses is to limit the maximum output power that the ICN converter delivers with a half-bridge rectifier. This can be ensured by designing the converter to deliver the same maximum half-bridge power $P_{\mathrm{OUT,max,HB}}$ at its minimum and maximum input voltages, resulting in the second design constraint:

$$P_{\mathrm{OUT,max,HB}} \mid_{V_{\mathrm{IN}}=V_{\mathrm{IN,min}}} = P_{\mathrm{OUT,max,HB}} \mid_{V_{\mathrm{IN}}=V_{\mathrm{IN,max}}} \,. \tag{B.2}$$

Using the maximum power expressions given in (5.1) and (5.2), the design constraints of (B.1) and (B.2) can be satisfied by choosing the ICN differential reactance X and transformer turns ratio N according to

the following relationships:

$$X = \frac{4}{\pi^2} \frac{V_{\text{IN,min}} \sqrt{3V_{\text{IN,min}}^2 + 4V_{\text{IN,max}}^2}}{P_{\text{OUT,rated}}}. \tag{B.3}$$

$$N = \frac{V_{\text{OUT}}}{\sqrt{V_{\text{IN,min}}^2 + V_{\text{IN,max}}^2}}. \tag{B.4}$$

With the given input voltage, output voltage and rated output power specifications, the design equations of (B.3) and (B.4) result in an ICN differential reactance X of 4.8 Ω and a transformer turns ratio N of 0.3 (corresponding to a 3.3:1 transformer). Since the transformer windings can only have integer numbers of turns, a 3.3:1 transformer requires multiple turns in the secondary winding (for instance, 10 primary turns and 3 secondary turns). However, since this ICN converter provides a voltage step-down, the secondary winding of the transformer carries high currents. To maintain low winding losses in the secondary winding, it is desirable to utilize a single-turn secondary. Therefore, the ICN converter is designed here with a more practical turns ratio of 4:1 (4 primary turns and 1 secondary turn). This higher turns ratio (or, lower value of N) than the ideal value given by (B.4) results in the ICN converter generating more power than required (see (5.1) and (5.2)); to compensate, the value of the ICN differential reactance X is selected to be 5.2 Ω – slightly higher than its ideal value of 4.8 Ω given by (B.3). Since these choices of N and X do not exactly satisfy (B.3) and (B.4), the resultant design may also be expected not to satisfy the design constraints of (B.1) and (B.2). However, the full-bridge maximum and half-bridge maximum power levels of the ICN converter designed with these values of N and X, shown in Fig. 5.7, indicate that the converter can deliver its rated output power of 120 W with a full-bridge rectifier across its entire input voltage range, hence fulfilling the purpose of (B.1). Furthermore, the half-bridge maximum power, though not equal at the minimum and maximum input voltages as required by (B.2), is still fairly constrained across the input voltage range, hence satisfying the intent of (B.2).

The next step is to select the inductance and capacitance values of the three resonant tanks of the ICN converter. These are selected to ensure that the two resonant tanks connected at the inverter outputs have

impedances of $+jX$ and $-jX$, and the third resonant tank has an impedance of zero (that is, it resonates) at the converter's switching frequency of 1 MHz. The inductors and the transformer are then designed using Litz wire windings and RM10 cores built with the Ferroxcube 3F46 material, which is suitable for low-loss operation at 1 MHz. The ac resistances of the inductor and transformer windings are estimated using the formulation provided in [129], and the Steinmetz parameters of the 3F46 material are computed using curve fitting on the core loss data provided in the manufacturer's datasheet [126]. The capacitors of the three resonant tanks are selected to be NP0 ceramic capacitors, and their equivalent series resistances (ESRs) at 1 MHz are also obtained from the manufacturer's datasheets. The resulting design of the step-down ICN converter is detailed in Table 5.1.

Appendix C
Expressions for Low-Frequency Ripple under Burst-Mode and Topology Morphing Control

This appendix derives the expressions for the low-frequency ripple in the output voltage of the ICN converter under burst-mode control and under topology morphing control, as given in (5.8) and (5.9), respectively. In the full-bridge rectifier mode, the low-frequency component of the current delivered by the converter to the output capacitor and the load is given by:

$$I_{\mathrm{OUT,conv,FB}} = \frac{P_{\mathrm{OUT,max,FB}}}{V_{\mathrm{OUT}}} = \frac{4V_{\mathrm{IN}}}{\pi^2 NXV_{\mathrm{OUT}}}\sqrt{4V_{\mathrm{OUT}}^2 - N^2V_{\mathrm{IN}}^2}\,. \tag{C.1}$$

The portion of this current delivered to the load is given by:

$$I_{\mathrm{OUT,load}} = \frac{P_{\mathrm{OUT}}}{V_{\mathrm{OUT}}}. \tag{C.2}$$

Therefore, the current flowing through the output capacitor is given by:

$$I_{C_{\mathrm{OUT}}} = I_{\mathrm{OUT,conv,FB}} - I_{\mathrm{OUT,load}} = \frac{P_{\mathrm{OUT,max,FB}} - P_{\mathrm{OUT}}}{V_{\mathrm{OUT}}}. \tag{C.3}$$

When the rectifier operates in full-bridge mode (in both burst-mode and topology morphing control), the output capacitor charges up and the output voltage swings from its minimum value to its maximum value. The peak-to-peak ripple in the output voltage is then given by:

$$\delta v_{\mathrm{out}} = \frac{I_{C_{\mathrm{OUT}}} T_{\mathrm{FB}}}{C_{\mathrm{OUT}}}. \tag{C.4}$$

Here T_{FB} is the time that the converter spends in full-bridge mode. This time is different for the conventional and proposed control methods; for the same output power requirement, the converter spends less time in the full-bridge mode in the proposed topology morphing control, as compared to that in the conventional burst-mode control. In burst-mode control, the full-bridge mode duration is given by:

$$T_{\mathrm{FB,burst}} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,FB}}}\frac{1}{f_{\mathrm{burst}}}. \tag{C.5}$$

Using (C.4) and (C.5), the output voltage ripple in burst-mode control can be expressed as:

$$\delta v_{\text{out,burst}} = \frac{P_{\text{OUT,max,FB}} - P_{\text{OUT}}}{C_{\text{OUT}}\, V_{\text{OUT}}} \frac{P_{\text{OUT}}}{P_{\text{OUT,max,FB}}} \frac{1}{f_{\text{burst}}}. \tag{C.6}$$

Rearranging the right-hand side of (C.6) results in the expression for burst-mode ripple given in (5.8). In topology morphing control, the full-bridge mode duration can be obtained using (5.4) and (5.5), and is given by:

$$T_{\text{FB,morph}} = \frac{P_{\text{OUT}} - P_{\text{OUT,max,HB}}}{P_{\text{OUT,max,FB}} - P_{\text{OUT,max,HB}}} \frac{1}{f_{\text{morph}}}. \tag{C.7}$$

Using (C.4) and (C.7), the output voltage ripple in topology morphing control can be expressed as:

$$\delta v_{\text{out,morph}} = \frac{P_{\text{OUT,max,FB}} - P_{\text{OUT}}}{C_{\text{OUT}}\, V_{\text{OUT}}} \frac{P_{\text{OUT}} - P_{\text{OUT,max,HB}}}{P_{\text{OUT,max,FB}} - P_{\text{OUT,max,HB}}} \frac{1}{f_{\text{morph}}}. \tag{C.8}$$

Rearranging the right-hand side of (C.8) results in the expression for topology-morphing ripple given in (5.9).

Appendix D
Expressions for Power Losses under Burst-Mode and Topology Morphing Control

This appendix derives the expressions for power losses in the ICN converter that are used in Chapter 5 to compare converter losses under topology morphing control with those under burst-mode control. The derivation begins by evaluating the inverter output currents and rectifier input current in terms of the full-bridge maximum and half-bridge maximum power levels of the ICN converter. Owing to near-ZCS operation, the output voltage and output currents of the two inverters are approximately in phase. Using fundamental frequency analysis to model the inverter output voltages and currents, the peak and RMS values of the two inverter output currents in the full-bridge rectifier mode can be expressed as:

$$\left|\hat{I}_{\mathrm{i1,FB}}\right| = \left|\hat{I}_{\mathrm{i2,FB}}\right| \stackrel{\mathrm{def}}{=} I_{\mathrm{pk,inv,FB}} = \sqrt{2} I_{\mathrm{rms,inv,FB}} = 2\frac{\left(\frac{P_{\mathrm{OUT,max,FB}}}{2}\right)}{\frac{2}{\pi}V_{\mathrm{IN}}}. \tag{D.1}$$

Here $\hat{I}_{\mathrm{i1,FB}}$ and $\hat{I}_{\mathrm{i2,FB}}$ are the phasor-domain output currents of the top and bottom inverters, respectively, and $I_{\mathrm{pk,inv,FB}}$ and $I_{\mathrm{rms,inv,FB}}$ are the peak and RMS values of these currents. Similarly, the peak and RMS values of the inverter output currents in the half-bridge rectifier mode are given by:

$$\left|\hat{I}_{\mathrm{i1,HB}}\right| = \left|\hat{I}_{\mathrm{i2,HB}}\right| \stackrel{\mathrm{def}}{=} I_{\mathrm{pk,inv,HB}} = \sqrt{2} I_{\mathrm{rms,inv,HB}} = 2\frac{\left(\frac{P_{\mathrm{OUT,max,HB}}}{2}\right)}{\frac{2}{\pi}V_{\mathrm{IN}}}. \tag{D.2}$$

Since the rectifier of the ICN converter also operates with near-ZCS, the rectifier input current in the full-bridge and half-bridge rectifier modes can be expressed in terms of the full-bridge and half-bridge maximum power levels, respectively, as:

$$\left|\hat{I}_{\mathrm{r,FB}}\right| \stackrel{\mathrm{def}}{=} I_{\mathrm{pk,rec,FB}} = \sqrt{2} I_{\mathrm{rms,rec,FB}} = 2\frac{P_{\mathrm{OUT,max,FB}}}{\frac{4}{\pi}V_{\mathrm{OUT}}}, \tag{D.3}$$

$$\left|\hat{I}_{\mathrm{r,HB}}\right| \stackrel{\text{def}}{=} I_{\mathrm{pk,rec,HB}} = \sqrt{2} I_{\mathrm{rms,rec,HB}} = 2\frac{P_{\mathrm{OUT,max,HB}}}{\frac{2}{\pi} V_{\mathrm{OUT}}}. \tag{D.4}$$

Next, the peak flux density in the cores of the inductors L_{X1} and L_{X2} in the full-bridge and half-bridge rectifier modes are related to the peak inverter output currents $I_{\mathrm{pk,inv,FB}}$ and $I_{\mathrm{pk,inv,HB}}$ defined in (D.1) and (D.2), as:

$$B_{\mathrm{pk,L_{Xp},FB}} = \frac{L_{\mathrm{Xp}}\, I_{\mathrm{pk,inv,FB}}}{n_{\mathrm{L_{Xp}}} A_{\mathrm{c,L_{Xp}}}} \stackrel{\text{def}}{=} K_{\mathrm{Xp}}\, I_{\mathrm{pk,inv,FB}}\,, \tag{D.5}$$

$$B_{\mathrm{pk,L_{Xp},HB}} = \frac{L_{\mathrm{Xp}}\, I_{\mathrm{pk,inv,HB}}}{n_{\mathrm{L_{Xp}}} A_{\mathrm{c,L_{Xp}}}} \stackrel{\text{def}}{=} K_{\mathrm{Xp}}\, I_{\mathrm{pk,inv,FB}}\,. \tag{D.6}$$

Here the subscript 'p' equals 1 for L_{X1} and 2 for L_{X2}, L_{Xp} is the inductance, $n_{\mathrm{L_{Xp}}}$ is the number of turns and $A_{\mathrm{c,L_{Xp}}}$is the core cross-sectional area of the corresponding inductor, and the factor $\frac{L_{\mathrm{Xp}}}{n_{\mathrm{L_{Xp}}} A_{\mathrm{c,L_{Xp}}}}$ is defined as a constant K_{Xp}. The peak flux density in the inductor L_{r} is similarly related to the peak rectifier input currents in the full-bridge and half-bridge rectifier modes, $I_{\mathrm{pk,rec,FB}}$ and $I_{\mathrm{pk,rec,HB}}$, as:

$$B_{\mathrm{pk,L_r,FB}} = \frac{L_{\mathrm{r}}\, I_{\mathrm{pk,rec,FB}}}{n_{\mathrm{L_r}} A_{\mathrm{c,L_r}}} \stackrel{\text{def}}{=} K_{\mathrm{r}}\, I_{\mathrm{pk,rec,FB}}\,, \tag{D.7}$$

$$B_{\mathrm{pk,L_r,HB}} = \frac{L_{\mathrm{r}}\, I_{\mathrm{pk,rec,HB}}}{n_{\mathrm{L_r}} A_{\mathrm{c,L_r}}} \stackrel{\text{def}}{=} K_{\mathrm{r}}\, I_{\mathrm{pk,rec,HB}}\,, \tag{D.8}$$

The current and flux density expressions in (D.1)-(D.8) can now be utilized to relate the losses in the ICN converter to its full-bridge and half-bridge maximum power levels. Under the conventional burst-mode control, the ICN converter remains turned on for a duty ratio D_{burst}, where D_{burst} is given by:

$$D_{\mathrm{burst}} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT,max,FB}}}. \tag{D.9}$$

Under topology morphing control, the ICN converter operates in the full-bridge and half-bridge rectifier modes for duty ratios D_{FB} and D_{HB}, respectively, as defined in (5.4) and (5.5). The sum of the conduction losses of the inverter transistors $Q_1 - Q_4$ and the ICN capacitors C_{X1} and C_{X2}, and the winding losses of the ICN inductors L_{X1} and L_{X2} under burst-mode control and under topology morphing control can be

expressed in terms of the RMS inverter output currents given in (D.1) and (D.2) and the duty ratios given in (D.9), (5.4) and (5.5), as:

$$P_{\text{cond,inv,X1,X2,b}} = D_{\text{burst}}\, I^2_{\text{rms,inv,FB}}\left(2R_{\text{DS,on,inv}} + R_{\text{LX1}} + R_{\text{CX1}} + R_{\text{LX2}} + R_{\text{CX2}}\right), \tag{D.10}$$

$$P_{\text{cond,inv,X1,X2,m}} = \left(D_{\text{FB}}\, I^2_{\text{rms,inv,FB}} + D_{\text{HB}}\, I^2_{\text{rms,inv,HB}}\right)\left(2R_{\text{DS,on,inv}} + R_{\text{LX1}} + R_{\text{CX1}} + R_{\text{LX2}} + R_{\text{CX2}}\right). \tag{D.11}$$

Here $R_{\text{DS,on,inv}}$ is the on-resistance of the inverter transistors, R_{LX1} and R_{LX2} are the ac resistances of the inductors L_{X1} and L_{X2}, respectively, and R_{CX1} and R_{CX2} are the ESRs of the capacitors C_{X1} and C_{X2}, respectively. The relative reduction in these losses as given in (5.11) can now be obtained using (D.10) and (D.11). Using (D.5) and (D.6), the core losses of the inductors L_{X1} and L_{X2} under burst-mode control and topology morphing control can similarly be expressed in terms of the peak inverter output currents given in (D.1) and (D.2) as:

$$P_{\text{core,L}_{\text{Xp}},\text{b}} = K_{\text{fe}}\, f_{\text{s}}^{\alpha}\, K_{\text{Xp}}^{\beta}\, D_{\text{burst}}\, I^{\beta}_{\text{pk,inv,FB}}, \tag{D.12}$$

$$P_{\text{core,L}_{\text{Xp}},\text{m}} = K_{\text{fe}}\, f_{\text{s}}^{\alpha}\, K_{\text{Xp}}^{\beta}\, \left(D_{\text{FB}}\, I^{\beta}_{\text{pk,inv,FB}} + D_{\text{HB}}\, I^{\beta}_{\text{pk,inv,HB}}\right). \tag{D.13}$$

Equation (5.12) can now be obtained using (D.12) and (D.13). Finally, the loss comparisons given in (5.13) and (5.14) can be obtained in a similar manner by relating the corresponding losses to the RMS and peak rectifier input currents given in (D.3) and (D.4).

As described in Chapter 5, owing to the highly non-sinusoidal nature of the voltage across the transformer windings, the transformer core losses are evaluated using the iGSE. For this purpose, first the voltage across the transformer secondary is evaluated under burst-mode control and under topology morphing control. Under burst-mode control with the resonant capacitor C_{r} on the transformer's primary side (as in the ICN converter of Fig. 5.1), the transformer secondary voltage can be modeled as a square-wave, given by:

$$v_{\text{Txs,burst}}(t) = \begin{cases} V_{\text{OUT}}, 0 \le t < \dfrac{T_{\text{s}}}{2} \\ -V_{\text{OUT}}, \dfrac{T_{\text{s}}}{2} < t \le T_{\text{s}} \end{cases}. \tag{D.14}$$

Here T_s is the converter's switching period. Under topology morphing control with the resonant capacitor $C_{r,DC}$ moved to the transformer's secondary side (as in the ICN converter of Fig. 5.2), the transformer secondary voltage in the full-bridge and half-bridge rectifier modes can be expressed as:

$$v_{Txs,FB}(t) = \begin{cases} V_{OUT} + \frac{I_{pk,rec,FB}}{\omega_s C_{r,DC}} \sin\left(\omega_s t - \frac{\pi}{2}\right), 0 \le t < \frac{T_s}{2} \\ -V_{OUT} + \frac{I_{pk,rec,FB}}{\omega_s C_{r,DC}} \sin\left(\omega_s t - \frac{\pi}{2}\right), \frac{T_s}{2} < t \le T_s \end{cases}, \tag{D.15}$$

$$v_{Txs,HB}(t) = \begin{cases} \frac{V_{OUT}}{2} + \frac{I_{pk,rec,HB}}{\omega_s C_{r,DC}} \sin\left(\omega_s t - \frac{\pi}{2}\right), 0 \le t < \frac{T_s}{2} \\ -\frac{V_{OUT}}{2} + \frac{I_{pk,rec,HB}}{\omega_s C_{r,DC}} \sin\left(\omega_s t - \frac{\pi}{2}\right), \frac{T_s}{2} < t \le T_s \end{cases}. \tag{D.16}$$

Here, ω_s $(= 2\pi f_s)$ is the angular switching frequency of the converter, $C_{r,DC}$ is the capacitance of the resonant/dc-blocking capacitor, and the resonant portion of this capacitor's voltage is modeled as a sine-wave. Using Faraday's law [3], (D.14)-(D.16) can be used to obtain the peak-to-peak value and the instantaneous slope of the flux density in the transformer core under burst-mode and under topology morphing control. The iGSE can then be applied in conjunction with the burst duty ratio defined in (D.9) and the topology morphing duty ratios defined in (5.4) and (5.5) to obtain the transformer core losses under the two control schemes.

Appendix E
Expressions for Efficiency of L-Section Matching Network Stages

This appendix derives expressions for the efficiency of the four types of L-section stages considered in Chapter 8, in the form given in (8.2). The efficiency of an L-section stage can be expressed as:

$$\eta = \frac{P_{out}}{P_{out}+P_{loss,L}+P_{loss,C}}, \tag{E.1}$$

where P_{out} is the output power of the stage, and $P_{loss,L}$ and $P_{loss,C}$ are the losses in the inductor and the capacitor, respectively. As discussed in Section 8.2, losses in capacitors are typically far smaller than those in inductors, that is, $P_{loss,C} \ll P_{loss,L}$. Therefore, capacitor losses can be neglected in comparison to inductor losses, and the efficiency of the L-section stage can be approximated as:

$$\eta \approx \frac{P_{out}}{P_{out}+P_{loss,L}} = \frac{1}{1+\frac{P_{loss,L}}{P_{out}}}. \tag{E.2}$$

In a high-efficiency L-section stage, the losses are significantly smaller than the output power of the stage, that is, $P_{loss,L} \ll P_{out}$. This enables (E.2) to be further approximated as:

$$\eta \approx 1 - \frac{P_{loss,L}}{P_{out}}. \tag{E.3}$$

In the following sections, (E.3) is used to express the efficiency of the L-section stages of Fig. 8.1 in terms of their current gain, G_i, and impedance characteristics, Q_{in} and Q_{load}.

A. L-section stage of Fig. 8.1(a)

The output power of the L-section stage shown in Fig. 8.1(a) is given by $\frac{|\hat{I}_{out}|^2}{2}R_{load}$, and the inductor losses are given by $\frac{|\hat{I}_{in}|^2}{2}R_L$, where R_L is the ac resistance of the inductor, modeling its winding and core losses at the operating frequency. The efficiency of this L-section stage can be expressed as:

$$\eta \approx 1 - \frac{|\hat{I}_{in}|^2 R_L}{|\hat{I}_{out}|^2 R_{load}}. \tag{E.4}$$

Using the definition of the current gain of the stage, $G_i = \frac{|\hat{I}_{out}|}{|\hat{I}_{in}|}$, and the inductor quality factor, $Q_L = \frac{2\pi f_s L}{R_L}$, (E.4) can be alternatively expressed as:

$$\eta \approx 1 - \frac{2\pi f_s L\left(\frac{1}{G_i^2 R_{load}}\right)}{Q_L}. \tag{E.5}$$

Finally, using the expression for the inductance L of the L-section stage of Fig. 8.1(a) given in Table 8.1, the efficiency of this L-section stage can be expressed in the following form:

$$\eta \approx 1 - \frac{\left(\frac{1}{G_i}\sqrt{(1-G_i^2)+Q_{load}^2}+Q_{in}\right)}{Q_L}. \tag{E.6}$$

The expression inside the parenthesis in (E.6) is defined as the effective transformation factor Q_{eff} of the L-section stage of Fig. 8.1(a).

B. L-section stage of Fig. 8.1(b)

The output power of the L-section stage of Fig. 8.1(b) is given by $\frac{|\hat{I}_{out}|^2}{2} R_{load}$, and the inductor losses can be expressed as $\frac{|\hat{I}_{in}-\hat{I}_{out}|^2}{2} R_L$. The efficiency of the L-section stage of Fig. 8.1(b) is then given by:

$$\eta \approx 1 - \frac{|\hat{I}_{in}-\hat{I}_{out}|^2 R_L}{|\hat{I}_{out}|^2 R_{load}}. \tag{E.7}$$

The input current of the stage $\hat{I}_{in}$ can be expressed in terms of the output current $\hat{I}_{out}$ as:

$$\hat{I}_{in} = \frac{R_{load}+j(X_L+X_{load})}{jX_L}\hat{I}_{out}. \tag{E.8}$$

Using (E.8) and replacing the inductor reactance X_L with $2\pi f_s L$, the efficiency expression in (E.7) can be simplified to:

$$\eta \approx 1 - \frac{\frac{1}{2\pi f_s L}\left(\frac{R_{load}^2+X_{load}^2}{R_{load}}\right)}{Q_L}. \tag{E.9}$$

The inductance L in (E.9) can now be replaced with the inductance expression for the L-section stage of Fig. 8.1(b) given in Table 8.1, and the resultant efficiency expression is given by:

$$\eta \approx 1 - \frac{\left(\frac{1}{G_i}\sqrt{(1-G_i^2)+Q_{load}^2}-Q_{load}\right)}{Q_L}. \tag{E.10}$$

The parenthesized expression in (E.10) represents the effective transformation factor Q_{eff} of the L-section stage of Fig. 8.1(b).

C. L-section stage of Fig. 8.1(c)

The output power of the L-section stage of Fig. 8.1(c) is given by $\frac{|\hat{I}_{out}|^2}{2}R_{load}$, and the inductor losses can be expressed as $\frac{|\hat{I}_{out}|^2}{2}R_L$. Using (E.3), the efficiency of the L-section stage of Fig. 8.1(c) is then given by:

$$\eta \approx 1 - \frac{R_L}{R_{load}}. \tag{E.11}$$

Expressing the inductor ac resistance R_L as $\frac{2\pi f_s L}{Q_L}$, the efficiency expression in (E.11) can be rewritten as:

$$\eta \approx 1 - \frac{2\pi f_s L\left(\frac{1}{R_{load}}\right)}{Q_L}. \tag{E.12}$$

The expression for the inductance L of the L-section of Fig. 8.1(c) given in Table 8.1 can now to be utilized to convert (E.12) to the following form:

$$\eta \approx 1 - \frac{\left(G_i\sqrt{\left(1-\frac{1}{G_i^2}\right)+Q_{in}^2}-Q_{load}\right)}{Q_L}. \tag{E.13}$$

The expression under the parenthesis in (E.13) is defined as the effective transformation factor Q_{eff} of the L-section stage of Fig. 8.1(c).

D. L-section stage of Fig. 8.1(d)

The derivation of the efficiency expression for the L-section stage of Fig. 8.1(d) proceeds identically as in sections A, B and C above. First, the output power of the L-section stage is expressed as $\frac{|\hat{I}_{out}|^2}{2}R_{load}$, and the inductor losses as $\frac{|\hat{I}_{in}-\hat{I}_{out}|^2}{2}R_L$. This results in the following expression for the efficiency of this L-section stage:

$$\eta \approx 1 - \frac{|\hat{I}_{in} - \hat{I}_{out}|^2 R_L}{|\hat{I}_{out}|^2 R_{load}}. \tag{E.14}$$

The input current of the L-section stage, $\hat{I}_{in}$, can be expressed in terms of its output current $\hat{I}_{out}$ as:

$$\hat{I}_{in} = \frac{R_{load} + j(X_L + X_C + X_{load})}{jX_L} \hat{I}_{out}. \tag{E.15}$$

Expressing the inductor and capacitor reactances as $2\pi f_s L$ and $-\frac{1}{2\pi f_s C}$, respectively, and utilizing the relationship given in (E.15), the efficiency expression in (E.14) can be alternatively written as:

$$\eta \approx 1 - \frac{\frac{1}{2\pi f_s L}\left(\frac{R_{load}^2 + \left(X_{load} - \frac{1}{2\pi f_s C}\right)^2}{R_{load}}\right)}{Q_L}. \tag{E.16}$$

The inductance L and capacitance C in (E.16) can be replaced with the corresponding expressions for the L-section stage of Fig. 8.1(d) given in Table 8.1, leading to the efficiency of this L-section stage being expressible as:

$$\eta \approx 1 - \frac{\left(G_i \sqrt{\left(1 - \frac{1}{G_i^2}\right) + Q_{in}^2} + Q_{in}\right)}{Q_L}. \tag{E.17}$$

The effective transformation factor Q_{eff} for the L-section stage of Fig. 8.1(d) is given by the parenthesized expression in (E.17).

Appendix F
Expressions for Asymptotic Maximum Efficiency of Multistage L-Section Matching Networks

This appendix derives the expression for the asymptotic maximum efficiency of the multistage matching networks of Fig. 8.2 as given in Table 8.3 of Chapter 8. For the network of Fig. 8.2(a), using the optimal design relationships of (8.8)-(8.10), the sum of the effective transformation factors of the n stages, $\Sigma_{k=1}^{n} Q_{eff,k}$, can be expressed as:

$$\sum_{k=1}^{n} Q_{eff,k} = (n-1)\left(\frac{1}{G_{i,eq}} - G_{i,eq}\right) + \frac{1}{G_{i,tot}^2}\left(\frac{G_{i,eq}^{2n-1}}{1+G_{i,eq}^2}\right). \tag{F.1}$$

As the number of stages n increases, the sum of the effective transformation factors approaches an asymptotic minimum value that can be evaluated using:

$$\lim_{n\to\infty} \sum_{k=1}^{n} Q_{eff,k} = \ell_1 + \ell_2, \tag{F.2}$$

where $\ell_1 = \lim_{n\to\infty} (n-1)\left(\frac{1}{G_{i,eq}} - G_{i,eq}\right)$ and $\ell_2 = \lim_{n\to\infty} \frac{1}{G_{i,tot}^2}\left(\frac{G_{i,eq}^{2n-1}}{1+G_{i,eq}^2}\right)$. Taking the natural logarithm of both sides of (8.9) and using the resulting expression for $n-1$, the limit ℓ_1 can be expressed as:

$$\ell_1 = \lim_{n\to\infty} \frac{1-G_{i,eq}^2}{2G_{i,eq}\ln(G_{i,eq})}\left(\ln\left(G_{i,tot}\frac{1+G_{i,eq}^2}{G_{i,eq}}\right) + \frac{\ln\left(G_{i,eq}^{2(n-1)} - G_{i,tot}^2\right)}{2}\right). \tag{F.3}$$

As the number of stages n increases, the optimal equal current gain $G_{i,eq}$ approaches 1. Using this property, ℓ_1 is further simplified to:

$$\ell_1 = \lim_{n\to\infty}\left(-\ln(2G_{i,tot}) - \frac{\ln\left(G_{i,eq}^{2(n-1)} - G_{i,tot}^2\right)}{2}\right). \tag{F.4}$$

Solving (8.9) as a quadratic equation in $G_{i,eq}^{n-1}$, it can be shown that:

$$\lim_{n\to\infty} G_{i,eq}^{n-1} = \sqrt{2}G_{i,tot}. \tag{F.5}$$

The limit in (F.4) can now be evaluated using (F.5), reducing ℓ_1 to the following expression:

$$\ell_1 = -\ln\left(2G_{i,tot}^2\right). \tag{F.6}$$

The limit ℓ_2 in (F.2) can be evaluated by solving (8.9) for $G_{i,tot}$, which results in the following relationship:

$$G_{i,tot} = G_{i,eq}^{n-1}\sqrt{\frac{1+\sqrt{1-\left(\frac{2G_{i,eq}}{1+G_{i,eq}^2}\right)^2}}{2}}. \tag{F.7}$$

Substituting the right-hand side of (F.7) in the expression for ℓ_2, and applying the property that $G_{i,eq} \to 1$ as $n \to \infty$, it can be shown that:

$$\ell_2 = 1. \tag{F.8}$$

Using the evaluated limits given in (F.6) and (F.8), the asymptotic minimum limit of the sum of the effective transformation factors of the n stages of the multistage matching network is given by:

$$\lim_{n\to\infty}\sum_{k=1}^{n} Q_{eff,k} = 1 - \ln\left(2G_{i,tot}^2\right) \tag{F.9}$$

This expression can be used to determine the asymptotic maximum efficiency of the multistage network of Fig. 8.2(a), which is then given by:

$$\eta_{max} = \lim_{n\to\infty}\eta_{multistage,opt} = 1 - \frac{1-\ln\left(2G_{i,tot}^2\right)}{Q_L}. \tag{F.10}$$

The procedure outlined above is applicable to the other multistage networks of Fig. 8.2 as well. For the network of Fig. 8.2(b), the asymptotic maximum efficiency has the same expression as that given by (F.10). Finally, for the networks of Fig. 8.2(c) and 8.2(d), the asymptotic maximum efficiency comes out to be:

$$\eta_{max} = \lim_{n\to\infty}\eta_{multistage,opt} = 1 - \frac{1+\ln\left(\frac{G_{i,tot}^2}{2}\right)}{Q_L}. \tag{F.11}$$

Appendix G
Reasoning behind Single-Stage L-Section Networks being Most Efficient for Certain Ranges of Gain

This appendix provides the reasoning behind the conclusion presented in Chapter 8 that for a certain range of total current gains $G_{i,tot}$, a single-stage network is the optimal choice under the proposed design approach. Consider the multistage network of Fig. 8.2(a), in which for total current gains greater than $\frac{1}{\sqrt{2}}$, the optimal current gains of the first $n-1$ stages are equal to 1 (as given in (8.15)). Hence, utilizing (8.1a) and (8.1b), the inductance and capacitance values of these stages simplify to:

$$L_k \big|_{G_i=1} = \frac{1}{2\pi f_s}\left(Q_{in,k} + Q_{load,k}\right)R_{load,k}, \tag{G.1}$$

$$C_k \big|_{G_i=1} = \frac{1}{2\pi f_s}\frac{2Q_{load,k}}{\left(1+Q_{load,k}^2\right)R_{load,k}}. \tag{G.2}$$

It is evident from (G.2) that for the first $n-1$ stages to have non-negative capacitance, their load impedance characteristics must also be non-negative, that is:

$$Q_{load,k} \geq 0 \;\forall\; k \in \{1, 2, \dots, n-1\}. \tag{G.3}$$

This property can now be utilized to demonstrate the optimal design for the first $n-1$ stages. Under the condition that the first $n-1$ stages provide current gains of 1, the sum of the effective transformation factors of the multistage network of Fig. 8.2(a) can be expressed as (see Table 8.2):

$$\sum_{k=1}^{n} Q_{eff,k} = 2\left(Q_{load,1} + Q_{load,2} + \cdots + Q_{load,n-1}\right) + \frac{1}{G_{i,tot}}\sqrt{1 - G_{i,tot}^2}. \tag{G.4}$$

Since the last term on the right-hand side of (G.4) is a fixed positive quantity, the sum of the effective transformation factors will be minimized, and efficiency maximized, when the sum of the load impedance characteristics of the first $n-1$ stages, $\left(Q_{load,1} + Q_{load,2} + \cdots + Q_{load,n-1}\right)$, is minimized. Since the load impedance characteristic of each of the first $n-1$ stages is non-negative (see (G.3)), this sum is

minimized when each load impedance characteristic is zero. Given that the load impedance characteristic of each stage equals the input impedance characteristic of the following stage (that is, $Q_{load,k} = Q_{in,k+1}$), it can be concluded using (G.1) and (G.2) that the first $n-1$ stages of this multistage network have inductance and capacitance values of zero. This eliminates the first $n-1$ stages, and the remaining single-stage network is the optimal design. A similar approach can be used to show that for an optimal design, the other multistage networks of Fig. 8.2 also collapse to single-stage networks for certain ranges of total current gain.