# Efficient Nanoscale Photonic Devices and Monolithic Electronic-Photonic Subsystems in Sub-100 nm SOI CMOS

(Invited Paper)

Fabio Pavanello[1], Mark T. Wade[1], Jelena Notaros[1], Jeffrey M. Shainline[1], Christopher V. Poulton[1], Chen Sun[2], Michael Georgas[2], Luca Alloatti[3], Amir Atabaki[3], Rajesh Kumar[1], Ben Moss[2], Sen Lin[2], Rajeev J. Ram[3], Vladimir Stojanović[2] and Miloš A. Popović[1]

[1]Department of Electrical, Computer, and Energy Engineering, University of Colorado Boulder, Boulder, CO 80309, USA
[2]Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720, USA
[3]Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA 02139, USA

***Abstract*—We demonstrate efficient photonic devices that rely on sub-100nm features in unmodified 45nm SOI CMOS, including photonic crystals, array-antenna grating couplers, and modulators. We then show monolithically integrated electronic-photonic systems comprising millions of transistors and thousands of photonic devices, including a complete chip-to-chip photonic link.**

## I. Introduction

Integration of photonics and electronics by taking advantage of *unmodified* CMOS platforms is widely regarded as one of the most viable approaches to solve the bottle-neck of current processor-to-memory communications [1]. Advanced CMOS platforms allow for high yield, high resolution due to state-of-the-art deep UV lithography [2], and a high-level of complexity (e.g. large number of dopants masks and metal layers with high resolution) due to the ever-growing requirements of interconnects communication, while at the same time leveraged fabrication costs due to high volume production. Clearly, these platforms represent the best candidate for tight integration of circuits and photonic devices [3]. However, it is less clear if high-efficient photonic devices can be realized with similar or superior performance compared to conventional silicon platforms due to constraints typical of CMOS processes e.g. minimum metal densities and area enclosure.

Here, we review our recent work on enabling high-efficiency devices in a native sub-100 nm commercial CMOS platform (IBM 12SOI 45 nm node) by presenting key photonic devices such as high tuning efficiency and low insertion loss (IL) photonic crystals (Ph.Cs) [4], [5], array nanoantenna grating couplers enabling sub-1 dB fiber-to-chip IL over large bandwidth (BW) [6], [7] and energy efficient spoked-ring cavity optical modulators [8], [9]. Finally, we will present an example of their integration in a monolithic transmitter with a full digital back end down to a record 20 fJ/bit wall-plug energy efficiency [10] (not including laser power); and a complete communication link [11].

## II. Photonic Crystal Cavities

Fig. 1 shows an example of designed Ph.C cavities. The main challenge of realizing Ph.Cs in such a process relies on the need of achieving sub-wavelength patterns without violating design rules such as minimum feature size and minimum enclosed area. This aspect leads to different design strategies depending on the operating wavelength. Nonetheless, intrinsic

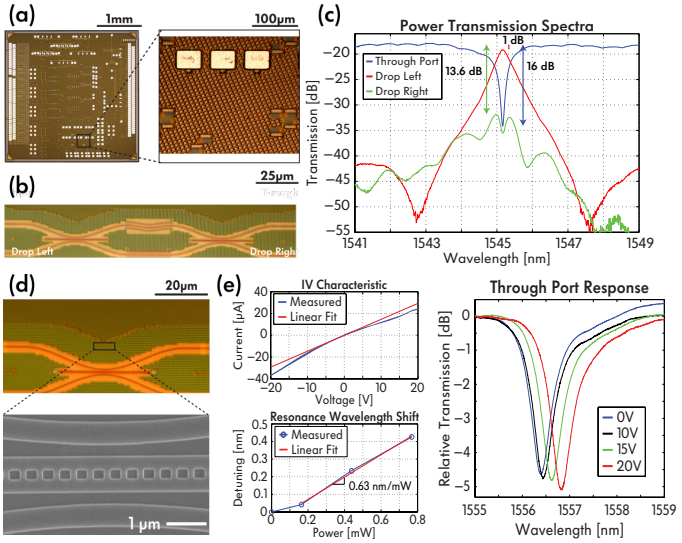


Fig. 1. Efficient PhCs in 45 nm CMOS (a) optical micrograph of a photonic chip with grating openings in the metal fill and respective electrical pads; (b) cascaded Ph.C cavities operating in push-pull configuration to enable the separation of the through and drop ports; (c) filter spectrum with IL = 1 dB; (d) design of a thermally tunable Ph.C with squared pattern holes; (e) electrical and optical characteristics showing a tuning efficiency of 13 $\mu$W/GHz [4], [5].

quality factor $Q$ as high as 100k (not reported here) and IL as low as 1dB for add-drop filters such as in Fig. 1(b) can be achieved (see Fig. 1(c)). Moreover, the addition of blanket dopings for single Ph.C cavities (Fig. 1(d)) enables high-efficiency 13 $\mu$W/GHz thermal tuning as reported in Fig. 1(e). The reason why the required voltage is considerably large is related to the low mid-level n-type doping concentration.

## III. Array Nano-antenna Grating Couplers

Fig. 2 shows our grating coupler design. One of the main requirements of grating based fiber-to-chip coupling is to achieve high directivity. Metallic or dielectric stack mirrors, not feasible in advanced CMOS processes and not easily integrable even in custom photonics processes, are sometimes employed to achieve the goal. Our approach is to realize the entire coupler function in the (two) device layers [12]. Here, it is adapted to CMOS whereby we use two lithographic layers to build an array antenna grating whose single "element" is comprised of two scatterers and has an unidirectional radiation

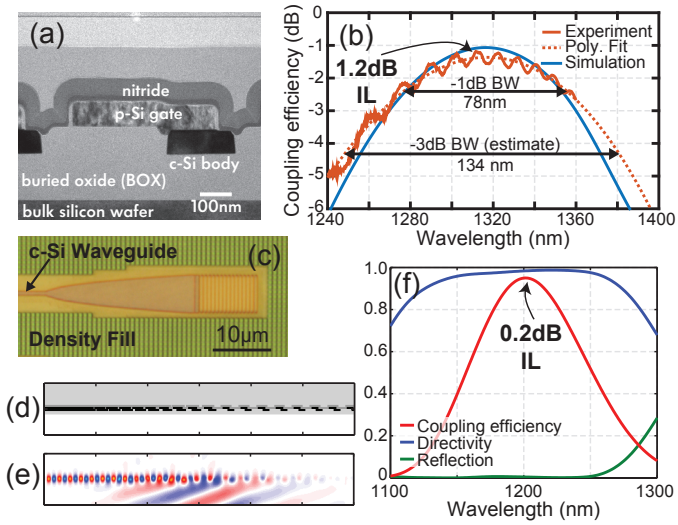


Fig. 2. Efficient grating couplers in 45 nm CMOS (a) TEM of a unit cell of the *periodic* Gen2 "array nanoantenna" design using poly-Si and body-Si blocks to provide unidirectional emission [top-view micrograph in (c)]; (b) experimental data showing IL = 1.2 dB and 1-dB BW = 78 nm [6]; (d) more advanced, tapered (Gen3) design [7] achieves both Gaussian beam forming and unidirectional emission and shows 0.2-0.3 dB loss in simulation.

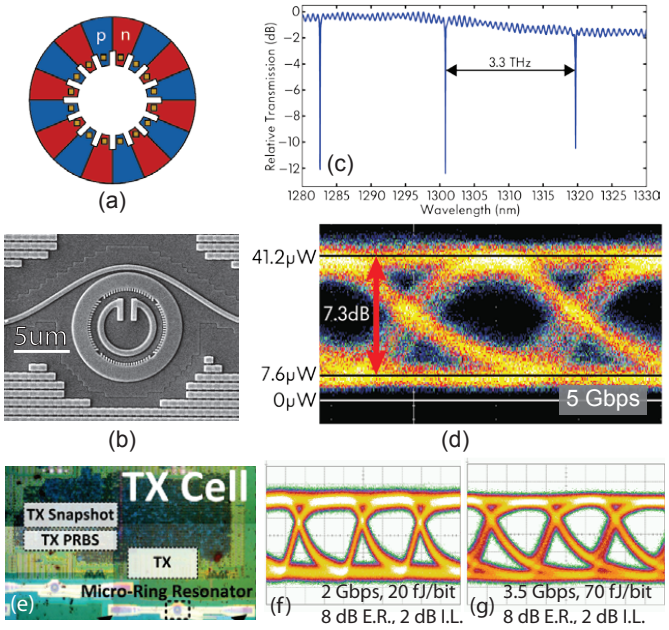


Fig. 3. Modulator [8], [15] and monolithic transmitter [10], [11]: (a) spoked-ring interdigitated p-n junction cavity concept enables depletion modulation in CMOS; (b) SEM image; (c) transmission spectrum; (d) eye diagram at 5 Gbps; (e) micrograph of monolithic transmitter including modulator and driver on chip; (f) eye diagrams showing ultra-low wallplug energy per bit.

pattern. In SOI CMOS, we can accomplish this using the two independently patternable silicon layers – the transistor body crystalline silicon layer, and the gate polysilicon layer. Fig. 2(a–c) shows a second generation design with a uniform periodicity, demonstrating experimentally IL = 1.2 dB, matching the design simulations, and a 1 dB BW $\approx$ 78 nm in the O band [6]. Tapering of the structure such that the four unit cell parameters vary radiation strength, while preserving unidirectionality and output angle, greatly improves the overlap with the fiber Gaussian mode leading to an even lower IL. A rigorous synthesis method based on a complex-momentum photonic band structure solver is used for the design [7]. IL as low as 0.2 dB was demonstrated in simulation [7] and process manufacturability limits it to 0.3 dB. Experimental characterization of these designs is as yet forthcoming.

## IV. Spoked Ring, Lateral Junction Modulators and Monolithic Transmitters

One of the key photonic components to enable an efficient optical transmitter is the optical modulator. Optical resonators can form energy efficient modulators, and have been typically realized with lateral junctions using ridge waveguides [13], or vertical junctions in a disk cavity [14]. However, both these structures cannot be realized in advanced sub-100 nm CMOS processes.

To accommodate sub-100 nm SOI CMOS platforms, we proposed the spoked-ring modulator structure [8], [9], a full-etch, hybrid ring-disk cavity with radially extending interdigitated lateral junctions, realized in the transistor body silicon device layer and using well implants to form $p$-$n$ junctions. Both implant polarities are electrically contacted along the inner radius of the resonator with sub-wavelength spokes (120 nm wide), while the outer radius provides whispering gallery confinement to the optical mode. Fig. 3(a–d) shows the concept, 3D rendering of the mask design, and an eye diagram of the device in operation. The first devices demonstrated 5 Gbps modulation [8] at as low as 5 fJ/bit estimated energy [15] with $\pm$0.6 V drive. Further improvements are expected in both speed and energy. Fig. 3(d,e) shows an integrated optical transmitter comprising a spoked-ring modulator alongside its electronic driver. The transmitter was demonstrated at speeds up to $\sim$8 Gbps, with measured wallplug energy as low as 20 fJ/bit at 2 Gbps [10] and 30 fJ/bit at 5 Gbps [11]. Further, complex thermal dynamics of the ring modulator was compensated with on-chip electronics, and a complete 5 Gbps chip-to-chip link demonstrated [11].

These results demonstrate that efficient photonic devices can be realized in advanced CMOS platforms and that the tight integration with electronics leads to efficient low energy per bit consumption subsystems.

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