Modeling and Control of a Modular Battery Management System for Lithium-Ion Battery Packs

by

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Modeling and Control of a Modular Battery Management System for Lithium-Ion Battery Packs

Thesis directed by Prof. Dragan Maksimović

High voltage (HV) traction battery packs in electric-drive vehicles (HEV, PHEV, BEV) consist of a large number of battery cells connected in series. As individual cells exhibit mismatches in characteristics such as capacity, inner resistance, and run-time state-of-charge (SOC), cell balancing must be incorporated into the battery management system (BMS). Conventional passive cell balancing does not fully address the mismatch issues, which leads to shorter battery lifetime, and the need to over-size the battery pack. To overcome the problems associated with the conventional architecture, a modular battery management system incorporating both active cell balancing and high voltage (HV) to low-voltage (LV) dc-dc conversion has been developed. The HV-to-LV converter is a series-input, parallel-output dc-dc system with inputs connected across the battery cells or cell modules, while paralleled outputs supply loads on the LV bus. This thesis is focused on modeling, control and design of the modular battery management system. Several critical issues are addressed: (1) stability of the converter system with distributed control in energy storage application is analyzed and simulated; (2) the steady-state model of the dual-active-bridge (DAB) isolated converter with phase-shift modulation is refined and applied to the modular converter system with cell balancing; (3) practical methods for estimation of the Lithium-ion battery state-of-charge (SOC) and state-of-health (SOH) are developed in forms suitable for implementation on low-cost microcontrollers. Finally, a modular hybrid balancing system with module-level active balancing and cell-level passive balancing is developed and experimentally validated. The techniques developed in this thesis can be applied to designs of large automotive battery packs with improved performance, reduced size, reduced cost, and longer lifetime.

Dedication

To my parents, and Shanshan, and Robin

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Chapter 1

Overview of Lithium-Ion Battery Packs and Battery Management Systems

Along with increasing demand and rapid development of clean energy worldwide, mid- to large-scale energy storage systems based on battery cells is becoming a key technology. One of the most important applications for large battery packs is in electric drive vehicles: hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), and electric vehicles (EV) or, more generally, xEV's. In recent years, the more electrified drivetrain trend has been accelerating. In addition to emerging EV companies, existing automotive manufacturers are incresaingly offering various xEV's. From year 2012 to year 2016, the number of electric drive vehicles sold in the U.S. nearly doubled [11].

Among technologies in electric drive vehicles, the design of a safe and compact traction battery pack with sufficient energy storage is critical. A traction battery pack typically provides dc voltage at hundreds of volts and power at tens to hundreds of kilowatts to the vehicle drivetrain. To meet the voltage and power specifications, a large number of battery cells are connected in parallel and in series. However, the cells in a battery pack exhibit mismatches in parameters, and dealing with the cell mismatch is a challenging issue in large battery pack.

This chapter gives an overview of the battery management systems (BMS) for large battery packs. In Section 1.1, the effect of cell mismatch and the necessity of balancing is discussed. In Section 1.2, typical battery balancing methods, including passive and active balancing, are reviewed. In Section 1.3, novel active balancing BMS incorporating other xEV functions are introduced. The focus and organization of the dissertation are given in Section 1.4.

1.1 Effect of Cell Mismatch in Large Battery Packs

A large battery pack is shown in Fig. 1.1. Individual battery cells are limited in voltage rating. The terminal voltage of a battery cell depends on cell chemistry, and is only in the order of 3-4 V for lithium-ion cells commonly used in xEV battery packs. As a result, a large number of cells should be stacked in series to achieve high battery pack output voltage. An individual battery cell is also limited in current rating, usually expressed in the cell's C rate. The C rate is the ratio of the cell current expressed in amperes and the cell total capacity value expressed in amp-hours. Several cells may be connected in parallel to achieve high battery pack output current. Unlike series connection, parallel connection is relatively immune to cell mismatch. A combination of paralleled cells is considered a super cell [63,64]. As the parallel connection does not make much difference in balancing, both a physical cell and a super cell are referred to as a cell in this work.

State-of-charge (SOC) is used to evaluate the level of remaining charge left in a battery cell or a battery pack, and is defined in Eq. (1.1). For example, $SOC = 100\,\%$ represents the case when the battery is fully charged and the remaining charge of the battery equals to the battery total capacity. $SOC = 0\,\%$ represents the case when the battery is fully discharged and the remaining charge is zero.

$$SOC = \frac{Current\ charge}{Total\ capacity:\ Q_{tot}} \tag{1.1}$$

Ideally, all the cells in a battery pack are identical. Charging or discharging the battery pack results in simultaneously charging or discharging of individual cells, so that the pack SOC and all the cell SOC's are ideally identical. However, practical cells exhibit mismatches in characteristics such as capacity, inner resistance, and self-discharing rate. The mismatches cause slow divergence in cell SOCs. The difference in SOC decreases the performance of the

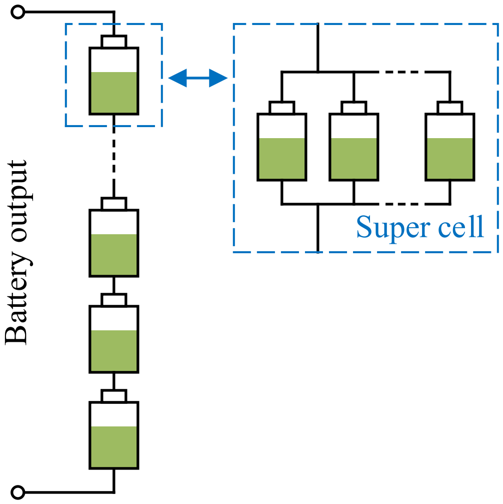
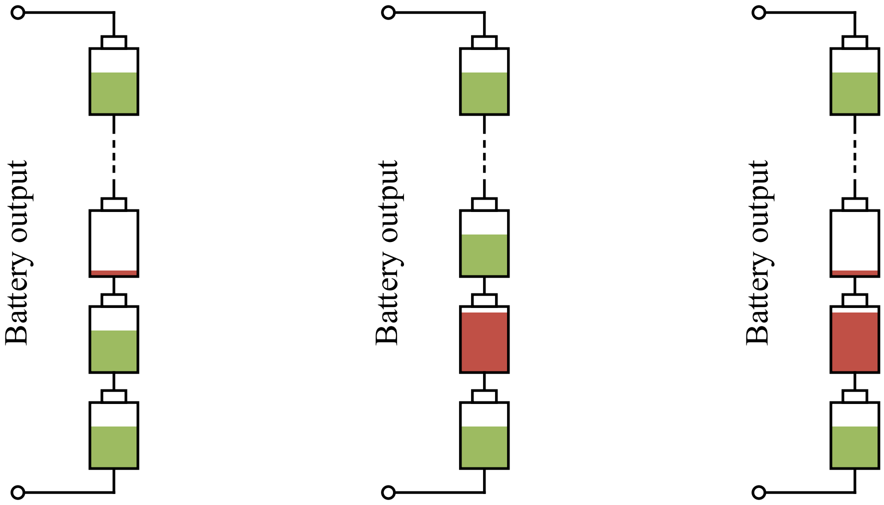


Figure 1.1: Large battery pack that consists of a large number of lithium-ion cells.



(a) (b) (c)

Figure 1.2: Scenarios in which the battery pack is (a) unable to be discharged; (b) unable to be charged; (c) unable to be either charged or discharged.

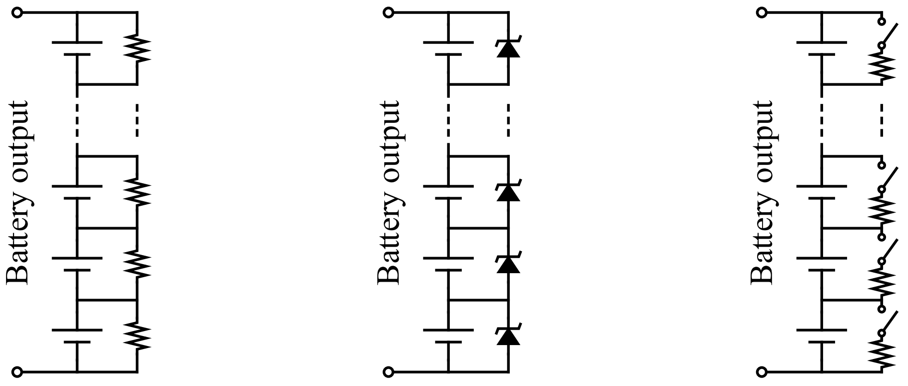
entire battery pack [49]. To understand the problem, three scenarios are examined. In all the scenarios, it is assumed that all the cells have identical total capacity, the SOC difference is caused by different self-discharging rate and leaking current. In the first scenario, shown in

Fig. 1.2 (a), the remaining charge of the entire battery string is limited by the cell with the lowest SOC. When any cell reaches 0 % SOC, the battery pack cannot be further discharged, even if there are plenty of remaining charges in the other cells. In the second scenario, shown in Fig. 1.2 (b), the battery charging process is limited by the cell with the highest SOC. When any cell reaches 100 % SOC, the entire battery pack cannot be further charged. In the extreme scenario shown in Fig. 1.2 (c), including both fully charged and discharged cells, the battery pack cannot be charged or discharged, i.e., cannot be cycled any further.

For lithium-ion batteries [47, 84], neither overcharge or overdischarge are acceptable. Violations of safety limits may not only cause irreversible capacity and power fade, but also lead to dangerous accidents such as catching fire or leaking toxic materials. As a result, simple balancing techniques used in lead-acid and nickel based batteries, known as extend charging, cannot be adopted for use with the lithium-ion chemistry. Additional circuits are necessary to achieve balancing in lithium-ion battery packs. Several balancing strategies are briefly reviewed in the next section.

1.2 Conventional Cell Balancing Techniques

Battery balancing using additional circuits are typically categorized into two classes: passive balancing and active balancing. Passive balancing is a dissipative process. If any cell in the battery string develops more stored electrical charge than the other cells, the excessive charge will be dumped and converted to heat. On the other hand, active balancing is recognized as a non-dissipative process. Rather than simply converting electricity to heat, the extra charge in a 'stronger' cell is transferred to a 'weaker' cell. As no electrical energy is wasted, active balancing is considered more advanced than passive balancing. However, the circuits for active balancing are usually more complicated due to the need for electrical power conversion, which in practice adds extra cost, size, and weight to the battery pack. Nowadays, passive balancing is still the most popular lithium-ion battery balancing strategy. Battery management systems (BMS) with passive balancing is widely commercialized and



(a) (b) (c)

Figure 1.3: Passive balancing with (a) shunt resistor connected all the time; (b) Zener diode; (c) shunt resistor controlled by switch.

used in electric vehicles, and many other applications with large battery packs.

Several classical passive and active balancing methods are reviewed next.

1.2.1 Passive Balancing

A very simple passive balancing method is shown in Fig. 1.3 (a), with a shunt resistor directly connected in parallel with the battery cell. As the terminal voltage of most battery cells changes monotonically with its SOC, the cell with higher SOC also has a higher terminal voltage, and naturally discharges faster than the cell with a lower SOC. However the discharging process is not controllable. The cells will keep dumping energy even if balanced or not. A low charging current is necessary to maintain the charge of the battery pack at all times.

A Zener diode could be used as an alternative to the resistor, as shown in Fig. 1.3 (b). The terminal voltage of each cell is limited by the Zener diode voltage in parallel. A major disadvantage of this method is that the balancing process only happens at the end of charging, and current sinking capability of the Zener diode limits the speed of charging.

Better passive balancing is achieved by adopting controllable power dissipation [28,49]. A switch is connected between the battery cell and a shunt resistor, as shown in Fig. 1.3 (c). The switch closes if charge dumping is necessary and opens if not. As a result, less electrical energy is wasted compared to the method in Fig. 1.3 (a), and faster charging is achieved compared with the method in Fig. 1.3 (b). However, performance of a passive balanced battery pack highly depends on the extent of cell parameter differences such as total capacity. With good manufacturing, the total capacity of the cells in a battery pack could be controlled within a narrow range, making the deficiency of passive balancing relatively small at the beginning of battery life. However, as the battery ages, the total capacity fades differently from cell to cell, making passive balancing increasingly wasteful and incapable of balancing cells sufficiently quickly. Moreover, the performance of the entire battery pack remains limited by the weakest cell.

1.2.2 Active Balancing

Due to the drawbacks of passive balancing, active balancing became a topic of interest. One of the very first concepts of active balancing is based on step-up dc-dc converters [25,26,28], as shown in Fig. 1.4 (a). The method significantly improved the battery charge usage and balancing speed. However, a major drawback is the necessity for high-voltage switches in each step-up converter. Another drawback, highlighted by other researchers in 1990s, is the necessity of precise cell monitoring and control. It should be noted that although sensing and control was a concern, it is no longer a barrier today due the great improvements and cost reductions in microelectronics technology. In fact, precise cell monitoring becomes mandatory in mordern xEV battery management systems. The state-of-the-art commercial lithium-ion BMS achieves less than 1 mV sensing error in cell voltage [44].

Another active balancing method without the need of precise cell voltage sensing was proposed and developed in [38–41,73]. Fundamentally, a multi-winding coaxial transformer is adopted to achieve voltage matching of the battery cells. A flyback converter with multi-

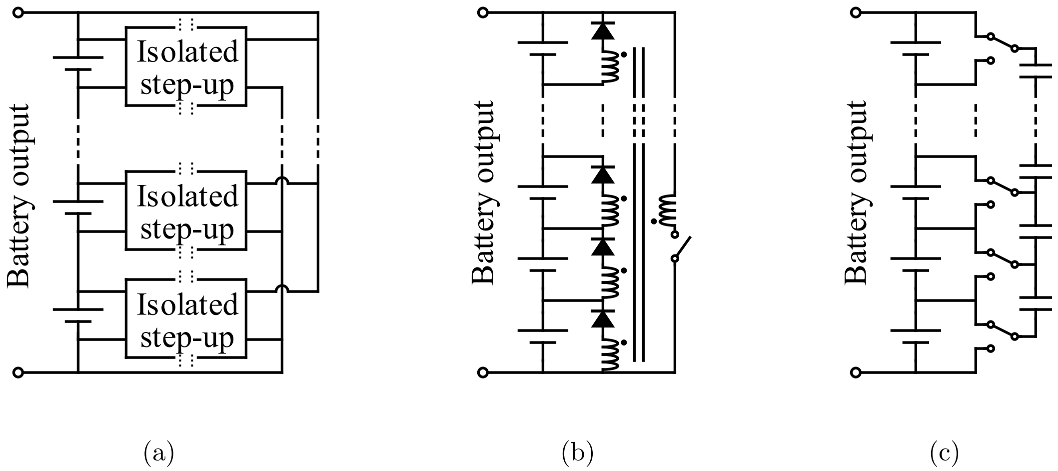


Figure 1.4: Active balancing with (a) step-up converter; (b) multi-winding transformer; (c) switched capacitor.

winding transformer is shown in Fig. 1.4 (b). Apparently, the multi-winding transformer may cause significant assembly difficulties, and thus becomes less practical especially in large batteries. In addition, a new transformer has to be designed whenever there is a change in battery cell quantity. More importantly, most BMSs today require more advanced SOC balancing rather than simple voltage balancing, the control scheme in 1.4 (b) actually becomes a drawback.

Switched capacitor based active balancing system was proposed and developed in [35, 56]. The architecture is shown in Fig. 1.4 (c). Going along the path of voltage balancing, neither sensing or closed-loop control, nor bulky magnetic devices are required. In addition, the architecture is able to be quickly adapted to different battery size and chemistry, leveraging from the concept of modular design. However, a significant disadvantage is the limitation in balancing speed. Charge has to be transferred through adjacent battery cells. The performance of the system is predominantly decided by how close the imbalanced cells are located in the battery string.

Motivated by the potential advantages of active balancing, many approaches have been investigated over the past few decades [5, 10, 20, 42, 51, 55, 85]. Benefits and drawbacks have been claimed in different applications and aspects. For example, [5] proposed a double-tied switch capacitor system to improve the balancing speed, but at the cost of using more capacitors. Reference [51] proposed a converter based cell-to-cell balancing in which a buck-boost converter connects adjacent cells with soft-switching, however the balancing speed is still limited due to the necessity of shuttling charge through adjacent cells. Although these methods achieve better balancing performance, none of them have demonstrated significant practical advantages over passive balancing.

Before going deeper into the research of better active balancing methods, the critical features of a practical BMS in xEV applications are summarized:

1. Accurate battery cell voltage (and current) monitoring is always mandatory to guarantee safe operation. Although many works claim that cell voltage measurement is not necessary in their balancing schemes, the elimination of cell voltage sensing has rarely been adopted or demonstrated in any practical lithium-ion battery system.

2. Accurate online SOC and SOH estimation becomes more and more important, motivated by potentials of prolonging battery lifetime. It should be noted that accurate SOC and SOH estimation also greatly depends on the cell voltage monitoring mentioned above.

3. In addition to SOC and SOH estimation, balancing speed is also playing an important role in prolonging battery life [69].

4. Various 'modular' concepts have received increasing attention. The BMS architecture should be quickly adapted to different battery size, chemistry, and balancing algorithms, without the need to re-designing hardware.

5. To demonstrate practical advantage over passive balancing, the additional cost, size, and weight associated with active balancing must be considered.

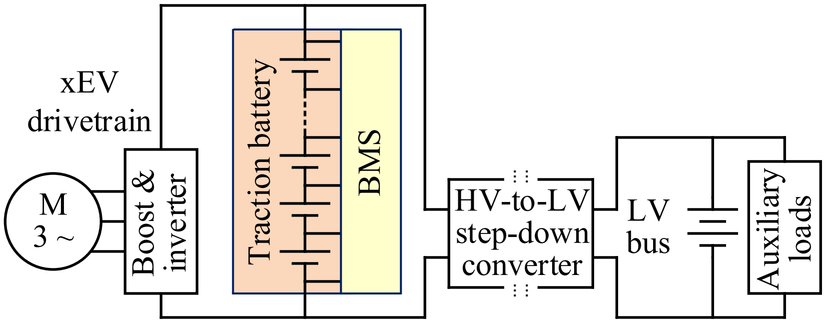


Figure 1.5: Conventional xEV battery and BMS architecture.

1.3 Novel Modular Active Balancing BMS

With the key points summarized above taken into consideration, it is found that novel active-balancing approaches could pursued at the system level, by incorporating other xEV functions in combination with BMS functions.

The conventional xEV power supply architecture shown in Fig. 1.5 is examined first. An xEV has two groups of loads. The primary load is the xEV drivetrain, which is directly connected to the battery high-voltage output. The traction battery provides energy in propulsion and absorbs energy during regenerative braking. In addition to the drivetrain, the vehicle also contains a variety of auxiliary loads, such as lighting, air-conditioning, and the vehicle controllers, and other systems. These loads require much lower voltage and are typically connected to a vehicle low-voltage (LV) bus — commonly rated at 12 V nominal. In a conventional internal combustion engine (ICE) vehicle, the main power for the LV bus comes from an alternator, which transfers energy from the engine. In addition, an automotive lead-acid battery is also tied to the LV bus to stabilize the voltage and provide engine start-up power. In xEV, however, the alternator is replaced by an HV-to-LV step-down dc-dc converter. The step-down converter transfers energy from the large traction battery to the LV bus. In an xEV, the need of an automotive battery is also debatable, as the traction

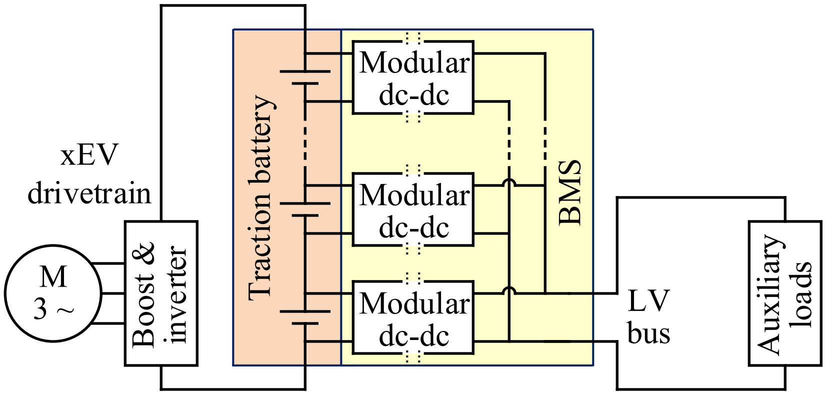


Figure 1.6: Modular BMS incorporating xEV LV bus voltage regulation.

battery already serves as an energy storage device. If the bandwidth of the HV-to-LV step-down converter is high enough to damp load transient on the LV bus, the automotive LV battery may be considered redundant.

A modular BMS incorporating xEV LV bus regulation was first proposed in [13]. The system is shown in Fig. 1.6. Each cell in the traction battery string is connected to an isolated low-power LV-to-LV modular converter, and the outputs of the modular converters are connected to the LV bus. The series-input-parallel-output converter system not only processes differential power for cell-level active balancing, but also supplies xEV auxiliary loads and performs fast LV bus regulation. As a result, the conventional HV-to-LV step-down converter and automotive battery are replaced by the novel BMS. A significant amount of cost associated with the active balancing BMS is thus alleviated. Follow-up works also report up to 40 % battery lifetime extension for BEV75 [67, 69, 77], which further reduces the battery cost.

Another option consists of designing modular BMS incorporating battery pack output voltage regulation. In many xEV drivetrains, a dc-dc converter is placed between the traction battery and the traction inverter. The dc-dc converter boosts the battery voltage to a higher value to improve the inverter and motor efficiency. In Fig. 1.7, the dc-dc function

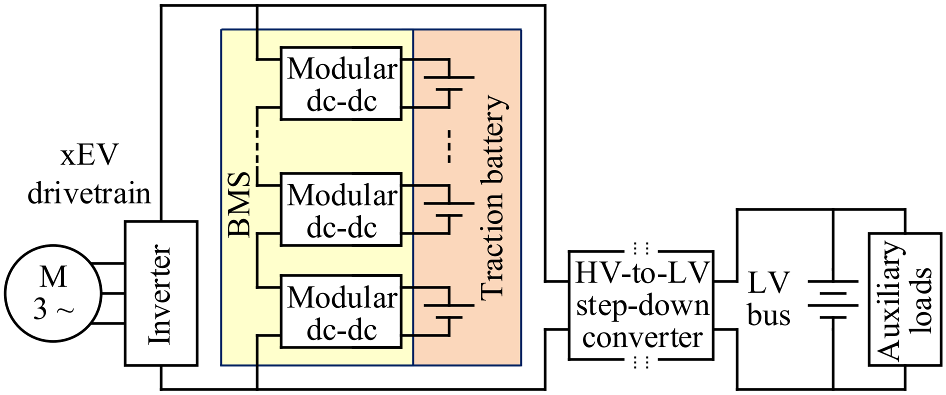


Figure 1.7: Modular BMS incorporating battery pack output voltage regulation.

is achieved by a group of series-output converters. Instead of directly connecting battery cells in series, the battery cells are stacked through modular converters. The series-output converter system combines both active balancing and the boost converter functions in xEV drivetrain. Different from the BMS in Fig. 1.6, the modular converters need to process full powertrain current for xEV cruising, increasing the importance of efficiency and reliability of the modular converters. Some work in this area has been done in [20, 48], however overall system benefits are yet to be fully demonstrated.

1.4 Thesis Objectives and Organization

This dissertation focuses on different aspects of the modular battery management system (BMS) with series-input-parallel-output converter system incorporating both cell-level active balancing and LV bus regulation in electric drive vehicles (xEV). The system architecture is shown in Fig. 1.6. Chapter 2 analyzes the stability of the modular BMS with autonomous converter control. Chapter 3 focuses on the modeling issue of the isolated dual-active-bridge converter used in the system. Chapter 4 develops a 1st-order sigma-point Kalman filter (SPKF) SOC estimation method for lithium-ion battery cells. Chapter 5 evaluates two state-of-the-art online state-of-health (SOH) estimation methods using data from long term aging tests. Chapter 6 extends the research in the direction of further reducing system complexity and cost, focusing on a new hybrid balancing scheme with module-level active balancing and cell-level passive balancing. Chapter 7 summarizes the contributions of the thesis, and gives a brief overview of some potential future directions.

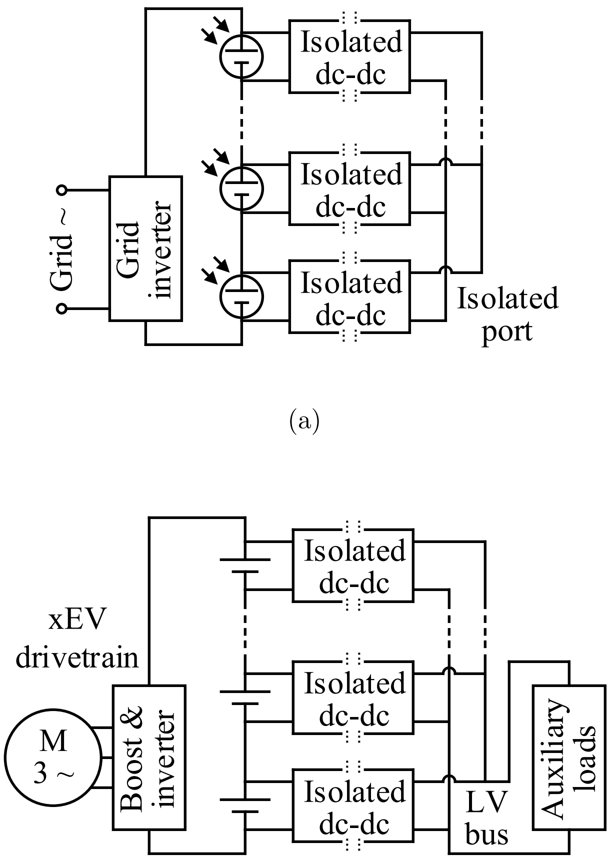
The work and the results reported in this thesis contributed to a multi-disciplinary project focused on robust cell-level modeling and control of large battery packs. Sponsored by ARPA-E AMPED program, the project was a collaboration between Utah State University (USU), University of Colorado Boulder (CU Boulder), University of Colorado Colorado Spring (UCCS), National Renewable Energy Lab (NREL), and Ford Motor Company. The results of this thesis were included in modeling, control, design and implementation of a large prototype battery pack based on modifications of a commercial PHEV battery with eighty-four lithium-ion cells in series. The modular active balancing BMS was applied to a half pack with forty-two cells, while conventional passive balancing was applied to the other half pack for comparison. The modular active balancing BMS demonstrated potentials for significant improvements in battery lifetime, verified by a 15-month cycling and aging test performed at NREL. The prototype also demonstrated potentials for cost and size reduction achieved by elimination of a separate high-voltage-to-low-voltage (HV-to-LV) step-down converter in the conventional xEV architecture.

Chapter 2

Stability of the Modular BMS with Distributed Control of the Series-Input-Parallel-Output Converter System

A modular active balancing BMS incorporating vehicle low votage (LV) bus has been proposed in [13]. The system adopts a series-input-parallel-output converter architecture, shown in 1.6. In the system, each cell in the battery string is connected to the vehicle LV bus through a modular isolated dc-dc converter. The converters not only perform cell-level active balancing, but also supply power to the auxiliary loads on the vehicle LV bus. High speed balancing is achieved as energy is directly transferred among the target cells, without the need of shuttling through adjacent cells. Different from the BMS using step-up converters in Fig. 1.4 (a), the modular BMS in Fig. 1.6 does not require any high-voltage (HV) devices. Both the input and output ports of the modular converter are connected to low-voltage (LV) sources — the lithium-ion cell and the vehicle LV bus. Using only LV devices, the converter system replaces the conventional kW-level HV-to-LV step-down converter in xEV. The kW-level power conversion from the battery pack HV output to the vehicle LV bus is achieved by the low-power LV-to-LV modular converters.

As there are a large number of converters in the system, practically controlling the system with good stability and robustness becomes a challenge. Central control relies on communication, and is therefore not practical for time-critical closed-loop regulation. Any latency or signal drops on the communication bus could easily cause stability problems or even compromise system safety. Moreover, with a central controller, performance of the



(a)

(b)

Figure 2.1: Active balancing with series-input-parallel-output converter system in (a) photovoltaic (PV) application; (b) xEV application.

converter system becomes highly dependent on the communication speed, which in most cases would be adversely affected by number of the converters, thus limiting scalability of the system.

Autonomous control increases system performance and robustness, as no communication is required for time critical control. For a practical strategy, the local controller should only access local converter variables such as its input/output current/voltage. In addition, the algorithm must be simple enough to be implemented on a low-cost microcontroller, and the computational effort for each local converter should not increase with the total number of converters in the system.

Automatic balancing could be achieved by distributed bus voltage regulation where each converter regulates the bus voltage autonomously Depending on the form of the transfer function of the bus voltage loop, the compenstator can be as simple as a standard proportional-integral (PI) controller. A key to achieve automatic balancing is that the reference for each voltage regulation loop should be dictated by the balancing objective. For example, in SOC balancing, the bus voltage reference can be mapped from the estimated cell SOC. In system steady state, the bus voltage equals the reference. As all the converters share the same bus voltage, the balancing targets also equal to each other. In another words, the bus not only processes the power for balancing, but also serves as a common reference for the balancing targets. As a result, balancing is naturally achieved through distributed bus voltage regulation. This concept was firstly developed in [43, 52] for photovoltaic (PV) cell balancing. The first attempts to apply a similar approach to xEV lithium-ion batteries was presented in [13, 67], as shown in Fig. 2.1 (a). As already mentioned, different from PV application, a significant benefit in xEV applications is that the converter system can also supply auxiliary loads in the vehicle and thus eliminate the need for the HV-to-LV step-down converter.

While the control strategy successfully balances photovoltaic cells, stability issues develop when the same approach is applied to lithium-ion batteries. The major focus of this chapter is in analyzing stability of the modular BMS with series-input-parallel-output converter system. The analysis is done in a design-oriented manner to enable simple design of the distributed loop compensators. The work has been presented in a conference paper [68] using slightly different terminology. The rest of the chapter is organized as follows: Section 2.1 describes the original design process of the bus voltage regulation and introduces the instability issues in SOC balancing. Section 2.2 reveals the reasons for the instability by analysis of the SOC control loop. An intuitive loop-gain analysis is developed to help understand the problem. Section 2.3 provides a more comprehensive loop-gain analysis, and

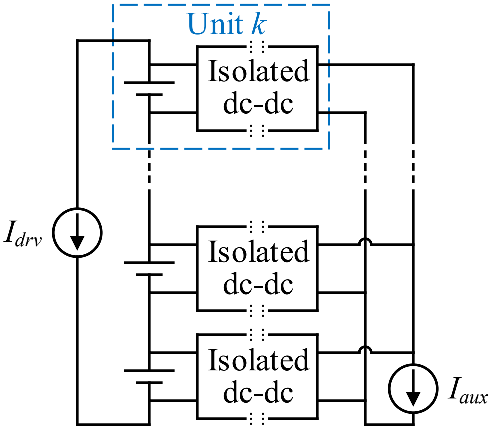


Figure 2.2: System model used in bus voltage regualtion design.

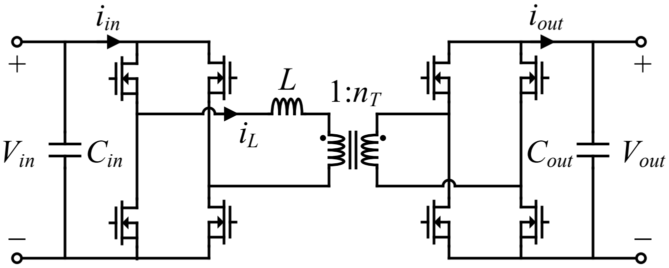


Figure 2.3: Isolated dc-dc with dual-active-bridge (DAB).

a second-order simplified form of the SOC loop-gain is given. The simplified form is used in the compensator design. Section 2.4 summarizes the chapter.

2.1 Automatic Balancing with Distributed Bus Voltage Regulation

First, system model used in bus voltage regulation design is introduced. The system model is shown in Fig. 2.2. A battery string with n cells in series is considered. Both the drivetrain and the LV bus load are modeled as constant current sources I_{drv} and I_{aux}, respectively. As the terminal voltage of a battery cell does not change significantly during bus voltage regulation, the battery cell is thus modeled as a constant voltage source. Regarding the isolated dc-dc converter, dual-active-bridge (DAB) converter with phase-shift modulation is employed. The DAB topology is shown in Fig. 2.3. Without going through details of the converter operation, which will be discussed in the next chapter, the steady-state model of the converter is given as follows:

$$\begin{aligned} I_{in} &= < i_{in} > = \frac{V_{out}}{2\pi n_T f_s L}(\Phi - sign(\Phi)\frac{\Phi^2}{\pi}) \\ I_{out} &= < i_{out} > = \frac{V_{in}}{2\pi n_T f_s L}(\Phi - sign(\Phi)\frac{\Phi^2}{\pi}) \end{aligned} \tag{2.1}$$

where V_{in} and V_{out} represent the DC input and output voltage, respectively, n_T is the transformer turns ratio, L is the tank inductance, f_s is the converter switching frequency, and phase-shift Φ is the control input of the converter. In a typical design, the phase-shift, represented as an angle, is much smaller than 2π. As a result, the higher order term in Eq. (2.1) is small enough to be neglected in analysis, and an approximated DAB steady-state equation is given by Eq. (2.2):

$$\begin{aligned} I_{in} &\approx \frac{V_{out}}{2\pi n_T f_s L}\Phi \\ I_{out} &\approx \frac{V_{in}}{2\pi n_T f_s L}\Phi \end{aligned} \tag{2.2}$$

The small signal model is derived by linearizing Eq. (2.2), as shown in Eq. (2.3):

$$\begin{aligned} \hat{i}_{in} &= \frac{V_{out}}{2\pi n_T f_s L}\hat{\varphi} + \frac{\Phi}{2\pi n_T f_s L}\hat{v}_{out} \approx \frac{V_{out}}{2\pi n_T f_s L}\hat{\varphi} = K_{DABi}\hat{\varphi} \\ \hat{i}_{out} &= \frac{V_{in}}{2\pi n_T f_s L}\hat{\varphi} + \frac{\Phi}{2\pi n_T f_s L}\hat{v}_{in} \approx \frac{V_{in}}{2\pi n_T f_s L}\hat{\varphi} = K_{DABo}\hat{\varphi} \end{aligned} \tag{2.3}$$

where K_{DABi} and K_{DABo} are assumed to be identical from unit to unit.

For convenience, small signal variables are represented without hats in the rest of the chapter, $\hat{i}_{in}$, $\hat{i}_{out}$, and $\hat{\varphi}$ are written simply as i_{in}, i_{out}, and φ, respectively, but it is understood that the dynamic model equations and frequency responses refer to small-signal perturbations. Eq. (2.3) is then expressed as:

$$\begin{aligned} i_{in} &\approx K_{DABi}\varphi \\ i_{out} &\approx K_{DABo}\varphi \end{aligned} \tag{2.4}$$

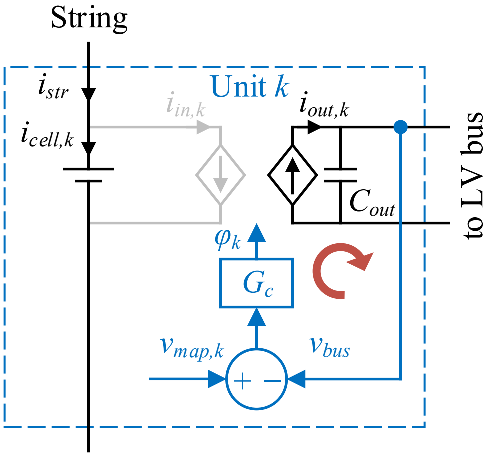


Figure 2.4: Unit k in the system, with the voltage loop modeled.

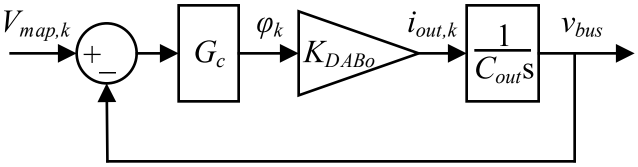


Figure 2.5: Control diagram of bus voltage regulation.

Each cell and its corresponding converter together is referred to as a unit. A unit k is selected for compensator design, the details of which are shown in Fig. 2.4. As all the units have the same converter topology and parameters, unit k is also seen as a virtual unit which represents the average of all the n units in the system. A compensator for bus voltage regulation is designed based on the model of the virtual unit. The compensator is then implemented on each physical unit in practice. A standard proportional-integral (PI) controller with the form shown in Eq. (2.5) is used:

$$G_C = K_p + \frac{K_i}{s} \tag{2.5}$$

The reference of the voltage regulation in each unit comes from mapping the SOC of the cell

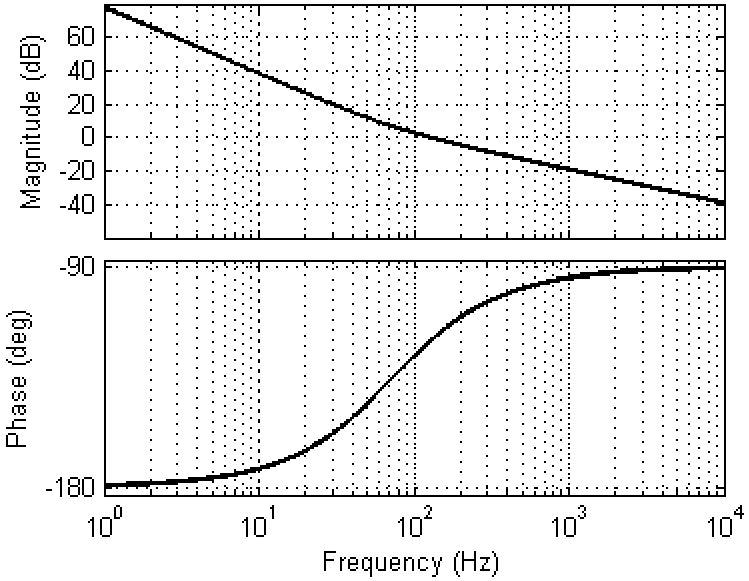


Figure 2.6: Loop-gain Bode plot for the bus voltage loop.

in the unit:

$$V_{map,k} = K_{map} SOC_k + constant \tag{2.6}$$

If all the converters are in linear operating mode without hitting any current or voltage limits, the bus voltage value represents the average value of the balancing target. With the unit model in Fig. 2.4, the control diagram of bus voltage regulation is shown in Fig. 2.5, and corresponding loop-gain transfer function is given by Eq. (2.7):

$$T_v = G_c K_{DABo} \frac{1}{C_{out} s} = \frac{K_i K_{DABo} (1 - \frac{K_p}{K_i} s)}{C_{out} s^2} \tag{2.7}$$

The Bode plot of the loop-gain in Eq. (2.7) is given in Fig. 2.6. The PI controller parameters are selected so that the crossover frequency of the voltage loop is at about 100 Hz.

The design is examined with a small battery system consisting of 3 units. The battery string current is 0 and the LV bus current is constant at 3 A. The converter input current is limited in a range from 0 A to 10 A. Simulation results are shown in Fig. 2.7. While the PI controller successfully regulates the bus voltage, slow cell current oscillations with large amplitude can be observed in the SOC balancing process.

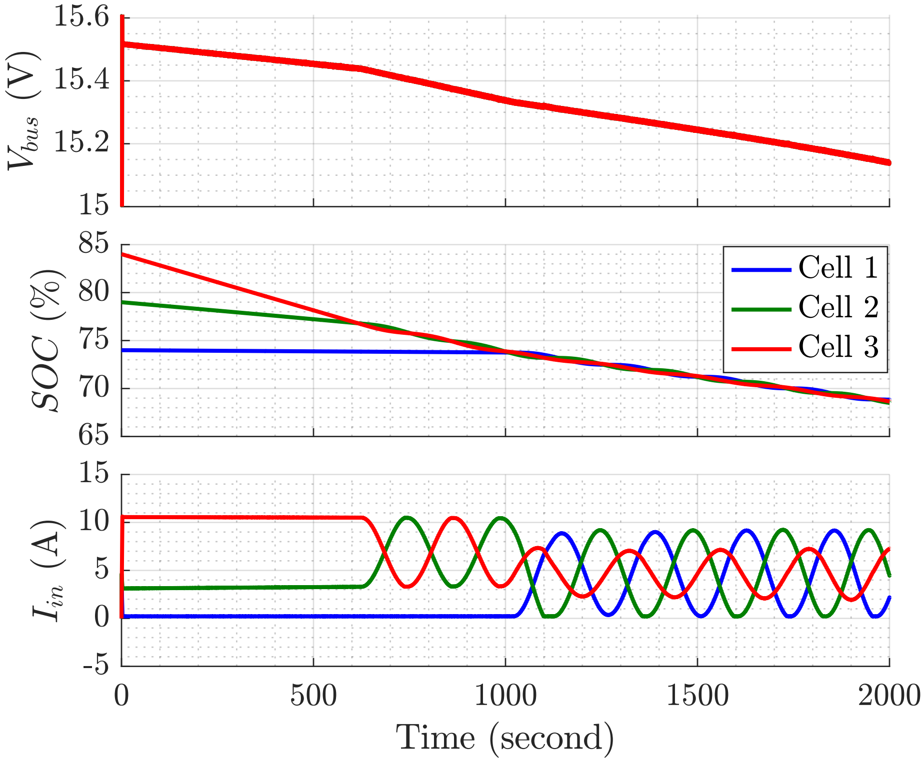


Figure 2.7: Converter input current oscillation.

2.2 SOC Control Loop

As an energy storage device, the SOC of a lithium-ion battery cell slowly varies during cycling, i.e. during charging and discharging. In Section 2.1, the SOC dynamic was considered to be so slow that it was neglected. The assumption is not problematic for the voltage loop-gain compensator design, and the simulation results in Fig. 2.7 confirm stability of the bus voltage regulation loop. However, automatic SOC balancing does not work as expected. The converter input current oscillations not only prevent the system from reaching a balanced state, but also significantly reduce efficiency in practice as large amounts of energy are unnecessarily transferred back and forth through the converters. In addition to voltage loop compensation, the stability of the balancing loop must be analyzed taking the slow SOC loop dynamics into consideration. It should be noted that, unlike current or voltage, SOC is not easily measurable in practice. SOC is an internal state of the battery. The information

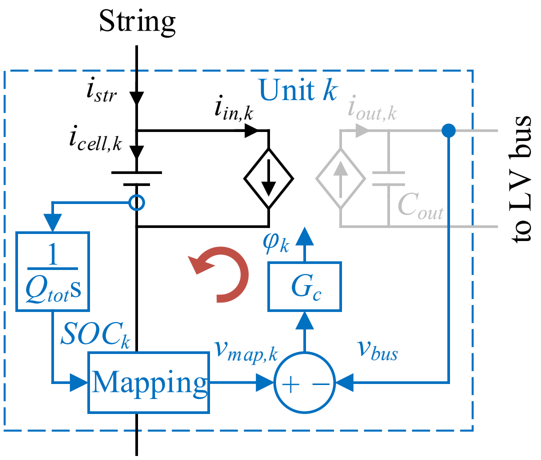


Figure 2.8: Unit k in the system, with the SOC loop modeled.

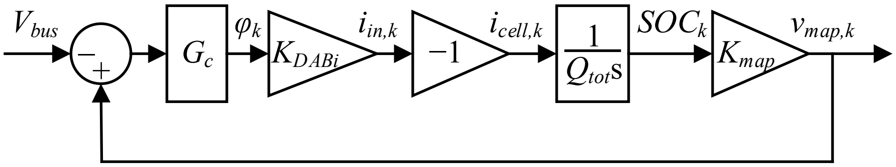


Figure 2.9: Control diagram of the SOC loop of unit k.

of SOC is usually obtained based on cell current, cell voltage, and cell temperature, which is known as SOC estimation. The SOC estimation process is discussed in more detail in Chapter 4. In this chapter it is assumed that the estimated SOC equals to the true SOC of the battery cell. In addition, it is also assumed that all the cells have identical total capacity of the nominal value. The SOC of cell k is thus expressed as:

$$SOC_k = SOC_{init,k} + \frac{1}{Q_{tot}} \int i_{cell,k} dt \tag{2.8}$$

in which Q_{tot} represents the total capacity of the battery cell. $SOC_{init,k}$ is the initial SOC value at the beginning of current integration.

The small signal model of Eq. (2.8) is shown in Eq. (2.9):

$$SOC_k = \frac{1}{Q_{tot}s} i_{cell,k} \tag{2.9}$$

With the slow SOC dynamics taken into account, an SOC loop is modeled in unit k, as shown in Fig. 2.8. For a preliminary analysis of the SOC loop in unit k, the bus voltage is considered perfectly regulated by the other units in the system. In practice, the more converters in the system, the less unit k affects the bus voltage. As converter number approaches infinity, unit k and the bus voltage become completely decoupled. Thus the bus voltage can be modeled approximately as a constant voltage source for the analysis of the SOC loop. Under the extreme condition with perfectly regulated bus voltage, a simple SOC loop model is shown in Fig. 2.9, with the loop-gain transfer function given by Eq. (2.10).

$$T_{soc} = G_c K_{DABi} \frac{1}{Q_{tot}s} K_{map} = \frac{K_i K_{DABi} K_{map} (1 - \frac{K_p}{K_i} s)}{Q_{tot} s^2} \tag{2.10}$$

The loop-gain of the SOC loop has the same pole and zero as the loop-gain of the voltage loop in Eq. (2.7). However, the DC gain of the SOC loop gain is much smaller, predominately due to the fact that the battery cell total capacity value is commonly much larger than the converter output capacitor value. With the same pole and zero but much smaller DC gain, the SOC loop crossover frequency is much lower than the bus voltage loop. As the PI parameters are specifically designed for the bus voltage loop in Eq. (2.7), the SOC loop in Eq. (2.10) exhibits nearly zero phase margin, causing instability and converter input current oscillations in the presence of even slight loop delays.

2.3 Comprehensive Analysis of the SOC Control Loop

In Section 2.2, a preliminary analysis is given to help understand the nature of the instability and the oscillating converter currents. However, the bus voltage is considered constant by assuming that an infinite number of units in the system perform bus voltage

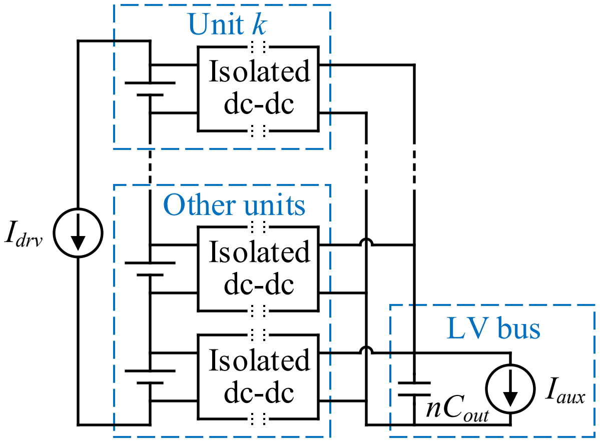


Figure 2.10: System model used in comprehensive SOC loop analysis.

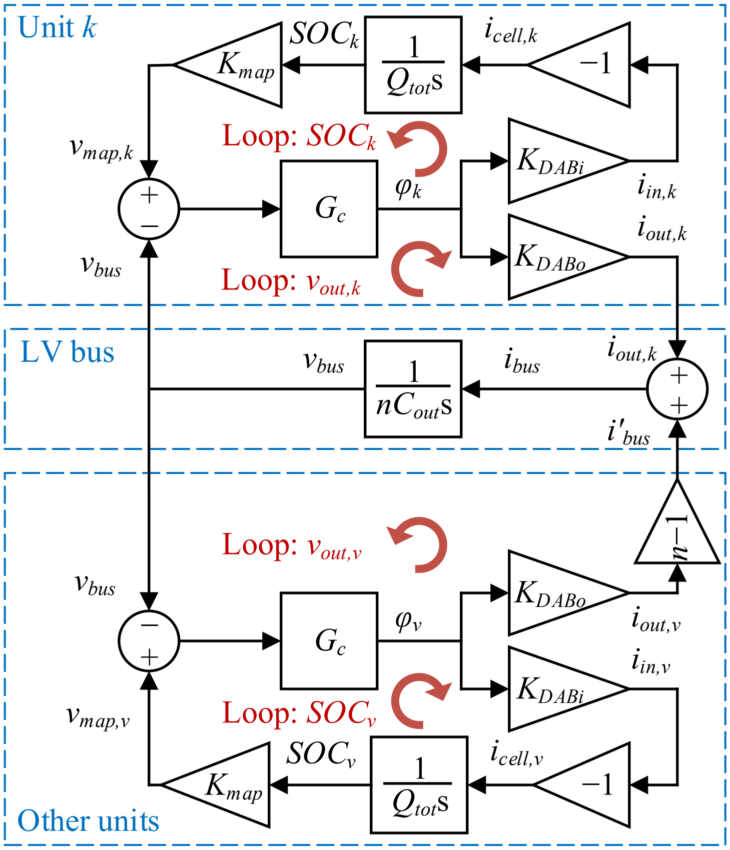


Figure 2.11: Comprehensive SOC loop analysis.

Table 2.1: Parameters in Eq. (2.11)

Parameter	**Expression**
T_0	$(n-1)+\frac{K_{DABi}K_{map}nC_{out}}{K_{DABo}}$
a_1	$\frac{2K_p}{K_i}$
a_2	$\frac{K_p^2}{K_i^2}+\frac{n}{K_i}(\frac{C_{out}}{K_{DABo}}+\frac{1}{K_{DABi}K_{map}})$
a_3	$\frac{K_p n}{K_i^2}(\frac{C_{out}}{K_{DABo}}+\frac{1}{K_{DABi}K_{map}})$
a_4	$\frac{nC_{out}}{K_i^2K_{DABi}K_{DABo}K_{map}}$
b_1	$\frac{K_p}{K_i}$
b_2	$\frac{K_p}{K_i}$
b_3	$\frac{nC_{out}}{K_i(K_{DABo}(n-1)+K_{DABi}K_{map}nC_{out})}$

regulation together. In a more practical scenario, there is a certain finite number of converters in the system. Thus bus voltage variation should be considered. A new system model is given in Fig. 2.10. There are three parts in the system. When the SOC loop of unit k is being examined, the other units are also modeled as a virtual unit replicated $n-1$ times. Different from Fig. 2.2 in voltage loop design, the output capacitors of all the converters are modeled together on the LV bus. The control diagram of the entire system is shown in Fig. 2.11.

The SOC loop-gain of unit k is derived by merging Loop: SOC_v, Loop: $v_{out,v}$, Loop: $v_{out,k}$, and Loop: SOC_k one by one into each other, resulting in a high-order transfer function with parameters given in Table 2.1:

$$T_{soc,k}=T_0\frac{(1+b_1s)(1+b_2s+b_3s^2)}{1+a_1s+a_2s^2+a_3s^3+a_4s^4} \tag{2.11}$$

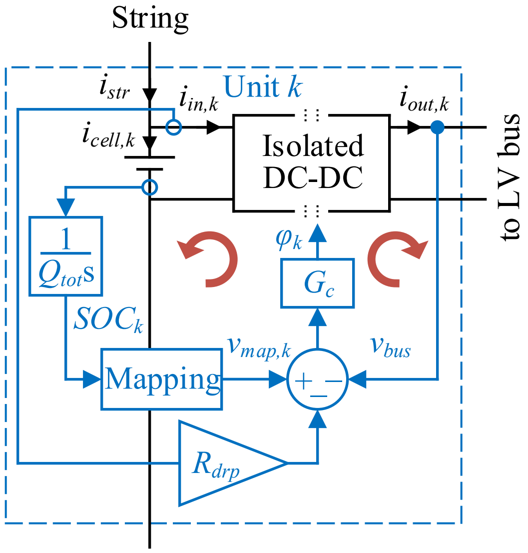


Figure 2.12: Introduction to additional droop control in unit k.

Considering the fact that the SOC loop bandwidth is much lower than the bus voltage loop bandwidth, high frequency dynamics from the bus voltage loop can be neglected. Eq. (2.11) is thus simplified to a second-order transfer function:

$$T_{soc} = (n-1)\frac{1}{1 + \dfrac{K_p}{K_i}s + \dfrac{nQ_{tot}}{K_i K_{DABi} K_{map}}s^2} \tag{2.12}$$

As the number of converter approaches infinity, Eq. (2.12) becomes:

$$T_{soc} = \frac{K_i K_{DABi} K_{map}}{Q_{tot}s^2} \tag{2.13}$$

Eq. (2.13) is almost the same as Eq. (2.10) in the frequency range of interest. The zero $1 + K_p s/K_i$ in the PI controller is neglected in Eq. (2.13) though, as the zero is out of the frequency range of interest. In other words, as the the PI zero is designed for the bus voltage loop, the zero is in the high frequency range and does not have much effect on the SOC loop stability. As a result, the SOC loop cannot be stabilized by tuning PI parameters.

Based on the analysis above, a method using droop control to compenstate the SOC loop has been proposed in [68], a result of collaboration with researchers at the Utah Power

Table 2.2: Parameters in Eq. (2.11), with Droop Control

Parameter	**Expression**
T_0	$(n-1)+\frac{K_{DABi}K_{map}nC_{out}}{K_{DABo}}$
a_1	$\frac{2K_p}{K_i}+\frac{nR_{drp}}{K_{map}}(1+\frac{K_{DABi}K_{map}C_{out}}{K_{DABo}})$
a_2	$\frac{K_p^2}{K_i^2}+\frac{n}{K_i}(\frac{C_{out}}{K_{DABo}}+\frac{1}{K_{DABi}K_{map}})$ $+\frac{nR_{drp}}{K_{map}}(\frac{2K_p}{K_i}(1+\frac{K_{DABi}K_{map}C_{out}}{K_{DABo}})+\frac{K_{DABi}C_{out}R_{drp}}{K_{DABo}})$
a_3	$\frac{K_pn}{K_i^2}(\frac{C_{out}}{K_{DABo}}+\frac{1}{K_{DABi}K_{map}})$ $+\frac{nR_{drp}}{K_{map}}(\frac{K_p^2}{K_i^2}(1+\frac{K_{DABi}K_{map}C_{out}}{K_{DABo}})+\frac{2C_{out}(1+K_{DABi}K_pR_{drp})}{K_{DABo}K_i})$
a_4	$\frac{nC_{out}(1+K_{DABi}K_pR_{drp})}{K_i^2K_{DABi}K_{DABo}K_{map}}$
b_1	$\frac{K_p}{K_i}$
b_2	$\frac{K_p}{K_i}+\frac{K_{DABi}R_{drp}nC_{out}}{K_{DABo}(n-1)+K_{DABi}K_{map}nC_{out}}$
b_3	$\frac{(1+K_{DABi}K_pR_{drp})nC_{out}}{K_i(K_{DABo}(n-1)+K_{DABi}K_{map}nC_{out})}$

Electronics Lab (UPEL). The droop control works simultaneously with the original PI regulator, as shown in Fig. 2.12. The converter input current goes through a virtual droop resistance R_{drp}, the virtual voltage drop is then subtracted from the original reference mapped from the cell SOC, the result of which becomes the new reference for the bus voltage regulation. With droop control, a new SOC loop-gain diagram is shown in Fig. 2.13. The SOC loop gain transfer function has the same form as Eq. (2.13), but the new expressions for the parameters are shown in Table 2.2.

Again, by considering the fact that the SOC loop bandwidth is much lower than the bus voltage loop bandwidth, high frequency dynamics from the bus voltage loop are neglected.

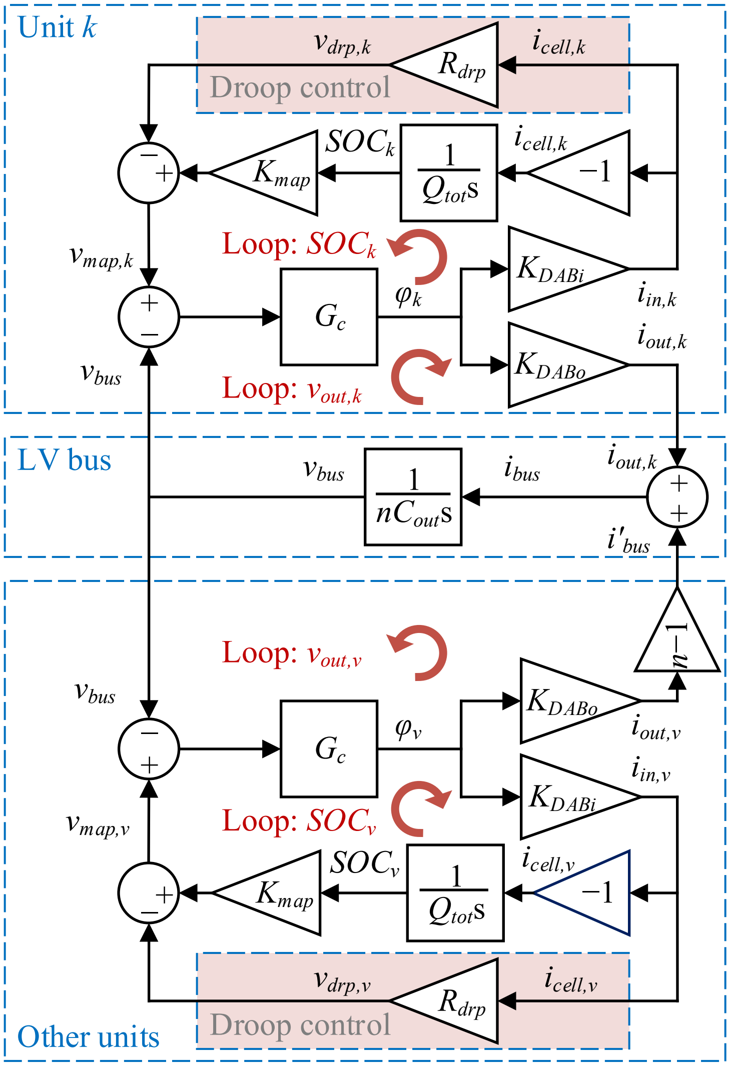


Figure 2.13: Comprehensive SOC loop analysis with droop control.

Eq. (2.11) is thus simplified to a second-order transfer function:

$$T_{soc} = (n-1)\frac{1}{1+(\frac{K_p}{K_i}+\frac{nR_{drp}}{K_{map}})s+\frac{nQ_{tot}}{K_iK_{DABi}K_{map}}s^2} \tag{2.14}$$

One may observe that the SOC loop is compensated through the virtual droop resistance. With Eq. (2.14), the value of the droop resistance can be quickly calculated. The stability is examined on a battery system consists of three units. The Bode plot of the SOC

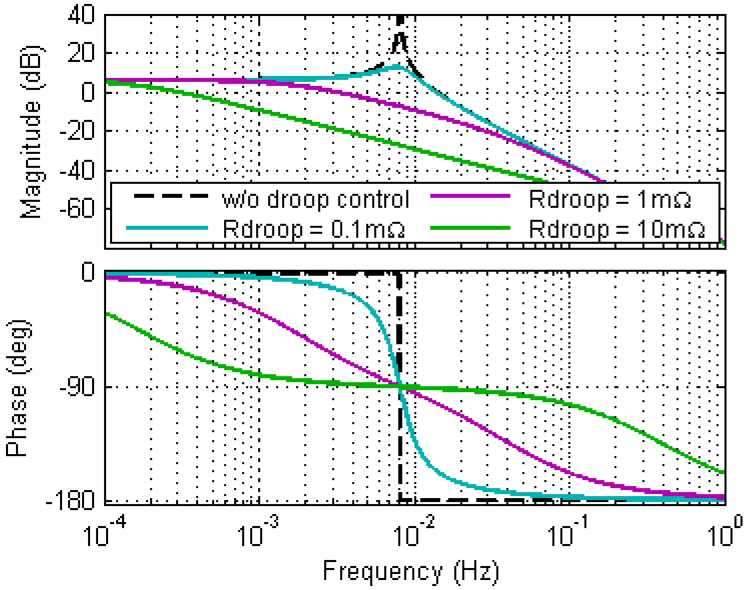
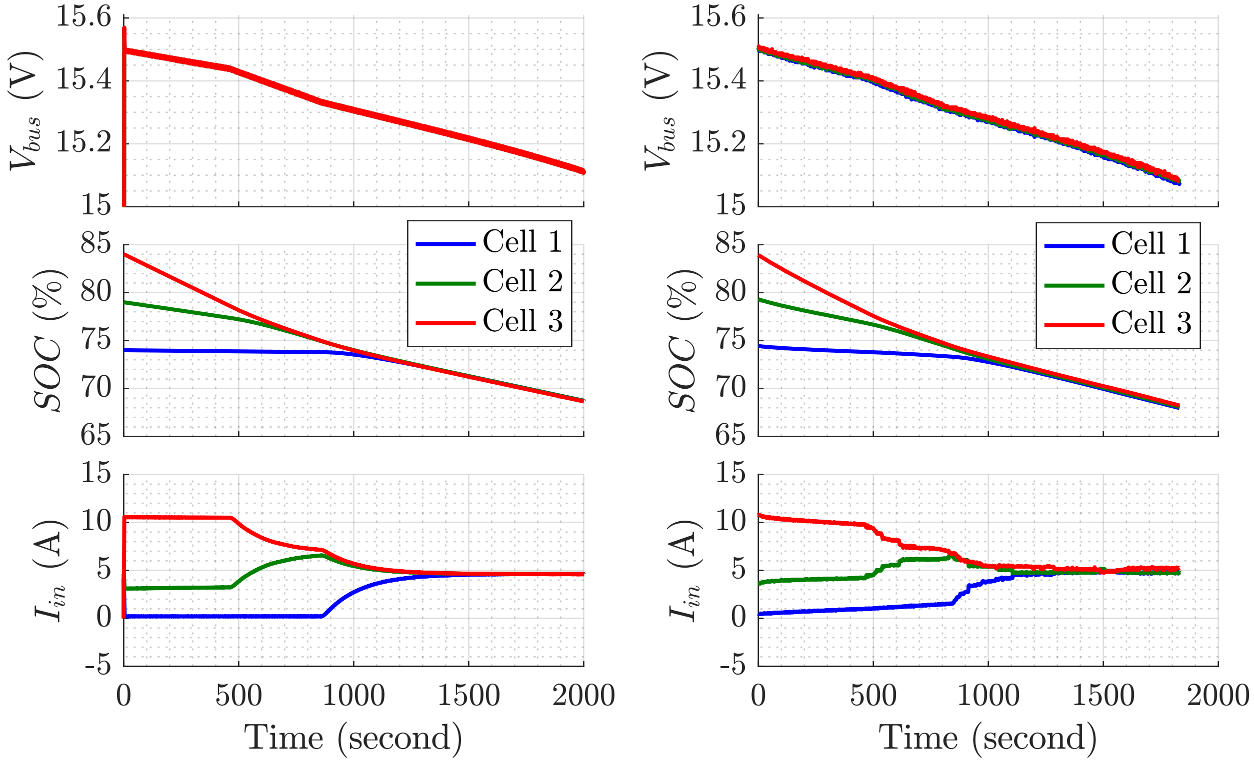


Figure 2.14: SOC loop loop-gain Bode plot with different droop resistance.



(a) (b)

Figure 2.15: 3-cell system with $R_{drp} = 6.4\,\text{m}\Omega$, (a) simulation results; (b) experimental results (experiment done by Mr. M. Muneeb Ur Rehman, Utah Power Electronics Lab, Utah State University).

loop loop-gain of unit k with different droop resistance is shown in Fig. 2.14. As droop resistance increases, the phase margin of the SOC loop improves. However the crossover frequency becomes lower, indicating slower balancing speed. In the battery system with 3 units, $6.4\,\mathrm{m\Omega}$ is chosen to achieve both stable system operation and high balancing speed. The simulation and experimental results are shown in Fig. 2.15 (a) and Fig. 2.15 (b), respectively.

2.4 Summary

This chapter analyzes stability of the modular BMS with distributed controlled series-input-parallel-output converters. It is found that in lithium-ion battery cell balancing, the SOC loop results in system instability and converter current oscillations. The SOC loop also shares the PI controller designed for voltage loop compensation. As the bandwidth of the SOC loop is much lower than the bandwidth of the bus voltage regulation loop, tuning PI parameters cannot be used to stabilize the SOC loop without significantly sacrificing voltage regulation performance. An alternative method, such as droop control, must be used to compensate the SOC loop. A simplified second-order transfer function of the SOC loop is derived, which allows simple design of the SOC loop compensator, and the results are verified by simulations and experiments.

Chapter 3

Improved Steady-State Model of the Dual-Active-Bridge Converter

In the previous chapter, stability of the modular BMS with series-input-parallel-output converter system is examined. In the system, dual-active-bridge (DAB) converter is used as the isolated dc-dc converter module. This chapter focuses on steady-state modeling of the DAB converter. The conventional DAB model is described and motivation for development of an improved DAB model is then presented.

The DAB converter with phase-shift modulation was developed in early 1990s [16, 32]. The topology of the DAB converter is shown in Figure 3.1. It consists of two full bridges, a transformer, and a series tank inductor L. In phase-shift modulation, the two full bridges are both switching at 50 % duty cycle, and the phase-shift φ between the two bridges controls the converter power flow. DAB advantages include low RMS current stresses, low input and output current ripples, capability of zero-voltage switching (ZVS) in both bridges, and bidirectional power flow. Numerous prior works have been devoted to DAB static and dynamic modeling, as well as power-stage design and efficiency optimization in various applications [16,22,32,36,37,50,53,54] Considering an ideal circuit model, the basic steady-state characteristics of the DAB converter are obtained by averaging over a switching period and are given in [32], where the symbols in the equations are defined in Table 3.1:

$$\begin{aligned} I_{in} &=< i_{in} >= \frac{V_{out}}{2\pi n_T f_s L}(\varphi - sign(\varphi)\frac{\varphi^2}{\pi}) \\ I_{out} &=< i_{out} >= \frac{V_{in}}{2\pi n_T f_s L}(\varphi - sign(\varphi)\frac{\varphi^2}{\pi}) \end{aligned} \tag{3.1}$$

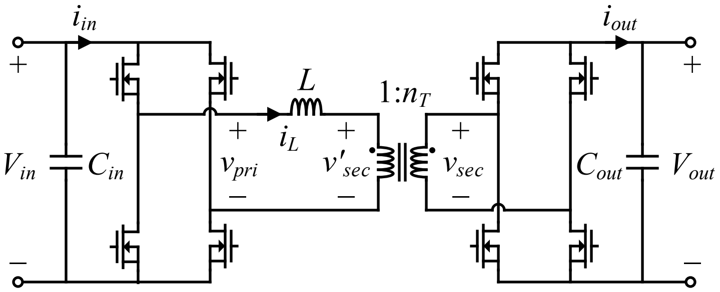


Figure 3.1: Topology of the dual-active-bridge (DAB) converter.

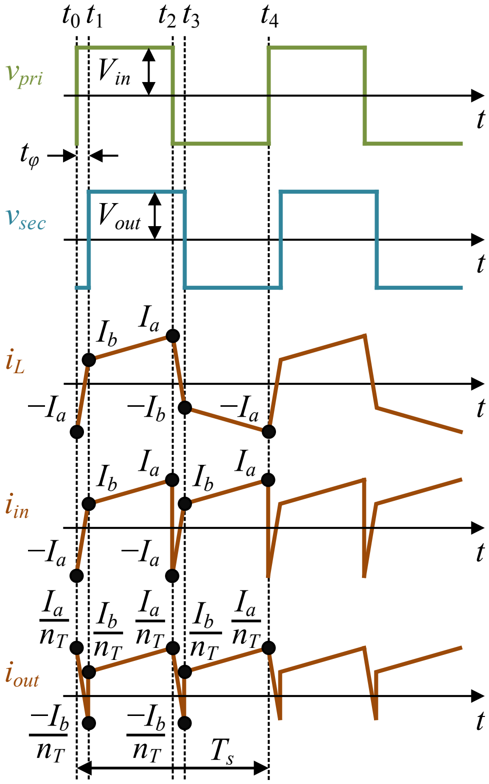


Figure 3.2: DAB switching waveforms with phase-shift modulation.

Note that the input dc current is a function of the phase-shift and the output voltage, and is ideally not affected by the input voltage at all. Similarly, the output dc current is a function of the phase-shift and the input voltage, and is not affected by the output voltage

Table 3.1: Symbol Definition

Symbol	**Definition**
V_{in}	Converter dc input voltage (V)
V_{out}	Converter dc output voltage (V)
v_{pri}	Tank input voltage (V)
v'_{sec}	Tank output voltage (V)
v_{sec}	Tank output voltage on transformer secondary-side (V)
I_{in}	Converter dc input current (A)
I_{out}	Converter dc output current (A)
i_{in}	Converter input current (A)
i_{out}	Converter output current (A)
i_L	Tank current (A)
n_T	Transformer turns ratio
L	Tank inductance (H)
f_s	Switching frequency (Hz)
T_s	Switching period (s): $T_s = 1/f_s$
t_φ	Phase-shift time (s)
φ	Phase-shift angle (rad): $\varphi = 2\pi t_\varphi f_s$

at all. The ideal steady-state model in Eq. (3.1) is well known and has successfully been used in many DAB applications. The work reported in this thesis is motivated by cases where it is found that DAB steady-state characteristics may significantly depart from the ideal steady-state model in Eq. (3.1). Consider, as an example, a DAB prototype shown in Fig. 3.3, with the parameters given in Table 3.2, which correspond to the converter parameters in the modular BMS discussed in the previous chapter. This is a relatively high-frequency, relatively low-power prototype where the tank inductance L is based entirely on the transformer leakage inductance, and is relatively small in value [13,67]. Fig. 3.4 compares the steady-state characteristics predicted by Eq. (3.1) with the characteristics measured in

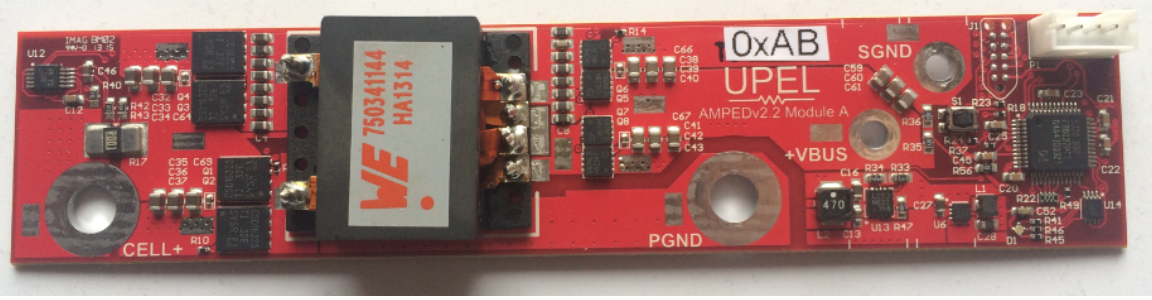
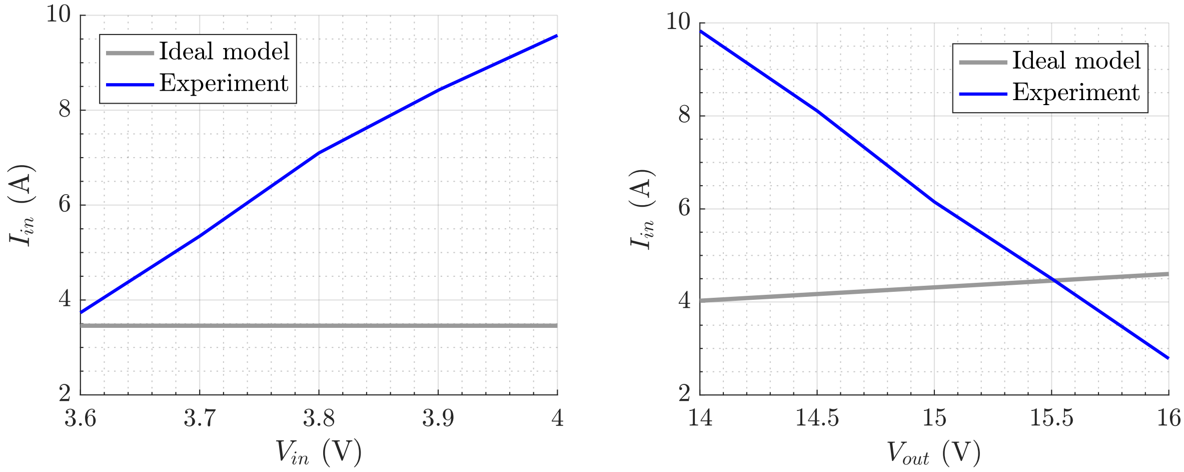


Figure 3.3: DAB prototype designed for the modular active balancing BMS.



(a)

(b)

Figure 3.4: Mismatch between the ideal model in Eq. 3.1 and the experimental results with the DAB prototype: (a) I_{in} vs. V_{in} ($t_\varphi = 30\,\text{ns}$, $V_{out} = 14.0\,\text{V}$); (b) I_{in} vs. V_{out} ($t_\varphi = 35\,\text{ns}$, $Vin = 4.0\,\text{V}$).

the experimental prototype. Note that the measured dc input current depends very strongly on both the dc input voltage and the dc output voltage. The deviations with respect to the ideal model in Eq. (3.1) are very significant. One may note that not even the slope of $I_{in}(V_{out})$ is predicted correctly by the ideal model.

A number of more detailed static and dynamic models have been developed for the DAB converter. For example, details of DAB converter losses are analyzed in [36, 54, 74], while [65] develops a generalized current averaging model targeting high-frequency dynamics. It has further been found that static and dynamic effects of zero-voltage switching become

Table 3.2: DAB Prototype

Symbol	**Definition**
f_s	200 kHz
V_{in}	2.5 V - 4.1 V
V_{out}	10 V - 16 V
n_T	1 : 4
L	$\approx$ 30 nH
R	$\approx$ 30 mΩ
Peak efficiency	94 %
Maximum power rating	40 W
Deadtime	16.7 ns

significant when the switching frequency is relatively high so that ZVS transitions take significant portions of a switching period [14, 15]. None of the prior works, however, have pointed to or explained the potential substantial discrepancies in steady-state characteristics exemplified in Fig. 3.4. The objectives of this chapter are to explain limitations of the basic ideal steady-state model Eq. (3.1), and to introduce an improved steady-state model capable of more accurately predicting DAB converter steady-state characteristics. A new method to derive the steady-state equations is developed in Section 3.1. An improved DAB steady-state model is then derived in Section 3.2, where it is shown that conduction losses and the time constant associated with the tank inductor play major roles in the converter steady-state characteristics. Experimental results demonstrating improved model predictions are given in Section 3.3, and a chapter summary is presented in Section 3.4.

3.1 A New Approach to Derivation of DAB Steady-State Model

Conventionally the ideal DAB steady-state equations in Eq. (3.1) are derived by analyzing the waveforms in Fig. 3.2. The corner points I_a and I_b in the waveforms of i_L are solved:

$$\begin{aligned} I_b &= -I_a + \frac{1}{L}\int_{t_0}^{t_1}(v_{pri} - v'_{sec})dt = -I_a + \frac{1}{L}\int_{0}^{t_\varphi}(V_{in} + \frac{V_{out}}{n_T})dt \\ I_a &= I_b + \frac{1}{L}\int_{t_1}^{t_2}(v_{pri} - v'_{sec})dt = I_b + \frac{1}{L}\int_{t_\varphi}^{\frac{T_s}{2}}(V_{in} - \frac{V_{out}}{n_T})dt \end{aligned} \tag{3.2}$$

Then the dc values of $i_{in}$and i_{out} are calculated by averaging the waveform over half switching period, which gives Eq. (3.1). The method is straightforward. However it does not give intuitive insights into the form of the dc model expressions.

A new method to derive DAB steady-state equation is developed in this section. Consider the DAB tank inductor in Fig. 3.5 (a) as a linear system. The primary-side voltage v_{pri} and the secondary-side voltage v_{sec} are two independent inputs. The difference of the two inputs is then integrated to generate the inductor current i_L, which is the output of the system. Using superposition, the inductor current can be decomposed into two components:

$$\begin{aligned} i_{L,1} &= \frac{1}{L}\int v_{pri}dx \\ i_{L,2} &= \frac{1}{L}\int v'_{sec}dx \\ i_L &= i_{L,1} + i_{L,2} \end{aligned} \tag{3.3}$$

The component $i_{L,1}$ is only affected by the tank primary-side voltage, while $i_{L,2}$ is only affected by the tank secondary side voltage. Since the duty cycle of both bridges is 50 %, v_{pri} is simply a square-wave waveform with magnitude equal to V_{in}; similarly, v_{sec} is a square-wave with magnitude equal to V_{out}. Both the current component waveform are triangular. Adding the two components results in the familiar DAB tank inductor current waveform shown in Fig. 3.6. The corresponding input and output current waveforms of each inductor current component can be found as shown in Fig. 3.7. From Fig. 3.7 (a), it follows that the input port voltage does not affect the input port current since the waveform of $i_{in,1}$ is symmetrical along the time axis, the area S_p above the time axis and the area S_n below the time axis equals to each other. The input port current is then decided by $i_{in,2}$ only and can easily be calculated by measuring the area S_e of the waveform in Fig. 3.7 (b). This approach

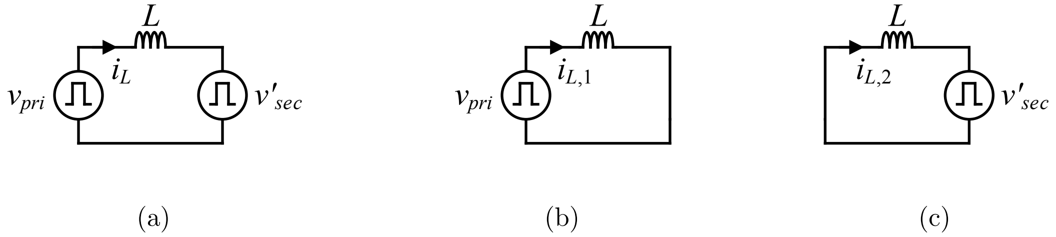


Figure 3.5: (a) Ideal DAB tank model; (b) superposition: primary-side source; (c) superposition: secondary-side source.

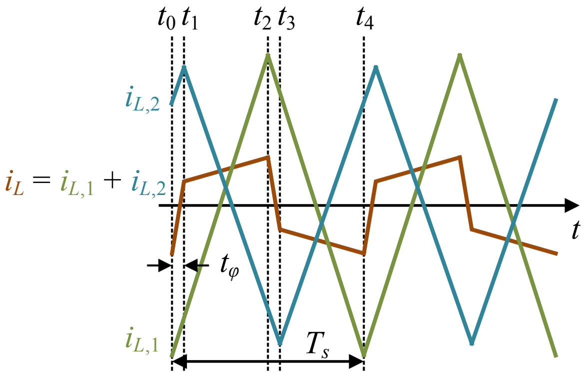
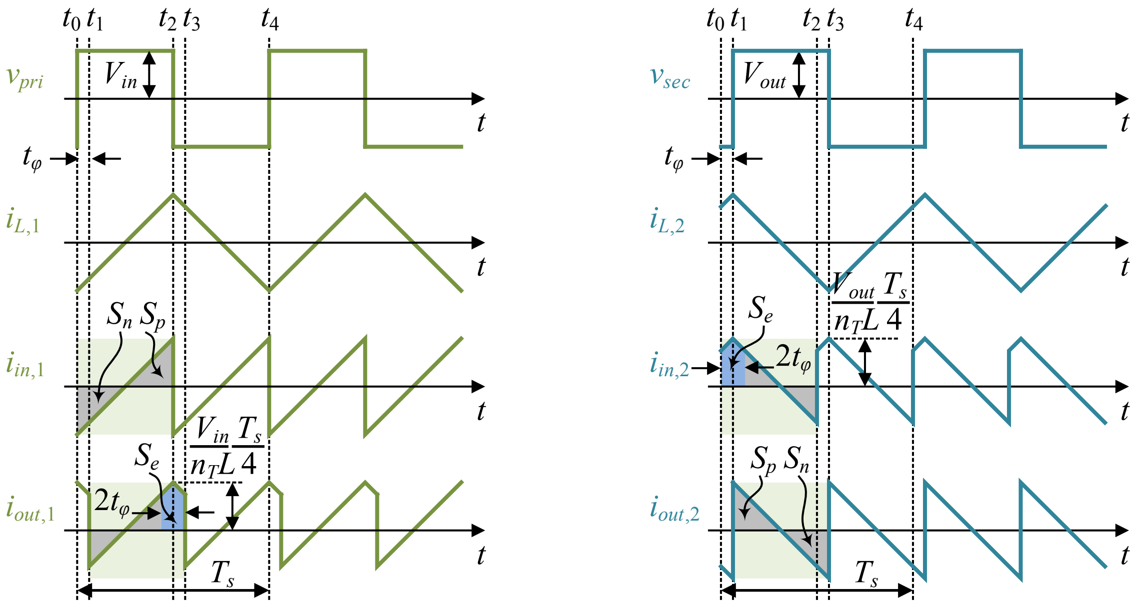


Figure 3.6: Superposition of the ideal DAB tank current waveform.

provides a new way to derive the ideal model equations given by Eq. (3.3). The advantage of this analysis approach will become clear as it leads to extensions necessary to derive an improved steady-state model in the next section.

3.2 Derivation of Improved DAB Steady-State Model

In this section, the analysis method of Section 3.1 is applied to the tank shown in Fig. 3.8, where a lumped series resistance R models series conduction losses due to switch on-resistances, tank and transformer resistances. In high-frequency switched-mode power converters, inclusion of conduction losses typically results in relatively small, second-order



(a) (b)

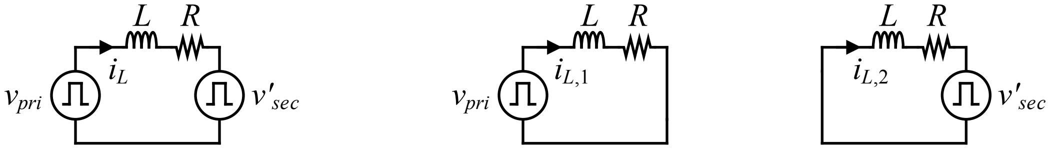
Figure 3.7: Ideal tank waveform for (a) superposition: primary-side source; (b) superposition: secondary-side source.

deviations with respect to converter ideal stead-state characteristics. In this section, it is shown that this is not the case for the DAB converter: even relatively small conduction losses can have profound effects on the steady-state characteristics.

With the lossy tank impedance model in Fig. 3.8, the inductor current waveform becomes distorted, as shown in Fig. 3.9. The deviation with respect to the ideal i_L waveform of Fig. 3.6 depends on the ratio of the tank time constant $\tau = L/R$ and the switching period T_s:

$$\delta = \frac{\tau}{T_s} = \frac{Lf_s}{R} \tag{3.4}$$

Following the analysis method of Section 3.2, the component waveform for the lossy tank are shown in Fig. 3.7. Note that averaging $i_{in,1}$ over $T_s/2$ does not equal to 0 anymore, which means that the dc input current is indeed affected by the input voltage, as seen in the experimental results shown in Fig. 3.4. Averaging waveforms in Fig. 3.10 (a) and (b) for a



(a) (b) (c)

Figure 3.8: (a) Lossy DAB tank model; (b) superposition: primary-side source; (c) superposition: secondary-side source.

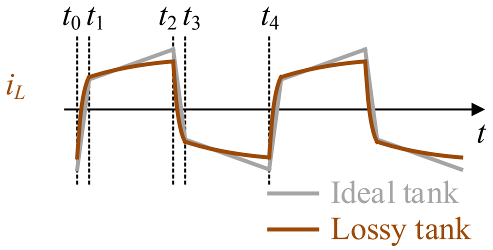


Figure 3.9: DAB tank current waveform with conduction loss.

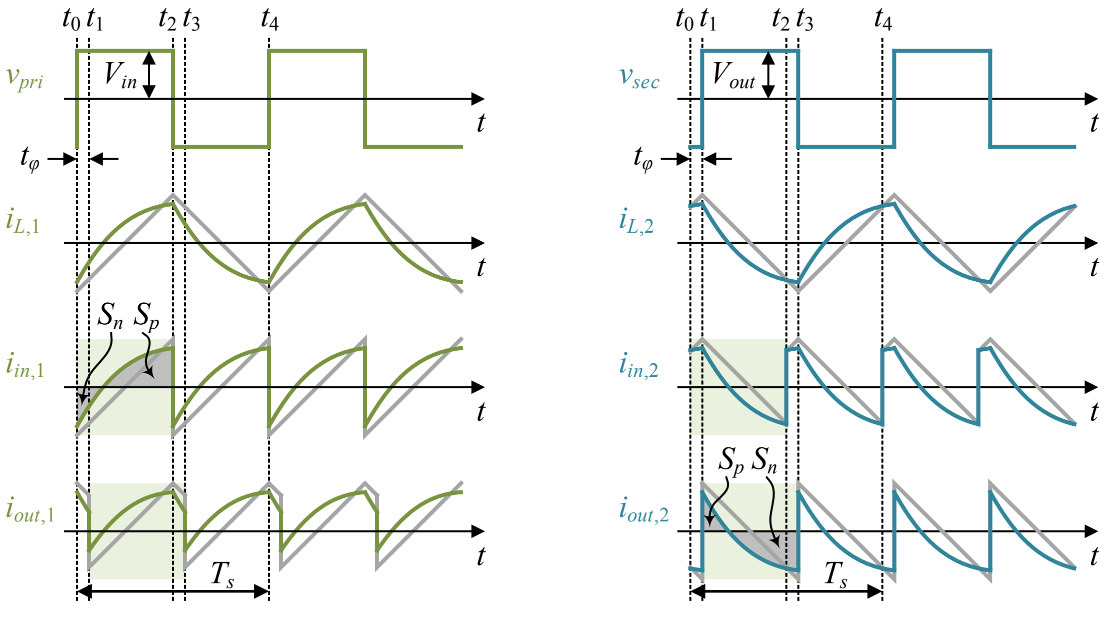
DAB converter with transformer turns ratio n_T yields:

$$\begin{aligned} < i_{in,1} >= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_{in,1}dt = \frac{V_{in}}{R}(1-K) \\ < i_{out,1} >= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_{out,1}dt = \frac{V_{in}}{n_T R}(1-f_o(\varphi)) \end{aligned} \tag{3.5}$$

$$\begin{aligned} < i_{in,2} >= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_{in,2}dt = \frac{V_{out}}{n_T R}(f_i(\varphi)-1) \\ < i_{out,2} >= \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_{out,2}dt = \frac{V_{out}}{n_T^2 R}(K-1) \end{aligned} \tag{3.6}$$

where the parameters are summarized in Table 3.3. By adding Eq. (3.5) and Eq. (3.6), the new improved steady-state model is obtained:

$$\begin{aligned} I_{in} =< i_{in} >=< i_{in,1} > + < i_{in,2} >= \frac{V_{in}}{R}(1-K) + \frac{V_{out}}{n_T R}(f_i(\varphi)-1) \\ I_{out} =< i_{out} >=< i_{out,1} > + < i_{out,2} >= \frac{V_{in}}{n_T R}(1-f_o(\varphi)) + \frac{V_{out}}{n_T^2 R}(K-1) \end{aligned} \tag{3.7}$$



(a) (b)

Figure 3.10: Lossy tank waveform for (a) superposition: primary-side source; (b) superposition: secondary-side source.

Table 3.3: Parameters in the Improved DAB Steady-State Model

Parameter	**Value**
f_s	$\frac{1}{f_s}$
τ	$\frac{L}{R}$
δ	$\frac{\tau}{T_s}$
K	$4\delta\frac{1-e^{\frac{-1}{2\delta}}}{1+e^{\frac{-1}{2\delta}}}$
$f_i(\varphi)$	$\frac{2\lvert\varphi\rvert}{\pi}+4sign(\varphi)\delta\frac{e^{\frac{1}{4\delta}}-2e^{-\frac{sign(\varphi)}{4\delta}+\frac{\varphi}{2\pi\delta}}+e^{-\frac{1}{4\delta}}}{e^{\frac{1}{4\delta}}+e^{-\frac{1}{4\delta}}}$
$f_o(\varphi)$	$\frac{2\lvert\varphi\rvert}{\pi}-4sign(\varphi)\delta\frac{e^{\frac{1}{4\delta}}-2e^{\frac{sign(\varphi)}{4\delta}-\frac{\varphi}{2\pi\delta}}+e^{-\frac{1}{4\delta}}}{e^{\frac{1}{4\delta}}+e^{-\frac{1}{4\delta}}}$

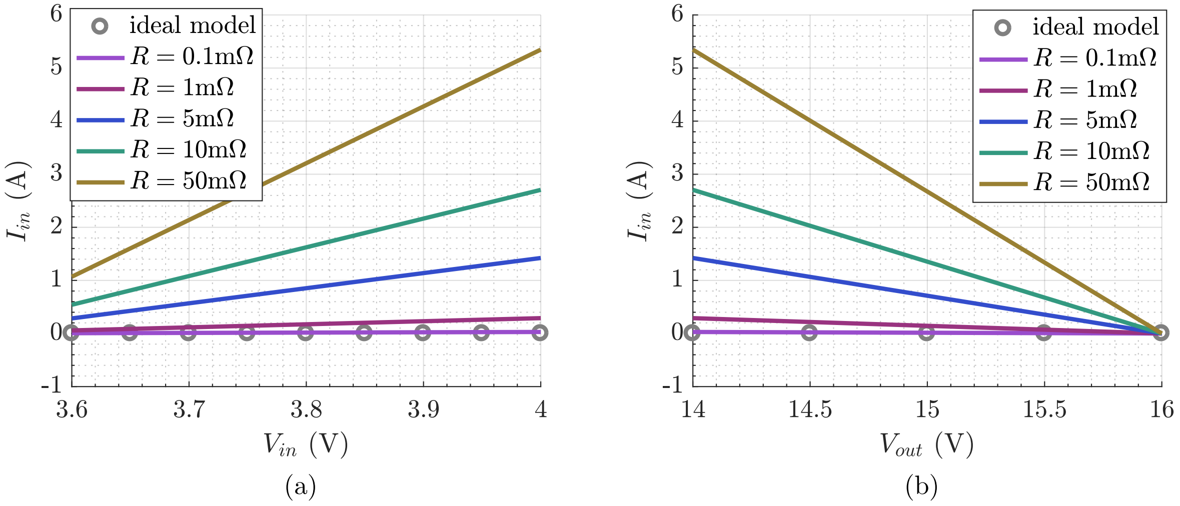


Figure 3.11: Steady-state DAB characteristics based on the improved model in Eq. (3.7) with different tank resistance R: (a) I_{in} vs. V_{in} ($t_\varphi = 0\,\text{ns}$, $V_{out} = 14.0\,\text{V}$); (b) I_{in} vs. V_{out} ($t_\varphi = 0\,\text{ns}$, $V_{in} = 4.0\,\text{V}$). DAB parameters are as shown in Table 3.2.

From Eq. (3.7), it follows that dc current at each port of the converter is always proportional to the voltage at the same port, with the slope decided by the conduction loss parameter R and the tank coefficient δ. Given the tank inductance value in Table 3.2, the input current as a function of input and output voltage with loss resistance R as a parameter is shown in Fig. 3.11. In addition, the new steady-state model Eq. (3.7) is also able to predict the fact that when φ is such that $f_i(\varphi) < 1$, the input current becomes inversely proportional to the output voltage, as exemplified in the experimental results of Fig. 3.4 (b). One may note remarkably strong dependence of steady-state characteristics on conduction losses, even when R is relatively small.

Eq. (3.7), which provide a more accurate steady-state model for a DAB converter, are more complex and not easily applicable in design. Unlike the simple form of the ideal steady-state equations in Eq. (3.1), variables and parameters in Eq. (3.7) are highly coupled and dependences are not easily observed. Intuitively, when the tank inductance is large enough, i.e. when δ is large enough, the ideal tank model and the simple steady-state equations in

Eq. (3.1) should provide an accurate approximation for the converter characteristics. In the limit, when conduction loss resistance tends to zero, the improved model Eq. (3.7) should reduce to Eq. (3.1). The objective of the analysis that follows is to simplify Eq. (3.7) to an approximate form better suited for design purposes, and to allow more intuitive interpretation of dependence in the DAB converter steady-state characteristics.

In Eq. (3.1), the steady-state input and output currents are second-order functions of the phase-shift φ. In order to bring Eq. (3.7) to a similar form, Taylors series expansion is applied to Eq. (3.7):

$$I = f(0) + f'(0)\varphi + \frac{f''(0)}{2!}\varphi^2 + ... \tag{3.8}$$

Taking only the first three terms into account, and neglecting higher order terms, an approximate form of the improved model Eq. (3.7) is obtained in Eq. (3.9), where the coefficients in the equations are defined in Table 3.4 and plotted in Fig. 3.12 as functions of the parameter δ. One may note that the approximation Eq. (3.9) to the improved model Eq. (3.7) has a form very similar to the simple ideal steady-state equations Eq. (3.1).

$$\begin{aligned} I_{in} &= \frac{V_{in}}{2\pi f_s L}K_0 + \frac{V_{out}}{2\pi n_T f_s L}(-K_0 + K_1\varphi - K_{2i}sign(\varphi)\frac{\varphi^2}{\pi}) \\ I_{out} &= \frac{V_{in}}{2\pi n_T f_s L}(K_0 + K_1\varphi - K_{2o}sign(\varphi)\frac{\varphi^2}{\pi}) - \frac{V_{out}}{2\pi n_T^2 f_s L}K_0 \end{aligned} \tag{3.9}$$

The coefficients K_0 decides how strongly the same-port voltage affects the port current. In the ideal model Eq. (3.1), $K_0 = 0$. With $K_0 \neq 0$, it should be noted that a phase-shift $\varphi = 0$ does not necessarily result in zero current. The power flow at $\varphi = 0$ can in fact be significant, as shown in Fig. 3.13. This may have important implications in the system design around the DAB converter. For example, start-up operation with the phase-shift initialized to zero may result in unexpected start-up dynamics. Furthermore, to limit the current in a DAB converter, a common approach is to set a limit for the phase-shift φ. However, if the limit is calculated based on Eq. (3.1), the actual current in the DAB converter may go well above the expected value.

Table 3.4: Parameters in the Simplified Improved DAB Steady-State Model

Parameter	**Value**
K_0	$2\pi\delta - 8\pi\delta^2 \frac{1-e^{\frac{-1}{2\delta}}}{1+e^{\frac{-1}{2\delta}}}$
K_1	$4\delta \frac{1-e^{\frac{-1}{2\delta}}}{1+e^{\frac{-1}{2\delta}}}$
K_{2i}	$(\frac{e^{-\frac{1}{4\delta}-sign(\varphi)\frac{1}{4\delta}}}{1+e^{\frac{-1}{2\delta}}})^{\|sign(\varphi)\|}$
K_{2o}	$(\frac{e^{-\frac{1}{4\delta}+sign(\varphi)\frac{1}{4\delta}}}{1+e^{\frac{-1}{2\delta}}})^{\|sign(\varphi)\|}$

The coefficient K_1 affects dynamic characteristics of the DAB converter. Using the ideal model in Eq. (3.1), DAB control-to-current small signal gains are:

$$\begin{aligned} \frac{\hat{i}_{in}}{\hat{\varphi}} &= \frac{V_{out}}{2\pi n_T f_s L} \\ \frac{\hat{i}_{out}}{\hat{\varphi}} &= \frac{V_{in}}{2\pi n_T f_s L} \end{aligned} \tag{3.10}$$

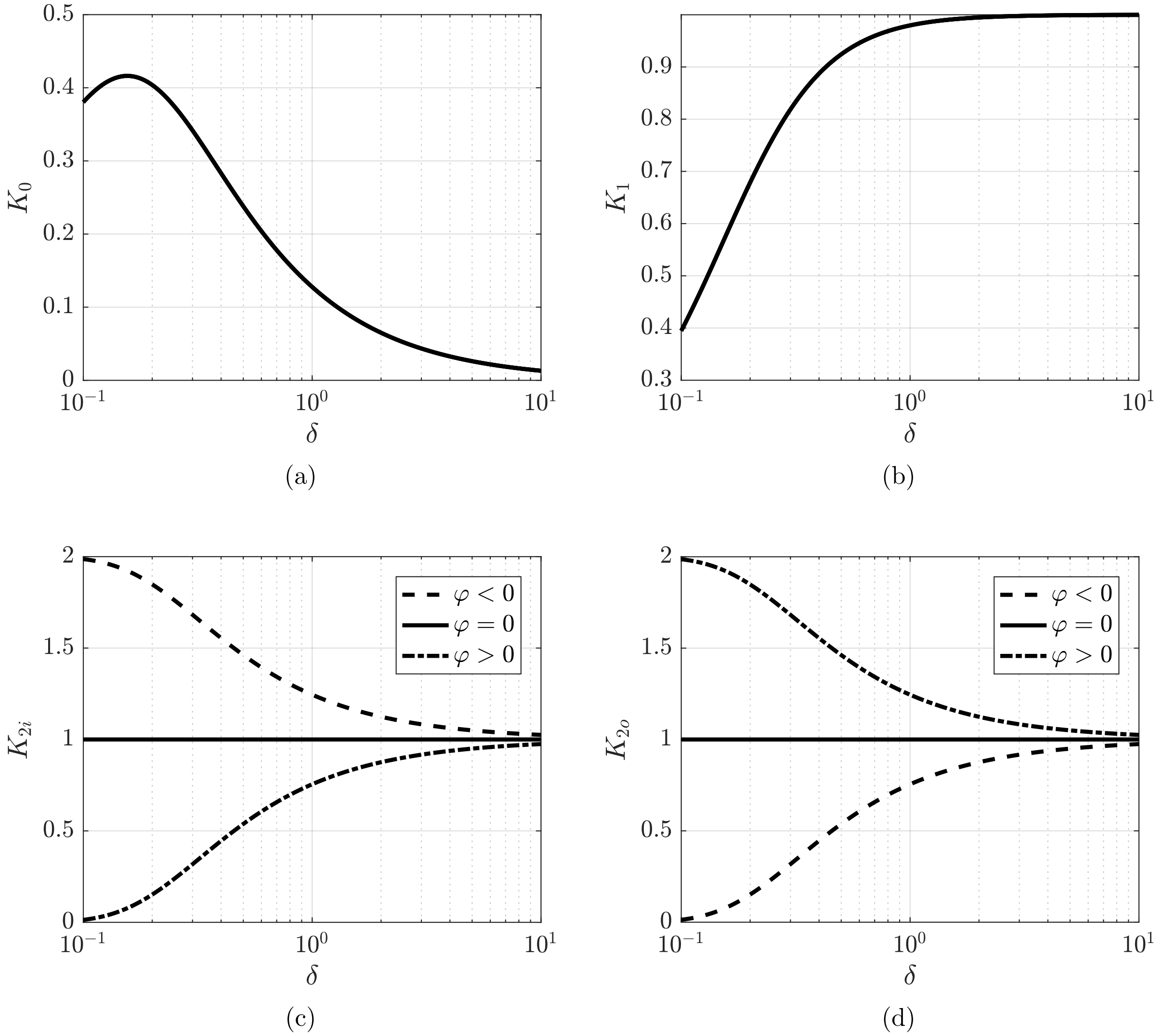
while the actual gains based on Eq. (3.9) are:

$$\begin{aligned} \frac{\hat{i}_{in}}{\hat{\varphi}} &= K_1 \frac{V_{out}}{2\pi n_T f_s L} \\ \frac{\hat{i}_{out}}{\hat{\varphi}} &= K_1 \frac{V_{in}}{2\pi n_T f_s L} \end{aligned} \tag{3.11}$$

A controller optimized based on the ideal steady-state model may not work well in practice if K_1 differs from 1 substantially.

When φ changes, K_2 varies in a range from 0 to 2, which has little impact on the design since the second-order term is usually much smaller than the first-order term.

Fig. 3.12 shows how δ affects the coefficients in Eq. (3.9). For an ideal tank, δ ap-



(a) (b)

(c) (d)

Figure 3.12: Coefficients for the simplified form of the improved DAB steady-state model in Eq. (3.9) as functions of δ: (a) K_0, (b) K_1, (c) K_{2i}, (d) K_{2o}.

proaches infinity. The coefficients in this case are as follows:

$$\begin{aligned}
&\lim_{\delta\to\infty} K_0(\delta) = 0\\
&\lim_{\delta\to\infty} K_1(\delta) = 1\\
&\lim_{\delta\to\infty} K_{2i}(\delta) = 1\\
&\lim_{\delta\to\infty} K_{2o}(\delta) = 1
\end{aligned} \tag{3.12}$$

and model Eq. (3.9) becomes exactly the same as the ideal steady-state equations

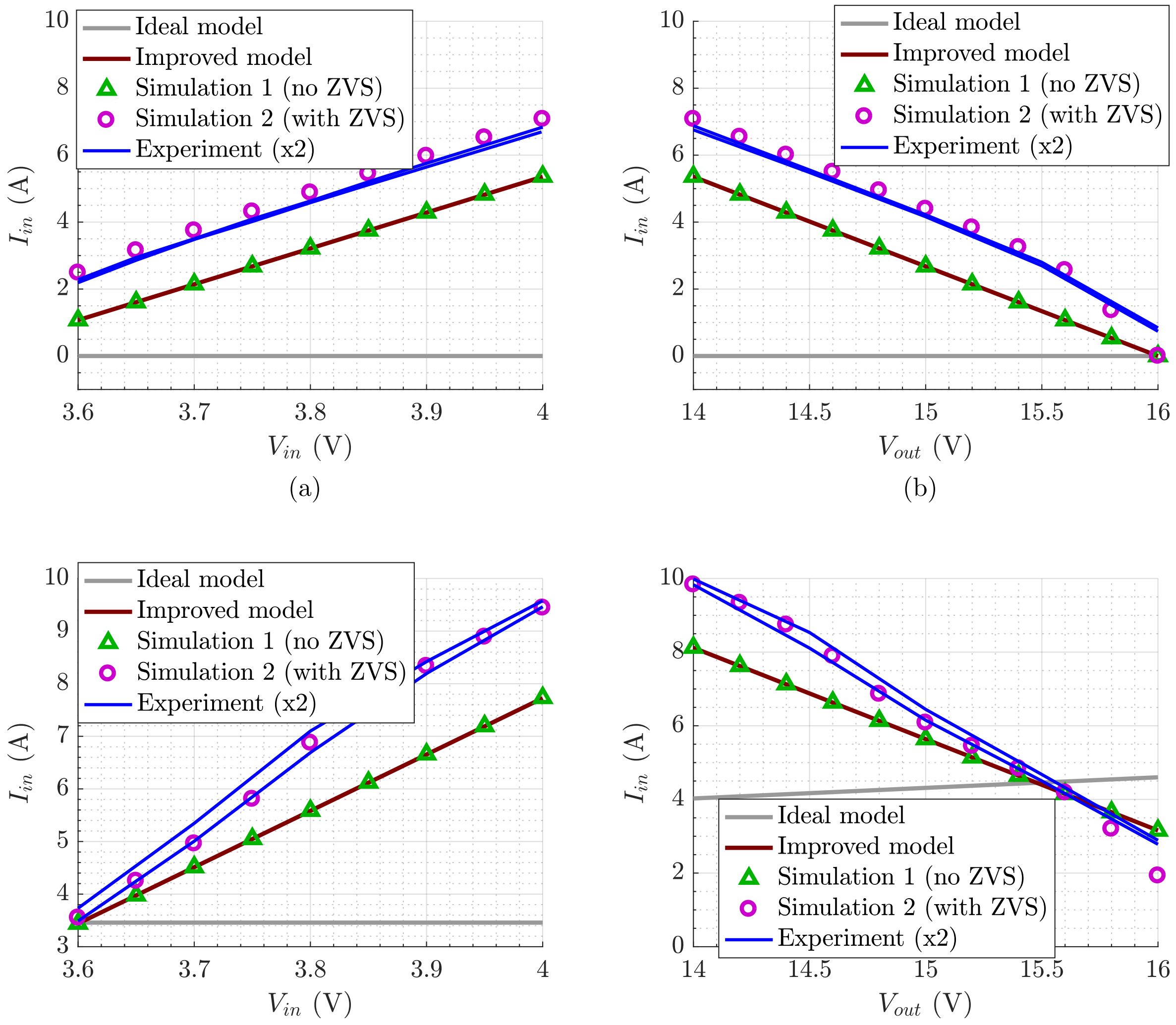
Eq. (3.1). To have a design where the ideal steady-state model can be considered accurate, δ should be sufficiently large. In other words, the equivalent series resistance R should satisfy:

$$R = \frac{L f_s}{\delta_{lim}} \tag{3.13}$$

where δ_{lim} is a minimum value of the tank coefficient δ, which may be decided based on the plots in Fig. 3.12.

3.3 Experimental Results

This section presents experimental results to verify predictions of the improved steady-state model developed in Section 3.2. The prototype and its corresponding controller are designed to maximize efficiency over an operating range. Furthermore, the series tank inductor consists only of the transformer leakage inductance. Since $\delta \approx 0.2$ in the experimental prototype, the steady-state characteristics are substantially different from the ideal. Two prototype boards have been tested and the testing results are shown in Fig. 3.13. While the ideal model Eq. (3.1) completely fails to match the experimental results, the improved model is able to correctly predict the observed proportionality between the port currents and port voltages. The errors observed can be attributed to the effects dead times, body diode conduction, and switching transitions have on the tank waveform and the resulting steady-state solution. In the prototype, fixed dead-times are applied for both the primary and the secondary side bridges, with zero voltage switching (ZVS) transitions obtained over most of the operating range. After the switch voltage crosses zero, it reverses polarity as the MOSFET body diode temporarily conducts until the MOSFET is turned on. The body diode forward voltage drop V_f in combination with the ZVS transition contribute to additional deviations of the inductor current waveform compared to the ideal, which further affects the steady-state characteristics.



(a) (b) (c) (d)

Figure 3.13: Comparison of the ideal model, the improved model, the simulation, and the experimental results with two prototypes: (a) I_{in} vs. V_{in} ($t_\varphi = 0\,\text{ns}$, $V_{out} = 14.0\,\text{V}$); (b) I_{in} vs. V_{out} ($t_\varphi = 0\,\text{ns}$, $V_{in} = 4.0\,\text{V}$); (c) I_{in} vs. V_{in} ($t_\varphi = 30\,\text{ns}$, $Vout = 14.0\,\text{V}$); (d) I_{in} vs. V_{out} ($t_\varphi = 35\,\text{ns}$, $V_{in} = 4.0\,\text{V}$). DAB parameters are as shown in Table 3.2.

3.4 Summary

In this chapter, it is shown that even small conduction losses can have substantial effects on the dual-active bridge (DAB) dc characteristics, especially when the DAB tank inductance is relatively small. A new method is developed to derive the DAB steady-state equations, leading to an improved steady-state model, which correctly predicts DAB dc characteristics.

Furthermore, a simplified version of the improved steady-state model is derived, which has a form similar to the ideal model, and which shows how DAB dc characteristics depend on the tank coefficient δ defined as the ratio of the time constant $\tau = L/R$ and the switching period T_s, where R is a conduction loss resistance. In the ideal case, $R = 0$, $\delta \rightarrow \infty$, and the improved model reduces to the ideal DAB dc characteristics. It is shown how the ideal model fails to predict DAB dc characteristics, and that differences in model predictions compared to experimental results can be very large, especially in cases where the DAB series tank inductance is relatively small, i.e., when δ is relatively small. The improved model offers much better predictions of DAB dc characteristics and is validated by simulations and experimental results on the prototype DAB converter used in the modular battery management system.

Chapter 4

Microcontroller Implementation of Lithium-Ion Battery State-of-Charge Estimation

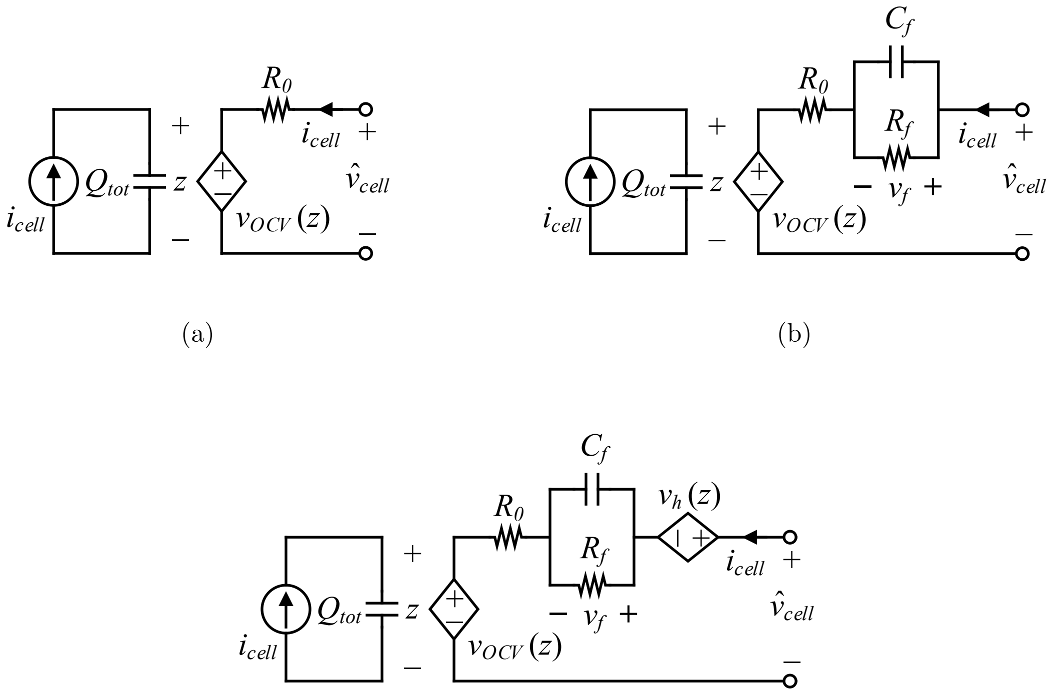
Chapter 2 and Chapter 3 discuss the system stability and the converter modeling of the modular BMS incorporating LV bus regulation. This chapter and the next chapter focus on lithium-ion battery state-of-charge (SOC) and state-of-health (SOH) estimation, respectively.

As introduced in Chapter 1, lithium-ion battery packs are widely used in electric and hybrid electric vehicles (xEV). A typical battery pack consists of a number of cells connected in series, which necessitates a BMS including passive or active cell balancing to fully exploit the cells and prolong the battery life [49,67]. Advanced battery management techniques rely on accurate state-of-charge (SOC) estimation. Various SOC estimation methods have been developed. Simple methods based on current measurement or voltage measurement are used in consumer and portable electronics. The current measurement based method is also referred to as Coulomb counting, in which the battery charge is computed by integrating measured current. While the method provide relative accurate SOC calculation over a short time period, error accumulate due to limited sampling rate and resolution of current measurement and limited knowledge of the change of cell capacity over time. Another group of methods are based on cell voltage measurement, using the terminal voltage and a cell model to calculate cell open-circuit voltage (OCV) and then use OCV to predict SOC based on an $OCV(SOC)$ curve obtained by cell characterization. The voltage based methods are adversely affected by the fact that $OCV(SOC)$ curves of lithoum-ion cells are relatively flat over a wide range of SOC values so that small errors or noise in voltage sensing result in large SOC errors. Overall, simple methods based on only current or voltage measurements fail to provide accurate SOC estimation in the harsh xEV environment with noisy measurements, model uncertainties, and highly dynamic cycling.

To properly estimate SOC in xEV applications, more comprehensive methods employing both cell voltage and cell current measurements have been developed [8, 24, 33, 57–61]. Of particular interest are Kalman filter based approaches [57–61], which have demonstrated excellent performance. The Kalman filter based methods rely on accurate cell modeling. Higher order state-space models make it difficult for Kalman filter based methods to be practically implemented on a low-cost microcontroller. The objectives in this chapter are to develop a simplified Kalman filter estimator and to demonstrate practical implementation of the algorithm on the same microcontroller that performs control functions around the dc-dc converter in the modular cell balancing system shown in Fig. 1.6 and further discussed in [13, 19, 67].

Each cell in the battery pack shown in Fig. 1.6 is connected to an isolated dc-dc converter operating autonomously. The controller around each converter relies on the SOC estimator to generate a control reference, as described in Chapter 2, and in [13, 19, 67].

Section 4.1 reviews three cell equivalent circuit models of varying complexity, together with corresponding discrete-time state-space models. Section 4.2 provides an introduction to SOC estimation using Kalman filtering, and benefits of the sigma-point Kalman filter (SPKF) are discussed. The proposed simplified 1st order SPKF approach is described in Section 4.3. The corresponding microcontroller implementation is presented in Section 4.4, together with experimental results obtained on a twenty-one cell pack based on the system shown in Fig. 1.6. The chapter conclusions are presented in Section 4.5.



(a)

(b)

(c)

Figure 4.1: Battery cell equivalent circuit models: (a) simple model; (b) RC model; (c) enhanced-self-correcting (ESC) model.

4.1 Battery Cell Modeling

The SOC estimation methods considered in this work are based on equivalent circuit models of battery cells. An equivalent circuit model is an electric circuit that models the relation between the cell terminal voltage and the cell current for a given state-of-charge (SOC) and temperature. It should be noted that cell equivalent circuit models are behavioral models, which attempt to reproduce the cell electrical characteristics. This section reviews three equivalent circuit models shown in Fig. 4.1 [27, 58].

Fig. 4.1 (a) shows a simple model, which consists of a dependent voltage source OCV in series with a resistor R_0. The dependent voltage source models the open-circuit voltage (OCV) of the cell, which is a function of the cell SOC, denoted as z, and temperature T.

Table 4.1: State-Space Forms for Different Cell Equivalent Circuit Models

Model	**Equations**	
Simple	State equation:	$z_k = z_{k-1} + \frac{T_i}{Q_{tot}} i_{cell,k-1}$
	Output equation:	$v_{cell,k} = v_{OCV}(z_k) + R_0 i_{cell,k}$
RC	State equation:	$z_k = z_{k-1} + \frac{T_i}{Q_{tot}} i_{cell,k-1}$ $v_{f,k} = e^{-\frac{T_i}{R_f C_f}} v_{f,k-1} + R_f(1 - e^{-\frac{T_i}{R_f C_f}}) i_{cell,k-1}$
	Output equation:	$v_{cell,k} = v_{OCV}(z_k) + R_0 i_{cell,k} + v_{f,k}$
ESC	State equation:	$z_k = z_{k-1} + \frac{T_i}{Q_{tot}} i_{cell,k-1}$ $v_{f,k} = e^{-\frac{T_i}{R_f C_f}} v_{f,k-1} + R_f(1 - e^{-\frac{T_i}{R_f C_f}}) i_{cell,k-1}$ $v_{h,k} = e^{-\frac{\lvert i_{cell,k-1}\rvert T_i \gamma}{Q_{tot}}} v_{h,k-1}$ $+M(1 - e^{-\frac{\lvert i_{cell,k-1}\rvert T_i \gamma}{Q_{tot}}}) sign(i_{cell,k-1})$
	Output equation:	$v_{cell,k} = v_{OCV}(z_k) + R_0 i_{cell,k} + v_{f,k} + v_{h,k}$

The OCV vs. SOC curve is different for cells of different chemistry, but is monotonically increasing in general. The OCV vs. SOC characteristics can be measured by cycling the cell at very low current rate at different temperature settings. The characteristic can be expressed in a formula by numerical curve fitting, or as a look-up table. In the model, the cell state-of-charge z, which is the only state in the model of Fig. 4.1 (a), is obtained by integration of the cell current i_{cell}.

In Fig. 4.1 (b), an RC filter is added to the circuit model, which introduces a new state variable v_f to the state-space equations. The RC filter models the diffusion effect in the terminal voltage and thus provides more detailed dynamics compared to the single resistor. The RC filter shown in Fig. 4.1 (b) describes the diffusion effect as a first-order process. A higher-order RC network can be added to model higher-order diffusion dynamics.

Fig. 4.1 (c) shows the enhanced self-correcting (ESC) model [58], including both the diffusion effect v_f and the hysteresis effect v_h in the cells terminal voltage.

Discrete-time state-space forms of the three aforementioned circuit models are shown in Table 4.1 [58]. In the state-space model, T_i is the sampling period, Q_{tot} is the cell total capacity, and z is the cell state-of-charge (SOC).

4.2 SOC Estimation Using Kalman Filter

State estimation is used in cases when the state variable of interest, such as a battery cell SOC, is not directly measurable. Given a system model in state-space form, consisting of a state equation and an output equation, Kalman filtering provides optimal estimation of the probabilistic mean and covariance of the state variables, with uncertainty in measurements and modeling taken into account as process noise ω and sensor noise v in the state equation and the output equation, respectively [30]. The process noise and the sensor noise are assumed to have zero mean.

4.2.1 Introduction to Kalman filter based SOC Estimation

There are two steps in the Kalman filter algorithm. In the first step, which is called a time update, the state vector x is updated using the state equation, in which the *a priori* estimate of the state vector $\hat{x}_k^-$ is a function of its previous *a posteriori* estimate $\hat{x}_{k-1}^+$ and the previous measured inputs u_{k-1}. The covariance matrix Σ_x of the state vector is also updated based on its previous value and the process noise covariance. In the second step, which is usually called a measurement update, the outputs of the system are found using the output equation and measurement. The error between the estimated and the measured outputs are used to correct the *a priori* estimate obtained in the time update using the Kalman filter gain K. The Kalman filter gain K is optimally calculated by minimizing the trace of the *a posteriori* estimation of the covariance matrix Σ_k^+ [57]. The basic Kalman filter algorithm

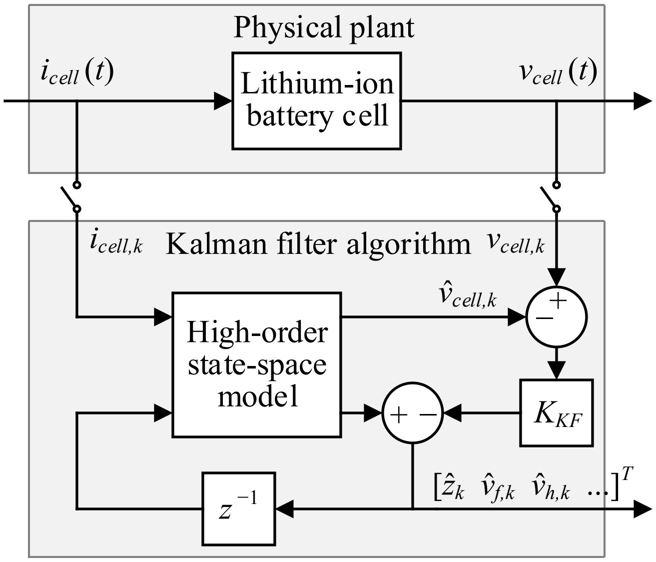


Figure 4.2: Kalman filter applied to a higher-order cell model.

is summarized in Table 4.2, where x is the vector of state variables, u is the vector of inputs, y is the vector of outputs, ω and υ are the process and the sensor noise, respectively, while Σ represent the corresponding covariance matrix.

The basic Kalman filter applies only to linear system models. Unfortunately, even the simplest cell model shown in Fig. 4.1 (a) is nonlinear, because of the nonlinear $OCV(z)$ characteristic. To apply Kalman filter to nonlinear models, an Extended Kalman filter (EKF) has been developed, with additional linearization steps in the algorithm, as shown in Table 4.3.

Consider the simple cell circuit model of Fig. 4.1 (a). In this case, there is only one state equation and one output equation. All the matrix calculations in the Kalman filter reduce to scalar equations. The state equation in this model updates $z = SOC$ by integrating the cell current, while the output equation describes the output voltage variation. In the EKF time update, the SOC estimate is calculated as:

$$\hat{z}_k^- = \hat{z}_{k-1}^+ + \frac{T_i}{Q_{tot}} i_{cell,k-1} \tag{4.1}$$

Table 4.2: Basic Kalman Filter Equations

Parameters:
State equation: $x_k = Ax_{k-1} + Bu_{k-1} + \omega_{k-1}$
Output equation: $y_k = Cx_k + Du_k + \upsilon_k$
State vector: $x_k = [x_{1,k}, x_{2,k}, ..., x_{n,k}]^T$
Input vector: $u_k = [u_{1,k}, u_{2,k}, ..., u_{l,k}]^T$
Output vector: $y_k = [y_{1,k}, y_{2,k}, ..., y_{m,k}]^T$
Process noise: $\omega_k = [\omega_{1,k}, \omega_{2,k}, ..., \omega_{m,k}]^T$
Measurement noise: $\upsilon_k = [\upsilon_{1,k}, \upsilon_{2,k}, ..., \upsilon_{m,k}]^T$
Time update:
$\Sigma^-_{x,k} = A\Sigma^+_{x,k-1}A^T + \Sigma_\omega$
$\hat{x}^-_k = A\hat{x}^+_{k-1} + Bu_{k-1}$
Measurement update:
$K_{KF,k} = \Sigma^-_{x,k}C^T[C\Sigma^-_{x,k}C^T + \Sigma_\upsilon]^{-1}$
$\Sigma^+_{x,k} = (I - K_{KF,k}C)\Sigma^-_{x,k}$
$\hat{y}_k = C\hat{x}^-_k + Du_k$
$\hat{x}^+_k = \hat{x}^-_k + K_{KF,k}(y_k - \hat{y}_k)$

which is the same equation that would be used in simple Coulomb counting. In the measurement update, the terminal voltage of the cell is estimated using the output equation:

$$\hat{v}_{cell,k} = v_{ocv}(\hat{z}^-_k) + R_0 i_{cell,k} \tag{4.2}$$

The terminal voltage is also measured and the error between the measurement $v_{cell,k}$ and the estimate $\hat{v}_{cell,k}$ is used to make a correction in the SOC estimate:

$$\hat{z}^+_k = \hat{z}^-_k + K_k(v_{cell,k} - \hat{v}_{cell,k}) \tag{4.3}$$

Correction in Eq. (4.3) effectively prevents accumulation of error commonly observed in simple Coulomb counting. It is well known that the simple model in Eq. (4.2) does not accurately represent the cell terminal voltage, especially when the cell is exposed to highly dynamic charging or discharging current. As a result, correction in Eq. (4.3) is compromised, which adversely affects performance of the estimator [7-9]. For better performance, the EKF

Table 4.3: Extended Kalman Filter Equations

Parameters:
State equation: $x_k = f(x_{k-1}, u_{k-1}) + \omega_{k-1}$
Output equation: $y_k = g(x_k, u_k) + \upsilon_k$
State vector: $x_k = [x_{1,k}, x_{2,k}, ..., x_{n,k}]^T$
Input vector: $u_k = [u_{1,k}, u_{2,k}, ..., u_{l,k}]^T$
Output vector: $y_k = [y_{1,k}, y_{2,k}, ..., y_{m,k}]^T$
Process noise: $\omega_k = [\omega_{1,k}, \omega_{2,k}, ..., \omega_{m,k}]^T$
Measurement noise: $\upsilon_k = [\upsilon_{1,k}, \upsilon_{2,k}, ..., \upsilon_{m,k}]^T$
Time update:
$\hat{A}_{k-1} = \dfrac{\partial f(x_{k-1}, u_{k-1})}{\partial x_{k-1}}\|_{x_{k-1}=\hat{x}^+_{k-1}}$
$\hat{C}_k = \dfrac{\partial g(x_k, u_k)}{\partial x_k}\|_{x_k=\hat{x}^+_k}$
$\Sigma^-_{x,k} = \hat{A}\Sigma^+_{x,k-1}\hat{A}^T + \Sigma_\omega$
$\hat{x}^-_k = f(\hat{x}^+_{k-1}, Bu_{k-1})$
Measurement update:
$K_{KF,k} = \Sigma^-_{x,k}\hat{C}^T[\hat{C}\Sigma^-_{x,k}\hat{C}^T + \Sigma_\upsilon]^{-1}$
$\Sigma^+_{x,k} = (I - K_{KF,k}\hat{C})\Sigma^-_{x,k}$
$\hat{y}_k = g(\hat{x}^-_k, u_k)$
$\hat{x}^+_k = \hat{x}^-_k + K_{KF,k}(y_k - \hat{y}_k)$

can be applied to more detailed, higher-order circuit models shown in Fig. 4.1 (b) and Fig. 4.1 (c). The EKF-based SOC estimation algorithm is summarized in the block diagram shown in Fig. 4.2. A further improvement, using the sigma-point Kalman filter (SPKF) is discussed next, based on [60, 61].

4.2.2 SOC Estimation using the Sigma-Point Kalman Filter (SPKF)

In the EKF, the model is linearized through Taylor series expansion under the assumption that the higher order terms are negligible. An improved approach for non-linear systems is the sigma-point Kalman filter (SPKF) [15]. Instead of linearizing the system under assumptions that may not be well justified, the SPKF keeps the non-linear form of the model as is. The SPKF algorithm begins with generating sigma-points of the state variables. Firstly, the state vector and the state covariance are augmented with the process noise and the sensor noise. The augmented state vector $\hat{x}^{a,+}_{k-1}$ is one of the sigma-points, while the rest of the sigma-points are generated by adding each column of the Cholesky decomposition of the augmented state covariance $\Sigma^{a,+}_{x,k-1}$ to the augmented state vector $\hat{x}^{a,+}_{k-1}$ (or subtracted from). This result in a sigma-point matrix $X^{a,+}_{k-1}$ in which each column is a sigma-point for the state vector. The sigma-points in $X^{a,+}_{k-1}$ are then mapped through the non-linear state equation and output equation, resulting in *a priori* estimation of the state and system output. The new *a priori* estimation of the sigma-points of the state vector are in matrix $X^{x,-}_{k,i}$ and those for the system outputs are in $Y_{k,i}$. These mapping results are then used to calculate the optimized Kalman filter gain K_k. Finally, the estimated mean and covariance of the state variables are the weighted mean and covariance of the new *a posteriori* estimation of the sigma-points. The SPKF algorithm is summarized in Table 4.4, and its very successful applications to SOC estimation using high-order cell models have been described in [60, 61].

4.3 1st-Order SPKF Approach Using Higher-Order Cell Model

An implementational challenge when using nonlinear Kalman filters is that both EKF and SPKF have computational complexity that scales with the cube of the number of states due to the required matrix operations. In SPKF, this includes the necessity of finding the Cholesky decomposition of the state covariance matrix in generating sigma-points. As a result, implementation of the SPKF based on a higher-order cell models is very challenging in the system shown in Fig. 1.6 where the bypass dc-dc controller is preferably based on a low-cost microcontroller. The implementation can be simplified by applying SPKF to the simple, 1st-order cell model of Fig. 4.1 (a), since all matrix computations then become scalar and thus the algorithm complexity is minimized. However, the performance is compromised by inaccuracies introduced by the simple model, as discussed in Section 4.2 4.2.1. The SOC

Table 4.4: Sigma-Point Kalman Filter (SPKF) Equations

Parameters:
State equation: $x_k = f(x_{k-1}, u_{k-1}, \omega_{k-1})$
Output equation: $y_k = g(x_k, u_k, \upsilon_k)$
State vector: $x_k = [x_{1,k}, x_{2,k}, ..., x_{n,k}]^T$
Input vector: $u_k = [u_{1,k}, u_{2,k}, ..., u_{l,k}]^T$
Output vector: $y_k = [y_{1,k}, y_{2,k}, ..., y_{m,k}]^T$
Process noise: $\omega_k = [\omega_{1,k}, \omega_{2,k}, ..., \omega_{m,k}]^T$
Measurement noise: $\upsilon_k = [\upsilon_{1,k}, \upsilon_{2,k}, ..., \upsilon_{m,k}]^T$
Generating sigma-points:
$\hat{x}^{a,+}_{k-1} = [(\hat{x}^{+}_{k-1})^T, (\bar{\omega})^T, (\bar{\upsilon})^T]^T$
$\Sigma^{a,+}_{x,k-1} = diag(\Sigma^{+}_{k-1}, \Sigma_{\omega}, \Sigma_{\upsilon})$
$X^{a,+}_{k-1} = [\hat{x}^{a,+}_{k-1}, \hat{x}^{a,+}_{k-1} + \eta(\Sigma^{a,+}_{x,k-1})^{\frac{1}{2}}, \hat{x}^{a,+}_{k-1} - \eta(\Sigma^{a,+}_{x,k-1})^{\frac{1}{2}}] = [(X^{x,+}_{k-1})^T, (X^{\omega,+}_{k-1})^T, (X^{\upsilon,+}_{k-1})^T]$
$X^{x,+}_{k-1} = [X^{x,+}_{k-1,0}, X^{x,+}_{k-1,1}, ..., X^{x,+}_{k-1,2n}]$
$X^{\omega,+}_{k-1} = [X^{\omega,+}_{k-1,0}, X^{\omega,+}_{k-1,1}, ..., X^{\omega,+}_{k-1,2n}]$
$X^{\upsilon,+}_{k-1} = [X^{\upsilon,+}_{k-1,0}, X^{\upsilon,+}_{k-1,1}, ..., X^{\upsilon,+}_{k-1,2n}]$
* $(\Sigma^{a,+}_{x,k-1})^{\frac{1}{2}}$ represent Cholesky decomposition
Time update:
$X^{x,-}_{k,i} = f(X^{x,+}_{k-1,i}, u_{k-1}, X^{\omega,+}_{k-1,i})$
$\hat{x}^{-}_{k} = \sum_{i=0}^{2n} W_{m,i} X^{x,-}_{k,i}$
$\Sigma^{-}_{x,k} = \sum_{i=0}^{2n} W_{c,i}(X^{x,-}_{k,i} - \hat{x}^{-}_{k})(X^{x,-}_{k,i} - \hat{x}^{-}_{k})^T$
Measurement update:
$Y_{k,i} = g(X^{x,+}_{k,i}, u_{k-1}, X^{\upsilon,+}_{k-1,i})$
$\hat{y}_k = \sum_{i=0}^{2n} W_{m,i} Y_{k,i}$
$\Sigma_{y,k} = \sum_{i=0}^{2n} W_{c,i}(Y_{k,i} - \hat{y}_k)(Y_{k,i} - \hat{y}_k)^T$
$\Sigma_{xy,k} = \sum_{i=0}^{2n} W_{c,i}(X^{x,-}_{k,i} - \hat{x}^{-}_{k})(Y_{k,i} - \hat{y}_k)^T$
$K_{KF,k} = \Sigma_{xy,k} \Sigma^{-1}_{y,k}$
$\hat{x}^{+}_{k} = \hat{x}^{-}_{k} + K_{KF,k}(y_k - \hat{y}_k)$
$\Sigma^{+}_{x,k} = \Sigma^{-}_{x,k} + K_{KF,k} \Sigma_{y,k} K^{T}_{KF,k}$

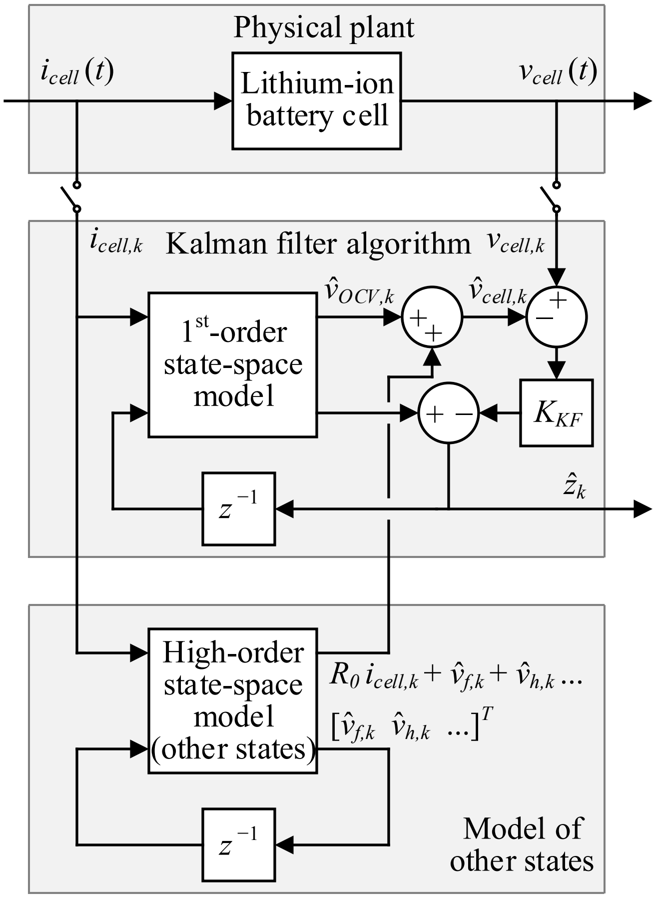


Figure 4.3: 1^{st}-order SPKF with high-order cell model.

estimates produced by this simple cell model of Fig. 4.1 (a) could be sufficient for balancing purposes, but a more detailed higher-order model should be considered when making SOC estimates for other purposes, e.g., calculating power and energy.

An improved method of simplifying the SPKF is introduced next. Considering the higher-order, more accurate models shown in Fig. 4.1 (b) and (c), it can be observed that the problem of accumulation of error in the state estimate is only associated with the $z = SOC$ state variable. The other state variables do not have such problem. For the diffusion voltage v_f and the hysteresis voltage v_h, Kalman filter may provide adequate accuracy without the correction step. The proposed improved, but still computationally simple approach is illustrated in Fig. 4.3, inspired by the fact that the full Kalman filter may not be essential in maintaining convergence of v_f and v_h estimation. In the new approach, a higher-order cell model, such as the model in Fig. 4.1 (b) or (c), including diffusion and hysteresis effects, is used only in the output equation in the SPKF algorithm. The SPKF algorithm only updates the SOC with its corresponding state equation and the output equation, while the rest of the state variables are updated outside the Kalman filter using the state equations only, without correction. Since the output equation in the higher-order models predicts the cell dynamics more accurately, the SOC estimation can be improved significantly. On the other hand, in the new approach, the SPKF algorithm is always of 1st order no matter what cell model is applied, which gives the designer the flexibility to increase or decrease state number while minimizing the computational effort.

4.4 Experimental Results

The improved 1st order SPKF algorithm shown in Fig. 4.3 is implemented on each microcontroller in the 21-cell battery pack of Fig. 4.4. The system parameters are shown in Table 4.5.

The microcontroller performs autonomous dc-dc converter controls, and LV bus voltage regulation, as described in Chapter 2 and in [13, 68]. The SPKF algorithm is programmed in C language, with different cell models shown in Fig. 4.1. The cycling of the battery pack is performed to record the cell voltages and cell currents. The recorded cell voltages and cell currents are then fed to the micro-controllers in each time step to emulate the on-line operation. In this way, SOC estimation experiments can be repeated several times using different algorithms, which allows comparisons of the performance of the improved 1st order SPKF algorithm using different cell models.

The testing current profile is shown in Fig. 4.5. The testing begins and ends with a constant charging at 1C rate (25 A). Discharging and charging based on US06 drive cycles occurs in between, with a peak current of 100 A.

Figure 4.4: 21-cell battery pack at Utah Power Electronics Lab, Utah State University.

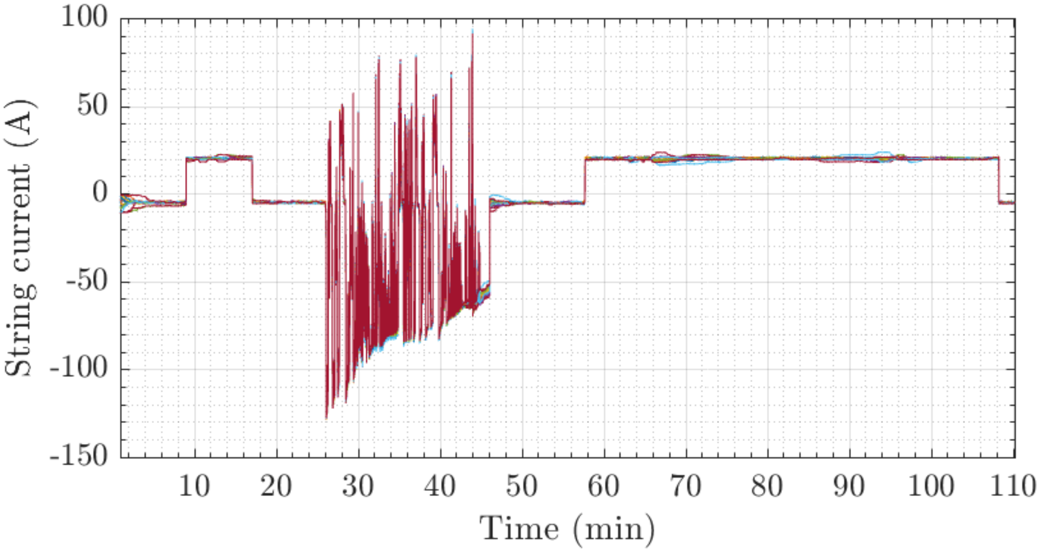


Figure 4.5: Battery cell current profile. Each color represents a different cell.

The true SOC of each cell is obtained by calibrated high-resolution Coulomb counting. The initial value is found by treating cells terminal voltage as OCV, which is acceptable since the pack is kept at rest for sufficiently long time before the start of cycling. The cell capacity

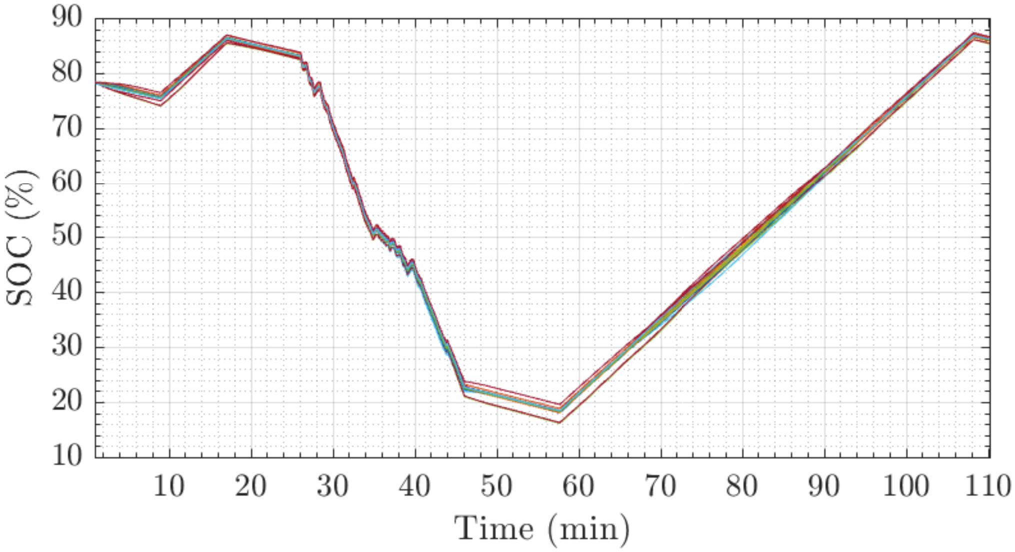
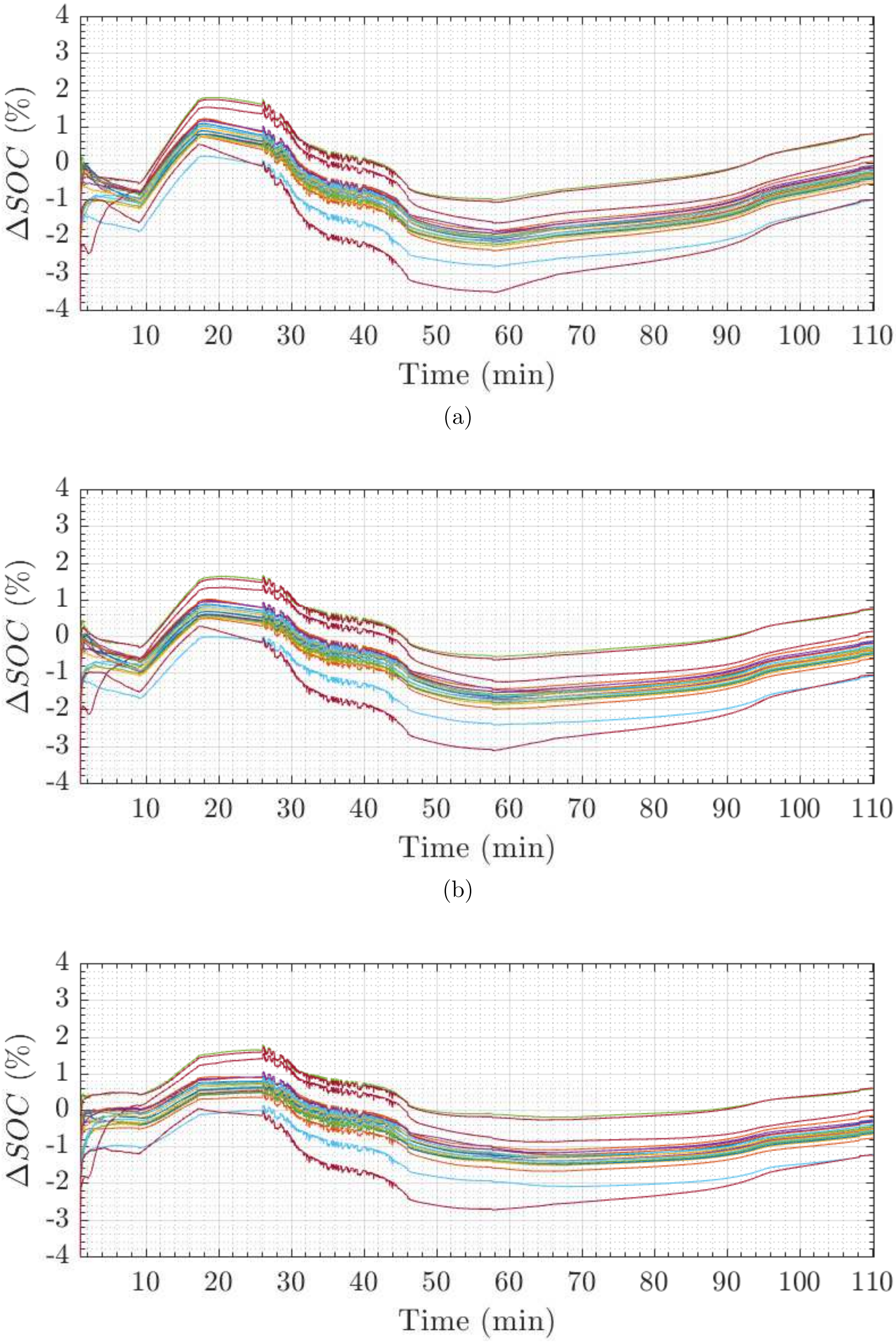


Figure 4.6: True SOC of each cell. Each color represents a different cell.

Table 4.5: Experimental Setup

Hardware Setup	
Microcontroller	TMS320F28027 (Texas Instrument)
Cell nominal total capacity	25 Ah
Cell initial SOC	≈ 78 %
1st-order SPKF Estimation Setup	
Updating period	1 second
Cell nominal total capacity	25 Ah
Initial SOC	30 %
Initial SOC standard deviation	20 %
Process noise (current) standard deviation	0.3 A
Sensor noise (voltage) standard deviation	50 mV

value is assumed to be the nominal capacity of the cell, while the true capacity of each cell varies in a range of less than 5 % around the nominal value. The true SOCs of the 21 cells are shown in Fig. 4.6. The 1st order SPKF SOC estimation values are recorded from each



(a)

(b)

(c)

Figure 4.7: Experimental results of 1^{st}-order SPKF SOC estimation errors: (a) simple model; (b) RC model; (c) ESC model. Each color represents a different cell.

microcontroller and compared to the true SOC. The differences are shown in Fig. 4.7 (a)-(c) for three different cell models used in the output equation in the improved 1st order SPKF based on Fig. 4.3. Fig. 4.7 (a) shows the results for the simple model: a maximum of 3.6 % SOC estimation error is achieved for all 21 cells. For most cells, the largest estimation error is around 2 %. Fig. 4.7 (b) and (c) show the testing results for the improved 1st order SPKF using the RC model and the ESC model, respectively. The maximum SOC estimation error with the RC model is 3.1 %, and for most cells the largest error is around 1.5 %. The maximum SOC estimation error with the ESC model is 2.6 %, and for most cells the largest error is around 1 %. In all cases, the complexity of the algorithm is low enough so that it can easily be implemented on the same microcontroller that performs dc-dc control and voltage regulation functions.

4.5 Summary

In this chapter, an improved 1st-order sigma point Kalman filter (SPKF) approach is proposed to perform real-time state of charge (SOC) estimation in battery packs with the modular active balancing system considered in this thesis. The method is practically implemented on a low-cost microcontroller that performs control and regulation functions around balancing dc-dc converters in the modular system. The approach is verified on a 21-cell battery pack cycled over a period of 120 minutes through realistic charge/discharge currents based on US06 driving cycles, with a peak current of 100 A. When applied in combination with the enhanced self-correcting cell model, the improved 1st order sigma-point Kalman filter (SPKF) yields a maximum SOC estimation error of 2.6 % for all of the 21 cells in the experimental prototype.

Chapter 5

Lithium-Ion Battery State-of-Health Estimation Using Long Term Aging Data

The change in lithium-ion battery performance over lifetime is often evaluated through battery state-of-health (SOH). There is no consensus on how SOH is defined. However, it is widely agreed that SOH is closely related to battery cell total capacity and inner cell resistance. Cell total capacity takes a significant part in SOH evaluation, and it also plays an important role in SOC estimation, as discussed in the previous chapter.

The total capacity of a cell is typically measured through a reference performance test (RPT). In RPT, the battery cell is fully charged and discharged. The total capacity is calculated by integrating cell current over a certain period. To make the integration as accurate as possible, the cycling current is kept constant. RPT requires certain equipment for battery cell cycling and measurement. It also takes long time to complete. While RPT is a good way to measure battery cell total capacity in research and lab experiments, it is difficult to apply RPT online in xEV applications. An xEV battery has large formation and requires much more energy for an RPT.

Online total capacity estimation, using data from daily driving, does not require critical testing conditions associated with RPT. However, the approach must deal with dynamics and noise present in the battery cell voltage and current. As the cell total capacity changes slowly over time, recursive-least-squre (RLS) based algorithms can be used to estimate total capacity in the noisy environment. The model used in capacity estimation is based on cell

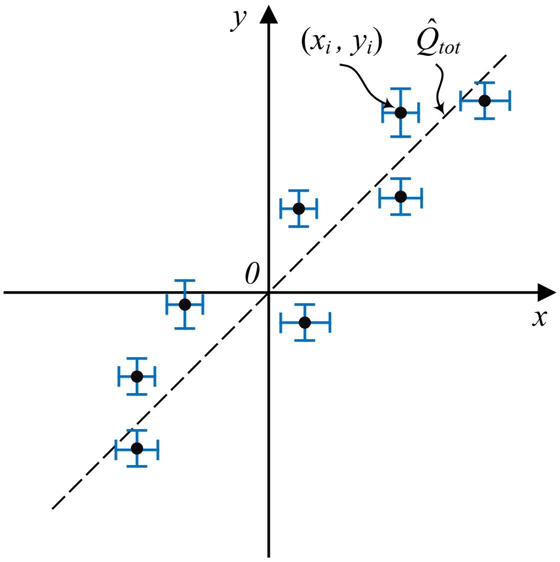


Figure 5.1: Curve fitting with weighted-total-least-square method.

current integration and SOC estimation:

$$y = Q_{tot}x \tag{5.1}$$

in which

$$\begin{aligned} x &\approx z_{end} - z_{start} \\ y &\approx \int_{t_{start}}^{t_{end}} i_{cell} dt \end{aligned} \tag{5.2}$$

z_{start} is the cell SOC at time t_{start}, z_{end} is the cell SOC at time t_{end}, and Q_{tot} is the cell total capacity to be estimated.

As both the current integration and the SOC estimation contain noise, weighted-total-least-square (WTLS) algorithm with both uncertainty in x and y taken into account, shown in Fig. 5.1, has demonstrated improved performance in capacity estimation [1,21,79]. However, it is difficult to implement the WTLS method in a recursive manner with reasonable computational effort.

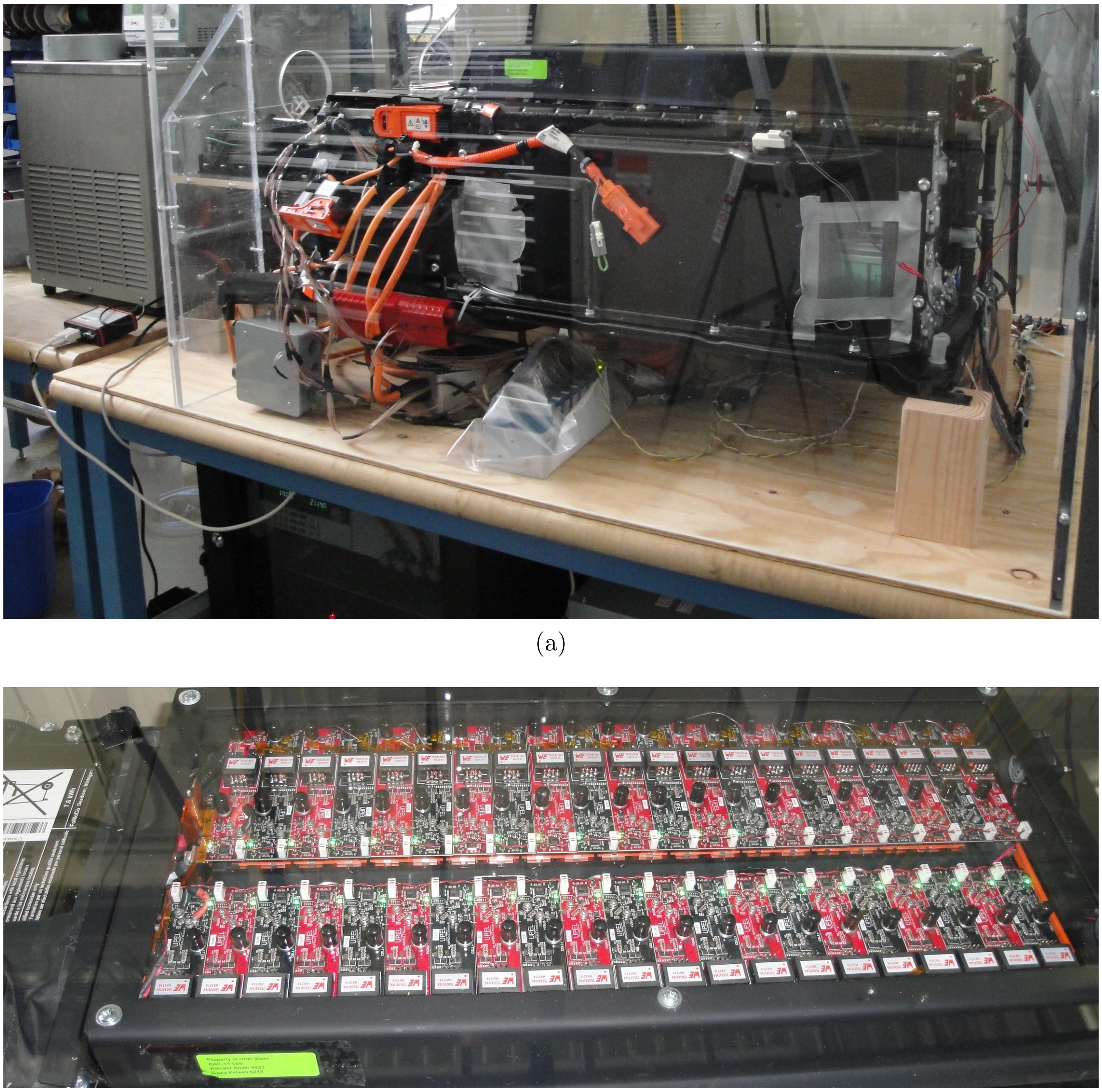
Two state-of-the-art WTLS based online total capacity estimation have been developed in [62] and [34], respectively. In [62], a recursive approximated weighted-total-least-square (RAWTLS) method is developed. The method significantly reduces the computational complexity, which makes it practical for implementation on low-cost microcontrollers. Inspired by the work in [62], [34] comes up with a Rayleigh-quotient based recursive total-least-square (RQ-RTLS) method, which improves speed of convergence, and computational complexity is reduced further.

This work examines the performance of the two state-of-the-art WTLS based online total capacity estimation methods described above. Section 5.1 describes the experimental setup and provides the estimation results, while Section 5.2 gives a summary of this chapter.

5.1 Experimental Results

Long term lithium-ion battery aging data is obtained from collaborators at the National Renewable Energy Lab (NREL) [77]. In the aging test at NREL, a modified commercial PHEV battery pack, shown in Fig. 5.2, with eighty-four cells underwent repeated daily cycles over a period of 15 months. The battery pack employed a standard passive balancing approach in one half of the pack, and the modular active balancing BMS described in Chapters 2-4 in the other half of the pack. Each half pack contains one quarter pack with new cells and another quarter pack with pre-aged cell. The battery pack configuration aims at verifying that the modular active balancing BMS is capable of controlling the degradation rate of individual cell SOH and thus significantly prolonging battery lifetime. In the daily aging cycles, the charge/discharge current patterns correspond to standard driving cycles. The cell voltages and cell currents are recorded every second. The RPT was performed every month to accurately measure the total capacity and inner resistance of each cell.

In this work, six cells in the half pack with modular active balancing BMS are selected to evaluate the online capacity estimation using RAWTLS and RQ-RTLS methods. Cells 2, 3, and 4 are in the quarter pack with new cells, and cell 25, 26 and 27 are in the quarter pack



(a)

(b)

Figure 5.2: The modified commercial PHEV battery pack tested at NREL, photos taken by Dr. Ying Shi: (a) entire battery pack setup; (b) modular active balancing BMS in one half pack. [77]

with pre-aged cells. The recorded cell voltages and cell currents of 9 months are shown in Fig. 5.3. 1st-order SPKF based SOC estimation is performed using the recorded cell voltages and cell currents. The SOC estimation was performed as discussed in Chapter 4. However, the process noise standard deviation is enlarged to further decouple the effects of the cell total capacity in SOC estimation. The SOC estimation setup is summarized in Table 5.1.

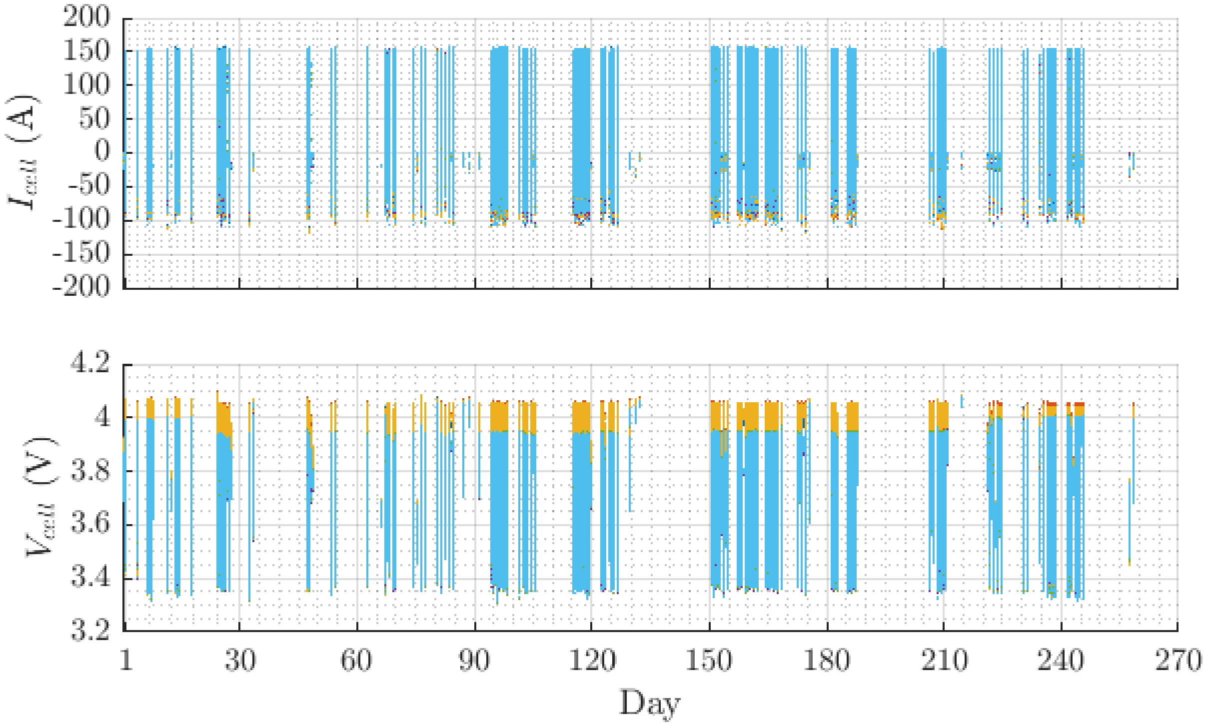
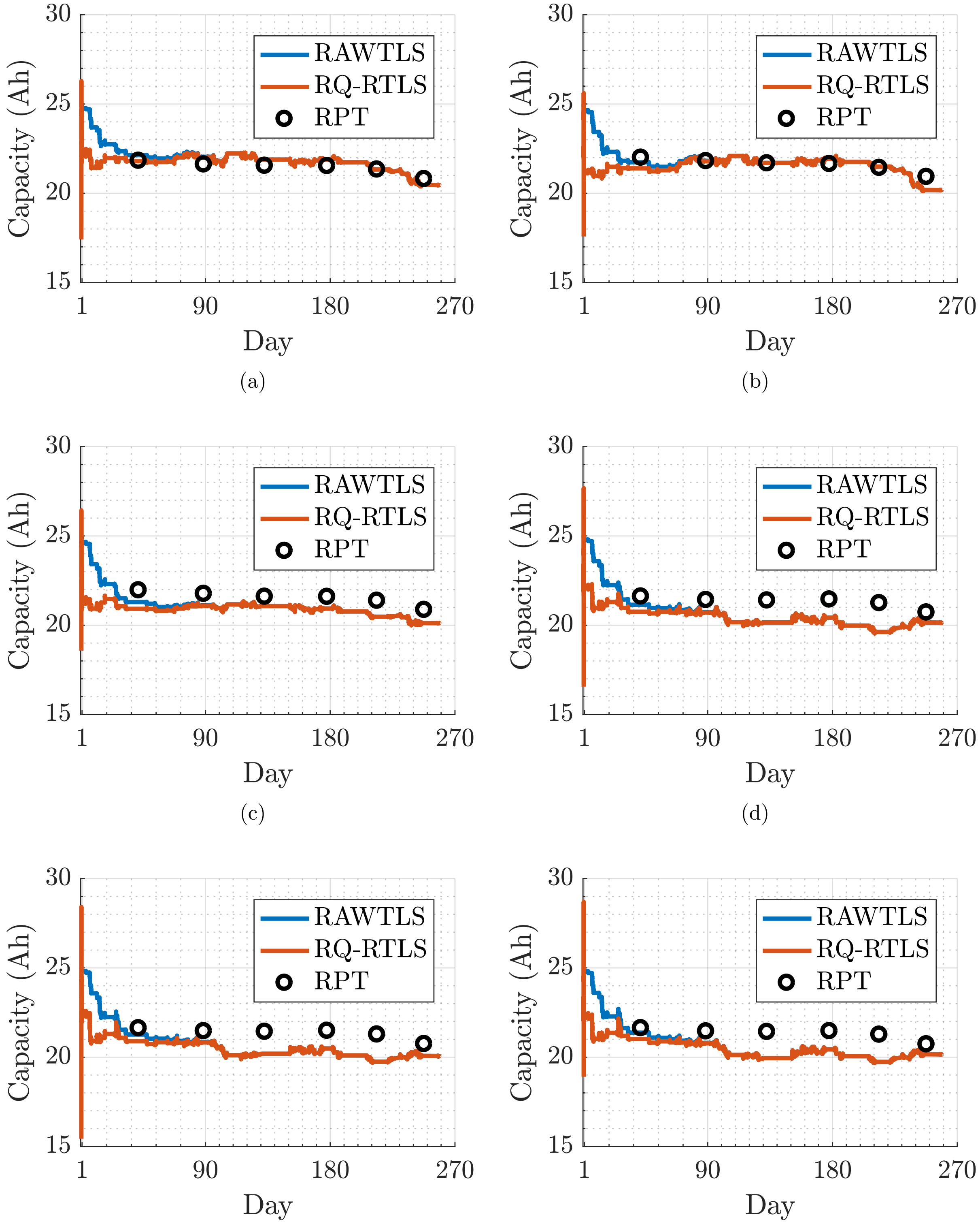


Figure 5.3: NREL lithium-ion battery aging data for 9 months. Cells 2, 3, 4, 25, 26, and 27 in the modular active balancing BMS are selected.

Table 5.1: SOC Estimation Setup

SOC Estimation Setup	
Method	1st-order SPKF
Updating period	1 second
Cell nominal total capacity	25 Ah
Initial SOC	based on cell terminal voltage
Initial SOC standard deviation	20 %
Process noise (current) standard deviation	10 A
Sensor noise (voltage) standard deviation	50 mV

The estimated SOC is used in total capacity estimation based on Eq. (5.1). The capacity estimation setup is summarized in Table 5.2.



(a) (b) (c) (d) (e) (f)

Figure 5.4: Total capacity estimation results (a) cell 2; (b) cell 3; (c) cell 4;(d) cell 25; (e) cell 26; (f) cell 27.

Table 5.2: Total Capacity Estimation Setup

Total Capacity Estimation Setup	
Method	RAWTLS and RQ-RTLS
Updating period	200 second
Initial capacity	25 Ah
Forgetting factor	0.999
Cell current noise standard deviation	0.3 A
Cell SOC noise standard deviation	5 %

The total capacity estimation results are shown in Fig. 5.4. The capacities estimated by RAWTLS and RQ-RTLS are represented by the blue and red lines, respectively, while the RPT measurements are shown as the black dots. The RAWTLS and RQ-RTLS results eventually equal to each other after a certain period. RQ-RTLS has a relatively higher convergence speed than RAWTLS, as expected. For cells 2 and 3 (in the quarter pack with new cells), the estimation results match very well with the RPT measurement. For cells 4 (in the quarter pack with new cells), 25, 26, and 27 (in the quarter pack with pre-aged cells), although the estimation results follow the battery cell degradation trend, there are mismatches between the estimation and the RPT measurements.

The experimental results demonstrate promising performance of RAWTLS and RQ-RTLS in a more practical scenario with a large quantity of cells under long term aging. However, the potential offset error deserves further investigation.

5.2 Summary

In this chapter, online capacity estimation algorithms are evaluated for lithium-ion battery cells tested in a 84-cell battery pack which underwent cycling tests over a period of 15 months, performed by collaborators at the National Renewable Energy Laboratory. Standard passive balancing was performed in one half of the pack, while the modular active balancing system considered in Chapters 2-4 was applied in the other half of the pack. Two state-of-the-art weighted-total-least-square (WTLS) based methods, RAWTLS and RQ-RTLS [34, 62], are examined based on the long term battery aging data of 9 months. The estimation results are compared with the measured cell total capacity from reference performance tests. The experimental results show that both methods are capable of successfully estimating cell total capacity. However, observed offset mismatches between the estimation results and the measurements for some cells deserve further investigation.

Chapter 6

Hybrid Balancing in a Modular Battery Management System

The previous chapters and [13, 67] discuss a modular active-balancing system with incorporated vehicle low-voltage (LV) bus, in which both active cell balancing and high-voltage-to-low-voltage (HV-to-LV) dc-dc conversion are achieved by a set of low-power, LV-to-LV isolated dc-dc converters. As the system eliminates the need for the high-power, HV-to-LV stepdown converter in a conventional power supply architecture shown Figure.6.1, the approach mitigates the cost penalty associated with active balancing.

In this chapter, the approach proposed in [13, 67] is further extended in the direction of finding the best trade-off between active-balancing benefits and the number of dc-dc converters. A modular BMS with hybrid balancing is proposed as shown in Fig. 6.2. The system reuses much of the hardware in a passive balancing BMS and thus significantly reduces the complexity and cost in development. Section 6.1 discusses the system concept and the hybrid balancing approach. Section 6.2 describes the modular BMS implementation, and Section 6.3 presents experimental results.

6.1 Hybrid Balancing Approach

In the hybrid modular system shown in Fig. 6.2, the battery cells in the battery pack are grouped into modules, each containing a subset of cells. Active balancing is applied at the module level by isolated dc-dc converters, while conventional passive balancing is applied at the cell level within a module. The module-level dc-dc converters combine to perform the

HV-to-LV conversion function.

6.1.1 Module-Level Active Balancing

Battery life extension is one of the most important benefits of active balancing in xEV applications. In a physically large xEV battery pack, inevitable temperature variations across the pack lead to uneven degradation among the cells, which is one of the major causes of shortened battery life. With specially designed active balancing algorithms enabled by the modular BMS considered in this thesis, up to 40 % battery life extension on a BEV75 (battery electric vehicle with 75 miles range) has been reported in [69]. The hybrid approach presented here is motivated by the fact that adjacent cells in a battery pack have much smaller temperature variations and thus degrade in a more uniform manner [78]. As a result, adjacent cells can be grouped into modules for module-level active balancing, while cell-level passive balancing can be performed within each module. Such system retains much of the life extension benefits of cell-level active balancing. On the other hand, as illustrated in the hybrid-balancing modular system shown in Fig. 6.2, the number of dc-dc converters required is significantly reduced compared to cell-level active balancing, leading to reduced overall hardware complexity.

6.1.2 Cell-Level Passive Balancing

While active balancing is performed at the module-level, ancillary passive balancing must be employed within each module using one of standard passive balancing algorithms [2,82,83]. Since the number of cells within a module is relatively small, as shown in Fig. 6.2, the cell-level passive balancing results in much lower energy dissipation compared to the conventional BMS with passive balancing applied across the entire battery pack shown in Fig. 6.1.

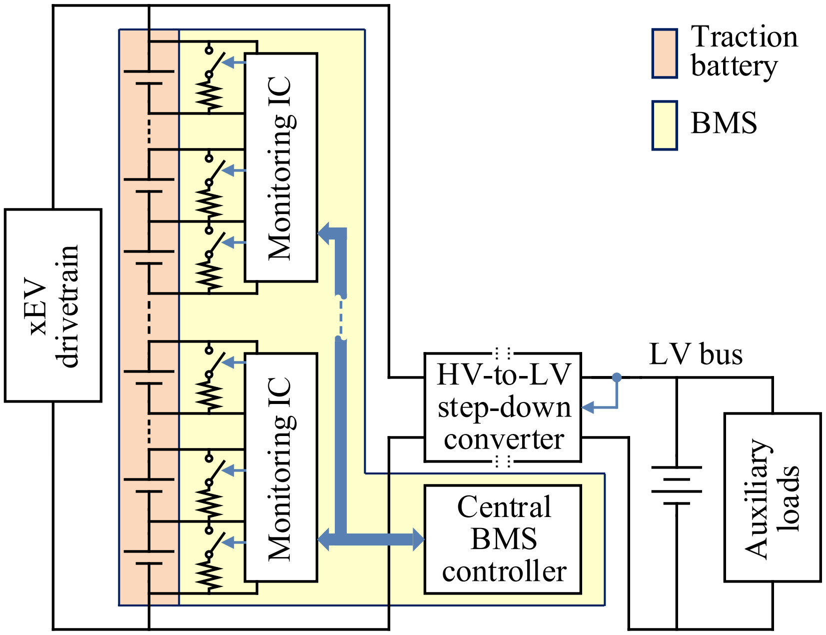


Figure 6.1: Conventional passive balancing system.

6.1.3 Module-Level SOC and SOH

Module-level state-of-charge (SOC) and state-of-health (SOH) must be known if active balancing is to be applied at the module-level. As noted in Chapters 4 and 5, a variety of advanced cell-level SOC and SOH estimation methods have been developed [2,62,69,82,83]. However, as the SOC and SOH are different from cell to cell in a module, extraction of module-level information must be carefully considered, especially during times when the cells within a module are not completely balanced by the slow passive balancing action.

As passive balancing is applied to the subset of cells in a module, the module SOH should be based on the worst-case cell within the module. The inner resistance and total capacity of Module i are given by Eq. (6.1) and (6.2), where n and j are the total number and the index of cells within a module.

$$R_{module,i} = n \cdot max(R_{cell,j}) \tag{6.1}$$

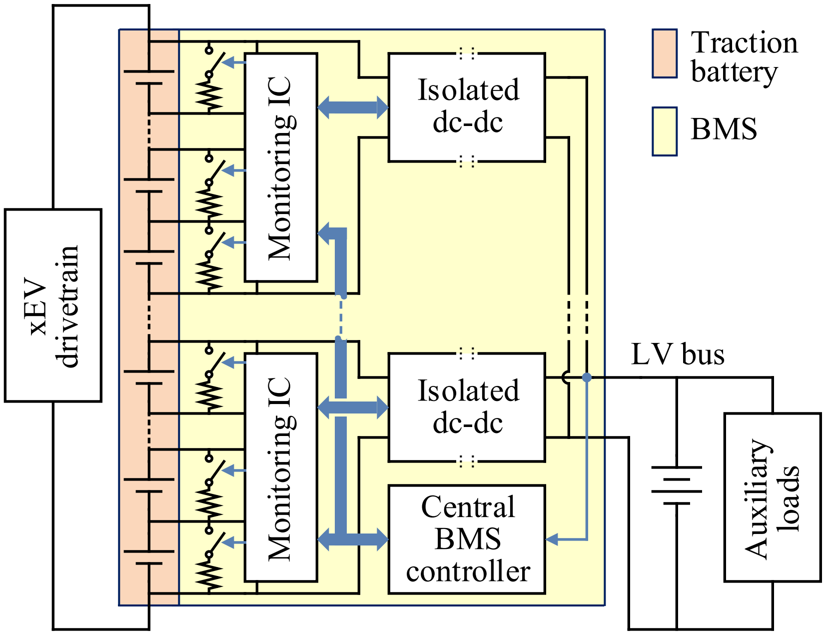


Figure 6.2: Modular system with hybrid balancing.

$$Q_{module,i} = min(Q_{cell,j}) \tag{6.2}$$

The calculation of module SOC requires more careful considerations. Suppose that the highest and the lowest cell SOC are $SOC_{max} > SOC_{min}$. If the module SOC is considered to be equal to the highest cell SOC (SOC_{max}), safety limits for the SOC_{min} cell may be violated during module discharging; similarly, if the module SOC is considered to be SOC_{min}, safety limits may be violated for the SOC_{max} cell during charging.

To properly accommodate different module-level active balancing schemes under different cell-level passive balancing conditions, the SOC of Module i is calculated as shown in Eq. (6.3),

$$SOC_{module,i} = \frac{min(SOC_{cell,j}Q_{cell,j})}{min(SOC_{cell,j}Q_{cell,j}) + min((1 - SOC_{cell,j})Q_{cell,j})} \tag{6.3}$$

When the cells in a module are balanced, $SOC_{cell,1} \approx SOC_{cell,2} \approx ... \approx SOC_{cell,n}$, and

Table 6.1: Comparison of Converter Specifications for An 84-Cell Lithium-Ion Battery Pack

	HV-to-LV step-down converter in the system of Fig. 6.1	**LV-to-LV modular converter in the system of Fig. 6.2**
Power-stage isolation	Yes	Yes
Stackable	No	Yes
Local controller	Current/voltage regulation	Current regulation
Input voltage	210 V - 350 V	15 V - 24.6 V
Output voltage	9 V - 16 V(12 V nominal)	9 V - 16 V(12 V nominal)
Converter power	6.7 kW max	480 W max
Converter quantity	1	14

Eq. (6.3) then becomes:

$$SOC_{module,i} \approx \frac{SOC_{cell,j} min(Q_{cell,j})}{SOC_{cell,j} min(Q_{cell,j}) + (1 - SOC_{cell,j}) min(Q_{cell,j})} \approx SOC_{cell,k} \tag{6.4}$$

where index k represents the cell with the least total capacity.

6.2 Modular Hybrid-Balancing System Implementation

The modular hybrid balancing system is shown in Fig. 6.2. Compared to the conventional system shown in Fig. 6.1, which includes a BMS and a HV-to-LV dc-dc converter as separate functional blocks, the modular hybrid-balancing system incorporates the LV dc output capability. The key change in the system architecture is that the original high-power, HV-to-LV stepdown converter is replaced by multiple low-power, module-level LV-to-LV dc-dc converters.

Table 6.1 compares the conventional system of Fig. 6.1 with the modular hybrid balancing system in Fig. 6.2 for the case when each module consists of six battery cells. Although the number of converters is higher, the LV-to-LV converters (referred to as modular converters in the rest of the chapter) have proportionally reduced power ratings, and employ only low-voltage components. In addition, the modular system can be easily adapted to different battery pack sizes. High-voltage high-power conversion can be achieved through stacking more modular converters.

The control architecture of the modular active-balancing system has been referred to in Chapter 2, and the particular version applied here is described in more detail in [70]. As shown in Fig. 6.4, each modular converter has a standard proportional-integral (PI) controller to accurately regulate its input current locally. The bus voltage compensator is implemented in the central BMS controller. The bus voltage compensator outputs a common current reference for the current loop in each modular converter. In addition to the voltage compensator, a delta SOC compensator runs simultaneously in the central BMS controller. The delta SOC compensator outputs differentiated current references to achieve module balancing.

The modular converter adopts dual-active-bridge (DAB) for the power-stage. The measured converter prototype efficiency as a function of power is shown in Fig. 6.3. Maximum measured efficiency is 95 %. Efficiency remains higher than 94 % for absolute values of output power down to 80 W or 17 % of the dc-dc module power rating.

Another significant advantage of the proposed hybrid system architecture is that the system can be constructed as an upgrade of a conventional BMS with passive balancing by reusing the majority of existing BMS functions in the conventional design, and by adding functions of module-level active balancing. These shared BMS features are further described in the following sub-sections.

6.2.1 Shared Battery Cell Measurements

In EV/HEV applications, cell-level monitoring is mandatory for battery pack state estimation and to ensure safe operation, regardless of whether passive or active balancing are employed. Typical measurements include cell voltage, cell current, and cell temperature. Cell voltage and cell temperature measurements are usually integrated into commercial battery

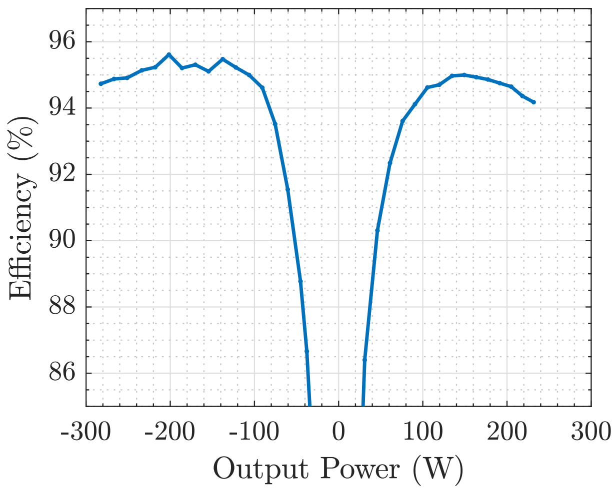


Figure 6.3: Efficiency of the dual-active-bridge (DAB) converter in the modular hybrid balancing system.

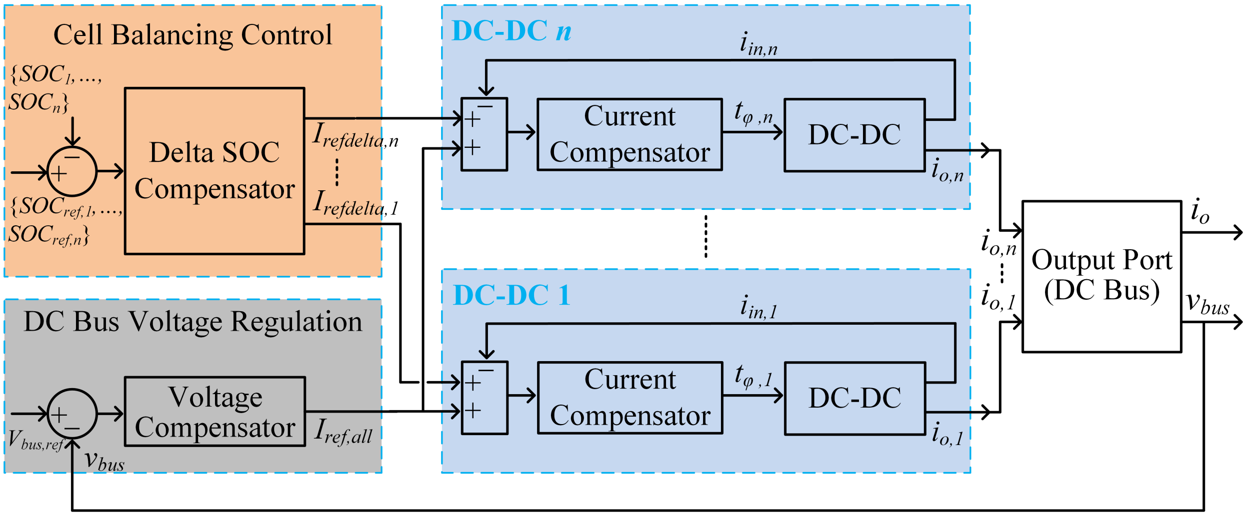


Figure 6.4: Control architecture for the active balancing system. [70]

monitoring ICs. Cell current is usually calculated by adding up the string current and the passive balancing current. The string current is centrally measured, while the passive balancing current is derived by dividing cell voltage by the nominal passive balancing shunt resistance. These measurements are reused to achieve module-level active balancing in this work, without the need for any additional sensors.

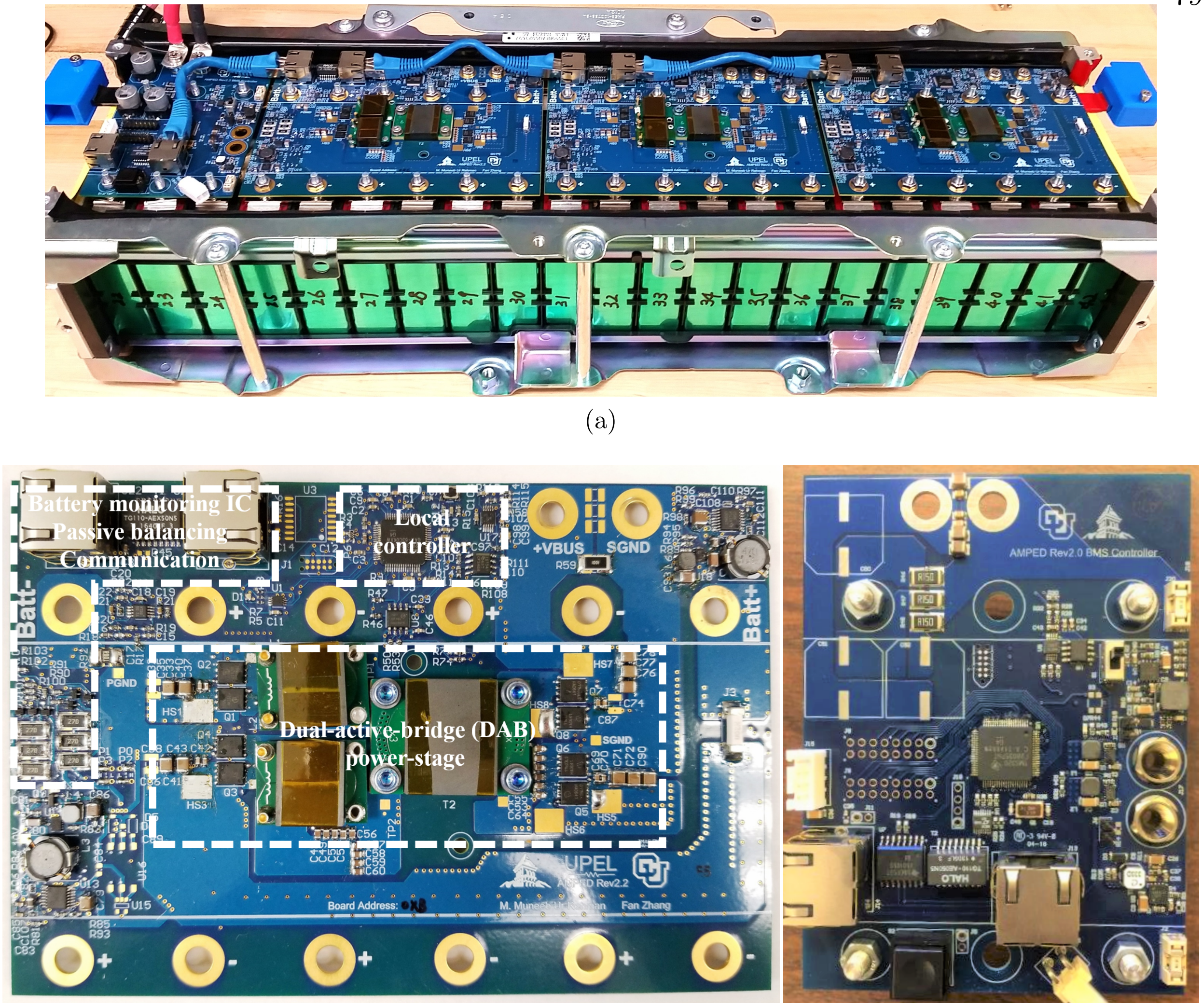
6.2.2 Shared Central BMS Controller

A conventional BMS with passive balancing typically operates with a central BMS controller and a number of battery monitoring ICs, as shown in Fig. 6.1. The central BMS controller collects cell information from the battery monitoring ICs, performs state-of-charge (SOC) and state-of-health (SOH) estimation, and runs necessary BMS algorithms including passive balancing. Typically, the BMS controller also extracts high-level battery pack information from the individual cells within the pack, and serve as an interface between the battery pack and a vehicle system controller. For the modular BMS with hybrid balancing, the active-balancing algorithms in [69, 70] can be integrated into the same central BMS controller within computational capability of the existing controller hardware. As shown in this work, the central BMS controller for the hybrid balancing system can be achieved using a low-cost micro-controller: TMS320F28035 (Texas Instruments).

Following the work described in Chapters 4 and 5, advanced SOC and SOH estimation are also implemented in the central BMS controller. A 1st-order sigma-point-Kalman-filter (SPKF) SOC estimation method of [60, 61] has been adapted to micro-controller implementation as discussed in Chapter 4 and in [86]. The method demonstrates a worst-case SOC estimation error of 1.5 % for twenty-one nickel-manganese-cobalt (NMC) Lithium-ion cells. The same method is applied to all eighteen pack cells individually. The inner resistance and capacity estimation methods are as described in Chapter 5, with reference to [60, 62].

6.2.3 Shared Communication Bus

In the conventional BMS with passive balancing, communication between the central BMS controller and the battery monitoring ICs is required to collect cell information and send necessary commands. Many commercial battery monitoring ICs have built-in functions for easy and robust communication. The IC used in this work, LTC6802-2 (Linear Technology) [44], also supports interface for one additional local device, which makes it possible to add



(a)

(b)

(c)

Figure 6.5: (a) 1.7 kWh modular hybrid system prototype assembled by collaborators at the Utah Power Electronics Lab; (b) modular LV-to-LV converter with battery monitoring IC; (c) central BMS controller.

the modular converters onto the already available communication bus without any additional hardware. To achieve the control algorithm developed in [70], a 16-bit time-critical control signal is broadcast to the modular converters every one millisecond, while all other necessary data are communicated at the rate of one second.

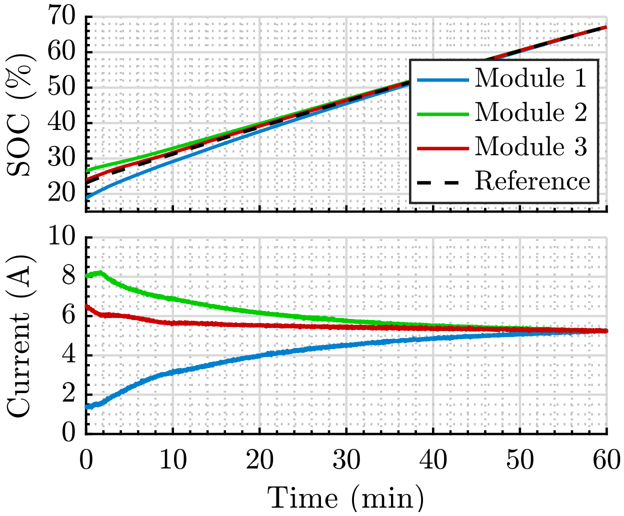


Figure 6.6: Module-level active balancing for 3 modules.

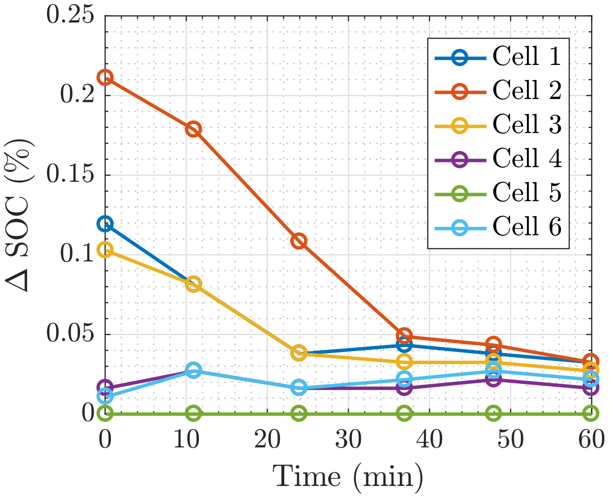


Figure 6.7: Cell-level passive balancing for the 6 cells within one module.

6.3 Experimental Results

The hybrid system is demonstrated on a battery pack that consists of eighteen 25 Ah NMC cells, grouped in three 6-cell modules, each including a dc-dc converter, as summarized in Table 6.1. The complete system is shown in Fig. 6.5 (a). The modular LV-to-LV converter and the central BMS controller are shown in Fig. 6.5 (b) and Fig. 6.5 (c), respectively.

In the experiment, active balancing is demonstrated on the three modules, while passive balancing is demonstrated on the six cells within each module. In the active balancing demonstration, the modules are charged from about 20 % SOC to 70 % SOC, with 8 % difference in SOC at the beginning. A constant current load is applied to the LV bus. The load is shared by the modular converters in such a manner that the module with higher SOC takes a larger share of the load. The resulting SOC and current waveforms of module-level active balancing are shown in Fig. 6.6. In the passive balancing demonstration, the cells with higher SOC dissipate energy through a 27 Ω per-cell shunting resistor — value selected to achieve average balancing speed of 0.5 % SOC per hour. The SOC convergence of cell-level passive balancing is shown in Fig. 6.7.

6.4 Summary

A hybrid modular battery management system with module-level active balancing and cell-level passive balancing is presented in this chapter. Module-level active balancing is performed by dc-dc converters, which simultaneously perform the high-voltage-to-low-voltage (HV-to-LV) dc-dc conversion required in electric-drive vehicles. Concepts for sharing BMS hardware resources for the active and passive balancing subsystems are described. The hybrid system features favorable cost/performance tradeoffs, and is capable of implementing a range of system and module-level control strategies. The system is experimentally demonstrated on a Lithium-ion battery pack, which consists of eighteen 25 Ah cells grouped in three 6-cell modules, each including a 480 W dc-dc converter simultaneously performing active balancing and supplying power to the vehicle 12 V LV bus.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This dissertation focuses on modeling, control, and design of a modular battery management system (BMS) using a series-input-parallel-output converter system incorporating both cell-level active balancing and low-voltage bus regulation in electric drive vehicles (xEV).

Stability of the system with autonomous control applied to cell-converter units is analyzed, and stability issues related to the state-of-charge (SOC) control loop are identified. The SOC loop and the bus voltage loop share the same proportional-integral (PI) compensator. The SOC loop bandwidth is much lower than the bus voltage control loop mainly due to the fact that the lithium-ion battery cell total capacity value is much larger than the capacitance at the converter output. As the PI parameters are designed for the bus voltage regulation, the SOC loop exhibits poor phase margin leading to instability and oscillating converter currents. A comprehensive analysis of the SOC loop is performed. The loop-gain transfer function is further simplified to second-order for simple SOC loop compensator design. The stability analysis leads to a droop-resistance approach, which results in stable system operation.

In the system prototype, the converter modules are based on the isolated dual-active-bridge (DAB) topology, controlled using phase-shift modulation. It is found that conventional DAB steady-state equations fail to model the low-voltage prototype converter in the system. A new DAB steady-state modeling method using superposition is developed. The new method makes it possible to directly visualize the DAB steady-state operating based on the switching waveforms. Based on the new method, an improved DAB steady-state model is derived, which takes into account conduction losses in the converter. The improved model successfully predicts the converter currents as functions of converter voltages and the phase-shift. Furthermore, a simplified form of the improved model decouples critical variables. Conditions are formulated in terms of the converter parameter values: the series tank inductance and the equivalent series resistance, which allow the designer to evaluate how well the conventional steady-state model represents the converter steady-state characteristics, and to employ the improved model if necessary.

In order to achieve autonomous control of cell-converter units, each unit in the system must estimate state-of-charge (SOC) of the corresponding lithium-ion battery cell. Sigma-point Kalman filter (SPKF) based SOC estimation has demonstrated excellent performance in xEV environments. This work significantly reduces the required computational complexity by introducing a simplified 1st-order SPKF SOC estimation method. With the simplified 1st-order SPKF, a high-order matrix computation becomes a simple scalar computation, which allows the method to be implemented on a low-cost micro-controller. The approach is tested on the prototype system with 21 cell-converter units using 25Ah Panasonic lithium-ion nickel-manganese-cobalt (NMC) cells.

In addition to SOC, state-of-health (SOH) estimation is also critically important in advanced BMS. Performance of two state-of-the-art online capacity estimation methods are examined using long term aging data obtained by prototype system testing performed at the National Renewable Energy Laboratory. The experimental results demonstrate performance of the two methods, and reveal the need to further investigate offset errors in estimated capacity values.

The modular BMS is extended in the direction of further reducing system complexity and cost. A hybrid balancing approach with module-level active balancing and cell-level passive balancing is introduced. Module-level active balancing aims at improving battery lifetime for modules with large temperature variation, while cell-level passive balancing targets aims at reducing system complexity and cost for cells with small temperature variation. A hardware prototype of the system is developed and demonstrated.

The work and the results reported in this thesis contributed to a multi-disciplinary project focused on robust cell-level modeling and control of large battery packs. Sponsored by ARPA-E AMPED program, the project was a collaboration between Utah State University (USU), University of Colorado Boulder (CU Boulder), University of Colorado Colorado Spring (UCCS), National Renewable Energy Lab (NREL), and Ford Motor Company. The results of this thesis were included in modeling, control, design and implementation of a large format prototype battery pack based on modifications of a commercial PHEV battery with eighty-four lithium-ion cells in series. The modular active balancing BMS was applied to a half pack with forty-two cells, while conventional passive balancing was applied to the other half pack for comparison. The modular active balancing BMS demonstrated potentials for significant improvements in battery lifetime, verified by a 15-month cycling and aging test performed at NREL. The prototype also demonstrated potentials for cost and size reduction achieved by elimination of a separate high-voltage-to-low-voltage (HV-to-LV) step-down converter in the conventional xEV architecture.

7.2 Future Work

The work presented in this thesis can be extended in several directions, including development of a system control architecture when the lead-acid battery is present on the low-voltage bus, evaluation of cost/performance trade-offs in the hybrid system architecture, further refinements of the SOC and SOH algorithms and their practical implementations, as well as full system evaluations in the xEV environment.

Investigation of other possible system architectures is another topic for future work. In particular, another modular BMS incorporating both active balancing and battery output

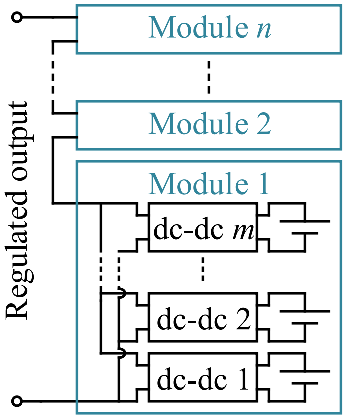


Figure 7.1: Modular BMS incorporating both active balancing and battery output voltage regulation.

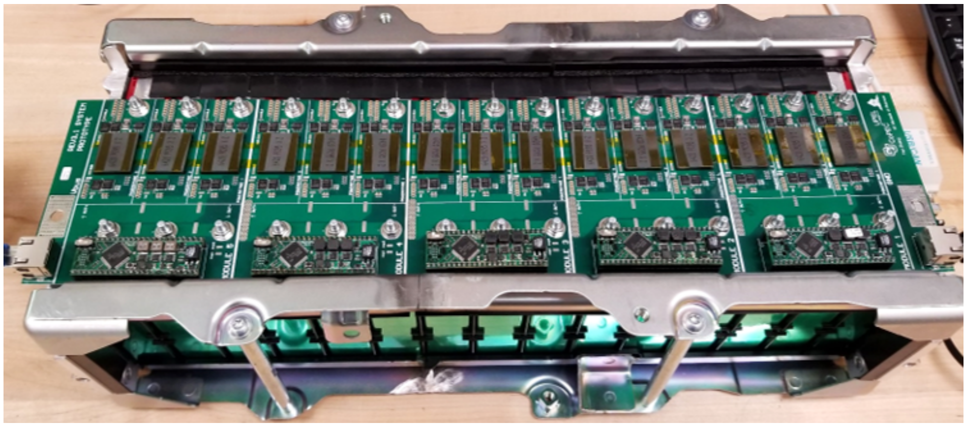


Figure 7.2: Hardware demonstration of the modular BMS incorporating both active balancing and battery output voltage regulation.

voltage regulation is shown in Fig. 7.1. In this system, which is well suited for dc microgrid applications, simple non-isolated converter such as the non-inverting buck boost converter can be used. Each converter processes the full battery current. A hardware prototype has been developed, shown in Fig. 7.2. Future work will include development of the system control architecture and evaluation of the system performance.

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