A Fast and Accurate GaN Power Transistor Model and Its Application for Electric Vehicle

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Abstract—In order to overcome the challenge of balancing accuracy with simulation speed of power electronics converters for system-level simulation, the paper proposes a GaN power transistor model that can accurately and rapidly predict power losses, which is suitable for system-level application such as an electric vehicle. The model is based on equivalent circuit and formed by behavioural equations to carefully model both conduction and switching losses. As a novelty, transistor power losses due to dynamic ON-state resistance is also included in the model. By comparison with experimental measurements and other available models of the similar type from the literature, it is shown that our model gives accurate results of the power losses and it helps to reduce the error by more than 70%. To accelerate simulation speed, power loss calculation and simulation time-step is decoupled. The power losses are represented in different levels and in the form of mathematical equations and look-up tables in MATLAB/Simulink. It is shown that our approach is able to reduce the simulation time by almost 18 times and maintain the same accuracy. The proposed GaN transistor loss model is finally implemented into a racing vehicle powertrain, where designers can obtain the power losses and temperature of the used power transistors in an easy and rapid way to optimise power electronics design.

Index Terms—Gallium nitride, Power conversion, Energy efficiency, Semiconductor device modeling, Systems simulation

I. INTRODUCTION

Power electronics converters with high efficiency and high-power-density play an important role for electro-mobility, as they can reduce the overall powertrain weight, battery size and extend the driving range [1], [2]. For this reason, wide bandgap power semiconductor devices based on Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming popular for this application. They can operate at higher temperature, higher frequency and higher efficiency than their silicon (Si) counterparts. Currently, power ratings of commercial GaN transistors are below 1.2kV and 150A, while that of SiC can reach above 1.2kV and 100A. Despite a mismatch of power, GaN is found to be more efficient than SiC due to lower device figure of merit ($R_{\mathrm{dson}} \cdot Q_{\mathrm{G}}$) [3]. Therefore, it is a good candidate for electric vehicle (EV) on-board application like battery charger, power converter and motor drive [4] as illustrated in Fig. 1.

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GaN is not yet a mainstream choice in on-board power electronics, which is still dominated by silicon today. However, as GaN transistors have twice lower resistance, four times higher operation temperature and ten times higher switching speed than silicon transistors [3], power converters can benefit from these superior characteristics to greatly improve the efficiency and power density. For instance, to name a few, ViSIC reported a 100 kW inverter design for motor drive [5]. Its peak efficiency can achieve 99.3% and the power density is 50 kW/L. GaN Systems reported a 7.2 kW EV on-board charger (OBC) and a 6 kW EV on-board DC-DC converter [6], [7]. The peak efficiency of the OBC can achieve 98.7%. The above data show a reduction of power losses and an increase of power density more than four times in comparison with silicon counterpart. In addition, it is worth noting that GaN has been proved to have better efficiency than SiC power transistors of the same power rating [8], [9]. Therefore, GaN will be a promising technology and popular choice in EV in the future. Despite a new technology with on-going reliability investigation, the recent reliability data summarised in [10] suggests that GaN transistors do not show a reliability issue that needs to be particularly concerned for EV application. The lifetime of the transistors is predicted to be at least 15 years when stressed at rated voltage and temperature of more than 125 °C.

EV on-board power electronics systems can be described, analyzed and designed on different levels concerning the regarded scale from components, circuits and their integration into the system level. Using simulation software is an effective way to rapidly design power electronics systems on each level. There are in general two requirements concerning the simulation model. One is the accuracy of the device characteristics such as power losses at component level, which affects the accuracy of circuit and system simulations. Another one is the simulation speed, which enables the possibility of benchmarking components and circuits under different system operation conditions in terms of efficiency. There are following approaches to model power semiconductor devices and losses:

1) Device compact model: The device compact model can be built on device physics or behavioural equations. Those models are usually operated at circuit-level in Spice simulation software. Modelling device switching transients, especially for GaN power transistors with switching transitions faster than 10 ns, requires fine simulation steps. If designers want to use device compact models in Spice simulation software for system-level simulation, such as a multilevel inverter, high computation time

and convergence may become a problem [11]. Designers can reduce the simulation time-step to accelerate the simulation speed, however, it would sacrifice the accuracy of switching loss estimation [12].

2) Look-up table: This approach is quite simple and suitable for system-level simulation software (e.g. MATLAB, PLECS). Nevertheless, it does not include device physics and therefore does not take into account device non-linear characteristics and the effect of parasitic elements [13]. To improve accuracy, designers need to edit additional look-up tables to include device losses for various operation parameters such as voltage, current, temperature etc., which requires additional computation and parametrization effort.

3) Analytical equations: These equations are usually satisfactory when the device is modulated under sinusoidal PWM. This model approach does not represent other modulation strategies [14], and it usually neglects the influence of junction temperature.

As switching frequency of GaN power converter is towards MHz range, device power losses during deadtime [15] and due to current collapse [16] can no longer be neglected. Still, they are not included in some of the existing models [11], [17]. Having an appropriate energy management strategy (EMS) for electric vehicles with multiple energy sources is important to extend the battery lifetime, driving range and reduce the size of the overall powertrain [18]–[20]. However, current EMS do not consider power converter losses and efficiency variation during a complete a driving cycle, which will bring mismatch with experimental results [20].

In order to overcome the above challenges, the paper proposes a fast and accurate modelling methodology of GaN power electronics converters. To validate the methodology, we choose electric vehicle as an application scenario in the paper, but it should be noted that the modelling methodology can be also easily applied into power electronics systems of different applications for transportation electrification, portable electronics and renewable energy systems. The model not only includes device conduction and switching losses and their evaluation with the temperature, but also accounts for the losses due to deadtime and dynamic-R_{dson}, which complements the existing models [11], [17]. Another advantage is the model can be easily applied to different simulation software at circuit-level and system-level, which overcomes the limitation of using models offered by manufacturers. The designers can obtain device power losses and temperature accurately and rapidly under different operation strategies. It should be noted that there are in general three types of the GaN transistors: high-electron-mobility-transistor (HEMT) with Schottky gate, gate injection transistor (GIT) and HEMT in cascode with Si-MOSFET [3]. In this paper, an enhance-mode GaN-HEMT with Schottky gate is modelled and analysed.

In comparison to our initial paper published in [21], there are following new contributions of this paper:

- A behavioural model of GaN transistor was proposed in section II-B of the paper. Both the conduction losses and switching losses are validated by experimental measure-
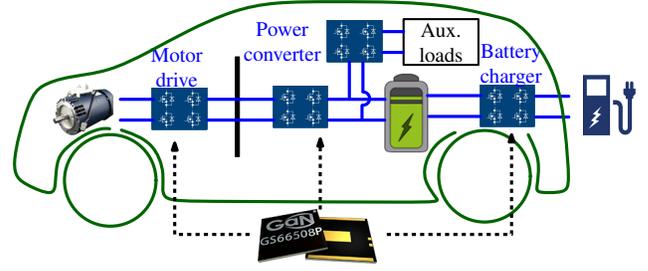

Fig. 1: Power electronics converters based on GaN transistors in EV [16].

ments in section IV-A.

- The model accuracy and simulation speed of the proposed multi-level loss model are analysed with more details to validate the modelling approach. The presented model also compares with other models from the literature to show the advantages in accuracy and simulation speed in section IV-B.
- The proposed GaN transistor loss model is implemented in a racing vehicle powertrain in section V, and both loss and temperature are obtained using real measurement data from a racing drive cycle.

The paper is structured within the following sections. At first, GaN power losses mechanism is described in details and a behavioural model is proposed. Afterwards, in order to represent different power losses mechanism, an N-level GaN transistor loss model is presented. The loss model is implemented into MATLAB. Following that, the accuracy and the simulation speed of both the transistor model and N-level loss model are experimentally validated. A case study to include the proposed model for an EV powertrain simulation is presented. The paper is concluded at last.

II. GaN Transistor Power Losses and Model

Half-bridge circuit formed by a high-side (HS) transistor and a low-side (LS) transistor with inductive or resistive-inductive load are one of the main circuit configurations used in power electronics converters. The half-bridge circuits can be used to form an inverter as motor drive, a rectifier as battery charger and DC-DC converter for low voltage battery powered vehicle auxiliary systems. The power losses obtained from the transistors of a half-bridge circuit can be easily extended to the above power converters, so it is focused on in the analysis of this section.

The power losses during one switching cycle in high-side and low-side transistor can be divided into conduction and switching losses. Conduction losses can be subdivided according to Fig. 2 into static-R_{dson}, dynamic-R_{dson} and deadtime conduction loss [22]. Switching losses are subdivided into C_{oss}- and VI-overlap loss. Similar to Si devices, GaN conduction losses occur in on-state due to the drain-source resistance R_{dson}, called $P_{\mathrm{cond}}^{\mathrm{on}}$, and in off-state during deadtime due to reverse conduction, called $P_{\mathrm{cond}}^{\mathrm{dt}}$. GaN shows an additional on-state loss mechanism, dynamic-R_{dson}, which is due to trapped electrons in the transistor. Those power losses are represented by $P_{\mathrm{cond}}^{\mathrm{dyn}}$. Switching losses can be
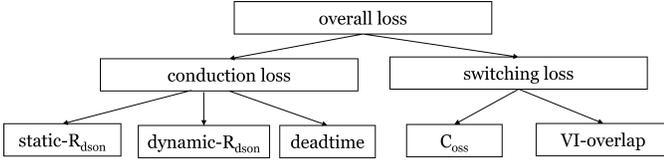
Fig. 2: Classification of loss mechanisms.

TABLE I: Loss mechanisms during switching cycle with positive load current.

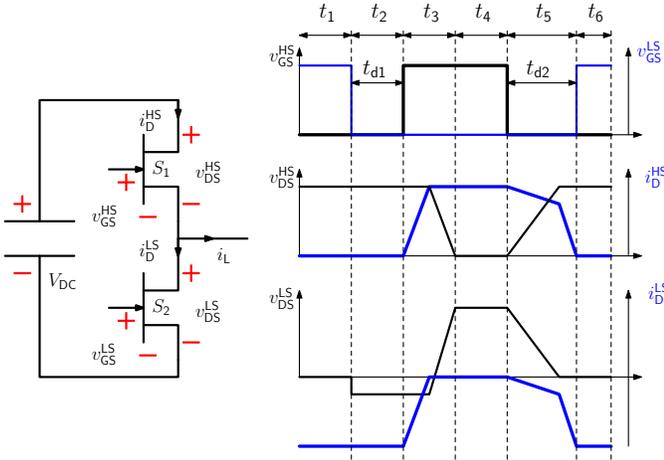|	t_1	t_2	t_3	t_4	t_5	t_6
HS	-	-	$E_{\text{sw-on}}^{\text{neg}}$	$P_{\text{cond}}^{\text{on}}+P_{\text{cond}}^{\text{dyn}}$	$E_{\text{sw-off}}^{\text{pos}}$	-
LS	$P_{\text{cond}}^{\text{on}}+P_{\text{cond}}^{\text{dyn}}$	$P_{\text{cond}}^{\text{dt}}$	$E_{\text{sw-off}}^{\text{neg}}$	-	$E_{\text{sw-on}}^{\text{pos}}$	$P_{\text{cond}}^{\text{on}}+P_{\text{cond}}^{\text{dyn}}$

Fig. 3: Device waveforms in a switching cycle with positive load current.

separated into capacitive losses E_{Coss}, due to the charging or discharging process of the output capacitance C_{oss}, and V-I overlap losses E_{VI}. Any power loss mechanism is largely dependent on the device characteristics, the gate-drive circuit and the layout of gate- and power-loop. Furthermore, the device junction temperature T_{J} influences the power losses. In terms of modelling, the change of power losses due to self heating of the device can be seen as an additional loss mechanism.

A. Power losses

1) Static-R_{dson}: Static-R_{dson} power losses occur in any switching cycle during on-state as long as the device is conducting current. The magnitude of $P_{\text{cond}}^{\text{on}}$ is mainly dependent on the drain current and the drain-source resistance (1).

$$P_{\text{cond}}^{\text{on}} = i_{\text{D}}^2(t) \cdot R_{\text{dson}}(i_{\text{D}}, T_{\text{J}}) \tag{1}$$

Referring to the switching cycle with positive load current, shown in Fig. 3, $P_{\text{cond}}^{\text{on}}$ for the low-side transistor occurs during t_1 and t_6. Table I shows an overview of the occuring loss mechanisms during one switching cycle. Even though, $v_{\text{GS}}^{\text{HS}}$ reaches on-state in the beginning of t_3, $P_{\text{cond}}^{\text{on}}$ occur only during t_4 after the switching transition is completed. For GaN, the switching time t_3 is in the range of ns. Therefore, compared to t_4, the switching time is mostly negligible.

2) Deadtime Conduction and Switching: $P_{\text{cond}}^{\text{dt}}$, E_{Coss} and E_{VI} are dependent on the type of switching transition. A switching transition includes always both transistors of a half-bridge circuit, of which one is turning-on and the other

turning-off. To distinguish switching transitions in a half-bridge with inductive load, the transistor conducting current before the switching transition is named as prior conducting transistor PCT. During t_1 the low-side transistor S_2 is turned-on and conducts a negative drain current which results in $P_{\text{cond}}^{\text{on}}$. For the following switching transition, S_2 is the negative current conducting PCT. After S_2 is turned-off, the deadtime t_{d1} starts. During t_2, S_2 still conducts the load current, which result in $P_{\text{cond}}^{\text{dt}}$. The switching transition is initialised by the turn-on signal of the high-side transistor S_1 and takes place during t_3. $v_{\text{DS}}^{\text{LS}}$ will not rise until i_{D}^{LS} reaches zero. In the first part of the transition, the fall of i_{D}^{LS} follows the trajectory of i_{D}^{HS}. After it, the rise of $v_{\text{DS}}^{\text{LS}}$ follows the trajectory of $v_{\text{DS}}^{\text{HS}}$. Therefore, no VI-overlap losses occur in the turning-off transistor S_2. As the switching transition is induced by the turning-on signal at the end of the deadtime, the turn-on energy $E_{\text{sw-on}}^{\text{neg}}$ and the turn-off energy $E_{\text{sw-off}}^{\text{neg}}$ are independent of deadtime. As Fig. 4 shows, $E_{\text{sw-on}}^{\text{neg}}$ is significantly larger than $E_{\text{sw-off}}^{\text{neg}}$. In this figure the energy refers to the actual power loss in the transistor and not to the external measured energy including the stored or released C_{oss} energy. After S_1 is turned-on, S_1 conducts the load current resulting in $P_{\text{cond}}^{\text{on}}$.

At t_5 (t_{d2}), for S_1, its drain current i_{D}^{HS} and $V_{\text{DS}}^{\text{HS}}$ voltage still have the same sign, which causes an overlapping during turn-OFF switching. For low side transistor S_2, its C_{oss} is discharged by load current i_{L} at this time, so i_{D}^{LS} and $V_{\text{DS}}^{\text{LS}}$ have different sign and the transistor is at soft switching. Therefore, if the deadtime t_{d2} is not sufficiently long or the inductive energy is not sufficiently big, the soft switching process of S_2 may not be complete and its remaining energy stored in C_{oss} will be lost in S_2 channel when it is switched ON at t_6.

Based on the above analysis, a complete soft switching should have two conditions: 1) drain current i_{D} and V_{DS} voltage should have different sign; 2) Inductive energy of the load and the deadtime should be sufficient.

The relation between t_{d2} and soft switching time t_{s} can be analysed by the equations below.

$$t_{\text{d2}} \geq t_{\text{s}} \tag{2}$$

The switching time t_{s} required for a soft transition is defined by:

$$t_{\text{s}} = \frac{2 \cdot Q_{\text{oss}}}{i_{\text{L}}} \tag{3}$$

Where Q_{oss} is the charge stored in the output capacitance of a transistor during off-state and L is the load inductance. In case of a deadtime greater than t_{s}, $P_{\text{cond}}^{\text{dt}}$ occurs in the turning-on transistor after the switching transition ended. If the
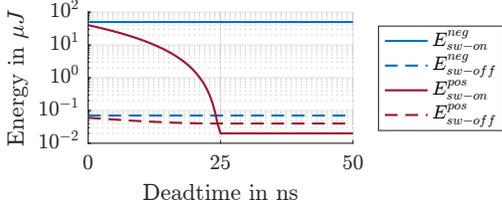
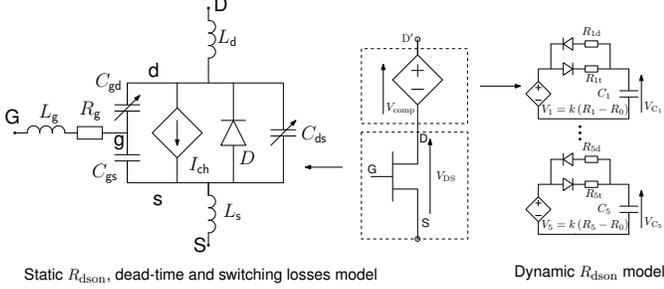Fig. 4: Switching and reverse conduction energies over deadtime.

Fig. 5: GaN Transistor Model Structure.

deadtime is smaller than t_s, a partially soft switching transition occurs and the residual Q_{oss} is lost in the transistor channel. The qualitative switching energies $E_{sw\text{-}on}^{pos}$ and $E_{sw\text{-}off}^{pos}$ over deadtime are shown in Fig. 4.

3) Dynamic-R_{dson} Loss: As static-R_{dson} losses, dynamic-R_{dson} power losses occur during device conduction period. Dynamic-R_{dson} power losses are dependent on the stress effects of the off-state blocking voltage amplitude and duration, turn-ON energy and gate voltage. Dynamic-R_{dson} will increase subject to the above stress effects. During on-state, charges are detrapping, which reduces the dynamic-R_{dson} value. The trapped charges influence not only conduction losses but also switching losses due to a shift of the threshold voltage [16]. However, as trapped charge increases conduction losses more than the switching losses, the impact on device switching characteristics is neglected here and will be studied in future.

4) Self Heating: The device temperature influences the carrier mobility and therefore the conductivity of the semiconductor. As a result of that, each power loss mechanism is dependent on temperature. Thus, self heating can be considered and modeled as an independent loss mechanism which scales the losses of other loss mechanisms.

B. GaN transistor model

In order to represent the above transistor power losses, a model shown in Fig. 5 is proposed. The model is formed by equivalent circuits with mathematical functions.

The circuits between terminals D, G and S are formed by a bi-directional current source I_{ch} to model channel current, which is represented by the equation that are adapted from Angelov GaN-HEMT model [23].

$$I_{ch} = I_{ch1} + I_{ch2}$$
$$I_{ch1} = a \cdot ln(1 + exp(\frac{V_{gs} - b}{c}))^e \cdot (1 + d \cdot V_{ds})$$
$$I_{ch2} = -a \cdot ln(1 + exp(\frac{V_{gs} - b - f \cdot V_{ds}^g}{c}))^e \cdot (1 + d \cdot V_{ds})$$
$$(4)$$

A diode is used to model reverse conduction characteristics, which is formed by a resistance R_s in series with a controlled current source I_s. The relation between I_s and its voltage drop V_{s1} can be represented by a classic p-n junction equation below [24]:

$$I_s = I_{s0} \cdot T_j^2 \cdot \left(exp \left(\frac{V_{s1}}{c_r \cdot (T_j + 273) \cdot \left(\frac{k}{q} \right)} \right) - 1 \right) \quad (5)$$

In the above equations, parameters a ($a = a_0 - a_1 \cdot T_j$), b ($b = b_0 - b_1 \cdot T_j + b_2 \cdot T_j^2$) and R_s ($R_s - b_r \cdot T_j$) are temperature dependent, and they can be modelled by a linear or a 2nd-order polynomial function.

Non-linear inter-electrode capacitances C_{ds}, C_{gd} and C_{gs} are modelled by tangent hyperbolic equations that are adapted from the model presented in [25].

$$C_{xy} = a_1 - b_1 \left(1 + \tanh \left(c_1 \left(V_{xy} + d_1 \right) \right) \right)$$
$$- e_1 \left(1 + \tanh \left(f_1 \left(V_{xy} + g_1 \right) \right) \right)$$
$$- h_1 \left(1 + \tanh \left(i_1 \left(V_{xy} + j_1 \right) \right) \right)$$
$$(6)$$

Therefore, power losses due to static R_{dson}, dead-time and switching losses can be modelled.

Dynamic resistance R_{DSon} is a special feature of the GaN transistor, which is due to trapped charges at GaN transistor buffer layer when transistor is at OFF-state. After suffering from certain stresses such as biased V_{DS} voltage, R_{DSon} will increase, which makes its value higher than device static R_{DSon}. When the biased voltage are removed and the device operates at ON-state, the trapped charges will recover, which lead to a decrease of R_{DSon} towards static R_{DSon} value. Therefore, both OFF-state time (t_{off}) and ON-state time (t_{on}) are important to influence on dynamic R_{DSon} value. To model this feature, the circuits connected between terminals D and D' are used. A compensation voltage V_{comp} equals to the sum of the capacitor voltage V_{C_i} of each cell. V_{comp} will increase with the bias voltage when device is in OFF-state and decrease towards zero when device is in ON-state. Therefore, conduction losses due to dynamic R_{dson} can be modelled. In each cell, voltage increase (τ_{off_i}) and decrease rate (τ_{on_i}) are modelled by a RC circuit to represent the lifetime of the trapped charge, which is from our previous work [26] and is given below.

$$R_{dson}(t) = \sum_{i=1}^{n} (R_i - R_0)(1 - e^{-\frac{t_{off}}{\tau_{off_i}}}) e^{-\frac{t_{on}}{\tau_{on_i}}} \quad (7)$$

A 650V/30A GaN-HEMT (GS-065-030-2-L) is modelled. The parameters in the above model are extracted by curve

TABLE II: Parameters used in the proposed model for GaN-HEMT forward I_{D}-V_{DS} characteristics.

Device	a_0	a_1	b_0	b_1	b_2	c	d	e	f	g
GaN-HEMT	0.023	10^{-3}	93.52	0.016	71.40	126.64	4.4×10^{-3}	1.54	0.27	8.8×10^{-4}

TABLE III: Parameters used in the proposed model for GaN-HEMT reverse I_{D}-V_{DS} characteristics.

Device	I_{s0}	R_{s}	c_{r}	b_{r}
GaN-HEMT	2.07×10^{-5}	0.099	8.19	2.07×10^{-5}

(a) I_{D}-V_{DS} characteristics

(b) Transfer characteristics
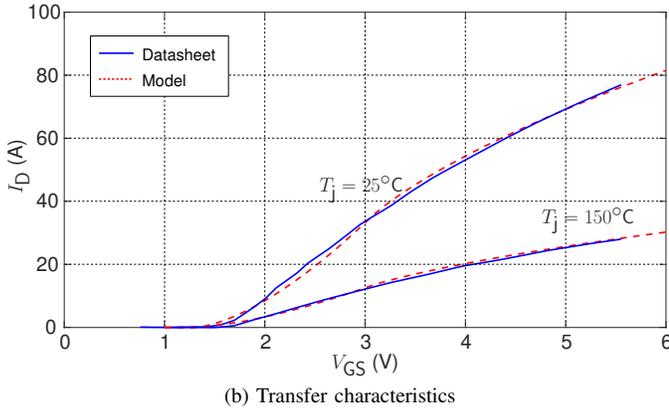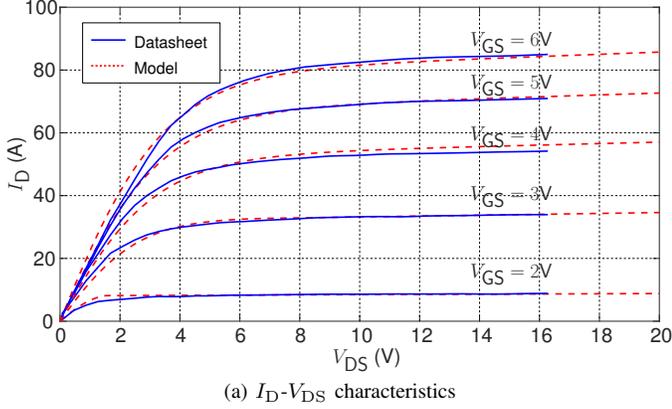
Fig. 6: Comparison between the datasheet and model for GaN-HEMT forward characteristics.

(a) Reverse characteristics
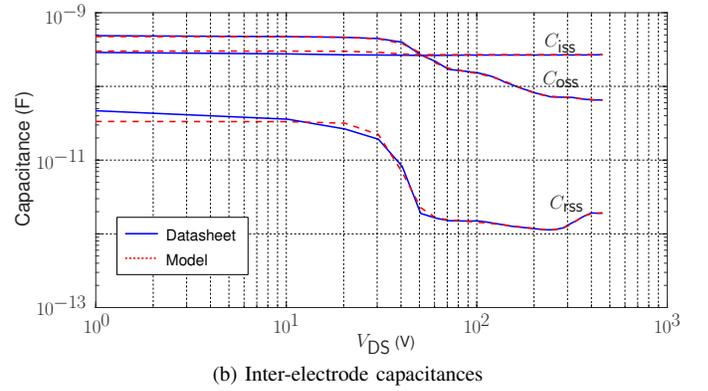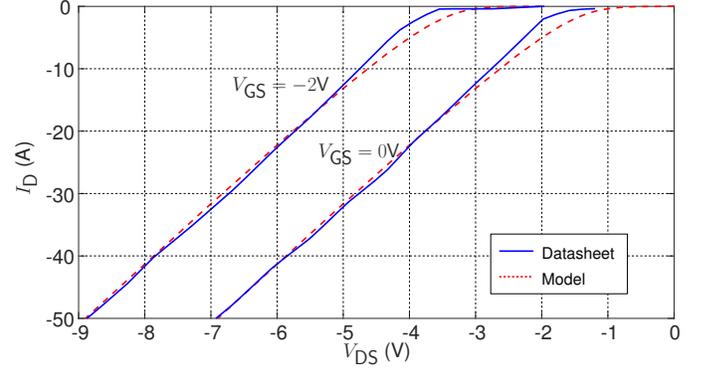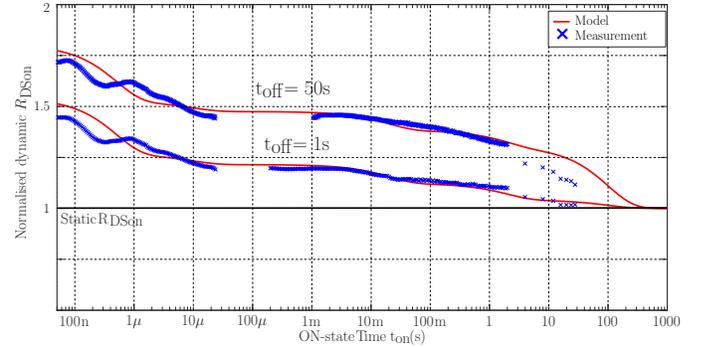

(b) Inter-electrode capacitances

Fig. 7: Comparison between the datasheet and model for GaN-HEMT reverse and inter-electrode capacitance values.

Fig. 8: Comparison between the model and the measurement on GaN device dynamic R_{dson} values.

fitting and are given in TABLE II-TABLE IV. For the characteristics of transistor I_{D}-V_{DS}, transfer, reverse conduction and inter-electrode capacitance values, datasheet values are used as a reference, and they are compared with the model in Fig. 6 and Fig. 7.

Regarding dynamic R_{dson} values, a bespoken characterisation circuit (with more details presented in [27]) is used to extract the parameters of R_{i}, $\tau_{\mathrm{off_i}}$ and $\tau_{\mathrm{on_i}}$, which is given in TABLE V. The comparison between the model and the measurement is presented in Fig. 8.

The above results demonstrate that the characteristics of the transistor are modelled in a satisfactory way, and the validation of the model for both conduction and switching losses will be presented in Section IV.

III. FAST AND ACCURATE MODELLING METHODOLOGY

A. Overview

The overall model structure is illustrated in Fig. 9. The proposed model will be used at first in a software of circuit simulator (e.g. LTspice, Synopsys Saber, Simetrix). LTspice is chosen here because it is widely used for power semiconductor devices electro-thermal simulation at circuit level. Nevertheless, the used equations and parameters of the GaN transistor

TABLE IV: Parameters used in the proposed model for GaN-HEMT C_{ds} and C_{gd} capacitance.

Capacitance	a_1	b_1	c_1	d_1	e_1	f_1	g_1	h_1	i_1	j_1
C_{ds}	7.33×10^{-10}	1.23×10^{-10}	0.077	-48.54	1.39×10^{-10}	-0.011	-199.84	2.12×10^{-10}	0.0093	-171.52
C_{gd}	3.64×10^{-11}	1.41×10^{-12}	$3.44\times10{-3}$	82.45	1.58×10^{-11}	0.11	-33.23	5.28×10^{-13}	-0.0165	-332.34

TABLE V: Different parameters used to model GaN-HEMT dynamic R_{dson}.

i	τ_{off_i} (s)	τ_{on_i} (s)	R_i (Ω)
1	10^{-6}	5×10^{-7}	0.066
2	0.002	9.9×10^{-6}	0.054
3	5×10^{-5}	0.02	0.056
4	0.198	2	0.055
5	6.8	100	0.066

model is given in Section II, so the application of the model is not limited to LTspice. After that, it will generate losses data of N-level. We will then use these losses data in a software suitable for system-level simulation (e.g. PLECS, Simulink, PSIM). Therefore, the designers can obtain the power losses and the temperature of the power converters at system level. One advantage of our proposed model is that it can be applied to different simulation software rather than limitation to one.

Existing circuit simulation tools such as LTspice require the computation of drain current and drain-source voltage waveform in order to obtain the power losses. An accurate calculation of power losses requires a detailed model of transistor, gate drive circuit and layout parasitics which result in high computational costs. For each timestep a complex set of differential equations needs to be solved. Especially during switching transitions with steep current and voltage transients and small timesteps, this results in high computational costs. Possible measures to decrease computational costs are reducing the circuit complexity or increasing the time step, which both result in less accurate results.

Decoupling the loss calculation from the circuit simulation is an approach to overcome the drawback. Fig. 9 shows the block diagram of the proposed modelling methodology. The proposed GaN transistor model is implemented in a simulator (e.g. LTspice) to obtain switching and conduction losses with current, voltage, temperature and deadtime, which will be used in the circuit simulation in the form of mathematical, physical equations and look-up tables. For the circuit simulation (e.g. MATLAB/Simulink), an ideal semiconductor switch model is used. This part of the model provides ideal transistor currents $i_{\mathrm{D}}^{\mathrm{HS}}$ and $i_{\mathrm{D}}^{\mathrm{LS}}$, the switch node voltage v_{SN} as well as the gate-source voltages $v_{\mathrm{GS}}^{\mathrm{HS}}$ and $v_{\mathrm{GS}}^{\mathrm{LS}}$. By combining with pre-obtained switching and conduction losses, power losses (P) and temperature (T_{j}) of each transistor in the half-bridge circuit can be obtained. No detailed switching transients simulation is needed in circuit simulation, therefore simulation speed can be greatly accelerated. The accuracy of the simulation results is then dependent on the transistor model used in LTspice, rather than simulation timestep in MATLAB/Simulink.

Due to varying simulation speed and accuracy requirements in circuit design, multiple levels of the GaN half-bridge model are provided. Table VI shows the considered loss mechanisms for each level. Each level corresponds to an application sce-
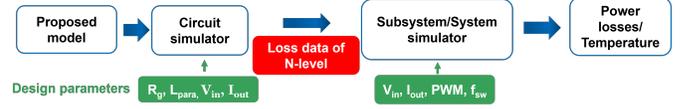

Fig. 9: Overall model structure.

Level 1: blue
Level 2: blue + green
Level 3: blue + green + thermal model
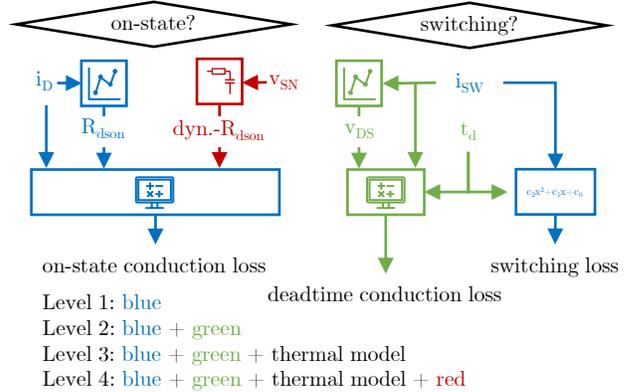Level 4: blue + green + thermal model + red

Fig. 10: Power loss calculation model structure excluding thermal model.

nario of the GaN transistors for power electronics converters. The model structure of the power loss calculation for all levels is shown in Fig. 10 and is described in detail in the following subsections.

B. N-level loss model

1) Level 1: Level 1, blue, is the most basic but the fastest model. It can be used to design a GaN DC/DC power converter with low switching frequency (f<100 kHz). Only conduction losses due to static-R_{dson}, $P_{\mathrm{cond}}^{\mathrm{on}}$, and switching losses are considered. The influence of deadtime on switching losses is neglected. $P_{\mathrm{cond}}^{\mathrm{on}}$ is calculated by means of (1). The actual R_{dson} value is modeled by a 1-D look-up table considering the drain current dependency.

As described, four different switching transitions according to the switching energies, $E_{\mathrm{sw-on}}^{\mathrm{pos}}$, $E_{\mathrm{sw-off}}^{\mathrm{pos}}$, $E_{\mathrm{sw-on}}^{\mathrm{neg}}$, $E_{\mathrm{sw-off}}^{\mathrm{neg}}$, may occur. A switching transition is indicated by a rising or falling edge of v_{SN}. Based on the edge type of v_{SN} and the load current direction, the correct switching energy is assigned to high- and low-side transistor according to TABLE VII. Each switching energy model underlies a separation of E_{VI} and E_{Coss} with a mathematical model approximating the power loss depending on the switched current. The used equations (8), (9), (10) and (11) are polynomials up to fourth-order.

$$E_{\mathrm{sw-on}}^{\mathrm{pos}} = a_{1\mathrm{Coss1}} \cdot i_{\mathrm{L}} \tag{8}$$

$$E_{\mathrm{sw-off}}^{\mathrm{pos}} = a_{1\mathrm{Coss}} \cdot i_{\mathrm{L}} + b_{4\mathrm{VI}} \cdot i_{\mathrm{L}}^4 + b_{3\mathrm{VI}} \cdot i_{\mathrm{L}}^3 \tag{9}$$

TABLE VI: Level structure of GaN half-bridge model.

	$P_{\text{cond}}^{\text{on}}$ loss	switching loss	$P_{\text{cond}}^{\text{dt}}$ loss	self heating	$P_{\text{cond}}^{\text{dyn}}$ loss
level 1	▲	●	■	■	■
level 2	▲	▲	▲	■	■
level 3	▲	▲	▲	▲	■
level 4	▲	▲	▲	▲	▲

▲ loss mechanism considered
● loss mechanism without effect of deadtime considered
■ loss mechanism not considered

TABLE VII: Assignment of switching loss energy.

v_{SN}	i_{L}	high-side		low-side	
		switching	deadtime	switching	deadtime
↑	> 0	$E_{\text{sw}-\text{on}}^{\text{neg}}$	-	$E_{\text{sw}-\text{off}}^{\text{neg}}$	$P_{\text{cond}}^{\text{dt}} \cdot t_{\text{d}}$
↑	< 0	$E_{\text{sw}-\text{on}}^{\text{pos}}$	$P_{\text{cond}}^{\text{dt}} \cdot (t_{\text{d}}-t_{\text{s}})$	$E_{\text{sw}-\text{off}}^{\text{pos}}$	-
↓	> 0	$E_{\text{sw}-\text{off}}^{\text{pos}}$	-	$E_{\text{sw}-\text{on}}^{\text{pos}}$	$P_{\text{cond}}^{\text{dt}} \cdot (t_{\text{d}}-t_{\text{s}})$
↓	< 0	$E_{\text{sw}-\text{off}}^{\text{neg}}$	$P_{\text{cond}}^{\text{dt}} \cdot t_{\text{d}}$	$E_{\text{sw}-\text{on}}^{\text{neg}}$	-

$$E_{\text{sw}-\text{on}}^{\text{neg}} = d_{3\text{Coss}} \cdot i_{\text{L}}^3 + d_{2\text{Coss}+\text{VI}} \cdot i_{\text{L}}^2 + d_{1\text{Coss}+\text{VI}} \cdot i_{\text{L}} + d_{0\text{Coss}+\text{VI}} \tag{10}$$

$$E_{\text{sw}-\text{off}}^{\text{neg}} = e_{2\text{VI}} \cdot i_{\text{L}}^2 + e_{1\text{Coss}} \cdot i_{\text{L}} + e_{0\text{Coss}} \tag{11}$$

2) Level 2: In addition to Level 1 model, the effect of deadtime on power losses is considered in Level 2. It can be used to design a synchronous GaN DC/DC power converter with high switching frequency (f>100 kHz). The switching loss calculation is extended by a dependency on the deadtime (green). Deadtime conduction loss is added to the model, whereby $P_{\text{cond}}^{\text{dyn}}$ and loss due to self heating are still neglected. During deadtime the load current is assumed as constant. The drain-source voltage during deadtime conduction is modelled, as the R_{dson}, by a drain current dependent 1-D look-up table. In case of a not sufficient deadtime, $E_{\text{sw}-\text{on}}^{\text{pos}}$ and $E_{\text{sw}-\text{off}}^{\text{pos}}$ are scaled according to the ratio of the actual deadtime to the necessary deadtime for a completely soft transition.

3) Level 3: The temperature dependency is included in Level 3. It can be used to design a fast switching synchronous GaN DC/DC power converter considering thermal effect. The influence of self-heating can be modelled by scaling the reference power loss for a junction temperature of 25 °C to the actual junction temperature. Furthermore, the scaling of power loss is similar for each loss mechanism appearing in the same material of the transistor. Loss mechanisms which occur in the same area of the device show the same temperature behaviour. To model the device temperature a Cauer-model is used. During each switching cycle, the average power losses of the last switching cycle are applied to the thermal model.

4) Level 4: Finally, conduction losses due to dynamic R_{dson} is included in Level 4. It can be used to design a fast switching synchronous GaN DC/DC power converter considering thermal and trapping effect. To include $P_{\text{cond}}^{\text{dyn}}$ the exponential growth and decay of dynamic-R_{dson} with several time constants, the method described in [26] is adopted. Instead of inserting a voltage source between drain- and

source, dynamic-R_{dson} is added to the static-R_{dson} model described for level 1.

IV. VALIDATION AND APPLICATION

A. Validation of model accuracy

The proposed GaN transistor model is first simulated in the circuit software LTspice. Simulation results are compared with experimental measurement to validate model accuracy.

1) Switching losses: The experimental measurement circuit for GaN transistor switching losses is given in Fig. 11(a), where it is a standard half-bridge circuit. Transistor 2 is the device under test (DUT). A similar circuit is simulated in LTspice, where parasitic inductances of the switching mesh (L_{D}), gate driver circuit (L_{G}), input capacitance (L_{C}) and transistor packaging (L_{d}, L_{s} and L_{g}) are extracted using Ansys Q3D. After applying a gate control signal shown in Fig. 11(b), turn-OFF switching losses (E_{swoff}) can be obtained at the end of the first pulse while turn-ON switching losses (E_{swon}) can be obtained at the beginning of the second pulse. The first pulse width can be adjusted to vary load current value (I_{L}). The realisation of the circuit is shown in Fig. 11(c).

The turn-ON and turn-OFF switching waveform comparison between the simulation and the experiment is shown in Fig. 12(a) and Fig. 12(b) at 300 V/10 A. The model predicts accurately switching transients in terms of both $\frac{\text{dI}_{\text{D}}}{\text{dt}}$ and $\frac{\text{dV}_{\text{DS}}}{\text{dt}}$. We note there is some mismatch between the simulation and the experiments in terms of the resonance. The resonance amplitude of the measurement is higher than that of the simulation. This is because there are two factors we did not consider in modelling: 1) the mutual inductance between different loops (such as the power loop and the gate driver loop); 2) the insertion impedance of the used voltage and current probe. Fine modelling of the resonance in the circuit is beyond the scope of this paper and shall be investigated by the authors in the near future. Despite that, as shown in the comparison of the switching losses in Fig. 12(c), the simulation matches well the experimental measurement. Thus, the accuracy and the robustness of the model for switching losses can be proved.

2) Conduction losses: The experimental measurement circuit for GaN transistor conduction losses is given in Fig. 13(a), where it is formed by two half-bridge circuits. In order to accurately measure the conduction losses (dynamic R_{dson}): a) A V_{DS} ON-state voltage (V_{DSon}) measurement circuit is connected in parallel with the DUT. The purpose of the voltage clamping circuit is to reduce V_{DS} measurement voltage when transistor is in OFF state, but equals to V_{DSon} voltage when transistor is in ON state. As shown in the measurement results in Fig. 13b, our circuit allows to reduce the V_{DS} measurement voltage $V_{\text{DS(m.)}}$ to around 2 V when transistor is in OFF state, so both measurement accuracy and resolution can be greatly improved than direct measurement taking the full V_{DS} range without the clamping circuit. b) Use an LC passive circuit connected between the mid-point of each half-bridge circuit. We will drive the H-bridge circuit and make the inductor current I_{L} in trapezoidal shape as shown in Fig. 13b. Therefore, we only obtain the conduction losses when current is constant
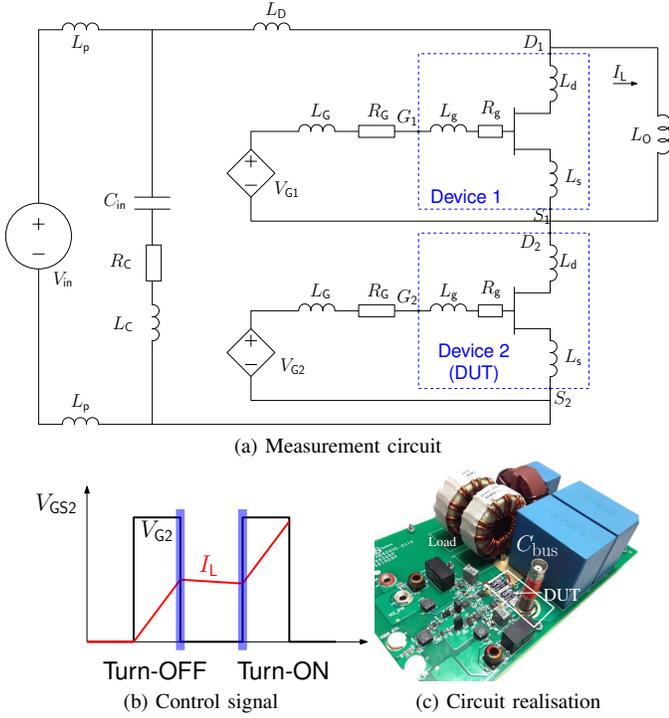
(a) Measurement circuit

(b) Control signal

(c) Circuit realisation

Fig. 11: Experimental measurement circuit, control signal and realisation.

(a) Turn-ON switching (300V/10A)

(b) Turn-OFF switching (300V/10A)

(c) Switching losses comparison

Fig. 12: Comparison between the simulation and measurement for switching losses at 300 V.

(illustrate by red curve I_D in Fig. 13b), which eliminates the influence of measurement circuit parasitic inductance L_c on measurement results by $V_{L_c} = L_c \frac{dI_D}{dt}$. Therefore, dynamic R_{dson} values can be obtained accurately by $\frac{V_{DSon}}{I_D}$.

The comparison of the normalised dynamic R_{dson} value to static R_{dson} value between simulation and experimental measurement is shown in Fig. 13(b). The dynamic R_{dson} are measured at different switching frequencies and duty cycles. The cross points represent the measurement results of different duty cycles when the transistor is switching at 100 kHz, while the diamond points correspond to the measurement results of different switching frequencies under a constant duty cycle 0.5. As the overall error between the simulation and experimental measurements is within 10%, the model accuracy can be thus validated.

B. Validation of N-level loss model

A synchronous buck converter with 400 V input voltage (close to the measured battery voltage from a racing vehicle given in Fig. 16 below), 13 A output current (around half of the rating current of the used GaN transistor (GS-065-030-2-L) by taking a safe operation margin), 100 ns deadtime and switching frequency of 200 kHz is chosen as a case study. The duty cycle is set to 0.5 and a resistive-inductive load is used. As the accuracy of the proposed GaN transistor model is experimentally validated, it is simulated in LTspice as a reference. The presented N-level loss model is simulated in MATLAB/Simulink to compare the accuracy and simulation time with the reference.

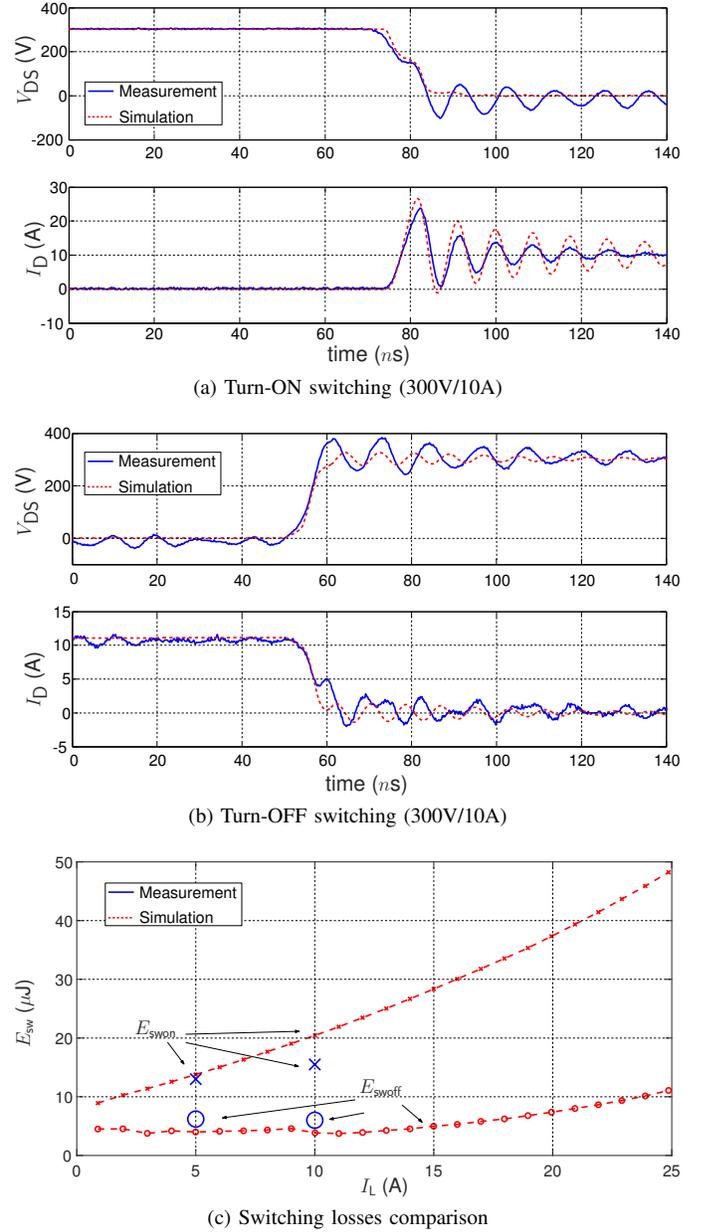It is presented in Fig. 14 the comparison between the Level 4 model and the reference. For both high-side and low-side

transistors, L4 model matches accurately with the reference in terms of both the power losses and the temperature. A breakdown of the losses is also illustrated. For high-side transistor, both switching and conduction losses are predominant. Deadtime losses is zero, as it is the low-side transistor that conducts the current during the deadtime. In comparison, both conduction and switching losses are predominant for low-side device. Its switching loss is almost zero, as it is operated under zero voltage soft (ZVS) switching. It should be noted the breakdown of the losses cannot be easily extracted using reference model in LTspice. With our proposed N-level modelling approach, the breakdown of the losses can be easily illustrated and therefore it is important for the design of the power converters.
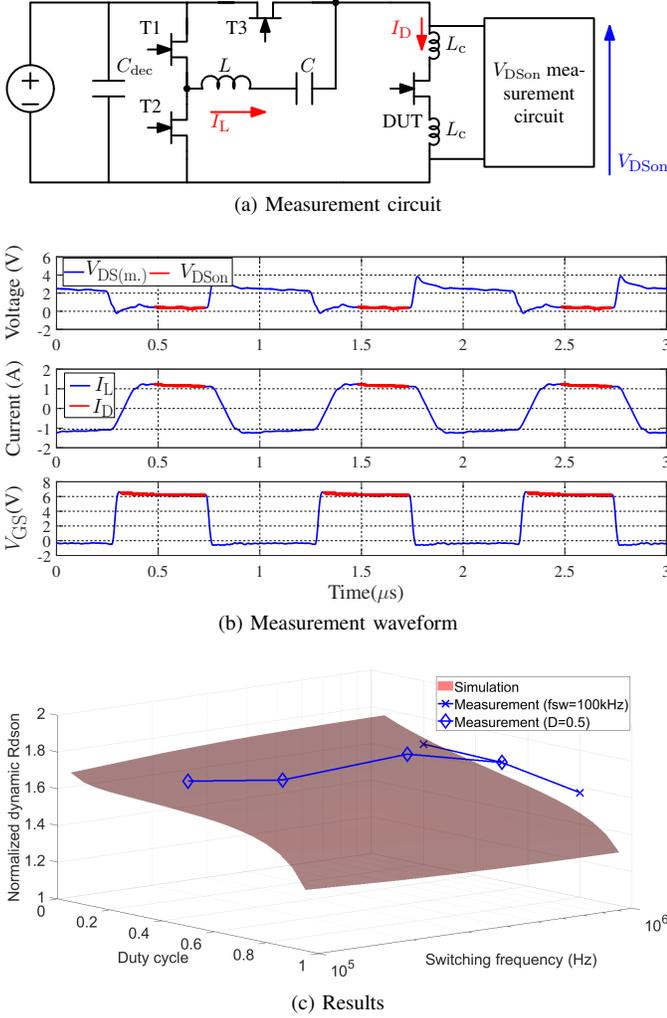
(a) Measurement circuit

(b) Measurement waveform

(c) Results

Fig. 13: Comparison between the model and simulation for conduction losses.
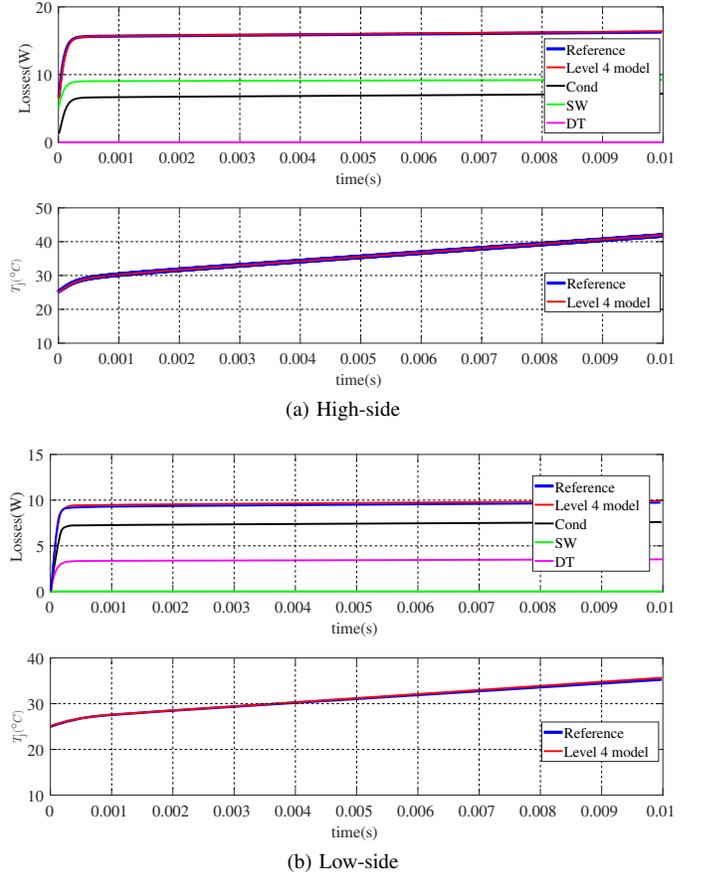

(a) High-side

(b) Low-side
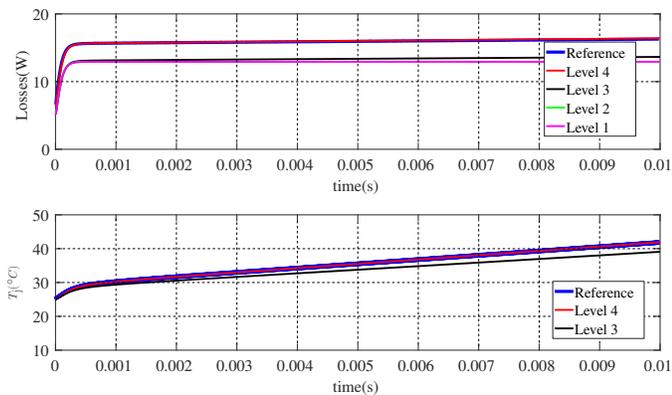
Fig. 14: Comparison between the reference and Level 4 loss model.

TABLE VIII: Comparison between the simulation time and accuracy of N-level loss model and the reference.

	Reference	L1	L2	L3	L4
Simulation time (s)	2708	50	46	74	154
P^{HS} (W)	16.3	12.9	13	13.6	16.4
P^{LS} (W)	9.5	3.9	6.6	7	9.8
T_j^{HS} (°C)	42	-	-	39	42
T_j^{LS} (°C)	34.8	-	-	32	35.1

The loss model (at different levels) are also compared with the reference in Fig. 15. For high-side transistor, the difference between Level 1-3 is not obvious, which is due to the relatively small temperature rise (17 °C) at the end of the simulation. Based on measurement results illustrated in Fig. 13 of the paper, dynamic R_{DSon} increases 1.6 times than static R_{DSon} value when power converter operates at 200 kHz, D=0.5. As shown in Fig. 14, the total conduction losses of high side and low side transistors are about 7.2 W (they are equal as the duty cycle is 0.5). If dR_{DSon} is not considered, then the total conduction losses are $\frac{7.2}{1.6} = 4.5$ W, which yields a difference of $7.2 - 4.5 = 2.7$ W. As shown in Fig. 15 and TABLE VIII, the difference of the total power losses between L3 and L4 model for both high-side (16.4-13.6=2.8 W) and low-side (9.8-7=2.8 W) transistors are 2.8 W, which confirms that the main difference between Level 3 and Level 4 model is due to dR_{DSon} losses. It also illustrates the importance of considering it for overall power losses calculation. For low-side transistor, as it is operated under ZVS switching, the deadtime losses is important to be analysed to find an optimal deadtime. Therefore, we see an obvious difference between

Level 1 model and the others.

TABLE VIII shows a significant simulation time reduction of all levels compared to the reference. Even though simulation time of Level 4 model increases almost 3 times than Level 1 model, it still reduces almost 18 times the simulation time than the reference. It also illustrates that by considering losses during the deadtime (L2), due to the temperature (L3) and dynamic resistance (L4), the model accuracy improves after each level and eventually achieves the same accuracy as the reference.

We also compare the difference between other models and the reference and summarise the results in TABLE IX. The model 1 [28] is offered by the manufacturer. Both the losses dependency with the temperature and during deadtime are considered. However, power losses due to dynamic R_{DSon} is not included in the model. Therefore, this model is similar as

(a) High-side
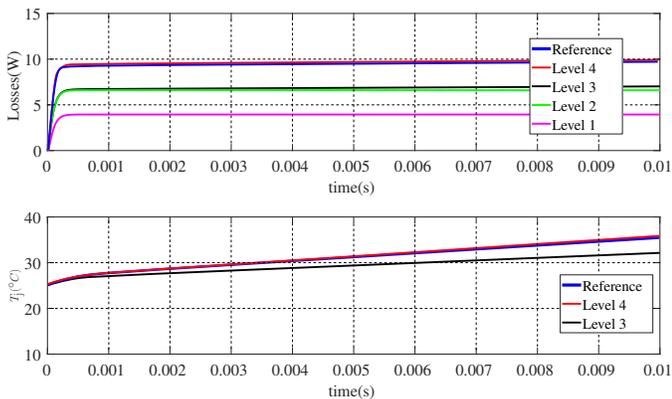
(b) Low-side

Fig. 15: Comparison between the reference and loss model of different levels.

TABLE IX: Comparison of the difference to the Reference between our proposed model with other models.

|	This paper	Model 1 [28]	Model 2 [22], [29]
P^{HS} (W)	0.1	-2.7	-1.3
P^{LS} (W)	0.3	-2.5	-1.1

Level 3 model. And the same results of the Level 3 model will be obtained if we use the same parameters, which yields a difference of -3 W and -2.5 W for total power losses of high-side transistor and low-side transistor. The model 2 proposed in [22], [29] is an improved one from the manufacturer model by adding the dynamic R_{DSon} value, which is similar to our proposed Level 4 model in the paper. However, the modelling of dynamic R_{DSon} is different. It simply uses a constant scaling factor (0.28) as presented in [29]. The drawback is that it neglects the accumulation rate of the traps under different duty cycles. When applying this model under our simulation condition, we would obtain high-side transistor power losses of 15 W and low-side transistor power losses of 8.4 W, which yields to -1.3 W and -1.1 W of difference to the reference. In comparison, our Level 4 model only has a difference of 0.1 W and 0.3 W, which helps to improve the accuracy by more than 70% in comparison with the above models from the manufacturer and the literature.

(a) Racing vehicle
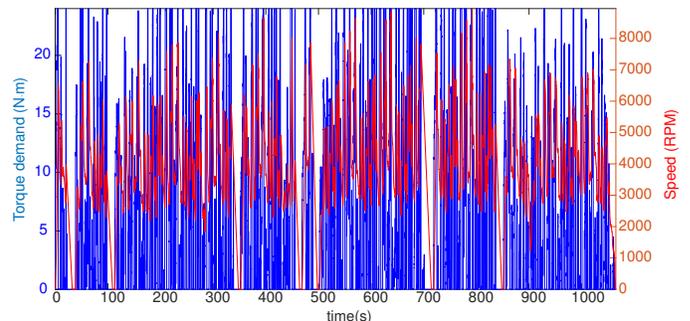
(b) Torque demand and measured speed
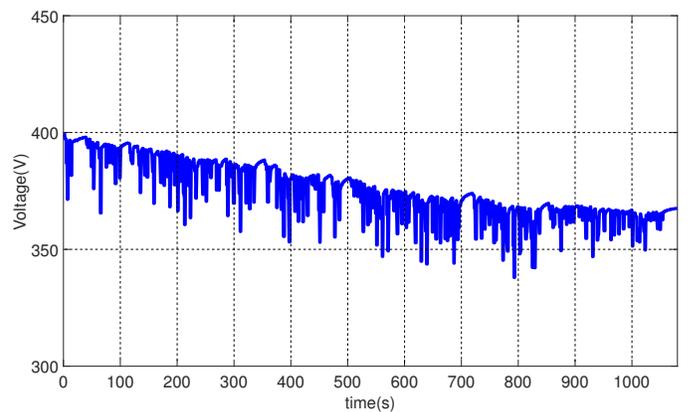
(c) Measured battery voltage

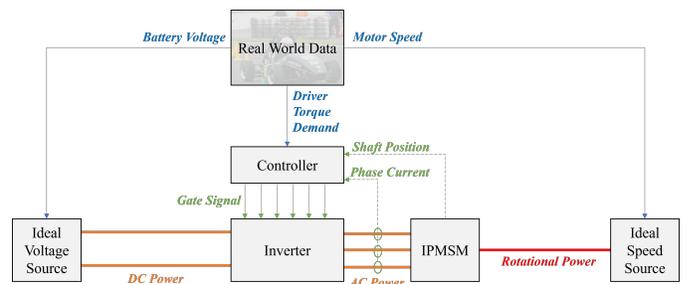Fig. 16: Measured data from a racing vehicle.

Fig. 17: Racing vehicle powertrain simulation model.

V. APPLICATION FOR RACING VEHICLE POWERTRAIN

In this section, we will apply the proposed model for a powertrain of an electric racing vehicle developed by the

University of Nottingham Racing Team. The racing vehicle is a new single-seater racing vehicle for a 22 km long endurance competition that tests the reliability and performance of the vehicle against competitors. Key variables such as driver inputs (accelerator, brake, steering), battery status (DC voltage and current), and motor drive status (speed, torque demand) were logged to generate a drivecycle. First half (11 km over approximately 18 minutes) of the endurance data has been used, which covered the interested operation range of the motor drive. Out of the variables that were logged during the race, the three variables processed for this application were battery voltage, motor speed, and torque demand. As shown in Fig. 16, the data was logged at 10 Hz and minimal processing has been applied (e.g., momentarily dropped packets have been interpolated) before feeding into the EV Powertrain model.

An existent electric powertrain model from MATLAB for Interior Permanent Magnet Synchronous Motor (IPMSM) torque control was adapted to represent the racing vehicle. The simulation model is given in Fig. 17, which is very similar when compared across vastly different applications like motorsport, light personal and commercial vehicles, heavy goods vehicles, and also marine and aerospace applications. To improve the accuracy and operation speed: 1) Battery model is replaced by a signal-controlled ideal voltage source as the measured battery terminal voltage in the drivecycle is used in the simulation (no need to model the battery). 2) The measured motor speed and torque demand are used as a reference to generate control signals of the inverters. All the simulation parameters are given in TABLE X, and the users only need to update some parameters for a normal vehicle if different e-machine, battery and drive condition (motor speed and torque) used. Therefore, it can be extrapolated easily to a normal vehicle for simulation.

The simulation was solved using 250 ns timestep (Fixed Step Discrete solver). The comparison of the I_q current between the experimental measurement and the simulation is given in Fig. 18. The RMS error between the model and the measurement is 2.33 A, which is only 3.4% of the I_q RMS current. As the torque is in linear relation with I_q current, it also has the same error (3.4%) as I_q current between the measurement and the simulation. Therefore, it is shown that the model matches well the experimental data.

For the inverter model, a three phase circuits with ideal switch model are used. For each phase, as shown in Fig. 9, it generates the signals of V_{GS}^{HS}, V_{GS}^{LS}, V_{SN}, I_D^{HS} and I_D^{LS} and they are fed into our proposed N-level GaN transistor losses model.

The phase current in the simulation is given in Fig. 19(a), where the maximal phase current can reach above 100 A. Therefore, each transistor in the phase is formed by 5 modelled 30 A GaN transistor in parallel. To estimate transistor junction temperature, a Cauer thermal model given in manufacturer datasheet is used [30], and the model has been verified for its accurate junction-case thermal impedance result as datasheet value. The power loss and temperature of high side transistor is then presented in Fig 19(b) (under given time scale, the power losses and the temperature of low side transistor has similar results). It should be noted that our proposed loss model can be

TABLE X: Powertrain parameters of the racing vehicle as used in the model.

Symbol	Description	Value
P_{max}	Motor maximum power	36 kW
T_{max}	Motor maximum torque	32 N·m
L_s^d	Stator inductance d-axis	290μH
L_s^q	Stator inductance q-axis	348μH
L_s^0	Stator inductance zero-axis	145μH
R_s	Stator phase resistance	25mΩ
ϕ	Permanent magnet flux linkage	0.02297 Wb
p	Pole pairs	6
J	Rotor inertia	0.00218 kg·m^2
C_{DC}	DC Link capacitance	500 μF
V_{bat}	Nominal battery voltage	350 V
f_{sw}	Converter switching frequency	100 kHz
t_d	Converter deadtime	1 μs
f_c	Current controller speed	10 kHz
K_P^d	Proportional gain D-axis	0.88
K_i^d	Integral gain D-axis	710
K_P^q	Proportional gain Q-axis	1.07
K_i^q	Integral gain Q-axis	1061
t_s	Solver step size	250 ns
t_{sample}	Logging sample time	10 μs
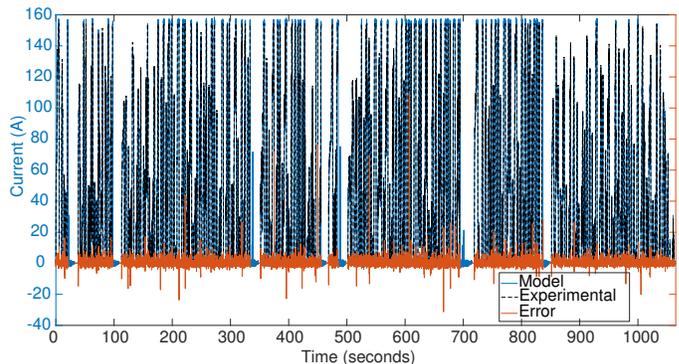
(a) Whole driving cycle
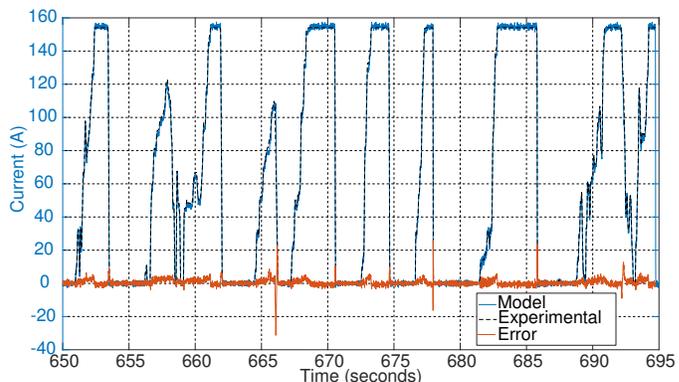
(b) Zoomed view

Fig. 18: Comparison between the simulation and experiment of I_q current.

easily used as black-box together with the powertrain model and can function in a "plug and run" mode. Because of that, designers of electric vehicle drive system can obtain the power losses and temperature of the used power transistors in an accurate and rapid way to optimise power electronics design.
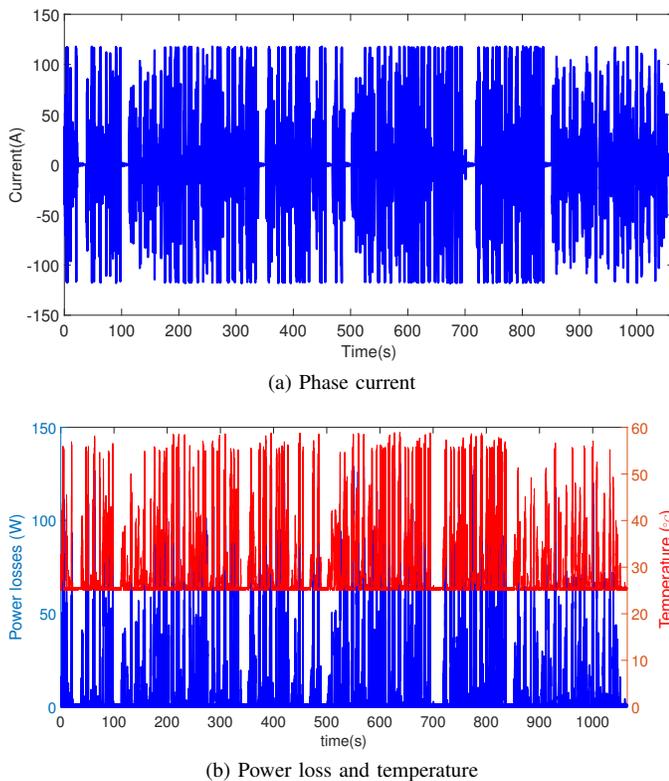
(a) Phase current

(b) Power loss and temperature

Fig. 19: Phase current, transistor power losses and temperature of the powertrain during a half racing cycle.

VI. CONCLUSION

In order to overcome the challenges of simulation speed and accuracy of power electronics converters losses using emerging GaN power transistors, the paper proposes a fast and accurate GaN transistor model to obtain power electronics converters losses. Electric vehicle powertrain is chosen as an application scenario to validate the methodology. A GaN transistor behavioural model is first proposed, and it accurately models transistor characteristics in terms of forward and reverse conduction, inter-electrode capacitances and dynamic resistance. The model is implemented into a simulator (LTspice), and both conduction and switching losses under different voltage, current, temperature and deadtime can be obtained. In order to accelerate simulation speed for circuit simulation, the previously obtained losses are divided into multi-levels (N-level) and used in the circuit simulation in the form of mathematical, physical equations and look-up tables.

By comparing with experimental measurement, the accuracy of both the switching losses and conduction losses of the GaN transistor behavioural model is validated. The simulation results of this model in LTspice is then used as a reference. The N-level loss model is implemented into MATLAB/Simulink, and compared with the results obtained in LTspice. It is shown that our approach can greatly reduce the simulation speed by almost 18 times and maintain the same accuracy. The proposed N-level loss model can be easily implemented into an electric vehicle powertrain model, where the designers can obtain the power losses and temperature of the used power transistors

in an accurate and rapid way to optimise power electronics design.

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