Journal of Applied Physics ARTICLE scitation.org/journal/jap

Detection of defect levels in vicinity of Al_2O_3/p-type GaN interface using sub-bandgap-light-assisted capacitance–voltage method

Cite as: J. Appl. Phys. **132**, 195302 (2022); doi: 10.1063/5.0109117
Submitted: 11 July 2022 · Accepted: 26 October 2022 ·
Published Online: 16 November 2022

Masamichi Akazawa,[1,a)] Yuya Tamamura,[1] Takahide Nukariya,[1] Kouta Kubo,[1] Taketomo Sato,[1] Tetsuo Narita,[2] and Tetsu Kachi[3]

AFFILIATIONS

[1]Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo 060-0813, Japan
[2]Toyota Central R&D Labs., Inc., Nagakute, Aichi 480-1192, Japan
[3]Institute of Materials and Systems for Sustainability, Nagoya University, Nagoya, Aichi 464-8601, Japan

[a)]**Author to whom correspondence should be addressed:** akazawa@rciqe.hokudai.ac.jp

ABSTRACT

Defect levels in the vicinity of the Al_2O_3/p-type GaN interface were characterized using a sub-bandgap-light-assisted capacitance–voltage (C–V) method. For metal–oxide–semiconductor (MOS) diodes prepared using p-type GaN (p-GaN) and Al_2O_3 formed by atomic layer deposition, the C–V curves measured in the dark showed capacitance saturation at a negative bias and a large negative voltage shift compared with ideal curves, which implied the effects of donor-like gap states in the vicinity of the Al_2O_3/p-GaN interface. Upon illumination with monochromated sub-bandgap light with photon energies higher than 2.0 eV under a large positive bias, the subsequently measured C–V curves showed three plateaus. The plateau under the positive bias voltage due to the surface inversion appeared despite the sub-bandgap illumination, which did not appear at 1.8 eV light illumination, indicating the existence of midgap defect levels. Moreover, the other plateaus were attributed to defect levels at 0.60 and 0.7–0.8 eV above the valence band maximum. For a sample whose surface was prepared by photo-electrochemical (PEC) etching to a depth of 16.5 nm, the C–V curve measured in the dark showed a reduced voltage shift compared with the unetched sample. Furthermore, sub-bandgap-light-assisted C–V curves of the sample with PEC etching showed no plateau at a positive bias, which indicated the reduction in the density of the midgap defect states. Possible origins of the detected defect levels are discussed. The obtained results showed that the interface control can improve the properties of p-GaN MOS structures.

I. INTRODUCTION

The application of GaN to power devices is promising. In particular, metal–oxide–semiconductor field-effect transistors (MOSFETs) can fully benefit from the advantageous characteristics of GaN, i.e., wide bandgap,[1] high-electron-mobility,[1] high breakdown electric field,[2] high-electron saturation velocity,[3] and good thermal conductivity.[1] To realize a highly efficient normally off GaN MOSFET using an inversion layer with electrons, properties of oxide/p-type GaN (p-GaN) interfaces should be controlled to minimize the interface-state density (D_{it}). Although excellent insulator/n-GaN interfaces with an extremely low D_{it} near the conduction band minimum have been reported,[4–7] higher D_{it} values near the valence band maximum have also been reported for the insulator/n- and p-GaN interfaces.[8–11] At insulator/p-GaN interfaces, frozen ionized interface states with large time constants distributed in a wide energy range can cause a large flatband voltage shift because the charge neutrality level (E_{CNL}) locates at 2.4 eV above the valence band maximum (E_V).[12] This situation may result in a low threshold voltage of a MOSFET if D_{it} is relatively high. Although effective carrier mobilities higher than 100 $cm^2 V^{-1} s^{-1}$ have been obtained in MOSFETs,[13–18] the electron mobility in the GaN bulk is much higher.[1] Therefore, the remaining issue is to improve the

interface quality. For this purpose, we should investigate the gap states at the insulator/p-GaN interfaces.

Capacitance–voltage (C–V) methods are convenient for characterizing a MOS structure. However, there is a possibility that the high densities of frozen donor-like interface states and defect states lead to a difficulty in applying C–V methods to p-GaN MOS diodes because of a large negative shift of C–V curves resulting in a deep depletion region across the usual bias range. A method of investigating the deep depletion region of C–V curves or detecting midgap states is required to solve this problem. One of the candidate methods is photo-assisted C–V measurement.

Photo-assisted C–V measurement was first applied to a Si MOS structure.[19] After white light from a tungsten lamp was irradiated at the starting voltage in a deep depletion region, C–V characteristics were measured at 77 K in the dark to confirm the generation of the inversion layer and the onset of interface-state response called the interface-state ledge. A similar technique using super-bandgap-light illumination was also applied to SiC MOS structures[20–24] and GaN metal–insulator–semiconductor (MIS) structures at room temperature.[25–27] Although D_{it} distributions were derived in some of these previous studies, the energy range is limited by the time constant of interface states for majority carriers. By using sub-bandgap light of various wavelengths, however, one can investigate the details of D_{it} distributions even at the midgap. Photo-assisted C–V measurement using sub-bandgap light was originally proposed by Mizue *et al.* and first applied to a metal/Al_2O_3/AlGaN/undoped GaN MOS high-electron-mobility transistor structure with two-dimensional electron gas to investigate the midgap states at the Al_2O_3/AlGaN interface.[28] As a result, a U-shaped D_{it} distribution was obtained at the Al_2O_3/AlGaN interface.[28] Further intensive study was carried out by Matys *et al.*[29] This method has also been applied to the Al_2O_3/n-GaN interface, which also resulted in the detection of the U-shaped D_{it} distribution in the entire bandgap, indicating relatively high D_{it} values on the near-E_V side of the bandgap.[30]

On the other hand, there is a possibility that the near-surface point defects in GaN affect the properties of MOS structures. There is also a possibility that defect levels can be detected by sub-bandgap-light-assisted C–V measurement. To remove near-surface defects, the photo-electrochemical (PEC) etching of the p-GaN surface is beneficial. PEC etching incurs minimal damage and enables the precise control of etching depth through current monitoring during etching.[31] It has been reported that the damaged layer on the GaN surface after dry etching can be removed without any further damage, thereby achieving excellent properties of MOS diodes.[31] If this method can be used for the removal of near-surface defects, a clue to controlling the properties of the oxide/p-GaN interface can be obtained.

This work is carried out to characterize the gap states, including interface states and near-surface defect states at the oxide/p-GaN interface, and to reveal critical defect states. In this work, we applied the sub-bandgap-light-assisted C–V measurement to the evaluation of the Al_2O_3/p-GaN interface formed at a relatively low temperature of 300 °C. Furthermore, an attempt was made to apply the PEC etching technique to the p-GaN surface to clarify whether near-surface point defects exist or not and to demonstrate that the surface/interface control is available for MOS structures with p-GaN.

II. EXPERIMENTAL PROCEDURE

The structure of a sample is shown in Fig. 1(a) with its equivalent circuit in Fig. 1(b) and the process flow in Fig. 1(c). The lightly Mg-doped p-GaN layer was grown by metalorganic vapor phase epitaxy on an n^+-GaN substrate via the p^+/n^+ buffer layer junction. The structure of the grown layers was p-GaN (1 μm, [Mg] = 1×10^{17} cm^{-3})/p^+-GaN (1 μm, [Mg]~1×10^{18} cm^{-3})/n^+-GaN (2 μm, [Si]~2×10^{18} cm^{-3}) from top to bottom. Thereafter, for dehydrogenation, the sample was annealed at 800 °C for 5 min in N_2. Each sample was cut from a 2-in. wafer as a 7×8 mm^2 square chip. One of the samples was subjected to PEC etching. Figure 2(a) shows the schematic of the experimental setup for PEC etching. The sample was sintered in an electrolyte and connected to the potentiostat, which is used for controlling the sample bias and monitoring the PEC current. In this study, a solution mixture (pH 6.88) of tartaric acid, propylene glycol, and

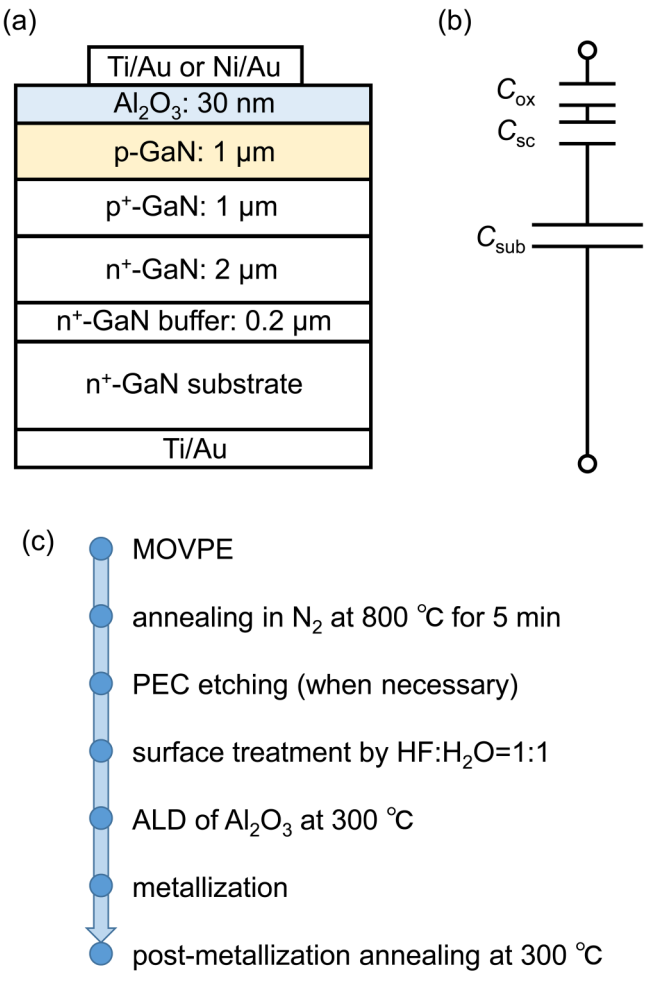

FIG. 1. Schematics of (a) sample structure, (b) its equivalent circuit, and (c) process flow.

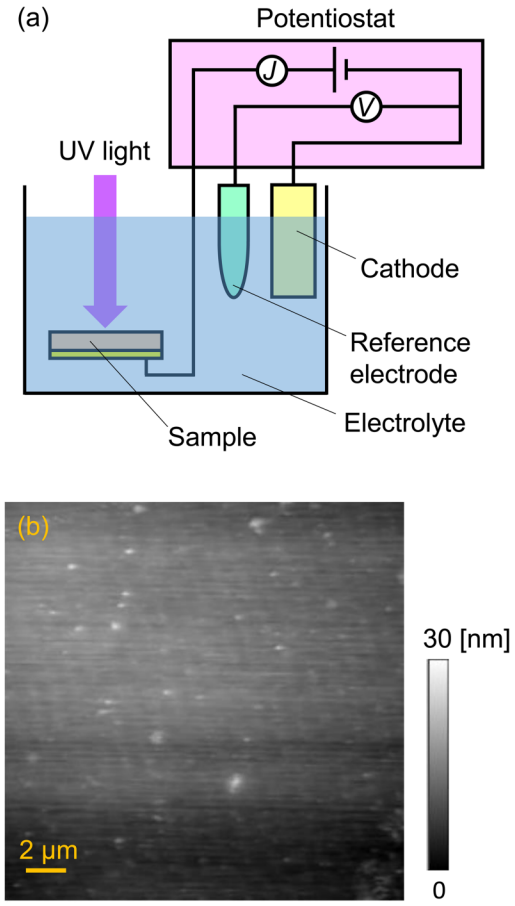

FIG. 2. (a) Schematic of PEC etching setup. (b) AFM image of p-GaN surface with PEC etching.

ammonium hydroxide was used as an electrolyte. To promote PEC reactions, an anodic voltage of 3.0 V was applied to the sample under illumination with ultraviolet light (UV, 360 nm) via the electrolyte. After flowing a current of 8.5×10^{-5} A/cm^2 for 3600 s, the sample was treated with tetramethylammonium hydroxide. The resultant PEC etching depth was 16.5 nm with the root mean square roughness of 1.04 nm measured by atomic force microscopy (AFM), as shown in Fig. 2(b). The surfaces of both unetched and etched samples were treated with a solution of HF:H_2O = 1:1 prior to the atomic layer deposition (ALD) of a 30-nm-thick Al_2O_3 layer at 300 °C using H_2O and trimethylaluminum. The Ti/Au or Ni/Au top circular electrode (300 μm diameter) and the Ti/Au bottom ohmic contact were formed by electron beam evaporation. Finally, post-metallization annealing was carried out at 300 °C in air for 3 h. As shown in Fig. 1(b), the small-signal equivalent circuit for the completed MOS structure is a series connection of capacitance elements, i.e., the oxide capacitance C_{ox}, the semiconductor space charge capacitance C_{sc}, and the substrate capacitance C_{sub} at the p^+/n^+ junction. Because of the large area and small depletion layer width, C_{sub} becomes much larger than the other capacitances. Therefore, C_{sub} can be ignored in the series connection. This concept was reported previously for Schottky barrier diodes (SBDs).[32,33] To perform the sub-bandgap-light-assisted C–V measurement, monochromatic light was prepared using optical band path filters for a xenon lamp light source.

III. RESULTS AND DISCUSSION

A. C–V characteristics measured in the dark

The typical C–V characteristics with the bias sweep from a positive voltage to a negative voltage measured in the dark are shown in Fig. 3(a) for the unetched MOS diode with the Ti/Au top electrode and in Fig. 3(b) for that with the Ni/Au top electrode. Although the deep depletion region was mainly observed, plateaus were seen at the negative bias ends in both Figs. 3(a) and 3(b). These plateaus indicated that the shift of the surface Fermi level (E_{FS}) was blocked by a high density of gap states, which is called Fermi level pinning. In these cases, the increase in negative voltage at the top electrode was compensated for by the change in gap state charge. This resulted from an increase in positive charge at the donor states or a decrease in negative charge at the acceptor states. As described later, the former case is more likely to occur here.

In addition, a marked frequency dispersion can be seen at negative bias voltages. Although the frequency dispersion can be caused by gap states, the saturation seen at 1 kHz corresponds to the time constant of relatively shallow states. This seems to contradict with the plateau capacitance indicating the deep depletion. On the other hand, the dispersion can essentially occur owing to the previously reported "depletion effect"[32,34] even without the defect states. Namely, since the distribution edges of ionized acceptors and holes are separated spatially owing to the high ionization energy of the Mg acceptor level (E_A), frequency dispersion can occur. As is seen in Figs. 3(a) and 3(b), the measurement frequency of 1 kHz is sufficiently low to achieve the low-frequency limit of this phenomenon. The ideal curve was calculated assuming the low-frequency limit. The absence of the influence of parasitic series resistance was confirmed by comparing the C–V characteristics assuming different equivalent circuits, i.e., series and parallel connections of one capacitor and one resistor.

The ideal curves in Fig. 3 were calculated by the numerical analysis of the Poisson equation assuming a high ionization energy E_A and the dependence of the Fermi level (E_F) on concentrations of ionized acceptors and holes. Here, $E_A - E_V = 212$ meV was assumed on the basis of a previous report.[35] As a result, the ideal curve was found to have a bump at the E_{FS} position around E_A. A similar bump has been experimentally observed at a low temperature of 5 K even in a p-Si (presumably B-doped) MOS diode with $E_A - E_V = 40$ meV[36] and has also been found by simulation for MOS diodes with p-SiC.[37] For calculating the ideal curve, the values of C_{ox} were determined by the measurement of C–V characteristics under UV light illumination.

Furthermore, both measured C–V characteristics showed a large horizontal shift to a negative voltage direction compared with the ideal curves. For a wide-gap semiconductor MOS structure, the voltage shift ΔV of a C–V curve in the deep depletion region can be

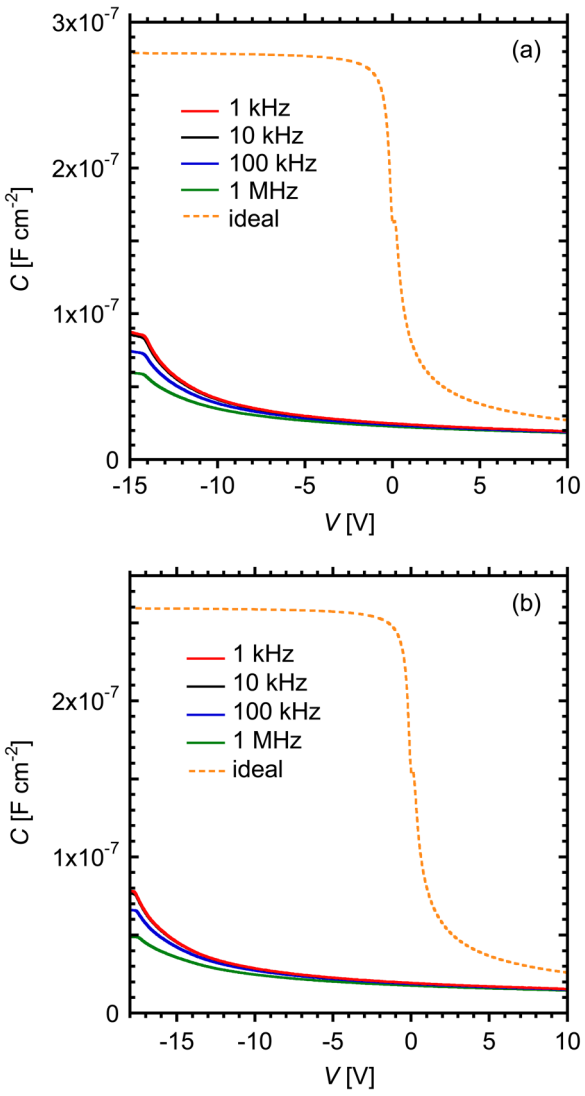

FIG. 3. *C–V* characteristics measured in the dark for unetched p-GaN MOS diodes with (a) Ti/Au and (b) Ni/Au top electrodes. The voltage was swept from 10 V to −15 or −18 V in the dark.

affected by the charges arising from the frozen deep gap states Q_{gs} as shown as follows:

$$\Delta V = \phi_{ms} - \frac{Q_{ox} + Q_{gs}}{C_{ox}}, \quad (1)$$

where ϕ_{ms} is the work function difference between the metal and the semiconductor and Q_{ox} is the sum of charges in the oxide layer.[38] Considering the electron affinity of 4.1 eV[39] for GaN, ϕ_{ms} is calculated to be as small as −3.0 and −2.1 eV for the Ti and Ni electrodes, respectively. On the basis of the *C–V* characteristics of the n-GaN MOS diodes, Q_{ox} is negligible in the ALD Al_2O_3 layer.[5]

Therefore, a large part of ΔV is due to a high density of frozen donor-like gap states, which indicates that the high density of donor-like gap states existed in the vicinity of the Al_2O_3/p-GaN interface. Although these donor states should be investigated, their detection is difficult because they are too deep in the bandgap, as shown by the *C–V* characteristics of the deep depletion region. As one of the solutions to this problem, we applied sub-bandgap-light-assisted *C–V* measurement.

B. Sub-bandgap-light-assisted *C–V* measurement

Figure 4(a) shows the schematics of the ionized interface states under a deep depletion bias (or a large positive bias) in the dark. The donor-like states, which distribute below E_{CNL} and above the maximum energy level with the time constant that is sufficiently small for hole emission, are ionized with positive charges. Upon illumination with monochromated light with a photon energy of $h\nu$, where h is the Planck constant and ν is the frequency of illumination light, the donor states below $E_V + h\nu$ should be neutralized by the emission of holes. When $h\nu$ is smaller than half of the

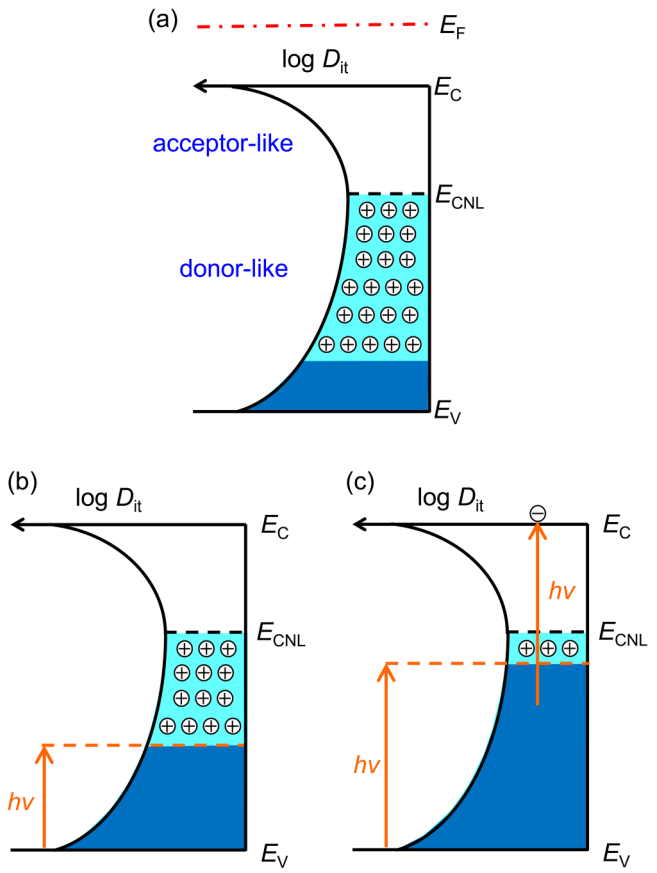

FIG. 4. Schematics of ionized interface states under deep depletion bias: (a) in the dark, (b) upon illumination of $h\nu < E_g/2$, and (c) upon sub-bandgap illumination of $h\nu > E_g/2$.

bandgap E_g, i.e., $h\nu \leq E_g/2$, the situation becomes as shown in Fig. 4(b). However, when $E_g > h\nu > E_g/2$, the two-step excitation of electrons via interface states occur. Namely, after excited electrons from the valence band occupy the ionized interface states, they are further excited to the conduction band by $h\nu$ as shown in Fig. 4(c). In this case, electrons may accumulate at the GaN surface to form an inversion layer. Nevertheless, this phenomenon can be negligible when the gap state density is sufficiently low around the midgap.

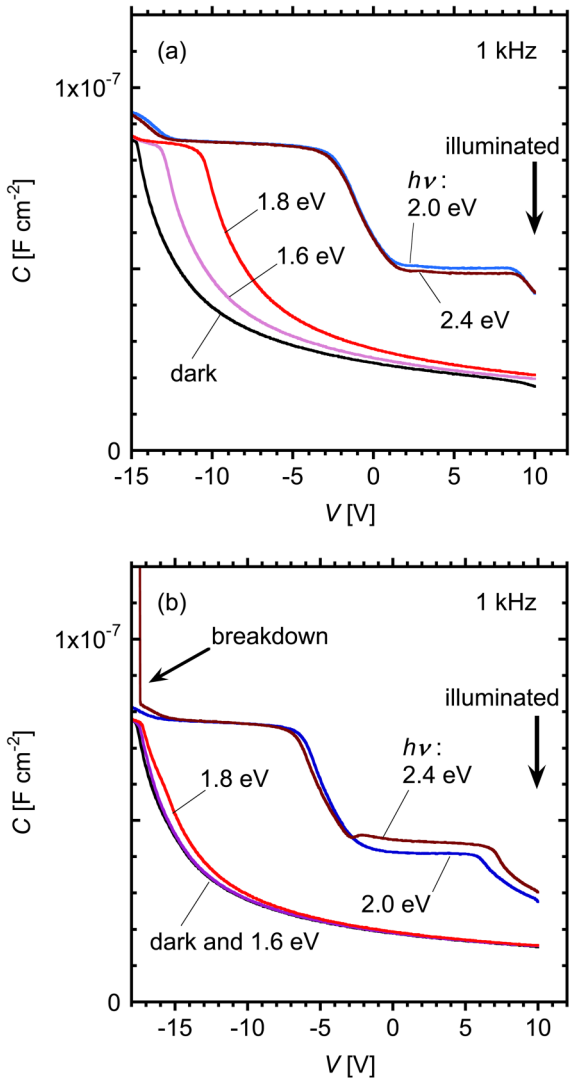

FIG. 5. Results of sub-bandgap-light-assisted C–V measurement of unetched p-GaN MOS diodes with (a) Ti/Au and (b) Ni/Au top electrodes. The measurement frequency was 1 kHz. The voltage was swept from 10 V to −15 or −18 V in the dark immediately after the irradiation of monochromated light at 10 V for 10 min.

The measured C–V curves for various $h\nu$ values of illumination light are shown in Figs. 5(a) and 5(b) for Ti/Au and Ni/Au top electrodes, respectively. The measurement frequency was 1 kHz considering the aforementioned depletion effect. Monochromatic light was illuminated for 10 min at a fixed bias voltage of 10 V for both electrodes. After turning off the light, C–V curves were measured by sweeping the bias voltage from 10 V to −15 or −18 V in the dark. The C–V curves for $h\nu \geq 2.0$ eV exhibited three plateaus. The plateau under the positive bias voltage was due to the inversion at the surface caused by the aforementioned two-step excitation of electrons. The evidence of this phenomenon was obtained by the illumination-power dependence measurement of the C–V curves shown in Fig. 6 for the sample with the Ni/Au top electrode. As the illumination power increased, the voltage shift and plateau capacitance increased, indicating the two-step excitation of electrons to form the surface inversion layer. In Figs. 5(a) and 5(b), note that the difference in the horizontal shift of the C–V curve between $h\nu = 1.8$ and 2.0 eV is significantly large for both samples despite the fact that $h\nu > E_g/2$ for both illuminations. In addition, no surface inversion was observed in 1.8 eV C–V curves, whereas the inversion appeared in 2.0 eV C–V curves. This result indicates that the density of gap states was locally high around the midgap. According to the disorder-induced gap state model, the origin of the interface states is the disorder at the interface, resulting in a U-shaped D_{it} distribution as a continuum in the entire bandgap.[40,41] Therefore, it is unlikely that D_{it} is locally high around the midgap. However, if defects of the semiconductor exist in the vicinity of the interface, a discrete level state can be detected.[42,43] Thus, there is a possibility that a discrete level originating from near-surface defects in p-GaN is relevant to this phenomenon. Schematics of a possible mechanism are illustrated in

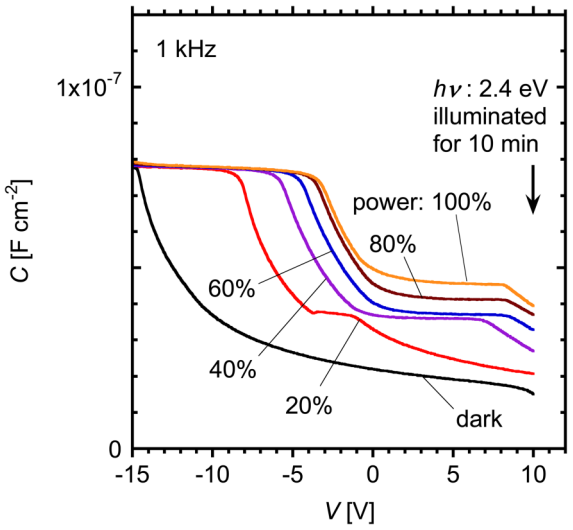

FIG. 6. Illumination-power dependence of C–V curves from sub-bandgap-light-assisted measurements using 2.4 eV monochromatic light for unetched p-GaN MOS diodes. The top electrode was Ni/Au.

Figs. 7(a) and 7(b). A trap level located at E_T between $E_V + h\nu$ and $E_C - h\nu$ induces the two-step excitation of electrons in the valence band as shown in Fig. 7(a). Owing to the abrupt band bending at the surface, the excited electrons accumulate at the Al_2O_3/GaN interface, whereas the generated holes transfer to deep inside GaN, resulting in the surface inversion as shown in Fig. 7(b). If we consider only the 2.0 eV C–V curves, E_T seems to locate between $E_V + 2.0$ and $E_C - 2.0 = E_V + 1.4$ eV. However, note that no plateau under the positive bias was observed in 1.8 eV C–V curves. This means that E_T did not locate between $E_V + 1.8$ and $E_V + 1.6$ eV. Consequently, E_T might have located between $E_V + 1.6$ and $E_V + 1.4$ eV or between $E_V + 2.0$ and $E_V + 1.8$ eV. In the above discussion, the Franc–Condon shift d_{FC} in the excitation energy of defect levels is ignored, which might apply to near-surface defects. Still, a similar threshold $h\nu = 1.8$ eV has been reported on the basis of deep-level optical spectroscopy of n^+–p junction diodes[44] and photocurrent spectroscopy of SBDs[45] although no assignment of the level has been made. As particularly reported in Ref. 45, the defect level at $E_V + 1.59$ eV with $d_{FC} = 0.25$ eV was detected. A defect level around the midgap should have contributed to the inversion.

If the C–V measurement is started from the deep depletion bias to a negative bias immediately after turning off the light, the neutralized states will be gradually occupied by holes according to the bias sweep. Therefore, the measured C–V curve with the bias sweep from a positive voltage to a negative voltage is affected by the gap states if the hole capture time constant τ_{cs} of the gap states at the GaN surface is sufficiently small compared with the delay time for measurement at each bias step. τ_{cs} is given by[19,46]

$$\tau_{cs} = \frac{1}{\sigma v_{th} p_s}, \tag{2}$$

where σ is the capture cross section, v_{th} is the thermal velocity of a hole, and p_s is the hole concentration at the GaN surface given by

$$p_s = N_V \exp\left(-\frac{E_{FS} - E_V}{kT}\right), \tag{3}$$

with N_V being the effective density of states at E_V. The examples of calculation results for τ_{cs} as a function of E_{FS} from Eqs. (2) and (3) for different σ values are plotted in Fig. 8. On the other hand, the hole emission time constant τ_e for a gap state is given by[47]

$$\tau_e = \frac{1}{\sigma v_{th} N_V} \exp\left(\frac{E_T - E_V}{kT}\right). \tag{4}$$

The formula of τ_e becomes the same as that of τ_{cs} if E_T is replaced by E_{FS} in Eq. (4). The gap states at an energy less than 0.4 eV above E_V can respond to a small 1 kHz AC signal, whereas the capture of holes by gap states at the surface cannot occur when E_{FS} is beyond 1.0 eV above E_V. Consequently, the Terman method can be applied to the measured C–V curves as long as E_{FS} locates roughly between 0.4 and 1.0 eV above E_V.

In Figs. 5(a) and 5(b), the plateau under negative bias showed almost the same capacitance independent of $h\nu$, which indicated the surface Fermi level pinning. The Terman method was applied to the C–V curves for $h\nu = 2.0$ eV in Figs. 5(a) and 5(b). The results are shown in Figs. 9(a) and 9(b). Here, the density of states is denoted as D_T because it can contain not only D_{it} but also the near-surface defect state density. It was revealed that the Fermi level pinning at the negative bias voltage originated from a discrete

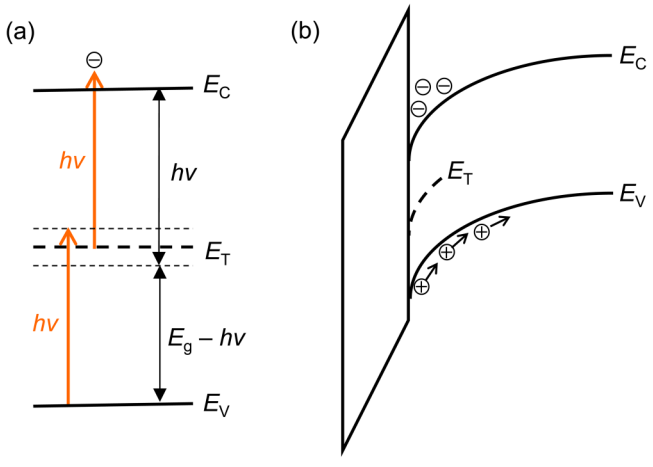

FIG. 7. Schematics. (a) Two-step electron excitation from valence band to conduction band via the defect level by monochromatic sub-bandgap light of $h\nu > E_g/2$. (b) Surface inversion caused by two-step electron excitation and surface band bending.

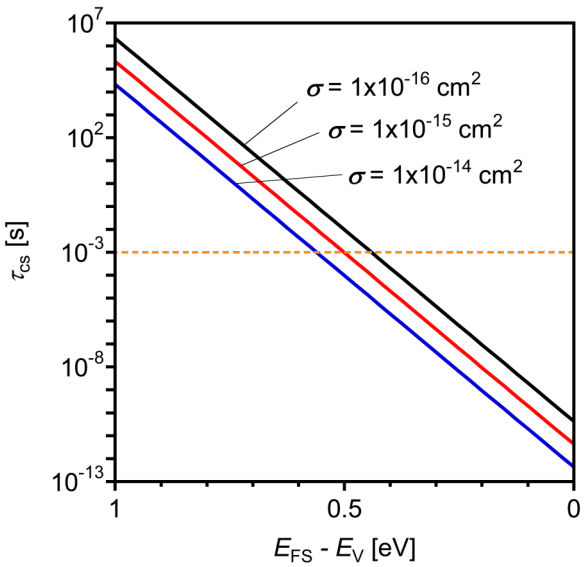

FIG. 8. τ_{cs} as a function of $E_{FS} - E_V$ for sample values of σ. The broken line indicates $\tau_{cs} = 10^{-3}$ as a guide to the eye.

defect level at 0.7–0.8 eV above E_V. The energy positions of these defect levels for the Ti and Ni electrode samples are in good agreement if we consider the experimental error of ±0.1 eV for each sample. The third plateau at −15 V can be seen in the C–V curves for the sample with the Ti/Au electrode. As shown in Fig. 9(a), the D_T distribution increased at around $E_V + 0.6$ eV. A similar defect level seems to exist in Fig. 9(b), even though the energy range of the D_T distribution is limited for the Ni/Au electrode sample to prevent the oxide breakdown at a high negative voltage.

If the Mg doping density is varied, the generation of the gap states at the p-GaN surface might be affected, resulting in different MOS C–V characteristics even in the dark. If the electric field due to surface band bending affects the diffusion of donor defects, the density of defect states at the p-GaN surface might be reduced in highly doped p-GaN. In addition, if the diameter of the top circular electrode of the MOS diode is varied, the effect of minority carriers in the perimeters on the sub-bandgap-light-assisted C–V characteristics might be determined. However, at this stage, any assertions cannot be made because we have no experimental data. These are left for future works.

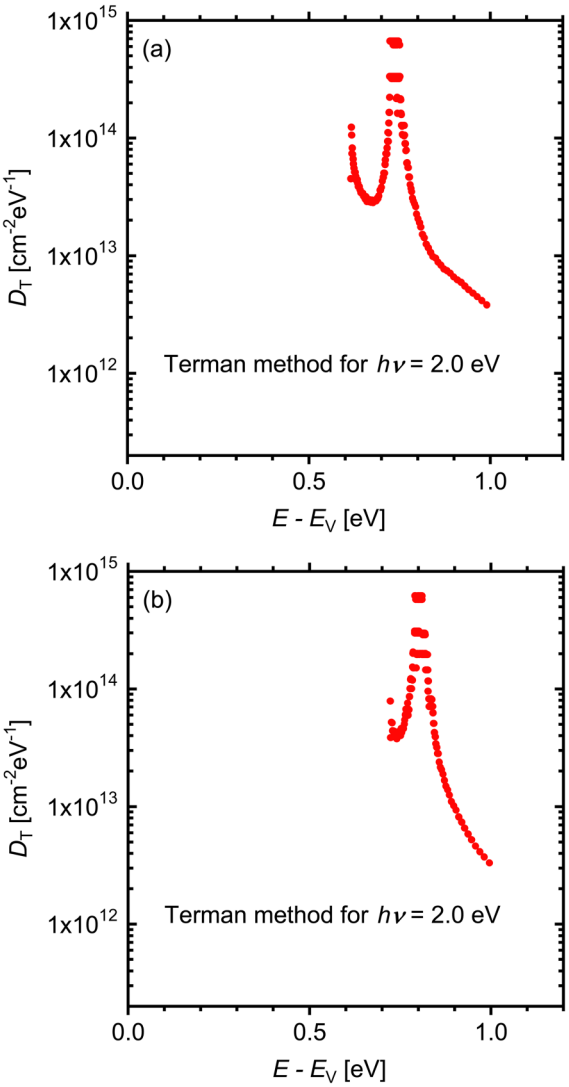

FIG. 9. D_T distribution derived from C–V characteristics from sub-bandgap-light-assisted measurements by the Terman method for unetched p-GaN MOS diodes with (a) Ti/Au and (b) Ni/Au top electrodes.

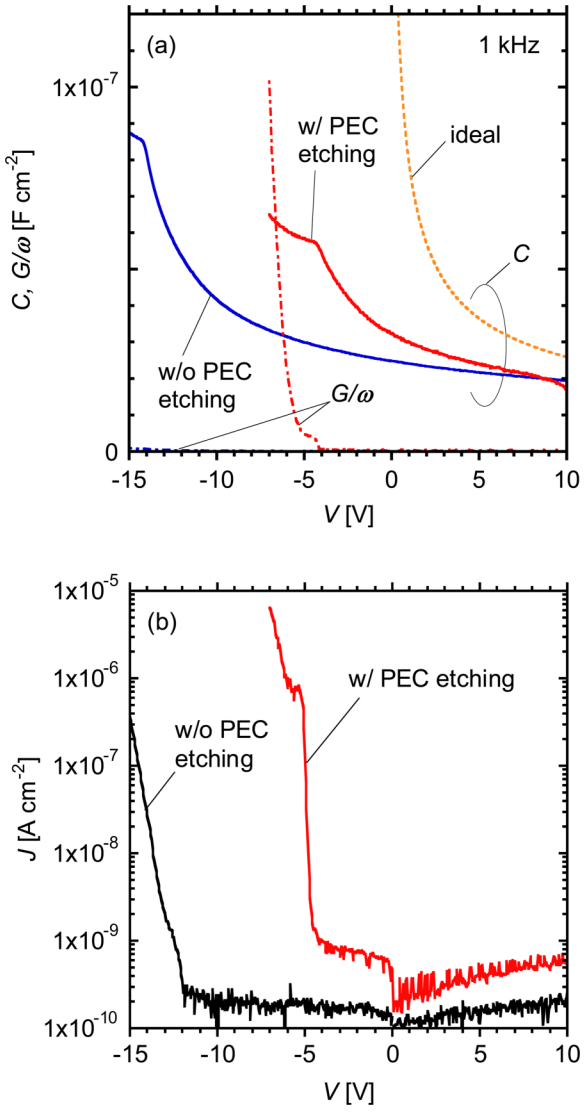

FIG. 10. Comparison of C–V and J–V characteristics between p-GaN MOS diodes without and with PEC etching. (a) C–V characteristics measured by sweeping the voltage from 10 V to −7 or −15 V in the dark. (b) J–V characteristics measured by sweeping the voltage from 0 V to −7 or −15 V and from 0 to 10 V in the dark. The top electrode was Ti/Au for both samples.

C. Effects of PEC etching

To investigate whether the detected discrete levels originate from the near-surface point defects, the sample prepared by PEC etching was investigated. The top electrode was Ti/Au. In Fig. 10(a), the C–V characteristics measured in the dark are compared between the unetched sample [shown in Fig. 3(a)] and the sample with PEC etching. A large reduction in the negative voltage shift of the C–V curve was observed, which indicated that the density of frozen donor-like gap states was reduced. At −6 V, an abrupt increase in parallel conductance (G/ω) was observed with the appearance of the capacitance ledge for the etched sample. The ledge in the C–V curves may correspond to the onset of interface-state response.[19,21–24,26] In Fig. 10(b), the current density–voltage (J–V) characteristics are compared between the samples with and without PEC etching. The positive shift of the leakage onset resulting from PEC etching is in good agreement with that in C–V characteristics. The origin of the abrupt increase in G/ω was leakage current through the Al_2O_3 layer. Since the valence band discontinuity between ALD Al_2O_3 and GaN is estimated to be 1.4 eV on the basis of x-ray photoelectron spectroscopy,[48] the leakage current with this magnitude seems to be reasonable if D_{it} is sufficiently high to concentrate the electric field in the Al_2O_3 layer. The abruptly increasing current may consist of the tunneling current through the insulator under a strong electric field and the charge-up current due to the interface states. Since the deposition condition of Al_2O_3 was the same for both samples with and without PEC etching, it is unlikely that the leakage current was due to the deterioration of the insulating property of the Al_2O_3 layer on the sample with PEC etching.

Figure 11 shows the comparison of the sub-bandgap-light-assisted C–V characteristics of the sample with PEC etching and the unetched sample [curve for $h\nu = 2.4$ eV in Fig. 5(a)]. It can be clearly seen that the plateau under positive bias disappeared, i.e., the electron accumulation was markedly reduced, for the etched sample. This is the evidence that the discrete level around the midgap in the unetched sample originated from the near-surface point defects in GaN. The other defect states shown in Fig. 9 could not be investigated because the negative bias voltage range was limited owing to the abrupt increase in G/ω at the bias corresponding to E_{FS} as deep as $E_V + 1.2$ eV. The sub-bandgap-light-assisted C–V characteristics in Fig. 11 indicate the $h\nu$-dependent capacitance change or dispersion around −5 V. The mechanism of this phenomenon is unclear and beyond the scope of this study. Still, the optimization of the interface formation process including PEC etching can lead to a reduction in D_{it} and presumably to a solution of this complex phenomenon.

D. Possible origins of detected defect levels

If we focus our attention on the native point defects, the calculated formation energy is relatively low for several donor-like point defects when E_F is close to E_V, especially for Ga-antisite (Ga_N), Ga interstitial, and N-vacancy (V_N)-related defects including the $Mg_{Ga}V_N$ complex.[49,50] The midgap deep level should have been a donor-like level considering the reduction in the negative voltage shift of the C–V curve upon PEC etching. Considering the low formation energy and the midgap energy position, Ga_N is one of the candidate origins. Since a deep level was detected at $E_V + 0.5$ eV by deep-level transient spectroscopy[51–53] and assigned to V_N by comparison with the calculation result,[49] the $E_V + 0.60$ eV deep level detected here might have originated from V_N-related defects. In addition, according to Ref. 50, we cannot deny the possibility that the origin of the defect level at 0.7–0.8 eV above E_V might be $Mg_{Ga}V_N$.

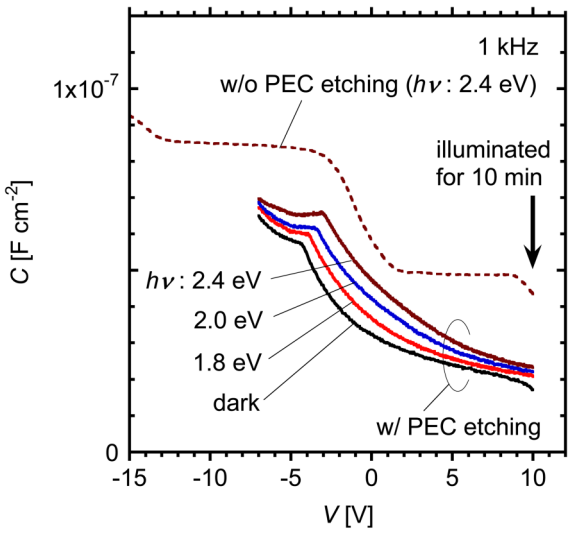

FIG. 11. Sub-bandgap-light-assisted C–V characteristics of p-GaN MOS diodes without and with PEC etching measured by sweeping the voltage from 10 V to −7 or −15 V in the dark immediately after irradiation of monochromated light at 10 V for 10 min. The top electrode was Ti/Au for both samples.

The present results indicate the possibility that surface/interface treatment can improve the electrical properties of the oxide/p-type GaN interface. The optimization of the PEC etching process might lead to further improvement of the properties of p-GaN MOS diodes. Thus, research on the surface/interface treatment of p-type GaN should be promoted further. Although PEC etching was adopted as the surface treatment process in this work, other candidate processes are also available. For example, since V_N-related defects near the GaN surface can be compensated for or terminated by adding nitrogen atoms, the nitrogen plasma treatment might be useful for minimizing the surface and near-surface gap states in GaN. Indeed, the property of the oxide/p-GaN interface formed after inductively coupled plasma reactive-ion etching was evidently improved by nitrogen plasma treatment.[54]

IV. SUMMARY

Gap states at the interface between the Al_2O_3 insulating layer formed by ALD and the p-GaN epitaxial layer on the free-standing GaN substrate were detected by applying the sub-bandgap-light-assisted C–V method to MOS diodes. The C–V characteristics measured in the dark showed deep depletion and very large negative voltage shifts, which indicated the existence of frozen donor-like gap states in the vicinity of the Al_2O_3/GaN interface. On the other

hand, the C–V curves obtained after the illumination of monochromatic sub-bandgap light with $h\nu > 2.0$ eV at a sufficiently large positive bias voltage showed three plateaus [Fig. 5(a)]. The rightmost plateau under the positive bias voltage was due to the formation of the surface inversion layer despite the illumination of the sub-bandgap light. This result indicated the existence of a high-density defect level around the midgap. By applying the Terman method, we can also detect discrete defect levels at 0.6 and 0.7–0.8 eV above E_V. Such high-density discrete defect levels can cause instability under a negative bias in MOSFETs on p-type GaN and should be reduced. Therefore, a surface/interface control method to remove them is sought. In this work, we attempted to reduce the density of gap states through the PEC etching of the GaN surface prior to Al_2O_3 deposition. The MOS sample with PEC etching showed a significant reduction in the negative voltage shift of the C–V curve in the dark, which indicated the reduction in the density of frozen donor-like gap states. In addition, the sub-bandgap-light-assisted C–V curve did not show the positive bias plateau, which indicated the removal of the near-surface defects that generated the midgap level. The obtained results indicated the significance of the surface/interface control process to improve the properties of the oxide/p-GaN interface.

ACKNOWLEDGMENTS

This work was supported by the MEXT Programs "Research and Development of Next-generation Semiconductor to Realize Energy-Saving Society" (Grant No. JPJ005357) and "Creation of Innovative Core Technology for Power Electronics" (Grant No. JPJ009777). The authors acknowledge Dr. M. Matys of Nagoya University for fruitful discussions.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Masamichi Akazawa: Conceptualization (lead); Data curation (lead); Investigation (equal); Methodology (equal); Writing – original draft (lead). **Yuya Tamamura:** Investigation (equal). **Takahide Nukariya:** Investigation (equal). **Kouta Kubo:** Investigation (equal). **Taketomo Sato:** Investigation (equal); Methodology (equal); Writing – original draft (supporting); **Tetsuo Narita:** Data curation (supporting); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Tetsu Kachi:** Investigation (equal); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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