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Research Article

Low-voltage ride-through capability improvement of Type-3 wind turbine through active disturbance rejection feedback control-based dynamic voltage restorer

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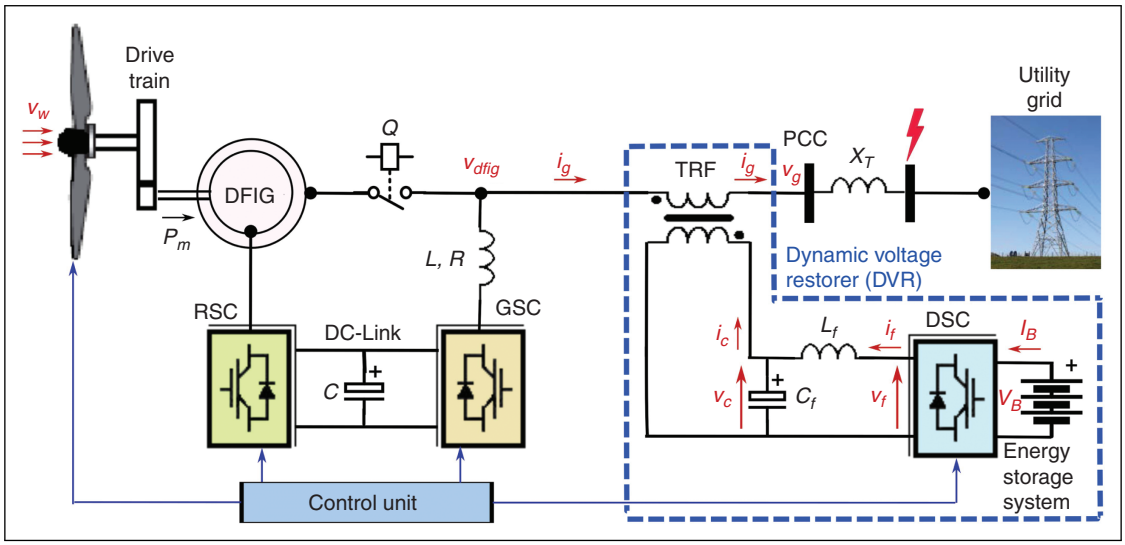
Abstract

Disconnections due to voltage drops in the grid cannot be permitted if wind turbines (WTs) contribute significantly to electricity production, as this increases the risk of production loss and destabilizes the grid. To mitigate the negative effects of these occurrences, WTs must be able to ride through the low-voltage conditions and inject reactive current to provide dynamic voltage support. This paper investigates the low-voltage ride-through (LVRT) capability enhancement of a Type-3 WT utilizing a dynamic voltage restorer (DVR). During the grid voltage drop, the DVR quickly injects a compensating voltage to keep the stator voltage constant. This paper proposes an active disturbance rejection control (ADRC) scheme to control the rotor-side, grid-side and DVR-side converters in a wind–DVR integrated network. The performance of the Type-3 WT with DVR topology is evaluated under various test conditions using MATLAB®/Simulink®. These simulation results are also compared with the experimental results for the LVRT capability performed on a WT emulator equipped with a crowbar and direct current (DC) chopper. The simulation results demonstrate a favourable transient and steady-state response of the Type-3 wind turbine quantities defined by the LVRT codes, as well as improved reactive power support under balanced fault conditions. Under the most severe voltage drop of 95%, the stator currents, rotor currents and DC bus voltage are 1.25 pu, 1.40 pu and 1.09 U_{DC}, respectively, conforming to the values of the LVRT codes. DVR controlled by the ADRC technique significantly increases the LVRT capabilities of a Type-3 doubly-fed induction generator-based WT under symmetrical voltage dip events. Although setting up ADRC controllers might be challenging, the proposed method has been shown to be extremely effective in reducing all kinds of internal and external disturbances.

Graphical Abstract



Keywords: active disturbance rejection controller (ADRC); dynamic voltage restorer (DVR); low-voltage ride-through (LVRT); Type-3 wind turbines (WTs); doubly-fed induction generator (DFIG)

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Introduction

The significance of wind energy as a key contributor to the clean-energy future has become more prominent on a global scale due to its lower levelized cost and improved technology. A stable and consistent contribution from wind power facilities is required for a robust contribution to the electrical grid [1, 2, 3, 4]. Type-3 wind turbines (WTs), based on a doubly-fed induction generator (DFIG), are widely used and achieve a speed variance of ±30% [7, 8, 11, 12, 26]. Low-voltage ride-through (LVRT) ability is an important factor in the topology of WTs. WTs are required to maintain their grid connection and voltage stabilization during and after a failure in order to fulfil LVRT capability [2, 4, 5, 6, 9, 10].

Type-3 WTs have exhibited troublesome LVRT behaviour [16, 17] and are extremely sensitive to changes in grid voltage (sag or swell), especially during voltage dips [4, 9, 17, 18, 19]. Various nations have revised their grid code requirements (GCRs) to emphasize the LVRT functionality of DFIG-WTs. For example, the German LVRT grid stipulates that (see Fig. 1) (i) after a fault occurs, the WTs must stay connected to the grid for ≥0.65 seconds; (ii) the allowed fault voltage is 15% of its nominal voltage; and (iii) the voltage must be restored to 90% of the rated voltage within 3 seconds after fault clearing [4, 11, 12, 13, 14, 15]. Furthermore, most GCRs recommend injecting reactive current during faults [2, 13, 14, 15, 16]. As shown in Fig. 2, the E.ON criteria for voltage support mandates that WTs must inject extra reactive

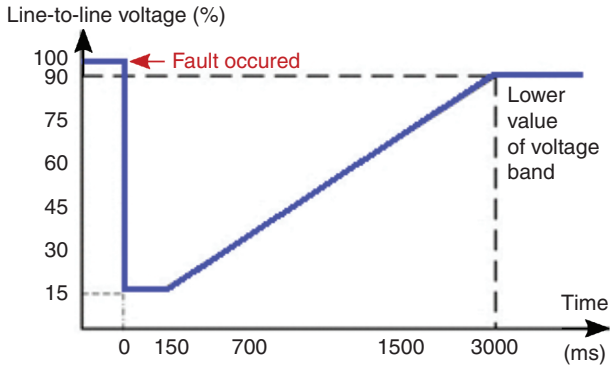

Fig. 1: The German LVRT grid voltage drop threshold for wind energy.

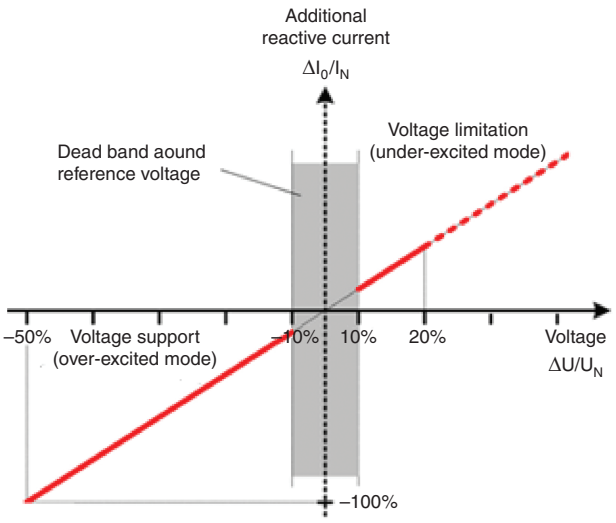

Fig. 2: Typical E.ON grid code for reactive power [13].

current when the voltage exceeds the dead band limit and as the voltage decreases. Within 20 milliseconds of fault detection, provision for reactive power in response to extreme voltage dips should be included [13, 14, 15, 16, 17, 18, 19].

Therefore, to meet the LVRT standards of the GCRs, the following must be addressed in the behaviour of Type-3 WTs during and after the voltage drop: (i) electromagnetic torque and turbine speed must be suitably regulated to guarantee safe operation; (ii) overvoltage and inrush current in the rotor and stator must be limited to avoid damage to the back-to-back converters; (iii) the grid-side converter (GSC) and rotor-side converter (RSC) must have a regulated DC-link voltage for proper operation; and iv) voltage grid recovery requires a specific amount of reactive power [4, 7, 8, 9, 10, 12, 17, 18, 19, 20].

Numerous approaches [7, 8, 9, 10, 12, 19, 20, 21, 22, 23, 24, 25, 28, 29] have been presented in the literature to improve the LVRT capabilities of DFIG-WTs. These solutions include external retrofit techniques and internal control techniques [12, 23]. The latter can meet most of the requirements of the LVRT capability. However, the hardware solution is costly and the complex control unit cannot meet the severe network code standards on its own. Other approaches involve crowbar shunt resistors to protect the rotor windings during a failure [10, 11, 12]. However, when activated, the DFIG is transformed into a squirrel cage induction generator, which requires a reactive power. Protecting the rotor circuit from sudden over-current requires additional components such as superconducting fault current limiters (SFCLs) and series dynamic braking resistors (SDBRs) [18, 27].

In this work, a powerful dynamic voltage regulator (DVR) is utilized to manage the transient oscillations of a DFIG without requiring an extra safety circuit. The DVR, characterized by its fast response time, consists of a voltage source converter (VSC), a coupling transformer, a DC energy source (e.g. a battery) and a harmonic filter (Fig. 3). Thus, under normal and fault conditions, the DFIG stator terminal is kept at rated voltage at all times. As a result, even if there are grid failures, the transient current and transient power of the DFIG do not alter [25, 30, 31].

Using online voltage measurements, the DVR control unit provides the reference voltage, the input control law and the modulation signal to provide switching pulses to the voltage source inverter. In [9, 32, 33], a feed-forward open loop control is used to design the control approach. This control approach is easy to implement and guarantees stability. However, it lacks accuracy and performs poorly during transients. Feedback controllers are used to improve the transient response and regulate the output compensating voltages [25, 34, 35, 36, 37]. Additionally, the conventional proportional–integral (PI) controller is not suitable for time-varying reference tracking and a highly non-linear inverter model [9, 41, 42, 43, 45, 47].

In light of the above discussion, this paper investigates an active disturbance rejection control (ADRC)-based feedback voltage control system for Type-3 DFIG–DVR architecture. To show the capabilities of the proposed ADRC controller, the performance of this Type-3 WT associated with the DVR is analysed under different operating conditions. The simulation results are compared with experimental results obtained by tests performed on a WT emulator using crowbar resistors and a DC chopper to enable the LVRT capability. The main contributions of this paper are:

To investigate the DVR topology for improving the LVRT capability of the Type-3 WT.

To design an ADRC-based feedback voltage control scheme for Type-3 DFIG-based WT–DVR topology.

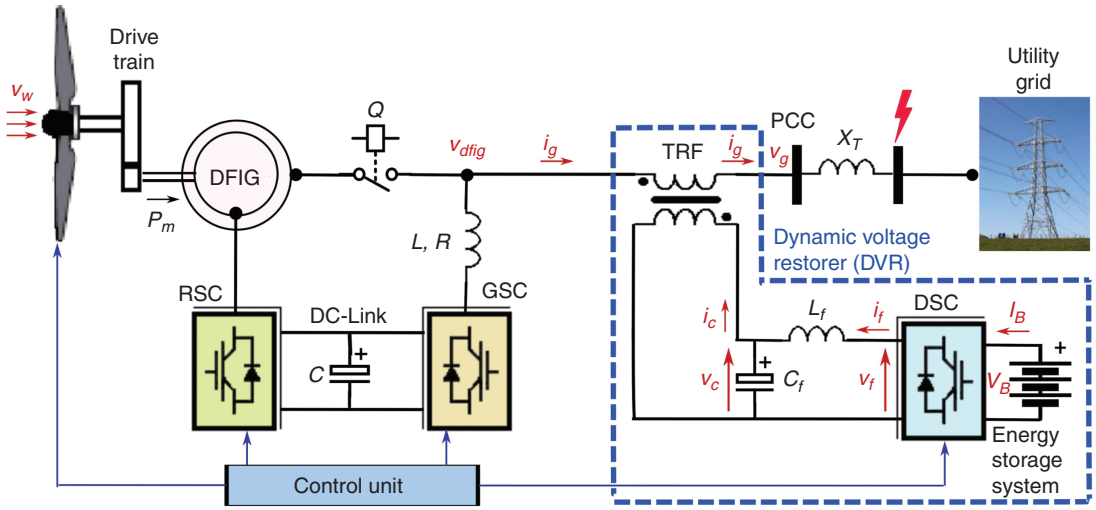

Fig. 3: Grid-connected Type-3 WT architecture with integrated DVR.

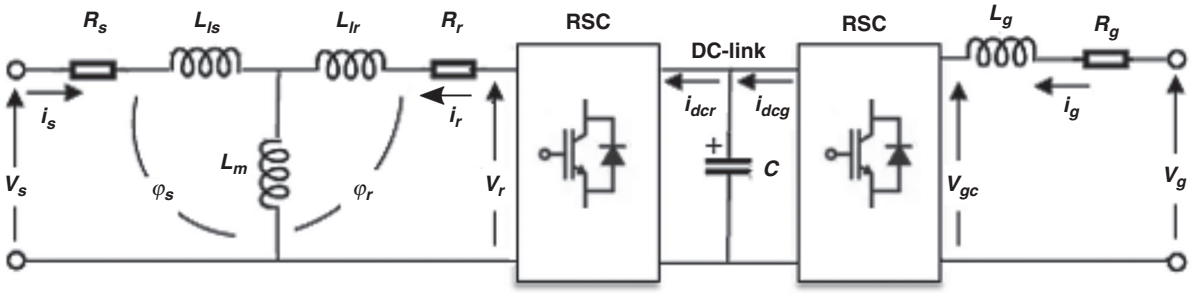

Fig. 4: Typical DFIG model, back-to-back converter and harmonic filter.

To analyse the performance of the proposed WT–DFIG–DVR structure under various operating scenarios controlled by ADRC through the MATLAB®/Simulink tool®.

To compare the simulation results with experimental results performed on a WT emulator using crowbar resistors and a DC chopper to enable LVRT capability.

The remaining sections of this article are organized as follows. The WT–DFIG–DVR model and the design of its ADRC control part are presented in Section 1. Then, the ADRC control architecture of the DVR converter is developed in Section 2. Section 3 provides the simulation and experimental results. Section 4 outlines the conclusion of the paper. For convenience, the main notation used throughout are described in the Nomenclature section.

1 System modelling

Fig. 3 depicts the grid-connected Type-3 WT architecture with integrated DVR in series. The overall architecture employs three power electronics converters, which consist of the GSC, the RSC and the DVR-side converter (DSC). The DFIG stator is connected to the grid through the DVR and the rotor windings are connected via the RSC to the DC link, which is connected to the grid through GSC using a resistor–inductor (RL) filter. The modelling of the WT and DVR is presented in the following paragraphs.

1.1 Type-3 WT modelling

The reduced-order electrical model of the Type 3 WT is presented in Fig. 4. Using the classic theory of rotating fields, the DFIG

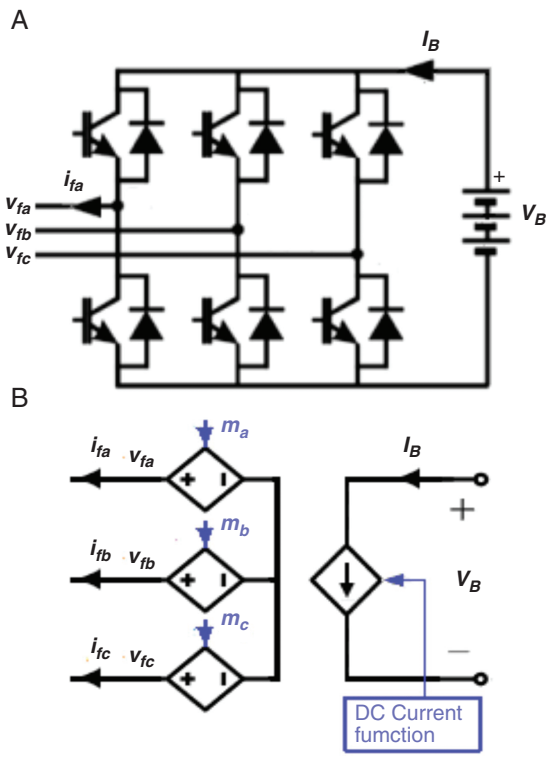

Fig. 5: Two-level VSC architecture. (a) Comprehensive model; (b) mean model.

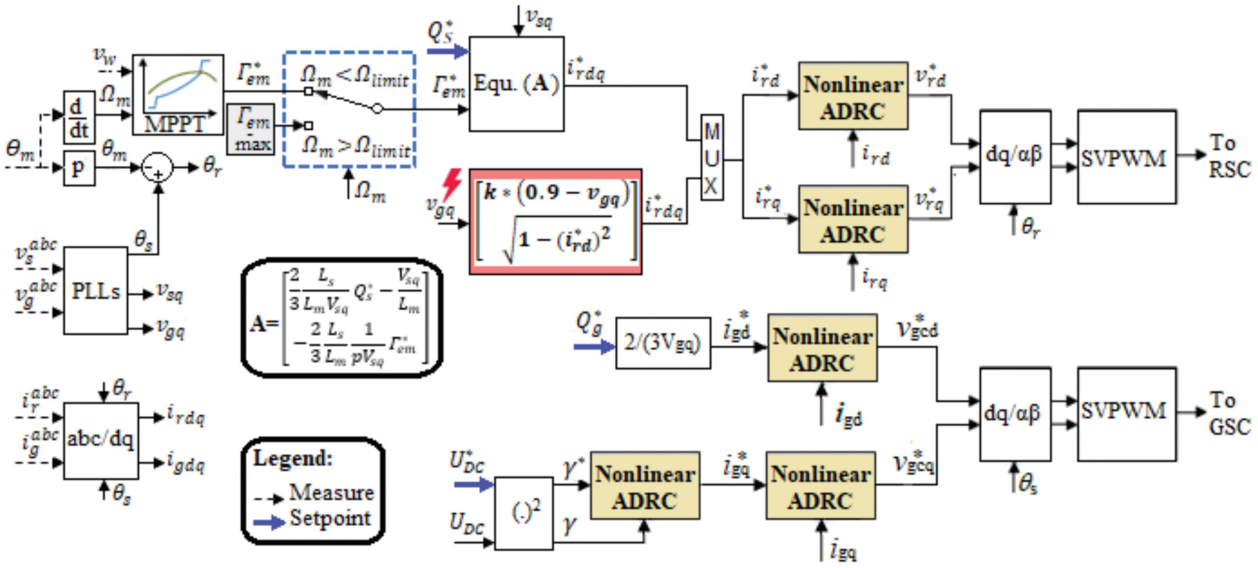

Fig. 6: RSC and GSC control system.

model is expressed through the voltage and flux variables of the stator and rotor in dq coordinates through the following equations [19, 20, 21]:

$$V_{sdq} = \frac{d\psi_{sdq}}{dt} + j\omega_s\psi_{sdq} + R_s I_{sdq} \quad (1)$$

$$V_{rdq} = \frac{d\psi_{rdq}}{dt} + j\omega_r\psi_{rdq} + R_r I_{rdq} \quad (2)$$

where I, V, R, Ψ and ω stand for the current, voltage, winding resistance, magnetic flux and pulsation, respectively. The stator, rotor and dq-axis are indicated by the s, r and dq prefixes, respectively.

Furthermore, the flow vectors in the stator and rotor are represented as:

$$\psi_{sdq} = L_s I_{sdq} + L_m I_{rdq} \quad (3)$$

$$\psi_{rdq} = L_r I_{rdq} + L_m I_{sdq} \quad (4)$$

where L_r and L_s are the self-inductances of the rotor and stator, respectively. The magnetizing inductance is denoted by L_m.

Powers in the stator are stated as follows:

$$S_s = P_s + jQ_s = \frac{3}{2}\left(V_{sdq} I^*_{sdq}\right) \quad (5)$$

where the reactive, apparent, active powers and complex conjugate are denoted by Q_S, S_S, P_S and $*$, respectively.

Substituting Equations (3) and (4) in Equation (2) yields the following dynamics for the rotor currents:

$$\frac{d}{dt} i_{rdq} = -\left(\frac{R_r}{\sigma L_r} + j\omega_r\right) i_{rdq} - \frac{L_m}{\sigma L_r L_s}\frac{d}{dt}\psi_{sdq} - j\omega_r \frac{L_m}{\sigma L_r L_s}\psi_{sdq} + \frac{V_{rdq}}{\sigma L_r} \quad (6)$$

where $\sigma = 1 - \frac{L_m^2}{L_r L_s}$ stands for the dispersion coefficient of the DFIG.

Similarly, the DC-link voltage and the currents that run through the harmonic filter are represented as follows:

$$\frac{d\gamma}{dt} = \frac{3}{C} v_{g,q} i_{g,q} - \frac{2}{C} p_r \quad (7)$$

$$\frac{d}{dt} i_{gdq} = \frac{1}{L_g} v_{gdq} + \left(j\omega_s - \frac{R_g}{L_g}\right) i_{gdq} - \frac{1}{L_f} v_{gcdq} \quad (8)$$

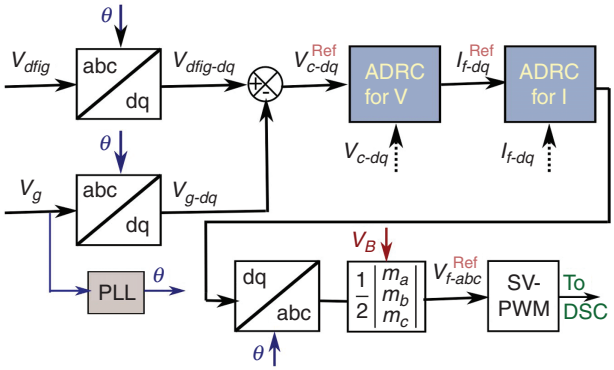

Fig. 7: DSC controller block diagram.

where $\gamma = u_{DC}^2$, p_r represents the rotor active power and further quantities are given in Fig. 4.

1.2 DVR modelling

As shown in Fig. 3, the DVR consists of a VSC connected in series with the DFIG–WT terminal through an ideal three-phase transformer. The energy storage system (ESS) supplies the energy required for voltage dip adjustment. Voltage harmonics induced by the DVR–VSC are filtered out by the inductor–capacitor (LC) filter.

1.2.1 DSC model

Fig. 5a depicts a comprehensive two-level VSC configuration in which the three-phase voltages and currents on the AC side of the DSC are indicated as v_{fabc} and i_{fabc}. In this study, the two-level mean value model of the DSC as shown in Fig. 5b is used [38, 39, 40]. This model is employed because it enhances simulation performance and has steady-state and low-frequency dynamics that are nearly identical to those of a comprehensive model [9, 39]. v_{fa}, v_{fb} and v_{fc} are the three components of the voltage v_{abc} produced by the DSC.

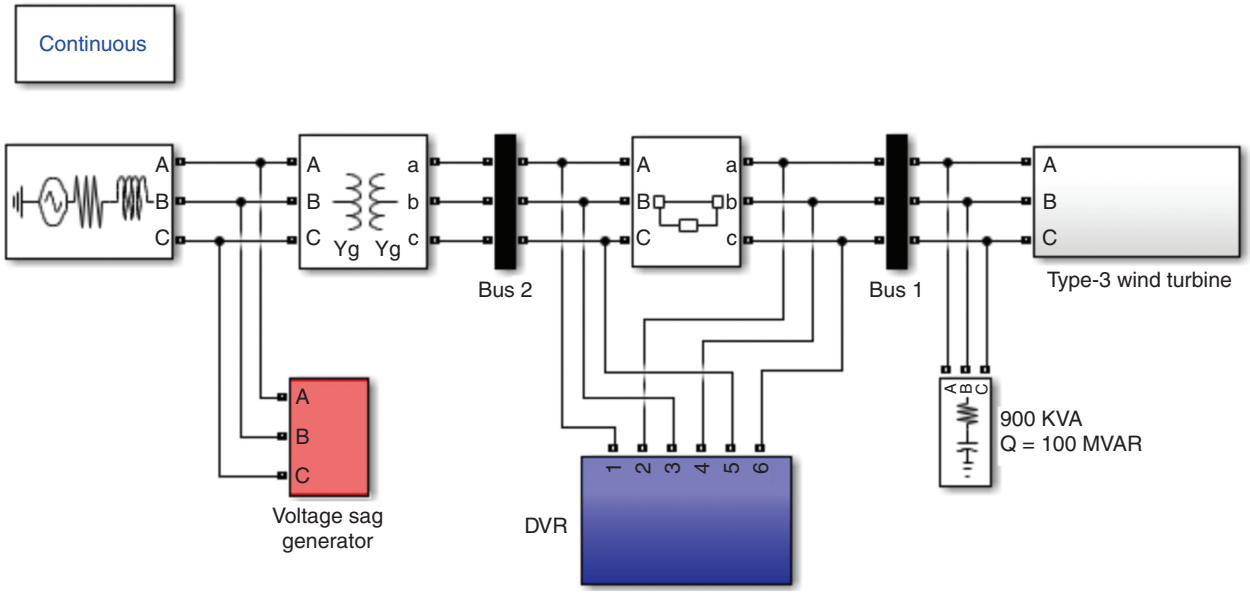

Fig. 8: Schematic simulation model of Type-3 WT with DVR.

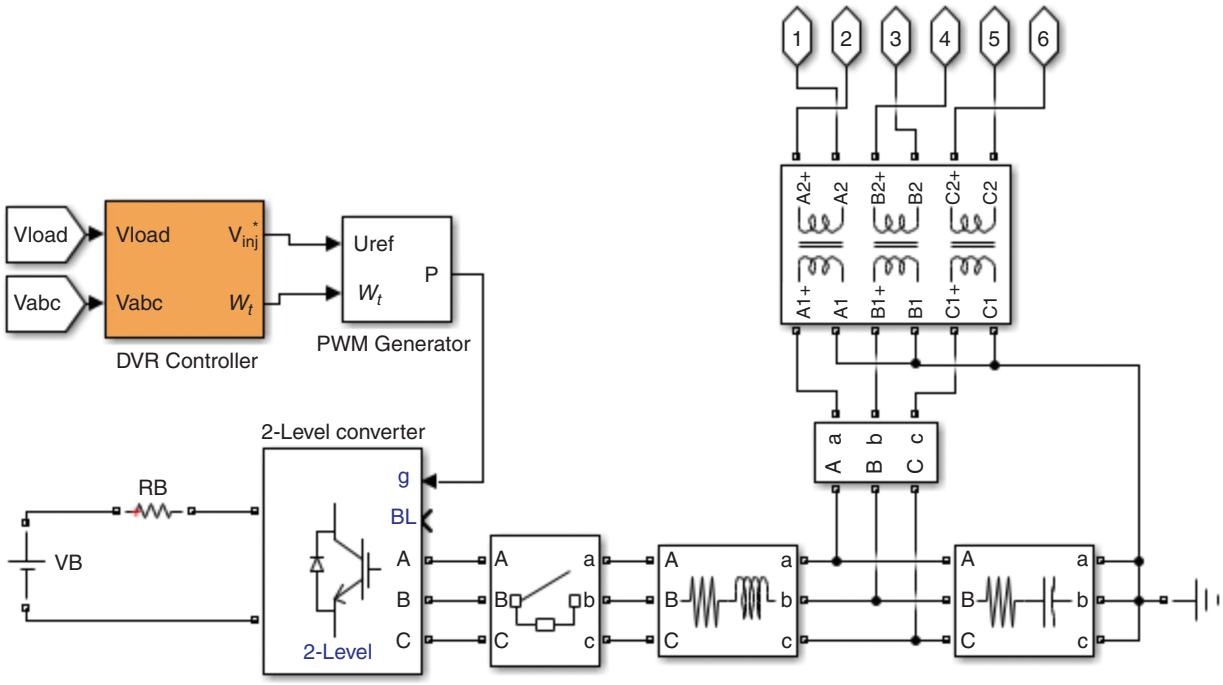

Fig. 9: DVR simulation model.

These three-phase components are stated in terms of m_a, m_b and m_c, the modulation indices of the alternating current voltage [37, 39, 40]:

$$\begin{bmatrix} v_{fa} & v_{fb} & v_{fc} \end{bmatrix}^T = \frac{1}{2}\begin{bmatrix} m_a & m_b & m_c \end{bmatrix}^T V_B \tag{9}$$

Assuming that the DSC is perfectly lossless, the power balance permits writing:

$$i_B = \frac{1}{2}\left(m_a i_{fa} + m_b i_{fb} + m_c i_{fc}\right) \tag{10}$$

1.2.2 *Model of an LC harmonic filter*

The input voltage–current and the output voltage–current are related, as illustrated in Fig. 3 for the modelled LC harmonic filter:

$$\begin{cases} v_c = v_f - L_f \dfrac{di_f}{dt} \\ i_c = -C_f \dfrac{dv_c}{dt} + i_f \end{cases} \tag{11}$$

where v_f–i_f is the voltage–current synthetized by the DSC, v_c–i_c is the compensation voltage–current and L_f and C_f are the filter parameters.

Table 1: Parameters for Type-3 WT with DVR [9, 23]

Component		Nominal value of quantities
Type-3 WT	**Turbine**	$R = 43.36$ m, $H = 5.8$ s, $\lambda_{opT} = 8.2$, $C_{popT} = 0.435$
	DFIG	$P_m = 3$ MW, $f = 50$ Hz $R_r = 21.264$ mΩ, $L_{lr} = 1.607$ mH, $L_m = 15.168$ mH $R_s = 27.285$ mΩ, $L_{ls} = 1.785$ mH $p = 2$, $n_{MAX} = 1850$ rpm
	DC link, harmonic filter, 3φ grid	$U_{DC} = 1220$ V, $C = 66.878$ mF $R_g = 1.59$ mΩ, $L_g = 0.084$ mH, $V_{g,ll} = 690$ V
DVR	**Transformer**	$S_T = 3$ MVA, ratio = 1
	Filter	$C_f = 10$ μF, $L_f = 0.3$ mH
	ESS	$P_B = 3$ MW, $V_B = 1200$, $R_B = 0.1$ Ω
Base value		$V_{Base} = 398.4$ V, $S_{Base} = 3$ MVA, $\omega_{Base} = 314.159$ rad/ s

1.2.3 *Ideal transformer*

Assuming that the transformer in Fig. 3 is an ideal transformer, the voltage–current relationships for the secondary and primary sides are provided by:

$$\begin{cases} \upsilon_{dfig} = \upsilon_c + \upsilon_g \\ i_g = -i_c \end{cases} \tag{12}$$

where the subscripts *dfig*, *g* and *c*, respectively, represent the DFIG, utility grid and DVR compensation.

2 ADRC scheme for Type-3 WT with DVR

This section presents complete control strategies for each converter design based on the non-linear ADRC technique. Based on the simplification of the controlled system, the ADRC control philosophy may be characterized as the control of a perturbed chain of integrators. An extended state observer in this chain estimates the overall disturbance (internal and external) and then cancels it out in the control law (for a full analysis of the topic, see [9, 41, 42, 43, 44, 45, 46]).

2.1 RSC and GSC controllers

Principally, the GSC is responsible for managing reactive power on the utility grid and maintaining a consistent DC-link voltage despite the direction and amount of rotor energy flow. The state variables of the GSC controller are considered as the *q*-axis and *d*-axis grid converter currents (I_{gq} and I_{gd}) and the DC-link voltage, U_{DC}. V_{gcd} and V_{gcq} are the two control signals synthesized by the GSC controller; however, when $V_{gd} = 0$ and $V_{gq} = U_s$, the GSC currents may independently regulate the active and reactive power exchanges of the network.

On the other hand, the RSC controller is designed to drive the reactive and active power outputs of the stator. When the rotor currents are regulated in the dq reference frame (in which ψ_s the stator flux lines up with the *d*-axis), independent control of active/reactive power is also achievable.

2.2 Remark 1

Fig. 6 illustrates the control scheme for the RSC and GSC by using the ADRC technique. The design of the RSC and GSC controllers is based on the model described by Equations (6–8) by following the steps of the ADRC technique outlined in the flow chart of Fig. A1 in the Appendix. The adjustment parameters of the different entities of the ADRC are described in Table A1 in the Appendix. The values of these parameters are determined by trial and error. A more in-depth explanation of these controller designs is presented in [47]. Fig. 6 illustrates the control scheme of the RSC and GSC through using the ADRC technique.

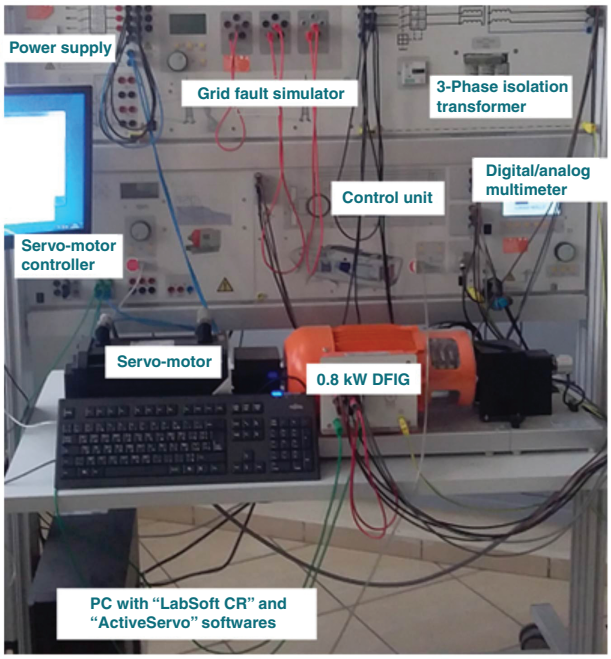

Fig. 10: Experimental set-up.

2.3 Controller design for the DSC

The key purpose of the DVR is to rapidly correct for grid voltage disruptions and maintain the sinusoidal injection voltage profile. The phase-locked loop (PLL) coordinates the DVR control with the supply voltage. The control computes the dq frame, which is afterward transformed into a three-phase quantity to provide the pulse-width modulation signals [23, 38, 48, 49]. The compensation voltages are fed into the network by the isolation transformer at the common coupling point.

Fig. 7 depicts the derivation of the *d*-axis and *q*-axis components of υ_{dfig}, υ_g and υ_c using the dq reference. The DFIG voltage υ_{dfig} is supposed to be aligned with the *q*-axis, i.e. $V_{dfig-d} = 0$ and $V_{dfig-q} = U_0$ (pre-sag voltage). To guarantee that the voltages across the DFIG are suitably corrected against the pre-failure values, the DVR must accurately calculate the compensating voltages injected. The compensating voltage reference V^{ref}_{c-dq} is stated as follows:

$$V^{ref}_{c-dq} = -V_{g-dq} + V^{ref}_{dfig-dq} \tag{13}$$

where V_{g-dq} and $V^{ref}_{dfig-dq}$ represent the grid voltage and the stator DFIG voltage, respectively.

Using the ADRC technique, the two DSC controllers are designed using the following steps:

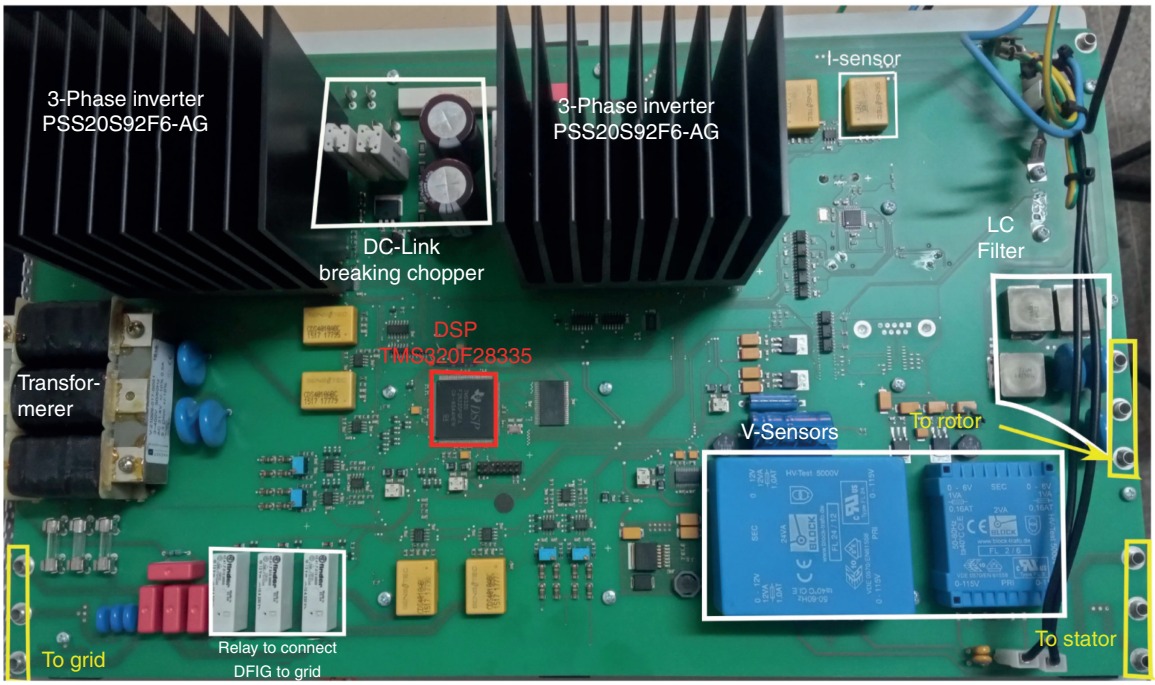

Fig. 11: Control unit board.

(i) In the context of the dq-axis, the subsystem (11) can be rewritten as follows:

$$\begin{cases} \dfrac{dV_{c-dq}}{dt} = -j\omega_s V_{c-dq} + \dfrac{1}{C_f} I_{f-dq} - \dfrac{1}{C_f} I_{c-dq} \\ \dfrac{dI_{f-dq}}{dt} = -\dfrac{1}{L_f} V_{c-dq} + \dfrac{1}{L_f} V_{f-dq} - j\omega_s I_{f-dq} \end{cases} \tag{14}$$

(ii) From the subsystem (14), the canonical ADRC can be presented as follows:

$$\dot{x} = f(x, t, \vartheta) + bu \tag{15}$$

Here the state vector is chosen as $x = \left[V_{cd}, V_{cq}, I_{fd}, I_{fq}\right]^T$, $u = \left[I_{fd}, I_{fq}, V_{fd}, V_{fq}\right]^T$ represents the control input, $\vartheta = [\vartheta_1, \vartheta_2, \vartheta_3, \vartheta_4]^T$ is the vector of unanticipated external disturbance and the overall perturbation matrix f may be expressed as follows:

$$f = \begin{bmatrix} -\dfrac{I_{cd}}{C_f}\left(\dfrac{1}{C_f} - b_{11}\right) u_2 + \omega_s V_{cq} + \vartheta_1 \\ -\dfrac{I_{cq}}{C_f} + \left(\dfrac{1}{C_f} - b_{22}\right) u_2 - \omega_s V_{cd} + \vartheta_2 \\ -\dfrac{V_{cd}}{L_f} - \left(\dfrac{1}{L_f} - b_{33}\right) u_3 + \omega_s I_{fq} + \vartheta_3 \\ \left(\dfrac{1}{L_f} - b_{44}\right) u_4 - \omega_s I_{fd} - \dfrac{V_{cq}}{L_f} + \vartheta_4 \end{bmatrix} \tag{16}$$

where

$$b = \begin{bmatrix} b_{11} & 0 & 0 & 0 \\ 0 & b_{22} & 0 & 0 \\ 0 & 0 & b_{33} & 0 \\ 0 & 0 & 0 & b_{44} \end{bmatrix} = \begin{bmatrix} C_f^{-1} & 0 & 0 & 0 \\ 0 & C_f^{-1} & 0 & 0 \\ 0 & 0 & L_f^{-1} & 0 \\ 0 & 0 & 0 & L_f^{-1} \end{bmatrix} \tag{17}$$

(iii) The further steps of the ADRC approach (design of tracking differentiator, extended state observer and non-linear state error feedback (NLSEF)) are described in Fig. A1 in the Appendix and will be easily applied to these four dynamics specified by Equations (14–17).

The control voltages provided by the I-ADRC controller are converted into an abc reference frame before being sent to the Space Vector Pulse Width Modulation (SVPWM) modulator, as illustrated in Fig. 7.

2.4 Remark 2

(i) The control strategy is prioritized to increase the reactive power and reduce the active power of the DFIG so that it can withstand the grid voltage during the fault. In this case, the set points for i_Q^* (Q) and i_P^* (P) must be adjusted as follows:

$$\begin{bmatrix} i_Q^* \\ i_P^* \end{bmatrix} = \begin{bmatrix} k * \left(0.9 - v_g\right) * I_{max} \\ \sqrt{I_{max}^2 - i_Q^2} \end{bmatrix} \tag{18}$$

where k is a coefficient (typically between 1.5 and 2) derived from grid codes, v_g is the grid voltage (in pu), I_{max} is the maximum stator current and i_Q^* and i_P^* are the active and reactive current, respectively.

(ii) During the transient stage, due to the fluctuating phase and amplitude of I/V, reactive power absorption (i.e. $Q < 0$) is conceivable.

3 Simulation and experimental test set-up

A series of tests are performed in (i) the MATLAB®/Simulink® environment and (ii) the wind emulator hosted in the laboratory of the Higher School of Technology, Ibn Zohr University of Agadir, Morocco. The goal of these wind emulation experiments is to show the success of the ADRC algorithm when applied to the control of a Type-3 WT with DVR. The proposed Type-3 WT with DVR simulation model in MATLAB®/Simulink® is presented in Figs 8 and 9. Table 1 presents the simulation

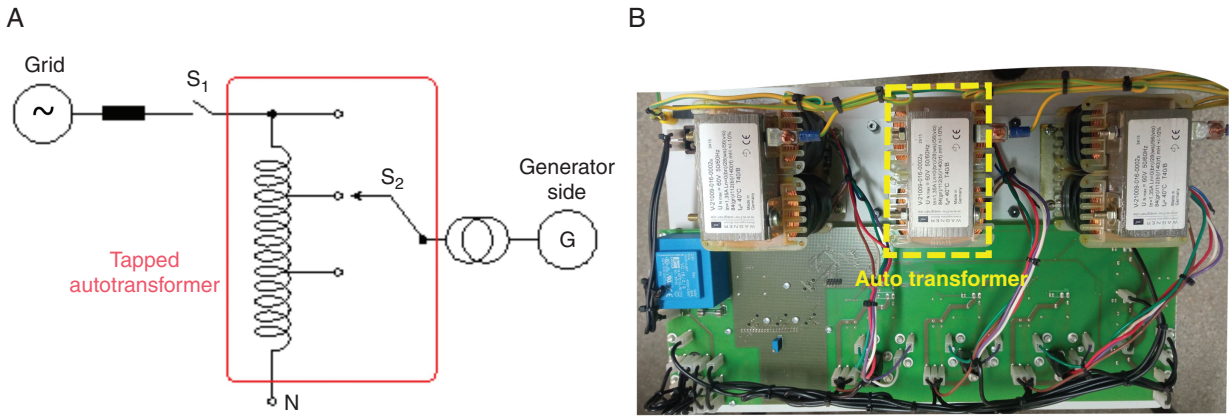

Fig. 12: Transformer-based voltage sag generator. (a) Typical structure; (b) set-up picture.

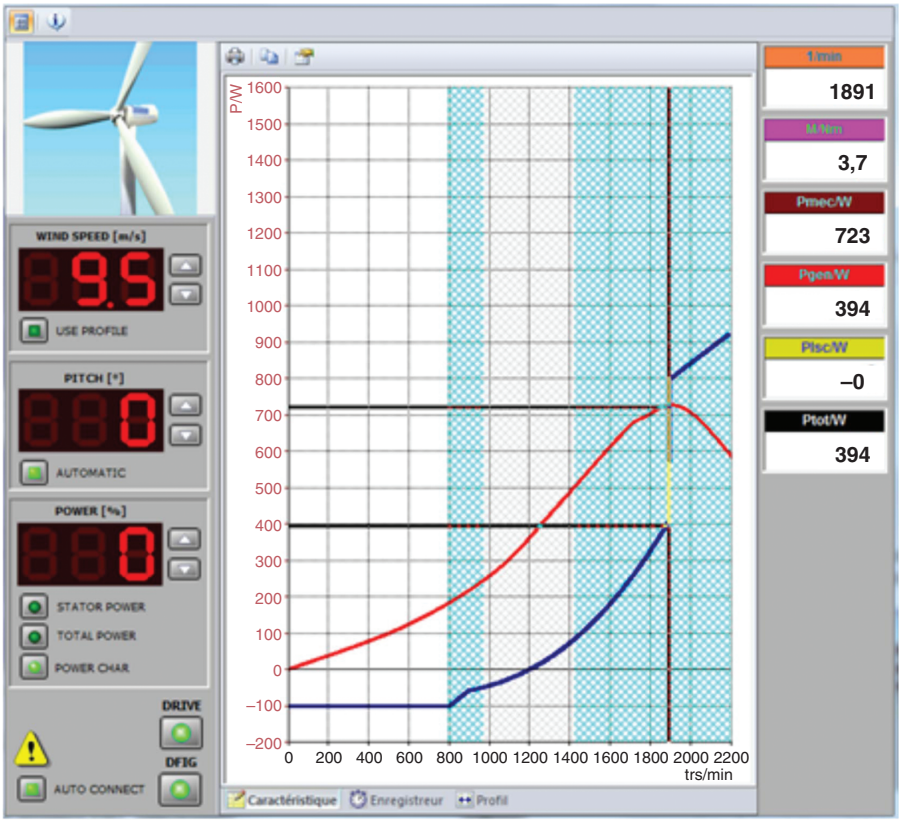

Fig. 13: Control centre instrument of the 'LabSoft Classroom Manager' platform.

parameters for the Type-3 DFIG-based WT and those for the DVR. The ranges defined in the block diagram of Fig. A1 and the tuning recommendations provided in [42, 50, 51] guide the trial-and-error procedure used to find the numerical values of the tuning parameters of the different ADRC controllers designed.

Two symmetric fault scenarios are simulated to assess the performance of the system planned to meet LVRT capability standards. The first test evaluates the LVRT capabilities of the Type-3 WT for a symmetrical voltage drop lasting for 7.5 cycles of between 0.5 and 0.65 s and corresponding to 35% of the rated voltage. The second examines the Type-3 WT–DVR behaviour in the case of a 150-ms utility grid short circuit. These tests are carried out with the assumption of a 10-m/s constant wind speed and assuming that the disruption of the grid is too short to cause any discernible variations in this speed. In addition, the generated reactive and real power are 0 and 0.6 pu, respectively.

Fig. 10 presents the experimental set-up of a Type-3 WT emulator used to validate the simulation results. The behaviour of a WT is emulated by the 1-kW servo-motor test bench and controller. This test bench comprises a numerical control unit, a brake and AktiveServo software along with the comprehensive control system for the analysis of the electrical machine and the drive. The 1-kVA, 400 V/300 V three-phase transformer is used to connect the Type-3 WT to the grid. The digital/analogue

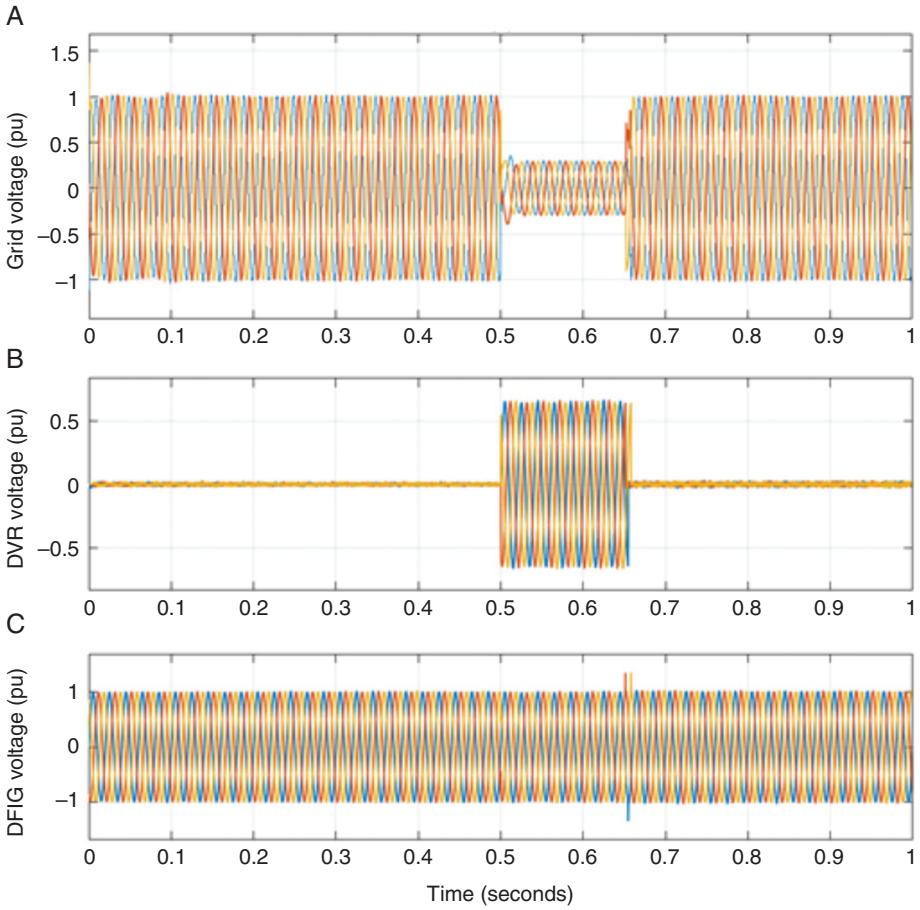

Fig. 14: A voltage drop of 35% on the power grid. (a) Mains voltage; (b) DVR-generated compensating voltage; (c) DFIG terminal voltage.

multimeter is a miniature data acquisition system for recording the root mean square and harmonic distortion of the current and voltage, as well as active, reactive and apparent power and power factor. The control unit permits the simulation and analysis of all practically relevant states. Fig. 11 depicts the control unit configuration that includes: (i) two three-phase inverters (PSS20S92F6-AG IGBT modules) for the operation of the DFIG (0.8 kW) in sub-synchronous and over-synchronous modes; (ii) integrated power switch for connecting the generator to the grid (Finder 43.41.7.012.2000 Relay); (iii) manual and automatic grid synchronization; (iv) integrated braking chopper for LVRT experiments. All control system objectives are carried out by a digital signal processor (DSP) TMS320F28335 using outputs from voltage sensors (FL24/12 and FL 2/6) and current sensors (CDS4010ABC). The grid fault simulator is a voltage sag generator (VSG) that is used to verify and simulate the LVRT capability of the wind emulator. Combining a step-down autotransformer with some switches is the optimal solution to implement a VSG in this case.

Fig. 12a depicts the structure of a typical transformer-based VSG. Suitable control sequences can be applied to the switch S2 in order to generate a voltage drop of the desired magnitude and duration. Opening the switch S1 produces a voltage sag of 100%. The VSG installed in this bench is illustrated in Fig. 12b. The autotransformer V-21009-016-0002$_B$ is utilized. It can generate four voltage fluctuations of 20%, 40%, 60% and 100% with a configurable duration of 0–300 ms.

Fig. 13 illustrates the experimental test settings in which the wind emulator is driven at a constant wind speed of 9.5 m/s, the DFIG works in super-synchronous mode at 1891 rpm and the maximum available power is 394 W.

4 Results and discussion

4.1 Simulation Test 1: Network voltage drop of 35% of its nominal voltage

Figs 14 and 15 depict the performance of the Type-3 WT with DVR during a symmetric 35% voltage drop. Fig. 14a shows a symmetric voltage disturbance with a duration of 150 ms beginning at time 0.5 s in the power system. Fig. 14b illustrates how the DVR quickly (15 ms) provides the compensating voltage. Therefore, the voltage across the DFIG remains almost constant, as shown in Fig. 14c.

The corresponding impact on the WT–DFIG parameters is presented in Fig. 15. As illustrated in Fig. 15a, the active power decreases and the reactive power increases in accordance with grid codes [9, 10]. After brief fluctuations, the active and reactive powers rapidly stabilize. After fault clearance, these powers will experience brief transients, after which the active power will recover to its steady value at a predetermined rate while the reactive power (around zero) will recover instantaneously. Fig. 15b and c reveals that the stator and rotor current magnitudes are less than the 2-pu threshold stipulated by the LVRT criterion. The DC bus voltage in Fig. 15d maintains a constant value and

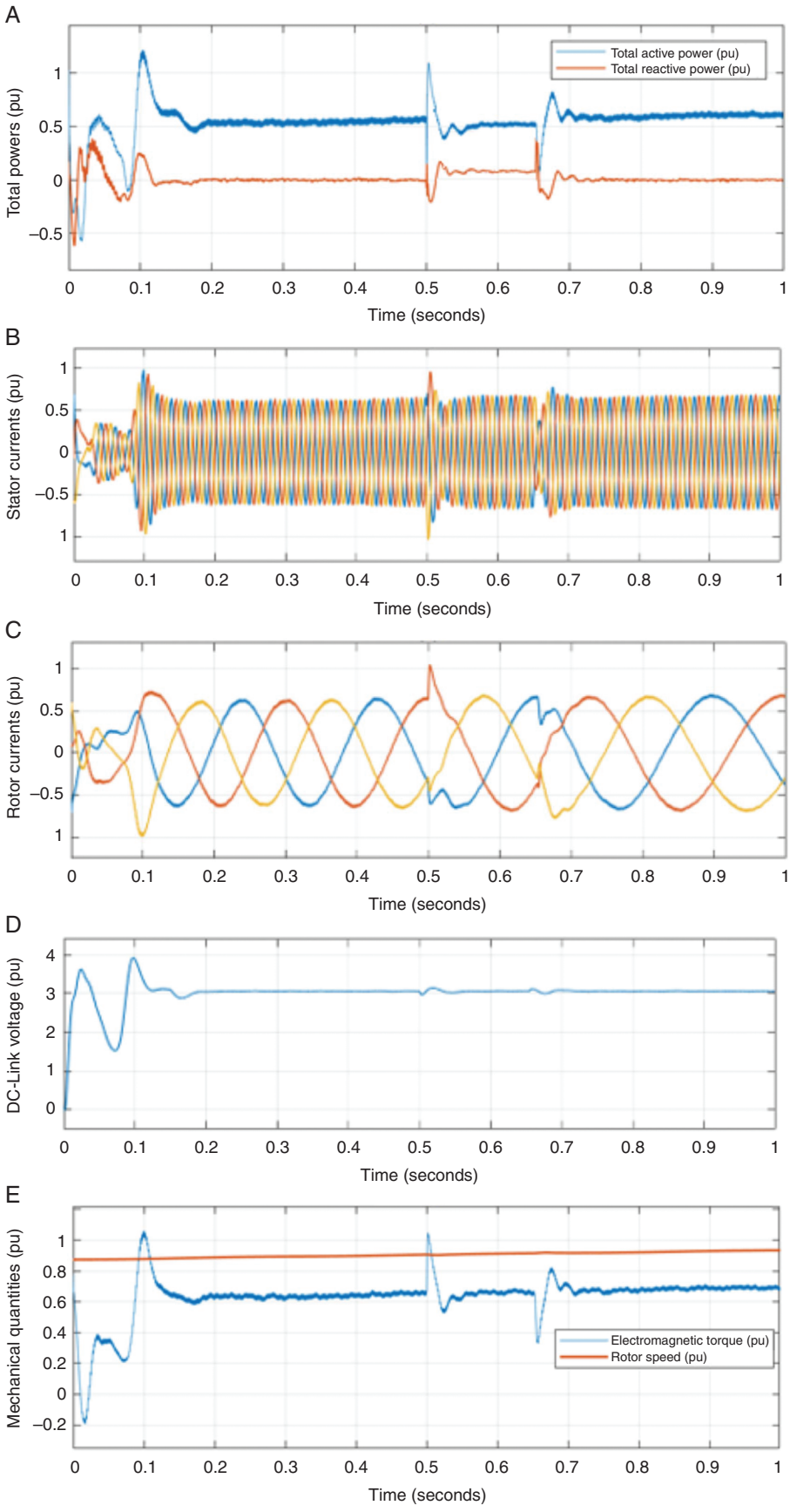

Fig. 15: (a) DFIG real and reactive power in pu; (b) stator currents in pu; (c) rotor currents in pu; (d) DC-link voltage in pu; (e) electromagnetic torque and rotor speed in pu.

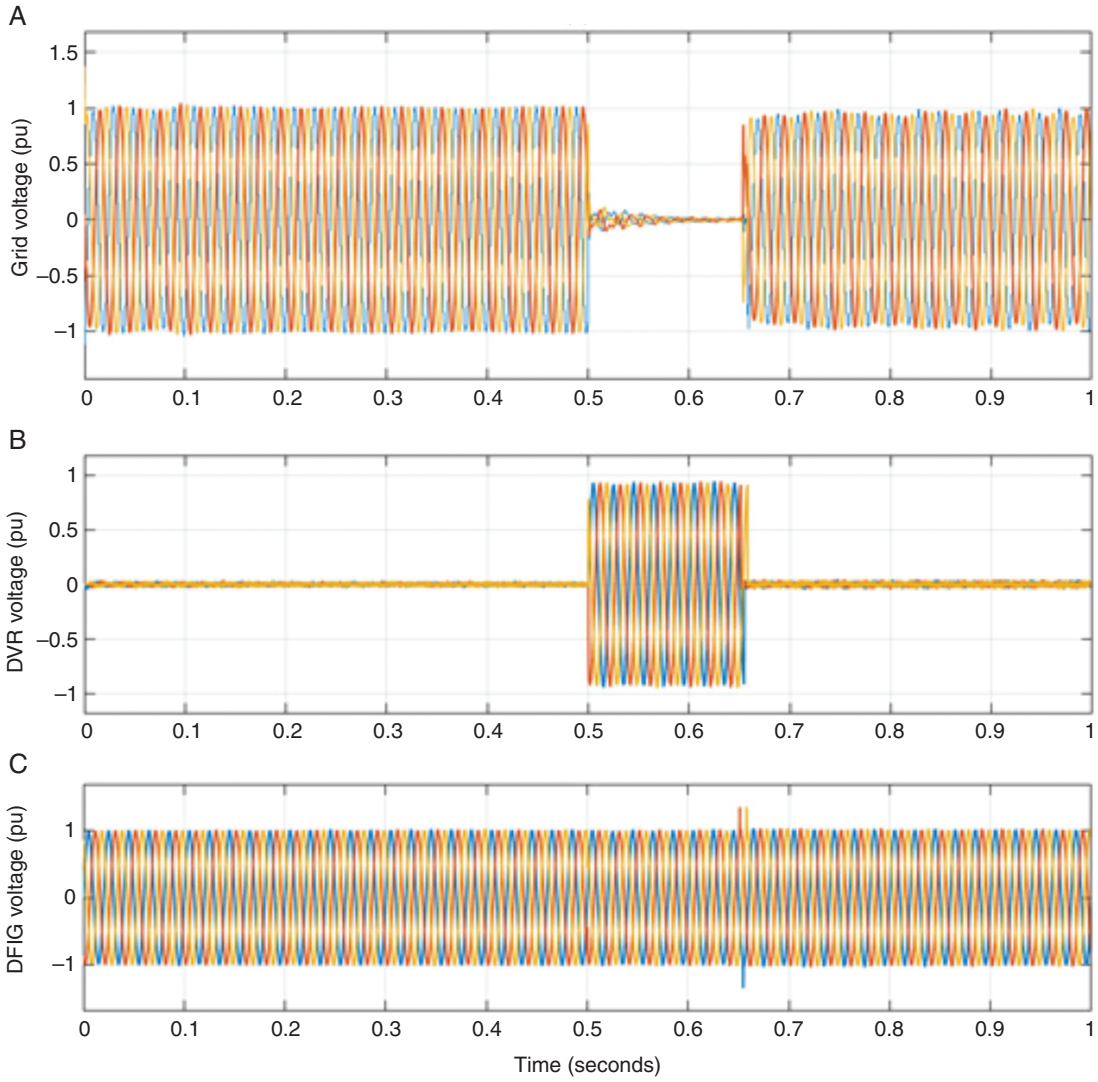

Fig. 16: Voltage drop of 95% on the power grid. (a) Network voltage; (b) DVR-generated compensating voltage; (c) DFIG terminal voltage.

any variation is well below the 1.35-U_{DC} level that the grid code criterion allows during voltage dips.

Fig. 15e illustrates the behaviour of the mechanical components, DFIG rotor speed and electromagnetic torque. The rotor speed is almost immune to disturbances. On the electromagnetic torque graph, oscillations are seen at the beginning and end of the fault, but their peak value is far below the limit of 2–2.5 pu provided by the LVRT network code.

These simulation results indicate that the ADRC approach controlling the DVR protects the Type-3 WT from high transient voltages and currents, and maintains connection to the grid throughout a 35% voltage sag.

4.2 Simulation Test 2: Network voltage drop of 95% of its nominal voltage

This test replicates a near-short circuit with a 95% drop in voltage. As seen in Fig. 16, the dynamics of the system are similar to the previous test (with a 35% voltage drop). Fig. 16b reveals that the DVR instantaneously adjusts the voltage drop across the DFIG (Fig. 16c) boosting the safety of the Type-3 WT and, in particular, enhancing its LVRT capabilities.

Fig. 17 displays the important quantities of a Type-3 WT that are restricted by the LVRT requirement in the majority of grid codes in a number of countries to safeguard the components of the WT while maintaining grid connection following a failure.

Fig. 17a–e shows the point of common coupling (PCC) active–reactive powers, rotor and stator DFIG currents, DC bus voltage and mechanical quantities, respectively. All these parameters exhibit oscillations, particularly during fault onset and fault clearing. Despite the fact that the magnitude of these oscillations is higher than that of the previous test, they are well within the grid standards for LVRT capability constraints for a Type-3 WT.

Table 2 presents the simulation results of the WT parameters at the beginning of the voltage drop along with the reactive power supply provided by the Type-3 WT.

Simulation results indicate that a DVR controlled by using the ADRC technique significantly increases the LVRT capabilities of a Type-3 DFIG-based WT under symmetrical voltage dip events. Although setting up ADRC controllers might be challenging, this method has been shown to be extremely

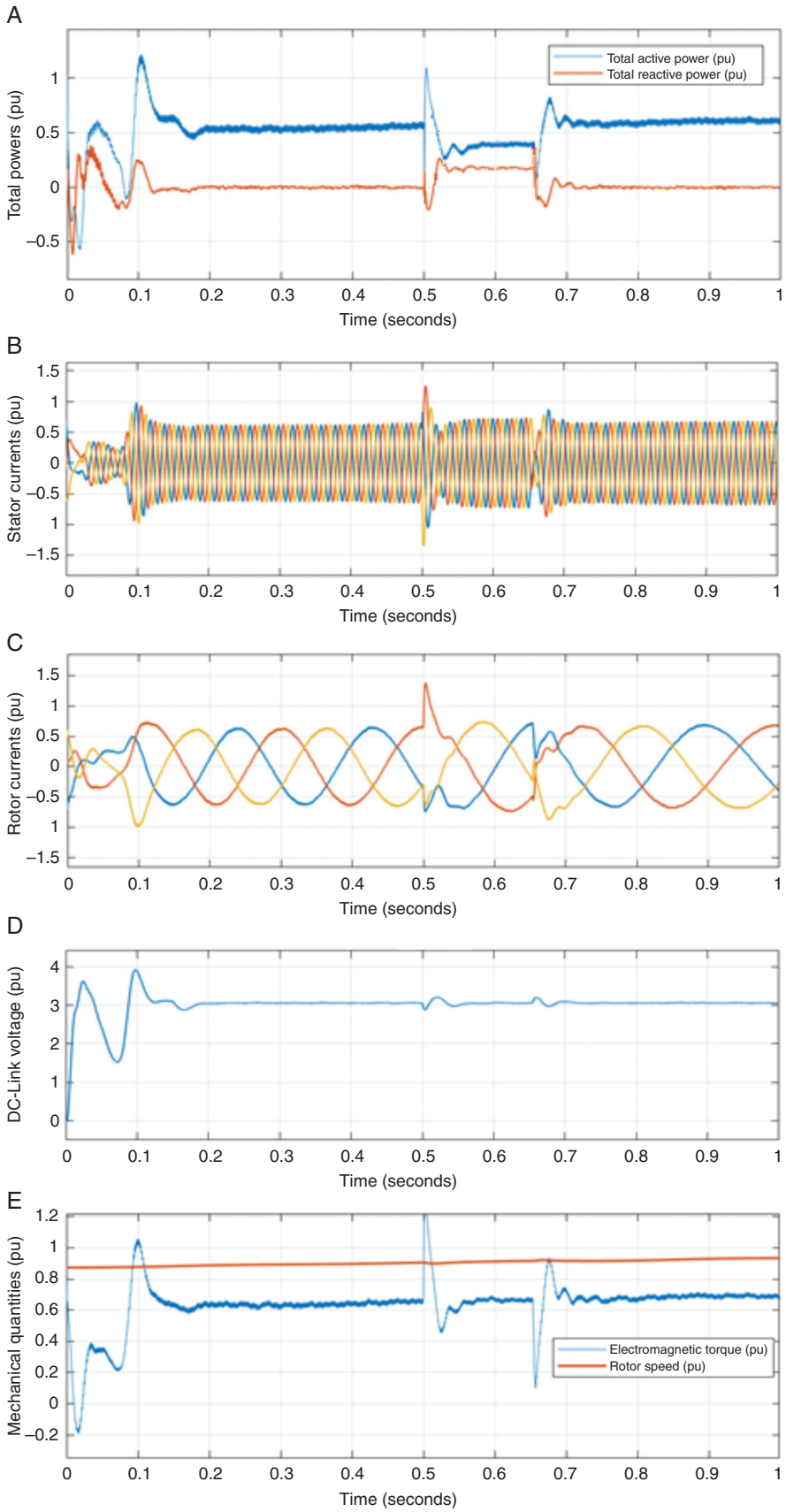

Fig. 17: (a) DFIG real and reactive power in pu; (b) stator currents in pu; (c) rotor currents in pu; (d) DC-link voltage in pu; (e) electromagnetic torque and rotor speed in pu.

Table 2: Peak of the Type-3 WT main parameters and reactive power supplied characteristics

Voltage drop (pu)	Peak (in pu) of				Reactive power supplied	
	Rotor current (<2 pu)	Stator current (<2 pu)	DC-link voltage (<1.35 U_{DC})	Electromagnetic torque (<2...2.5 pu)	Transient duration (ms)	Value (pu)
0.35	0.92	1.05	1.05 U_{DC}	1.05	20	0.15
0.95	1.25	1.4	1.09 U_{DC}	1.25	23	0.3

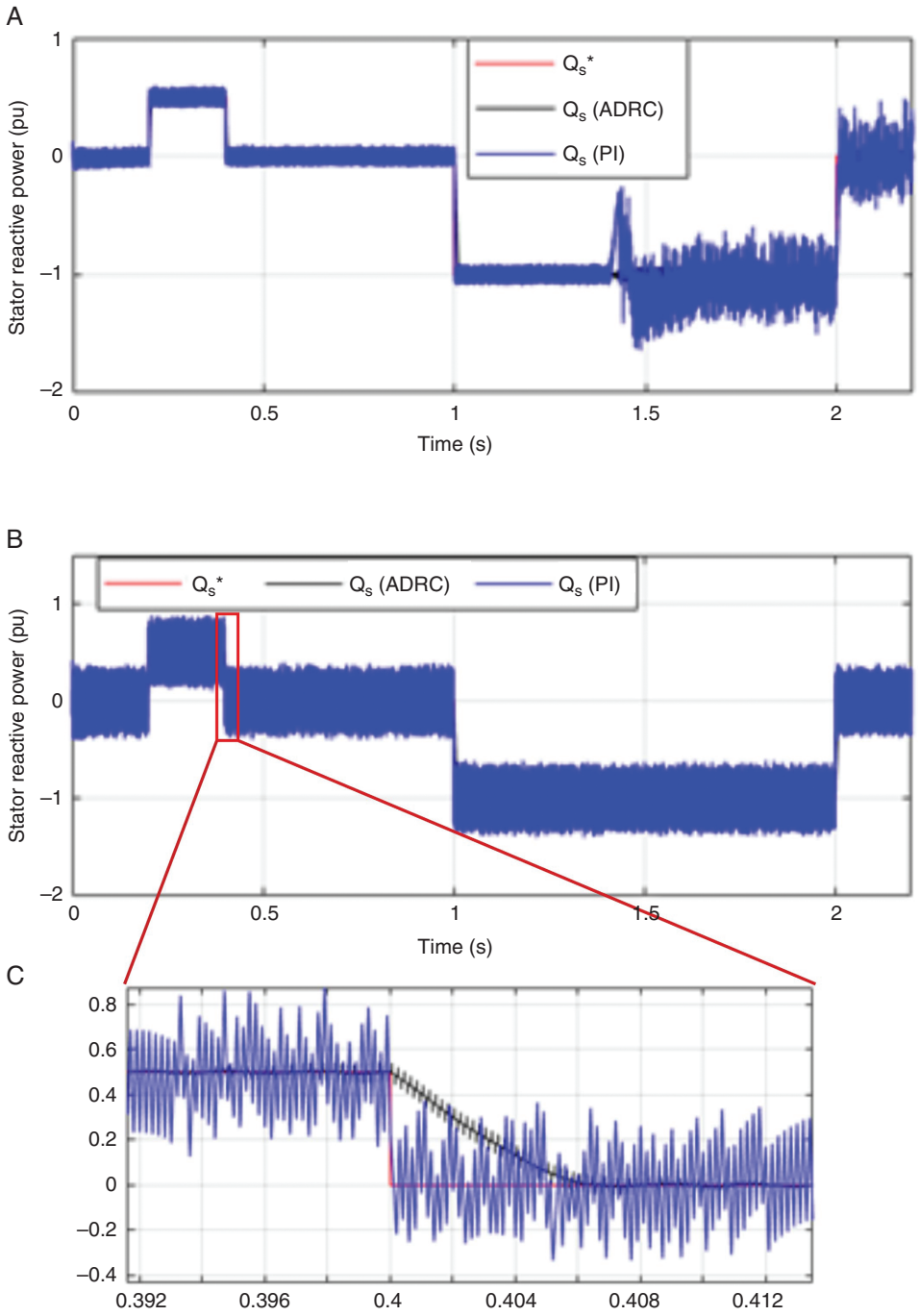

Fig. 18: Robustness tests. (a) Stator reactive power Q_s (external perturbation at 1.5 s); (b) Q_s (case of parametric variation: $R_r + 0.6R_r$ and $L_r - 0.4L_r$).

effective in reducing all kinds of internal and external disturbances. The DVR is strongly recommended for existing WTs that do not have enough LVRT capability, regardless of its expensive cost.

4.2.1 *Comparison with the PI controller*

The proposed ADRC controller is compared with the PI controller to highlight the superior performance. Fig. 18 shows the comparative results of the ability of the two controllers to respond

Table 3: Integral of absolute error quantifier of PI and ADRC controllers

	IAE_{Qs}		
Controller	**No perturbation**	**External perturbation (sudden change of v_w)**	**Internal perturbation ($-0.4\ L_r - +0.6\ R_r$)**
PI	13.77×10^{-2}	21.88×10^{-2}	37.51×10^{-2}
Designed nonlinear ADRC	2.18×10^{-2}	3.13×10^{-2}	4.28×10^{-2}

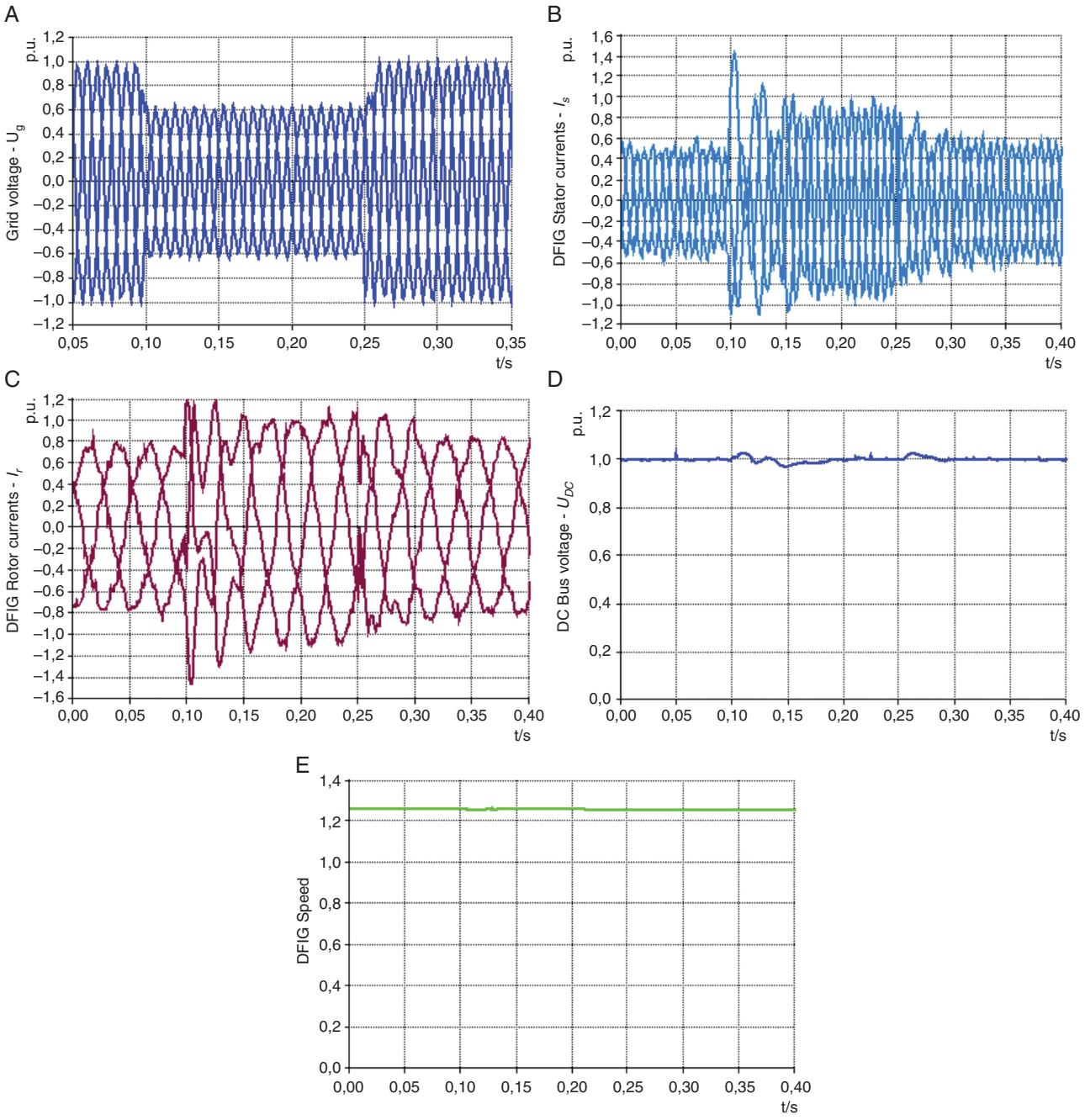

Fig. 19: Experimental results of typical quantities of the wind emulator under a 40% dip in the network voltage during 150 ms. (a) Grid voltage—U_g; (b) DFIG stator currents—I_s; (c) DFIG rotor currents—I_r; (d) DC bus voltage—U_{DC}; (e) DFIG speed.

to the set point for the reactive power Q_s on the stator. Clearly, the ADRC controller outperforms the PI controller in terms of better reference tracking and reduced transients. Fig. 18a illustrates the reactive power Q_s of each controller when there is an abrupt change in wind speed, considered an external disturbance, starting at time $t = 1.5$ s. The PI regulator fails to adequately decouple the active power (P_S) and reactive power (Q_s) controls, whereas the ADRC meets this criterion. Fig. 18b and its zoomed-in portion depict the waveform of the Q_s responses of the two controllers during a parametric variation in the intrinsic quantities of the system (in this case, R_r and L_r). The Q_s of the ADRC effectively follows the

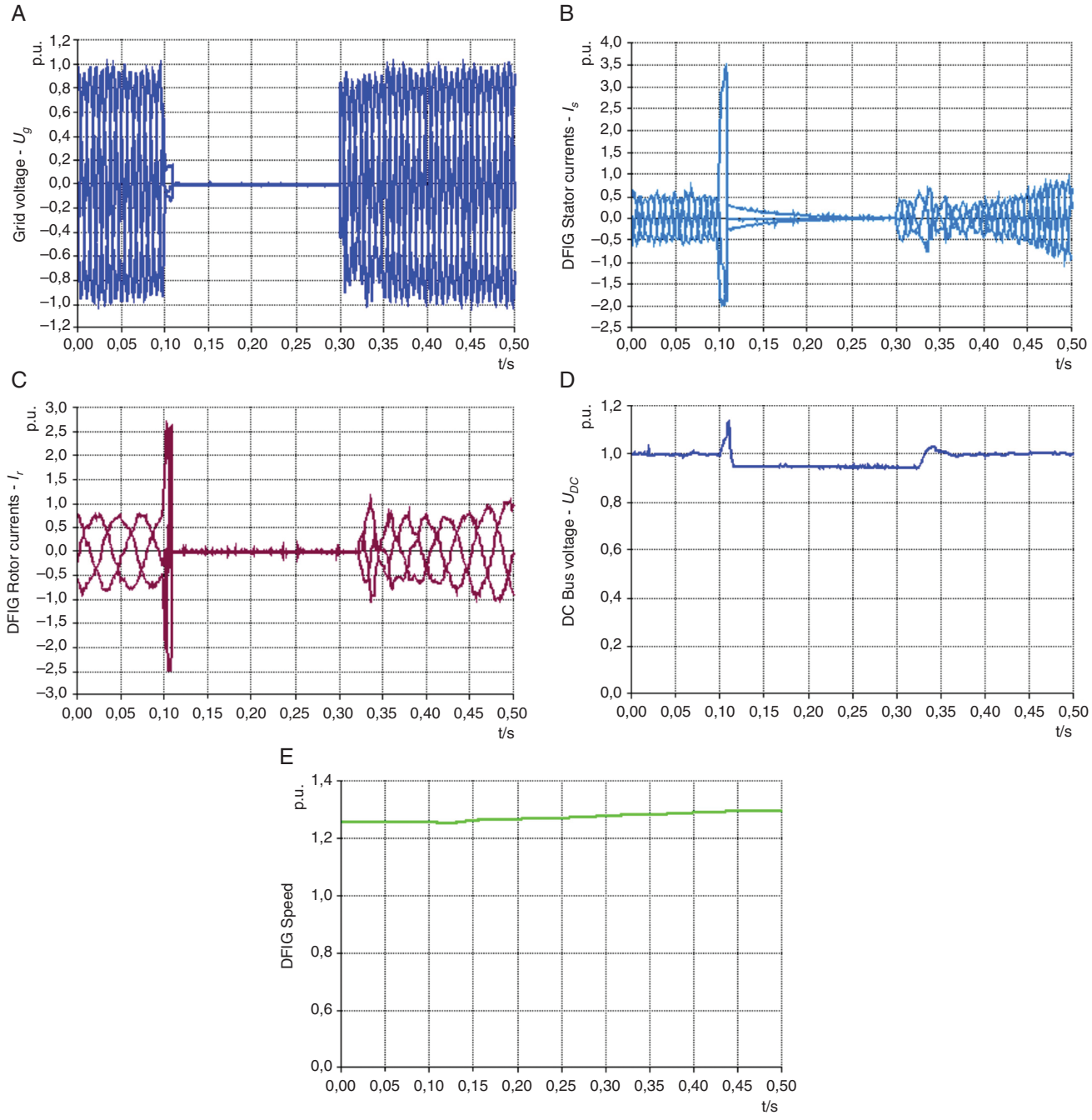

Fig. 20: Experimental results of typical quantities of the wind emulator under a short circuit in the network for 150 ms. (a) Grid voltage—U_g; (b) DFIG stator currents—I_s; (c) DFIG rotor currents—I_r; (d) DC bus voltage—U_{DC}; (e) DFIG speed.

designated point whereas the Q_s of the PI oscillates noticeably around it.

The integral of absolute error performance index (**IAE**$x = \int |x - x_{ref}|dt$, where $x = Q_s$) is evaluated for each test conducted with the PI and ADRC controllers. The IAE_{Qs} values in Table 3 demonstrate that the ADRC control strategy is more precise than the conventional PI control strategy.

4.2.2 *Experimental Test 1: Symmetrical voltage sag of 40% of the nominal voltage*

The first step in the preliminary operations of this experiment is the manual tuning of the VSG to 40% of U_n for each phase of the grid to have a symmetric sag. The actions are then successively carried out to start the emulator, synchronize it with the grid and set it to the appropriate operating point (9.5 m/s—394 W). The aforementioned voltage sag is activated for 150 ms starting at 0.1 s.

Table 4: Type-3 WT main parameters peak

	Peak (in pu) of		
Voltage drop (in pu)	**Rotor current (<2 pu)**	**Stator current (<2 pu)**	**DC-link voltage) (<1.35 U_{DC})**
0.40	1.43	1.2	1.03 U_{DC}
1.00	3.5	2.5	1.15 U_{DC}

Table 5: Benefits and drawbacks of investigated LVRT methods

LVRT solution	Benefits (+) and drawbacks (–)
DVR (simulations)	+ Eliminates generator current and power transients in the event of a grid failure + Reduces the stator power reference + Rapid voltage recovery and a reactive supply that can be controlled – To prevent voltage drops, large energy storage capacity is required – Expensive solution
Crowbar and DC chopper (experiments)	+ Activated during fault conditions to avoid RSC over-current + Inhibits DC-link voltage changes and expands the standard working range of the DFIG – Probability of control inactivation of RSC – The time to disable the converter and restore it is slower

Table 6: Impacts of LVRT enhancement techniques on DFIG–WT. √: Within the acceptable range as per the grid code; χ: not within the range specified by the grid code.

LVRT enhancement techniques	ADRC-controlled DVR (simulation results)	Crowbar and DC chopper (emulator experiments)	ADRC-controlled DFIG flux [9] (simulation results)
Rotor current peak	√	√	√
Rotor current oscillations	√	√	χ
Stator current peak	√	χ	√
Stator current oscillations	√	χ	χ
DC-link voltage peak	√	√	√
DC-link voltage oscillations	√	√	χ
Electromagnetic torque	χ	χ	√
Reactive power support	√	χ	√

Fig. 19 presents the impact of a 40% voltage drop on the emulated Type-3 WT parameters. Fig. 19a shows the voltage at the PCC and demonstrates how the voltage. VSG can provide the appropriate sag with precision. Due to the active crowbar block, the currents in the DFIG stator and rotor are below their maximum limit, as shown in Fig. 19b and c. It is noticed that the voltage drop at the PCC leads to an increase in the current to compensate for the reduced voltage drop and the reduced amount of power delivered to the network.

Almost no change is observed in the DC bus voltage in Fig. 19d due to the activation of the DC chopper during the fault. Fig. 19e demonstrates the negligible effect of the voltage drop on the DFIG speed.

4.2.3 *Experimental Test 2: Symmetrical voltage dip of 100% of the nominal voltage*

To prepare for the experiment, the VSG is manually set to 100% of U_n (short circuit) for each network phase. The voltage drop described above is triggered for 200 ms starting at 0.1 s.

Fig. 20 shows the influence of the most severe voltage drop (short circuit) on key quantities of the Type-3 WT emulator. Fig. 20a, which shows the voltage at the PCC point, illustrates the ability of the VSG to produce a short circuit across the DFIG. Fig. 20b shows the stator current pattern during the failure, which indicates that the power generation of the emulator to the grid has been interrupted. Fig. 20c shows that the rotor is no longer powered ($I_r = 0$) and the DFIG is unmagnetized.

At the onset of a short circuit at the PCC, current peaks are seen in the rotor and stator; however, these current peaks are instantly attenuated by the activation of the crowbar. The DC-chopper damper circuit keeps the DC bus voltage within permitted limits, exhibiting robust fault behaviour as seen in Fig. 20d. A slight increase in the DFIG speed is observed in Fig. 20e due to the absence/reduction of the load torque (network).

Table 4 displays the peak values of the critical parameters of the Type-3 WT at the onset of the voltage drop, as determined by using experimental tests. On the basis of these tests, the crowbar at the DFIG rotor terminals and the DC-chopper absorber at the DC bus terminals enable the WT emulator to retain grid connection during voltage drops at the PCC (induced by the VSG). During its voltage drop fault, this emulator is unable to produce reactive power to sustain the grid voltage.

Table 5 lists the advantages and disadvantages of the LVRT capability of a DFIG-based WT system under the influence of DVR integration, crowbar and DC-chopper integration. Table 6 outlines the impacts of LVRT capacity improvement techniques on critical DFIG WT quantities as a consequence of a power system voltage drop.

5 Conclusions

In this paper, DVR has been proposed as a means of enhancing the LVRT capability of Type-3 WTs. The system configuration and its control scheme are designed and simulations are conducted under fault operation conditions to test the system performance. In addition, experiments are conducted in the order of comparison and verification. The key findings are as follows: (i) a series compensation scheme utilizing a DVR is very effective for voltage control; (ii) during the initial phase of a voltage drop, the over-currents in the stator and rotor of the DFIG are effectively suppressed; (iii) the voltage fluctuations at the DFIG terminal and DC link are within acceptable limits; (iv) the fluctuation in the electromagnetic torque is reduced.

The use of a DVR can considerably enhance the LVRT capability of the wind energy conversion system (WECS) under symmetrical voltage fault conditions and it is ideally suited for Type-3 WTs with insufficient LVRT capability that have already been implemented. However, combinations of proposed solutions must be investigated to achieve the maximum requirements of the LVRT grid codes. Further research is required on the DVR's treatment of asymmetric voltage sag and techniques for reducing the power rating of the DVR.

Nomenclature

Ω	Rotation speed (rad/s)
Γ	Torque (Nm)
β	Pitch angle (°)
λ	Tip speed ratio
D, q	Subscripts of dq-axis frame
s, r	Subscripts of DFIG stator and rotor, respectively
B	Subscript of base value
H	Total inertia constant (s)
f_v	the viscosity coefficient
p	number of pole pairs in the generator
I, V, Ψ	Current (A), voltage (V), flux (Wb), respectively
R, L, C	Resistance (Ω), inductance (H), capacitance (F), respectively
ω	Pulsation (rad/ s)
σ	DFIG dispersion coefficient
S, P, Q	Apparent (VA), real (W), reactive (VAR) power, respectively

Conflict of interest statement

There is no conflict of interest among authors.

Data Availability

All data used to support the findings of this study are included in the article.

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Appendix

Table A.1: Setting controller parameters[a]

Controller of	Control variable		Parameters
DVR-side converter	V_{cdq}	NLESO	$b_\Omega = 45 \times 10^{-3}$ pu $\beta_{\Omega 1} = 76$ $\beta_{\Omega 2} = 58\,900$ $\alpha_1 = 1$, $\alpha_2 = 0.5$, $\delta = 0.005$
		NLSEF	$\beta_{\Omega 0} = 3 \times 10^4$ $\alpha_{\Omega 0} = 0.75$, $\delta_{\Omega 0} = 0.0045$
	I_{fdq}	NLESO	$b_r = 5643.4$ pu $\beta_{r1} = 200$, $\beta_{r2} = 10^9$ $\alpha_1 = 1$, $\alpha_2 = 0.5$, $\delta = 0.005$
		NLSEF	$\beta_{r0} = 15 \times 10^4$ $\alpha_{r0} = 0.85$, $\delta_{r0} = 0.0075$

[a]The adjustment settings of the other RSC and GSC controllers are given in [47].

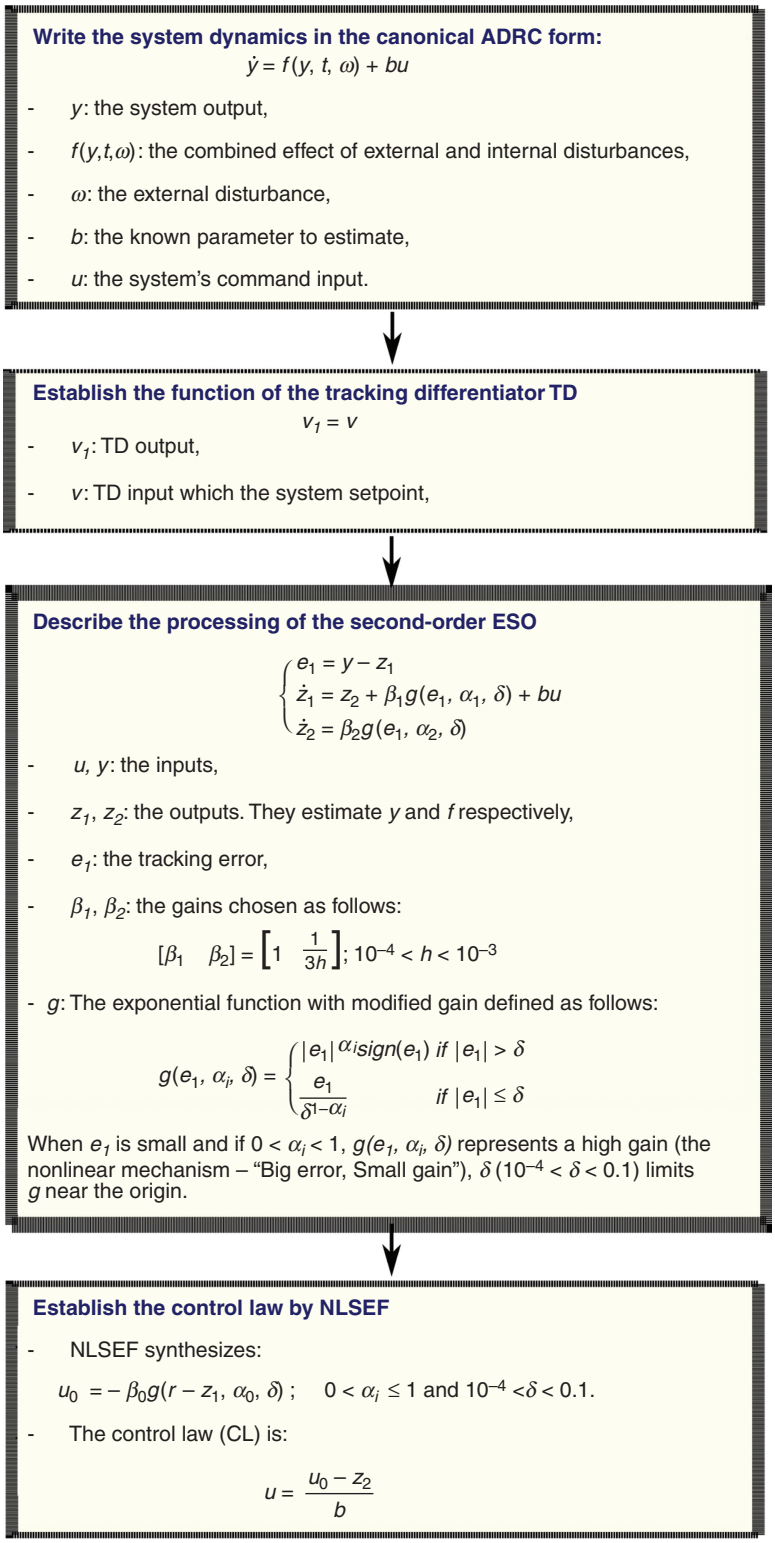

Fig. A.1: Flowchart for application of the ADRC approach.