An Ultra-Low-Voltage class-AB OTA exploiting local CMFB and Body-to-Gate interface

Francesco Centurelli, Riccardo Della Sala*, Pietro Monsurrò, Pasquale Tommasino, Alessandro Trifiletti

Università di Roma La Sapienza, DIET Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni, 00184 Roma, Italy

Abstract

In this work a novel bulk-driven (BD) ultra-low-voltage (ULV) class-AB operational transconductance amplifier (OTA) which exploits local common mode feedback (LCMFB) strategies to enhance performance and robustness against process, voltage and temperature (PVT) variations has been proposed. The amplifier exploits body-to-gate (B2G) interface to increase the slew rate and attain class-AB behaviour, whereas two pseudo-resistors have been employed to increase the common mode rejection ratio (CMRR). The architecture has been extensively tested through Monte Carlo and PVT simulations, results show that the amplifier is very robust in terms of gain-bandwidth-product (GBW), power consumption and slew rate. A wide comparison against state-of-the-art has pointed out that best small-signal figures of merit are attained and good large-signal performance is guaranteed, also when worst-case slew rate is considered.

Keywords: Body-Driven, OTA, CMRR, Class-AB, Ultra-Low-Voltage, Ultra-Low-Power.

1. Introduction

The recent years have seen an ever-increasing diffusion of novel and smart electronic applications, pervading all aspects of daily life. Many fields of applications have been completely rethought thanks to the ever increasing inno-

*Corresponding author

vation of biomedical [1, 2, 3, 4] and Internet of Things (IoT) apparatuses such as portable and wearable devices, and smart sensors [5]. These architectures demand for low power consumption, to extend battery life or to be able to operate on harvested energy sources. Furthermore, in biomedical applications an excessive power consumption would imply system overheating that would cause irreversible damages [2, 4]. All this has motivated a strong interest in the research of Ultra-Low-Voltage (ULV) and Ultra-Low-Power (ULP) electronics, driving power consumption to ever lower values.

The operational transconductance amplifier (OTA) is a key building block for analog applications, and is among the most challenging and hard-to-design architectures in the ULV and ULP context [5]. Several solutions have been proposed in the literature to allow operation at very low supply voltages and to minimize power consumption without compromising performance.

This ULV context requires suitable techniques and a careful design to guarantee good small-signal and large-signal performance with a rail-to-rail signal swing. Cascoding and gain-boosting can still be exploited at supply voltages lower than 1V to improve the performance of the OTA, but their use becomes impossible when the supply voltage drops to 0.5V or lower, thus leading to the use of multistage amplifiers to achieve the required gain[6]. In [7], state-of-the-art small- and large-signal figures-of-merit (FOMs) have been achieved by designing the OTA as a cascade of low-gain stages without high-impedance internal nodes. Body-biasing techniques can be exploited [8] to set the bias current without losing voltage headroom for the tail current generator. However, at extremely low supply voltages, body-biasing techniques become ineffective due to the limited body transconductance gain, that would require a voltage swing higher than the supply voltage to compensate variations and fix the bias point. The most recent trend for ULV OTAs is to use non-tailed body-driven stages [9, 10, 11, 12, 13, 14]. Indeed, at supply voltages lower than 0.5V, body-driven stages are typically used instead of gate-driven (GD) ones, to allow a large input common mode range (ICMR) [9, 15]. These architectures exploit the gate terminals to set the bias current, since gate transconductances are high enough

to allow large control range even with the reduced voltage swing set by the supply voltage. Main drawbacks of the body-driven approach are higher noise, lower bandwidth and worse slew rate (SR) performance for a given bias current. Recently, the "digital OTA" approach has also been proposed, it allows linear amplification through the use of pulsewidth modulation (PWM) and exploits only digital standard-cells [16]. Also floating-gate and quasi-floating-gate [17] approaches are viable alternatives to design ULV OTAs.

To minimize power consumption, one of the most used and effective biasing techniques is the subthreshold region operation, which is often adequate for most applications, resulting in an extremely low static power consumption and demanding for $|V_{gs}|$ lower than the threshold voltage. Further power reduction can be achieved by exploiting class-AB operation, because it allows to bias circuits at low quiescent currents, mainly determined by the required small-signal performance, and guarantees peak currents large enough to provide a fast response to step input variations. In order to attain class-AB behaviour at low supply voltages, standard approaches are the use of adaptive biasing techniques [18] or topologies like the ones of Peluso [19] in GD [20] or BD [21] configuration as well as BD flipped voltage follower stages [22]. It is worth noting that setting a stable DC bias point and achieving class-AB behaviour are often contrasting requirements: in particular at very low supply voltages the gate-bias would maintain the common mode current approximately constant.

Inverter-based stages intrinsically provide a class-AB behaviour [23], due to the characteristics of CMOS inverters and, because of this, combined with BD techniques are among the most promising architectures [24, 25, 26]. Thanks to these approaches, voltages down to 0.25V could be guaranteed and many works have been proposed in literature [26, 27].

In this paper we present a novel OTA topology for ULV and ULP applications, that exploits body input to achieve a rail-to-rail input range, and a local common mode feedback (LCMFB) combined with current cancellation to improve the CMRR, providing good performance also under process, voltage and temperature (PVT) variations. A body-to-gate interface is used as a novel

non-linear current mirror and has been exploited to boost the output current, achieving class-AB behaviour with good efficiency. The overall architecture is that of a symmetrical OTA, able to drive large capacitive loads. The OTA has been simulated in a 130nm CMOS technology by STMicroelectronics, achieving state-of-the-art FOMs.

The paper is structured as follows: Section 2 introduces the proposed OTA topology, whose circuit analysis is reported in Section 3. Section 4 deals with design and simulation results, and conclusions are drawn in Section 5.

2. Topology

Fig. 1 shows the topology of the proposed OTA, and the implementation of the two (matched) resistors by means of pseudo-resistors composed of two devices biased in deep subthreshold region.

The input stage ($M_{n_{1,2}}$) is a BD pseudo-differential pair, biased by the gate terminals with voltage V_b, generated by a biasing circuit which is composed of M_{n_b}. Because of gate-biasing, the bias current of the stage is well defined, and because of body-driving, the input common mode signal swing is rail-to-rail (at 0.3V supply, forward biasing of the body diodes is negligible). Body-driving comes at a cost in terms of gain, bandwidth and noise performance, but it is necessary in ULV applications due to the limited signal swing of GD stages, and the poor performance of body-biasing in pseudo-differential stages.

The load ($M_{p_{1,2}}$) is composed of two PMOS devices whose gate is biased by the common mode signal by means of the two resistors R_1 and R_2 (implemented as in Fig. 2). For the differential mode, the gates of M_{p_1} and M_{p_2} are connected to ground, and the equivalent resistance at the drains of M_{n_1} - M_{n_2} is given by the parallel connection of the pseudo-resistor (which is very high), the output resistance of $M_{n_{1,2}}$ and $M_{p_{1,2}}$ (which is high), and the body transconductance of $M_{p_{1,2}}$ since it is body-diode connected. The pseudo-resistors allow to set the common mode voltage with a limited load effect at the output of the first stage: though they can be non-linear under large-signals, the available signal

swing is limited, because the only node with large (rail-to-rail) signal swing is the output, and the second stage has large gain. Hence, the first stage has a gain of $-g_{mb_{n_1}}/g_{mb_{p_1}} \approx -1$. For the common mode signal, however, M_{p_1} and M_{p_2} form a diode load, as the gate and drain voltages are the same (at low frequencies), and the load admittance is the g_m of the PMOS devices. Hence, the common mode gain is much lower, about $-g_{mb_{n_1}}/g_{m_{p_1}}$. This improves the CMRR of the device. Usually this local CMFB (LCMFB) is exploited to achieve class-AB behaviour [28], however in this case the body-diode connection masks this effect. Such connection is needed to achieve an internal low impedance node, thus increasing the bandwidth for a given phase margin.

The second stage ($M_{p_{3,4}}$ with the GD current mirror $M_{n_{3,4}}$) is a differential-to-single-ended stage with large gain, which sets the bandwidth of the system because of the gain of the current mirror, the large output resistance and the load capacitance. This stage also sets the gain of the OTA. For the differential signal, the two signal paths from M_{p_3} and M_{p_4} sum in phase, thus doubling the differential gain, whereas for the common mode signal the two paths are in phase opposition, thus cancelling most of the common mode gain. This technique further improves the CMRR.

The first stage bias currents are accurately set by the gate biasing of $M_{n_{1,2}}$, whereas the second stage is set by the output of the first stage, which for the common mode voltage operates as a GD current mirror ($M_{p_{1,2}}$ vs $M_{p_{3,4}}$). A small error arises in $M_{n_{1,2}}$ under the input signal because of variations in the body voltages, and in the second stage because of the same reason, as the body voltages of M_{p_1} and M_{p_3} are not the same.

Transistors M_{p_1} and M_{p_3} form a non-linear current mirror, with a body-connected diode that drives the gate of the output stage. A suitable sizing of the devices allows setting the DC current of the output stage, but dynamic current variations are amplified non-linearly, thus resulting in a class-AB behaviour.

By expressing the subthreshold current as $I_{d_p} = I_{0_p} \exp\left(\frac{V_{sg}-|V_{th}|}{nU_t}\right)$ and approximating the threshold voltage as $|V_{th}| = V_{th_0} - \alpha V_{bs}$ the output current

given by the body-to-gate (B2G) interface can be derived as:

$$I_{d_{M_{P_{3(4)}}}} = \left(\frac{I_{d_{M_{P_{1(2)}}}}}{I_{0_{P_{1(2)}}}}\right)^{\frac{1}{\alpha}} I_{0_{P_{3(4)}}} e^{\frac{(1-\alpha)V_{th_0}-V_g}{\alpha n U_t}} \quad (1)$$

where it has been denoted with $I_{d_{M_{P_i}}}$ the drain current of the i-th PMOS transistor. The usage of a BD input stage demands for a triple-well technology that however is not a concern since modern CMOS technologies allow this feature.

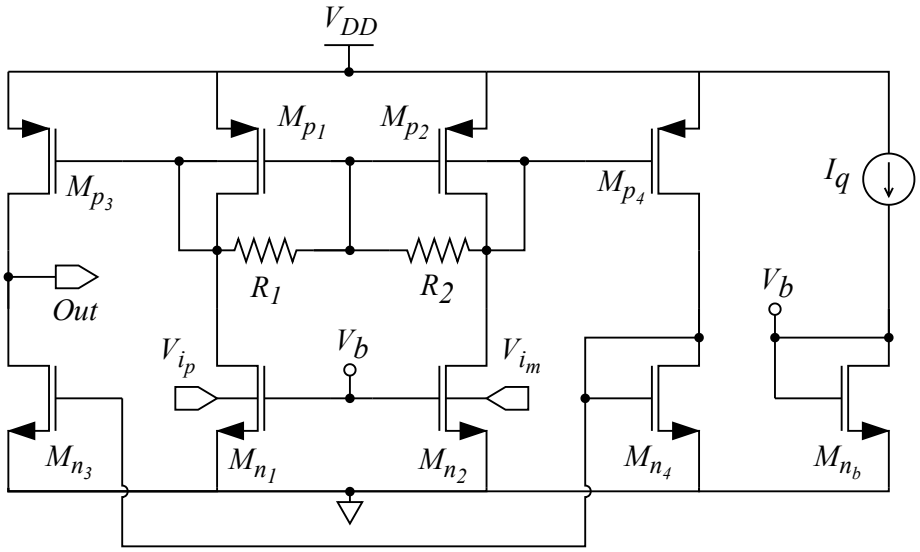


Figure 1: Schematic of the proposed OTA (where not explicitly shown, bodies are connected to $V_{DD}/2$).

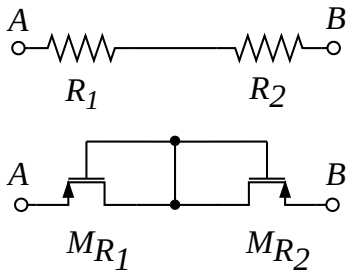


Figure 2: Implementation of the resistors.

3. Circuit Analysis

This section aims to analyze the performance of the proposed OTA, mainly focusing on small-signal and large-signal performance. Circuit analysis has been carried out and design choices have been highlighted by considering frequency response, SR and noise performance as well as DC-gain and CMRR.

3.1. Differential Gain

We refer to the small signal model of the circuit in Fig. 1 and by considering $R_1 = R_2 = R$, we derive the differential gain as:

$$A_{v_D} = \frac{g_{mb_{n_1}}}{g_{mb_{p_1}}} \frac{g_{mp_3}}{g_{ds_{p_3}} + g_{ds_{n_3}}} \frac{1 + s\tau_{zy}}{(1 + s\tau_{py})(1 + s\tau_x)(1 + s\tau_L)} \tag{2}$$

where:

$$\tau_{zy} \approx \frac{C_{gs_{n_4}} + C_{gs_{n_3}} + C_{gd_{n_3}} \cdot A_{v_{n_3}}}{2\ g_{m_{n_4}}} \tag{3}$$

$$\tau_{py} \approx \frac{C_{gs_{n_4}} + C_{gs_{n_3}} + C_{gd_{n_3}} \cdot A_{v_{n_3}}}{g_{m_{n_4}}} \tag{4}$$

$$\tau_x \approx \frac{C_{bs_{p_1}} + C_{gs_{p_3}} + C_{gd_{p_3}} \cdot A_{v_{p_3}}}{g_{mb_{p_1}}} \tag{5}$$

$$\tau_L \approx \frac{C_{gd_{p_3}} + C_{gd_{n_3}} + C_L}{g_{ds_{n_3}} + g_{ds_{p_3}}} \tag{6}$$

where $A_{v_{n_3}} = g_{m_{n_3}}/(g_{ds_{n_3}} + g_{ds_{p_3}})$ and $A_{v_{p_3}} = g_{m_{p_3}}/(g_{ds_{n_3}} + g_{ds_{p_3}})$. Furthermore, the following approximations are taken into account:

$$g_{mb_{p_1}} >> g_{ds_{p_1}} + g_{ds_{n_1}} + 1/R; \qquad g_{m_{n_4}} >> g_{ds_{p_4}} + g_{ds_{n_4}}; \tag{7}$$

and thus it follows that:

$$g_{m_{n_3}} + g_{m_{n_4}} >> g_{ds_{p_4}} + g_{ds_{n_4}}; \tag{8}$$

The DC gain could be split in two parts: $\frac{gm_{b_{n_1}}}{gm_{b_{p_1}}}$ which is set by CMOS technology and process variation, $\frac{gm_{p_3}}{gds_{n_3}+gds_{p_3}}$ which is the differential gain of a classic

differential pair.

The Gain-Bandwidth (GBW) product of the proposed OTA is given by:

$$GBW = \frac{1}{2\pi}\frac{g_{m_{p3}}}{C_L}\frac{g_{mb_{n1}}}{g_{mb_{p1}}} \tag{9}$$

It is worth noting that the overall GBW is that of a classic GD symmetrical OTA that typically operates at voltages greater than 0.3V. Due to the B2G interface, the architecture mitigates the drawbacks of BD OTAs and achieves larger transconductance which results in higher GBW. That behaviour has resulted in higher FOM_S as it will be shown later.

The phase margin can be computed as:

$$\varphi m \approx \frac{\pi}{2} - \arctan\left[\frac{C_{bs_{p_1}} + C_{gs_{p_3}} + C_{gd_{p_3}} \cdot A_{v_{p_3}}}{2\,C_L} \cdot \frac{g_{m_{p_3}}}{g_{mb_{p_1}}}\right] \tag{10}$$

where τ_{py} and τ_{zy} given by the current mirror $M_{n_{3,4}}$have been neglected.

3.2. Common mode rejection ratio

The common mode rejection ratio is mainly due to the ratio between the body and gate transconductances, thanks to the use of the LCMFB, and to the mirror common mode cancellation. The common mode gain of the OTA is:

$$A_{v_c} \approx \frac{g_{mb_{n_1}}}{g_{mb_{p_1}} + g_{m_{p_1}}}\left(\frac{g_{ds_{n_4}} + g_{ds_{p_4}}}{g_{m_{n_4}}}\right)\frac{g_{m_{p_3}}}{g_{ds_{p_3}} + g_{ds_{n_3}}} \tag{11}$$

and as a consequence the CMRR could be expressed as:

$$CMRR = \left(1 + \frac{g_{m_{p_1}}}{g_{mb_{p_1}}}\right)\frac{g_{m_{n_4}}}{g_{ds_{n_4}} + g_{ds_{p_4}}} \tag{12}$$

Therefore, the exploitation of pseudoresistors allows to improve the CMRR of the standard symmetrical OTA by a factor of about $g_{m_{p_1}}/g_{mb_{p1}}$ which depends on the CMOS technology.

3.3. PSRR Performance

In order to compute the PSRR of the architecture, the model depicted in Fig. 3 has been employed. The V_x voltage can be thereafter computed as:

$$V_x = \frac{g_{mb_{p_1}} + g_{ds_{p_1}} + g_{m_{p_1}}}{g_{mb_{p_1}} + g_{ds_{p_1}} + g_{m_{p_1}} + g_{ds_{n_1}}} V_{DD} \tag{13}$$

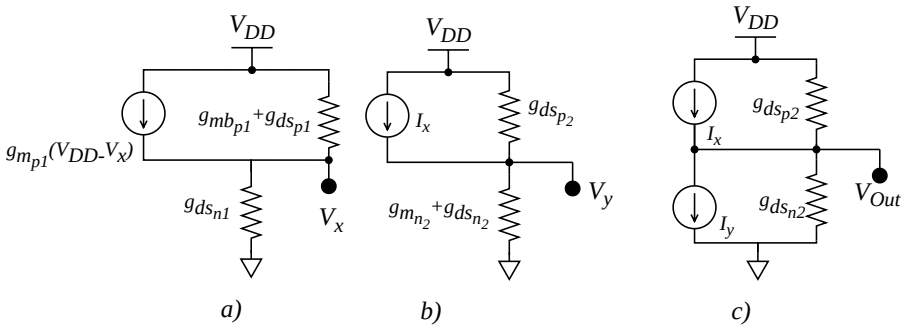


Figure 3: PSRR equivalent circuit employed for the first stage (a), for the mirror stage (b) and for the output stage (c).

Now the current I_x of the model depicted in Fig. 3b can be defined as:

$$I_x = g_{mp_2} \frac{g_{ds_{n_1}}}{g_{mb_{p_1}} + g_{ds_{p_1}} + g_{m_{p_1}} + g_{ds_{n_1}}} V_{DD} \tag{14}$$

With referring to Fig. 3b the V_y voltage can be written as:

$$V_y = \frac{g_{ds_{p_2}} V_{DD} + I_x}{g_{ds_{n_2}} + g_{m_{n_2}} + g_{ds_{p_2}}} \tag{15}$$

and hence the I_y can be defined as $g_{mn_2} V_y$. It follows that with referring to Fig. 3c the V_{out} voltage can be computed as:

$$V_{Out} = \left(\frac{g_{ds_{p_2}}}{g_{mn_2}} + \frac{g_{m_{p_2}}}{g_{m_{n_2}}} \frac{g_{ds_{n_1}}}{g_{m_{p_1}} + g_{mb_{p_1}}} \right) V_{DD} \tag{16}$$

therefore the PSRR can be expressed as:

$$PSRR = \frac{A_{v_D}}{A_{v_{DD}}} = \frac{g_{mb_{n_1}}}{g_{mb_{p_1}}} \frac{g_{m_{p_2}}}{g_{ds_{p_2}} + g_{ds_{n_2}}} \frac{g_{m_{n_2}}}{g_{ds_{p_2}}(1+\nu)} \tag{17}$$

where ν is defined as:

$$\nu = \frac{g_{ds_{n_1}}}{g_{ds_{p_2}}} \frac{g_{m_{p_2}}}{g_{m_{p_1}} + g_{mb_{p_1}}} \tag{18}$$

hence the PSRR behaves as A_v^2.

3.4. Large-Signal Performance

Due to the body-diode connection, the LCMFB doesn't result in class-AB behaviour as usual in the literature [28] because of the high body-transconductance

with respect to 1/R. However, the class-AB behaviour is provided by the B2G interface that yeld a non-linear current gain $I_o \approx I_{in}^{\frac{1}{\alpha}}$ as shown in Eq. 1. The slew rate is determined by the load capacitance and the maximum positive and negative output currents are given by:

$$I_{0_{max}}^{+} = I_{0_{M_{p_3}}} \exp \frac{V_{DD} - V_{th_p}}{n_p U_t} \tag{19}$$

and:

$$I_{0_{max}}^{-} = \min \left(I_{0_{M_{n_3}}} \exp \frac{V_{DD} - V_{th_n}}{n_n U_t}, k_{cm}\ I_{0_{M_{p_3}}} \exp \frac{V_{DD} - V_{th_p}}{n_p U_t} \right) \tag{20}$$

where k_{cm} denotes $g_{m_{n_3}}/g_{m_{n_4}}$ which is the aspect-ratio of transistors M_{n_3} and M_{n_4}. For the latter it has to be noted that the B2G interface gives a non-linear current amplification which could result in an effective voltage limitation for the gate M_{n_3}, and thus the minimum between the two currents should be considered.

3.5. Noise Analysis

In the following noise analysis it was assumed that each transistor contributes to the overall noise by assuming a current generator which involves both thermal and flicker noise. The power spectral density of the noise current generator can be expressed as follows:

$$S_{n_i} = \overline{i_{i_w}^2} + \overline{i_{i_f}^2} \tag{21}$$

where:

$$\overline{i_{n(p)_w}^2} = 4kTn_{n(p)}\gamma g_{m_i} \approx 2qI_d \tag{22}$$

$$\overline{i_{n(p)_f}^2} = \frac{K_{n(p)}}{fC_{ox}} \frac{g_m^2}{WL} \tag{23}$$

The resistors of the LCMFB are implemented as pseudo-resistors, since very high resistance values are desired. Their noise spectral density is therefore higher than $4kT/R$, where R is the equivalent resistance provided, and is denoted as S_{n_R}. Therefore the mean square of the equivalent input noise voltage can be

expressed as follows:

$$\overline{v_{ieq}^2} \approx 2\frac{1}{gm_{b_{n_1}}^2}\Bigg[S_{n_{p_1}} + S_{n_{n_1}} + S_{n_R} + \frac{1}{2}\left(\frac{gmb_{p_1}}{gm_{p_3}}\right)^2\left(S_{n_{p_3}} + S_{n_{n_3}}\right) + \\ + \frac{1}{2}\left(\frac{gmb_{p_1}}{gm_{p_3}}\frac{g_{mn_3}}{g_{mn_4}}\right)^2\left(S_{n_{p_4}} + S_{n_{n_4}}\right)\Bigg] \quad (24)$$

4. Amplifier Design and Simulation Results

In this section, design techniques are highlighted and small-signal and large-signal FOMs are outlined. The circuit has been designed and simulated in 130nm CMOS process from STMicroelectronics. The technology is a triple-well process which allows for separate body wells for both NMOS and PMOS devices. Circuit simulations have shown robustness against PVT variations, and state-of-the-art large- and small-signal FOMs have been attained.

4.1. Sizing

Transistors depicted in Fig. 1 have been sized as reported in Tab. 1. Transistors' widths and lengths have been accurately chosen in order to guarantee a low input referred noise and increase SR performance through the body-gate interface given by $M_{p_{1(2)}}$ and $M_{p_{3(4)}}$. Furthermore, transistors' areas have been carefully selected to take advantage of the deep-sub-threshold biasing technique, which is the best operating condition at such low supply voltages [29]. The bias voltage V_b is set through the M_{n_b} diode-connection and it is used to bias the quiescent current of the first stage to $I_q = 7.125nA$. In Tab.1, the quiescent current of each transistor is reported.

Table 1: Transistors' sizing

	Width [μm]	Length [μm]	I_q [nA]
$M_{p_{1,2,4,b}}$	4.463	1.000	7.125
$M_{n_{1,2,4,b}}$	0.375	3.000	7.125
M_{p_3}	111.0	1.000	178.125
M_{n_3}	9.375	3.000	178.125

4.2. Circuit Simulations

The proposed configuration has been simulated within the Cadence Virtuoso environment, supplied with 0.3V and loaded by a 50 pF output capacitance. In

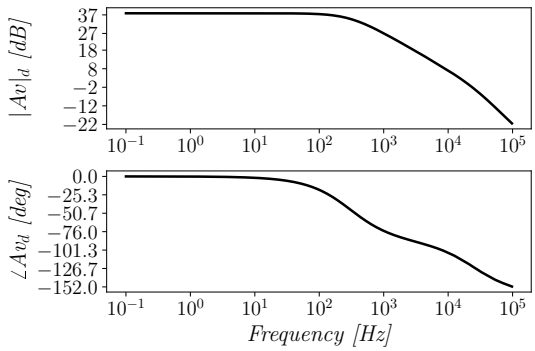
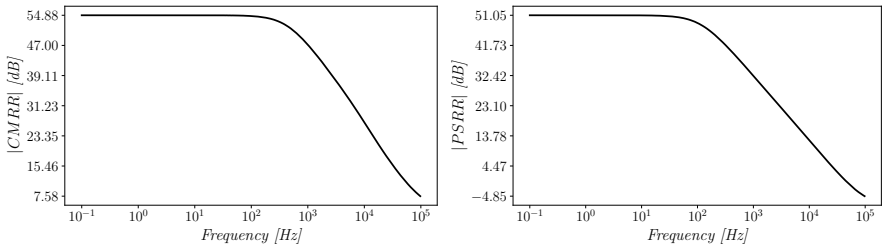


Figure 4: Differential Gain of the proposed OTA.

open loop configuration the architecture is capable to achieve 38.1 dB differential gain, 60° phase margin and 24.14 kHz GBW, as depicted in Fig. 4. The local CMFB allows to achieve very high CMRR, which amounts to about 55 dB as depicted in Fig. 5a. Fig. 5b shows a power supply rejection ratio (PSRR) as



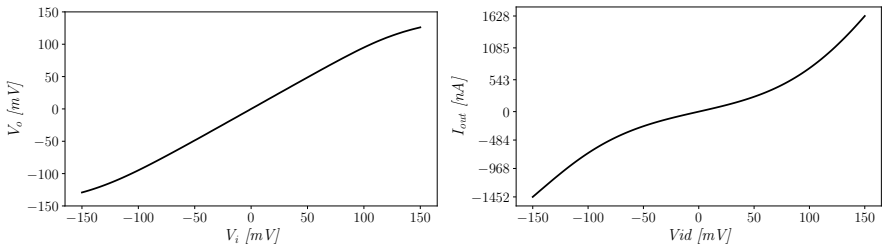
(a) (b)

Figure 5: a)Common Mode Rejection Ratio (CMRR) of the proposed OTA; b) Power Supply Rejection Ratio (PSRR) of the proposed OTA.

high as about 51 dB, and that is in accordance with Eq. 17.

In order to characterize large-signal performance, the OTA has been closed in unity-gain loop configuration, and simulation results have shown rail-to-rail

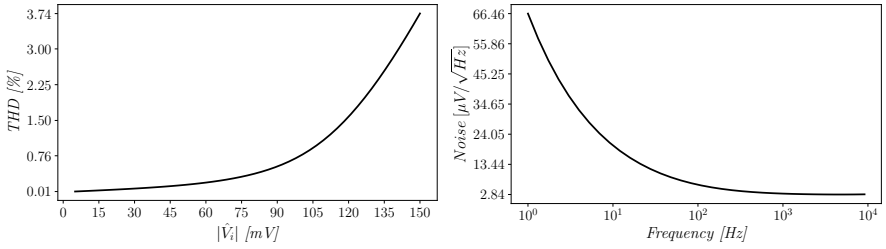
capability, as shown in Fig. 6a. In Fig. 6b it has been depicted the short-circuit output current which shows a slight asymmetry with respect to the input differential signal. Indeed, the body-to-gate interface allows to achieve a ratio of peak load current to quiescent output branch current of $I_{out_{max}}/I_{out_q} \approx 9.14$ and $|I_{out_{min}}|/I_{out_q} \approx 8.15$ respectively, where I_{out_q} is the quiescent current of M_{n_3} and M_{p_3}, highlighting a good class-AB efficiency even at very low supply voltages. The buffer configuration has been stimulated with a 200 Hz sinusoidal



(a) (b)

Figure 6: a) Unity-gain amplifier transcharacteristics; b) Short-circuit current vs differential input signal.

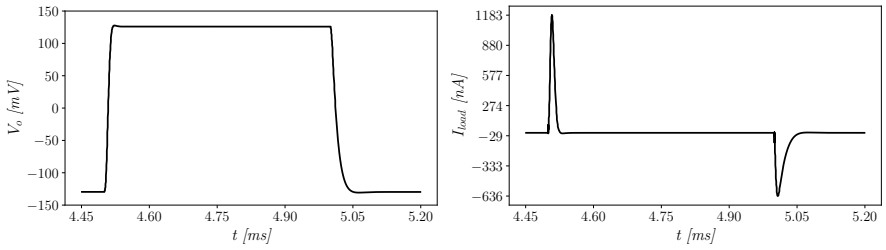
input signal, and total harmonic distortion (THD) for different signal amplitudes has been investigated and is reported in Fig. 7a. It has been found that the THD amounts to 2.57% when 90% of input swing is taken into account. Noise performance has been evaluated, and a 2.85 $\mu V/\sqrt{Hz}$ voltage spectral density has been found in the flat region, as shown in Fig. 7b. Furthermore, to assess



(a) (b)

Figure 7: a) Distortions vs input signal level in unity-gain configuration; b) Noise vs frequency.

the SR performance of the amplifier, a full range square wave has been used, and results are shown in Fig. 8a. The amplifier shows positive and negative SR (SR_p and SR_n) equal to 20.02 and 8.44 V/ms, respectively. Figure 8b



(a) (b)

Figure 8: a) Response to square input wave.; b) Load current in closed-loop configuration.

shows the corresponding load current, highlighting peaks much higher than the quiescent current of the output stage. This is a clear demonstration of class-AB behaviour. The simulation shows that the maximum output current is larger than the minimum output current, thus highlighting an asymmetric SR behaviour of a factor approximately equal to 2.

4.3. Robustness to Mismatch and PVT Variations

In order to test the robustness of the OTA against device mismatches, an extensive simulation campaign involving Monte Carlo simulations has been carried out. Table 2 reports the results of a 200-iterations Monte Carlo mismatch analysis. Power dissipation (P_D) shows a standard deviation lower than 10% of the mean value. Moreover, an output offset with a mean value of 0.57 mV and a standard deviation of about 25 mV has been found. Standard deviation lower than 15% of the mean value has been found for large-signal performance (i.e. SR_p and SR_m), whereas the phase margin $m\varphi$ is always very close to 60°.

The performance under PVT variations has been investigated taking into account ±10% supply voltage variation and a [-10,110] °C temperature range. In Tab. 3 the performance under temperature variations is summarized. A significant variation is found for the total power consumption, whereas GBW, SR,

Table 2: Performance under Mismatch Variations

	Mean	StdDev
Offset [mV]	0.568	25.18
P_D [nW]	60.19	5.214
SR_p $[V/ms]$	20.08	2.260
SR_m $[V/ms]$	8.491	1.148
Gain (1 Hz)[dB]	37.01	1.305
CMRR [dB]	42.22	8.081
Mphi $[deg]$	60.08	0.648
GBW [kHz]	23.70	1.874

Table 3: Performance vs Temperature Variations

Temp [°C]	-10.0	0.0	20.0	27.0	50.0	80.0	110.0
Offset $[mV]$	0.495	0.361	0.083	-0.022	-0.424	-1.190	-2.565
P_D [nW]	49.11	51.93	57.78	59.88	67.17	78.21	93.81
SR_p $[V/ms]$	17.980	18.930	19.900	20.020	19.850	18.750	16.940
SR_m $[V/ms]$	7.826	8.074	8.386	8.435	8.375	7.844	7.136
Gain (1 Hz)[dB]	39.07	38.86	38.30	38.07	37.20	35.67	33.25
CMRR (1 Hz) [dB]	54.12	54.81	55.10	54.88	54.45	51.57	45.66
Mphi [deg]	61.64	61.08	60.31	60.15	59.94	60.77	64.23
GBW [kHz]	22.08	22.77	23.84	24.14	24.87	25.19	24.42

gain, phase margin and CMRR slightly differ from the typical case: therefore, an overall good temperature stability is achieved. Table 4 shows that the amplifier is sufficiently stable under power supply variations in terms of power dissipation and, in addition, SR and bandwidth don't increase significantly with the supply voltage. The architecture has been tested under different corners conditions, and the proposed OTA shows good performance in all process corners as it can be seen in Tab. 5.

4.4. Discussion and Comparison with the Literature

With the aim of comparing the proposed amplifier with those proposed in literature, the standard FOM_S and FOM_L have been employed for small- and

Table 4: Performance vs Voltage Variations

V_{DD} [V]	270.0	285.0	300.0	315.0	330.0
Offset [mV]	0.39	0.16	-0.02	-0.18	-0.32
P_D [nW]	48.84	54.24	59.88	65.77	71.97
SR_p [V/ms]	16.21	18.36	20.02	21.22	22.17
SR_m [V/ms]	7.51	8.02	8.44	8.78	9.09
Gain (1 Hz)[dB]	35.90	37.08	38.07	38.93	39.67
Mphi [deg]	62.57	61.17	60.15	59.33	58.67
GBW [kHz]	21.44	22.89	24.14	25.25	26.27

Table 5: Performance vs Corners

V_{DD} [V]	TYP	SS	FF	SF	FS
Offset [mV]	-0.02	-0.4	-0.4	0.5	-0.7
P_D [nW]	59.88	54.77	65.39	65.56	55.26
SR_p [V/ms]	20.02	18.33	21.02	24.37	15.52
SR_m [V/ms]	8.44	7.87	8.86	9.33	7.35
Gain (1 Hz)[dB]	38.07	38.16	37.91	38.84	37.16
Mphi [deg]	60.15	61.40	59.29	57.56	63.29
GBW [kHz]	24.14	22.26	25.84	28.12	20.29

large-signal performance respectively. The FOM_S is defined as:

$$FOM_S = \frac{GBW \cdot C_L}{P_D} \tag{25}$$

whereas the FOM_L is computed as:

$$FOM_L = \frac{SR_{avg} \cdot C_L}{P_D} \tag{26}$$

The SR_{avg} is given by averaging the positive and negative SR.

However, it is much more effective and of interest to compare the large-signal performance by considering only the worst-case SR (SR_{WC}), also by taking into account that most of the ULV amplifiers show asymmetric SR [9]. Therefore the $FOM_{L_{WC}}$ is defined as:

$$FOM_{L_{WC}} = \frac{SR_{WC} \cdot C_L}{P_D} \tag{27}$$

Tab 6 compares the performance of the proposed OTA with other 0.3V OTAs proposed in literature. The proposed amplifier exhibits the largest small-signal FOM among the comparable ULV literature, with a FOM_S of 20.2k against the previously reported record of about 15.9k: the proposed OTA outperforms GD, BD and also digital OTAs. Large-signal performance is also very good, especially if the worst-case FOM is considered: the proposed amplifier is the second best in the literature after [10]. It has to be noted that the DC gain voltage is the one of a single-stage amplifier and, as consequence, it results limited if compared to other works that enable multistage architectures. However, among the low DC gain architectures, it attains comparable CMRR and PSRR performance. The proposed amplifier has small area occupation with respect to comparable BD designs, though area is larger than digital and GD designs.

5. Conclusion

In this paper, we propose a body-driven gate-biased class-AB OTA. The architecture is supplied at 0.3V and tail-less stages have enabled an Ultra-Low-Voltage profile. The architecture makes use of the gate-biasing strategy to select the quiescent current of first and second stage. The architecture employs Local Common Mode Feedback strategy by exploiting two pseudoresistors to improve the CMRR. Furthermore, very good PSRR has been achieved. Though body-driven stages allow to reach rail-to-rail ICMR also at such scanty voltages, compromises in terms of input-referred noise should be accepted. Indeed, the proposed OTA presents higher noise with respect to gate-driven stages. In addition, sub-threshold body-driven stages share asymmetric slew rate but, in this specific configuration, they are not so bad if compared with others reported in literature. Simulation's results have shown state-of-the-art performance and highest FOM_S have been attained (of about 20.16k). Moreover, the body-to-gate interface allows to achieve class-AB behaviour, and large-signal performance comparable with state-of-the-art FOM_L is guaranteed, also considering the $FOM_{L_{WC}}$. The topology doesn't show any high impedence internal node

and is output-compensated. An extensive campaign of Monte Carlo and PVT simulations has highlighted good robustness under ±10% V_{DD} voltage variations and [-10,110] °C temperature variations.

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Table 6: Comparison Table

	This Work*	[16]†	[9]*	[30]*	[6]†	[24]*	[10]†	[11]†	[25]†	[15]*	[31]†
Year	2021	2021	2021	2021	2020	2020	2020	2019	2019	2018	2018
Technology $[\mu m]$	0.13	0.18	0.13	0.13	0.065	0.18	0.18	0.18	0.13	0.065	0.18
V_{DD} $[V]$	0.3	0.3	0.3	0.3	0.25	0.3	0.3	0.3	0.3	0.3	0.3
V_{DD}/V_{TH} $[V]$	0.86	0.6	0.86	0.86	-	0.6	0.6	0.6	0.86	-	0.6
DC_{gain} $[dB]$	38.07	30	40.80	64.6	70	39	98.1	64.7	49.8	60	65.8
C_L $[pF]$	50	150	40	50	15	10	30	30	2	5	20
GBW $[kHz]$	24.14	0.25	18.65	3.58	9.5	0.9	3.1	2.96	9100	70	2.78
$m\varphi$ $[deg]$	60.15	90	51.93	53.76	89.9	90	54	52	76	53	61
SR_p $[\frac{V}{ms}]$	20.02	-	10.83	1.7	2	-	14	1.9	-	25	6.44
SR_m $[\frac{V}{ms}]$	8.44	-	32.37	0.15	2	-	4.2	6.4	-	25	7.8
SR_{avg} $[\frac{V}{ms}]$	14.23	0.085	21.60	0.93	2	-	9.1	4.15	3.8	25	7.12
THD [%]	1.635	2	1.4	0.84	-	1	0.49	1	-	-	1
% of input swing	80	90	80	100	-	23	83.33	85	-	-	93.33
$CMRR$ $[dB]$	54.88	41	67.49	61	62.5	30	60	110	-	126	72
$PSRR$ $[dB]$	51.05	30	45	26/28	38	33	61	56	-	90/91⋆	62
$spot-noise$ $[\frac{\mu V}{\sqrt{Hz}}]$	3.156	-	2.12	2.69	-	0.81	1.8	1.6	0.035	2.82	1.85
@freq	1000	-	1000	100	-	1000	-	-	100000	1000	36
$Power$ $[nW]$	59.88	2.4	73	11.4	26	0.6	13	12.6	1800	51	15.4
$Mode$	BD	DIG	BD	BD	BD	GD	BD	BD	GD	BD	BD
FOM_S $[\frac{MHz \cdot pF}{mW}]$	20.16k	15.89k	10.20k	15.72k	5.48k	15.00k	7.15k	7.05k	10.11k	6.86k	3.61k
FOM_L $[\frac{V \cdot pF}{\mu s \cdot mW}]$	11.88k	5.40k	11.82k	4.08k	1.15k	-	21.00k	9.88k	4.67k	2.45k	9.25k
$FOM_{L_{WC}}$ $[\frac{V \cdot pF}{\mu s \cdot mW}]$	7.04k	-	5.93k	4.52k	1.15k	-	6.30k	4.52k	-	2.45k	8.36k
$Area$ $[mm^2]$	0.0027	0.000982	0.0036	0.0036	0.002	0.00047	0.0098	0.0085	-	0.003	0.0082

* Simulated; † Measured; ⋆ $PSRR_+/PSRR_-$ $[dB]$.

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