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Combined DC-Link Fed Parallel-VSI-Based DSTATCOM for Power Quality Improvement of a Solar DG Integrated System

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Abstract: In present day power systems, Power Quality (PQ) issues are causing great concern owing to the increased use of power electronic controlled drives and fluctuating and other non-linear loads. This problem is further aggravated by a steady increase in the integration of renewable energy-based Distribution Generation (DG), employing power electronic converters to distribution systems. Custom power devices with suitable control strategies provide an effective solution to these power quality issues. In this work, a typical three-phase distribution system supplying non-linear load and with DG integration is considered. A shunt connected DSTATCOM at PCC of the system is employed to mitigate power quality concerns. Initially, a parallel-VSI based DSTATCOM configuration, employing individual DC-Link and working basically on the principle of current sharing, has been proposed. The analysis is carried out for variable load conditions for PQ enhancement making use of a more effective control theory viz. Instantaneous Real-Reactive Power (IRP) theory for the generation of suitable switching patterns to the individual VSIs of the parallel DSTATCOM. Further, an improvement over the above configuration viz. combined/common DC-Link-fed parallel DSTATCOM is proposed. This configuration has the advantages of minimized sensing elements, reliable operation and low-cost compensation. A similar analysis is carried out for PQ improvement, making use of the same IRP theory with some modifications (known as MIRP theory). The effectiveness of this configuration is established from the simulation results. In all the above cases, the analyses are carried out using MATLAB/Simulink platform and the simulation results are presented in detail. Thus, the proposed parallel VSIs-based DSTATCOM configurations employing suitable control strategies provide effective solutions for power quality issues under varying load conditions in conventional distribution systems.

Keywords: DSTATCOM; power quality; distributed generation; PV system; common DC link

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1. Introduction

Application of the traditional VSI-DSTATCOM is discussed for PQ enhancement in a distribution system. However, it suffers from limitations such as non-presence of current sharing principle, high dv/dt switch stress, high switching losses and low efficiency. To overcome these limitations, a novel parallel-VSIs-based DSTATCOM has been proposed

for PQ enhancement and for use in DG operations with good operating features by making use of the proposed control scheme [1].

The application of proposed parallel-VSI-based DSTATCOM topologies have created a lot of interest for extending several research studies in CPD technology. For the last two decades, the usage of parallel-VSI topologies has been increasing in CPD technology for attaining high-performance features in various domestic and industrial applications [2]. The parallel connected VSIs, employing the compensation current sharing principle between the dual VSIs, reduce the over-all current ratings of DSTATCOM, provide flexible active power sharing and facilitate master and slave operations of VSIs for achieving high robustness, good thermal management and fault tolerance [3].

The parallel connected dual VSIs distribute the required compensation currents to compensate current-related PQ issues in a distribution system. To integrate these dual VSIs in parallel form, certain conditions are to be satisfied, such as phase displacement and output voltage magnitude of dual VSIs should be strictly the same to guarantee that every VSI shares an equal compensation current [4]. Otherwise, circulating currents and over-compensation characteristics of VSIs may arise, which affect the over-all performance of the distribution system [5].

The significant way to integrate dual VSIs is described as parallel formation by utilizing DC-link capacitor and interfacing inductor after the VSI modules [6]. This formation can be accomplished in two ways viz. Isolated DC-link-based parallel-VSIs DSTATCOM and Combined/Common DC-link-based parallel-VSIs DSTATCOM for enhancing PQ features in a three-phase distribution system. Of these two techniques, the common DC-link type parallel-DSTATCOM is best suited because it requires a common/combined DC-link source, minimizes the number of sensing elements and ensures reliable operation and low-cost compensation [7].

An effective control strategy is a pre-requisite for generation of suitable switching patterns to both the VSIs in parallel-VSI-based DSTATCOM configuration. Several control strategies are studied and presented in the literature [8]. In this work, Modified Instantaneous Real-Reactive Power (MIRP) theory is proposed for generation of reference currents to the switching pattern scheme of the novel parallel-VSI configuration-based DSTATCOM. In the following sections, critical evaluation of the proposed, isolated and combined DC-Link fed parallel-VSIs-based DSTATCOM configurations is carried out under constant and variable load conditions. MATLAB/Simulink platform is used for analysis and the results are illustrated with proper comparisons [9]. Major Contributions in this paper are as follows.

The present work mainly focuses on developing new control strategies for the operation of proposed parallel VSIs-based DSTATCOM topologies with Isolated DC-Link and common DC-Link, respectively, for a three-phase distribution system supplying non-linear load. Power quality enhancement, which includes power factor improvement and harmonic compensation, are analyzed for constant and variable non-linear loads. The results obtained using MATLAB/Simulink platform are presented in detail for each case. The details of major contributions are presented below.

- To study the performance of the traditional VSI-based DSTATCOM for PQ improvement in a distribution system using conventional control/compensation strategy.
- To develop a parallel-VSI based DSTATCOM topology with Isolated DC-Link for a three-phase distribution system for improving PQ concerns arising from constant and variable non-linear load devices.
- To propose/develop a modified-IRP (MIRP) control theory to the above parallel-VSI-based DSTATCOM topology with Isolated DC-Link for a three-phase distribution system for improving PQ concerns arising from constant and variable non-linear load devices.
- To develop a parallel-VSI-based DSTATCOM topology with Common DC-Link for a three-phase distribution system for improving PQ concerns arising from constant and variable non-linear load devices.

- To adapt the modified-IRP (MIRP) control theory to the common DC-Link operated parallel DSTATCOM for achieving harmonic compensation.
- To carry out Performance Analysis and compare the results of both the Proposed Isolated and Combined DC-Link fed Parallel VSI-Based DSTATCOM for PQ Improvement.

2. Proposed Combined DC-Link Fed Parallel VSI-Based DSTATCOM Configuration

The proposed combined parallel-VSI-based DSTATCOM compensates for the various PQ issues such as harmonic current distortions, reactive power control, power-factor correction, load balancing, etc., in a three-phase distribution system [10]. It consists of two VSIs connected in parallel formation driven by combined (common) DC-link capacitor, sensing elements, control strategy, switching pattern circuits, and line-interfacing filtering units. The configuration of the proposed combined parallel-VSIs DSTATCOM is depicted in Figure 1.

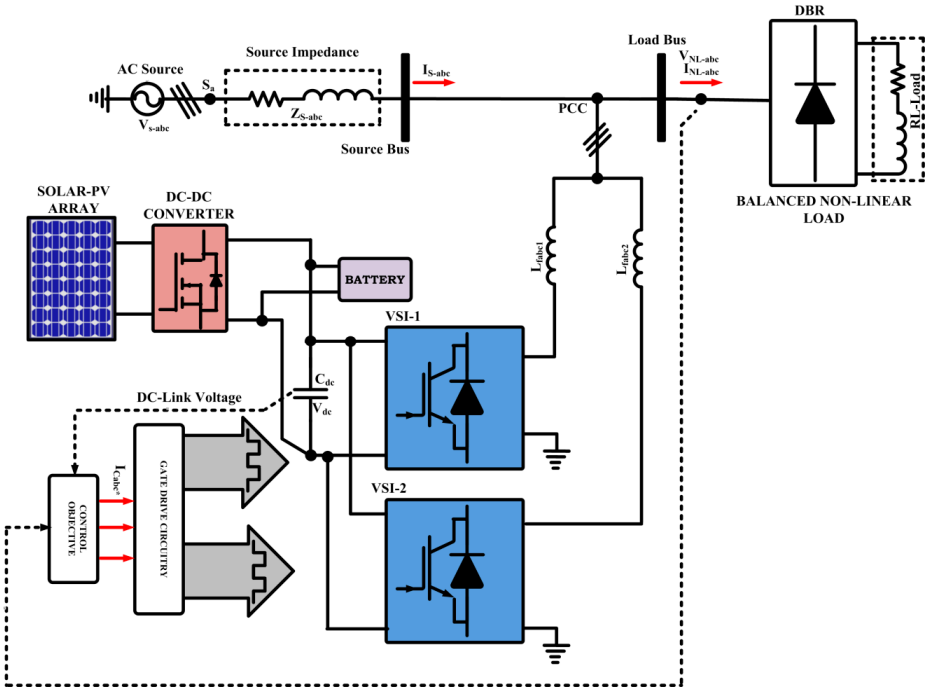


Figure 1. Configuration of the Proposed Common DC-Link Fed.

Various components in the proposed configuration involve, source voltage Vs-abc, source current Is-abc, non-linear load voltage VNL-abc, load current INL-abc, compensator currents IC-abc1 abd IC-abc2 and line impedance Zs-abc, respectively. In this configuration, the load considered is a non-linear DBR with a Resistive-Inductance (RL) load. Additionally, a common DC-link capacitor Cdc is used to drive the dual parallel-VSIs of DSTATCOM for regulating PCC voltages [11,12]. The proposed combined DC-Link fed parallel-VSI topology requires a single DC-link capacitor and offers merits such as reduced sensing elements, reliable operation and low-cost compensation compared to the isolated DC Link Fed parallel-VSIs topology. To minimize the circulation currents flow between the DC-link capacitor and the VSIs and to maintain constant voltage Vdc across common points, an active DC-link regulator is used. The line-interfacing filters are introduced after the VSIs module for filtering the notching and uneven effects during the injection of compensation currents from VSI modules [13].

Both the VSIs share the compensation currents leading to the reduction in the capacity of high rated compensators and maintain the PCC voltage as constant. The parallel-VSI-based DSTATCOM injects required currents into the PCC of three-phase distribution system for mitigating all current-related PQ concerns with greater mitigation characteristics [14]. The current injected into the PCC is in quadrature with the PCC voltage, thus implying

that the parallel-VSI DSTATCOM exchanges or consumes the requisite reactive power. A reference current extraction is required to switch the parallel-VSI for controlling the injected currents by using a suitable control strategy.

3. Control Strategy of Proposed Parallel VSI-Based DSTATCOM

The proposed combined DC-Link fed parallel-VSI-based DSTATCOM requires an effective control strategy to attain greater PQ compensation features in a three-phase distribution system [15]. The control strategy plays a significant role in power-electronic converter-based CPD technology to regulate the specific system dynamics for extracting reference currents from sensing the load currents and voltage signals. The extracted reference currents provide suitable switching signals to the parallel-VSIs of DSTATCOM through gate-drive circuitry.

In isolated topology, IRP control theory is used for generation of reference currents but, it is unsuitable to the combined topology because of the individual control action of VSIs. For the combined dual parallel-VSI topology, a novel Modified Instantaneous Real-Reactive Power (MIRP) control strategy has been used for generation of reference currents to the parallel-VSI-based DSTATCOM. The MIRP control theory is designed similar to the formal IRP theory with slight changes with respect to switching the parallel VSIs.

The MIRP control theory makes use of dual-transformation process in which the three-phase a-b-c coordinates are transformed into α-β coordinates in a rotating orthogonal reference frame [16]. The source voltage Vs-abc and non-linear load currents INL-ab, are the main inputs of the MIRP control theory, which are forwarded to Clarke's transformation procedure for obtaining rotating reference values such as ($V_{s-\alpha\beta}$, $I_{NL-\alpha\beta}$) to extract the real-reactive power components. The three-phase source voltages and non-linear load currents are described in Equations (1) and (2),

$$\begin{aligned} v_{s-a} &= V_a \sin(\omega t) \\ v_{s-b} &= V_b \sin\left(\omega t - \tfrac{2\pi}{3}\right) \\ v_{s-c} &= V_c \sin\left(\omega t - \tfrac{4\pi}{3}\right) \end{aligned} \tag{1}$$

$$\begin{aligned} i_{NL-a} &= \sum I_{a-n} \sin(n(\omega t) - \theta_{a-n}) \\ i_{NL-b} &= \sum I_{b-n} \sin\left(n\left(\omega t - \tfrac{2\pi}{3}\right) - \theta_{b-n}\right) \\ i_{NL-c} &= \sum I_{c-n} \sin\left(n\left(\omega t - \tfrac{4\pi}{3}\right) - \theta_{c-n}\right) \end{aligned} \tag{2}$$

Clarke's transformation is applied to the above sensed load currents and voltage signals and the same is described in Equations (3) and (4),

$$\begin{bmatrix} v_{s-\alpha} \\ v_{s-\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_{s-a} \\ v_{s-b} \\ v_{s-c} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_{NL-\alpha} \\ i_{NL-\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} i_{NL-a} \\ i_{NL-b} \\ i_{NL-c} \end{bmatrix} \tag{4}$$

The direct active and reactive power values in the orthogonal reference frame are acquired from Equations (3) and (4) and can be represented as (5) and (6),

$$p = v_{s-\alpha} i_{NL-\alpha} + v_{s-\beta} i_{NL-\beta} \tag{5}$$

$$q = -v_{s-\beta} i_{NL-\alpha} + v_{s-\alpha} i_{NL-\beta} \tag{6}$$

The above are represented in a matrix form as (7),

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{s-\alpha} & v_{s-\beta} \\ -v_{s-\beta} & v_{s-\alpha} \end{bmatrix} \begin{bmatrix} i_{NL-\alpha} \\ i_{NL-\beta} \end{bmatrix} \tag{7}$$

The load currents in ($\alpha\beta$) frame can be defined as (8)

$$\begin{bmatrix} i_{NL-\alpha} \\ i_{NL-\beta} \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{s-\alpha} & v_{s-\beta} \\ -v_{s-\beta} & v_{s-\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{8}$$

where

$$\Delta_k = v_{s-\alpha}^2 + v_{s-\beta}^2 \tag{9}$$

The real-current component is passed through the second-order High-Pass Filter (HPF) and a current calculator for extracting harmonic sequences to acquire desired reference current signals [17]. This filter eliminates the low-order components and allows only the high-order components into the system as a reference current in the orthogonal (α-β) frame. The DC-link regulator controls the voltage across the DC-link capacitor by using the Proportional-Integral (PI) controller. The extracted actual DC-link voltage (V_{dca}) is directly compared with the reference DC-link voltage (V_{dcr}^*) and the resulting error signal is fed to the PI controller, which provides a dominant signal as a loss component (P_{Loss}). The error signal and PI controller responses at nth instant can be described as (10) and (11),

$$V_{dcer} = V_{dcr}^* - V_{dca} \tag{10}$$

$$\Delta_{idc} = \Delta_{idc-n} - K_p * \left(V_{dcer(n)} - V_{dcer(n-1)}\right) + K_i * \left(V_{dcer(n)}\right) \tag{11}$$

The instantaneous powers comprise oscillatory and averaged DC components as described in (12),

$$\begin{aligned} p &= \overline{p} + \widetilde{p} \\ q &= \overline{q} + \widetilde{q} \end{aligned} \tag{12}$$

where $\overline{p}, \overline{q}$ are the DC averaged values and $\widetilde{p}, \widetilde{q}$ are the AC oscillatory values of the MIRP control theory. Thus, the reference currents $\left(i_{c-\alpha\beta}^*\right)$ in the orthogonal (α-β) frame can be represented as (13),

$$\begin{bmatrix} i_{c-\alpha}^* \\ i_{c-\beta}^* \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{s-\alpha} & -v_{s-\beta} \\ v_{s-\beta} & v_{s-\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{13}$$

The reference currents from the MIRP control theory are re-transformed into regular a-b-c coordinates by using inverse-transformation procedure such as (14),

$$\begin{bmatrix} i_{cr-a}^* \\ i_{cr-b}^* \\ i_{cr-c}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{c-\alpha}^* \\ i_{c-\beta}^* \end{bmatrix} \tag{14}$$

The reference currents $\left(i_{cr-abc}^*\right)$ are compared to the actual line currents (i_{a1-abc}) and (i_{a2-abc}) of two VSIs in the Hysteresis Current Controllers (HCC-1 and HCC-2) that have certain band limits. The outputs of these controllers are used for generation of feasible switching patterns to the individual parallel-VSIs of DSTATCOM [18–20]. The limits of the controllers act as boundary limits to control the compensation current between the upper and lower bands, which are related to ON and OFF states of the parallel-VSI topologies.

The switching actions of parallel-VSIs are highly influenced by the actual currents of both the VSIs and the reference current components. The respective switches are conducted when the actual current is greater than reference current; otherwise, they are in an OFF-state. Likewise, the actual currents of both the VSIs continuously swing between the lower and upper band limits followed by the reference currents generated by the proposed MIRP control theory. The representation of the MIRP control theory for PQ improvement is illustrated in Figure 2. The over-all configuration of the proposed common DC-link fed parallel-VSIs-based DSTATCOM for PQ improvement is depicted in Figure 3.

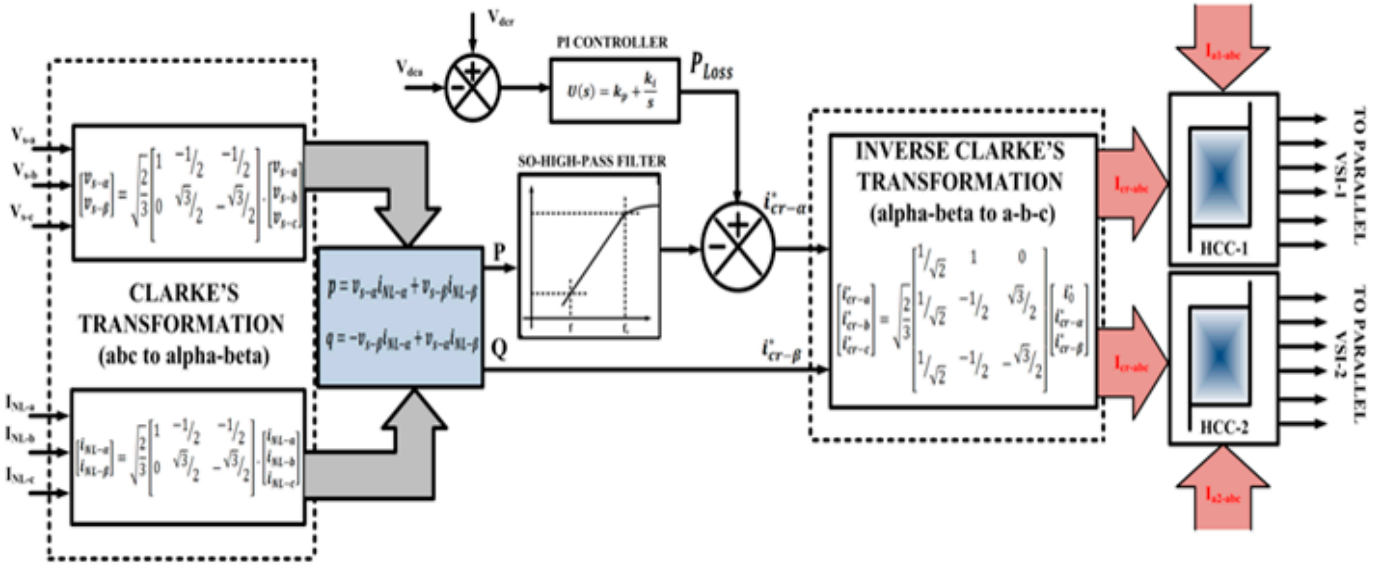


Figure 2. Representation of the MIRP Control Theory for PQ Improvement.

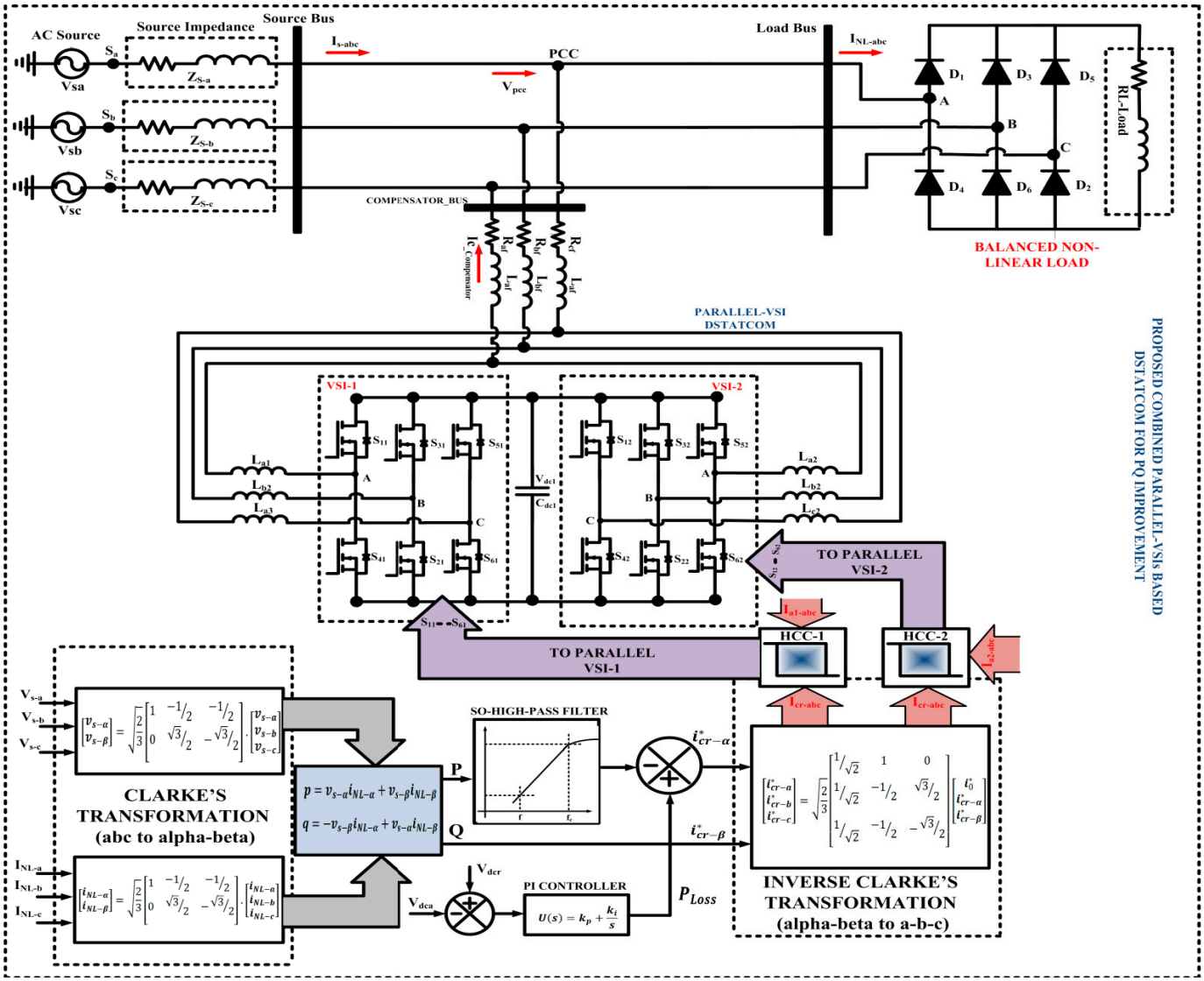


Figure 3. Over-all Configuration of the Proposed Common DC-Link Fed Parallel-VSI-Based DSTATCOM for PQ Enhancement.

4. Results and Discussion

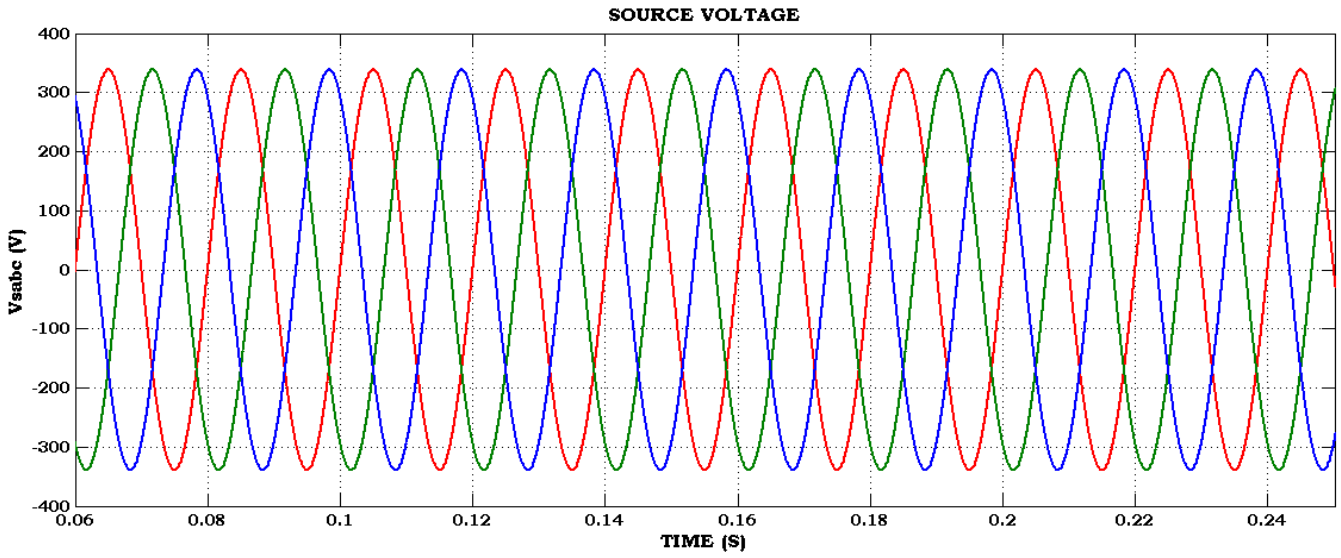
The MATLAB/Simulink results of the proposed Common DC-Link fed parallel-VSIs-based DSTATCOM employing MIRP control scheme for PQ enhancement in a three-phase distribution system under constant and variable non-linear load conditions are presented below. The specifications of the proposed system are same as those presented in Table 1.

Table 1. System Specifications of the Proposed Parallel-VSI DSTATCOM for PQ Improvement.

S. No	Specifications	Values
1	Main Source Voltage	Vsabc-415 V (rms), Fs-50 Hz
2	Source Impedance	R-0.1 Ω, L-0.9 mH
3	Load Impedance (Constant/Variable)	R-25 Ω, L-25 mH
4	DC-Link Capacitor	1500 μF
5	Line Interfacing Filter (VSI)	R-0.0001; L-5 mH
6	PI Regulator Parameters	Kpd-0.1; Kid-0.05

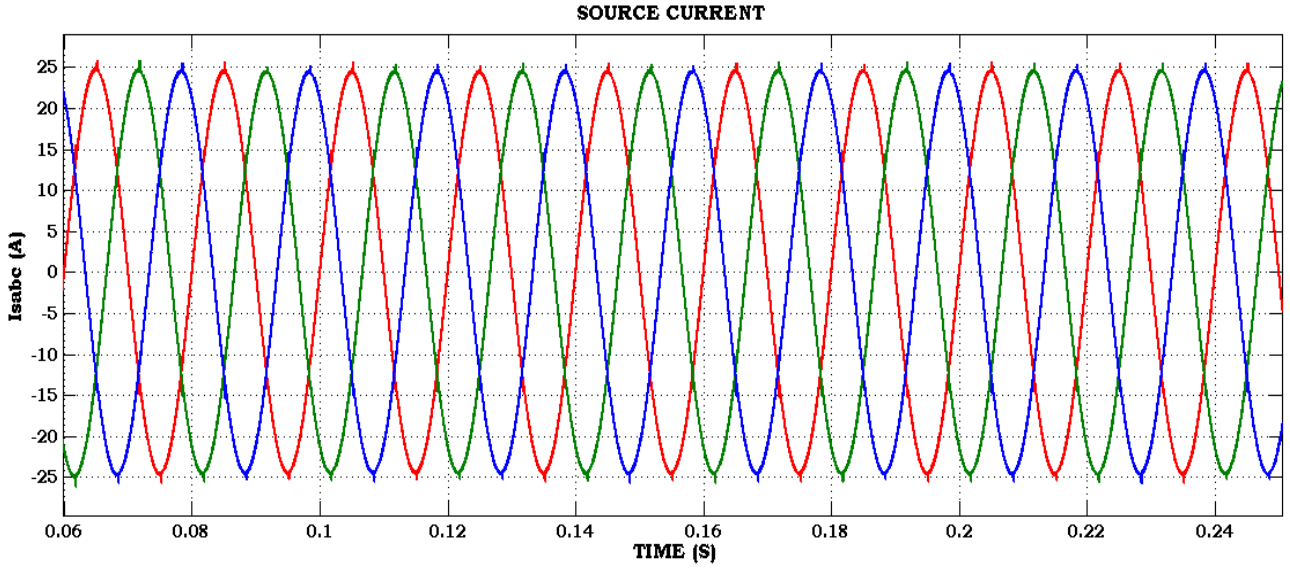
4.1. Performance Analysis under Constant Load Condition

The simulation results of the proposed Common DC-Link Fed Parallel-VSIs-based DSTATCOM for PQ improvement under constant load condition are presented in Figure 4a–k. They include, (a) Source Voltage, (b) Source Current, (c) Non-Linear Load Current, (d) Compensation Current of VSI-1, (e) Compensation Current of VSI-2, (f) Source Voltage & Source Current In-Phase condition, (g) Source Active and Reactive Power, (h) Non-Linear Load Active and Reactive Power, (i) DC-Link Voltage, (j) THD Analysis of Non-Linear Load Current and (k) THD Analysis of Source Current.

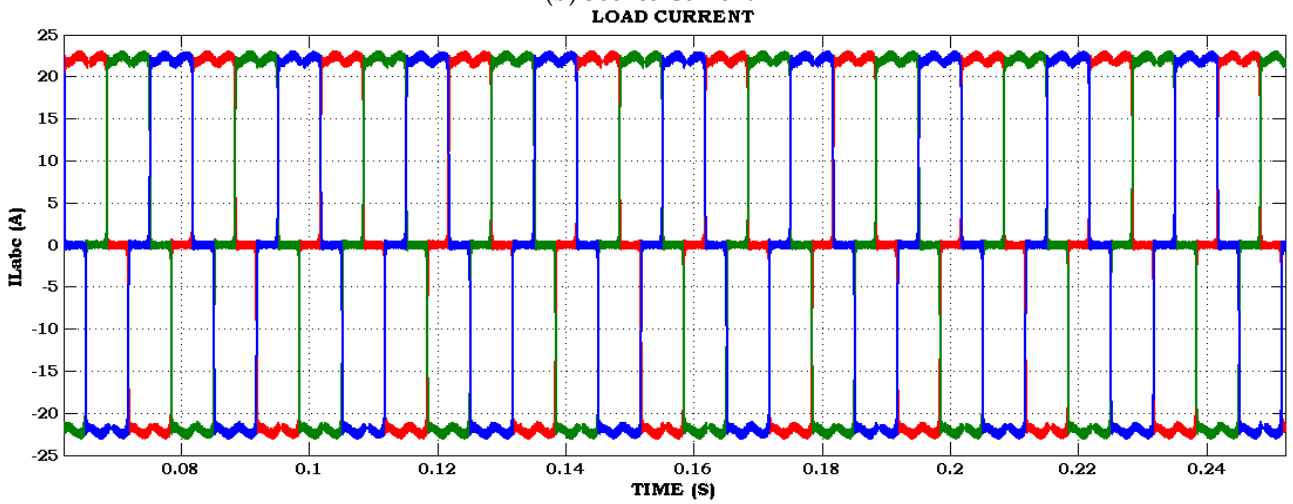


(**a**) Source Voltage

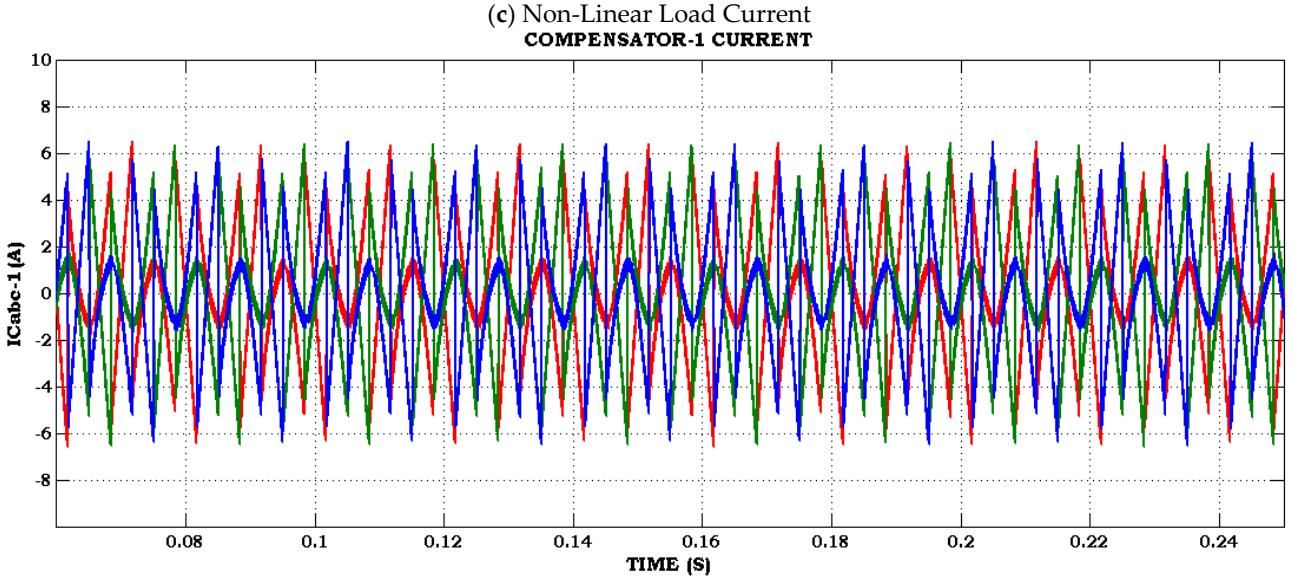
Figure 4. *Cont.*



(**b**) Source Current

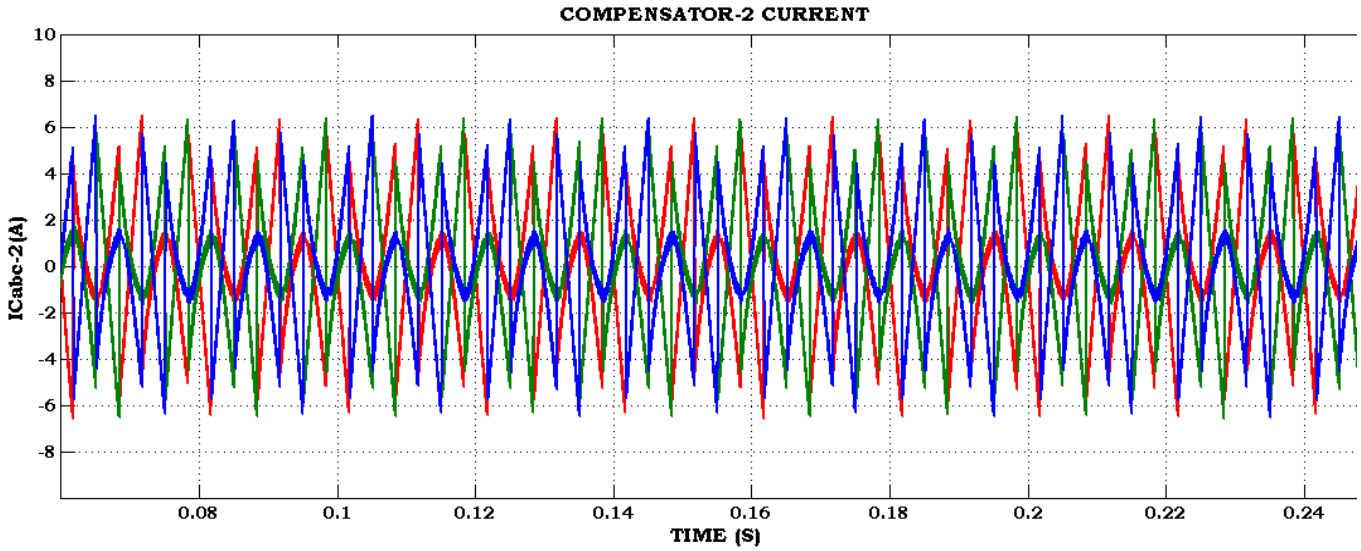


(**c**) Non-Linear Load Current

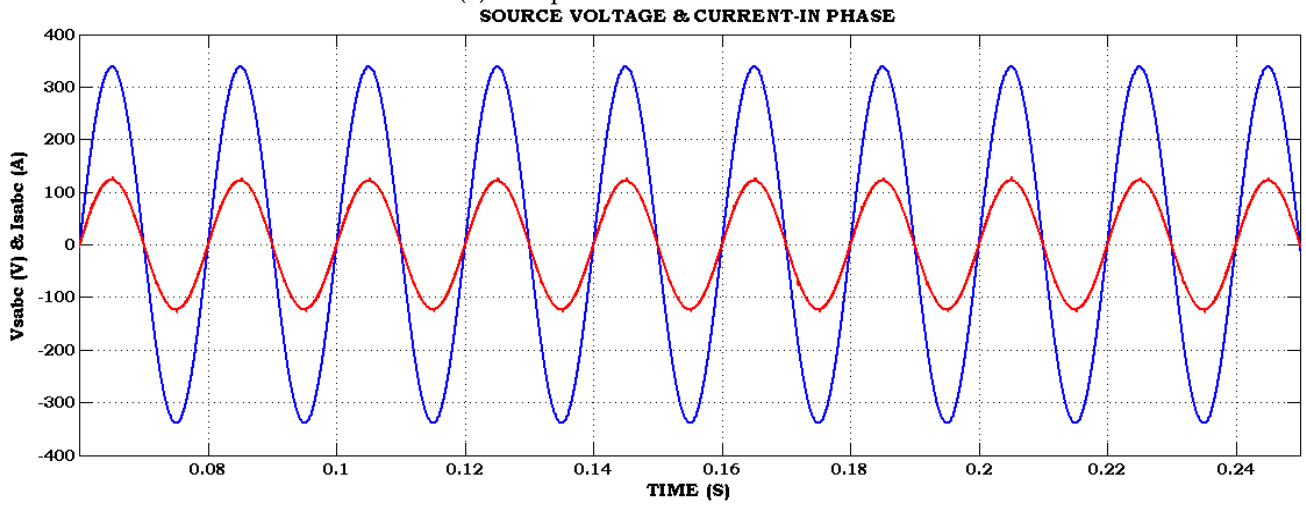


(**d**) Compensation Current of VSI-1

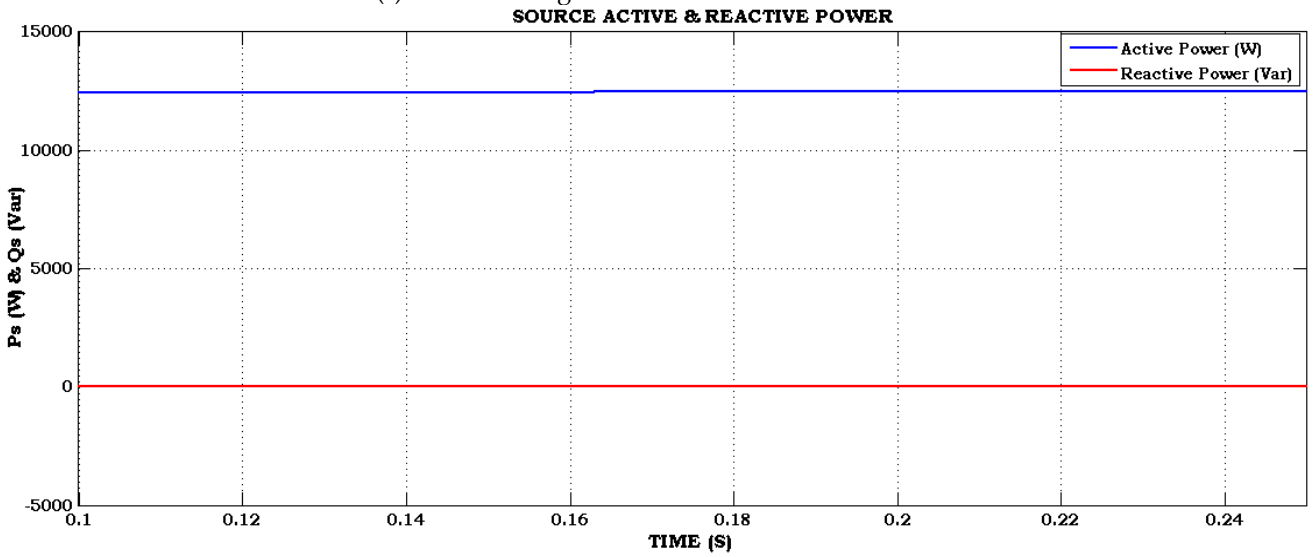
Figure 4. *Cont.*



(**e**) Compensation Current of VSI-2

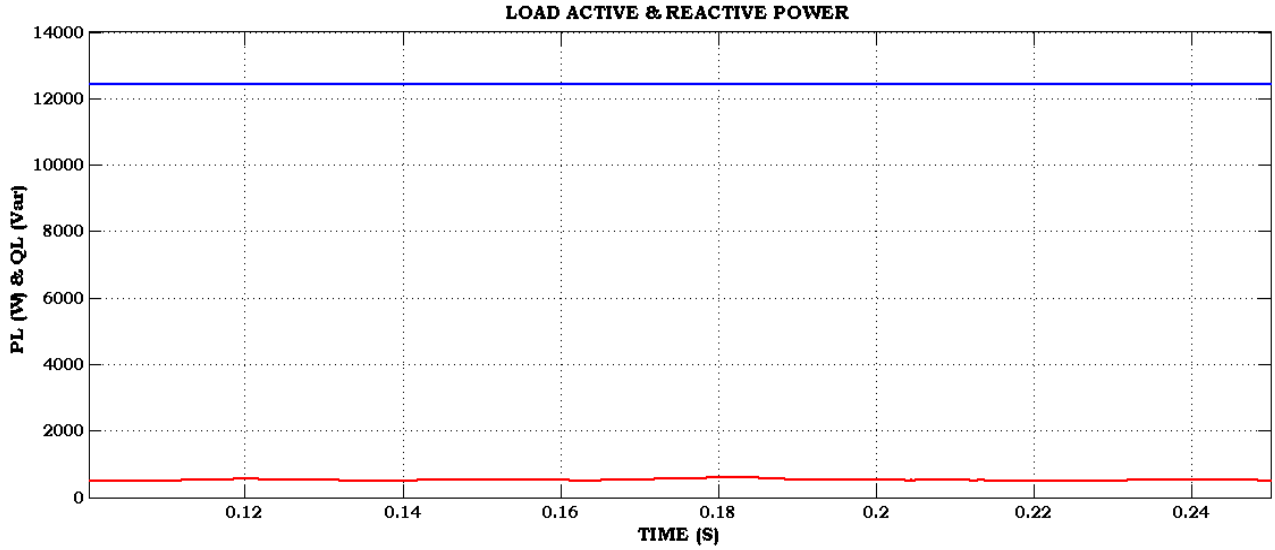


(**f**) Source Voltage and Source Current—In Phase

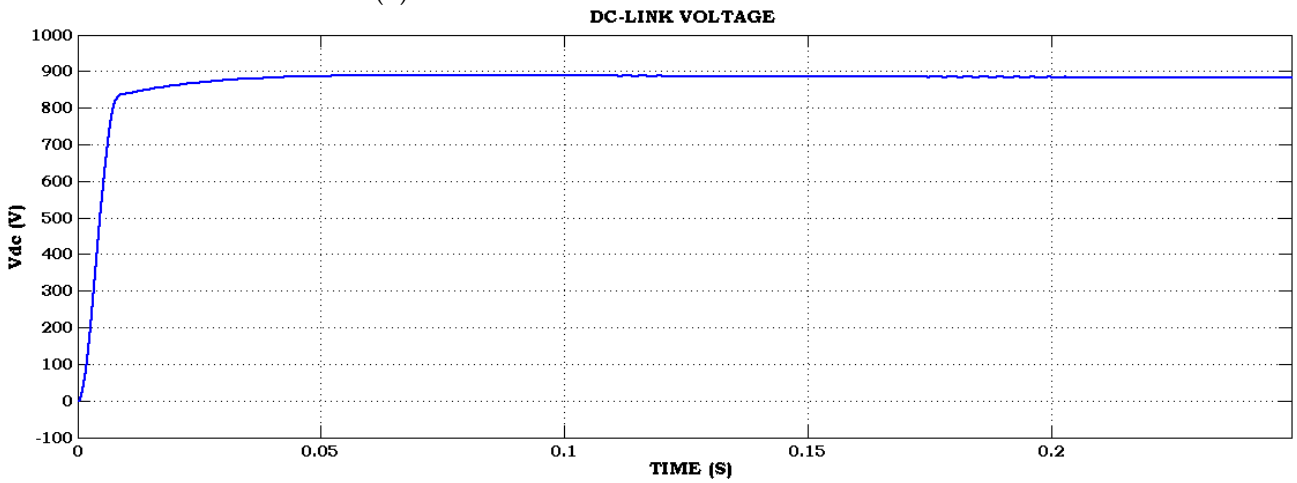


(**g**) Source Active & Reactive Power

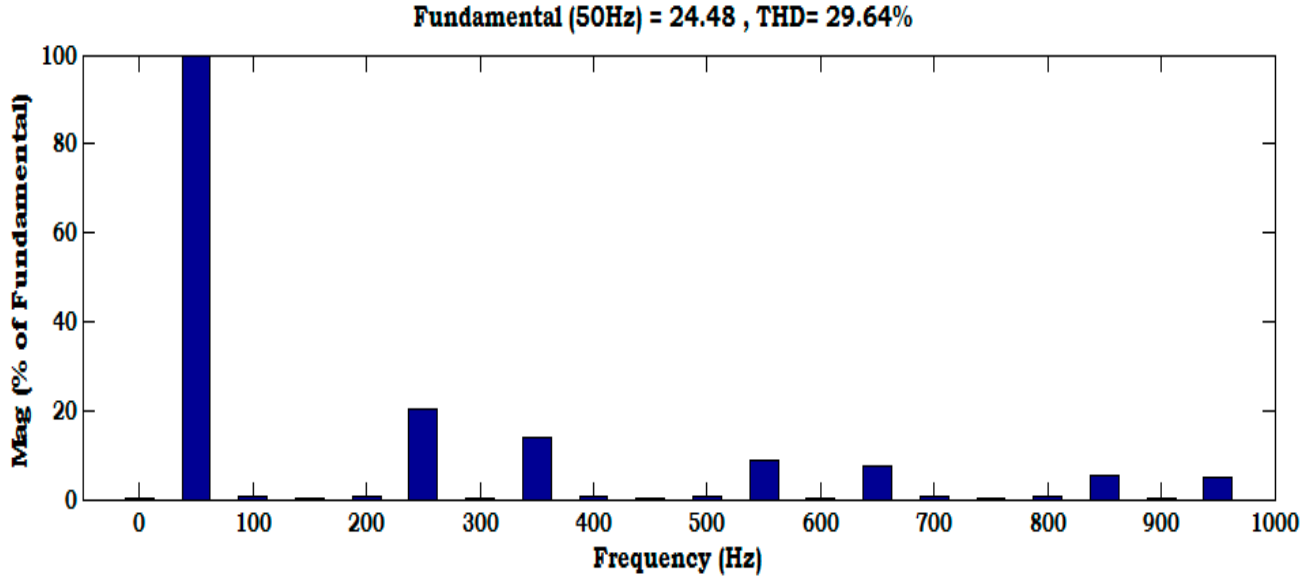
Figure 4. *Cont.*



(**h**) Non-Linear Load Active and Reactive Power

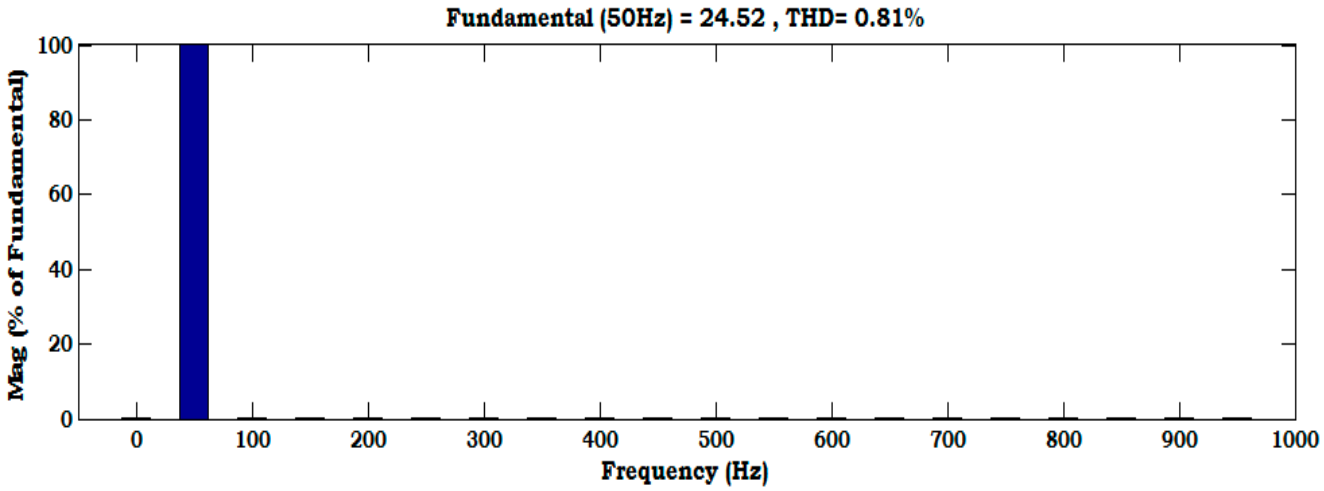


(**i**) DC-Link Voltage



(**j**) THD Analysis of Non-Linear Load Current

Figure 4. *Cont.*



(**k**) THD Analysis of Source Current

Figure 4. Simulation Results of the Proposed Combined DC-Link Fed Parallel-VSIs-Based DSTATCOM for PQ Improvement under Constant Load Condition.

The three-phase distribution system furnishes required energy to drive the Diode-Bridge Rectifier (DBR) as constant non-linear load with a source voltage of 415 Vrms, 50 Hz fundamental frequency. In this case, the load is considered as a non-linear power-electronic device, which generates harmonic distortions in a source or PCC current and proliferates other load connected close to the PCC of the distribution system. These current harmonics disrupt the frequency level and produce high loss resulting in more heat, thereby damaging the loads connected near to PCC point.

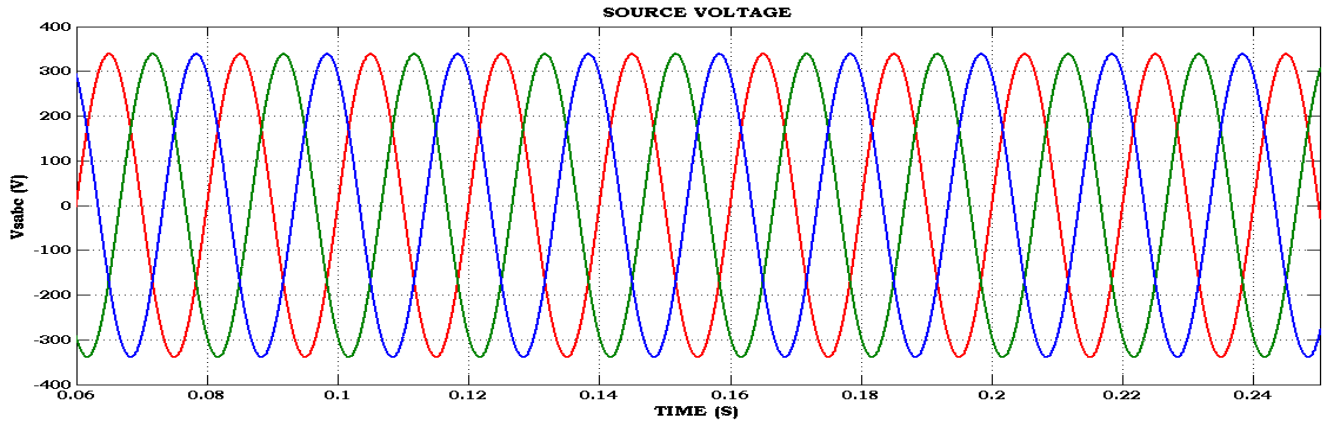
The proposed combined DC-Link fed parallel-VSIs-based DSTATCOM is adopted to counteract the harmonic distortions in source current and maintains PCC parameters that are balanced, sinusoidal and linear in nature. The proposed parallel-VSI-based DSTATCOM operates by injecting compensation currents to counteract the harmonic distortions and regulates PCC voltage as a constant. Compared to the traditional VSI-DSTATCOM, presented in Section 3, the proposed common DC-Link fed parallel-VSIs- based DSTATCOM shares the required compensation current and reduces the over-all current rating of the DSTATCOM. The required compensation current is 12 A, and VSI-1 and VSI-2 produce equal currents of 6 A each. As both the VSIs are connected in parallel form, the required compensation current of 12 A is met to comply with PQ enhancement features. The source and load currents are maintained constant at values of 25 A and 23 A, respectively. The source voltage is maintained constant at a peak value of 340 V.

The source voltage and current are in-phase conditions that represent an ideal power-factor at the source/PCC (source current is multiplied by five times for clear view of in-phase condition). The input source generates the required active and reactive powers of 12.5 KW and 0.02 KVAR, respectively, to meet the load active and reactive powers of 12.4 KW and 0.55 KVAR through the proposed common DC-Link fed parallel-VSI DSTATCOM. The DC-link voltage is also maintained constant at a value of 900 V with the help of a DC-link regulator, which also reduces the circulation current flow towards the VSI and DC-link capacitor. The THD of the non-linear load current is 29.64% because of the presence of non-linear load devices and these harmonic currents appear in the system. The proposed combined DC-Link fed parallel-VSIs-based DSTATCOM compensates for the harmonics because of the non-linear load and the THD of source current is now 0.81%, thus complying with IEEE-519/2014 standards.

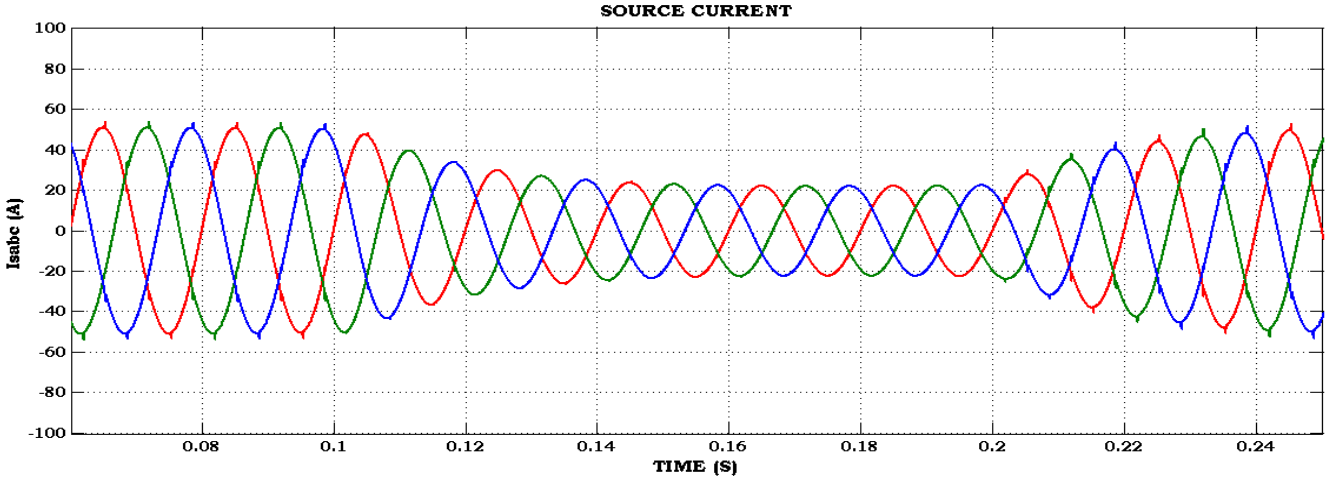
4.2. Performance Analysisunder Variable Load Conditions

The simulation results of the proposed combined DC-Link Fed Parallel-VSIs-based DSTATCOM for PQ improvement under variable load conditions are presented in

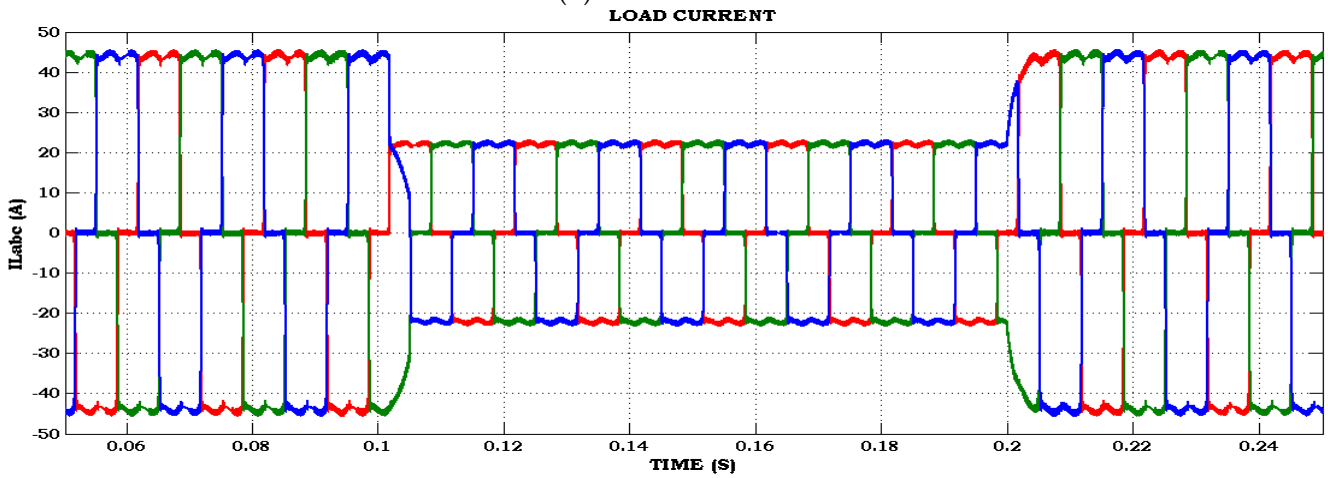
Figure 5a–k. These include (a) Source Voltage, (b) Source Current, (c) Non-Linear Load Current, (d) Compensation Current of VSI-1,(e) Compensation Current of VSI-2, (f) Source Voltage & Source Current In-Phase, (g) Source Active and Reactive Power, (h) Non-Linear Load Active and Reactive Power, (i) DC-Link Voltage, (j) THD Analysis of Non-Linear Load Current and (k) THD Analysis of Source Current.



(**a**) Source Voltage

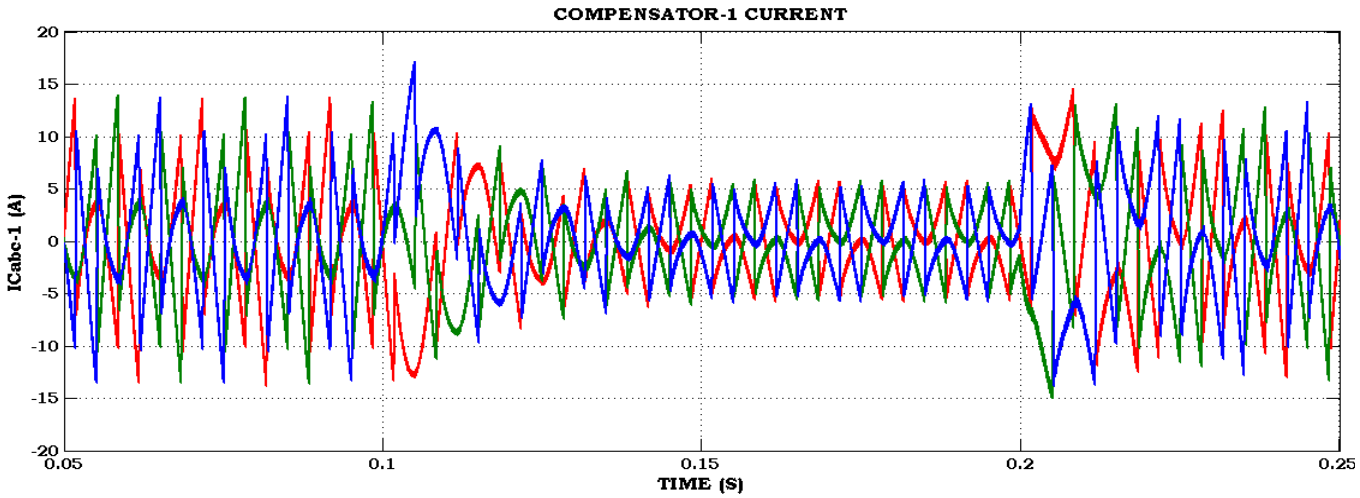


(**b**) Source Current

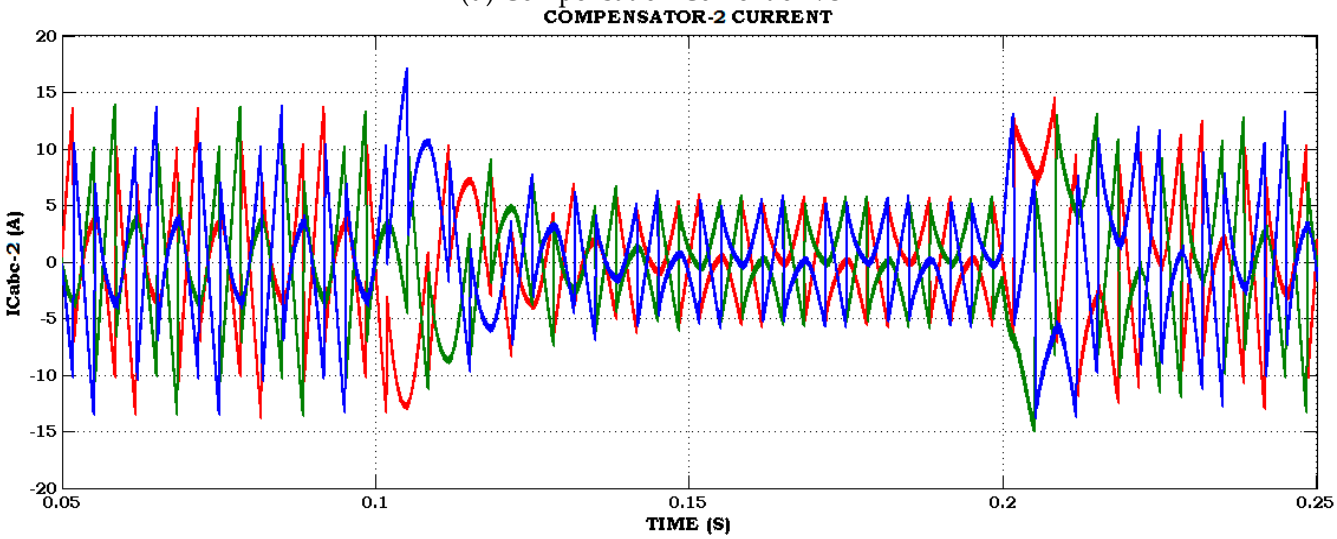


(**c**) Non-Linear Load Current

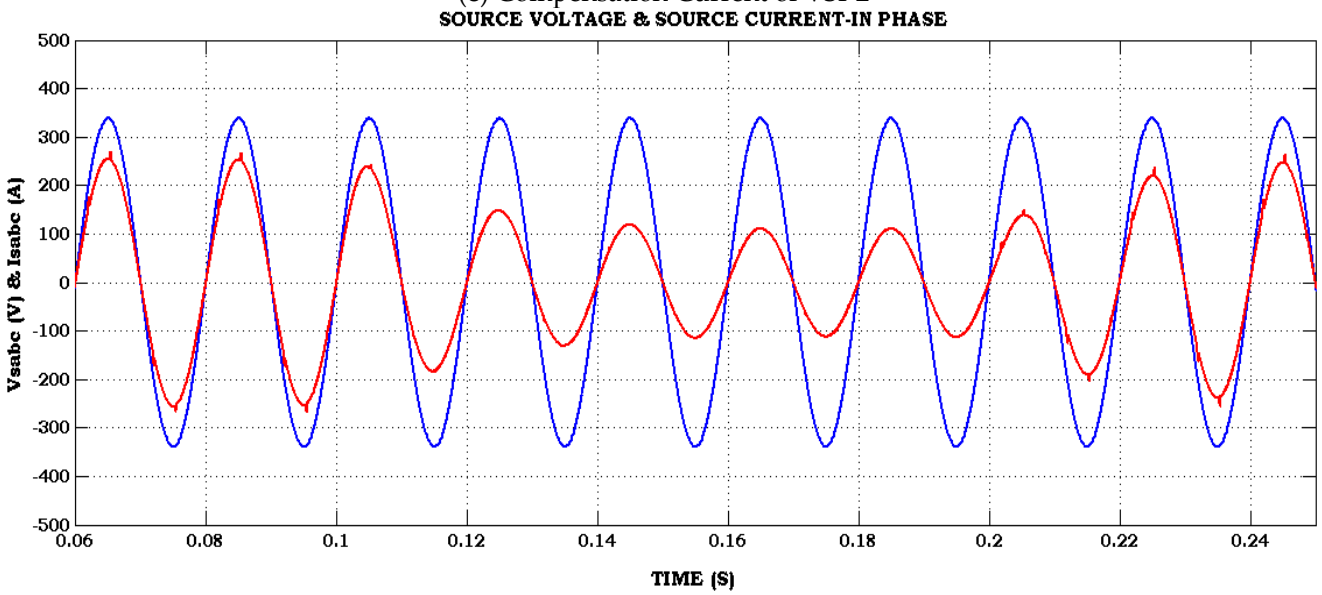
Figure 5. *Cont.*



(**d**) Compensation Current of VSI-1

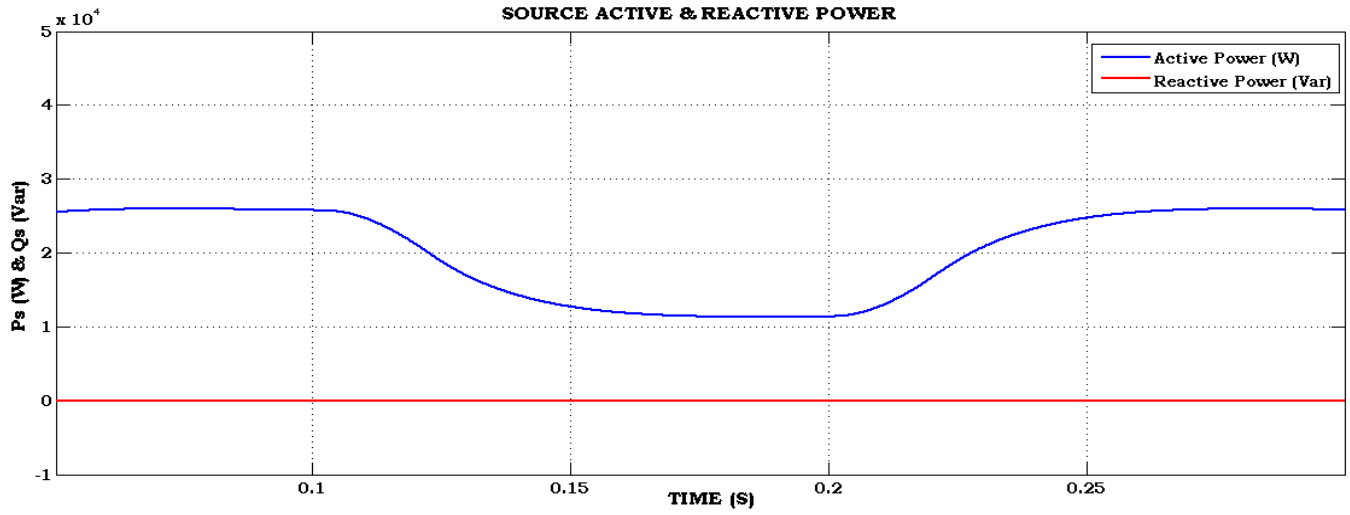


(**e**) Compensation Current of VSI-2

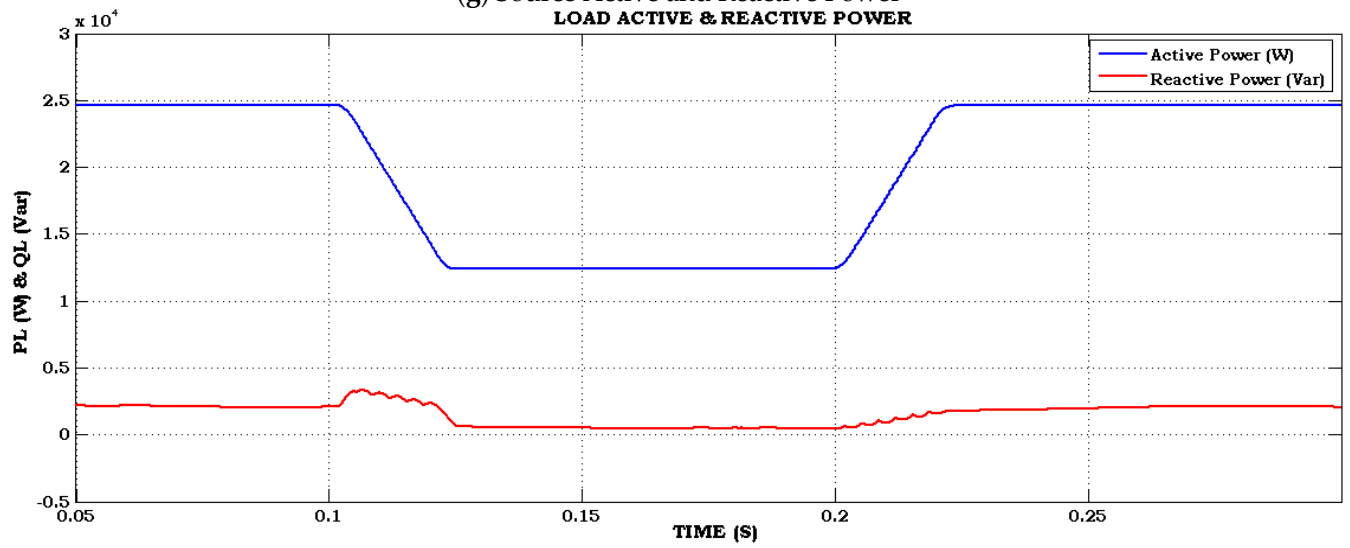


(**f**) Source Voltage and Source Current—In Phase

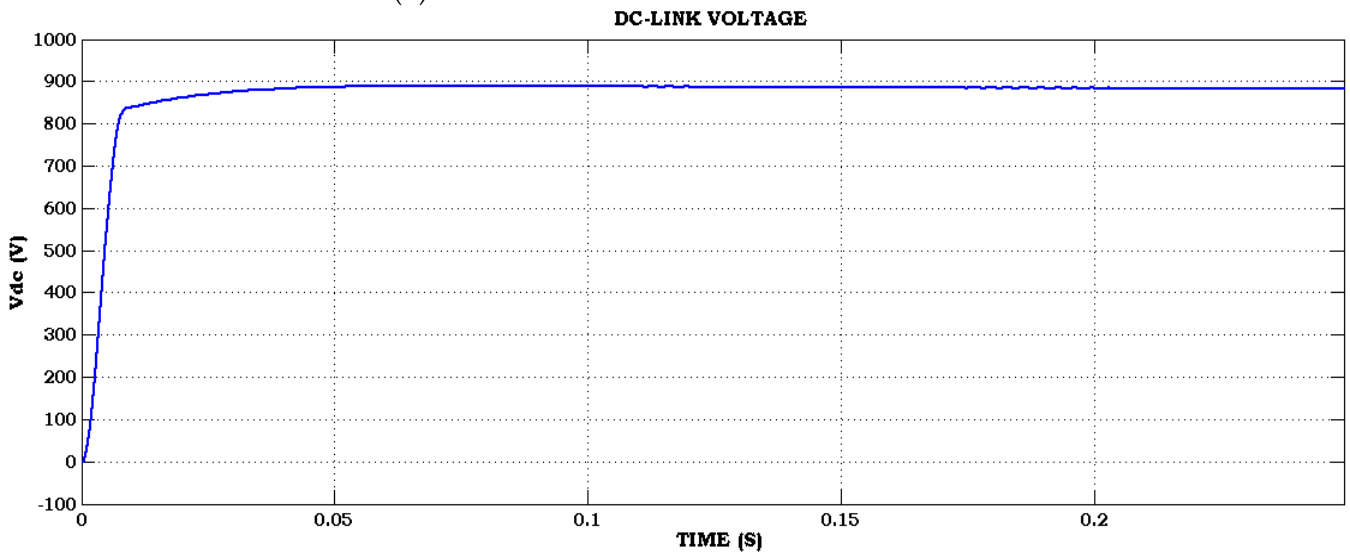
Figure 5. *Cont.*



(**g**) Source Active and Reactive Power

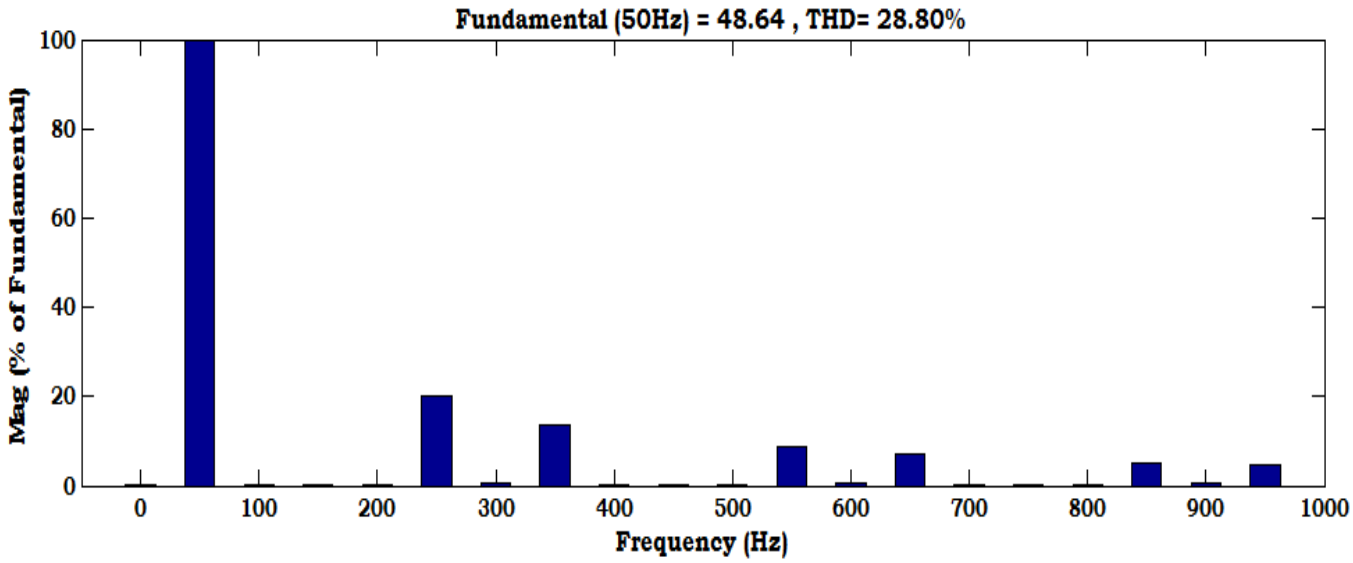


(**h**) Non-Linear Load Active and Reactive Power

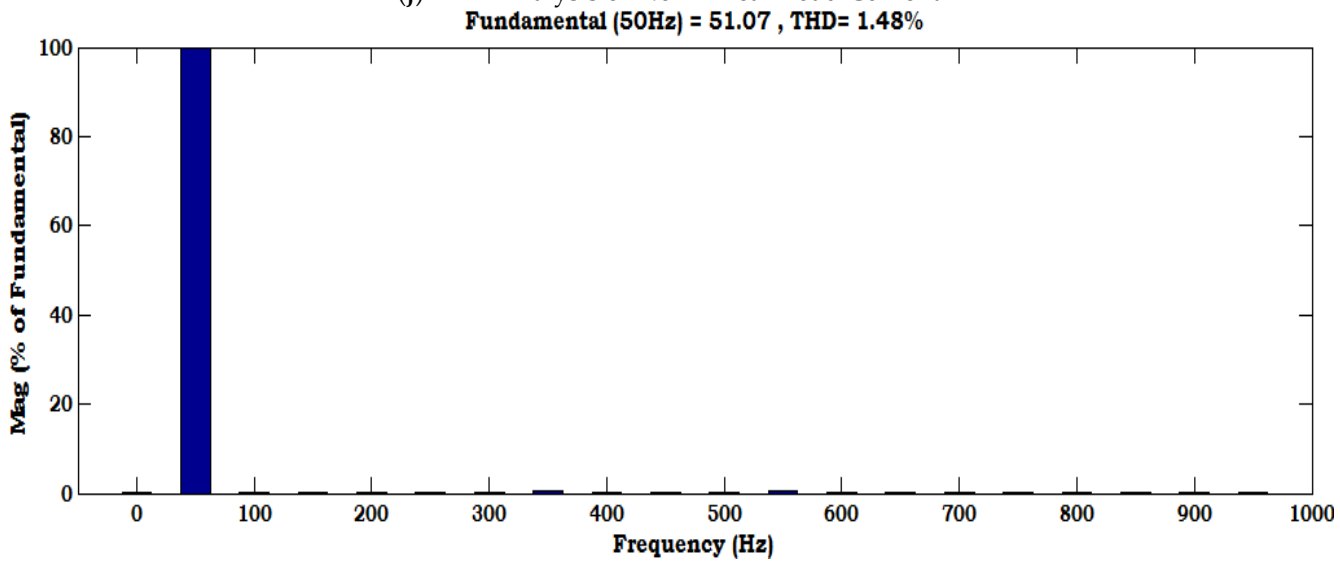


(**i**) DC-Link Voltage

Figure 5. *Cont.*



(**j**) THD Analysis of Non-Linear Load Current



(**k**) THD Analysis of Source Current

Figure 5. Simulation Results of the Proposed Combined Dc-Link Fed Parallel-VSIs-Based DSTATCOM for PQ Improvement under Variable Load Conditions.

The three-phase distribution system furnishes required energy to drive the Diode-Bridge Rectifier (DBR) as a variable non-linear load with a source voltage of 415 Vrms at 50 Hz fundamental frequency. In this case, the load considered is a variable non-linear power-electronic device switching between time instants 0.1 s < t < 0.2 s, which generates the sudden interrupted harmonic distortions in the source or PCC current and affecting the other loads connected close to the PCC of the distribution system. These current harmonics disrupt the frequency level and produce more heat, high loss quantities and damage the loads connected close to the PCC point.

The proposed combined DC-Link fed parallel-VSIs-based DSTATCOM is adopted to counteract the sudden interruptions and harmonic distortions in source current and maintain PCC parameters that are balanced, sinusoidal and linear in nature. The proposed common DC-Link fed parallel-VSI-based DSTATCOM operates by injecting compensation currents to counteract the harmonic distortions and regulates PCC voltage as a constant.

At time before t = 0.1 s, the load is considered as constant and the required compensation current is 20 A. The VSI-1 produces 10 A and the VSI-2 produces 10 A and as both are

connected in parallel form, the required compensation current of 20 A is met to comply with PQ enhancement features. The source current is maintained constant at a value of 52 A and the source voltage is maintained constant at a peak value of 340 V.

During sudden switching of reduction of non-linear loads, at time interval 0.1 s < t < 0.2 s, the proposed parallel-VSI DSTATCOM is able to mitigate the issues arising from such sudden interruptions. During this time interval, the required compensation current is 10 A, the VSI-1 produces 5 A and VSI-2 produces the remaining 5 A, and since both the VSIs are connected in parallel form, the required compensation current of 12 A is met to comply with PQ enhancement features. The source current is maintained constant at a value of 24 A and the source voltage is maintained constant at a peak value of 340 V.

The source voltage and the source current are in-phase conditions that represent an ideal power factor at the source/PCC (source current is multiplied by five times for a clear view of the in-phase condition). At time before t = 0.1 s, the input source generates requisite active power and reactive powers of 27 KW and 0.06 KVAR to achieve the load active and reactive powers of 25 KW and 2.2 KVAR through the proposed common DC-Link fed parallel-VSI DSTATCOM. During the sudden reduction of a load, at time 0.1 s < t < 0.2 s, the required power is injected/extracted by DSTATCOM. During this disturbance, the input source generates requisite active and reactive powers of 13 KW and 0.01 KVAR to meet the load active and reactive powers of 12.4 KW and 0.6 KVAR through the proposed common DC-Link fed parallel-VSI DSTATCOM.

Furthermore, the DC-link voltage is maintained constant at a value of 880 V with the help of DC-link regulator. It also reduces the circulation current flow towards the VSI and the DC-link capacitor. The THD of non-linear load current is 28.80% because of the presence of non-linear load devices that inject harmonic currents into the system. As it can be seen, the proposed combined parallel-VSIs-based DSTATCOM compensates for the sudden interruption and harmonics coming from the non-linear load, and thus the THD of source current is 1.48%, which complies with IEEE-519/2014 standards.

Comparative analysis and Graphical representation of THD values of load current and source currents of traditional & proposed DSTATCOM topologies under constant and variable load conditions are presented in Table 2 and in Figure 6, respectively.

Table 2. Comparison of THD Values of Load Current and Source Currents of Traditional and Proposed DSTATCOM Topologies under Constant and Variable Load Conditions.

THD (%)	Constant Load		Variable Load	
	Load Current	**Source Current**	**Load Current**	**Source Current**
Traditional VSI-DSTATCOM	29.55%	3.63%	–	–
Proposed Isolated Parallel-VSI DSTATCOM	29.61%	0.84%	28.72%	1.96%
Proposed Combined Parallel-VSI DSTATCOM	29.64%	0.81%	28.80%	1.48%

Compared to the traditional single VSI-based DSTATCOM topology, the proposed isolated and combined parallel VSIs-based DSTATCOM topologies offer low THD values, which represent good PQ enhancement features in a three-phase distribution system under both constant and variable load conditions. The current sharing principle of the traditional VSI and proposed parallel-VSIs-based DSTATCOM topologies is presented in Table 3 and the graphical representation of current sharing principle is illustrated in Figure 7, respectively.

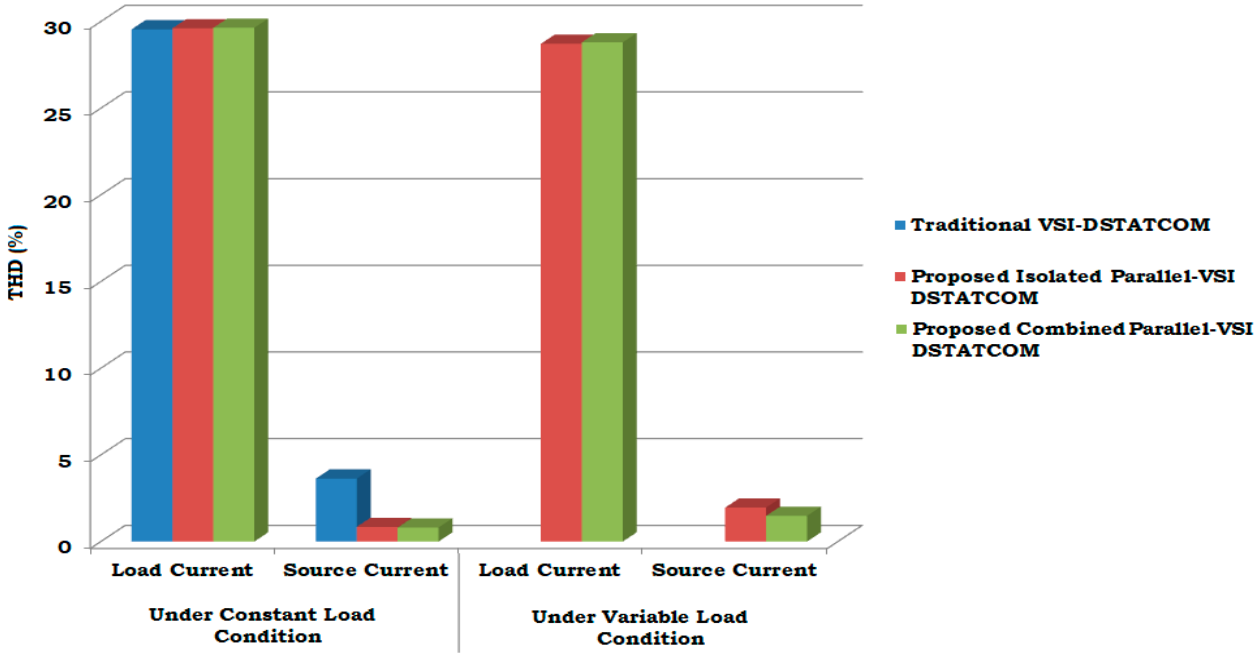


Figure 6. Graphical View-THD Values of Load Current and Source Currents of Traditional and Proposed DSTATCOM Topologies under Constant and Variable Load Conditions.

Table 3. Current Sharing Principle of Traditional VSI and Proposed Parallel-VSIs-Based DSTATCOM Operations.

	VSI-1 Current	VSI-2 Current	Total Current
Traditional VSI-DSTATCOM	12 A		12 A
Proposed Isolated DC-Link-Fed Parallel-VSI DSTATCOM	6 A	6 A	12 A
Proposed Combined DC-Link-Fed Parallel-VSI DSTATCOM	6 A	6 A	12 A

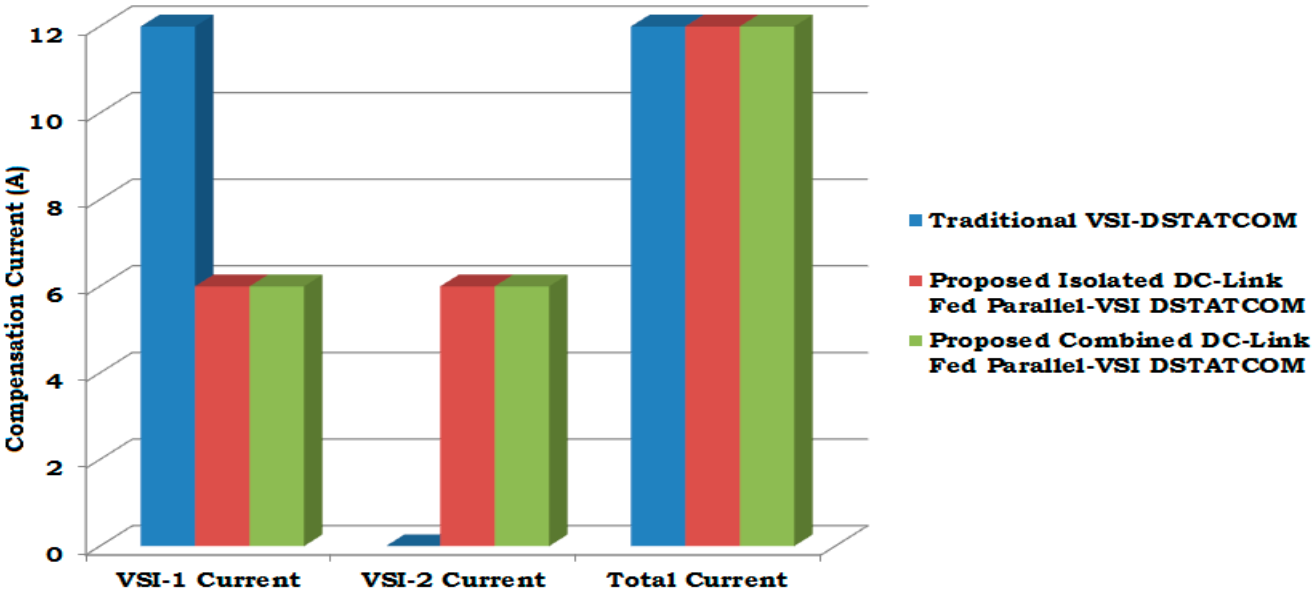


Figure 7. Current Sharing Principle of Traditional VSI and Proposed Parallel-VSIs-Based DSTATCOM.

In the traditional single VSI-based DSTATCOM, the total compensation current of 12 A is injected by single-VSI, which not only increases the burden on the VSI but also causes high switch stress, high switching losses, and decreased efficiency. In the proposed parallel VSIs-based DSTATCOM topologies, the total compensation current is shared and injected by coordinated control of both the VSIs. The VSI-1 and VSI-2 inject required current of 6 A each to achieve the required compensation current of 12 A. Thus, the proposed parallel-VSIs-based DSTATCOM topologies ensure less burden on the VSIs for many functions, low switch stress, low switching losses, high efficiency, etc.

5. Conclusions

In this article, the novel parallel-VSIs-based DSTATCOM topologies are employed for mitigating the harmonic distortions in the source current caused by the non-linear load. The proposed parallel DSTATCOM topologies compensate all the current-related PQ issues and maintain the PCC parameters as balanced, sinusoidal and linear in nature during sudden interruptions. The proposed novel topologies reduce the harmonic components in the source currents and maintain constant and continuous required load power flow during sudden interruptions. Furthermore, the proposed topologies, in conjunction with the novel proposed MIRP control scheme, provide the required reactive power to the load, improve power-factor and eliminate unbalanced loading and neutral current effects.

The proposed Isolated DC-link-based parallel-VSIs DSTATCOM and Combined DC-link-based parallel-VSIs DSTATCOM are highly suitable for enhancing PQ features in a three-phase distribution system. Over the above methods, the combined DC-link-type parallel-DSTATCOM is best suited because it requires a common/combined DC-link source, minimizes the number of sensing elements, ensures reliable operation and provides low-cost compensation.

Based on the above-specified merits, the proposed common DC-link-fed parallel DSTATCOM topology can be extended to the present day DG Integrated distribution systems for mitigation of various power quality issues and control of active and reactive powers in the system. For DG operations, the proposed combined DC-link based parallel-DSTATCOM does not require additional switching devices and advanced control schemes, which reduces the over-all compensation cost of the system, reliable power flow and high efficiency, etc.

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