# Real-time SSVEP measurements through Lock-in detection in FPGA-based platform

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**Abstract—** In this work, a method for measuring steady-state visually evoked potentials using the Lock-In technique is presented. The proposed method involves acquiring the electroencephalography signal through channel averaging from an ADS1299 sigma-delta converter, without the need for additional hardware to accommodate the signal and processing in real-time using an Intel MAX10 FPGA, while visual stimuli synchronized with the sampling and processing are generated. The result is a robust platform that allows determining a user's attention focus on visual stimuli flickering at 14.70, 16.67, and 19.23 Hz. The initial experimental tests of the system with three subjects validated the platform, obtaining an average signal-to-noise ratio of 3.2 in the detection, with a maximum of 6.2 in the case of an experienced SSVEP user.

**Keywords:** SSVEP, FPGA, EEG, Lock-in.

## 1 Introduction

Steady-state visual evoked potentials (SSVEPs) are useful in brain-computer interfaces since they allow a user's focus of attention to be associated to specific commands. Its operation is based on the presence of a visual stimulus $E_1$ flashing at a known frequency $f_{e1}$, used in conjunction with an electroencephalography (EEG) acquisition equipment that measures the response in the occipital area of the brain, responsible for visual processing. When the user is focusing their attention on $E_1$, the measured EEG signal contains components of frequency $f_{e1}$ and its harmonics. In this way, if a sufficiently strong component at that frequency is detected, the associated command is activated.

SSVEP-based systems use a variety of strategies for stimulation and detection. The first stage of such equipment is biopotential acquisition. Thanks to high-resolution analog-digital converters (ADCs) based on Sigma-Delta ($\Sigma\Delta$) modulators, it is possible to digitize EEG signals with bandwidths starting in low frequencies, avoiding otherwise necessary AC-couplings with large time constants that take time to recover the baseline after artifacts. Moreover, acquisition stages with low gains are possible, allowing signal integrity to be maintained in the face of large artifacts or electrode offset levels. Recently, a method that allows increasing the dynamic range of commercial converters,

achieving low noise levels compatible with direct EEG measurement while maintaining the maximum input dynamic range was published [1].

Achieving low noise levels on the input analog stage improves the robustness of the system. Furthermore, there are digital techniques that allow recovering signal components even with low signal-to-noise ratio (SNR), which can be applied to the detection of SSVEPs. In particular, the Lock-in technique is based on the injection of a reference carrier to obtain an indicator of the presence of components of the desired frequency in real time. Previous studies have used the Lock-In technique for the detection of SSVEP [2, 3, 4, 5] demonstrating similar or superior performance to traditional methods based on the discrete Fourier transform (DFT).

The methods needed to detect SSVEP components in intrinsically low SNR signals require extensive digital processing. Field Programmable Gate Arrays (FPGAs) have been identified as a lower cost alternative compared to a personal computer (PC) with sufficient processing power. One outstanding feature of these devices is to allow the implementation of modules that perform operations in parallel [6], which makes it possible to perform extensive calculations in real-time. In the case of detection with the Lock-in method this can be especially beneficial, since many channels can be implemented in parallel to detect different stimulus frequencies, only limited by the logic and memory units of the device. Furthermore, the system's implementation in an embedded system instead of a PC facilitates synchronization when implementing coherent detection schemes [7].

This work thus presents a SSVEP platform based on an FPGA, which performs real-time detection by the Lock-In method and the synchronized generation of visual stimuli. This strategy is combined with noise reduction by averaging independent measurement channels, making signal acquisition possible using commercially available components while reducing the analog stage to a minimum and maximizing the dynamic range. Evidence is provided of the feasibility of obtaining EEG with the averaging technique, and a method for obtaining the output of the detector in real time is shown.

## 2 Materials and methods

In the following subsections, the physical implementation of the system is presented. Next, the data processing strategy, its principle of operation, and its associated implementation is shown. Lastly, the experimental setup used to validate the platform is presented.

### 2.1 System description

The main blocks of the acquisition system and their interconnection are presented in Fig. 1. Part of this system was described in a previous publication [1]; thus, a brief description is provided here, highlighting the modifications made for the present work.

Analog-to-digital conversion is implemented with an ADS1299 ADC from Texas Instruments. This ADC has 8 independent channels, each with a programmable gain

amplifier (PGA). The 8 channels perform simultaneous sampling of each differential input. The data rate is configurable, and it is set to its lower value of 250 Hz which results in a 0 to 65 Hz bandwidth due to the ADC's digital filter and is sufficient for the intended measurement. The only additional analog elements are active electrodes implemented with TLC2201 operational amplifiers (OAs) in unity-gain buffer configuration, and an independent DRL circuit [8] that sets the reference voltage on the patient and rejects electromagnetic interference.

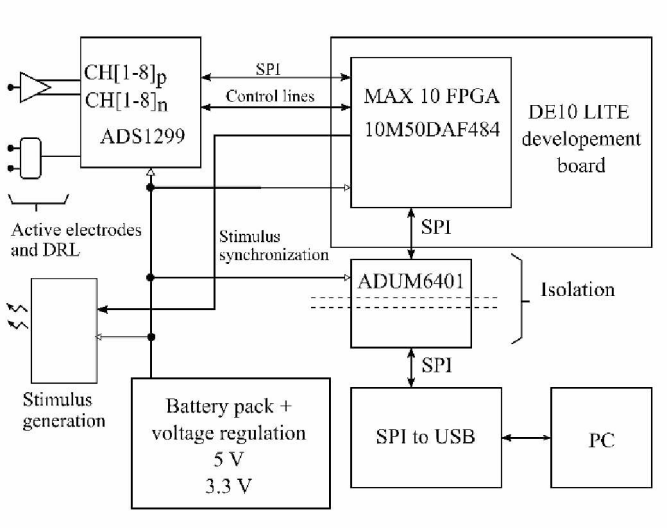


**Fig. 1.** Acquisition system block diagram.

The central control element of the system is a MAX 10 10M50DAF484C7G FPGA from Intel (previously Altera), available in a DE10 Lite development board from Terasic. The system was configured with a set of finite-state machines (FSMs) controlling:

- A communications interface that programs the ADS1299 registers and receive its data output.
- Summing logic that performs the channel averaging, minimizing the input noise.
- The generation and detection subsystems implemented through Lock-In modules, including outputs to produce the stimulus.
- A communications interface to send data in real-time to a PC.

The ADS1299 interface consists of a serial peripheral interface (SPI) bus operating as Master, in addition to control lines required by the converter. The interface to the PC is implemented using a second master SPI bus that transmits the processed output data in a format compatible with serialized transmission.

The system was designed as a complete biopotential acquisition platform including medical grade isolation to allow in-vivo measurement. The isolation was achieved through the use of an ADuM6401 chip from Analog Devices which implements an

isolated SPI bus. The power supply for the system is a pack of regulated lithium batteries on the isolated side and the USB bus from the PC on the opposite side. The digital system power supply was kept separate from the analog power supply for the ADC, active electrodes, and the DRL.

The complete block diagram of the processing system is shown in Fig. 2. A 50 MHz clock signal available in the DE10 Lite board was used and fed as input to a phase locked loop (PLL) to obtain the master clock signal at 100 MHz. The master SPI module was obtained from the project SPI MASTER/SLAVE from OpenCores [9], while the rest of the implemented modules were developed by the authors, with the inclusion of proprietary blocks (IPs) available in the free version of Quartus II software.

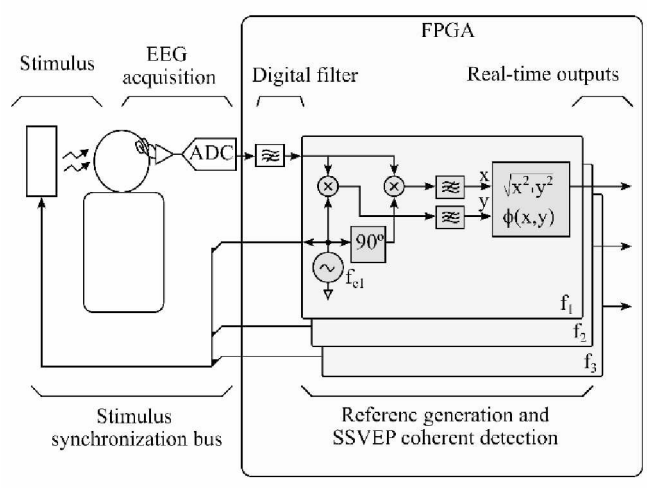


**Fig. 2.** Schematization of the detection process.

## 2.2 Acquisition stage

EEG signals require a very low noise-floor. An exhaustive evaluation of the noise level necessary for EEG acquisition systems was conducted in [10], where the authors conclude that an spectral noise amplitude of 10 nV/√Hz is appropriate, and only in the case of using skin abrasion or puncturing would a lesser value be required.

The aforementioned noise level is less than that achievable with a single channel of ADS1299, so the EEG signal $x_i(t)$ is sampled in parallel using the 8 available independent channels and averaged to reduce the noise-floor and augment dynamic range, obtaining:

$$x[k] = \frac{1}{8}\sum_{i=1}^{8} x_i[k] = s_i[k] + n[k]/\sqrt{8}.$$

For the ADS1299 in its 250 Hz data-rate configuration, this results in a 7 nV/√Hz noise level which allows, for example, when using the TLC2201 OA, the resulting DEP being dominated by the OA and not the ADC. When conducting measurements with superficial electroencephalography electrodes, a higher noise level is generally obtained; however the design of the presented equipment guarantees that EEG acquisition can be successfully conduced with sufficient SNR in any condition.

### 2.3 Detection stage

SSVEP detection is implemented with a Lock-In stage per each stimulus frequency as depicted in Fig. 2. For each stimulus frequency $f_e$ a reference signal of value $r(n) = A\ sin(2\pi f_e n)$ is produced in a "generation and detection" module. This signal is gated to produce a square wave made available on a general-purpose output pin of the FPGA.

The output of the ADC is a sequence (discrete signal) $s(n)$, where $n$ is the discrete time variable. This signal is high pass filtered to remove its mean value resulting in $s_{ac}(n)$ which is then routed to the generation and detection modules. Each detection module multiplies the measured signal with its corresponding reference and a quadrature version of the reference, obtaining:

$$r_c(n) = r(n)e^{j\pi/2}$$
$$x(n) = s_{ac}(n) \times r(n)$$
$$y(n) = s_{ac}(n) \times r_c(n)$$

For the component of the signal $s_{ac}(n)$ which has the same frequency as the reference signal, this multiplication generates a base-band component and another component at twice the frequency. If a low-pass filter is applied after each multiplication, the high frequency component can be eliminated and signals x and y result which contain the modulus and phase information of the signal $s_{ac}(n)$ at the frequency of interest. These values can be obtained according to:

$$s_{o,m}(n) = \sqrt{x^2 + y^2},$$
$$s_{o,p}(n) = \arctan\left(\frac{y}{x}\right).$$

Further, this combination of multiplier (or mixer) and low-pass filtering has the property of greatly attenuating components of the signal of other frequencies different from $f_e$. This operation is known as applying a two-phase Lock-In [11].

A crucial element in the described system is the low-pass filter that is utilized for eliminating out-of-band components after the mixing stage. The more selective this filter is, the better it can reject unwanted components close to $f_e$. In this implementation, moving average filters were employed which are updated sample-by-sample encompassing a configurable time window of N samples in total.

The N-sample moving-average filter also presents transmission zeros at integer dividers of N [12]. This means that if N is chosen as an integer number of signal cycles a complete filtering of the component at $2f_e$ can be achieved after mixing. At the same time, there is a restriction on the frequencies that can be generated, since they must be synchronized with the sampling frequency. After preliminary tests, a window size N

equivalent to 2 seconds was determined as a compromise between the filter selectivity and the system responsiveness.

The phase signal $s_{o,p}(n)$ can be useful in the case of producing phase-codifies stimulus [13]. In the case of experimental tests conducted for this work, 3 different stimuli of different frequencies $f_1$, $f_2$, and $f_3$ were configured, hence only the modulus output was necessary.

### 2.4 Experimental set-up

First, to verify the equipment's operating parameters, noise measurements were taken by short-circuiting the active electrodes with the DRL and recording 60 seconds of the resulting output signal. Additionally, the frequency response of each Lock-In was calculated using an algorithm identical to the one implemented in the FPGA. This calculation was performed by applying sinusoidal waves of known frequencies and capturing the values settled after a 10-second period.

Secondly, for conducting experimental SSVEP tests, a stimulator was implemented using a commercially available 8x8 matrix of WS2812B LEDs, to which a diffuser was applied thus generating uniform illumination in a 6 cm × 6 cm rectangle, enhancing SSVEP responses [7]. Previous studies have shown that LED panel stimulation produces a greater amplitude in the fundamental SSVEP frequency compared to other options such as CRT or LCD monitors [14]. The LED panel was managed by a microcontroller that received stimulus synchronization signals through a bus from the FPGA (Fig. 2). The microcontroller further implemented an automated test protocol: it displayed a green light for 5 seconds signaling the start of the experiment, followed by 5 seconds without stimulation, and then 5 seconds with stimulation at frequencies $f_1$, repeating this pattern for frequencies $f_2$ and $f_3$. The generated data was captured on a PC, where an AC-coupled version (high-pass filtered with 3 Hz cut-off frequency) of the measured signal together with the output from each Lock-In was received.

The electrodes used were of the gold cup type, applied with EEG paste and placed at positions O1, O2, while the DRL electrode was positioned on the forehead using standard wet Ag/AgCl adhesive electrodes. Tests were conducted with three participants, S1, S2, and S3, each with low, high, and medium levels of prior training with other SSVEP-based interfaces, respectively.

## 3 Results

The equipment's operating parameters are presented in Table I, and the FPGA compilation report is detailed in Table II. The spectral noise amplitude, referred to the input (RTI), is depicted in Fig. 3, while the frequency response of the detection system is illustrated in Fig. 4. The experimental setup during a measurement is displayed in Fig. 5.

**Table 1.** Operating parameters

| Parameter | Value |
|---|---|
| RTI noise | 0.24 $\mu V_{rms}$ |
| Data rate | 250 Hz |
| Acquisition bandwidth | 64 Hz |
| Detection bandwidth | 0.45 Hz |
| Stimulus frequency | $f_1$=16.67 Hz<br>$f_2$=19.23 Hz<br>$f_3$=14.70 Hz |

**Table 2.** FPGA usage report

| Element | Used number (percentage) |
|---|---|
| Logic elements | 28016 (56%) |
| Memory bits | 386560 (23%) |
| Embedded multipliers | 216 (75%) |
| PLLs | 1 (4%) |
| Registers | 8763 (18%) |

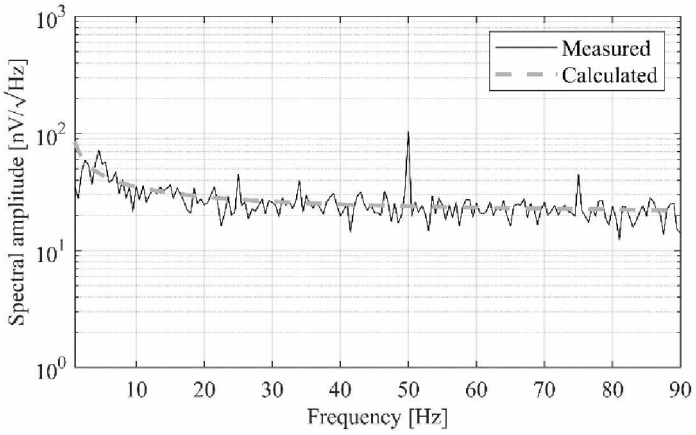


**Fig. 3.** Noise measurement with active electrodes connected to the system's DRL

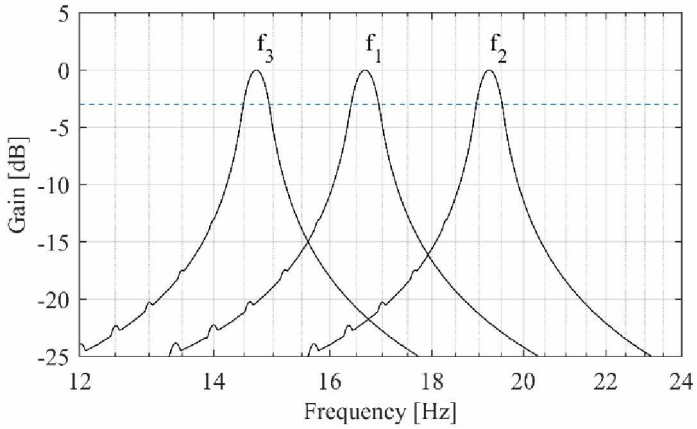


**Fig. 4.** Frequency response of the implemented Lock-Ins

**Fig. 5.** Experimental setup. The measurement electrodes, DRL on the forehead, and stimulator are observed.

The outputs of the system for two trials of each of the 3 participants are shown in Fig. 6, where the detection signals for the SSVEP elicited by each stimulation frequency can be verified by visual inspection. Reference markers were included in dashed line to assess the stimulus timing. This information was used for the calculation of the resulting SNR, considering the presence of the stimulus in 5-second windows separated by 5-second intervals (generated by the automated testing protocol). A delay was included to account for the Lock-In time window and an indeterminate period of the order of tenths of a second between the green light signaling the commencement of the protocol and the start of the recording performed by the experimenter through the push of a button.

The SNR was obtained through the following equation:

$$SNR_i = \frac{\sum_{t_i}^{t_i+5s} x_{f_i}(t)}{\sum_{t_i-5s}^{t_i} x_{f_i}(t)}$$

where $x_{f_i}$ is the output from each detector and $t_i$ is the starting time of each 5 s window containing the response to the stimulus. An average value of $3.2 \pm 1.7$ was obtained and by visual inspection it can be corroborated that in windows with SNR>2 the stimulus response presence can be easily distinguished.

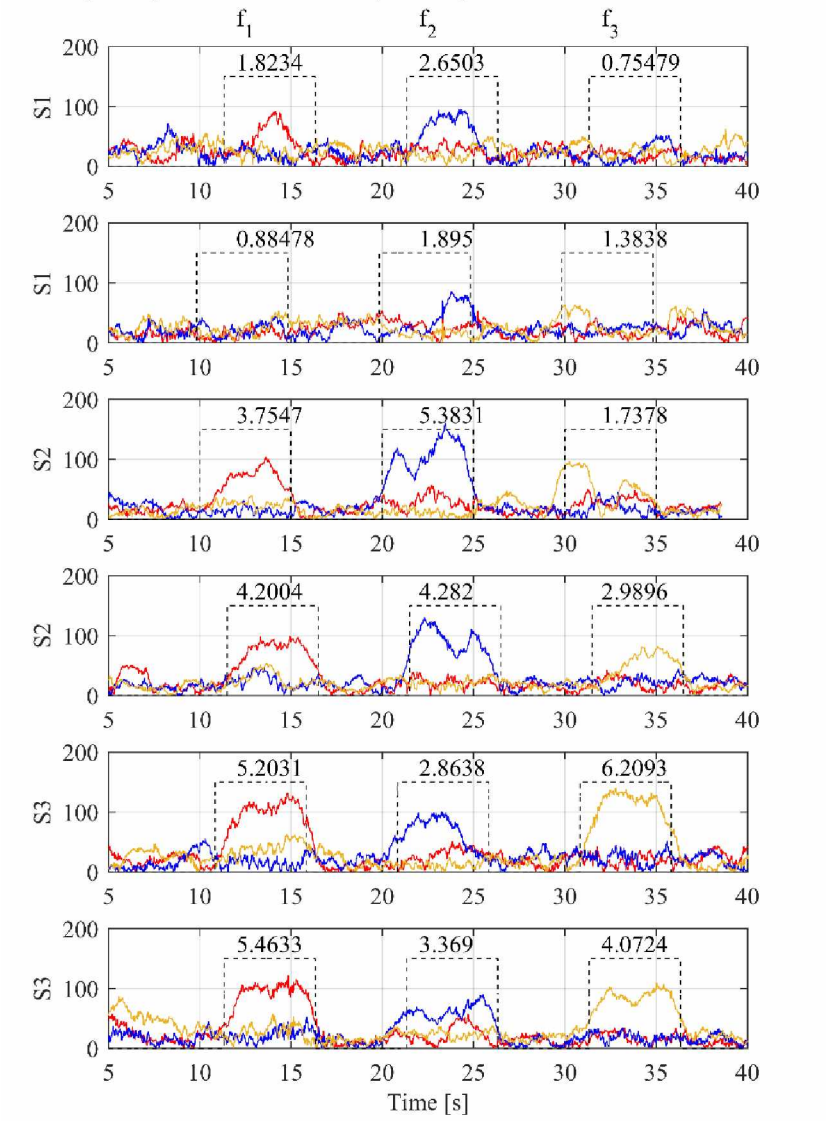


**Fig. 6.** Outputs from the implemented detectors. The superposed numbers indicate the SNR comparing the signal between the 5 s period marked in dashed line and the immediately previous 5 s period. S1, S2 and S3 identify the participants.

## 4 Discussion

The conducted experiments demonstrated the system's ability to acquire electroencephalography signals, detect the presence of SSVEPs in real-time using a 2-second moving average Lock-in filter, and simultaneously transmit data to a PC. Furthermore, by analyzing the records of subjects S1, S2, and S3, a consistent result was obtained in comparison with the previously reported observation [7] that training improves SSVEP levels. While a longer time constant could be used to achieve greater selectivity in the filters, potentially compensating for the lack of training, this would lead to a degradation in system responsiveness.

The choice of an FPGA as the processing platform enabled the parallel implementation of generation and detection modules, ensuring complete synchronization between stimuli, data acquisition, and signal processing. As seen in the FPGA's compilation report and considering that embedded multipliers can be replaced with other logic elements in the design, more modules could still be implemented with this platform, making it easily scalable. For example, an increase in the associated commands could be explored by implementing a combination of phase and frequency encoding for the stimuli [15].

## 5 Conclusions

A method was presented that allows measuring EEG signals and detecting the presence of SSVEPs. The primary contribution was demonstrating the Lock-In technique for SSVEP detection on an FPGA, which was achieved by integrating existing methods from the literature into a novel platform capable of performing stimulation, measurement, and SSVEP detection using commercially available components.

The system was experimentally validated, successfully detecting SSVEPs with an average signal-to-noise ratio of 3.2 times, indicating the feasibility of employing the system in future brain-computer interface implementations.

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