COMPACT MODELING OF VARIABILITY IN ORGANIC THIN-FILM TRANSISTORS

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Compact Modeling of Variability in Organic Thin-Film Transistors

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DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
and Prof. Dr.-Ing. Alexander Kloes

Department of Electronic,
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I STATE that the present study, entitled “Compact Modeling of Variability in Organic Thin-Film Transistors”, presented by Aristeidis Nikolaou for the award of the degree of Doctor, has been carried out under my supervision at the Department of Electronic, Electrical and Automatic Control Engineering of this university.

Tarragona, Spain, July 3, 2023

Doctoral Thesis Supervisor/s

Prof. Dr.-Ing. Alexander Kloes

Prof. Benjamin Iñiguez Nicolau

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List of Acronyms

Latin Alphabet

Symbol	Description	Unit
B1	Bending state 1	
B2	Bending state 2	
BSIM-BULK	Commercial compact model	
C10-DNTT	pseudo-transistor 4	
CMOS	Complementary metal oxide semiconductor	
DNTT	pseudo-transistor 6	
DOS	pseudo-transistor 7	
DPh-DNTT	pseudo-transistor 8	
EDA	Electronic design automation	
EKV	Compact model	
F1	pseudo-transistor 11	
F2	pseudo-transistor 12	
HOMO	Highest occupied molecular orbital	
LUMO	Lowest unoccupied molecular orbital	

MC	Monte Carlo
NOVA	Noise Based Variability Approach
PEN	Polyethylene naphthalate
PFBT	Pentafluorobenzenethiol
PSD	Power spectral density
RMS	Root-mean-square
SAM	Self-assembling monolayer
T1	Pseudo-transistor 1
T2	Pseudo-transistor 2
TFT	Thin-film transistor
U_T	Thermal voltage
VerilogA	Industry standard modeling language
V_{T0}	Threshold voltage

List of Symbols

Latin Alphabet

Symbol	Description	Unit
a	Subthreshold slope factor	$[-]$
a_c	Coulomb scattering coefficient	$[Vs/C]$
a^*	Parameter that is related to the Coulomb scattering coefficient	$[Vs/m^2]$
AF	Flicker Noise frequency exponent	$[-]$
C^*	One-dimensional	ii
C^*_{noise}	One-dimensional	ii
C'_{ox}	unit-area gate-dielectric capacitance a	$[F]$
E	Energy	$[eV]$
E_0	Center of the Gaussian distribution of the density of states	$[eV]$
E_a	Activation energy	$[eV]$
E_c	Conduction band energy	$[eV]$
E_F	Fermi energy	$[eV]$
E_g	Band gap energy	$[eV]$
$E\mu$	Energy at which the states are regarded as mobile states	$[eV]$
G	Conductance	$[S]$
G_1	Conductance of the T1 pseudo-transistor	$[S]$

G_2	Conductance of the T2 pseudo-transistor	$[S]$
G_{CH}	Local channel conductance in a transistor	$[S]$
G_m	Gate conductance	$[S]$
id	Normalized drain-current	$[-]$
$I_{D(x)}$	Drain-current at point x	$[A]$
I_{DS}	Drain-source current	$[A]$
I_{ON}	On-state current	$[A]$
I_{out}	Output current	$[A]$
I_{ref}	Reference current	$[A]$
I_{vt0}	Drain-source current at threshold voltage	$[A]$
k	Bolzmann constant	$[JK^{-1}]$
L	Channel length	$[m]$
l_{ch}	Channel length parameter used for Monte Carlo simulation	$[m]$
$N(x)$	Number of charge carriers per unit area	$[Vs/m^2]$
$Nst0$	One-dimensional	$[Vs/m^2]$
Nt	One-dimensional	$[Vs/m^2]$
q	Elementary charge	$[C]$
Q^*	One-dimensional	$[Vs/m]2$
Q_{CH}	Charge density per gate area in the channel of the transistor	$[Vs/m^2]$
q_{ch}	Normalized charge density per gate area in the channel of the transistor	$[-]$
$Q_{CH}(x)$	Charge density per gate area in the channel of the transistor	$[Ascm^{-2}]$
Q_D	Total charges at source terminal	$[As]$
q_s	Normalized charge density at the drain end of the channel	$[-]$
Q_g	Total charges opposing the channel-charge at the gate terminal	$[As]$

Q_S	Total charges at source terminal	$[As]$
q_s	Normalized charge density at the source end of the channel	$-$
R_{ij}	Distance between localized states	$[m]$
R_{max}	Critical distance	$[m]$
S	Subthreshold swing	$[mV/dec]$
S_{ID}	PSD of the total drain-current fluctuation	$[A^2Hz^{-1}]$
T	Temperature	$[K]$
T_0	Characteristic temperature	$[K]$
V_{CH}	Channel voltage	$[V]$
v_{ch}	Normalized channel voltage	$[-]$
V_D	Voltage at drain terminal	$[-]$
v_d	Normalized voltage at drain terminal	$[V]$
V_S	Voltage at source terminal	$[-]$
v_s	Normalized voltage at source terminal	$[V]$
W	Nominal channel width	$[m]$

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CHAPTER 1

Introduction

1.1 Organic Transistors and Variability Overview

Organic thin-film transistors (OTFTs) share the same operation principles with these of the typical inorganic solid state FETs, with the difference that in the former, the semiconductor material usually consists of a thin polycristalline layer of conjugated organic molecules [1]. OTFTs, due to their low-temperature processing properties, are commonly used as the basic building blocks for low-cost and large-area electronics integrated circuits such as printed bio-sensing configurations [2, 3], flexible sheet-type Braille displays [4] and organic light-emitting diode (OLED) applications [5]. In contrast to conventional silicon MOSFETs, where the conduction channel is formed due to an inversion of the semiconductor material, organic TFTs are operational when biased on accumulation [14]. The materials used in an OTFT are different from those used in a conventional MOSFET and typically, the source/drain electrodes consist of gold. Between the electrodes of the device and the channel, the metal-semiconductor interface behaves similarly to a Schottky contact. Typically, p-type organic transistors are fabricated and utilized. More detailed information regarding the structure and layout of organic TFTs are discussed later in the manuscript.

Although organic TFTs are in principle different from conventional MOSFETs the theory of band bending due to the applied voltages can be used during

transistor modeling. There are numerous models used to describe the charge transport in organic materials [6] namely, the mobility-edge model, the multiple-trap-and-release model, the variable-range-hopping model, or the percolation model [7]. In the variable-range-hopping model, it is assumed that the charge transport occurs mainly by the hopping of charge carriers between molecules. If several molecules are located close to each other, each of them has its own energy diagram. Unlike the crystalline semiconductors, there is not "distinctive" valence and conduction bands. The delocalized electrons of a π conjugated system can move within the system "space". This means that an electron can move freely around the molecule. Furthermore, a delocalized electron can leave its original molecule and can move over to the $\pi-$ orbital of an adjacent molecule. This mechanism allows the charge transport over several molecules and it is typically described as a variable-range hopping transport . In Fig. 1.1 a simplified demonstration of the variable-range-hopping transport in OSCs is shown. Despite the fact that charge transport in organic materials is different from that in crystalline semiconductors, it is possible to model the current flowing through the organic device assuming a band-like transport of a very low mobility [36]. A model accounting for the hopping transport can then be adapted in terms of an effective mobility [37] and will be discussed later in the current manuscript.

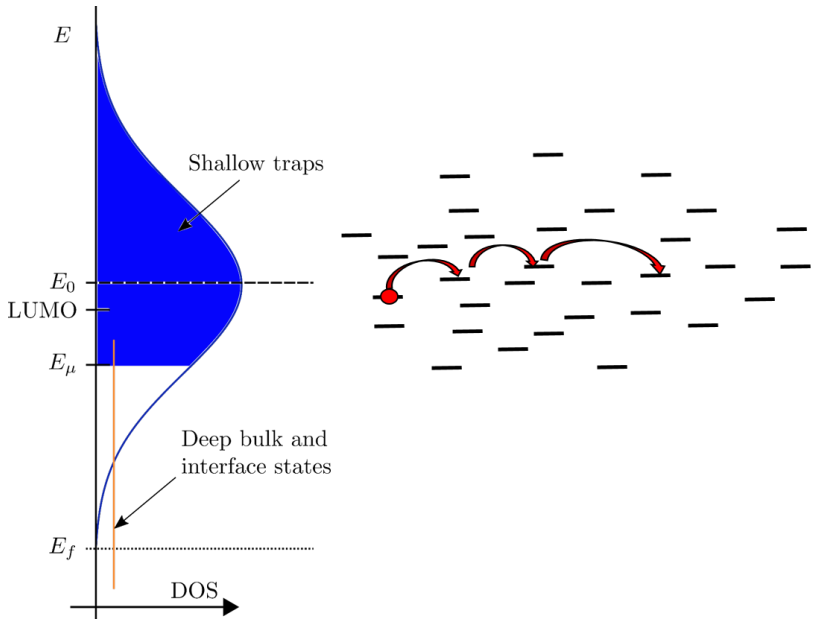

Figure 1.1.: Demonstration of the variable-range-hopping transport in OSCs [8].

1.2 Compact Modeling

Compact Modeling refers to the development of models for integrated semiconductor devices for use in circuit simulations. The models are used to reproduce device terminal behaviors with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit or system-level simulation. Typically, the users of the models are the IC designers. The industry's dependence on accurate compact models continues to grow as circuit operating frequencies increase and device tolerances scale down with concomitant increases in chip device count, and analog content in mixed-signal circuits. Compact modeling is a critical step in the design cycle of modern IC products. BSIMBULK [9] and HISIMHV [10] are two widely known commercial models.

In the case of organic TFTs, the efficient design of electronic systems is accomplished with the help of circuit simulators, which require physics-based compact models that accurately predict the electrical behavior of the organic

transistors. Similarly as in the commercial silicon technology, physics-based compact models need to cover a wide range of the organic transistor properties, such as DC behavior [11, 12], AC behavior [13], short-channel effects [14], drain-current variability [15, 16] and low-frequency noise (LFN) [17].

1.3 State of the Art

In this section, an overview of similar or related research-work to the one that is presented in the current PhD dissertation manuscript is discussed. The study of the variability of the electrical characteristics of organic TFTs, similarly as in silicon MOS transistors, is a topic still under investigation. Drain-current variability can be perceived as the time-independent variation of the drain current of two or more nominally identical transistors under the same biasing conditions. Drain-current variability of organic-TFT-based circuits is commonly determined using circuit-based Monte Carlo simulations [18], mismatch modeling [19] or novel noise-based simulation approaches [20]. Here, a device-level charge-based variability model is introduced [15]. The proposed physical model has two fitting parameters, can be applied directly to the experimental statistical population without the need for Monte Carlo simulations and accurately describes the bias-dependent variability of organic TFTs, fabricated either in the coplanar or the staggered device architecture.

Parameter variability can be perceived as statistical fluctuations in the values of the electrical parameters of electronic devices. In the case of field-effect transistors, this includes fluctuations in the threshold voltage, the charge-carrier mobility and the channel dimensions [21, 22]. The impact of transistor-parameter variability on the performance of integrated circuits is usually predicted by Monte Carlo (MC) simulations [23]. As an alternative, a noise-based simulation technique initially introduced in [20] with the name ”Noise Based Variability Approach” (NOVA) is presented here. The proposed method is suitable for commercial electronic device automation (EDA) software tools and is expected to accelerate the process of approximating the influence of parameter variability on integrated circuits.

In order to expand further the effect of variability occurs in device-level,

the variability of analog organic-TFT-based circuits was studied by considering experimental data acquired from a large number of TFT-based current mirrors, fabricated on a flexible polymeric substrates [24].

In organic TFTs, Low Frequency Noise (LFN) is dominated mainly by carrier-number fluctuations due to grain-boundary traps, and less by carrier scattering at the semiconductor-dielectric interface [25]. Accurate LFN modeling of organic TFTs has been successfully demonstrated by adopting the theory of carrier-number-correlated mobility fluctuations [26, 27] and the empirical Hooge approach [28–30]. In the current manuscript, a bias-dependent model for the drain-current low-frequency noise (LFN) in organic TFTs is introduced [17]. The charged-based model proposed here takes into account the two discrete effects that constitute the sources of the flicker noise in organic TFTs, namely the noise due to the carrier-number and correlated mobility-fluctuation effect (ΔN or McWorther model) and the noise due to the fluctuation of the charge-carrier mobility ($\Delta\mu$ or Hooge model).

Over the past few years, research aiming at a better understanding and improved modeling of the behavior of flexible organic TFTs under mechanical stress has been conducted [31–33]. In the current manuscript, we analyze the bending-induced changes occurring in the DC performance of organic TFTs by considering experimental data acquired from a large number of TFTs, fabricated on flexible polymeric substrates [35].

1.4 Outline

In the current manuscript a set of subjects covering modeling and simulation aspects of the variability of the electrical properties of organic TFTs are presented.

In Chapter 2, a device-level charge-based variability model, suitable for organic-TFTs is introduced [15]. The proposed model is based on charge-carrier-number-fluctuation and correlated-mobility-fluctuation effects and can be applied to TFTs fabricated in the coplanar or the staggered device architecture.

An efficient alternative to the Monte Carlo statistical-analysis methodology is presented in Chapter 3 [20, 34]. The proposed "Noise-Based Variability Approach" (NOVA) method has been tested on circuits based on organic TFTs and has been

shown to be suitable for fast process and mismatch statistical circuit analyses.

In Chapter 4, the variability-aware characterization of organic TFT-based circuits is studied [24]. Here, a large number of discrete organic TFTs and TFT-based current mirrors were fabricated on flexible polymeric substrates and characterized, accordingly.

A bias-dependent model for the drain-current low-frequency noise (LFN) in organic TFTs is introduced in Chapter 5 [17]. The proposed model takes into account the noise due to the carrier-number and correlated mobility-fluctuation effect (ΔN or McWorther model) and the noise due to the fluctuation of the charge-carrier mobility ($\Delta\mu$ or Hooge model).

In Chapter 6, the bending-induced changes in the electrical-performance of organic TFTs are shown [35].

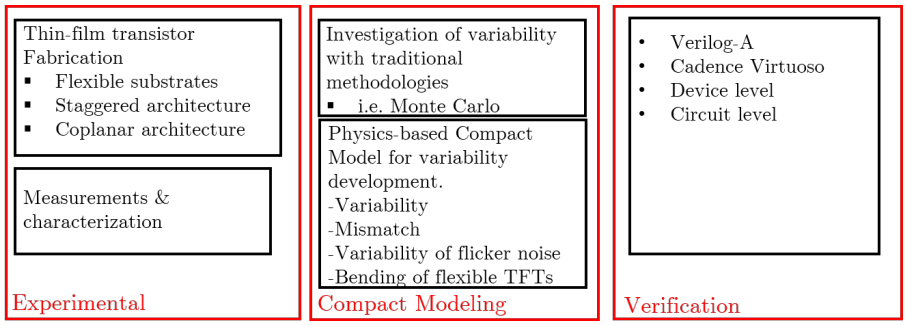

Figure 1.2.: Block diagram of the procedure followed in order to realize the current study.

CHAPTER 2

Drain-Current Variability Charge-Based Model

In the current section, a device-level charge-based drain-current variability model is introduced [15]. The proposed physical model has two fitting parameters, can be applied directly to the experimental statistical population without the need for Monte Carlo simulations and accurately describes the bias-dependent variability of organic TFTs, fabricated either in the coplanar or the staggered device architecture.

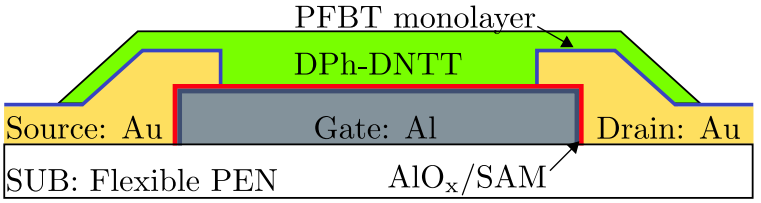

Figure 2.1.: Cross-section of the organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) architecture.

2.1 Charge-Based DC Model

For the derived variability model, the charge-based organic-TFT model that was initially introduced in [11] and extended accordingly in [36, 37] and [38], will be used as the basis. The proposed current-voltage model assumes a band-like hopping charge-transport inside the organic semiconductor (OSC) and Gaussian

density of states (DOS) according to:

$$\Gamma(E) = \frac{N_{st0}}{\sqrt{2\pi}\sigma_{DOS}} exp\left(-\frac{(E-E_0)^2}{2\sigma_{DOS}^2}\right). \tag{2.1}$$

The term N_{st0} account for the maximum number of states, E_0 is the center of

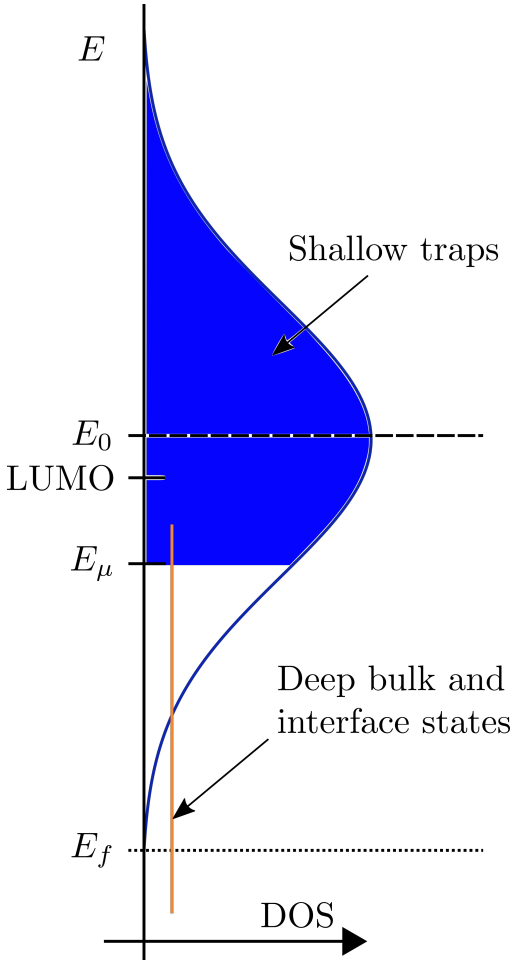

Figure 2.2.: Gaussian density of states (DOS).

the distribution and σ_{DOS} is the standard deviation. The model provides a single

current equation that is valid for all operation regions that can be obtained from

$$I_{DS} = \mu W \left(\frac{kT}{q} \frac{Q_S - Q_D}{L} + \frac{Q_S^2 - Q_D^2}{2LC'_{ox}} \right) \times \left(1 + \lambda \left(V_{DS} - V_{Dsat}\right)\right), \tag{2.2}$$

where W is the channel width, L is the channel length, C'_{ox} is the unit-area gate-dielectric capacitance and λ is the channel-length modulation factor. The effective carrier-mobility μ, which is described by the typical power-law mobility, is given by

$$\mu = \mu_0 \left(\frac{Q_S}{C'_{ox}} \right)^{\beta}, \tag{2.3}$$

where μ_0 is the low-field mobility and β is the unitless exponent of the power-law. Q_S and Q_D describe the density of quasi-mobile charges per gate area at the source and drain end of the channel, respectively, and can be expressed as

$$Q_{S,D} = \frac{S}{\ln(10)} C'_{ox} \mathcal{L} \left\{ \exp\left(\frac{V_{GS,D} - V_{T0}}{S/\ln(10)} \right) \right\}, \tag{2.4}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, V_{T0} is the threshold voltage and

$$S = aln(10)U_T \tag{2.5}$$

is the subthreshold swing. The thermodynamic voltage U_T is given by

$$U_T \triangleq \frac{kT}{q}, \tag{2.6}$$

where k is the Bolzmann constant and q is the elementary charge. Its value is 25.8 mV at 300 K.

2.2 Drain-Current-Variability-Model Derivation

In the current section, the detailed derivation of the proposed drain-current variability model is demonstrated. The fluctuation of the drain-current around its nominal value is considered to be a result of the sum of all local fluctuation

contributions along the channel. The transistor channel is divided into a noisy

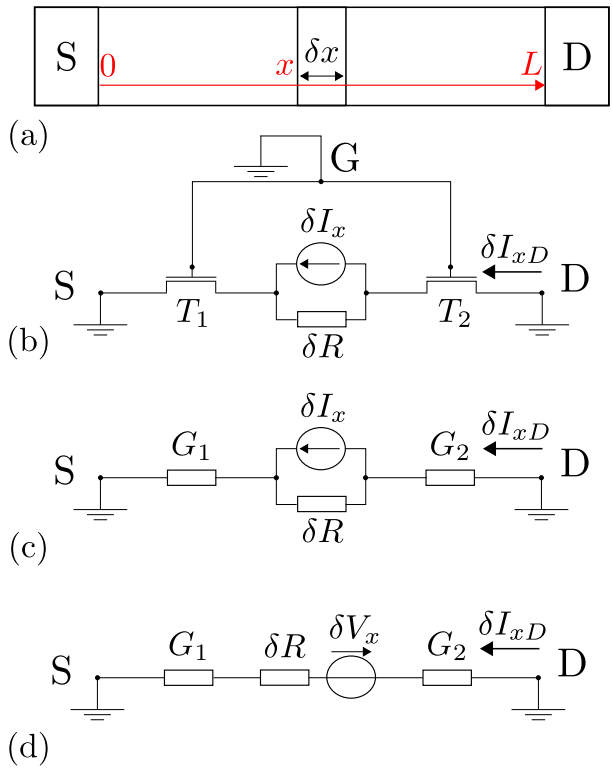

Figure 2.3.: Transistor channel divided into a noisy element between positions x and $x + \delta x$, accounting for the local current fluctuation δI_x, and two noiseless transistors T1 and T2.

element between positions x and $x + \delta x$ and two noiseless pseudo-transistors T_1 and T_2 (Fig. 5.1) of channel lengths x and $L - x$, respectively. The local drain-current fluctuation is modeled as a current source δI_x connected in parallel to the resistance δR of the channel element. The term δI_x is considered to be a zero-mean stationary process on x. The equivalent small-signal circuits of transistors T1 and T2 can be reduced to the conductances G_1 and G_2 [39]. Alternatively, as shown in Fig. 5.1(d), a Thevenin equivalent noise voltage source can be used ($\delta V_x = \delta R\, \delta I_x$) and by applying Kirchhoff's voltage law from Drain to Source nodes, the following can be obtained:

$$\delta I_{xD}/G_1 - \delta V_x + I_{xD}\delta R + \delta I_{xD}/G_2 = 0 \Leftrightarrow$$
$$\delta I_{xD}\left(\frac{1}{G_1} + \frac{1}{G_2} + \delta R\right) = \delta V_x \Leftrightarrow$$
$$\delta I_{xD}\left(\frac{1}{G_1} + \frac{1}{G_2}\right) = \delta V_x = \delta R\,\delta I_x \Leftrightarrow$$

$$\delta I_{xD} = G_{CH}\,\delta R\,\delta I_x, \tag{2.7}$$

where

$$\frac{1}{G_{CH}} = \frac{1}{G_{CH}(x)} = \frac{1}{G1(x)} + \frac{1}{G2(x)}. \tag{2.8}$$

Furthermore, conductance at any point of the channel and resistance δR, assuming constant mobility, can be expressed as

$$G_{CH} = \frac{dI_D}{dV} = \mu\,\frac{W}{L}\,(-Q_{CH}) \tag{2.9}$$

and

$$\delta R = \frac{\delta V}{I_D} = \frac{\delta x}{W\mu(-Q_{CH})} \tag{2.10}$$

respectively. By substituting (2.9) and (2.10) into (2.7) the following can be obtained:

$$\delta I_{xD} = \frac{\delta x}{L}\delta I_x. \tag{2.11}$$

Considering again the elementary section of the channel between x and $x + \delta x$, the current at position x is given by

$$I_D = WqN(x)\mu\frac{dV}{dx}, \tag{2.12}$$

where $N(x) = Q_{CH}(x)/q$ is the number of charge carriers per unit area. Following [40], if a certain number of carriers get trapped at position x of the channel, the relative local current fluctuation can be described as

$$\frac{\delta I_x}{I_D} = \frac{\delta I_D(x)}{I_D} = \frac{\delta Q_{CH}}{Q_{CH}} + \frac{\delta\beta}{\beta}, \tag{2.13}$$

where the term $\delta\beta/\beta$ describes the effect of charge trapping or edge effects [19] on $\beta = \mu C'_{ox}\frac{W}{L}$. Attributing all variations to charge trapping and following [40], based on Matthiessen's rule, the carrier mobility including the effect of the trapping mechanism can be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_0} + a_c Q_t \Leftrightarrow \mu = \frac{\mu_0}{1 + a_c Q_t \mu_0}, \tag{2.14}$$

where $Q_t = -qN_t$ is the density of trapped charges and $a_c = \tilde{a_c}/q$ is the Coulomb scattering coefficient [41]. Using (2.14), the following can be obtained:

$$\frac{\delta\beta}{\delta Q_t} = \frac{\delta\left(\mu C'_{ox}\frac{W}{L}\right)}{\delta Q_t} = -\frac{a_c\mu_0^2 C'_{ox}\frac{W}{L}}{(1 + a_c Q_t \mu_0)^2} \Leftrightarrow$$

$$\frac{\delta\beta}{\delta Q_t} = -a_c\mu^2 C'_{ox}\frac{W}{L} = -a_c\mu\beta \tag{2.15}$$

and the relative current fluctuation can be expressed as

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{Q_{CH}}\frac{\delta Q_{CH}}{\delta Q_t} + \frac{1}{\beta}\frac{\delta\beta}{\delta Q_t}\right)\delta Q_t = \left(\frac{1}{Q_{CH}}\frac{\delta Q_{CH}}{\delta Q_t} - a_c\mu\right)\delta Q_t, \tag{2.16}$$

where δQ_t is the local charge fluctuation related to the fluctuation in the trap density.

Considering that the variation δQ_t will cause a surface-potential variation $\delta\psi_s$, the number of charges depending directly on ψ_s will also change. Consequently, the charge-conservation principle yields

$$-\delta Q_t = \delta Q_g + \delta Q_{CH}, \tag{2.17}$$

where δQ_g and δQ_{CH} are the induced fluctuations of charges on the gate electrode and of mobile charges in the channel, respectively. Furthermore, δQ_g and δQ_{CH} are related to the surface-potential variation $\delta\psi_s$ according to [42]

$$\delta Q_g = -C'_{ox}\delta\psi_s, \;\; \delta Q_{CH} = -C_{CH}\delta\psi_s, \tag{2.18}$$

where C_{CH} is the channel-charge capacitance. Recalling that C_{CH} can be

approximated by

$$C_{CH} \simeq -Q_{CH}/U_T, \tag{2.19}$$

and combining (2.17) and (2.18), the following can be obtained [42]:

$$\frac{\delta Q_{CH}}{\delta Q_t} = \frac{C_{CH}}{C_{CH} + C'_{ox}}. \tag{2.20}$$

Using (2.19), equation (2.20) can be transformed into

$$\frac{\delta Q_{CH}}{\delta Q_t} \simeq \frac{Q_{CH}}{Q_{CH} + Q^*/a} = \frac{q_{ch}}{q_{ch} + 1/a}. \tag{2.21}$$

For simplicity reasons, similarly as in some of the widely-used commercial compact-models (i.e. BSIM-BULK, EKV) [9, 41], charges and voltages are normalized according to

$$\frac{Q_{CH}}{q_{ch}} = \frac{Q_D}{q_d} = \frac{Q_S}{q_s} = Q^* \tag{2.22}$$

and

$$\frac{V_{CH}}{v_{ch}} = \frac{V_D}{v_d} = \frac{V_S}{v_s} = aU_T \tag{2.23}$$

respectively, where

$$Q^* \triangleq aU_T C'_{ox}. \tag{2.24}$$

The terms q_s and q_d account for the normalized charge densities at the source and drain end of the channel, respectively. By substituting (2.21) into (2.16), the relative local current fluctuation can be rewritten as

$$\begin{aligned} \frac{\delta I_D(x)}{I_D} &= \left(\frac{1}{Q_{CH}} \frac{q_{ch}}{q_{ch} + 1/a} - a_c\mu \right) \delta Q_t \Leftrightarrow \\ \frac{\delta I_D(x)}{I_D} &= \left(\frac{1}{q_{ch}Q^*} \frac{q_{ch}}{q_{ch} + 1/a} + \frac{a^*}{Q^*}\mu \right) \delta Q_t \Leftrightarrow \\ \frac{\delta I_D(x)}{I_D} &= \left(\frac{1}{q_{ch} + 1/a} + a^*\mu \right) \frac{\delta Q_t}{Q^*}, \end{aligned} \tag{2.25}$$

where $a^* = a_c(-Q^*)$ is a parameter related to the Coulomb scattering coefficient given in units of Vs/m^2.

Using (2.11), the mean square of the total drain-current fluctuation can be expressed as [39]

$$\sigma^2 I_D = \overline{\delta I_D^2} = \sum_L \overline{\delta I_{xD}^2} = \lim_{\delta x \to 0} \sum \overline{\left(\frac{\delta x}{L} \delta I_x\right)^2} = \frac{1}{L^2} \int_0^L \delta x \overline{\delta I_D^2(x)} dx. \tag{2.26}$$

Furthermore, from (5.10), the relative local drain-current fluctuation normalized to the square of the drain current can be expressed as

$$\frac{\delta I_D^2(x)}{I_D^2} = \left(\frac{1}{q_{ch} + 1/a} + a^* \mu\right)^2 \frac{\delta Q_t^2}{Q^{*2}}. \tag{2.27}$$

Following [39], the square of the standard deviation of the local fluctuations of the trap density, assuming a Poisson distribution, is given by

$$\sigma^2(\delta Q_t) = q^2 N_t / W \delta x, \tag{2.28}$$

where N_t, given in units of m^{-2}, is the density of traps in which charge carriers may be accumulated and which will be treated as a fitting parameter. Combining (2.26), (2.27) and (2.28), the variance of the total normalized drain-current fluctuation can be expressed as

$$\frac{\sigma^2 I_D}{I_D^2} = \frac{\overline{\delta I_D^2}}{I_D^2} = \frac{1}{L^2} \int_0^L \delta x \left(\frac{1}{q_{ch} + 1/a} + a^* \mu\right)^2 \frac{\sigma^2(\delta Q_t)}{Q_{sp}^2} dx \Leftrightarrow$$

$$\frac{\sigma^2 I_D}{I_D^2} = \frac{1}{L^2} \int_0^L \left(\frac{1}{q_{ch} + 1/a} + a^* \mu\right)^2 \frac{q^2 N_t}{W} \frac{1}{Q_{sp}^2} dx \Leftrightarrow$$

$$\frac{\sigma^2 I_D}{I_D^2} = \frac{q^4 N_t}{W L^2 a^2 (kT)^2 C_{ox}'^2} \int_0^L \left(\frac{1}{q_{ch} + 1/a} + a^* \mu\right)^2 dx, \tag{2.29}$$

or

$$\frac{\sigma^2 I_D}{I_D^2} = C^*|_{\Delta N} \, B^*(q_{ch})|_{\Delta N}, \tag{2.30}$$

where

$$C^*|_{\Delta N} = \frac{q^4 N_t}{WL^2 a^2 (kT)^2 C_{ox}'^2} \tag{2.31}$$

and

$$B^*(q_s, q_d)|_{\Delta N} = \int_0^L \left(\frac{1}{q_{ch} + 1/a} + a^* \mu \right)^2 dx. \tag{2.32}$$

Term $B^*(q_s, q_d)$ can be then rearranged as follows

$$B^*(q_s, q_d)|_{\Delta N} = L \int_0^1 \left(\frac{1}{q_{ch} + 1/a} + a^* \mu \right)^2 d\omega \Leftrightarrow$$

$$B^*(q_s, q_d)|_{\Delta N} = L \frac{1}{i_d} \int_{q_d}^{q_s} \left(\frac{1}{q_{ch} + 1/a} + a^* \mu \right)^2 (1 + q_{ch})\, dq_{ch} \Leftrightarrow$$

$$B^*(q_s, q_d)|_{\Delta N} = L \frac{1}{i_d} \left(\frac{2(a-1)a^* \mu}{a} + 1 \right) ln \left(\frac{1 + aq_s}{1 + aq_d} \right) +$$

$$+ \frac{1}{i_d} \left(\frac{1-a}{1+aq_s} - \frac{1-a}{1+aq_d} \right) + (a^* \mu)^2 + \frac{1}{i_d} 2(a^* \mu)(q_s - q_d), \tag{2.33}$$

where $\omega = x/L$ is the normalized position x along the channel. Finally, using (2.31) and (2.33), the square of the standard deviation of the total drain current fluctuation is given by

$$\frac{\sigma^2 I_D}{I_D^2} = C^*|_{\Delta N}\, B^*(q_{ch})|_{\Delta N} \tag{2.34}$$

where

$$C^*|_{\Delta N} = \frac{q^4 N_t}{WLa^2 (kT)^2 C_{ox}'^2} \tag{2.35}$$

and

$$B^*(q_s, q_d)|_{\Delta N} = \frac{1}{i_d} \left(\frac{2(a-1)a^* \mu}{a} + 1 \right) ln \left(\frac{1 + aq_s}{1 + aq_d} \right) +$$

$$+ \frac{1}{i_d} \left(\frac{1-a}{1+aq_s} - \frac{1-a}{1+aq_d} \right) + (a^* \mu)^2 + \frac{1}{i_d} 2(a^* \mu)(q_s - q_d). \tag{2.36}$$

The normalized drain current i_d can be expressed as $i_d = I_D/\mu(aU_T)^2C'_{ox}W/L$. Alternatively, excluding the channel length modulation effect and assuming ideal subthreshold slope ($a = 1$), i_d can be approximated by the following equation:

$$i_d = (q_s - q_d)(1 + \frac{1}{2}q_s + \frac{1}{2}q_d). \tag{2.37}$$

In Fig. 2.4, the bias dependent factor $B^*(q_s, q_d)|_{\Delta N}$ is plotted as a function

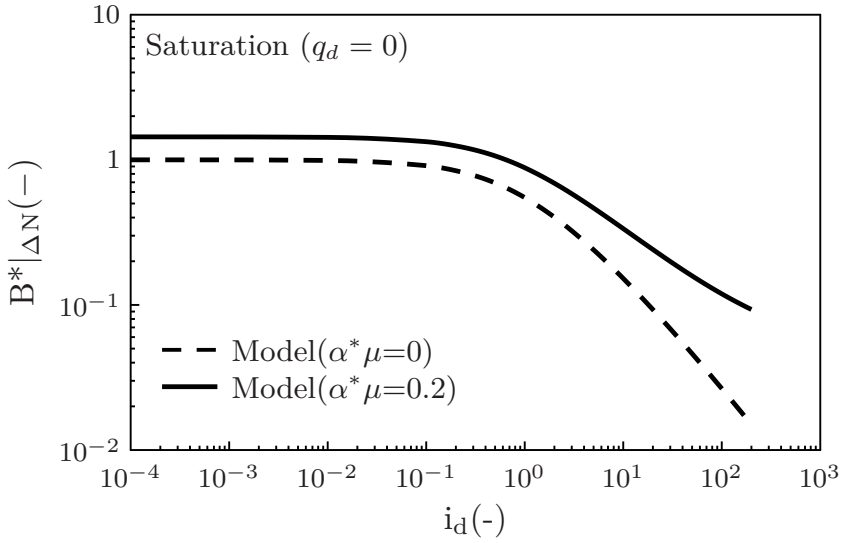

Figure 2.4.: Variability-model bias-dependent factor $B^*(q_s, q_d)|_{\Delta N}$ versus normalized drain current i_d in saturation ($q_d = 0$).

of the normalized drain current i_d, for two different values of the product $a^*\mu$, in saturation ($q_d = 0$). The impact of the parameter a^* is greatly reduced for gate-source voltages approaching the subthreshold region. Note that neither the current-voltage model nor the proposed variability model cover the off-state regime (leakage current region) below the turn-on (switch-on) voltage, i.e., the range of gate-source voltages between 0 and $-0.5\,\mathrm{V}$.

2.3 Parameter Extraction Procedure

In the current section, the parameter extraction procedure of the drain-current variability model is described. In Fig. 2.5, the normalized drain-current variance

$\sigma^2 I_{DS}/I_{DS}^2$ of the coplanar DPh-DNTT TFTs having channel length (L) of 5 µm is plotted as a function of the mean-value drain current $E[I_{DS}]$. The values of the parameters N_t and a^* were extracted as follows. In the first step, the parameter a^* was set to zero. In the subthreshold region, (i.e., above the leakage-current regime), a specific gate-source voltage was selected (i.e. $V_{GS} = -0.7\,\mathrm{V}$), and N_t at this gate-source voltage was calculated. In the second step, using the extracted value of N_t, the parameter a^* was calculated at the maximum gate-source voltage, in our case $V_{GS} = -3.0\,\mathrm{V}$. Note that the two selected gate-source voltages, (subthreshold region and maximum $|V_{GS}|$) correspond to specific experimental values of $\sigma^2 I_{DS}/I_{DS}^2$ that define the subthreshold and maximum-$|V_{GS}|$ asymptotes that are depicted in Fig. Fig. 2.5 as red dashed lines.

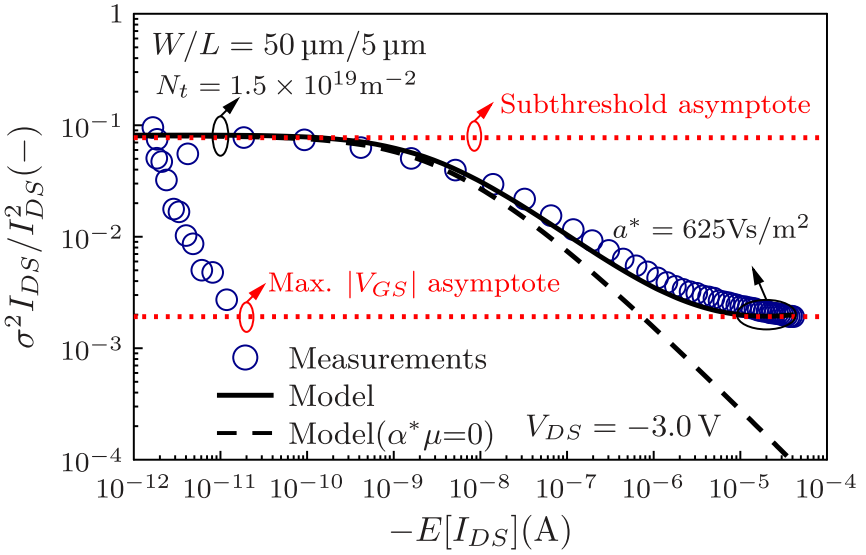

Figure 2.5.: Normalized drain-current variance $\sigma^2 I_{DS}/I_{DS}^2$ versus mean-value drain current $E[I_{DS}]$ of coplanar DPh-DNTT TFTs with $L = 5\,\mu\mathrm{m}$. Symbols: measurement data, black solid/dashed lines: model, red dashed lines: asymptotes.

2.4 Model Verification

Organic p-channel TFTs with channel lengths (L) of 2 µm, 3 µm and 5 µm and a channel-width-to-length ratio (W/L) of 10, were fabricated on a 125 µm-thick flexible polyethylene naphthalate (PEN) substrate in the inverted coplanar (bottom-gate, bottom-contact) device architecture, using stencil lithography based on high-resolution silicon stencil masks [43]. The TFTs consist of 25 nm-thick aluminum gate electrodes, a 5.3 nm-thick hybrid AlO_x/SAM gate dielectric, 30 nm-thick gold (Au) source and drain contacts coated with a pentafluorobenzenethiol (PFBT) monolayer and a 25 nm-thick vacuum-deposited layer of the small-molecule organic semiconductor DPh-DNTT [44]. The maximum process temperature was 90 °C. For each channel length, 16 nominally identical TFTs were fabricated and characterized. The measurement protocol comprises transfer characteristics at a drain-source voltage (V_{DS}) of −3.0 V and gate-source voltages (V_{GS}) from 0 to −3.0 V with a step size of −50 mV, recorded at room temperature. In order to verify the proposed model for TFTs fabricated in the staggered device architecture, experimental data from [45], for bottom-gate top-contact DNTT TFTs with dimensions of $W/L = 10\,\mu m/1\,\mu m$, are used. Fig. 2.6 shows the actual fabricated PEN substrate.

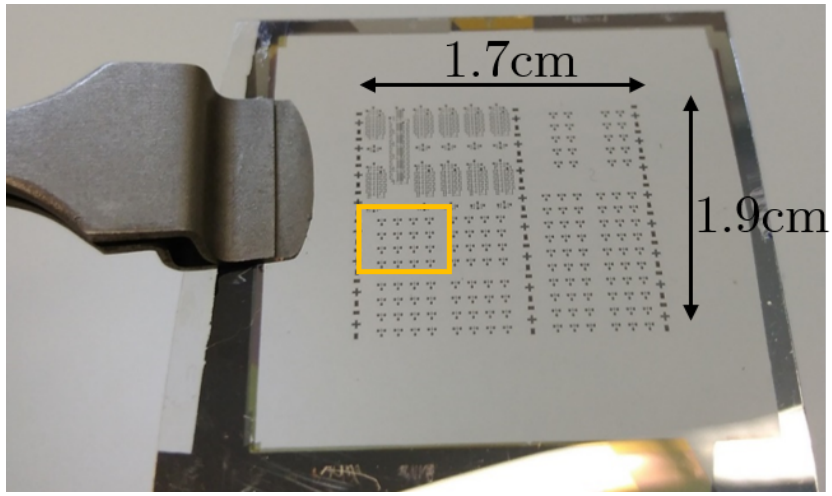

Figure 2.6.: Actual fabricated flexible PEN substrate.

Fig. 2.7 shows the mean-value transfer characteristics of DPh-DNTT TFTs fabricated in the coplanar device architecture, having channel lengths (L) of 2 µm,3 µm and 5 µm, for a drain-source voltage of −3.0 V. The experimental mean values were calculated over a population of 16 nominally identical TFTs fabricated on the same substrate. Symbols represent the measurement data and lines represent the results of the current-voltage model.

In 2.8(a) and (b), the normalized drain-current variance $\sigma^2 I_{DS}/I_{DS}^2$ of the coplanar DPh-DNTT TFTs is plotted as a function of the mean-value drain current $E[I_{DS}]$. To improve the agreement between model and experiment, the extraction of N_t and a^* was performed for each channel length individually as proposed in [39]. In Fig. 2.9, the standard deviation of the drain current normalized to the device area $\sigma(I_{DS}/WL)$ is plotted as a function of the gate-source voltage V_{GS} for the three different channel lengths.

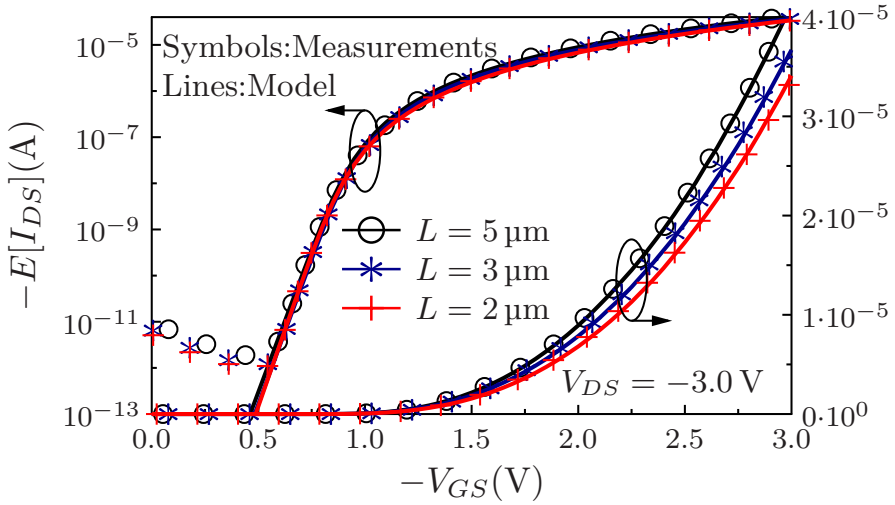

Figure 2.7.: Mean-value drain current $E[I_{DS}]$ versus gate-source voltage of coplanar DPh-DNTT TFTs with channel lengths (L) of 2 µm,3 µm and 5 µm. Symbols: measurement data, solid lines: model.

In Fig. 2.10, the normalized drain-current variance multiplied by the square-root of the device area $\sigma^2 I_{DS}/I_{DS}^2 \times \sqrt{WL}$ of the coplanar DPh-DNTT TFTs is plotted as a function of $1/\sqrt{WL}$. The dashed line is the result from the model calculated for $N_t = 6.9 \times 10^{18}\mathrm{m}^{-2}$ and $a^* = 750\mathrm{Vs/m}^2$. This set of parameters

was extracted by fitting the model to the experimental results obtained for each channel length. In this case, the model assumes the same value of N_t regardless of the channel length and predicts the number of traps ($N_t \times WL$) for each channel length, which yielded values of 1.73×10^9, 6.21×10^8 and 2.76×10^8 for the TFTs having channel lengths of 5 µm, 3 µm and 2 µm, respectively. Using the alternative approach in which a different set of parameters N_t and a^* was extracted for each channel length, the predicted numbers of traps are 3.75×10^9, 6.75×10^8 and 2.40×10^8 for channel lengths of 5 µm, 3 µm and 2 µm, respectively. Both approaches correctly predict that the number of traps increases approximately linearly with the TFT area [46].

In Fig. 2.11(a) and (b), the results obtained for the staggered DNTT TFTs having a channel length of 1 µm [45], are summarized. The values of the parameters N_t and a^* were extracted at gate-source voltages of -0.25 V (subthreshold region) and -2.0 V (maximum $|V_{GS}|$). The threshold voltage (V_{T0}) was found to be -0.33 V. Compared with the coplanar DPh-DNTT TFTs, the measured transfer characteristics of the DNTT TFTs.
show a larger off-state drain current (leakage) and a larger subthreshold swing, which prevent the formation of a clear plateau in the measured $\sigma^2 I_{DS}/I_{DS}^2$ curve.

Table 2.1 summarizes the values of N_t and a^* extracted from the variability model and the effective carrier mobilities of the coplanar DPh-DNTT TFTs and of the staggered DNTT TFTs for each channel length at the maximum gate-source and drain-source voltages. As can been seen, the value of a^* is significantly smaller for the coplanar DPh-DNTT TFTs than for the staggered DNTT TFTs. The reason is that the coplanar DPh-DNTT TFTs have a larger intrinsic channel mobility, a larger channel length and a smaller contact resistance than the staggered DNTT TFTs, all of which leads to a significantly larger effective carrier mobility [44], which in turn leads to a smaller value of a^*, in agreement with Equation 2.14. In addition, the parameter a^* also accounts for the drain-current variability caused by edge effects (Equation 2.13), and since these tend to be more pronounced in TFTs with a smaller area [19], the value of a^* is expected to increase with decreasing TFT area. The observation that the extracted effective carrier mobility of the DPh-DNTT TFTs decreases with decreasing channel length is consistent with the fact that the contribution of the contact resistance

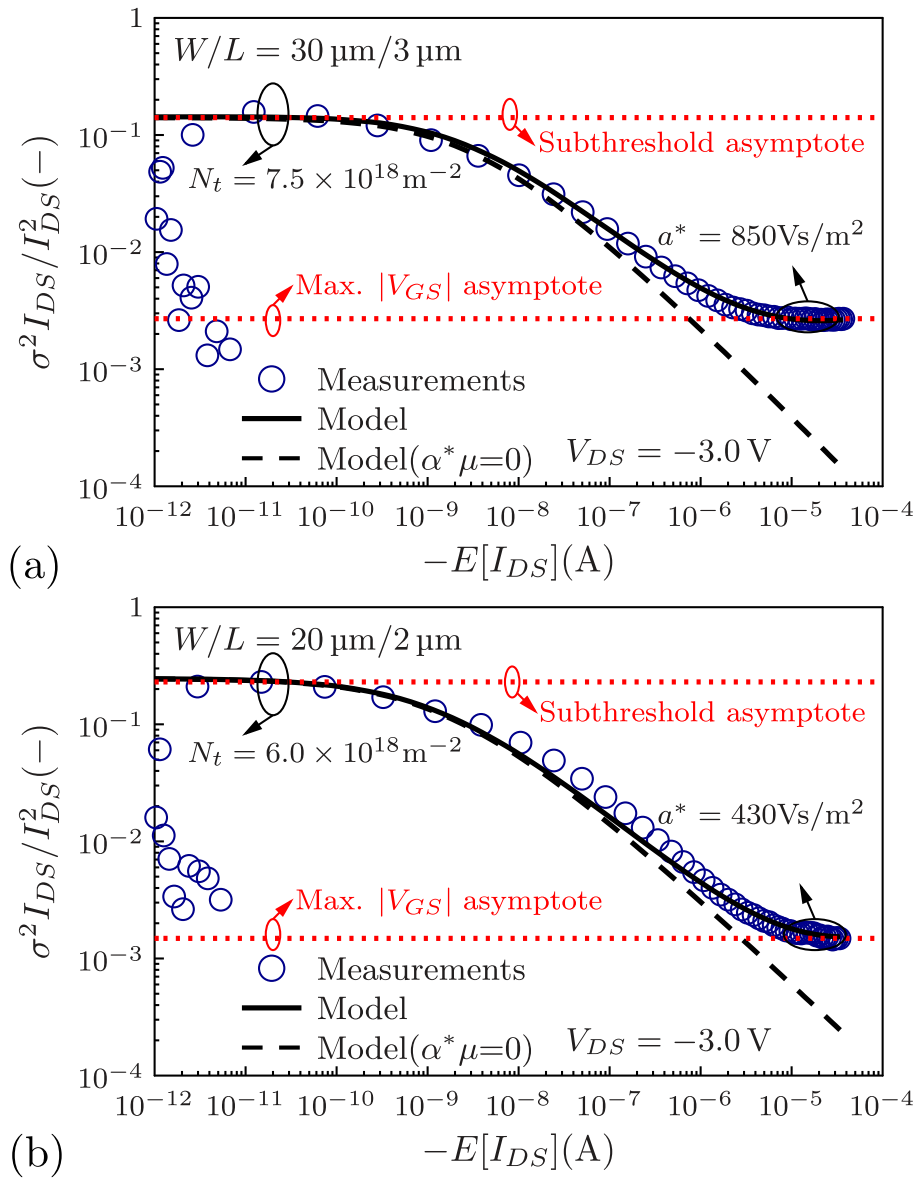

Figure 2.8.: Normalized drain-current variance $\sigma^2 I_{DS}/I_{DS}^2$ versus mean-value drain current $E[I_{DS}]$ of coplanar DPh-DNTT TFTs with (a) $L = 3\,\mu\text{m}$ and (b) $L = 2\,\mu\text{m}$. The experimental mean values were calculated over a population of 16 nominally identical TFTs. Symbols: measurement data, black solid/dashed lines: model, red dashed lines: asymptotes.

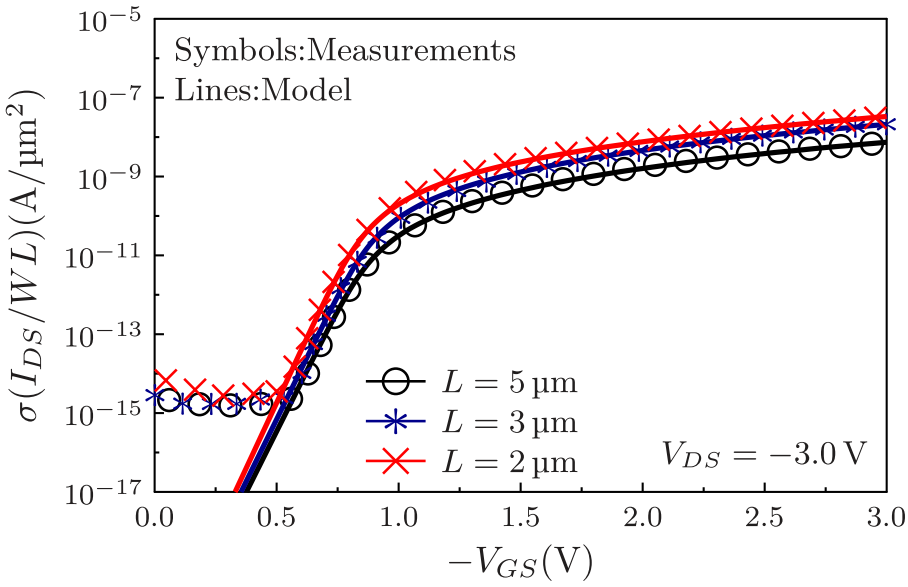

Figure 2.9.: Standard deviation of the drain current normalized to the device area $\sigma(I_{DS}/WL)$ versus gate-source voltage of the same TFTs. The experimental mean values were calculated over a population of 16 nominally identical TFTs. Symbols: measurement data, black solid/dashed lines: model

to the total device resistance increases with decreasing channel length [44]. The trap densities predicted by our model are smaller by three to four orders of magnitude than the trap density predicted in [19] for staggered DNTT TFTs with a channel length of 30 µm and a channel width of 100 µm ($6.8 \times 10^{21} m^{-2}$), but larger by about two orders of magnitude than the trap densities reported in [46] for devices based on DNTT and DPh-DNTT ($10^{16} m^{-2}$).

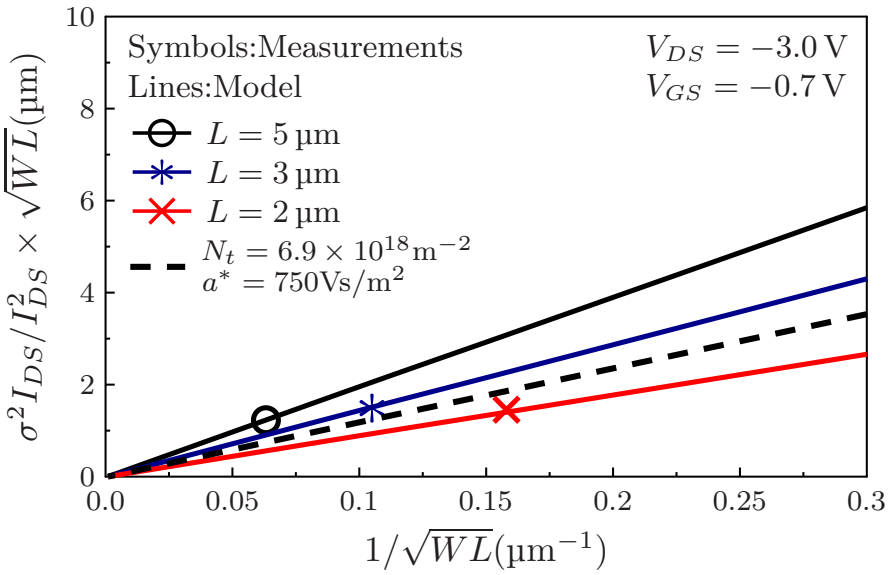

Figure 2.10.: Normalized drain-current variance multiplied by the square-root of the device area $\sigma^2 I_{DS}/I_{DS}^2 \times \sqrt{WL}$ versus $1/\sqrt{WL}$ of coplanar DPh-DNTT TFTs. Symbols: measurement data, solid lines: model (different set of parameters extracted per geometry), dashed line: model (one set of parameters extracted after simultaneously fitting the model to the three different geometries).

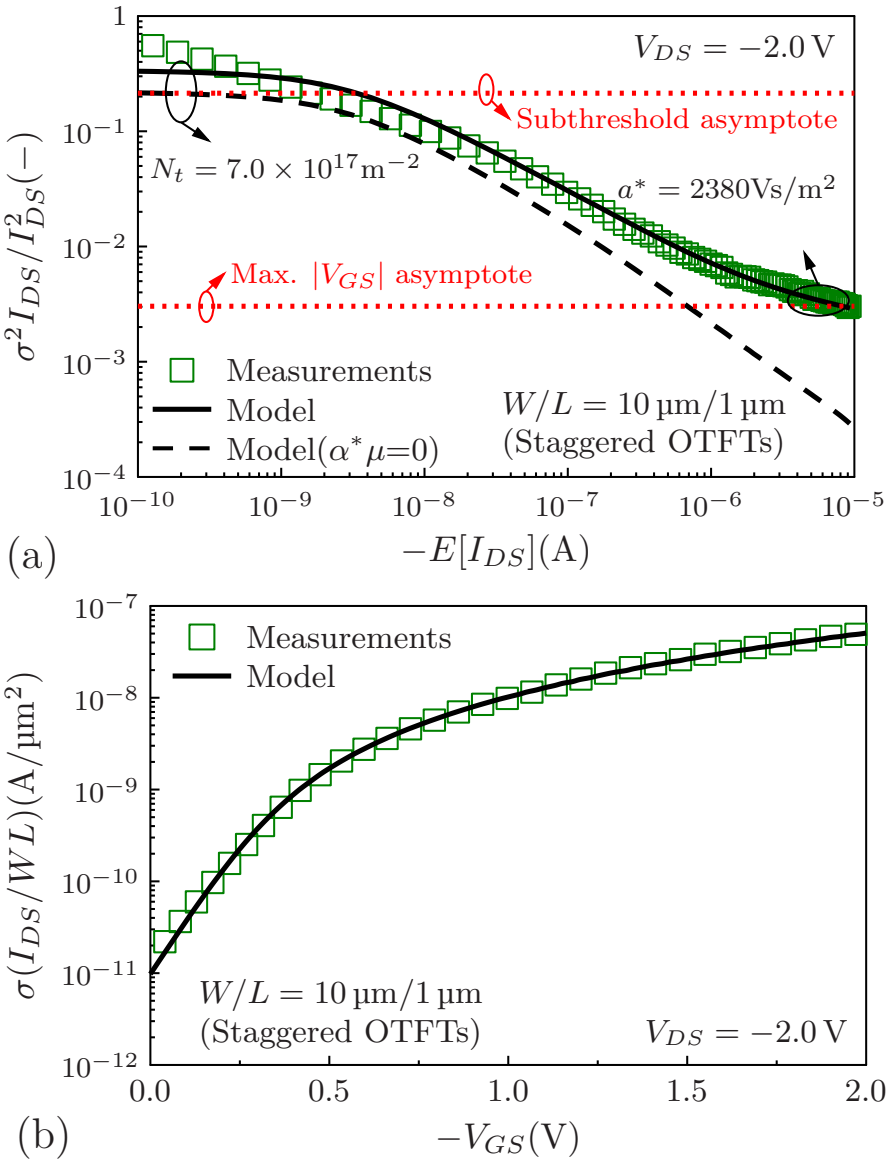

Figure 2.11.: (a) Normalized drain-current variance $\sigma^2 I_{DS}/I_{DS}^2$ versus mean-value drain current $E[I_{DS}]$ of staggered DNTT TFTs with $L = 1\,\mu\mathrm{m}$. (b) Standard deviation of the drain current normalized to the device area $\sigma(I_{DS}/WL)$ versus gate-source voltage of the same TFTs. Symbols: measurement data, black solid/dashed lines: model, red dashed lines: asymptotes.

2.5 Conclusions

In conclusion, we have developed a physical charge-based drain-current variability model suitable for organic thin-film transistors. The proposed model is based on charge-carrier-number-fluctuation and correlated-mobility-fluctuation effects and can be applied to TFTs fabricated in the coplanar or the staggered device architecture. We have shown that the drain-current variability decreases with increasing TFT area (product of channel length and channel width), particularly in the subthreshold region. We also found that the mobility-fluctuation effect is less pronounced in coplanar DPh-DNTT TFTs than in staggered DNTT TFTs and that the value of the parameter a^* tends to increase with decreasing channel length, due to the fact that a smaller channel length causes a smaller effective carrier mobility and more pronounced edge effects. Regardless of the channel dimensions and the device architecture, the results of the proposed model are in good agreement with the experimentally measured bias-dependent drain-current variability of organic TFTs.

Table 2.1.: Extracted parameters of the variability model

	N_t (m^{-2})	a^* ($\mathrm{Vs/m}^2$)	μ_{eff} ($\mathrm{cm}^2/\mathrm{Vs}$)
$L = 5\,\mu\mathrm{m}$	1.5×10^{19}	625	3.3
$L = 3\,\mu\mathrm{m}$	7.5×10^{18}	850	3.0
$L = 2\,\mu\mathrm{m}$	6.0×10^{18}	430	2.7
$L = 1\,\mu\mathrm{m}$	7.0×10^{17}	2380	1.4

UNIVERSITAT ROVIRA I VIRGILI
COMPACT MODELING OF VARIABILITY IN ORGANIC THIN-FILM TRANSISTORS
Aristeidis Nikolaou

CHAPTER 3

Noise-Based Simulation Technique for Circuit-Variability Analysis

3.1 Introduction

In the current section, a Monte Carlo (MC) simulation [23] alternative, a noise-based simulation technique initially introduced in [20] with the name "Noise Based Variability Approach" (NOVA) is presented here. The proposed method is suitable for use in commercial electronic device automation (EDA) software tools and is expected to accelerate the process of circuit simulation during the application of statistical parameter variation on the utilized model card, in the current case a model-card based on a Verilog-A organic TFT model.

Organic thin-film transistors (TFTs) are field-effect transistors in which the semiconductor is a thin, usually polycrystalline layer of conjugated organic molecules [1]. Organic TFTs are typically processed at temperatures below 100 °C [47] and can therefore be useful for a variety of large-area flexible electronics applications [48]. The statistical analysis of organic TFT-based circuits is typically performed using either Monte Carlo simulations (similar to those developed for silicon-CMOS circuits) [18] or novel physics-based variability compact models (which were developed to accurately describe the drain-current variability in organic TFTs) [15]. Here, the proposed NOVA method [20] is validated for a number of organic-TFT-based circuit topologies.

The context of this Chapter is organized as follows: Section 3.2 describes the

technology of the organic-TFTs used for verification. Section 3.3 summarizes the compact model used for the simulations. In Section 3.4 the typical Monte Carlo analysis performed using Cadence Virtuoso ADE and Spectre simulator framework [49] is presented. The proposed NOVA method is analytically explained in Section 3.5. Section 3.6 includes the results of the current analysis. In Section 3.7 conclusions are drawn.

3.2 Devices and Measurements

The experimental population comprises 16 nominally identical p-channel organic TFTs having a nominal channel length (L) of 1 µm and a nominal channel width (W) of 10 µm. The TFTs were fabricated on a flexible polyethylene naphthalate (PEN) substrate with a thickness of 125 µm in the inverted staggered (bottom-gate, top-contact) device architecture, using stencil lithography based on high-resolution silicon stencil masks (Fig. A.1) [45]. The TFTs consist of 20-nm-thick aluminum gate electrodes, a 5.3-nm-thick hybrid AlO_x/SAM gate dielectric, 20-nm-thick gold (Au) source and drain contacts and a 20-nm-thick vacuum-deposited layer of the small-molecule semiconductor 2,9-didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (C_{10}-DNTT). The maximum process temperature was 90 °C. The transfer characteristics of all TFTs were recorded at room temperature by applying a drain-source voltage (V_{DS}) of −2.0 V and sweeping the gate-source voltage (V_{GS}) from 0 to −2.0 V with a step size of −25 mV.

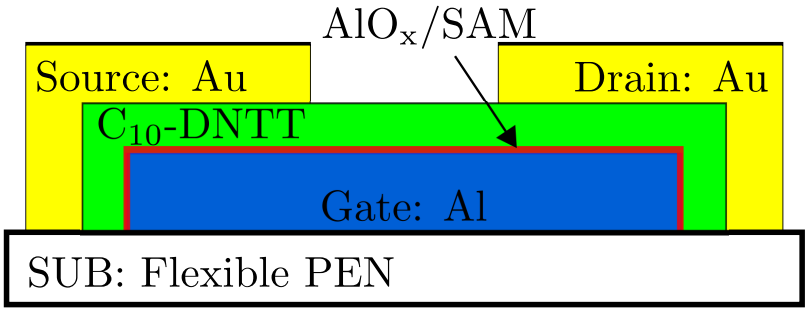

Figure 3.1.: Schematic cross-section of the organic TFTs fabricated in the inverted staggered (bottom-gate, top-contact) architecture [45].

3.3 Compact Modeling

In this section, the core of the simulation, namely the application of a compact model to the measured current-voltage characteristics, will be described. The charge-based organic-TFT model previously presented in Section 2.1 [11] will be used as the basis.

Table 3.1.: Parameter variations of the extracted model cards

	μ model	$\mu - \sigma$ model	$\mu + \sigma$ model	variation $\times\%$
$vt0$	$-333\,\mathrm{mV}$	$-363\,\mathrm{mV}$	$-304\,\mathrm{mV}$	$\simeq \pm 8.7\%$
lch	$1\,\mu\mathrm{m}$	$1.023\,\mu\mathrm{m}$	$0.975\,\mu\mathrm{m}$	$\simeq \pm 2.5\%$

The process of extracting the variability-aware parameter set using the compact model is described in the following. First, the mean-value μ and the corner-value $\mu \pm \sigma$ transfer characteristics were acquired from the experimental current-voltage curves by calculating the sample-mean $E[I_{DS}]$ and the sample-standard-deviation $\sigma(I_{DS})$ of the drain current I_{DS} at each gate-source voltage step. Next, one parameter set determining the mean-value model card was

Table 3.2.: Current variation of the extracted model cards

	μ model	$\mu \pm \sigma$ model variation $\times\%$
I_{vt0}	$-1.49 \times 10^{-8}\,\mathrm{A}$	$\simeq \pm 32\%$
I_{ON}	$-9.39 \times 10^{-6}\,\mathrm{A}$	$\simeq \pm 6\%$

produced by fitting the compact model to the measured mean-value transfer characteristic. For the derivation of the $\mu \pm \sigma$ parameter sets, the mean-value model card was used as the basis, and a subset of newly adjusted parameters was obtained from the $\mu \pm \sigma$ experimental transfer characteristics using the fitting procedure. Specifically, the values of the Verilog-A parameters $vt0$ and lch that correspond to the threshold-voltage (V_{TO}) and the channel-length (L) parameters of utilized drain-current compact model [11] (Section 2.1), respectively, where varied accordingly. The variability of the drain current in the subthreshold region can be attributed to the variation of the threshold voltage. In addition, the channel-length variation caused by edge effects [19] impacts the saturation current linearly in the above-threshold regime [23]. The parameters $vt0$ and lch

are considered to be statistically independent.

In Fig. 3.2(a), the experimental transfer characteristics of the 16 nominally identical p-channel C_{10}-DNTT TFTs are depicted as black lines. Fig. 3.2(b) shows the μ and $\mu \pm \sigma$ transfer characteristics of the same TFTs. Symbols denote the measurements, and lines correspond to the simulation results calculated from the three different model cards. Tables 3.1 and 3.2 summarize the values and variations of the parameters $vt0$ and lch and the drain-current variation of the extracted model cards, respectively. I_{vt0} and I_{ON} are the simulated drain currents at the threshold voltage and at the maximum gate-source voltage, respectively.

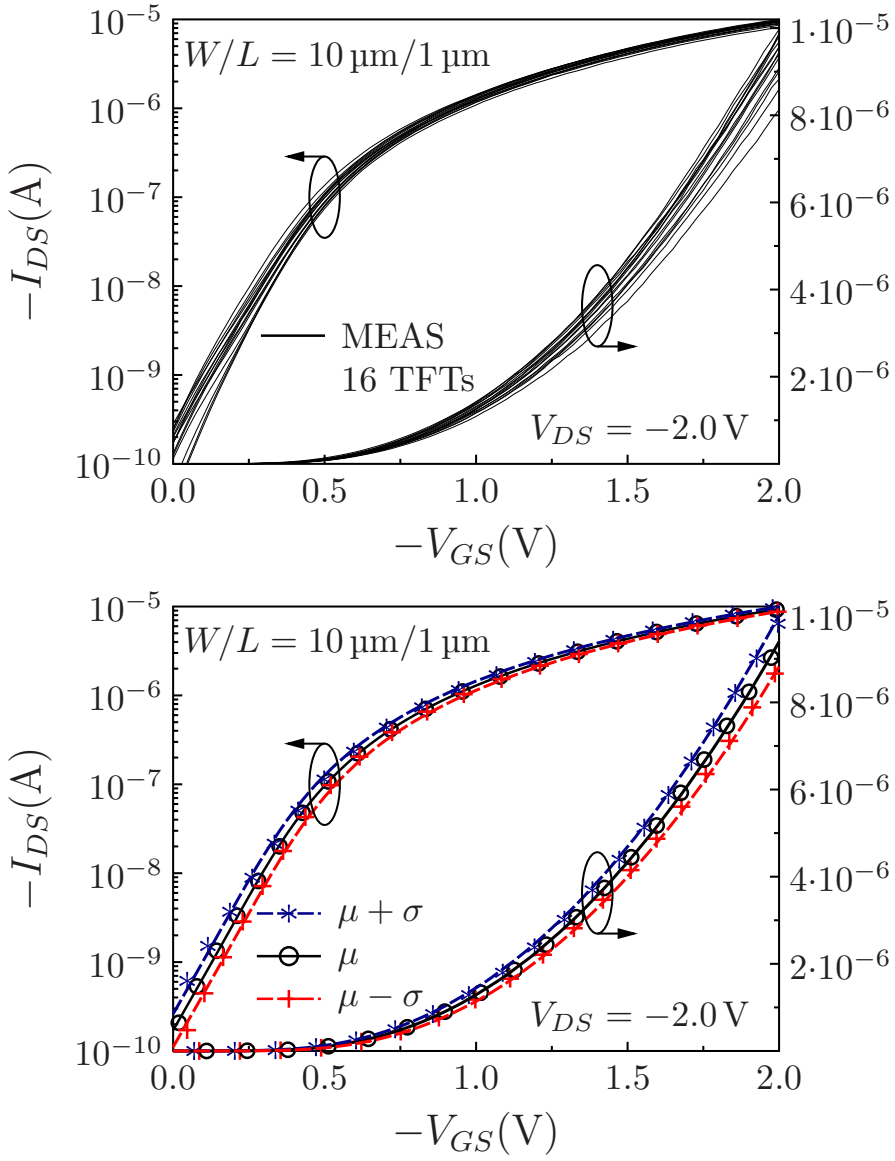

Figure 3.2.: (a) Measured transfer characteristics of the 16 nominally identical p-channel C_{10}-DNTT TFTs ($W = 10\,\mu m$, $L = 1\,\mu m$) in the saturation regime (black lines). (b) μ and $\mu \pm \sigma$ transfer characteristics of the same TFTs. Symbols: Values calculated from measurements. Lines: Simulation results calculated from the three different model cards.

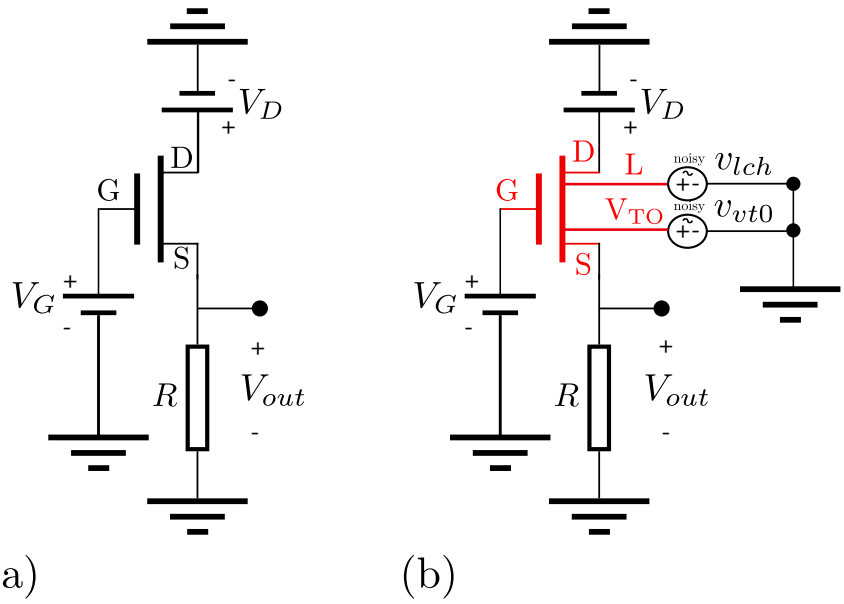

Figure 3.3.: (a) Schematic of a source follower comprising an instance of a Verilog-A three-terminal p-channel organic TFT, two DC voltage sources and an output resistor $R = 1\,\Omega$. (b) Same circuit topology as in (a) with the difference that the transistor instance is replaced by a five-terminal organic-TFT structure, with the two additional terminals connected to alternating "noisy" voltage sources in order to modify the Verilog-A parameters threshold voltage ($vt0$) and channel length (lch) according to the proposed NOVA method. All simulations are performed in Cadence Virtuoso ADE [49].

3.4 Typical Monte Carlo Analysis

The Monte Carlo analysis is a popular approach to determine the statistical distribution of the performance of integrated circuits. It consists of a sequential number of simulations in which for each iteration, the values of a parameter subset of a particular circuit component are randomly varied and the circuit is simulated accordingly. Subsequently, the statistical results are collected and the yield of the examined circuit is estimated. To achieve sufficient accuracy, the statistical Monte Carlo analysis of a circuit requires a sufficiently large number of iterations.

Fig. 3.3(a) shows the circuit schematic of a source follower designed for the Monte Carlo analysis to evaluate the impact of process variability on the experimental performance of the p-channel C_{10}-DNTT TFTs. This source follower consists of a three-terminal Verilog-A p-channel organic TFT, two DC voltage sources and a “dummy" resistor $R = 1\,\Omega$. The TFT instance is configured with the parameter values of the mean-value (μ) model card. The resistance of the resistor was chosen to create zero effect on the simulated values of the drain current I_{DS}. Fig. 3.4(a) shows the custom “.scs" library file that is used for the interaction between the simulator and the TFT instance during the Monte Carlo analysis. In the “process" section of the source code, the parameters that are of statistical interest are listed. For each parameter, the distribution type and the deviation with respect to its mean value are determined. Specifically, both parameters have a Gaussian distribution, and their standard deviations are assigned in percent. The numerical values of the simulation set-up are derived from the results listed on Table 3.1. It has to be mentioned that the actual parameters $vt0$ and lch of the Verilog-A TFT instance of the circuit are affected during the Monte Carlo iterations via the variation of the parameters $vt0\_stat$ and lch_stat, respectively (Fig. 3.4(b)).

Fig. 3.6(a) and (b) show the derived Gaussian-shaped histograms of the statistical variations of the Verilog-A parameters threshold voltage ($vt0$) and channel length (lch) after a Monte Carlo simulation with 5000 iterations. The estimated mean values ($E[vt0]$, $E[lch]$) and the standard deviations ($\sigma(vt0)$, $\sigma(lch)$) are included in Fig. 3.6(c) and (d), and they are in very good agreement

with the experimental results (Table 3.1).

```
simulator lang=spectre
parameters vt0_stat =-0.333
parameters lch_stat =1e-6
statistics {
process {
vary vt0_stat dist=gauss std=8.7 percent=yes
vary lch_stat dist=gauss std=2.5 percent=yes } }
```

(a)

```
(*cds_inherited_parameter*)parameter real vt0_stat=0;
(*cds_inherited_parameter*)parameter real lch_stat=0;
localparam real vt0_var=vt0_stat+vt0;
localparam real lch_var=lch_stat+lch;
```

(b)

Figure 3.4.: (a) Library ".scs" file and (b) Verilog-A part of the source code used for the Monte Carlo analysis.

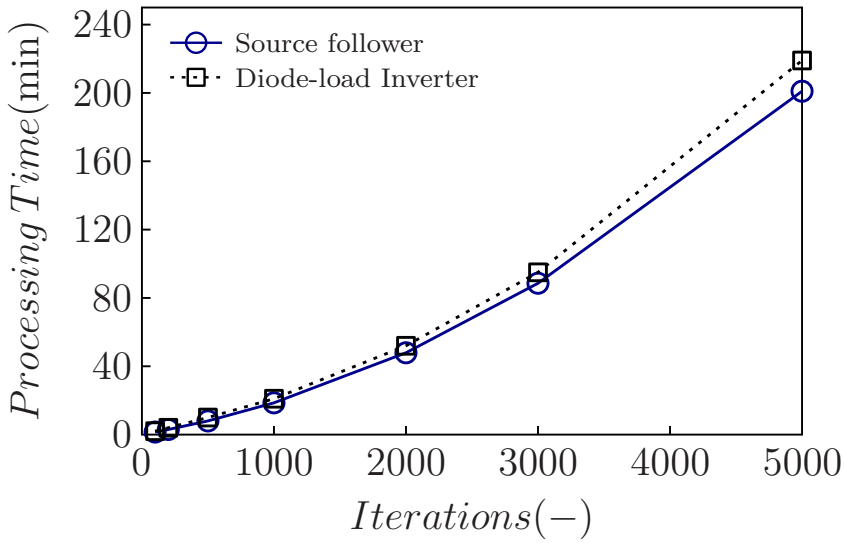

Figure 3.5.: Actual processing time of Monte Carlo simulation of the same parameters, for 100, 200, 500, 1000, 2000, 3000 and 5000 iterations.

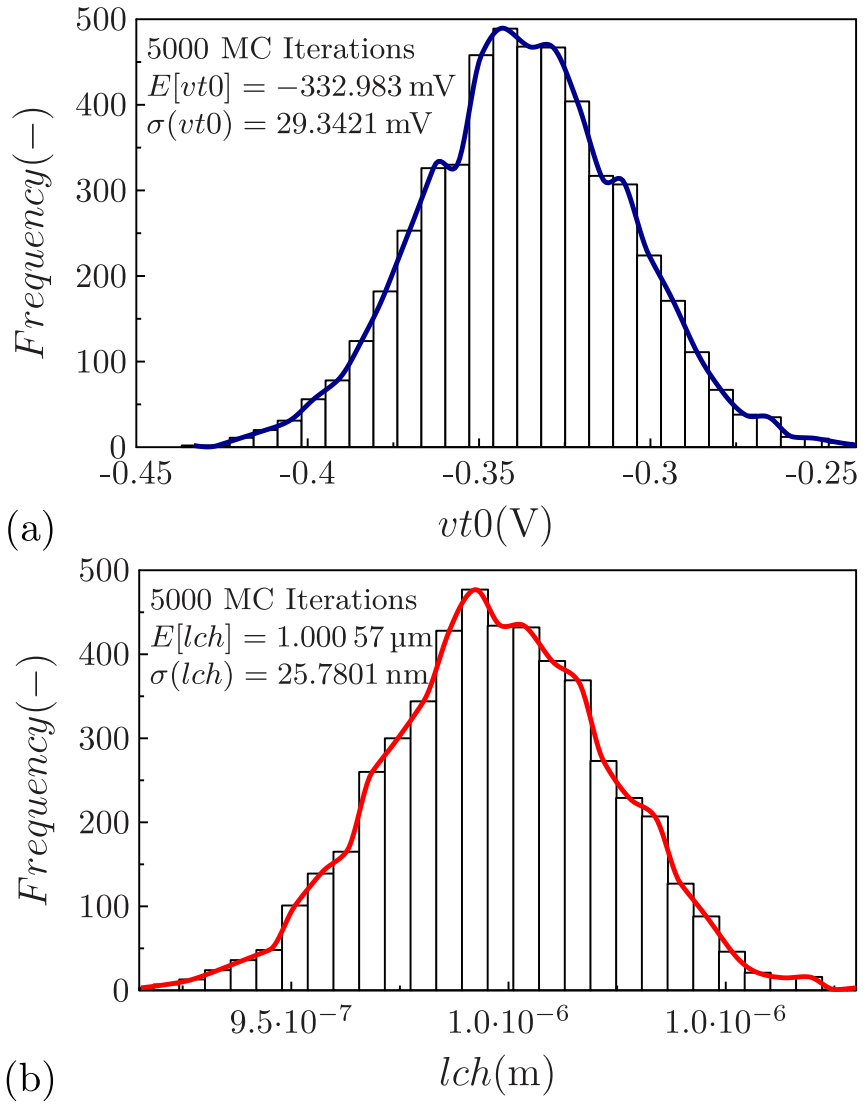

Figure 3.6.: Histograms of the statistical variations of the Verilog-A model parameters threshold voltage $vt0$ and channel length lch after a Monte Carlo simulation with 5000 iterations.

3.5 Noise-Based Variability Approach (NOVA)

In this section, an alternative to the Monte Carlo simulation method that is capable of fast DC statistical evaluation of integrated circuits will be discussed.

The proposed technique, namely "Noise-Based Variability Approach" (NOVA) [20], is based on noise-simulation principles and is validated here for organic-TFT-based circuit topologies, although it can be expanded to circuits based on silicon MOSFETs or inorganic TFTs. In simulator-based noise analyses, the input of the circuit is connected to ground and the spectra of all noise-contributing circuit components are added to calculate the output signal. The result corresponds to the variance of the output signal. In Cadence [49] simulators, similar to other EDA software tools, a "noisy" voltage source can be implemented in the form of an AC voltage source instance representing the desired mean-square value of noise. In this way, a thermal-noise Thèvenin equivalent circuit is implemented. The central-limit theorem indicates that thermal noise is Gaussian distributed with zero mean [50]. Furthermore, for Gaussian-distributed noise, the standard deviation σ is equal to the root-mean-square value of noise [51]. In Fig. 3.3(b),

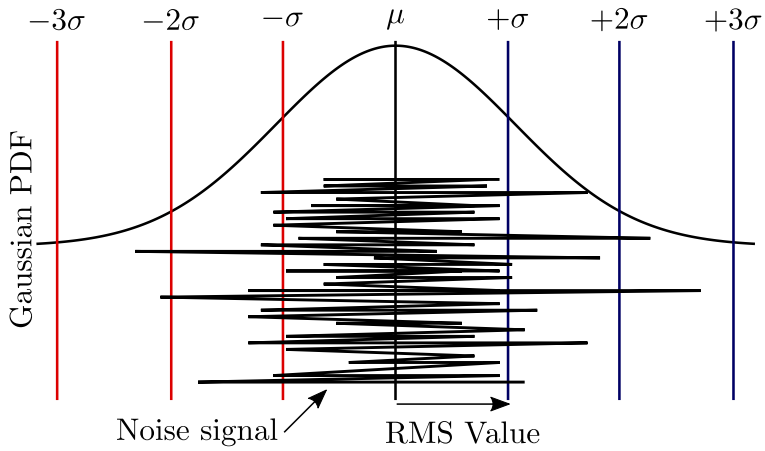

Figure 3.7.: For Gaussian distributed noise, standard deviation σ is equal to the root-mean-square (RMS) value of noise.

the schematic of the source follower used to evaluate the proposed NOVA method is depicted. The NOVA circuit topology is identical to the one that was used for the Monte Carlo analysis, with the difference that the transistor instance is replaced by a five-terminal organic-TFT structure. The two additional terminals are connected to alternating "noisy" voltage sources in order to modify the numerical values of the Verilog-A parameters threshold voltage ($vt0$) and channel length (lch). The setup of each additional voltage source is described next. The

DC voltage and the mean-square values of noise are configured to be equal to the mean value and the variance of the targeted Verilog-A parameter, respectively. The Verilog-A code of the TFT instance is updated accordingly. Note that the number of additional terminals depends on the number of Verilog-A parameters of statistical interest (i.e., two in our case). After the circuit has been properly configured, a parametric noise analysis with respect to the different gate-source voltage bias points is performed. The result corresponds to the variance of the output signal.

3.6 Results and Discussion

Fig. 3.8(a) shows the standard deviation of the output current $\sigma(-I_{DS})$ of the source follower (Fig. 3.3(a), (b)). The blue circles indicate the result derived from the measurements, the black line indicates the prediction from a Monte Carlo simulation with 5000 iterations, and the red crosses account for the standard deviation of the drain current estimated using the proposed NOVA method. Both simulation methods are able to coherently describe the circuit-bias-dependent process variability and predict the same trends with regard to the gate-source voltage; Fig. 3.8(b) shows that the deviation between the results from the two methods is approximately 10 % across the full range of gate-source voltages.

In Fig. 3.9, the use of the proposed NOVA method for the variability study of an organic-TFT-based diode-load inverter is presented. The circuit (Fig. 3.9(a)) consists of a drive TFT (T1) and a load TFT (T2) to implement the pull-up and pull-down functionalities, respectively. For simplicity, both TFTs are designed to have the same channel dimensions as the experimental TFTs ($W = 10\,\mu m$, $L = 1\,\mu m$). For circuits that consist of more than one transistor, the simulator permits both process and mismatch Monte Carlo statistical analyses. In order to extend this ability to the NOVA method, the NOVA mismatch analysis is performed using different noisy voltage sources for transistors T1 and T2 (Fig. 3.9(b)), while for the NOVA process-variations analysis, the same noisy voltage source was used for all TFTs (Fig. 3.9(c)). In both cases, the Verilog-A parameters $vt0$ and lch of the TFTs where statistically varied according to Table 3.1. Fig. 3.10(a) and (b) show the estimated standard deviation $\sigma(V_{out})$ of the

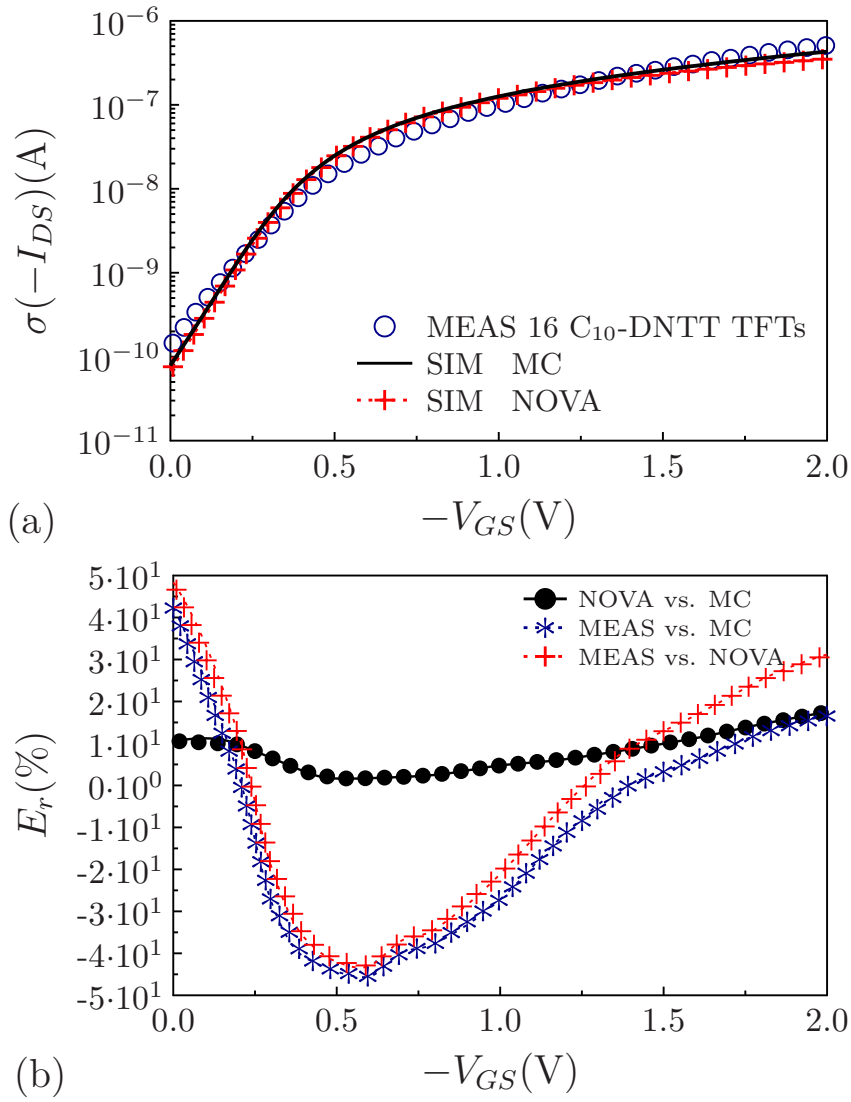

Figure 3.8.: (a) Standard deviation of the output current $\sigma(-I_{DS})$ of the source follower of Fig. 3.3 as a function of the gate-source voltage V_{GS}. Blue circles: Measurements. Black line: Monte Carlo simulation with 5000 iterations. Red crosses: Proposed method (NOVA). (b) Relative errors.

transfer characteristics for both the mismatch and the process analyses. In Fig. 3.11(a) and (b), the MC-versus-NOVA mean-value μ and corner-value $\mu \pm \sigma$ ($\mu \pm 3\sigma$ for process-variation-analysis) transfer characteristics are depicted. In

all cases, the NOVA method accurately predicts the results of a Monte Carlo simulation with 5000 iterations.

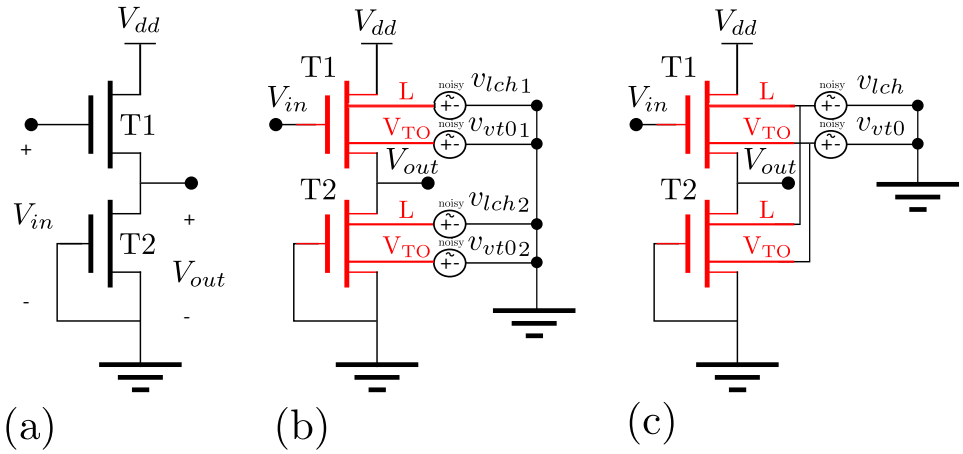

Figure 3.9.: (a) Schematic of a diode-load inverter used for Monte Carlo simulation. The topology is based on two identical p-channel TFTs ($W = 10\,\mu m$, $L = 1\,\mu m$) operated with a supply voltage $V_{dd} = 2.0\,V$. Schematics of the same circuit designed for (b) the NOVA mismatch and (c) the NOVA process-variation analyses.

A current mirror based on two identical p-channel TFTs ($W = 10\,\mu m$, $L = 10\,\mu m$) is depicted in Fig. 3.13(a). Both the reference TFT and the mirror TFT are connected to a load resistor ($R = 1\,\Omega$). In the basic DC simulation, the output voltage V_{out} was swept from zero to V_{dd}, and the output current I_{out} was recorded. Fig. 3.12(a) shows the standard deviation $\sigma(I_{out})$ of the output current, estimated after a NOVA-mismatch analysis (red crosses). The results are identical to those obtained using a Monte Carlo mismatch analysis with 5000 iterations (black line). The mean-value μ and the corner-value $\mu \pm \sigma$ output currents of the same circuit are shown in Fig. 3.12(b).

The processing times required for the Monte Carlo method and the proposed NOVA method are listed in Table 3.3. NOVA offers an improvement of almost 99 % compared to the typical Monte Carlo simulation.

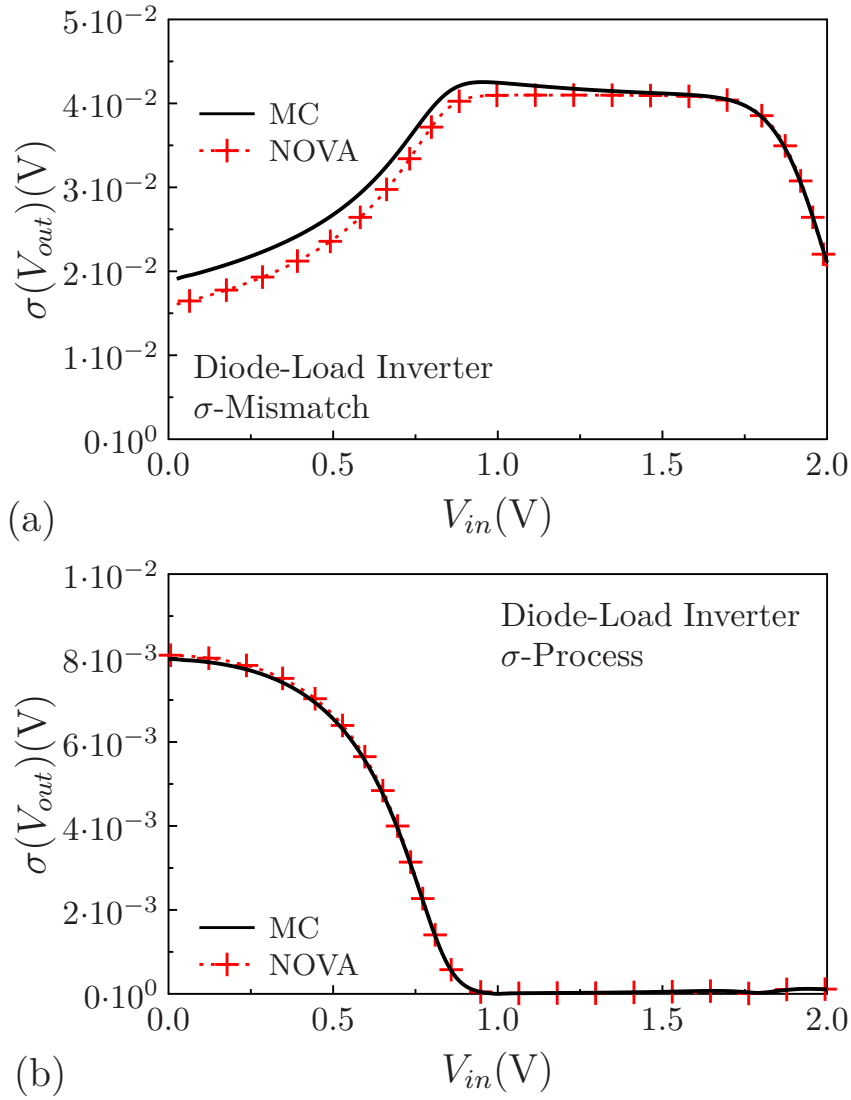

Figure 3.10.: Standard deviation of the output voltage $\sigma(V_{out})$ of the diode-load inverter of Fig. 3.9 as a function of the input voltage (V_{in}) for (a) mismatch and (b) process variations. Black line: Monte Carlo simulation with 5000 iterations. Red crosses: Proposed method (NOVA).

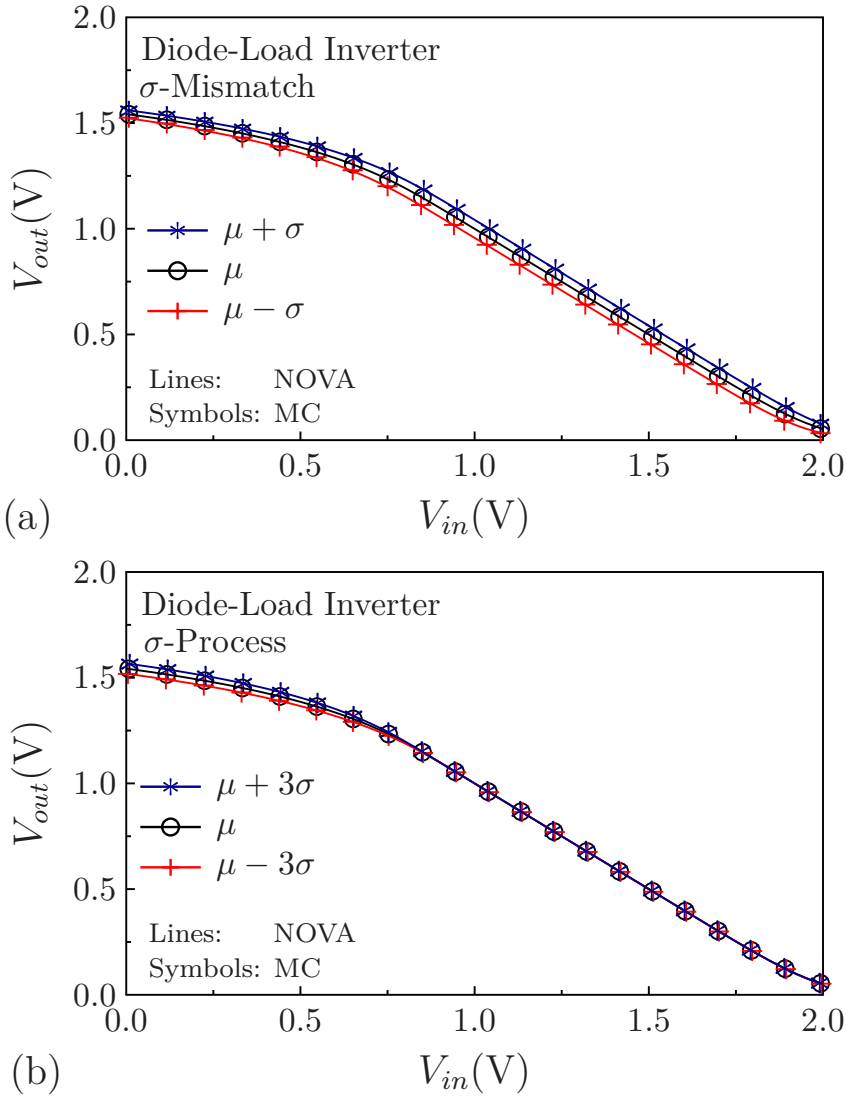

Figure 3.11.: Mean-value μ and corner-value $\mu \pm \sigma (\mu \pm 3\sigma)$ transfer characteristics of the diode-load inverter of Fig. 3.9 for (a) mismatch and (b) process variations. Symbols: Monte Carlo simulation with 5000 iterations. Lines: NOVA method.

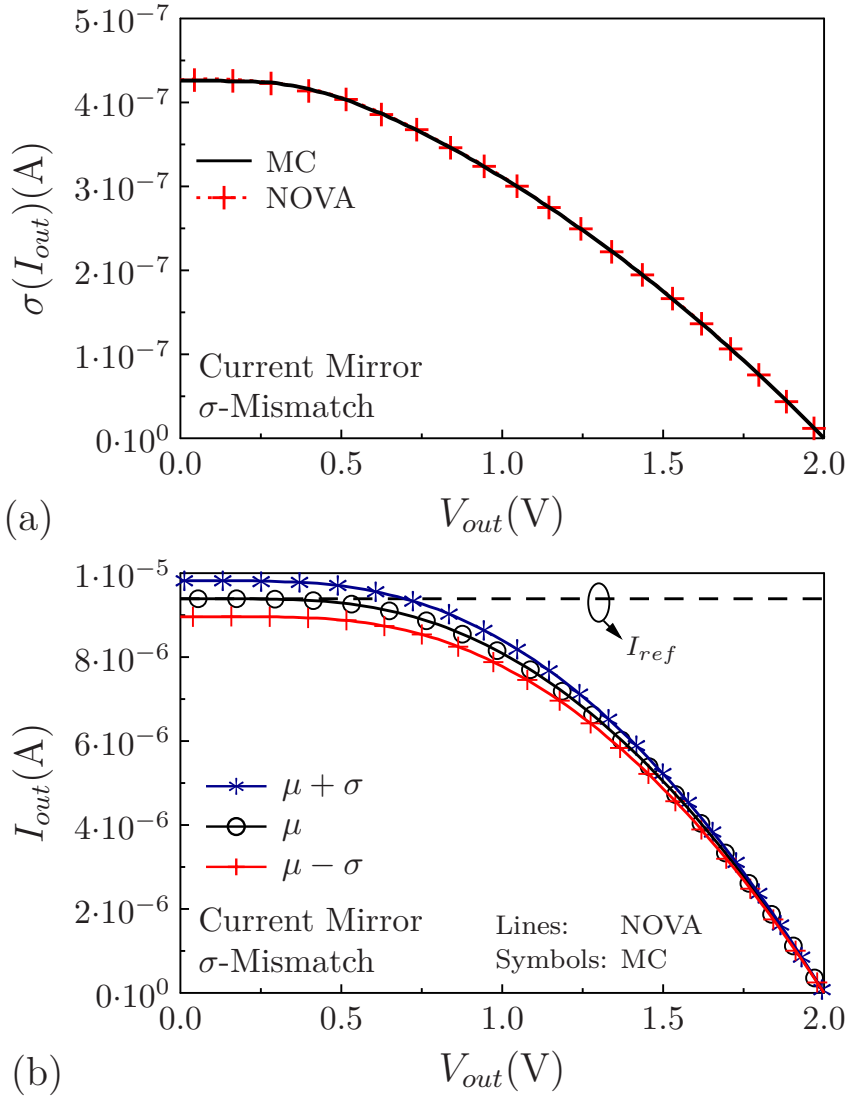

Figure 3.12.: (a) Standard deviation of the output current $\sigma(I_{out})$ of the current mirror of Fig. 3.13 as a function of the output voltage V_{out}. (b) Mean-value μ and corner-value $\mu \pm \sigma$ output currents of the same circuit. Symbols: Monte Carlo simulation with 5000 iterations. Solid lines: NOVA method. Dashed lines: Reference current I_{ref} of the mean-value μ model card.

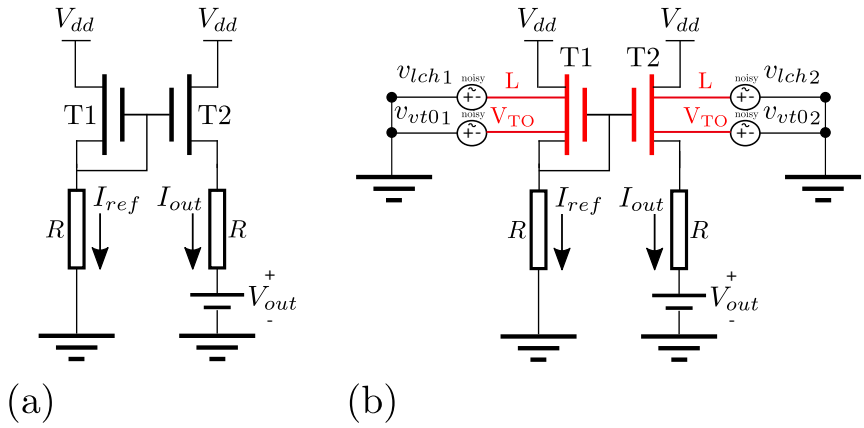

Figure 3.13.: (a) Schematic of a current mirror, used for Monte Carlo simulation, based on two identical p-channel TFTs ($W = 10\,\mu m$, $L = 1\,\mu m$) and two load resistors ($R = 1\,\Omega$) operated with a supply voltage (V_{dd}) of 2.0 V. (b) Schematic of the same circuit used for the NOVA mismatch variation analysis.

Table 3.3.: Simulation processing times

	5000-iteration MC	NOVA method
Source Follower	$\simeq$ 201 min	$\simeq$ 2 min
Inverter mismatch analysis	$\simeq$ 214 min	$\simeq$ 2 min
Inverter process variations	$\simeq$ 202 min	$\simeq$ 2 min
Current Mirror	$\simeq$ 210 min	$\simeq$ 2 min

3.7 Conclusions

An efficient alternative to the Monte Carlo statistical-analysis methodology that can be used for the variability study of integrated circuits has been presented. The proposed "Noise-Based Variability Approach" (NOVA) method has been tested on circuits based on organic TFTs and has been shown to be suitable for fast process and mismatch statistical circuit analyses. NOVA can be easily implemented through a small number of minor modifications to the Verilog-A transistor instances and by a few simple rearrangements of the circuit topology. Unlike Monte Carlo, the NOVA method is applicable only for Gaussian-shaped statistical distributions. The principle advantage of NOVA over Monte Carlo is the significantly shorter processing time, which makes NOVA beneficial for circuit designers.

CHAPTER 4

Variability-Aware Characterization of Organic TFT-Based Circuits

4.1 Introduction

The variability analysis of organic TFT-based circuits is typically performed using Monte Carlo simulations [18], accurate physics-based variability compact models [15] or novel noise-based simulation approaches [20, 34]. The experimental data based on which the impact of variability on the circuit characteristics is analyzed are usually obtained exclusively at the device level, i.e., from the transistors. Here, we analyze the variability of analog organic-TFT-based circuits by considering experimental data acquired not only from a large number of discrete organic TFTs, but in addition from a large number of TFT-based current mirrors, both of which were fabricated on a flexible polymeric substrate [24].

4.2 Devices and Circuits

All transistors and circuits were fabricated on a 125 µm-thick flexible polyethylene naphthalate (PEN) substrate. The TFTs were fabricated in the inverted coplanar (bottom-gate, bottom-contact) device architecture [47] and using stencil lithography based on high-resolution silicon stencil masks [52]. Fig. 4.10 shows the actual layout of the masks that designed and used for the circuit fabrication. The TFTs consist of 25 nm-thick aluminum gate electrodes, an

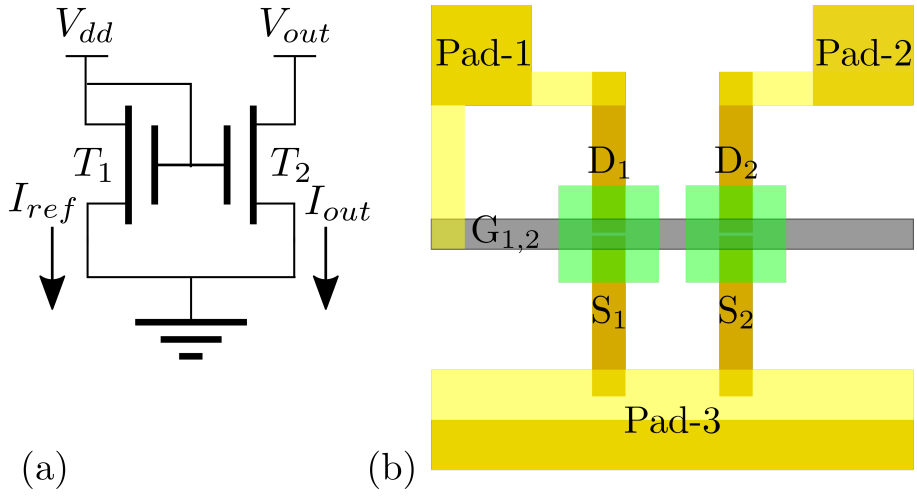

Figure 4.1.: (a) Schematic and (cb) layout of a current mirror comprised of two nominally identical p-channel TFTs with a channel width (W) of 50 µm and a channel length (L) of 5 µm. The total layout area of a single current mirror is $720 \times 685\,\mu m^2$.

Table 4.1.: layout layers

Name	Material	Layer	Color
Bottom metal	Gold	1	Brown
Bottom Gate	Aluminum	2	Gray
Semiconductor p-channel	DNTT	3	Green
Top metal	Gold	4	Yellow

8 nm-thick hybrid AlOx/SAM gate dielectric [53], 30 nm-thick gold (Au) source and drain contacts coated with a pentafluorobenzenethiol (PFBT) monolayer, and a nominally 25 nm-thick vacuum-deposited film of the small-molecule semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) (Fig. A.2(a)). The TFTs are p-channel transistors and have a channel lengths (L) of 5 µm and 2 µm and channel-width-to-length ratio (W/L) of 10. The maximum process temperature was 60 Â°C. For each channel length, 60 nominally identical TFTs and 99 nominally identical current mirrors were fabricated.

The circuit schematic and the layout of a current mirror are shown in Fig. 4.1(b) and (c), respectively. The circuit consists of two nominally identical TFTs

T_1 (reference TFT) and T_2 (output TFT), both having a channel width (W) of 50 µm, a channel length (L) of 5 µm, and a total gate-to-contact overlap area of 20 µm^2. The interconnect lines have a width of 50 µm, and the distance between the two DNTT patterns is 40 µm. The probe pads Pad-1 and Pad-2 have an area 150 × 150 µm^2 each, and Pad-3 has an area of 150 x (maximum-layout-length) µm^2. In Table 4.1, the available layout layers are listed. Note that the AlOx/SAM gate dielectric, the PFBT contact-functionalization layer and the PEN substrate are not drawn layers. Note that more details on the layout implementation are listed in APPENDIX B.

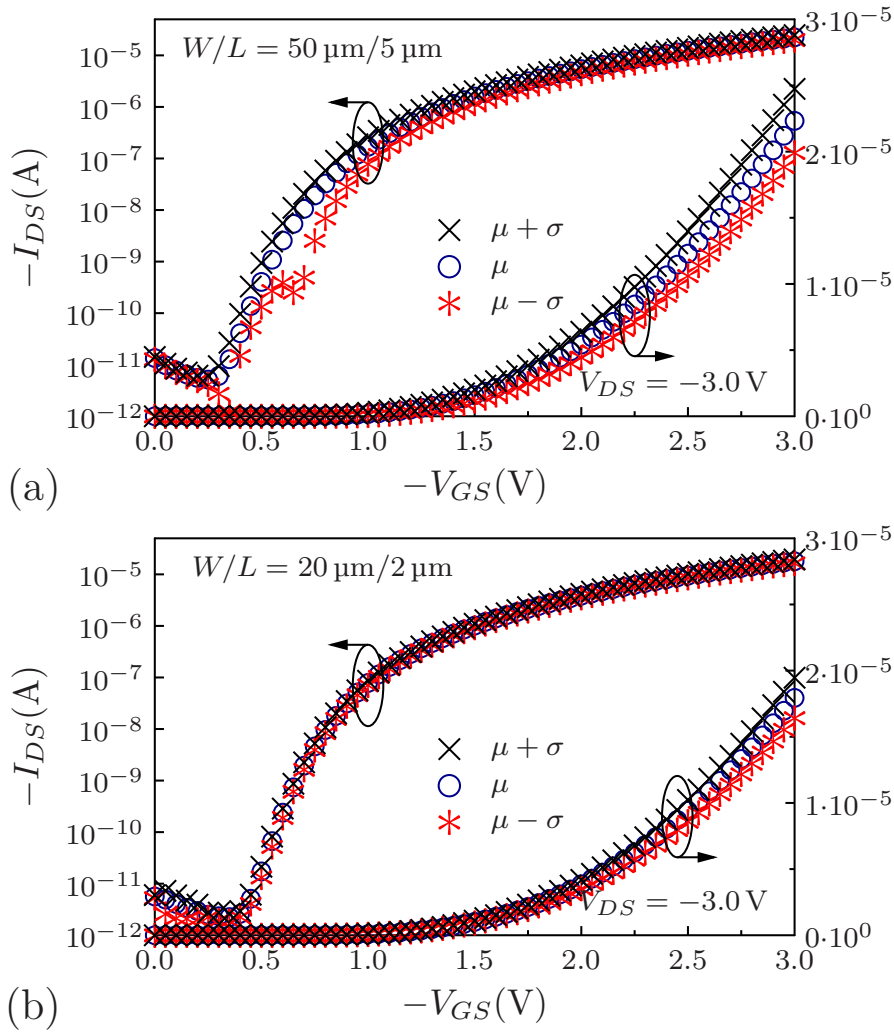

Figure 4.2.: Experimental (μ) and ($\mu \pm \sigma$) (a, b) transfer characteristics of the p-channel coplanar DNTT TFTs with channel lengths (L) of 5 µm and 2 µm in the saturation regime. Symbols: Measurement data.

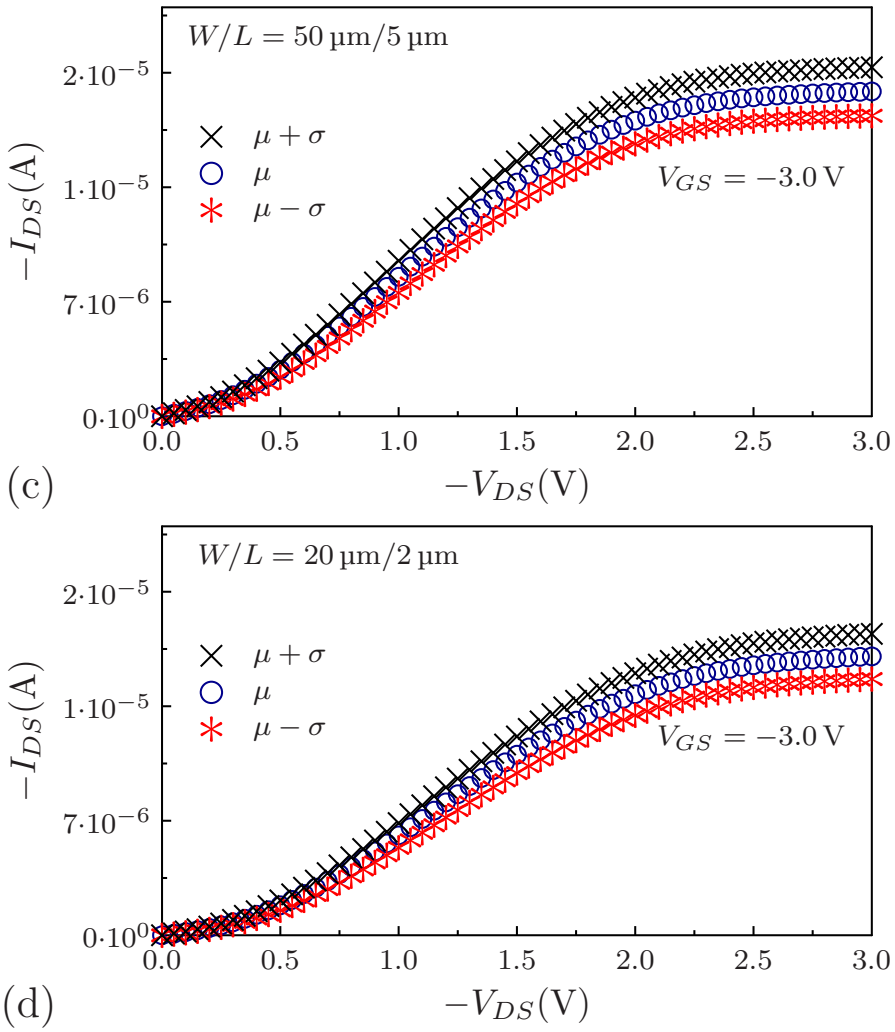

Figure 4.3.: Experimental (μ) and ($\mu \pm \sigma$) output characteristics of the p-channel coplanar DNTT TFTs with channel lengths (L) of 5 µm and 2 µm in the saturation regime. Symbols: Measurement data.

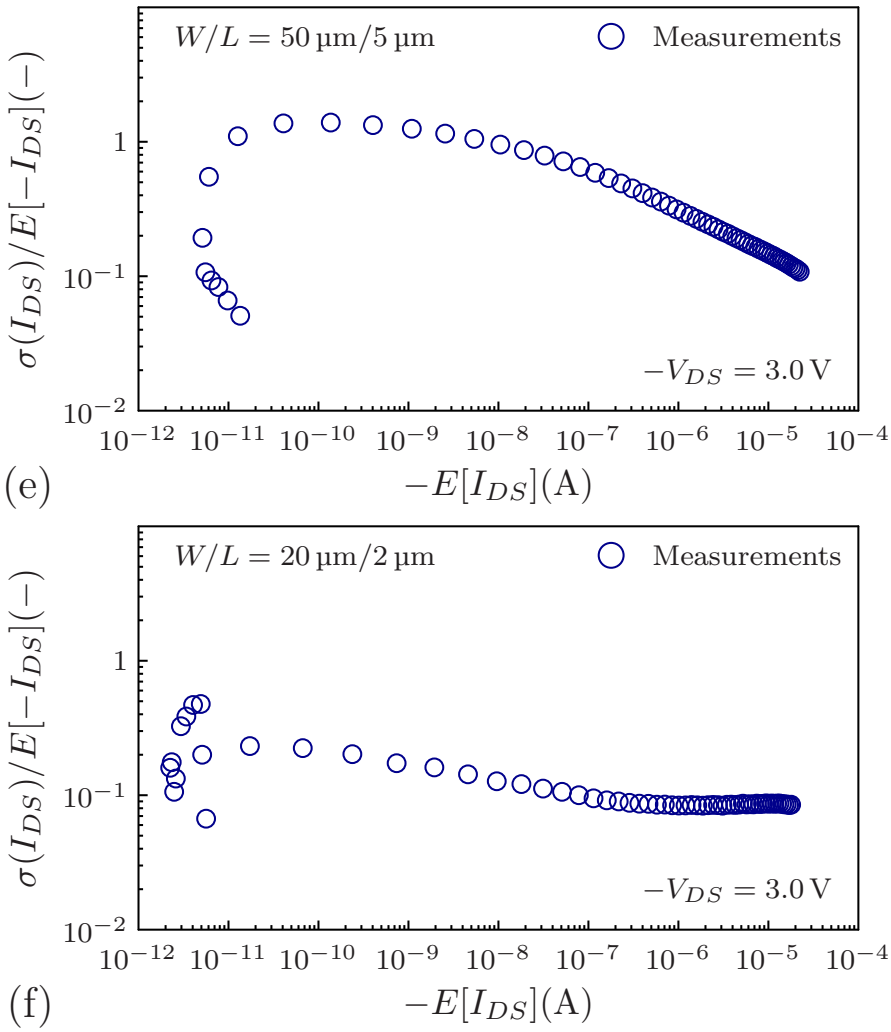

Figure 4.4.: Normalized drain-current standard deviation $\sigma(I_{DS})/E[-I_{DS}]$ versus mean-value drain current $E[-I_{DS}]$ of the p-channel coplanar DNTT TFTs with channel lengths (L) of 5 µm and 2 µm. Symbols: Measurement data.

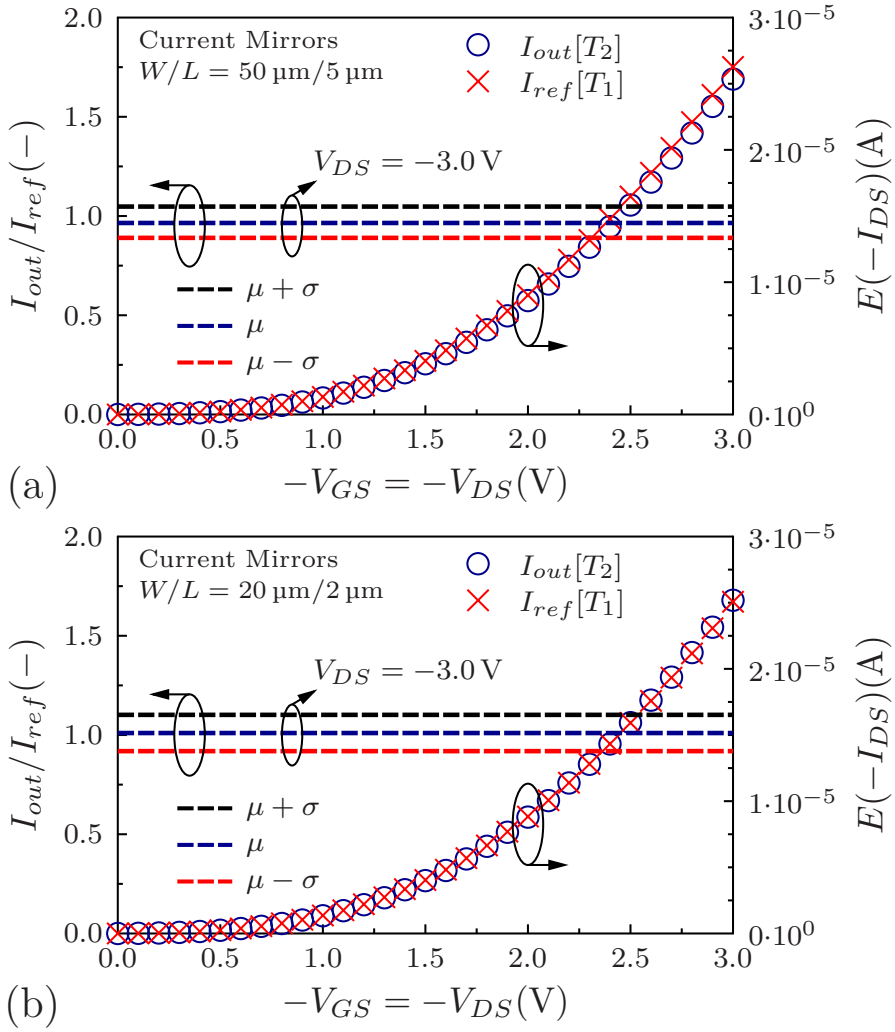

Figure 4.5.: Symbols: Mean value drain current $E[-I_{DS}]$ of the reference TFT ($I_{ref}[T_1]$) and of the output TFT ($I_{out}[T_2]$) employed in the current mirrors. Dashed lines: Mean-value (μ) and corner-value ($\mu \pm \sigma$) characteristics of the parameter I_{out}/I_{ref} at the maximum gate-source and drain-source voltages ($V_{GS} = V_{DS} = -3.0V$). The results were obtained during Step 1 of the measurement protocol, during which both TFTs are biased in saturation ($-V_{GS} = -V_{DS}$) and the currents $I_{ref}[T_1]$ and $I_{out}[T_2]$ are recorded.

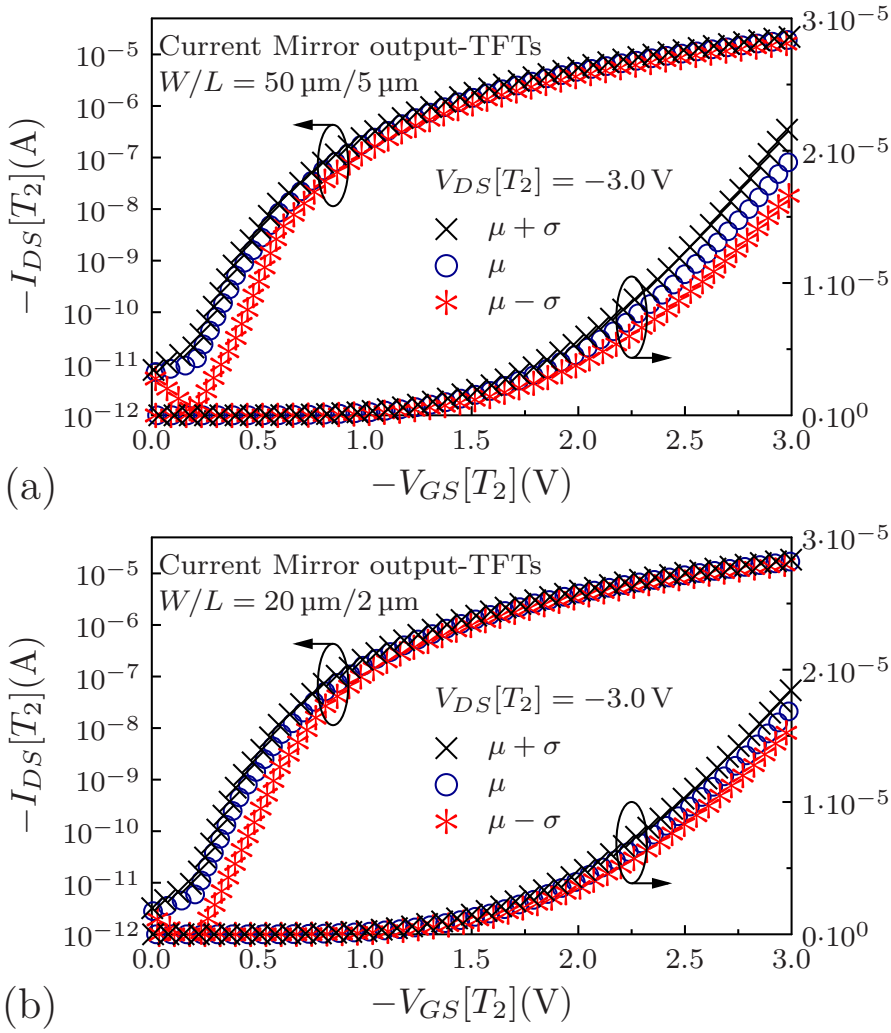

Figure 4.6.: Experimental (μ) and ($\mu \pm \sigma$) transfer (a, b) characteristics of the reference and output TFTs employed in the current mirror. The results were obtained during Step 2 of the measurement protocol, during which both TFTs are biased separately. Symbols, lines: Measurement data.

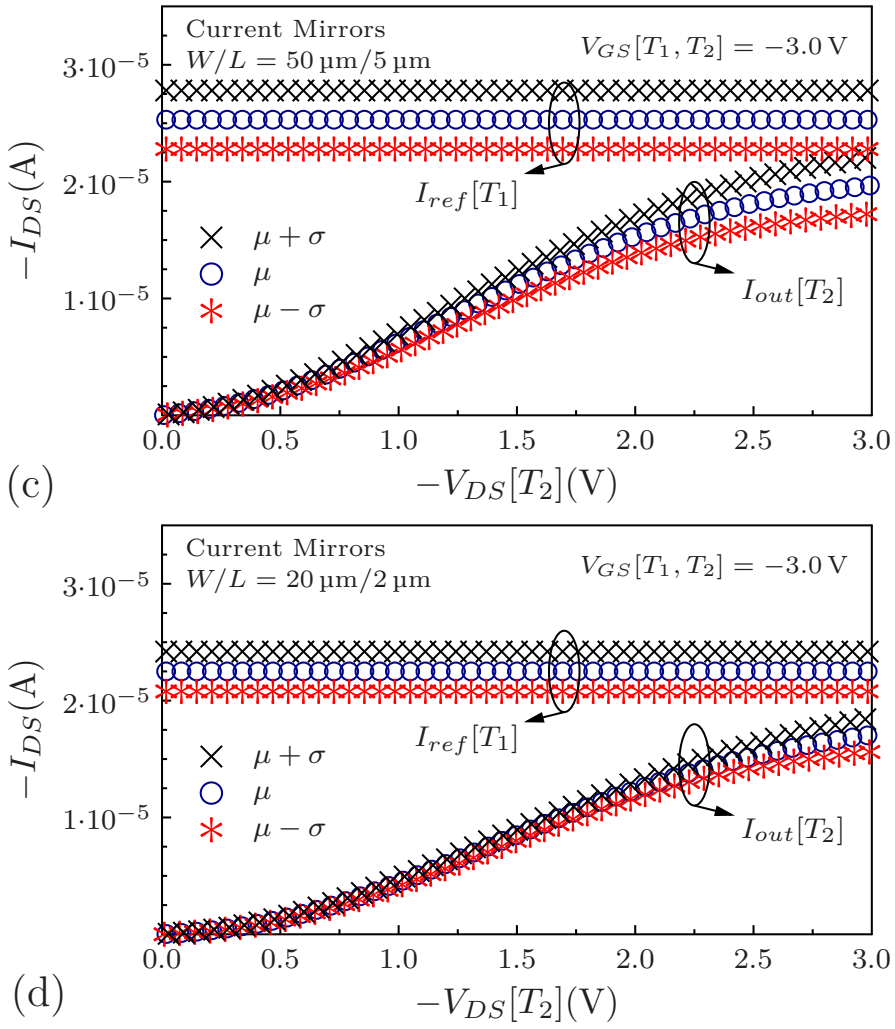

Figure 4.7.: Experimental (μ) and ($\mu \pm \sigma$) output (c, d) characteristics of the reference and output TFTs employed in the current mirror. The results were obtained during Step 2 of the measurement protocol, during which both TFTs are biased separately. Symbols, lines: Measurement data.

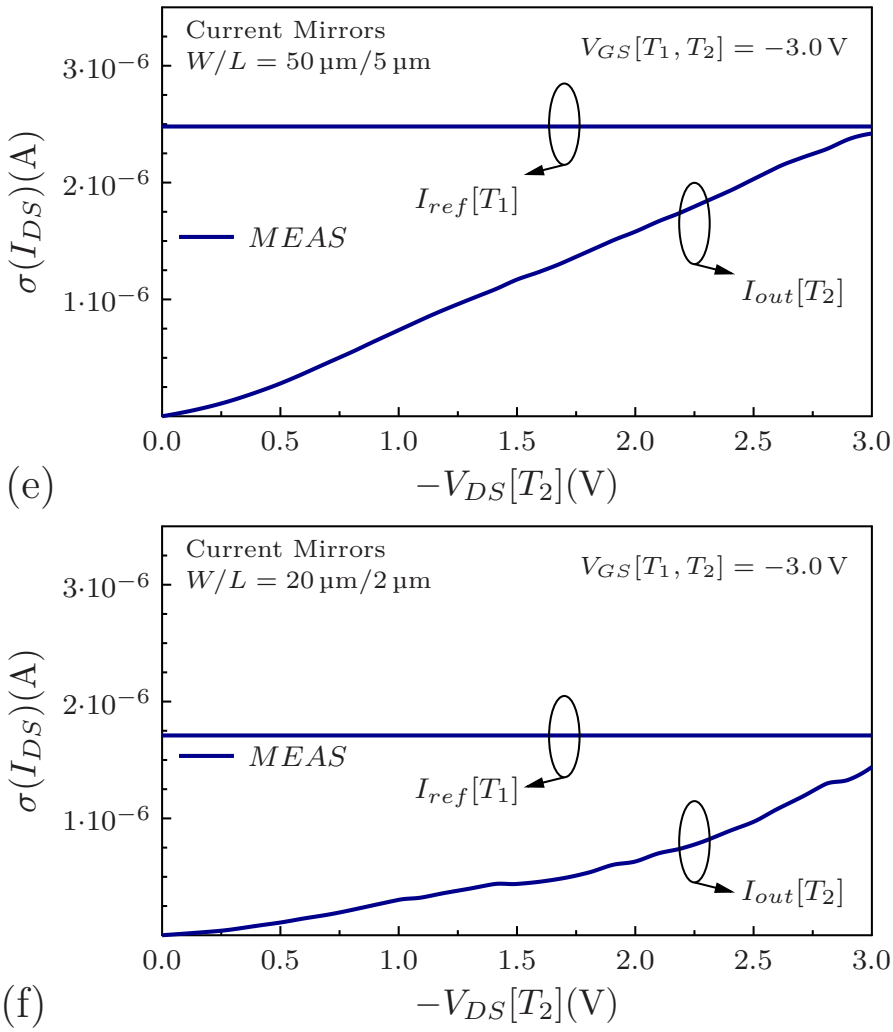

Figure 4.8.: (e, f) Standard deviation $\sigma(I_{DS})$ of the circuit currents. The results were obtained during Step 2 of the measurement protocol, during which both TFTs are biased separately. Symbols, lines: Measurement data.

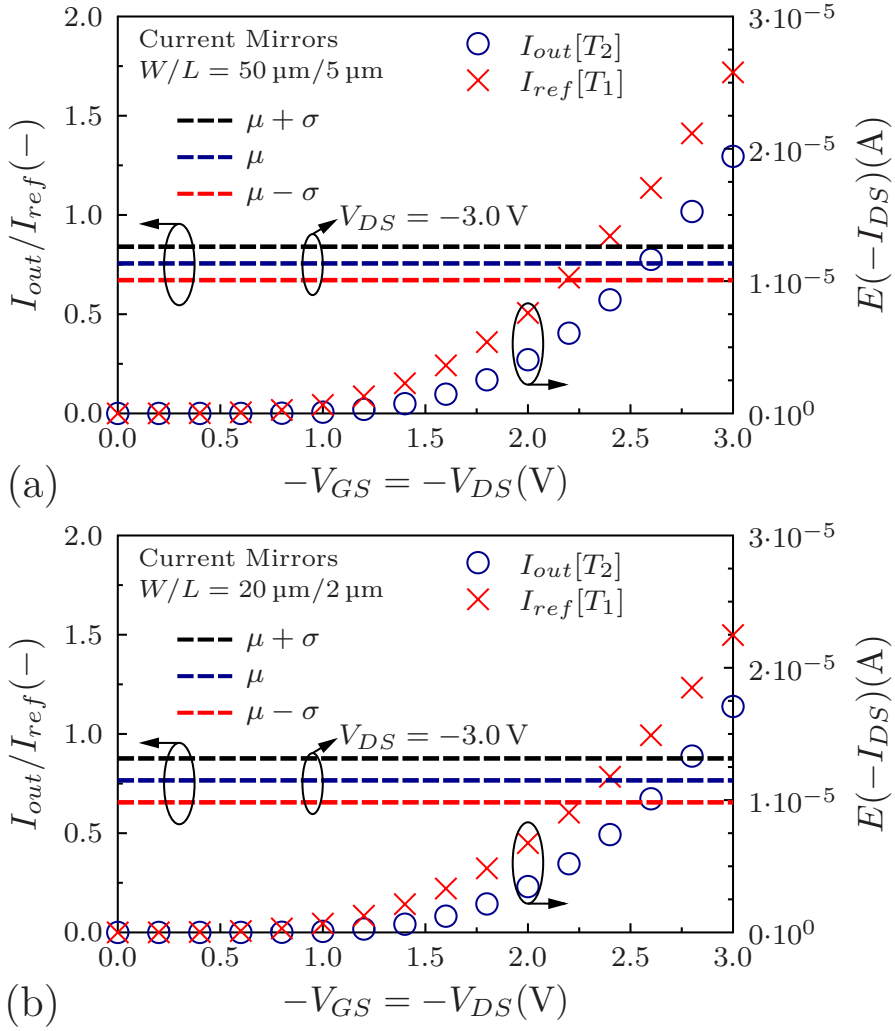

Figure 4.9.: Symbols: Mean value drain current $E[-I_{DS}]$ of the reference TFT ($I_{ref}[T_1]$) and of the output TFT ($I_{out}[T_2]$) employed in the current mirrors. Dashed lines: Mean-value (μ) and corner-value ($\mu \pm \sigma$) characteristics of the parameter I_{out}/I_{ref} at the maximum gate-source and drain-source voltages ($V_{GS} = V_{DS} = -3.0V$). The results were obtained during Step 2 of the measurement protocol, during which both TFTs are biased separately.

4.3 Measurements

The current-voltage characteristics of the TFTs and current mirrors were recorded in ambient air at room temperature. To measure the transfer characteristics of the discrete TFTs, a constant drain-source voltage (V_{DS}) of $-3.0\,\mathrm{V}$ was applied while sweeping the gate-source voltage (V_{GS}) from 0 to $-3.0\,\mathrm{V}$ with a step size of $-50\,\mathrm{mV}$. To measure the output characteristics, the drain-source voltage was swept from 0 to $-3.0\,\mathrm{V}$ at a fixed gate-source voltage of $-3.0\,\mathrm{V}$.

For the current mirrors, the following measurement protocol was applied:

Step 1: The reference and output currents (I_{ref}, I_{out}) were recorded while sweeping the gate-source and drain-source voltages applied to T_1 and T_2 simultaneously from 0 to $-3.0\,\mathrm{V}$ with a step size of $-100\,\mathrm{mV}$, thus keeping both TFTs in the saturation regime by maintaining $V_{GS} = V_{DS}$.

Step 2: The transfer and output characteristics of T_2 were recorded using the voltages given in the previous paragraph (transfer characteristics: $V_{DS} = -3.0\,\mathrm{V}$, $V_{GS} = 0$ ... $-3.0\,\mathrm{V}$; output characteristics: $V_{GS} = -3.0\,\mathrm{V}$, $V_{DS} = 0$ ... $-3.0\,\mathrm{V}$).

In all the above cases, the mean-value (μ) and the corner-value ($\mu \pm \sigma$) characteristics were acquired from the experimental current-voltage curves by calculating the sample-mean $E[I_{DS}]$ and the sample-standard-deviation $\sigma(I_{DS})$ of the drain current I_{DS} at each data point.

4.4 Results and Discussion

The experimental mean-value (μ) and corner-value ($\mu \pm \sigma$) transfer and output characteristics of the TFTs having channel lengths (L) of 5 µm and 2 µm are shown in Fig. 4.2(a)-(b). In Fig. 4.2(e) and (f), the normalized drain-current standard deviation $\sigma(I_{DS})/E[-I_{DS}]$ is plotted as a function of the mean-value drain current $E[-I_{DS}]$. For both channel lengths, the bias-dependent variability of the drain current has its maximum in the subthreshold region and its minimum near the largest applied gate-source voltage, in agreement with the results reported in [15]. The TFTs with the smaller channel length (2 µm) have smaller drain-current variability in the subthreshold region than the TFTs with the larger channel length (5 µm). The mobility-fluctuation effect [15], which is related to

the variability at the maximum gate-source voltage, is similar for both channel lengths.

In Fig. 4.5(a) and (b), the mean value drain current $E[-I_{DS}]$ of the reference (T_1) and output (T_2) TFTs of the current mirrors is plotted as a function of the drain-source voltage. In the same plot, the mean-value (μ) and corner-value ($\mu \pm \sigma$) of the parameter I_{out}/I_{ref} at the maximum gate-source and drain-source voltages ($V_{GS} = V_{DS} = -3.0V$) are depicted as dashed lines. In Table B.1 the statistics of the parameter I_{out}/I_{ref} are listed in detail. These results were obtained during Step 1 of the measurement protocol. The current mirrors show excellent drain-current matching, with a variability of 3% when the TFTs have a channel length of 5 µm and a variability of 1% when the channel length is 2 µm.

In Fig. 4.6, the results obtained during Step 2 of the measurement protocol, during which both TFTs of the current mirror are biased separately, are shown. Fig. 4.6 and 4.7 show the mean-value (μ) and corner-value ($\mu \pm \sigma$) transfer and output characteristics of the output TFT T_2 of the current mirror. The reference currents of the circuits (Iref) are also included. In Fig. 4.8(e) and (f) the standard deviation $\sigma(I_{DS})$ of the circuit currents is depicted. Mean value and standard deviation of the reference and output currents of the current mirrors are similar to those of the discrete TFTs.

Fig. 4.9(a) and (b) show the drain current mismatch and the statistics of the parameter I_{out}/I_{ref} of the current mirrors obtained during Step 2 of the measurement protocol (Table 4.3). For both channel lengths (5 µm and 2 µm), the mismatch of the on-state current ($I_{DS} = I_{on}$ at $V_{GS} = V_{DS} = -3.0V$) is close to 25%. This can be attributed to the greater impact of the hysteresis effect [54, 55] on the output TFT of the circuit.

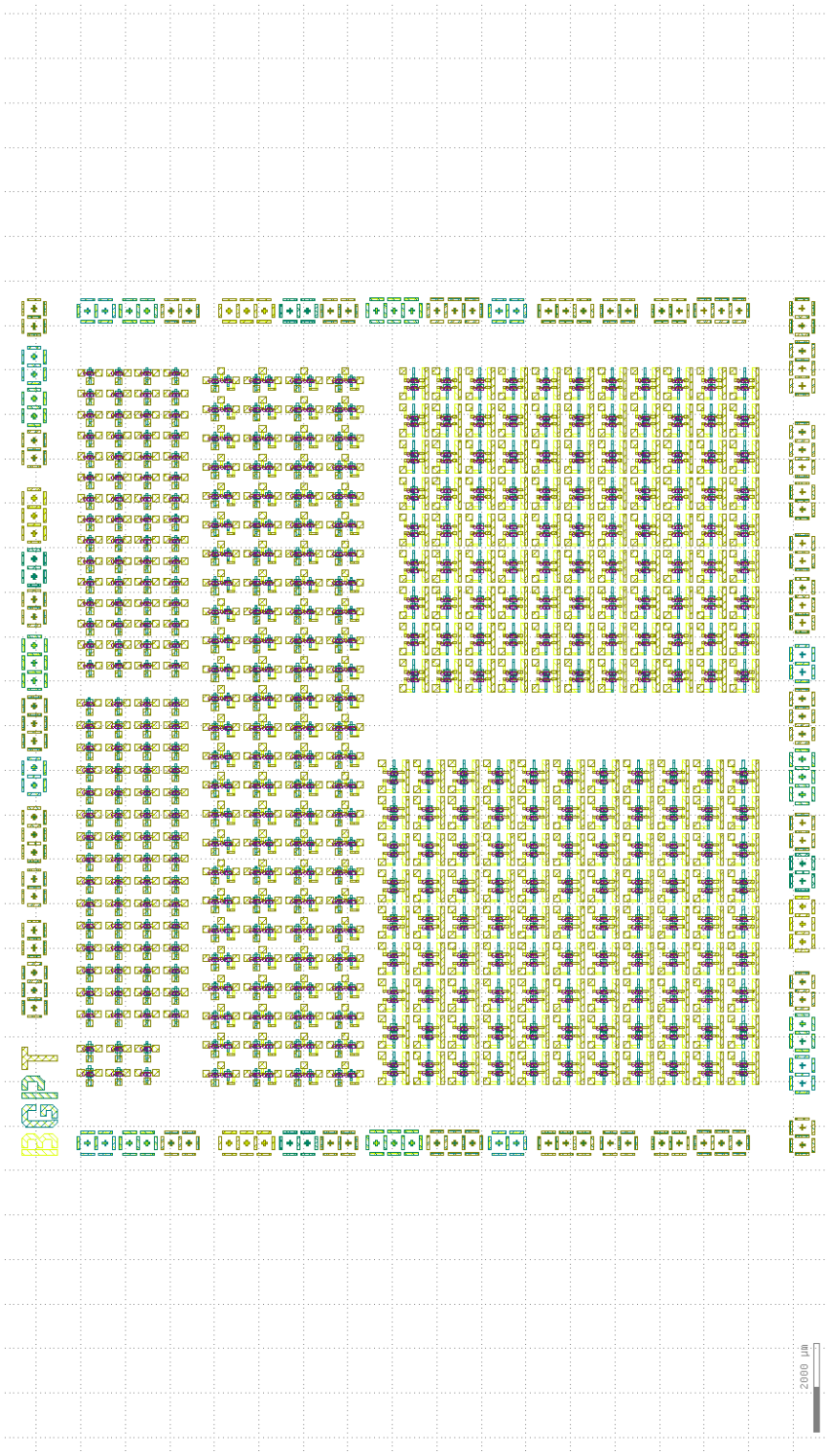

Figure 4.10.: Actual layout of the silicon stencil mask-set designed for the organic TFT circuit fabrication.

4.5 Conclusions

Using experimental data obtained from discrete organic TFTs and from TFT-based current mirrors, we have analyzed the variability of the circuit characteristics. For this purpose, a large number of nominally identical TFTs and nominally identical current mirrors were fabricated and characterized. For the discrete TFTs, the expected behavior of the bias-dependent drain-current variability was confirmed. The statistical behavior of the TFT-based current mirrors, quantified here in terms of the mean value and the standard deviation of the reference and output currents, are similar to those of the discrete TFTs. The drain-current mismatch of the current-mirrors is as small as 1% when both TFTs of the circuit are biased simultaneously and as large as $\sim 25\%$ when the TFTs are biased separately.

Table 4.2.: $\frac{I_{out}}{I_{ref}}$ statistics - Step 1 setup, $V_{DS}(T_1) = V_{DS}(T_2) = -3.0V$

	area5 [L=5um]	area6 [L=2um]
$E[I_{out}/I_{ref}]$	0.968	1.01
$\sigma(I_{out}/I_{ref})$	0.079	0.09
$E + \sigma[I_{out}/I_{ref}]$	1.047	1.1
$E - \sigma[I_{out}/I_{ref}]$	0.895	0.981

Table 4.3.: $\frac{I_{out}}{I_{ref}}$ statistics - Step 2 setup, $V_{DS}(T_1) = V_{DS}(T_2) = -3.0V$

	area5 [L=5um]	area6 [L=2um]
$E[I_{out}/I_{ref}]$	0.7558	0.766
$\sigma(I_{out}/I_{ref})$	0.0840	0.112
$E + \sigma[I_{out}/I_{ref}]$	0.8457	0.876
$E - \sigma[I_{out}/I_{ref}]$	0.6715	0.655

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COMPACT MODELING OF VARIABILITY IN ORGANIC THIN-FILM TRANSISTORS
Aristeidis Nikolaou

CHAPTER 5

Charge-Based Compact Model for the Low-Frequency Noise in Organic Thin-Film Transistors

5.1 Introduction

In this Chapter, a bias-dependent model for the drain-current low-frequency noise (LFN) in organic TFTs is introduced. The charged-based model proposed here takes into account the two discrete effects that constitute the sources of the flicker noise in organic TFTs, namely the noise due to the carrier-number and correlated mobility-fluctuation effect (ΔN or McWorther model) and the noise due to the fluctuation of the charge-carrier mobility ($\Delta\mu$ or Hooge model). As a result, the model is more flexible in accurately predicting the bias-dependent behavior of LFN in organic TFTs of the inverted staggered device architecture, from the subthreshold regime to the maximum-effective-gate-voltage regime. Additionally, the LFN-model equations are fully combined with a current-voltage compact model for organic TFTs [11, 56], and the complete model is implemented in Verilog-A. For the verification, a large number of organic transistors were fabricated and characterized.

5.2 LFN Model Derivation

In this section, the derivation of a drain-current LFN model suitable for organic TFTs is presented. As mentioned above, the proposed model treats the flicker

noise as the sum of two contributions, namely the noise due to ΔN effects and the noise due to $\Delta\mu$ effects.

For the LFN noise model derived here, the charge-based organic-TFT current-voltage model described in [11] will be used as the basis. The proposed model provides a single current equation that is valid for all operation regions and can be obtained from

$$I_{DS} = \mu W \left(U_T \frac{Q_S - Q_D}{L} + \frac{Q_S^2 - Q_D^2}{2LC'_{ox}} \right), \tag{5.1}$$

where $U_T = kT/q$ is the thermodynamic voltage, W is the channel width, L is the channel length, C'_{ox} is the unit-area gate-dielectric capacitance, and μ is the effective carrier mobility. Q_S and Q_D are the densities of quasi-mobile charges per gate area at the source and drain ends of the channel, respectively, and can be expressed as

$$Q_{S(D)} = aU_T C'_{ox} \mathcal{L} \left\{ \exp\left(\frac{V_{GS(D)} - V_{T0}}{aU_T} \right) \right\}, \tag{5.2}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, a is the subthreshold slope factor and V_{T0} is the threshold voltage.

5.2.1 ΔN Model Derivation

Here, the impact of local charge-density fluctuations in the carrier channel as one of the sources of the drain-current LFN in organic TFTs will be discussed. This noise originates from local random fluctuations of the carrier density or carrier velocity, leading to a local fluctuation of the drain current [12]. The fluctuation of the drain current around its nominal value is thus considered to be a result of the sum of all local fluctuation contributions along the channel. Following the methodology described in [41] for silicon transistors and in [15] for organic TFTs, the transistor channel is divided into a noisy element located between the positions x and $x + \delta x$ and two noiseless pseudo-transistors T1 and T2 that have channel lengths x and $L - x$, respectively (see Fig. 1). The relative local current fluctuation at the position x of the channel can be described as [15]

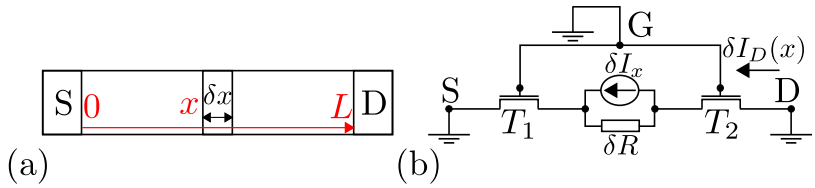


Figure 5.1.: (a) Schematic of a transistor channel divided into a noisy element located between the positions x and $x + \delta x$ and two noiseless pseudo-transistors having channel lengths x and $L - x$, respectively. (b) Small-signal representation [15].

$$\frac{\delta I_x}{I_D} = \frac{\delta I_D(x)}{I_D} = \frac{\delta Q_{CH}}{Q_{CH}} + \frac{\delta \beta}{\beta}, \tag{5.3}$$

where the term $\delta\beta/\beta$ describes the charge-trapping effects or edge effects [19] on $\beta = \mu C'_{ox}\frac{W}{L}$. Attributing all variations exclusively to charge trapping, and by following [40], based on Matthiessen's rule, the carrier mobility, including the effect of the trapping mechanism, can be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_0} + a_c Q_t \Leftrightarrow \mu = \frac{\mu_0}{1 + a_c Q_t \mu_0}, \tag{5.4}$$

where $Q_t = -qN_t$ is the density of trapped charges and $a_c = \tilde{a_c}/q$ is the Coulomb scattering coefficient [41]. Using (5.4), the following can be obtained:

$$\frac{\delta\beta}{\delta Q_t} = -\, a_c \mu \beta \tag{5.5}$$

and the relative current fluctuation can be expressed as

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{Q_{CH}}\frac{\delta Q_{CH}}{\delta Q_t} - a_c\mu\right)\delta Q_t, \tag{5.6}$$

where δQ_t is the local charge fluctuation related to the fluctuation in the trap density. Furthermore, according to [15], the following can be obtained

$$\frac{\delta Q_{CH}}{\delta Q_t} \simeq \frac{Q_{CH}}{Q_{CH} + Q^*/a} = \frac{q_{ch}}{q_{ch} + 1/a}. \tag{5.7}$$

Similar to some of the widely-used commercial compact models (i.e. BSIM-BULK, EKV) [9, 41], charges are normalized according to

$$\frac{Q_{CH}}{q_{ch}} = \frac{Q_D}{q_d} = \frac{Q_S}{q_s} = Q^*, \tag{5.8}$$

where

$$Q^* = aU_T C'_{ox}. \tag{5.9}$$

The terms q_s and q_d are the normalized charge densities at the source and drain ends of the channel, respectively. By substituting (5.7) into (5.6), the relative local current fluctuation can be rewritten as

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{q_{ch} + 1/a} + a^*\mu\right)\frac{\delta Q_t}{Q^*}, \tag{5.10}$$

where $a^* = a_c(-Q^*)$ is a parameter related to the Coulomb scattering coefficient given in units of Vs/m^2. Accordingly, the power spectral density (PSD) of the local noise current source δI_x, normalized to the square of the drain current, is expressed as [41]

$$\frac{S_{\delta I_x^2}}{I_D^2} = \left(\frac{1}{q_{ch} + 1/a} + a^*\mu\right)^2 \frac{S_{\delta Q_t^2}}{(Q^*)^2}. \tag{5.11}$$

The PSD $S_{\delta N_t^2}$ is given by

$$S_{\delta Q_t^2} = \frac{kTq^2\lambda N_T}{W\delta x f^{AF}}, \tag{5.12}$$

where f is the frequency, AF is the frequency-exponent [57], k is the Boltzmann constant, T is the temperature, λ is the tunneling attenuation distance and N_T is the gate-dielectric volumetric trap density per unit energy (in units of $\mathrm{eV}^{-1}\mathrm{m}^{-3}$).

Following [41], by integrating along the transistor channel, the PSD of the total drain-current fluctuation S_{I_D}, normalized to the square of the total drain

current, can be expressed as

$$\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} = \frac{1}{L^2}\int_0^L \delta x \frac{S_{\delta I_x^2}}{I_D^2} dx, \tag{5.13}$$

and by substituting equations (5.9), (5.11) and (5.12) into (5.13), the following can be obtained:

$$\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} = \frac{q^4 \lambda N_T}{WL^2 a^2 kTC_{ox}'^2 f^{AF}} \int_0^L \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 dx. \tag{5.14}$$

Solving the integral above yields:

$$\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} = C^*_{noise}|_{\Delta N} \times B^*_{noise}(q_{ch})|_{\Delta N} \tag{5.15}$$

where

$$C^*_{noise}|_{\Delta N} = \frac{q^4 \lambda N_T}{WLa^2 kTC_{ox}'^2 f^{AF}} \tag{5.16}$$

and

$$B^*_{noise}(q_s, q_d)|_{\Delta N} = \frac{1}{i_d}\left(B_1 + B_2 + B_3 + B_4\right). \tag{5.17}$$

The coefficients B_1, B_2, B_3 and B_4 are given by

$$\begin{aligned} B_1 &= \left(\frac{2(a-1)a^*\mu}{a} + 1\right) ln\left(\frac{1+aq_s}{1+aq_d}\right), \\ B_2 &= \left(\frac{1-a}{1+aq_s} - \frac{1-a}{1+aq_d}\right), \\ B_3 &= i_d \left(a^*\mu\right)^2, \\ B_4 &= 2\left(a^*\mu\right)\left(q_s - q_d\right). \end{aligned} \tag{5.18}$$

The normalized drain current i_d can be expressed as $i_d = I_D/\mu(aU_T)^2 C'_{ox} W/L$. Similarly as demonstrated previously for silicon transistors [39, 58], the results we obtained for the $1/f$ noise in organic TFTs are closely related to those derived in [15] for the drain-current variability, since the physical mechanisms at the origin of both phenomena are similar.

5.2.2 $\Delta\mu$ Model Derivation

The drain-current flicker noise arising from the fluctuations of the carrier mobility can be modeled using the so-called Hooge ($\Delta\mu$) model. Accordingly, the total PSD of a local noise-current source δI_x due to the delta μ effect can be expressed as [41]

$$\frac{S_{\delta I_x^2}}{I_D^2}\bigg|_{\Delta\mu} = \frac{a_H q}{W\delta x(-Q_{ch})f^{AF}}, \tag{5.19}$$

where a_H is the unitless Hooge parameter. By using equation (5.13) and integrating along the channel, the PSD of the total fluctuation of the drain current due to the $\Delta\mu$ effect, normalized to the square of the total drain current, is then given by

$$\frac{S_{ID}}{I_D^2}\bigg|_{\Delta\mu} = C^*_{noise}|_{\Delta\mu} \times B^*_{noise}(q_{ch})|_{\Delta\mu}, \tag{5.20}$$

where

$$C^*_{noise}|_{\Delta\mu} = \frac{a_H q^2}{WLkTaC'_{ox}f^{AF}} \tag{5.21}$$

and

$$B^*_{noise}|_{\Delta\mu} = \frac{1}{i_d}(lnq_s - lnq_d + q_s - q_d) \tag{5.22}$$

is the bias-dependent factor.

5.2.3 Total Drain-Current Low-Frequency Noise

The total LFN as the sum of the two noise sources described above can be expressed as follows:

$$\frac{S_{ID}}{I_D^2} = \frac{S_{ID}}{I_D^2}\bigg|_{\Delta N} + \frac{S_{ID}}{I_D^2}\bigg|_{\Delta\mu} \tag{5.23}$$

5.3 Statistical Model

In this section, an analytical charge-based model for the bias-dependent variability of the low frequency noise in organic TFTs is presented. The model is an extension of the mean-value LFN model presented in the previous section. The derivation procedure is described next.

By using equations (5.11) and (5.12) the following can be obtained:

$$\frac{S_{\delta I_x^2}}{I_D^2}\Big|_{\Delta N} \times f = \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 \frac{N_T^*}{W\delta x N_{sp}^2}, \tag{5.24}$$

where $N_T^* = kT\lambda N_T$ is the trap density in cm^{-2}. The term N_{sp} is given by

$$N_{sp} = -\frac{Q^*}{q}. \tag{5.25}$$

Furthermore, by integrating along the channel, (5.24) becomes

$$\begin{aligned}\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} \times f &= \frac{1}{L^2}\int_0^L \delta x \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 \frac{N_T^*}{W\delta x N_{sp}^2} dx \\ &= \frac{1}{L^2}\int_0^L \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 \frac{N_T^*}{W N_{sp}^2} dx \\ &= \frac{1}{L}\int_0^1 \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 \frac{N_T^*}{W N_{sp}^2} d\omega,\end{aligned} \tag{5.26}$$

where $\omega = x/L$ is the normalized position x along the channel [41]. Since the local noise current sources δI_x are considered to be uncorrelated, using (5.26) and Taylor's series approximation $(Var(g(x)) \approx Var(x)g'(\theta)^2)$, $Var\left(\frac{S_{ID}}{I_D^2} \times f\right)$, similarly as demonstrated at [59], can be calculated in the following way

$$\begin{aligned}&Var\left(\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} \times f\right) = \\ &Var\left(\frac{1}{L}\int_0^1 \left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 \frac{N_T^*}{W N_{sp}^2} d\omega\right) = \\ &\left(\frac{1}{LWN_{sp}^2}\right)^2 \int_0^1 Var\left(\left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 N_T^*\right) d\omega = \\ &\frac{1}{L^2W^2N_{sp}^4}\int_0^1 Var\left(\left(\frac{1}{q_{ch}+1/a} + a^*\mu\right)^2 N_T^*\right) d\omega.\end{aligned} \tag{5.27}$$

Furthermore, the quantity $\left(\frac{1}{q_{ch}+1/a}+a^*\mu\right)^2 N_T^*$ is a function of N_T^* and therefore, using the Taylor's series approximation that was mentioned above, the following can be obtained:

$$\begin{aligned} &Var\left(f(N_T^*)\right) = \\ &Var\left(\left(\frac{1}{q_{ch}+1/a}+a^*\mu\right)^2 N_T^*\right) = \\ &\left[\left(\left(\frac{1}{q_{ch}+1/a}+a^*\mu\right)^2 N_T^*\right)'\right]^2 Var(N_T^*) = \\ &\left(\frac{1}{q_{ch}+1/a}+a^*\mu\right)^4 N_T^*. \end{aligned} \tag{5.28}$$

Please note that since the number of traps N_T^* follow the Poisson distribution, $Var(N_T^*) = N_T^*$. By substituting (5.28) into (5.27), the variance of the PSD of the LFN due to the ΔN effect (carrier-number correlated-mobility fluctuation

effect) can be expressed as:

$$
\begin{aligned}
&Var\left((S_{ID}/I_D^2)|_{\Delta N} \times f\right) = \\
&\frac{1}{L^2W^2N_{sp}^4}\int_0^1\left(\frac{1}{q_{ch}+d}+a^*\mu\right)^4 N_T^* d\omega = \\
&\frac{N_T^*}{L^2W^2N_{sp}^4}\frac{1}{i_d}\int_{q_d}^{q_s}\left(\frac{1}{q_{ch}+d}+a^*\mu\right)^4 (1+q_{ch})dq_{ch} = \\
&\frac{N_T^*}{L^2W^2N_{sp}^4}\frac{1}{i_d}\Bigg|\ \frac{2a^*\mu(3(d-1)a^*\mu-2)}{d+q_{ch}}+\frac{4(d-1)a^*\mu-1}{2(d+q_{ch})^2} \\
&+\frac{d-1}{3(d+q_{ch})^3}+\frac{(a^*\mu)^4q_{ch}^2}{2}+(a^*\mu+4)(a^*\mu)^3q_{ch} \\
&-2(a^*\mu)^2(2(d-1)a^*\mu-3)ln(d+q_{ch})\Bigg|_{q_d,q_s} = \\
&\frac{N_T^*}{L^2W^2N_{sp}^4}\frac{1}{i_d}\Bigg|\ B_1\frac{1}{d+q_{ch}}+B_2\frac{1}{(d+q_{ch})^2}+B_3\frac{1}{(d+q_{ch})^3} \\
&+B_4q_{ch}^2+B_5q_{ch}-B_6ln(d+q_{ch})\Bigg|_{q_d,q_s} = \\
&\frac{N_T^*}{L^2W^2N_{sp}^4}\frac{1}{i_d}\Bigg[\Bigg(\ B_1\frac{1}{d+q_s}+B_2\frac{1}{(d+q_s)^2}+B_3\frac{1}{(d+q_s)^3} \\
&+B_4q_s^2+B_5q_s-B_6ln(d+q_s)\ \Bigg)- \\
&\Bigg(\ B_1\frac{1}{d+q_d}+B_2\frac{1}{(d+q_d)^2}+B_3\frac{1}{(d+q_d)^3}+B_4q_d^2+C_5q_d \\
&-B_6ln(d+q_d)\ \Bigg)\Bigg] = C^*|_{\Delta N}\times B^*(q_{ch})|_{\Delta N},
\end{aligned}
$$

where

$$
C^*|_{\Delta N} = \frac{N_T^*}{L^2W^2N_{sp}^4} \tag{5.29}
$$

and

$$\begin{aligned} B^*(q_{ch})|_{\Delta N} = \frac{1}{i_d} \Bigg[& B_1 \left(\frac{1}{d+q_s} - \frac{1}{d+q_d} \right) \\ & + B_2 \left(\frac{1}{(d+q_s)^2} - \frac{1}{(d+q_d)^2} \right) \\ & + B_3 \left(\frac{1}{(d+q_s)^3} - \frac{1}{(d+q_d)^3} \right) \\ & + B_4(q_s^2 - q_d^2) + C_5(q_s - q_d) - B_6 ln(\frac{d+q_s}{d+q_d}) \Bigg] . \end{aligned} \tag{5.30}$$

Coefficients B_1, B_2, B_3, B_4, B_5 and B_6 can be calculated from

$$\begin{aligned} B_1 &= 2a^*\mu(3(d-1)a^*\mu - 2), \\ B_2 &= \frac{4(d-1)a^*\mu - 1}{2}, \\ B_3 &= \frac{d-1}{3}, \\ B_4 &= \frac{(a^*\mu)^4}{2}, \\ B_5 &= (a^*\mu + 4)(a^*\mu)^3, \\ B_6 &= 2(a^*\mu)^2(2(d-1)a^*\mu - 3). \end{aligned} \tag{5.31}$$

The normalized drain current i_d and factor d, can be expressed as $i_d = I_D/\mu(aU_T)^2 C'_{ox} W/L$ and $d = 1/a$, respectively. The number of traps N_T^* and a^*, are the fitting parameters of the model.

5.4 LFN variance due to $\Delta\mu$ effect

The total PSD of a local noise current source δI_x due to $\Delta\mu$ effect (Hooge Model) can be expressed as

$$\frac{S_{\delta I_x^2}}{I_D^2}\Bigg|_{\Delta\mu} = \frac{a_H}{q_{ch} W \delta x N_{sp} f}, \tag{5.32}$$

where a_H is the unitless Hooge parameter. By integrating along the channel, the PSD of the total fluctuation of the drain current is then given by

$$\frac{S_{ID}}{I_D^2}\Big|_{\Delta\mu} \times f = \frac{1}{WLN_{sp}} \int_0^1 \frac{1}{q_{ch}} a_H d\omega. \tag{5.33}$$

By following identical methodology as in (5.27) and (5.28), similarly as in [60], variance $Var\left(\frac{S_{ID}}{I_D^2}\Big|_{\Delta\mu} \times f\right)$ can be calculated in the following way

$$\begin{aligned} &Var\left(\frac{S_{ID}}{I_D^2}\Big|_{\Delta\mu} \times f\right) = \\ &Var\left(\frac{1}{WLN_{sp}} \int_0^1 \frac{1}{q_{ch}} a_H d\omega\right) = \\ &\frac{1}{W^2L^2N_{sp}^2} \int_0^1 \frac{1}{q_{ch}^2} a_H^* d\omega = \\ &\frac{a_H^*}{W^2L^2N_{sp}^2} \frac{1}{i_d} \int_{q_d}^{q_s} \frac{1+q_{ch}}{q_{ch}^2} dq_{ch} = \\ &C^*|_{\Delta\mu} \times B^*(q_{ch})|_{\Delta\mu}, \end{aligned} \tag{5.34}$$

where

$$C^*|_{\Delta\mu} = \frac{a_H^*}{W^2L^2N_{sp}^2} \tag{5.35}$$

and

$$B^*|_{\Delta\mu} = \frac{1}{i_d}(lnq_s - lnq_d + \frac{q_s - q_d}{q_s q_d}). \tag{5.36}$$

Parameter $a_H^* = \sigma^2(a_H)$, will be treated as a fitting parameter. The total variance of LFN can be calculated from the sum of ΔN and $\Delta\mu$ variances.

$$Var\left(\frac{S_{ID}}{I_D^2} \times f\right) = Var\left(\frac{S_{ID}}{I_D^2}\Big|_{\Delta N} \times f\right) + Var\left(\frac{S_{ID}}{I_D^2}\Big|_{\Delta\mu} \times f\right) \tag{5.37}$$

5.5 Devices and Measurements

In order to verify the model, organic p-channel TFTs with a channel width (W) of 100 µm and channel lengths (L) of 40 µm and 20 µm were fabricated on a 125 µm-thick flexible polyethylene naphthalate (PEN) substrate in the inverted staggered (bottom-gate, top-contact) device architecture using polyimide shadow masks [53]. The TFTs consist of 30 nm-thick aluminum gate electrodes, an 8 nm-thick hybrid AlO_x/SAM gate dielectric, a 25 nm-thick vacuum-deposited layer of the small-molecule organic semiconductor DNTT, and 30 nm-thick gold (Au) source and drain contacts [53]. The maximum process temperature was 60 °C.

Protocol for the current-voltage measurements: All transfer characteristics were measured at a drain-source voltage (V_{DS}) of -3.0 V by sweeping the gate-source voltage (V_{GS}) from 0 to -3.0 V with a step size of -50 mV. All measurements were performed in ambient air at room temperature.

Protocol for the LFN measurements: All LFN measurements where performed with the TFTs biased in saturation ($V_{DS} = -3.0$ V) and with gate-source voltages (V_{GS}) of -1.2V, -1.5V, -2.0V, -2.5V and -3.0V. For each applied gate-source voltage, the PSD of the drain-current noise was measured in the frequency range between 1Hz and 10^5Hz. All measurements were performed in ambient air at room temperature.

Approximately 15 TFTs of each channel length (20 µm and 40 µm) were measured. The mean-value characteristics were generated from the measured transfer characteristics by calculating the sample-mean $E[I_{DS}]$ of the measured drain current I_{DS} at each applied gate-source voltage. The mean-value transconductance $E[G_m] = \Delta E[I_{DS}]/\Delta V_{GS}$ was approximated from the mean-value transfer characteristics. Each PSD sample of the drain-current noise S_{ID} was multiplied by the corresponding frequency, the average $S_{ID}f$ value was calculated in the frequency range between 10 Hz and 100 Hz, and the mean value of the noise $E[S_{ID}f]$ was calculated by averaging over all TFTs. This procedure was executed for each gate-source voltage at which a noise measurement had been performed. For gate-source voltages in the deep subthreshold regime, the corner frequency value of the noise spectrum is relatively small and thus the white-noise regime is

noticeable from lower frequency values [61]. Additionally, in the same biasing regime, the deviation of the noise spectrum from the ideal $1/f$ LFN trend is quite large, leading to AF exponent values smaller than unity [57]. This was taken into account during the calculation of the experimental $S_{ID}f$ values.

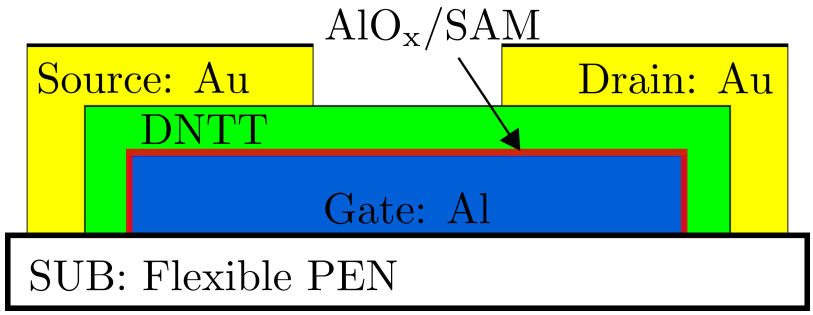


Figure 5.2.: Schematic cross-section of the organic TFTs fabricated in the inverted staggered (bottom-gate, top-contact) device architecture [16].

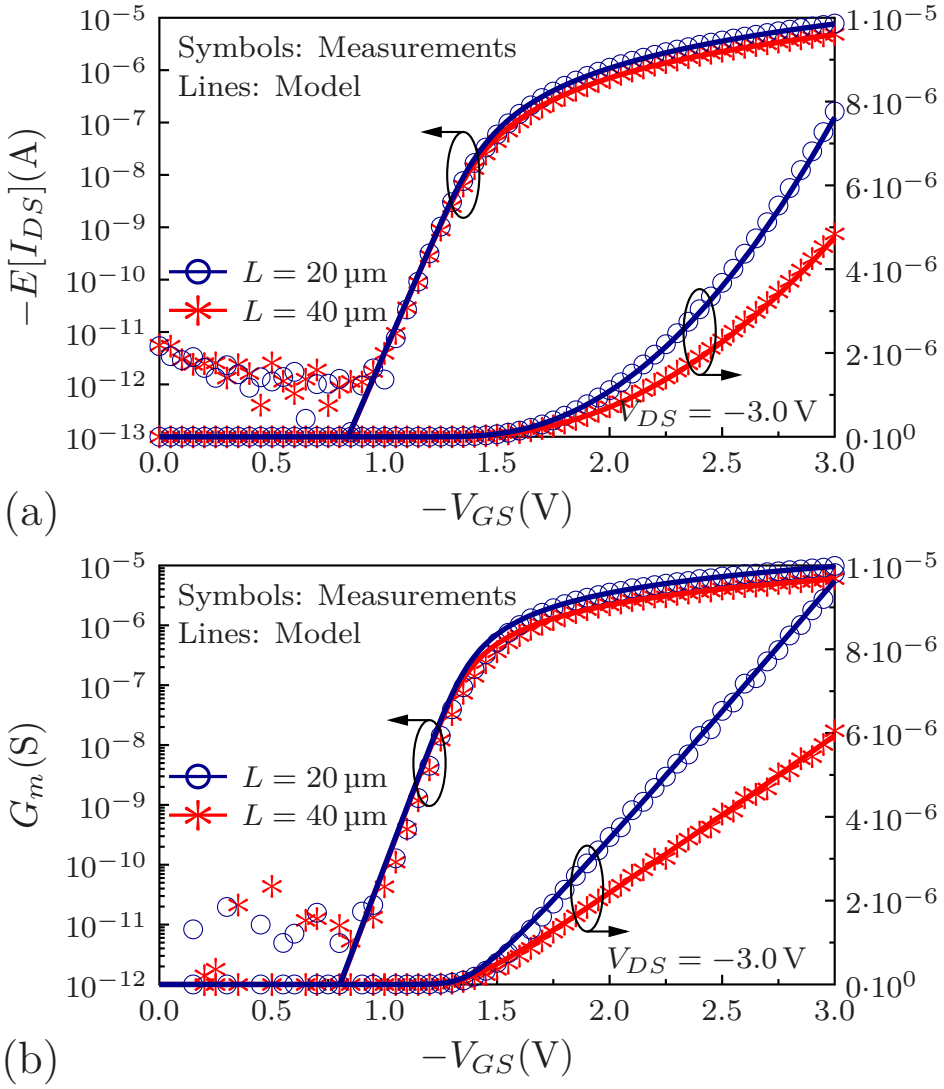


Figure 5.3.: (a) Mean-value drain current $E[I_{DS}]$ and (b) transconductance g_m plotted versus the gate-source voltage V_{GS} of TFTs with channel lengths of 40 µm and 20 µm. The transfer characteristics were recorded in the saturation regime ($V_{DS} = -3.0\,V$). Symbols: Values calculated from experimental data. Lines: Simulation results.

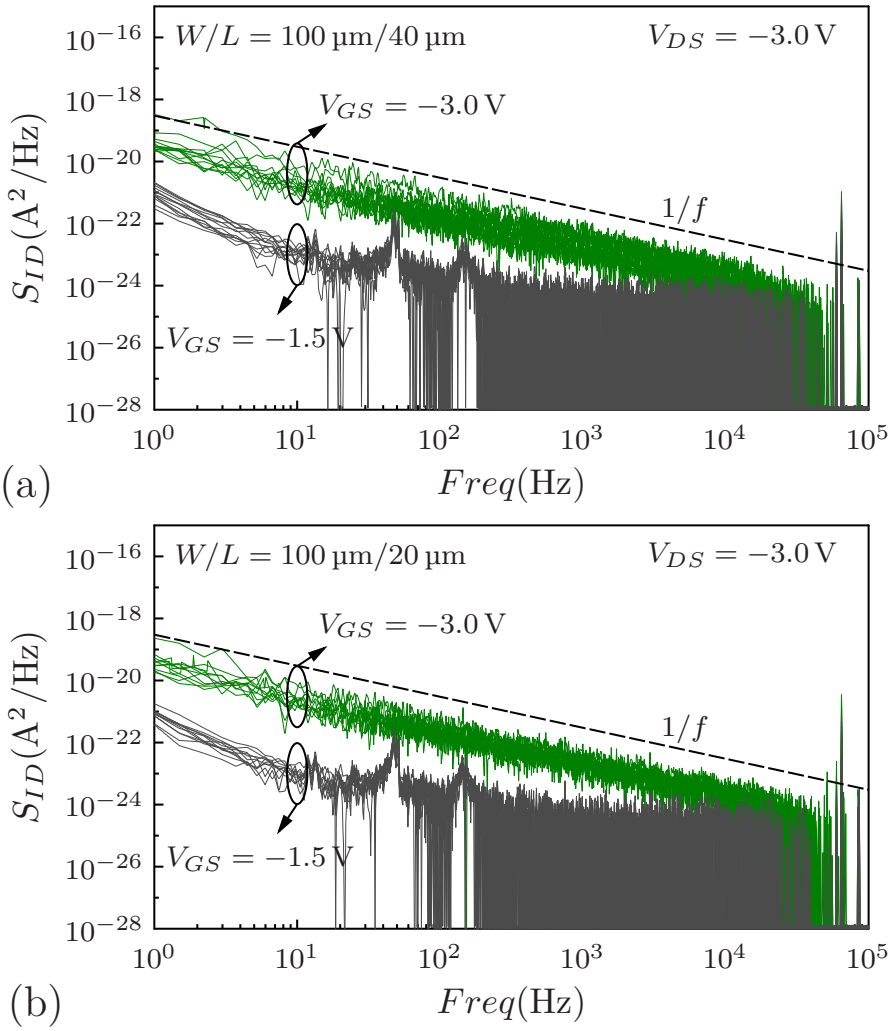


Figure 5.4.: Flicker-noise spectra of TFTs with channel lengths L of (a) 40 µm and (b) 20 µm, measured at gate-source voltages (V_{GS}) of −1.5 V and −3.0 V and with a drain-source voltage V_{DS} of −3.0 V, i.e., with the TFTs operating in saturation. The dashed line indicates the ideal $1/f$ slope.

5.6 Results and Discussion

Fig. 5.3 shows the mean-value transfer characteristics and the transconductance G_m of TFTs with channel lengths of 40 µm and 20 µm, recorded using the current-voltage-measurement protocol described above. Experimental data and simulation results are shown as symbols and lines, respectively, and both are in good agreement, except for the off-state region (i.e., the range of gate-source voltages between between 0 and −0.9 V), which is not covered by the model. In Fig. 5.4, the discrete noise spectra of the TFTs, measured at gate-source voltages (V_{GS}) of −1.5 V (subthreshold regime) and −3.0 V (maximum gate-source voltage), are depicted. In all cases, the measured flicker noise represents typical $1/f^{AF}$ behavior, particularly at lower frequencies between 1Hz and 100Hz, a fact which is in agreement with findings presented in [29].

In Fig. 5.5(a) and (b), the PSDs of the average LFN S_{ID} and S_{ID}/I_{DS}^2 at a frequency of 1 Hz of TFTs with channel lengths of 40 µm and 20 µm are plotted versus the drain current I_{DS}. Both the $S_{ID}f$ and the $S_{ID}f/I_{DS}^2$ PSDs follow a trend that is also typically observed in silicon transistors, namely that the noise is smaller in TFTs that have a smaller active area (product of channel length and channel width) [57]. The $\Delta\mu$ model-component covers the noise behavior at lower drain currents, predicting accurately the observed increase of the noise with decreasing drain current in the subthreshold regime (i.e., for drain currents below about 10^{-7} A), were the $\Delta\mu$ effect is more prominent, similar to silicon transistors [41]. The ΔN model-component is used to predict the measured LFN towards higher drain current. In the subthreshold regime, the distance between localized states is relatively large, which is expected to affect the mobility fluctuation [35], whereas in the above-threshold regime, the hopping distance will be smaller, and thus the effect of the Hooge parameter a_H is expected to be minimal. Overall, the agreement between model ($\Delta N + \Delta\mu$ sum) and experiment is quantitatively satisfactory, both in the below-threshold and the above-threshold regimes of operation.

The noise PSD referred to the gate, $S_{VG} = S_{ID}/G_m^2$, is depicted in Fig. 5.5(c). As can be seen, the LFN is smaller in the TFTs that have a smaller active area, i.e., a smaller channel length. Again, the model correctly predicts the

experimentally measured LFN in both the subthreshold- and the above-threshold regimes.

Table 5.1 summarizes the values of the parameters N_T, a^* and a_H extracted from the LFN model for each channel length in saturation ($V_{DS} = -3.0\,\mathrm{V}$). The trap densities N_T predicted by the model are similar to the values reported previously for organic TFTs [27]. Following a similar approach as in [15], a different set of the model parameters (N_T, a^* and a_H) was extracted for the two different available device geometries. The value of N_T was found to be smaller in the TFTs that have a smaller active area. This finding is consistent with results presented in [15]. The extracted value of the Hooge parameter a_H has also been found to be consistent with the values reported in [62] for several organic-TFT technologies.

In Fig. 5.6 and 5.7 the LFN variability model described in Sections 5.3 and 5.4 is shown versus the obtained experimental data, for saturated TFTs of channel lengths L of 4 µm and 2 µm, respectively.

Table 5.1.: Extracted parameters of the LFN model

	N_T $(\mathrm{eV}^{-1}\mathrm{cm}^{-3})$	a^* $(\mathrm{Vs/m}^2)$	a_H $(-)$
$L = 40\,\mu\mathrm{m}$	1.3×10^9	1465	8.2×10^{-2}
$L = 20\,\mu\mathrm{m}$	1.3×10^8	1375	7.8×10^{-3}

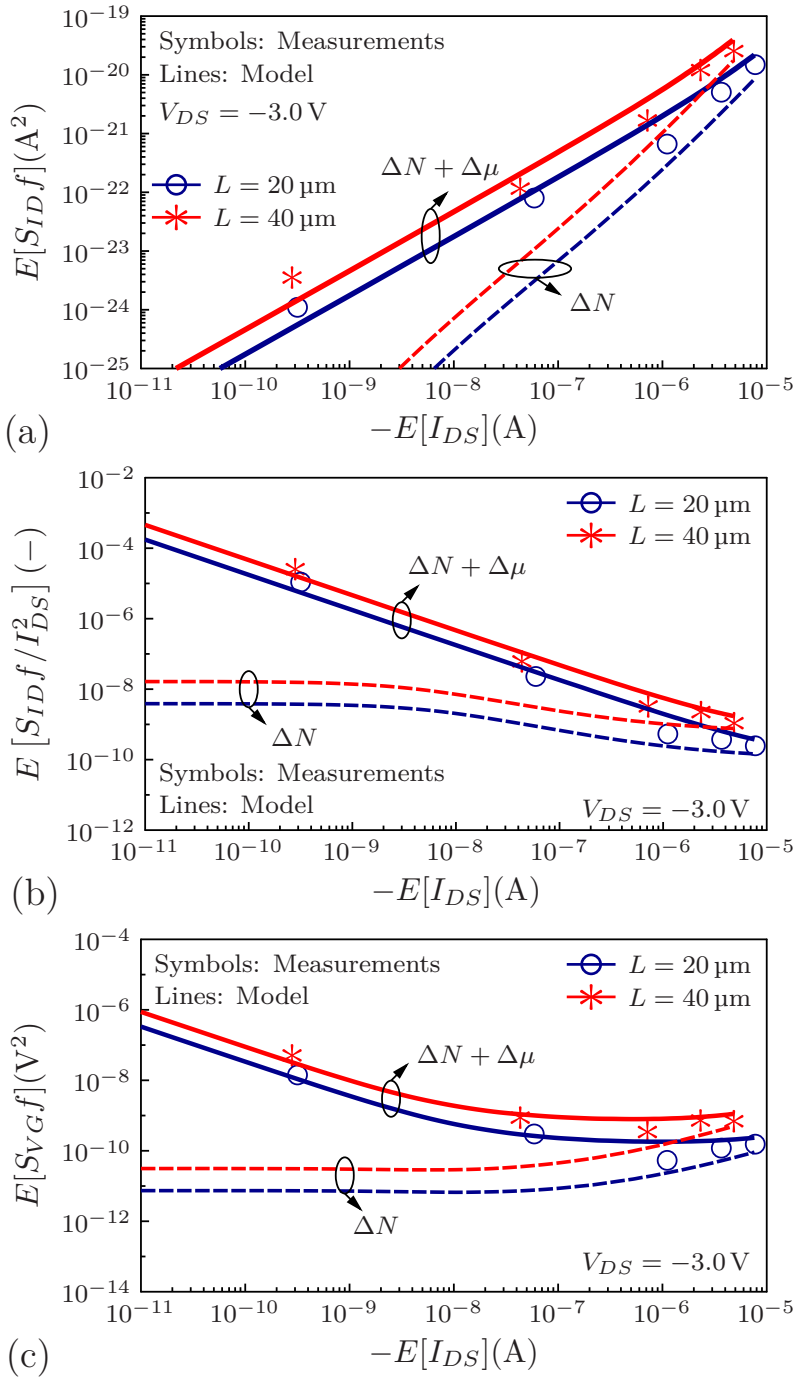


Figure 5.5.: Power spectral densities (a) S_{ID} and (b) S_{ID}/I_{DS}^2 at a frequency of 1 Hz, measured at a drain-source voltage V_{DS} of $-3.0\,\mathrm{V}$ and plotted versus the drain current I_{DS}. (c) Input-referred noise $S_{VG}f$ of the same transistors. All measurements were performed with the TFTs biased in saturation ($V_{DS} = -3.0\,\mathrm{V}$). Symbols: Values calculated from experimental data. Lines: Simulation results.

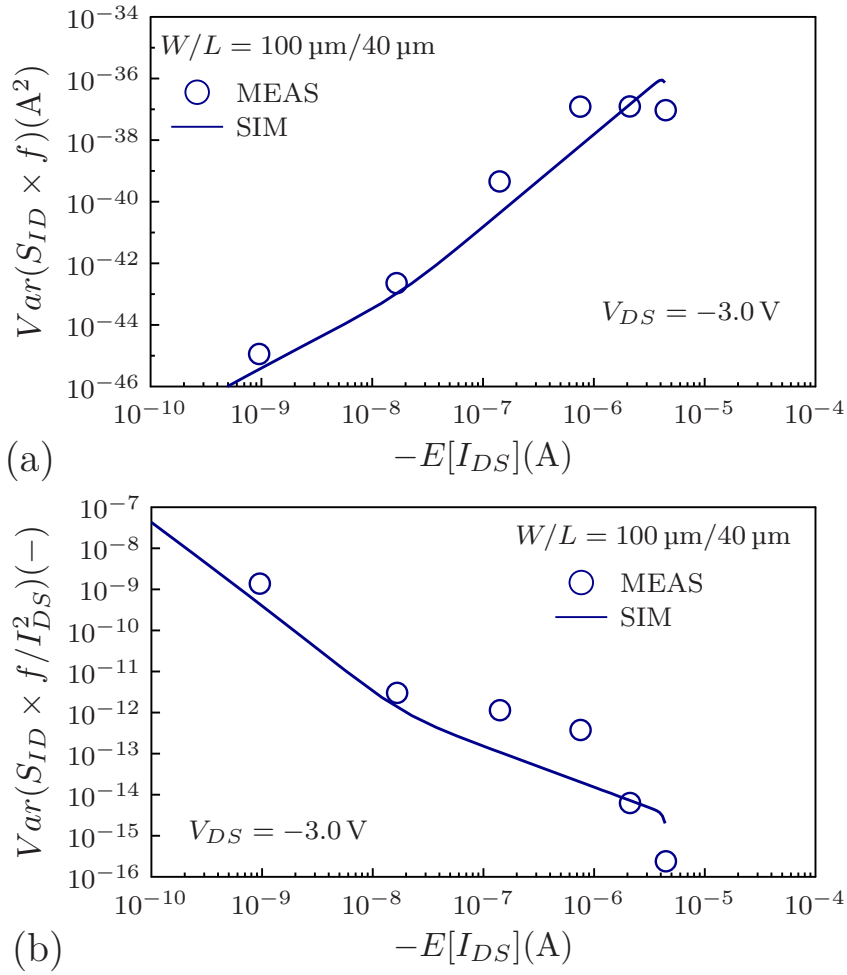


Figure 5.6.: Variability of the $S_{ID} \times f$ PSD of TFTs with channel lengths L of 4 µm at $V_{DS} = -3.0\,V$).

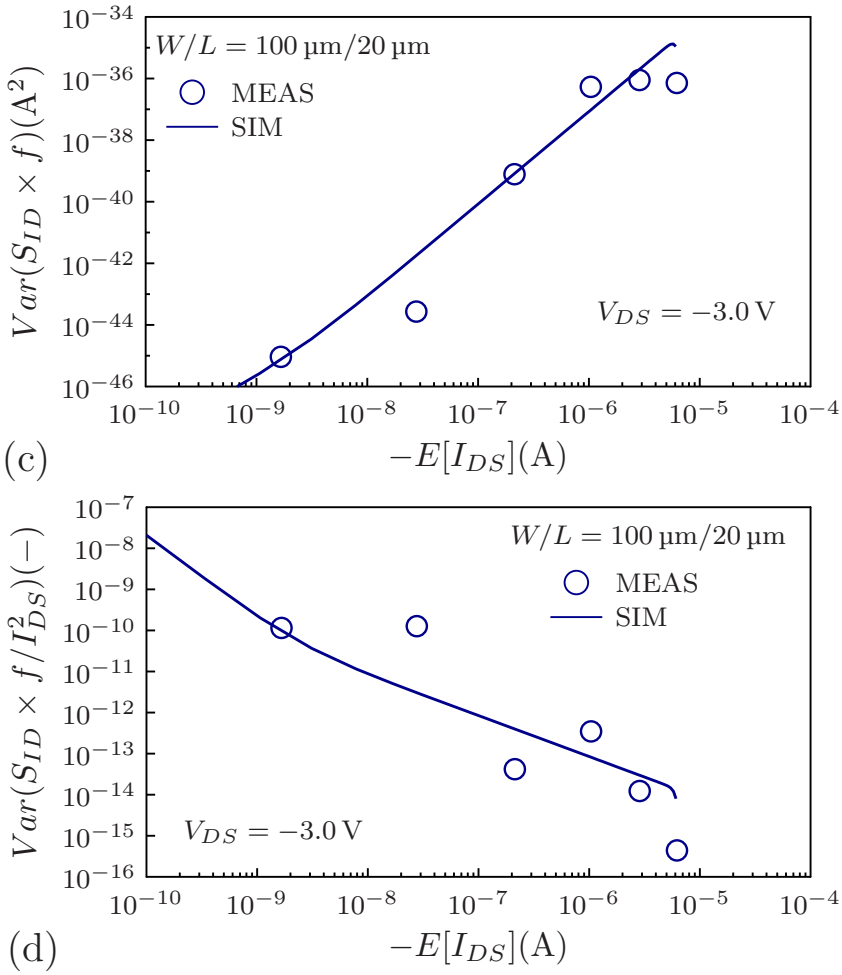


Figure 5.7.: Variability of the $S_{ID} \times f$ PSD of TFTs with channel lengths L of 2 µm, at $V_{DS} = -3.0\,V$).

5.7 Conclusions

In conclusion, we have developed a semi-physical bias-dependent charge-based low-frequency noise model for organic thin-film transistors. The proposed model is based on charge carrier-number fluctuation-correlated mobility fluctuation (ΔN) and mobility-fluctuation (Hooge) ($\Delta\mu$) effects, and it can be applied to TFTs fabricated in the inverted staggered device architecture. We have shown that the drain-current noise is smaller in TFTs with a smaller active area. The ΔN effect was found to dominate over the $\Delta\mu$ effect in the above-threshold regime. The observed trend of the drain-current-normalized noise increasing with decreasing drain current in the subthreshold regime can be attributed mainly to the $\Delta\mu$ effect. Regardless of the channel length, the results of the proposed model are in good agreement with the experimentally measured bias-dependent drain-current LFN of organic TFTs, especially in the below and above-threshold regimes.

UNIVERSITAT ROVIRA I VIRGILI
COMPACT MODELING OF VARIABILITY IN ORGANIC THIN-FILM TRANSISTORS
Aristeidis Nikolaou

CHAPTER 6

Mechanical Bending of Organic Thin-Film Transistors

6.1 Introduction

Organic thin-film transistors (TFTs) are field-effect transistors in which the semiconductor is a thin, usually polycrystalline layer of conjugated organic molecules [1]. Organic TFTs are typically fabricated at temperatures below 100 °C [47] and can thus potentially be employed in a variety of flexible electronics applications [48, 63]. The electrical performance of organic TFTs fabricated on flexible substrates can degrade under mechanical stress that may arise from bending, twisting or stretching of the substrate [64, 65]. By adapting a physics-based compact model to the measurement results, conclusions regarding the impact of bending on the device physics are drawn.

The current Chapter is organized as follows: Section II describes the fabrication of the organic TFTs employed for this study and the experimental bending and characterization procedure. In section III, the effect of bending on the organic semiconductor is discussed. Section IV summarizes the compact model that was used for the bending-performance investigation of the TFTs. Section V presents and discusses the experimental results. In Section VI, conclusions are drawn.

6.2 Devices and Measurements

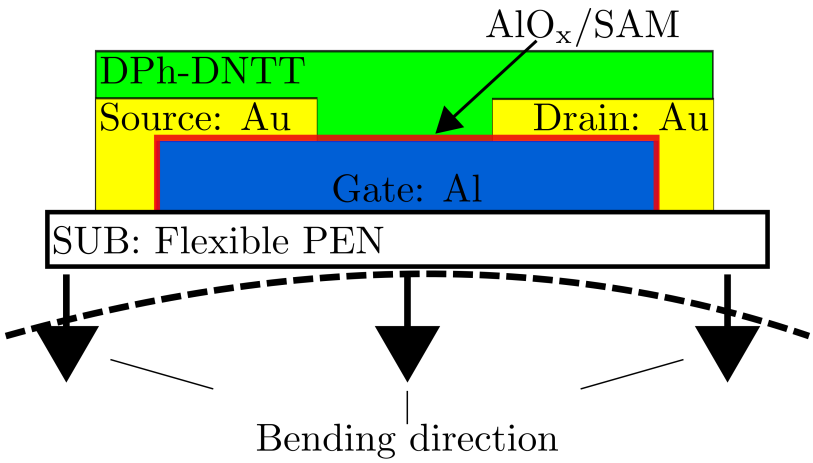
Organic p-channel TFTs with a channel width (W) of 100 µm and channel lengths (L) of 40 µm and 20 µm, were fabricated on 125-µm-thick flexible polyethylene naphthalate (PEN) substrates in the inverted coplanar (bottom-gate, bottom-contact) device architecture [47] using polyimide shadow masks [53]. The TFTs consist of 25-nm-thick aluminum gate electrodes, an 8-nm-thick hybrid AlO_x/monolayer gate dielectric, 30-nm-thick gold (Au) source and drain contacts coated with a pentafluorobenzenethiol (PFBT) monolayer [47] and a 50-nm-thick vacuum-deposited layer of the small-molecule organic semiconductor DNTT [53]. The maximum process temperature was 60 °C. Three nominally identical substrates (substrates 1, 2 and 3) were fabricated. On each substrate, the transistors are located in two separate areas, one with the TFTs that have a channel length of 40 µm and one with the TFTs having a channel length of 20 µm. Each area contains 130 nominally identical TFTs in a 10×13 array. The distance between any two TFTs within an array is 100 µm in each direction. Fig. 6.2 shows the actual layout of the masks that designed and used for the TFT fabrication.

6.2.1 Experimental (part A)

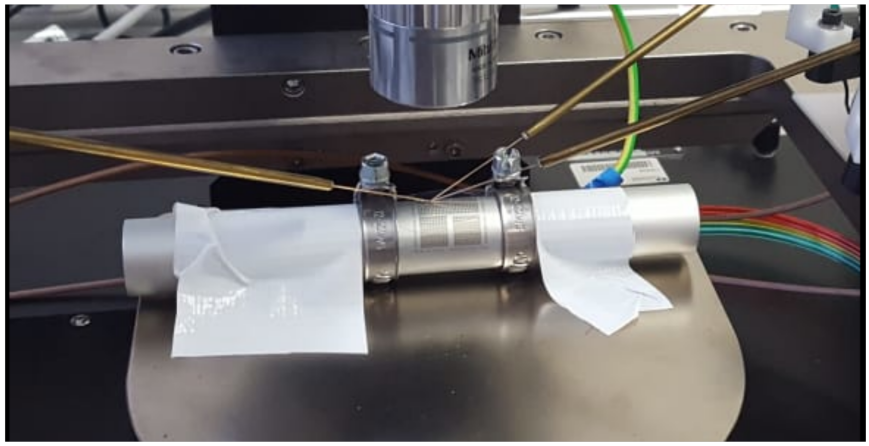
During part A of the experiment, the effects of the mechanical bending on the current-voltage characteristics of the TFTs were evaluated. These measurements were performed on substrate 1. The measurement protocol comprised the following sequence of steps:

Step-1-flat (F1): The substrate was placed flat onto the wafer chuck of the probe station, and the transfer characteristics of 20 nominally identical TFTs of each channel length were measured (drain current measured as a function of the gate-source voltage (V_{GS}, swept from 0 to −3.0 V with a step size of −50 mV) for a drain-source voltage (V_{DS}) of −3.0 V).

Step-1-bent (B1): The substrate was attached to the outside of a cylindrical tube with a diameter of 20 mm, and the transfer characteristics of 20 nominally identical TFTs of each channel length on which no electrical characterization had been performed up to this point were measured under bending stress.



(a)



(b)

Figure 6.1.: (a) Schematic cross-section of organic TFTs fabricated in the inverted coplanar (bottom-gate, bottom-contact) device architecture on a flexible polymeric substrate. Mechanical bending is performed in the direction perpendicular to the path of the electric current in the transistor channel. (b) Photograph of the bending experiment. The substrate is attached to the outside of a cylindrical tube with a diameter of 20 mm.

Step-2-flat (F2): The substrate was placed flat onto the wafer chuck, and the transfer characteristics of 20 nominally identical TFTs of each channel length on which no electrical characterization had been performed up to this point were measured.
Step-2-bent (B2): The procedure of Step-1-bent was repeated.
During steps B1 and B2, the substrate remained in the bent state for 36 hours, and bending was performed in the direction perpendicular to the path of the electrical current in the transistor channel. All measurements were performed in ambient air at room temperature.

6.2.2 Experimental (part B)

During part B of the experiment, the bending-induced degradation of the TFT performance was compared to the possible (bending-independent) degradation caused by aging [66]. These measurements were performed by repeatedly applying the measurement protocol described above to TFTs on substrates 2 and 3, starting on day zero (D0) and repeating the same measurements after two (D2), four (D4), seven (D7) and eleven days (D11). On each of these days, 10 adjacent fresh TFTs with a channel length of 40 µm were measured in the flat state. Between measurements, substrate 2 was stored in the bent state (attached to the outside of the cylindrical tube), while substrate 3 remained in the flat state. The substrates were stored (and all measurements were performed) in ambient air at room temperature.

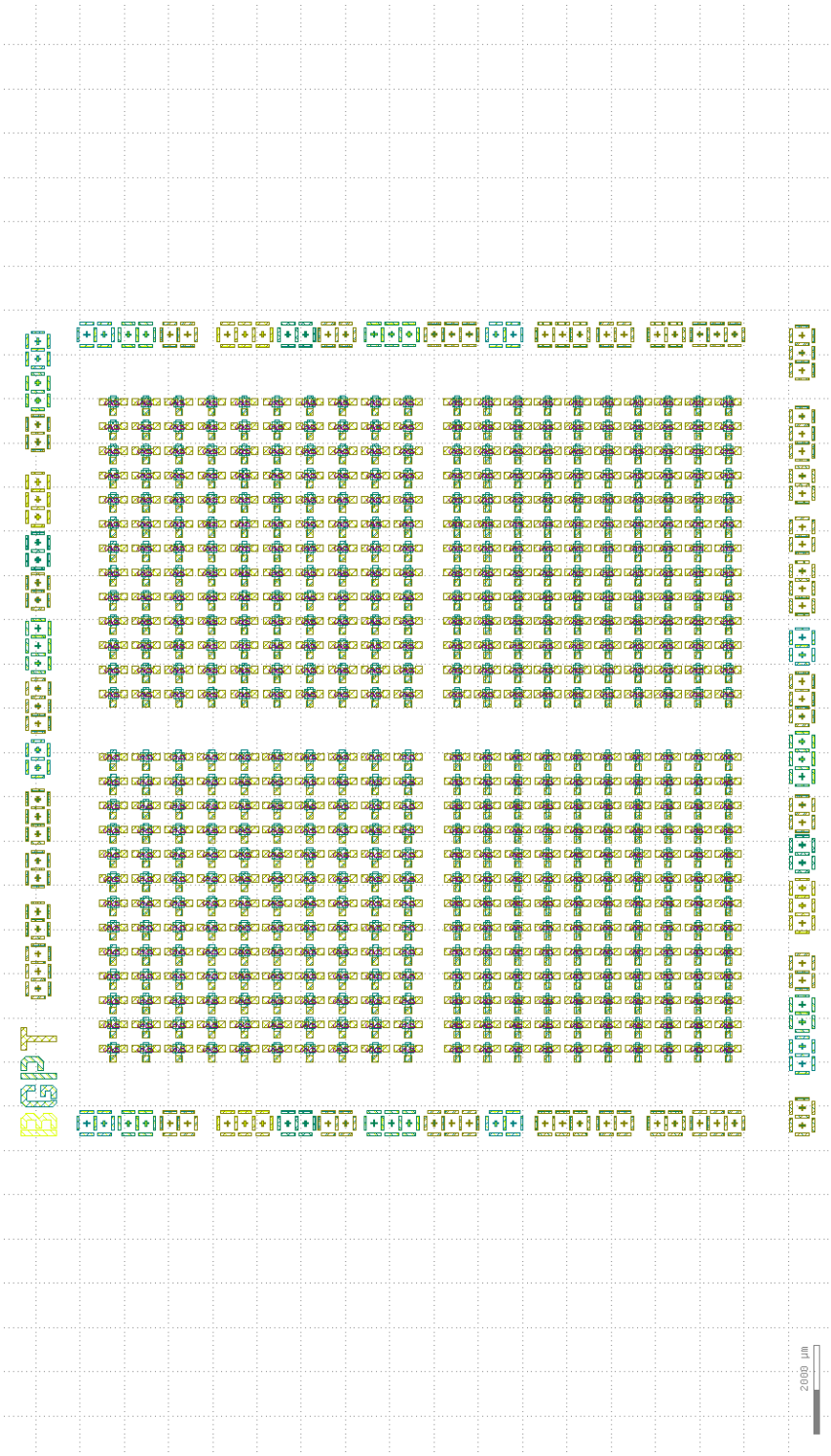


Figure 6.2.: Actual layout of the polyimide shadow masks designed for the organic TFT.

6.3 Effect of Bending on the OSC

In this section, the effect of mechanical bending on the charge-carrier mobility in the organic semiconductor will be discussed. The analysis is based on the model for the hopping conductivity in disordered semiconductors described in [67], in conjunction with the impact of bending on the characteristic temperature T_0 of the organic semiconductor (Fig. 6.3(a)). For n-channel organic semiconductors, the trap distribution near the LUMO level can be modeled as a Gaussian density of states (DOS), $\Gamma(E)$ [11]. The shape of the tail of the DOS is described by the characteristic temperature T_0 [68] (Fig. 6.3(b)). It is assumed that $\Gamma(E)$ describes only traps that contribute to the current flow and which are thus taken into consideration even if they do not satisfy equation 4.8 in [67] together with a neighboring trap. At the lower end of the tail of $\Gamma(E)$, the DOS is expected to be small, so that only a few traps satisfy equation 4.8 in [67] or $R_{ij} < R_{max}$ [67], where R_{ij} is the distance between localized states and R_{max} is the critical distance that characterizes the critical conductance between two sites in the context of the hopping conductivity model [67]. Nevertheless, due to the Fermi distribution, most of these states are occupied and thus contribute to the current flow. Conversely, at higher energy levels, the DOS is larger, so that a larger number of traps satisfy equation 4.8 in [67], but fewer states are occupied. Upon mechanical bending, the distance R_{ij} between localized states is expected to increase [32]. At the lower end of the tail of the $\Gamma(E)$ distribution, the density of traps at a distance $R_{ij} < R_{max}$ will decrease substantially, since the DOS at these energies is already small even without bending. The DOS at higher energy levels will also be reduced by the bending, but the density of localized states having a distance of $R_{ij} < R_{max}$ will still be large. In this way, the shape of $\Gamma(E)$ will change due to bending. At the lower tail, a large number of traps will be removed from the subset of traps that satisfy equation 4.8 in [67]. At higher energy levels, the DOS is high, so that a large number of traps will continue to satisfy equation 4.8 in [67], even during bending. In conclusion, bending is expected to narrow the tails of $\Gamma(E)$) in the organic semiconductor, an event that will manifest itself as a decrease of T_0 according to (Fig. 6.3(b)).

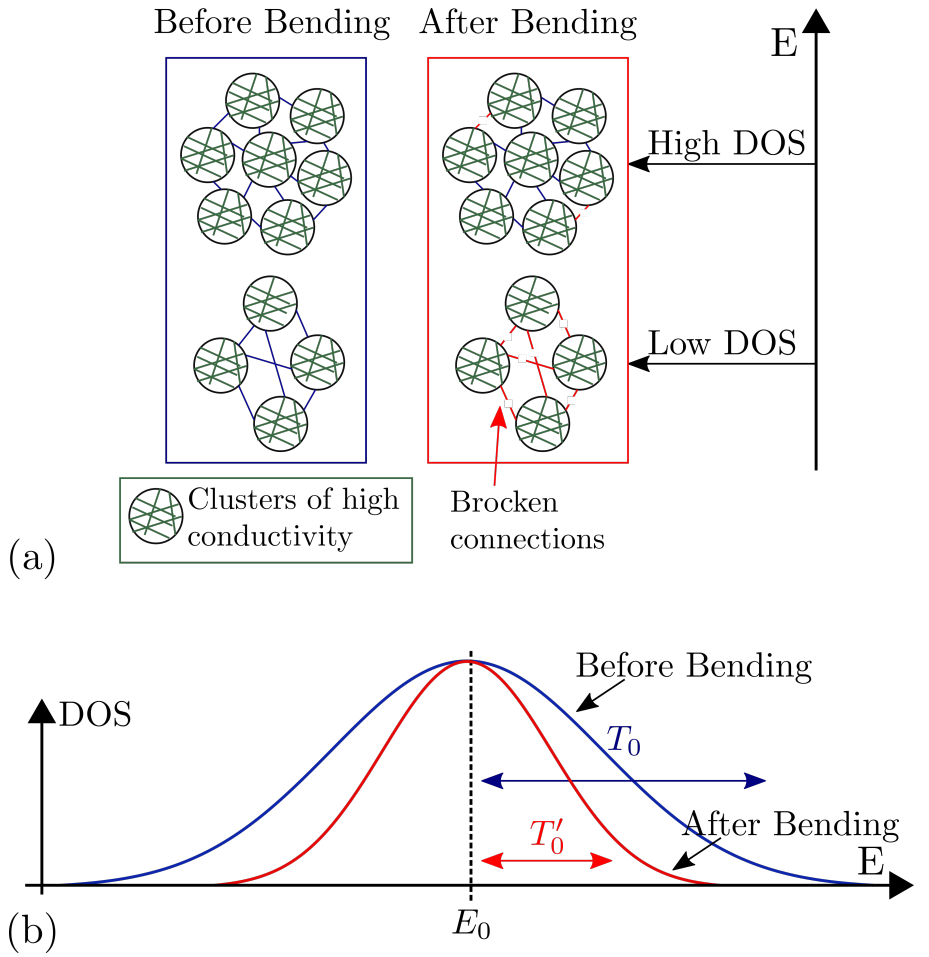


Figure 6.3.: (a) Schematic representation of a resistance network as proposed in [67] (percolation problem) applied to an organic semiconductor. This network is composed of (1) isolated regions of high conductivity (clusters) that do not limit the overall conductance; (2) a relatively small number of resistors connecting a subset of clusters to form an infinite network that spans the entire system; (3) remaining resistors with low conductivity that can be neglected. (b) Narrowing of the tails of the Gaussian DOS due to the bending of the flexible substrate. The characteristic temperature T_0 (prior to bending) is decreased to T_0' upon bending.

6.4 Verification by Physics-Based Compact Model

To validate the effects of bending on the current-voltage characteristics of the TFTs and on the characteristic temperature T_0, the charge-based organic-TFT model introduced in [11] and extended in [36, 37] and [15] is employed here. This model provides a single current equation that is valid for all operation regions that can be obtained from

$$I_{DS} = \mu W \left(\frac{kT}{q} \frac{Q_S - Q_D}{L} + \frac{Q_S^2 - Q_D^2}{2LC'_{ox}} \right) \times \left(1 + \lambda \left(V_{DS} - V_{Dsat}\right)\right), \tag{6.1}$$

where W is the channel width, L is the channel length, C'_{ox} is the unit-area gate-dielectric capacitance, and λ is the channel-length modulation factor. The effective carrier-mobility μ, which is described by the typical power-law mobility, is given by

$$\mu = \mu_0 \left(Q_S / C'_{ox}\right)^{\beta}, \tag{6.2}$$

where μ_0 is the low-field mobility and β is the unitless exponent of the power law. Furthermore, parameter β is related to the characteristic temperature T_0 according to the following equation [68]:

$$\beta = 2 \left(\frac{T_0}{T} - 1 \right). \tag{6.3}$$

Q_S and Q_D are the densities of quasi-mobile charges per gate area at the source and drain ends of the channel, respectively, and can be expressed as

$$Q_{S,D} = \frac{S}{\ln(10)} C'_{ox} \mathcal{L} \left\{ \exp\left(\frac{V_{GS,D} - V_{T0}}{S/\ln(10)} \right) \right\}, \tag{6.4}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, S is the subthreshold swing, and V_{T0} is the threshold voltage.

The numerical values of the compact-model parameters were extracted as follows: The mean-value ($E[I_{DS}]$) transfer characteristics were obtained from the current-voltage characteristics acquired during each step of parts A and B

of the experiment, by calculating the sample mean of the drain current I_{DS} at every gate-source voltage. Next, the parameter sets that specify the mean-value model cards of steps F1 and D0 were derived, by fitting the compact model to the corresponding mean-value transfer characteristics. Note that in the case of part A of the experiment, separate parameter sets were extracted for the TFTs having different channel lengths. In all cases, the parameter μ was calculated by fitting the model to the transfer characteristics measured for the maximum gate-source voltage ($V_{GS} = -3.0\,\mathrm{V}$). The expected degradation of the effective mobility μ caused by the bending was captured for each step of the experiment by modifying the value of parameter β. This is in agreement with the physical explanation of the bending effect on organic TFTs as described in Section III. The characteristic temperature T_0 and the parameter β are correlated according to Equation (3). Specifically, during each step (B1, F2, B2 during part A; D2, D4, D7, D11 during part B of the experiment), the parameter β was fitted anew, while the values of all other model card parameters remained constant. Note that in order to fine-tune the fitting of the compact model to the experimental data, the numerical values of the parameters V_{TO} (threshold voltage) and μ_0 (low-field mobility) were readjusted slightly.

6.5 Results and Discussion

Fig. 6.4 ans 6.5 show the mean-value transfer characteristics and the transconductance g_m of the TFTs measured during part A of the experiment (substrate 1). Experimental measurement data and simulation results are shown as symbols and lines, respectively. During the transition from the flat state to the bent state (i.e., from F1 to B1 and from F2 to B2) and vice versa (from B1 to F2), the on-state drain-current (I_{ON}) and the transconductance (g_m) degraded by about 14%.

Fig. 6.6 and 6.7 show the mean-value transfer characteristics and the transconductance of the TFTs recorded during part B of the experiment (substrates 2 and 3). Experimental measurement data and simulation results are shown as symbols and lines, respectively. In each plot, the results from day 0 (D0) to day 11 (D11) are included.

Table 6.1 summarizes the values of the effective carrier mobility (μ) of the TFTs measured during part A of the experiment (substrate 1) in the flat state and in the bent state (steps F1, B1, F2, B2). The values were extracted from the measurement data with the help of the current-voltage model.

Tables 6.2 and 6.3 summarize the effective carrier mobilities measured during part B of the experiment (substrates 2 and 3). These measurements were performed in the flat state. Table II shows that from day 0 to day 11, the carrier mobility of the TFTs on substrate 2 (which was stored in the bent state between measurements) degraded by 46%, whereas the carrier mobility of the TFTs on substrate 3 (which was kept in the flat state and thus degraded only due to aging) degraded by 22%.

Fig. 6.8 (a) and (b) illustrate the evolution of the mean-value drain current $E[I_{DS}]$ and of the transconductance g_m from day 0 to day 11 (part B of the experiment). Experimental measurement data and simulation results are shown as symbols and lines, respectively, and both are in good agreement. The TFTs stored in the bent state between measurements (substrate 2), degraded by 30%. The evolution of the of the subthreshold slope and of the mobility power-law factor β are illustrated in Fig. 6.9 (c) and (d).

Fig. 6.10 (a) shows the evolution of the effective carrier mobility μ (left vertical axis) and of the characteristic temperature T_0 at $T = 300\,\mathrm{K}$ (right vertical axis) during part B of the experiment (substrates 2 and 3). In Fig. 6.10 (b), the estimated value of the low-field mobility μ_0 is shown.

Table 6.1.: Setup-A: Extracted effective mobility values

L(µm)	μ_{flat} (cm^2/Vs)	μ_{bent} (cm^2/Vs)	$\delta\mu/\mu_{flat} \times 100$
[Step 1]			
40	1.68	1.44	−14.2%
20	1.34	1.15	−14.3%
[Step 2]			
40	1.1	0.93	−15.5%
20	0.83	0.71	−14.5%

Table 6.2.: Setup-B [SUB #2]: Extracted mobility values

Day interval	$\mu_{D[N]}$ (cm^2/Vs)	$\mu_{D[N+k]}$ (cm^2/Vs)	$\delta\mu/\mu_{D[N]}$ $\times 100$
$0 \rightarrow 2$	3.51	3.06	-12.8%
$2 \rightarrow 4$	3.06	2.60	-15.0%
$4 \rightarrow 7$	2.60	2.25	-13.5%
$7 \rightarrow 11$	2.25	1.90	-15.6%
$\mathbf{0 \rightarrow 11}$	**3.51**	**1.90**	$\mathbf{-45.9\%}$

Table 6.3.: Setup-B [SUB #3]: Extracted mobility values

Day interval	$\mu_{D[N]}$ (cm^2/Vs)	$\mu_{D[N+k]}$ (cm^2/Vs)	$\delta\mu/\mu_{D[N]}$ $\times 100$
$0 \rightarrow 2$	3.83	3.36	-12.3%
$2 \rightarrow 4$	3.36	3.21	-4.4%
$4 \rightarrow 7$	3.21	3.14	-2.2%
$7 \rightarrow 11$	3.14	2.98	-5.1%
$\mathbf{0 \rightarrow 11}$	**3.83**	**2.98**	$\mathbf{-22.2\%}$

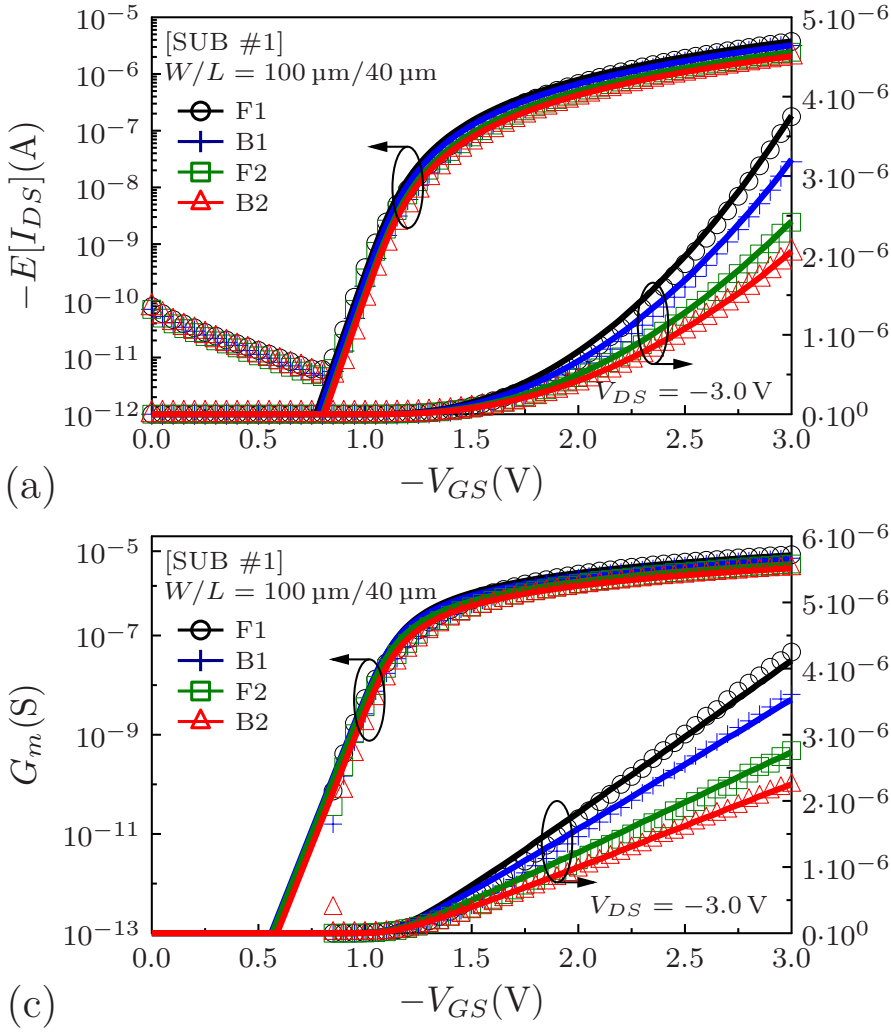


Figure 6.4.: Mean-value drain current $E[I_{DS}]$ and transconductance G_m versus gate-source voltage V_{GS} of the TFTs with channel lengths of (a, c) 40 µm and (b, d) 20 µm. The current-voltage characteristics were recorded during part A of the experiment (steps F1, B1, F2 and B2), with the TFTs biased in saturation ($V_{DS} = -3.0\,V$). Symbols: Values calculated from experimental data. Lines: Simulation results.

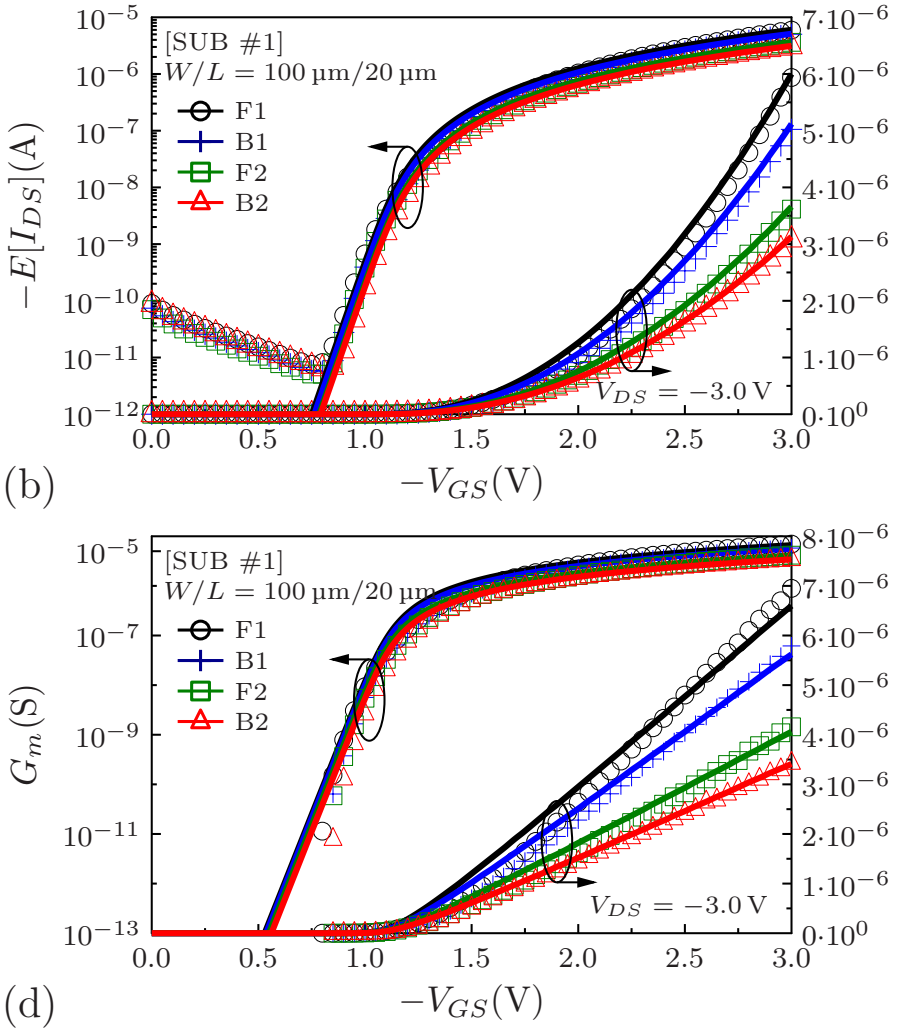


Figure 6.5.: Mean-value drain current $E[I_{DS}]$ and transconductance G_m versus gate-source voltage V_{GS} of the TFTs with channel lengths of (a, c) 40 µm and (b, d) 20 µm. The current-voltage characteristics were recorded during part A of the experiment (steps F1, B1, F2 and B2), with the TFTs biased in saturation ($V_{DS} = -3.0$ V). Symbols: Values calculated from experimental data. Lines: Simulation results.

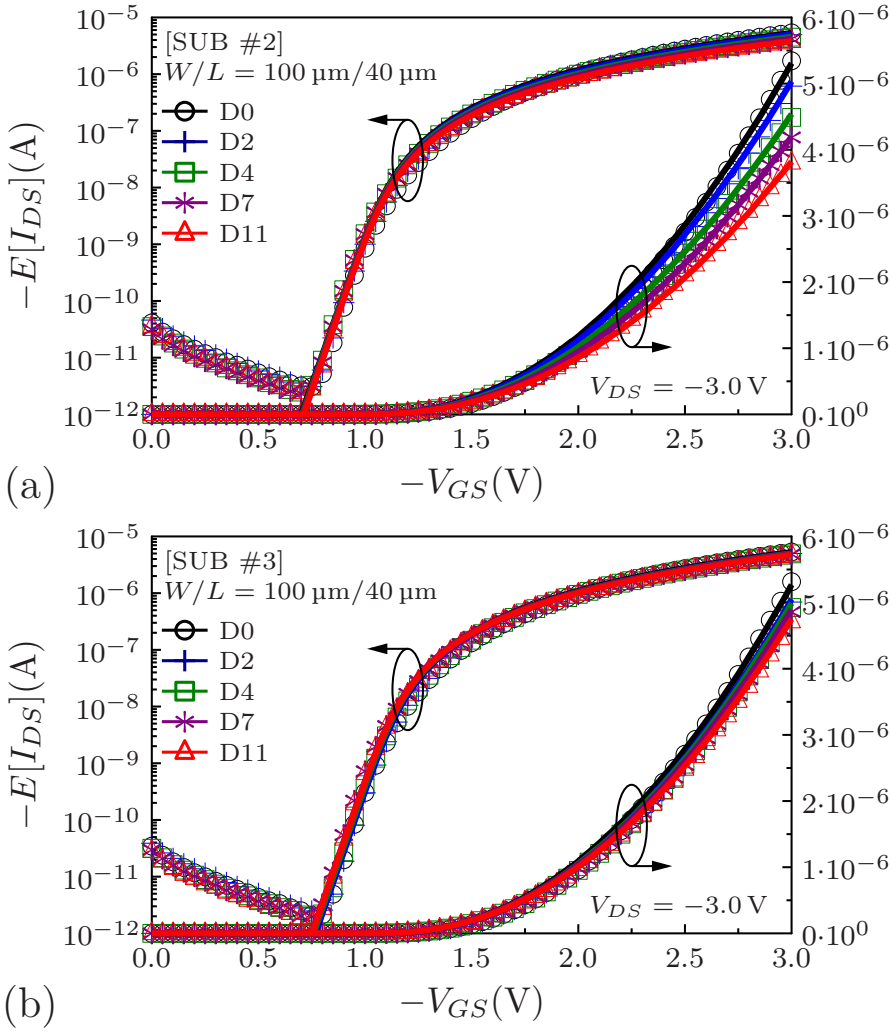


Figure 6.6.: Mean-value drain current $E[I_{DS}]$ and transconductance G_m versus gate-source voltage V_{GS} of the TFTs with a channel length 40 µm. The current-voltage characteristics were recorded during part B of the experiment on substrate 2 (graphs (a) and (c)) and substrate 3 (graphs (b) and (d)). Symbols: Values calculated from experimental data. Lines: Simulation results.

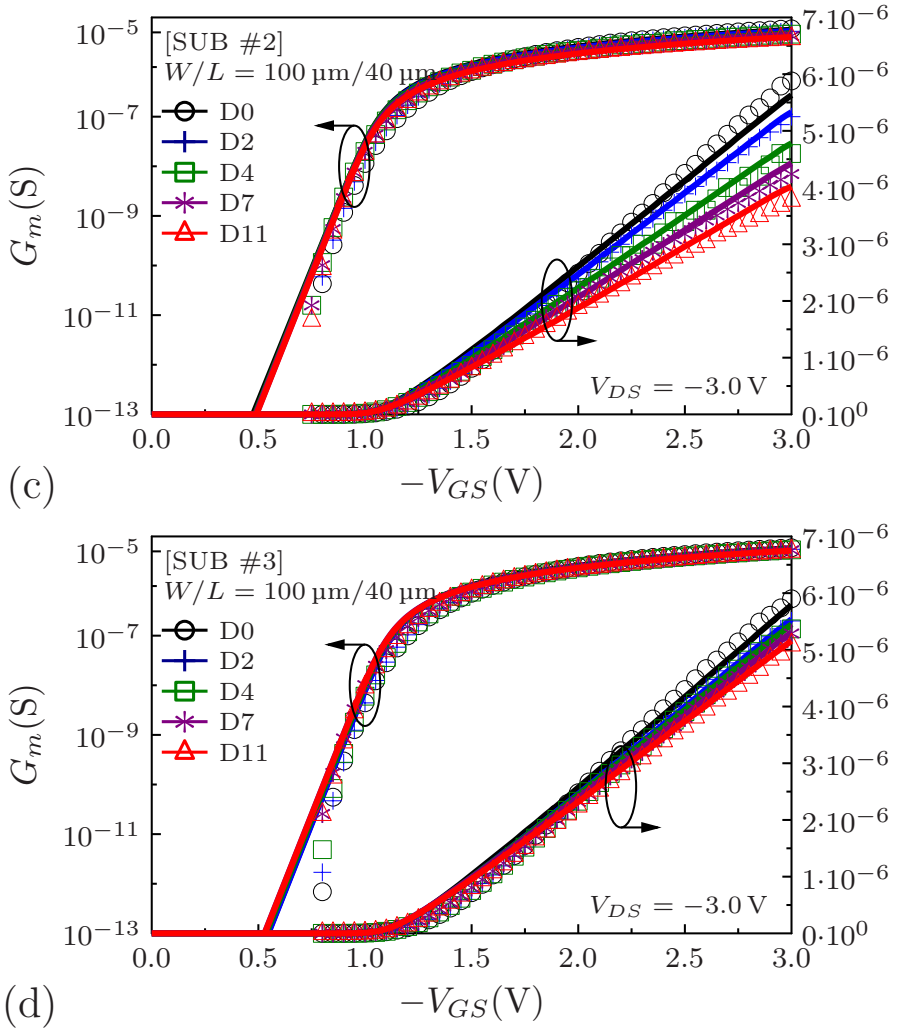


Figure 6.7.: Mean-value drain current $E[I_{DS}]$ and transconductance G_m versus gate-source voltage V_{GS} of the TFTs with a channel length 40 µm. The current-voltage characteristics were recorded during part B of the experiment on substrate 2 (graphs (a) and (c)) and substrate 3 (graphs (b) and (d)). Symbols: Values calculated from experimental data. Lines: Simulation results.

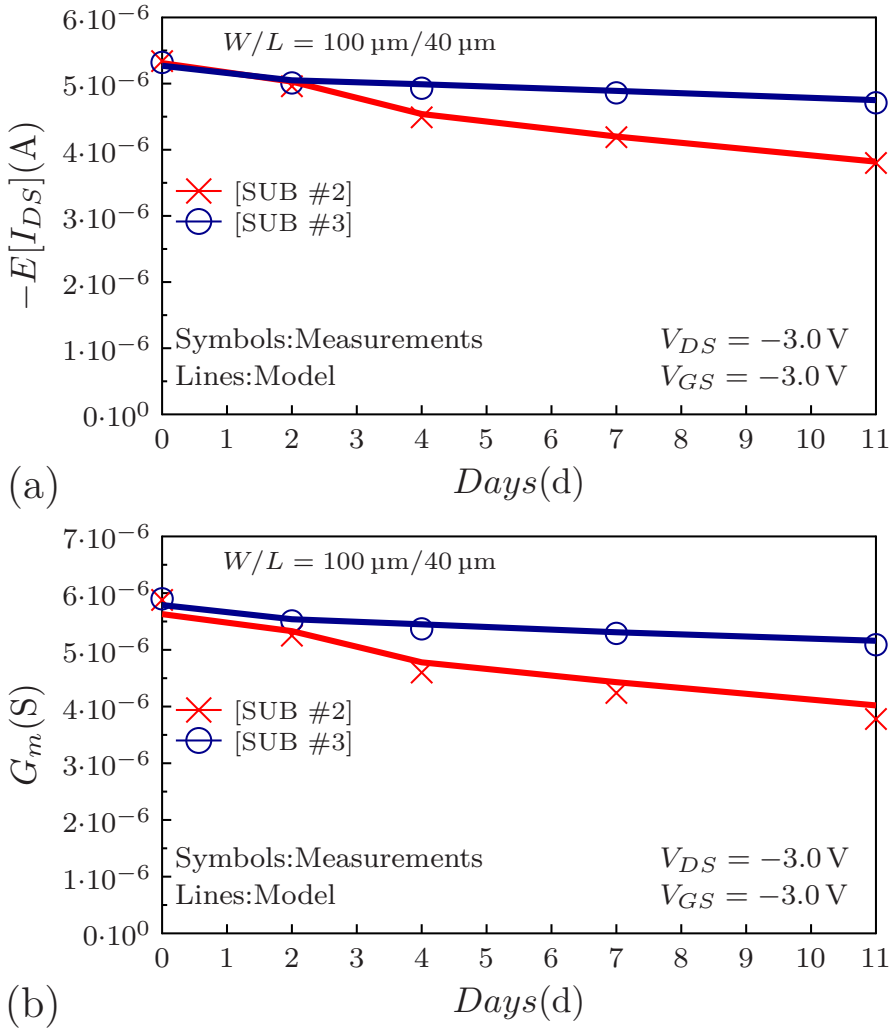


Figure 6.8.: Evolution of (a) the mean-value drain current $E[I_{DS}]$ and (b) the transconductance G_m of the TFTs with a channel length of 40 µm. The measurements were performed during part B of the experiment on substrates 2 and 3. Symbols: Values calculated from experimental data. Lines: Simulation results.

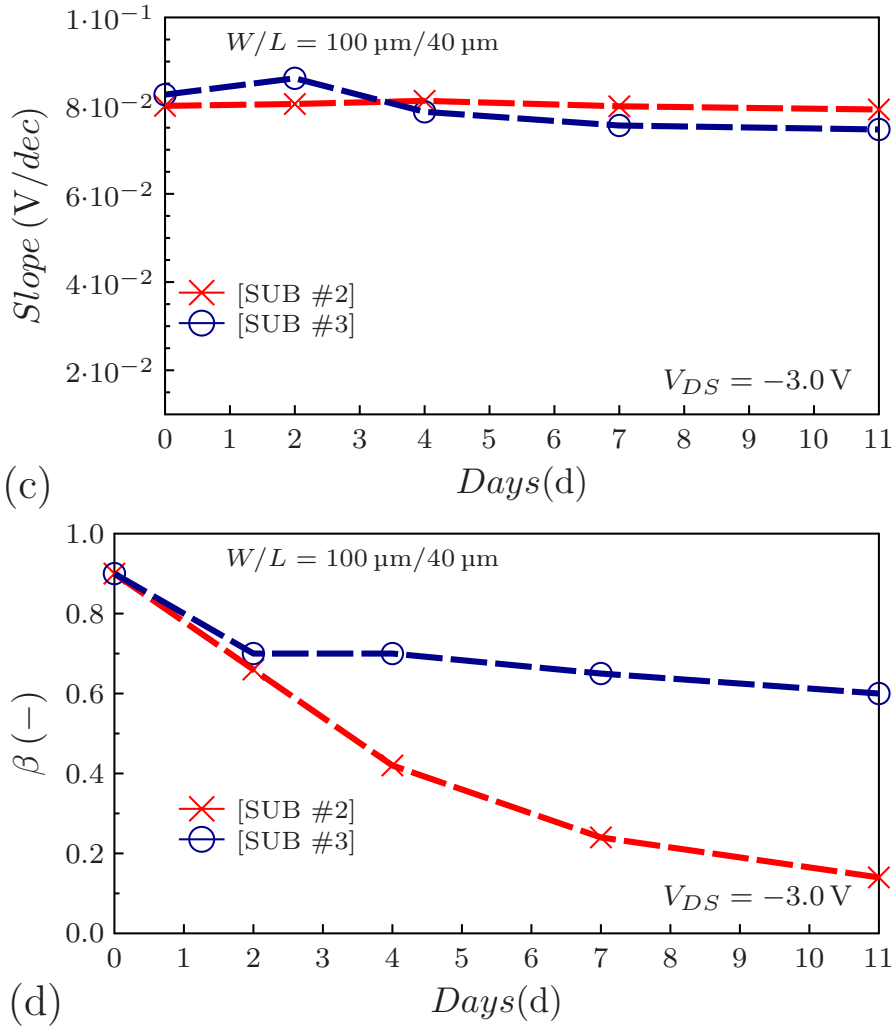


Figure 6.9.: Evolution of (a) the mean-value drain current $E[I_{DS}]$ and (b) the transconductance G_m of the TFTs with a channel length of 40 µm. The measurements were performed during part B of the experiment on substrates 2 and 3. Symbols: Values calculated from experimental data. Lines: Simulation results. (c) Subthreshold slope and mobility power law factor β.

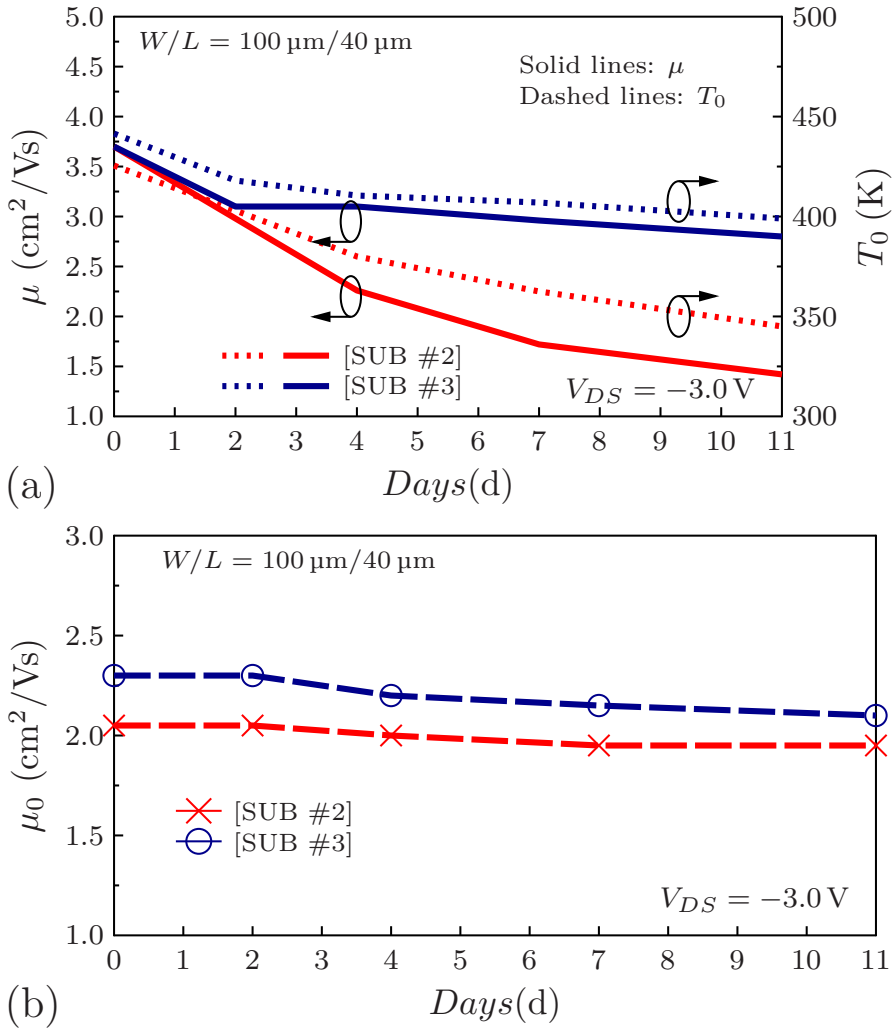


Figure 6.10.: (a) Evolution of the effective carrier mobility μ (left vertical axis) and the characteristic temperature T_0 at $T = 300\,\mathrm{K}$ (right vertical axis). The measurements were performed during part B of the experiment on substrates 2 and 3. Solid lines: Effective carrier mobility μ. Dashed lines: characteristic temperature T_0. (b) Evolution of the estimated low-field carrier mobility μ_0.

6.6 Conclusions

In conclusion, we have investigated how the performance of organic TFTs changes when they are subjected to mechanical bending. For this purpose, a large number of nominally identical TFTs were fabricated on three substrates. In the first part of the experiment (part A; substrate 1), we found that the transition from the flat state to the bent state (i.e., from F1 to B1 and from F2 to B2) and vice versa (from B1 to F2) causes a degradation of the on-state drain current of the TFTs by about 14%, along with a small threshold-voltage shift. Under the bending-induced mechanical strain, the energy barrier for charge-carrier hopping increases due to the larger distance between the molecules in the organic semiconductor layer, which causes a decrease of the charge-carrier mobility [32]. Prior to bending, charge transport in the organic semiconductor can mainly be attributed to hopping transport via localized states at lower energies, described by an exponential tail with a characteristic temperature T_0 of the Gaussian DOS. Bending causes the distance between the localized states to increase [67], which results in broken connections between localized states at lower energies, which in turn leads to the localized states at higher energies (where the DOS is larger) to contribute mainly to the charge transport. Thus, the characteristic temperature is expected to decrease (T_0'). The compact model utilized here [11] is able to capture this effect by adjusting the value of the power-law exponent parameter β.

In part B of the experiment, we investigated how much of the performance degradation observed during the bending tests was caused by the bending itself and how much was caused instead by the (bending-independent) device aging. We found that the charge-carrier mobility degraded by 46% when the TFTs were subjected to both bending and aging (substrate 2), compared to 22% when the TFTs were subjected only to aging, but not to bending (substrate 3). The compact-model parameters threshold voltage, subthreshold slope and low-field mobility extracted from the TFTs that had been subjected to bending and aging (substrate 2) are similar to the values extracted from the TFTs that had been subjected only to aging, but not to bending (substrate 3). This is in line with the fact that the drain-current degradation in the TFTs under bending stress

can be mainly attributed to the degradation of the effective carrier mobility, caused by a decrease of the characteristic temperature of the exponential tail of the DOS in the organic semiconductor. In all cases, the results of the compact model utilized here are in good agreement with the measurement results.

CHAPTER 7

Conclusion

In conclusion, in the current PhD thesis, a significant amount of research regarding topics that cover modeling aspects of variability of organic TFTs were presented. For verification reasons, seven flexible substrates containing organic TFTs and TFT-based circuits were fabricated and tested, accordingly. A physical charge-based drain-current variability model suitable for organic thin-film transistors was developed and verified, as the core of this research. The proposed model is based on charge-carrier-number-fluctuation and correlated-mobility-fluctuation effects and can be applied to TFTs fabricated in the coplanar or the staggered device architecture. Regardless of the channel dimensions and the device architecture, the results of the proposed model are in good agreement with the experimentally measured bias-dependent drain-current variability of organic TFTs.

Subsequently, an efficient alternative to the Monte Carlo statistical-analysis methodology that can be used for the variability study of integrated circuits has been presented. The proposed "Noise-Based Variability Approach" (NOVA) method has been tested on circuits based on organic TFTs and has been shown to be suitable for fast process and mismatch statistical circuit analyses. The principle advantage of NOVA over Monte Carlo is the significantly shorter processing time, which makes NOVA beneficial for circuit designers.

Next, a semi-physical bias-dependent charge-based low-frequency noise model for organic thin-film transistors, a topic relevant to compact modeling of vari-

ability aspects, was implemented. The proposed model is based on charge carrier-number fluctuation-correlated mobility fluctuation (ΔN) and mobility-fluctuation (Hooge) ($\Delta\mu$) effects, and it can be applied to TFTs fabricated in the inverted staggered device architecture.

As described in Chapter 5, using experimental data obtained from TFT-based current mirrors, the variability of the circuit characteristics were analyzed. For this purpose, a large number of nominally identical current mirrors were fabricated and characterized. The layout of the test structures was implemented from the author specifically to study variability and mismatch issues that occur in the electrical characteristics of organic TFTs. The statistical behavior of the TFT-based current mirrors, quantified here in terms of the mean value and the standard deviation of the reference and output currents, are similar to those of the discrete TFTs. The drain-current mismatch of the current-mirrors can vary from 1% to $\sim 25\%$ based on the circuit biasing conditions.

Finally, the performance of organic TFTs changes when they are subjected to mechanical bending was investigated. Under the bending-induced mechanical strain, the energy barrier for charge-carrier hopping increases due to the larger distance between the molecules in the organic semiconductor layer, which causes a decrease of the charge-carrier mobility [32]. Prior to bending, charge transport in the organic semiconductor can mainly be attributed to hopping transport via localized states at lower energies, described by an exponential tail with a characteristic temperature T_0 of the Gaussian DOS. Bending causes the distance between the localized states to increase [67], which results in broken connections between localized states at lower energies, which in turn leads to the localized states at higher energies (where the DOS is larger) to contribute mainly to the charge transport. Thus, the characteristic temperature is expected to decrease. The DC compact model utilized in the current manuscript [11] is able to capture this effect by adjusting the value of the power-law exponent parameter β. In all cases, the results of the compact model utilized here are in good agreement with the measurement results.

APPENDIX A

Analytical Model for Transconductances of Long-Channel Organic Thin-Film Transistors

In the current paper, an analytical model for predicting the transconductances of long-channel organic thin-film transistors is presented. The proposed model is verified using experimental data of p-channel DNTT TFTs in the inverted staggered device architecture [69].

A.1 Devices and Measurements

The experimental p-channel organic TFTs have nominal channel widths (W) of 400 µm and nominal channel lengths (L) of 200, 100 and 80 µm. The TFTs were fabricated on a flexible polyethylene naphthalate (PEN) substrate with a thickness of 125 µm in the inverted staggered (bottom-gate, top-contact) device architecture, using stencil lithography based on high-resolution silicon stencil masks (Fig. A.1) [45]. The TFTs consist of 30-nm-thick aluminum gate electrodes, a 5.3-nm-thick hybrid AlO_x/SAM gate dielectric, 25-nm-thick gold (Au) source and drain contacts and a 11-nm-thick vacuum-deposited layer of the small-molecule semiconductor dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [69]. The maximum process temperature was 90 °C. The transfer characteristics of all TFTs were recorded at room temperature by applying a drain-source voltage (V_{DS}) of −2.0 V and sweeping the gate-source voltage (V_{GS}) from 0 to −2.0 V with a step size of −30 mV.

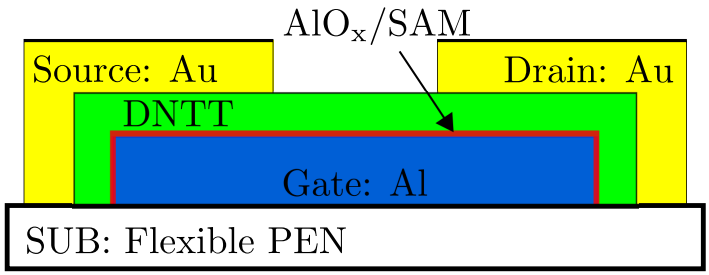


Figure A.1.: Schematic cross-section of the organic TFTs fabricated in the inverted staggered (bottom-gate, top-contact) architecture [45].

A.2 Normalized Q(V) function

Following [11] the total mobile charge at any point of the channel can be expressed as

$$Q_{CH} = \frac{S}{ln10} C'_{ox} LambertW \left\{ e^{\left(\frac{V_G - V_{CH} - V_{TO}}{S/ln10} \right)} \right\} \tag{A.1}$$

where

$$S = aln(10)U_T, \tag{A.2}$$

a is the subthreshold slope factor and $U_T \triangleq kT/q$ is the thermal voltage. Please note that Q_{CH} is the absolute value of the mobile charge. Charges and voltages can be normalized according to

$$\frac{Q_{CH}}{q_{ch}} = \frac{Q_D}{q_d} = \frac{Q_S}{q_s} = Q_{sp} \tag{A.3}$$

and

$$\frac{V_{CH}}{v_{ch}} = \frac{V_D}{v_d} = \frac{V_S}{v_s} = aU_T \tag{A.4}$$

respectively, where

$$Q_{sp} \triangleq aU_T C'_{ox} \tag{A.5}$$

is the specific charge. By introducing (A.2) into (A.1) and normalizing all charges and voltages the following can be obtained:

$$Q_{CH} = aU_T C'_{ox} LambertW\left\{e^{\left(\frac{V_G - V_{CH} - V_{TO}}{aU_T}\right)}\right\} \Leftrightarrow$$

$$Q_{CH} = aU_T C'_{ox} LambertW\left\{e^{\left(\frac{V_G - V_{TO}}{aU_T} - \frac{V_{CH}}{aU_T}\right)}\right\} \Leftrightarrow$$

$$Q_{CH} = Q_{sp} LambertW\left\{e^{(v_o - v_{ch})}\right\} \Leftrightarrow$$

$$q_{ch} = LambertW\left\{e^{(v_o - v_{ch})}\right\} \Leftrightarrow$$

$$q_{ch} e^{q_{ch}} = e^{(v_o - v_{ch})} \Leftrightarrow$$

$$e^{q_{ch} + lnq_{ch}} = e^{(v_o - v_{ch})} \Leftrightarrow$$

$$\boxed{q_{ch} + lnq_{ch} = v_o - v_{ch}.} \tag{A.6}$$

For a specific value of gate voltage the mobile charge becomes zero for a particular value of V_{CH} called pinch-off voltage V_P.

$$v_p = \frac{V_P}{aU_T} \triangleq v_{ch}\left(q_{ch} + lnq_{ch} = 0\right) = v_{ch}\left(q_{ch} = 0.567143\right). \tag{A.7}$$

For $q_{ch} \ll 1$, the channel is weakly depleted and the linear term of (A.6) becomes negligible. In this case the mobile charge can be approximated by

$$q_{ch} = e^{v_o - v_{ch}}. \tag{A.8}$$

For $q_{ch} \gg 1$, the channel is strongly depleted and the logarithmic term of (A.6) becomes negligible. Therefore, the mobile charge can be approximated by

$$q_{ch} = v_o - v_{ch}. \tag{A.9}$$

A.3 Normalized Q(I) function

Typical drain current model, assuming constant μ, including both drift and diffusion components is given by

$$I_D = \mu \frac{W}{L} \int_{V_S}^{V_D} Q_{CH} dV_{CH}, \tag{A.10}$$

where Q_{CH} is the absolute value of the mobile charge. Equation (A.10) shows that the drain current can be obtained directly from $Q_{CH}(V)$. Furthermore, the result is independent of the shape of $Q_{CH}(V)$. In terms of normalized charges

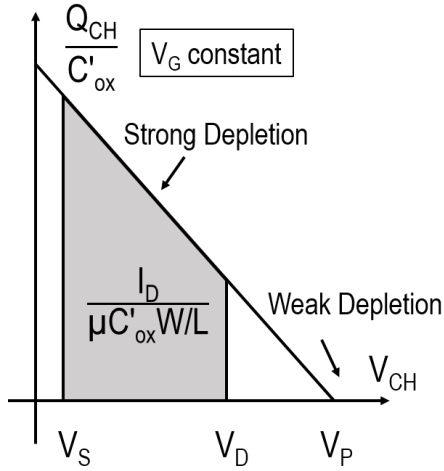


Figure A.2.: Drain current I_D according to (A.10)

and voltages the general drain current expression can be written as

$$I_D = \mu a U_T Q_{sp} \frac{W}{L} \int_{v_s}^{v_d} q_{ch} dv_{ch} = I_{sp} \int_{v_s}^{v_d} q_{ch} dv_{ch}, \tag{A.11}$$

where

$$I_{sp} = \mu a U_T Q_{sp} \frac{W}{L} \overset{Q_{sp}=aU_T C'_{ox}}{=} \mu a^2 U_T^2 C'_{ox} \frac{W}{L}. \tag{A.12}$$

All currents are normalized to I_{sp} according to

$$\frac{I_D}{i_d} = I_{sp}. \tag{A.13}$$

Therefore the normalized general drain current expression can be expressed as

$$i_d = \int_{v_s}^{v_d} q_{ch} dv_{ch}. \tag{A.14}$$

When the drain or source voltage tend to infinity the mobile charge tends to zero. Therefore, (A.14) in terms of forward i_f and reverse i_r current components can be rewritten as

$$i_d = \int_{v_s}^{v_d} q_{ch} dv_{ch} = \int_{v_s}^{\infty} q_s dv_{ch} - \int_{v_d}^{\infty} q_d dv_{ch} = i_f - i_r. \tag{A.15}$$

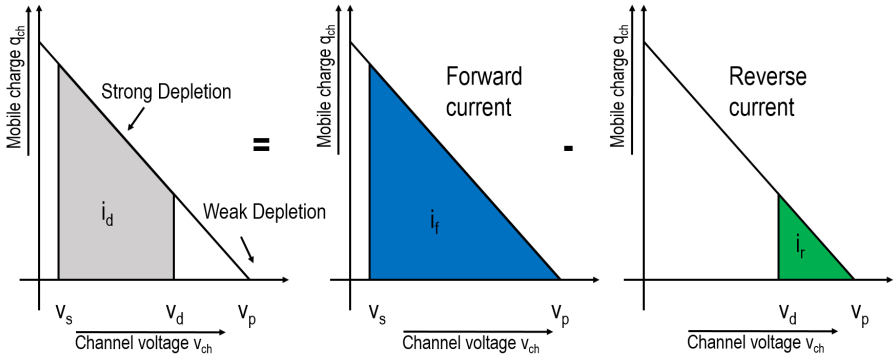


Figure A.3.: Decomposition of normalized drain current i_d into normalized forward i_f and reverse i_r current components

From (A.6) the following can be obtained:

$$\begin{aligned} v_{ch} &= v_o - (q_{ch} + lnq_{ch}) \Leftrightarrow \\ \frac{dv_{ch}}{dq_{ch}} &= -(1 + \frac{1}{q_{ch}}) \Leftrightarrow \\ \frac{dv_{ch}}{dq_{ch}} &= -(\frac{1 + q_{ch}}{q_{ch}}) \Leftrightarrow \\ q_{ch}dv_{ch} &= -(1 + q_{ch})dq_{ch} \end{aligned} \tag{A.16}$$

which when introduced to (A.15) yields

$$i_{f,r} = \int_0^{q_{s,d}} (1 + q_{ch})dq_{ch} = \frac{1}{2}q_{s,d}^2 + q_{s,d}, \tag{A.17}$$

where q_s and q_d are the normalized mobile charges at the source and drain end of the channel respectively. When substituting (A.17) into (A.15) the general normalized drain current equation can be obtained

$$i_d = \left(\frac{1}{2}q_s^2 + q_s\right) - \left(\frac{1}{2}q_d^2 + q_d\right). \tag{A.18}$$

Furthermore, (A.6) can be rewritten as

$$v_o - v_{s,d} = q_{s,d} + lnq_{s,d} \tag{A.19}$$

and by inverting (A.17) the normalized mobile charges q_s and q_d can be expressed as

$$q_{s,d} = \sqrt{2i_{f,r} + 1} - 1. \tag{A.20}$$

By introducing (A.20) into (A.19) the general current-voltage equation can be obtained:

$$v_o - v_{s,d} = \sqrt{2i_{f,r} + 1} + ln(\sqrt{2i_{f,r} + 1} - 1) - 1. \tag{A.21}$$

A.4 Transconductances model

The total variation of drain current ΔI_D with respect to source, drain and gate transconductances can be defined as

$$\Delta I_D = -G_{ms}\Delta V_S + G_{md}\Delta V_D + G_m\Delta V_G. \tag{A.22}$$

G_{ms} depends only on forward current and is independent of the drain voltage V_D, whereas G_{md} depends only on reverse current and is independent of source voltage V_S. Therefore (A.22) can be rewritten as [41, 70]

$$\Delta I_D = \frac{\vartheta I_F}{\vartheta V_S}\Delta V_S - \frac{\vartheta I_R}{\vartheta V_D}\Delta V_D + \{\frac{\vartheta I_F}{\vartheta V_P} - \frac{\vartheta I_R}{\vartheta V_P}\}\frac{\vartheta V_P}{\vartheta V_G}\Delta V_G. \tag{A.23}$$

In Figure 3 the transconductances are identified in the Q-V plot where β is given by

$$\beta = \mu C'_{ox}\frac{W}{L}. \tag{A.24}$$

Small variations of V_S and V_D voltages must be multiplied by the specific values Q_s/C'_{ox} and Q_D/C'_{ox} at the source and drain end of the channel respectively in order to obtain the corresponding variation of the area I_D/β. Therefore, G_{ms} and G_{md} can be expressed as

$$G_{ms} = \frac{\beta}{C'_{ox}}(Q_S) = \mu\frac{W}{L}Q_{sp}q_s = \mu\frac{W}{L}aU_TC'_{ox}q_s = G_{sp}q_s \tag{A.25}$$

and

$$G_{md} = \frac{\beta}{C'_{ox}}(Q_D) = \mu\frac{W}{L}Q_{sp}q_d = \mu\frac{W}{L}aU_TC'_{ox}q_d = G_{sp}q_d, \tag{A.26}$$

where

$$G_{sp} \triangleq \frac{I_{sp}}{aU_T}. \tag{A.27}$$

Forward and reverse current components depend on the differences $V_S - V_P$ and

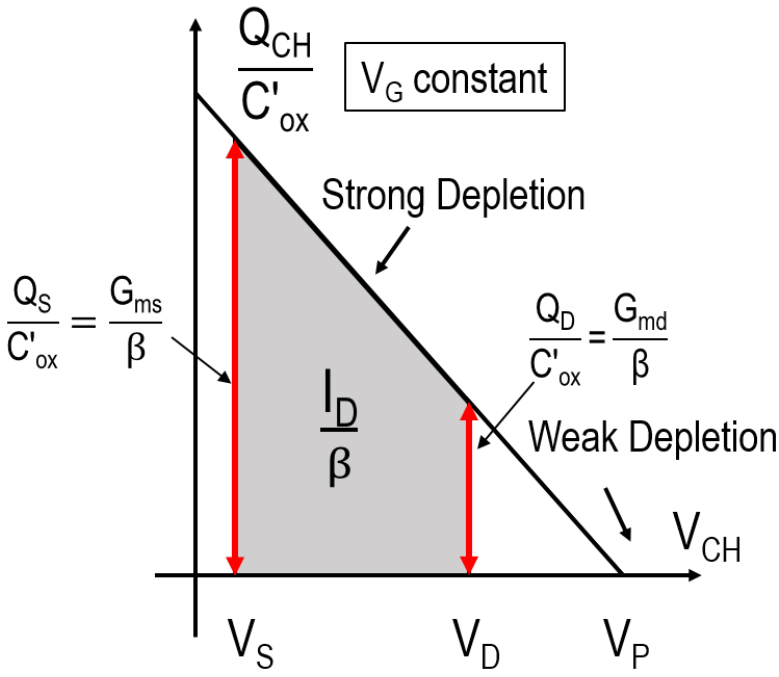


Figure A.4.: Relation between transconductances and mobile charge

$V_D - V_P$ respectively. Consequently, a variation on V_S and V_D will effect equally I_F and I_R with an opposite sign equal variation on V_P. Therefore source and drain transconductances can be expressed as

$$G_{ms,d} = \frac{\vartheta I_{F,R}}{\vartheta V_P}. \tag{A.28}$$

Furthermore according to (A.6), $dV_P/dV_G = 1$ and the expression of G_m in (A.23) can be rewritten as

$$G_m = G_{ms} - G_{md}. \tag{A.29}$$

From (A.20), (A.25) and (A.26) the following can be obtained

$$g_{ms,d} = q_{s,d} = \sqrt{2i_{f,r} + 1} - 1 = \frac{G_{ms,d}}{G_{sp}} \tag{A.30}$$

and

$$g_m = \sqrt{2i_f + 1} - \sqrt{2i_r + 1}. \tag{A.31}$$

Next, the conductance at any point x of the channel will be calculated. The (normalized) voltage-charge and current-charge equations at point x can be expressed as

$$v = v_p - v(x) = q_{ch}(x) + lnq_{ch}(x) \tag{A.32}$$

and

$$i = \frac{1}{2}q_{ch}^2(x) + q_{ch}(x), \tag{A.33}$$

respectively. The normalized conductance at point x is given by

$$g_{ch} = \frac{di}{dv} = \frac{\frac{\partial i}{\partial q_{ch}}}{\frac{\partial v}{\partial q_{ch}}} = \frac{(q_{ch} + lnq_{ch})'}{\left(\frac{1}{2}q_{ch}^2 + q_{ch}\right)'} = q_{ch} \tag{A.34}$$

and from (A.12) and (A.27), the conductance at any point of the channel can be expressed as

$$G_{CH} = \mu \frac{W}{L} (-Q_{ch}). \tag{A.35}$$

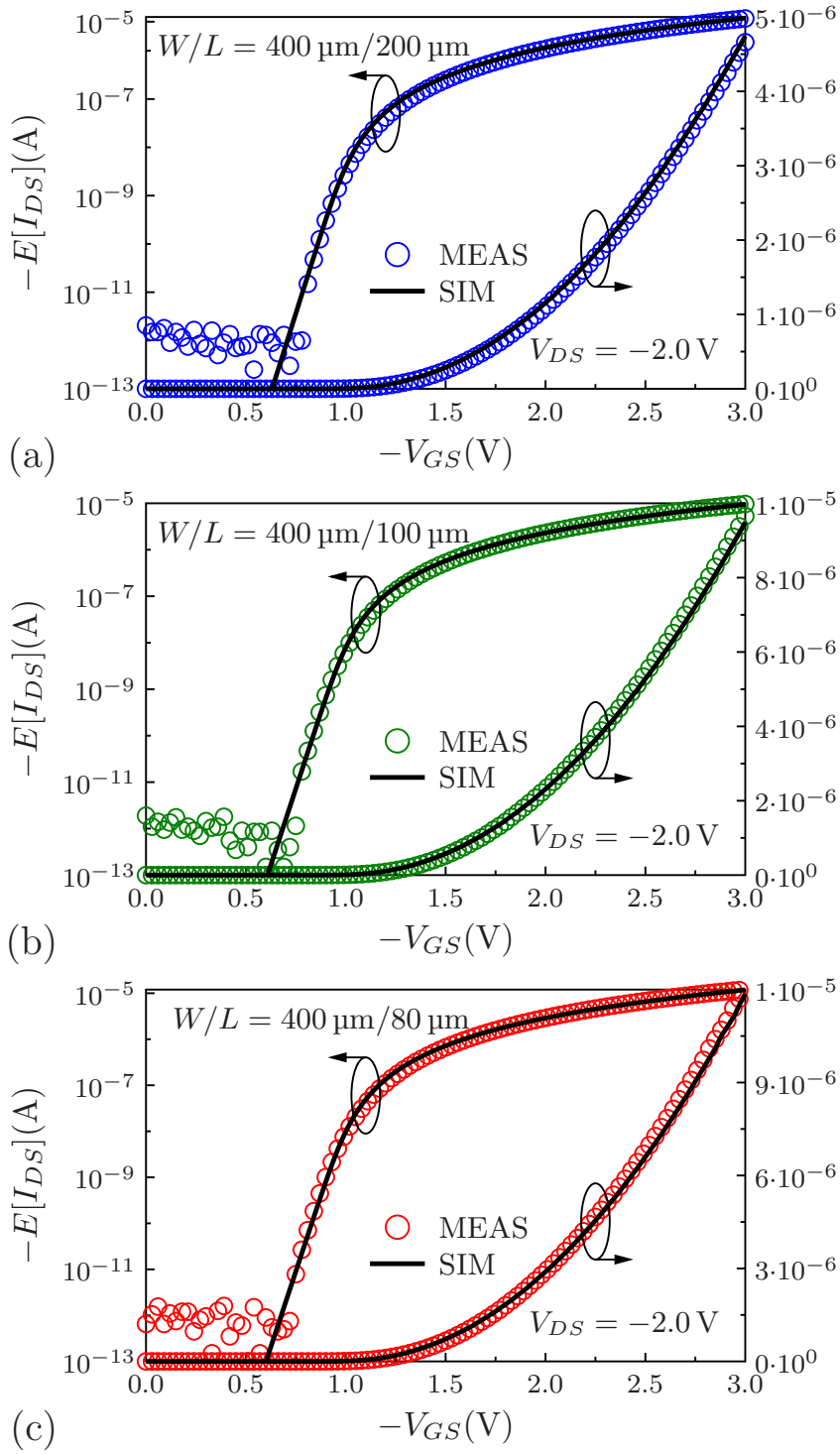


Figure A.5.: Transfer characteristics of p-channel DNTT TFTs with channel widths (W) of 400 µm and channel lengths (L) of (a) 200, (b) 100 and (c) 80 µm. Symbols: Measurements. Lines: Simulation results.

A.5 Results and Discussion

Fig. A.5 shows the measured (Symbols) versus the simulated (Lines) transfer characteristics of the experimental p-channel DNTT TFTs with channel widths (W) of 400 µm and channel lengths (L) of (a) 200, (b) 100 and (c) 80 µm, respectively. The applied current-voltage model consists of one parameter set (A.1) that accurately predicts the current for all the TFTs with different geometries.

In Fig. A.6, the gate transconductance G_m versus the gate voltage V_{GS} of the same TFTs is depicted. Symbols account for the gate transconductance that was derived form the measured data and lines correspond to the model.

Table A.1.: Extracted parameters of the static I-V model

C'_{ox} (F/m^2)	5.6
V_{TO} (V)	0.97
a (−)	1.28
μ (cm^2/Vs)	2.25

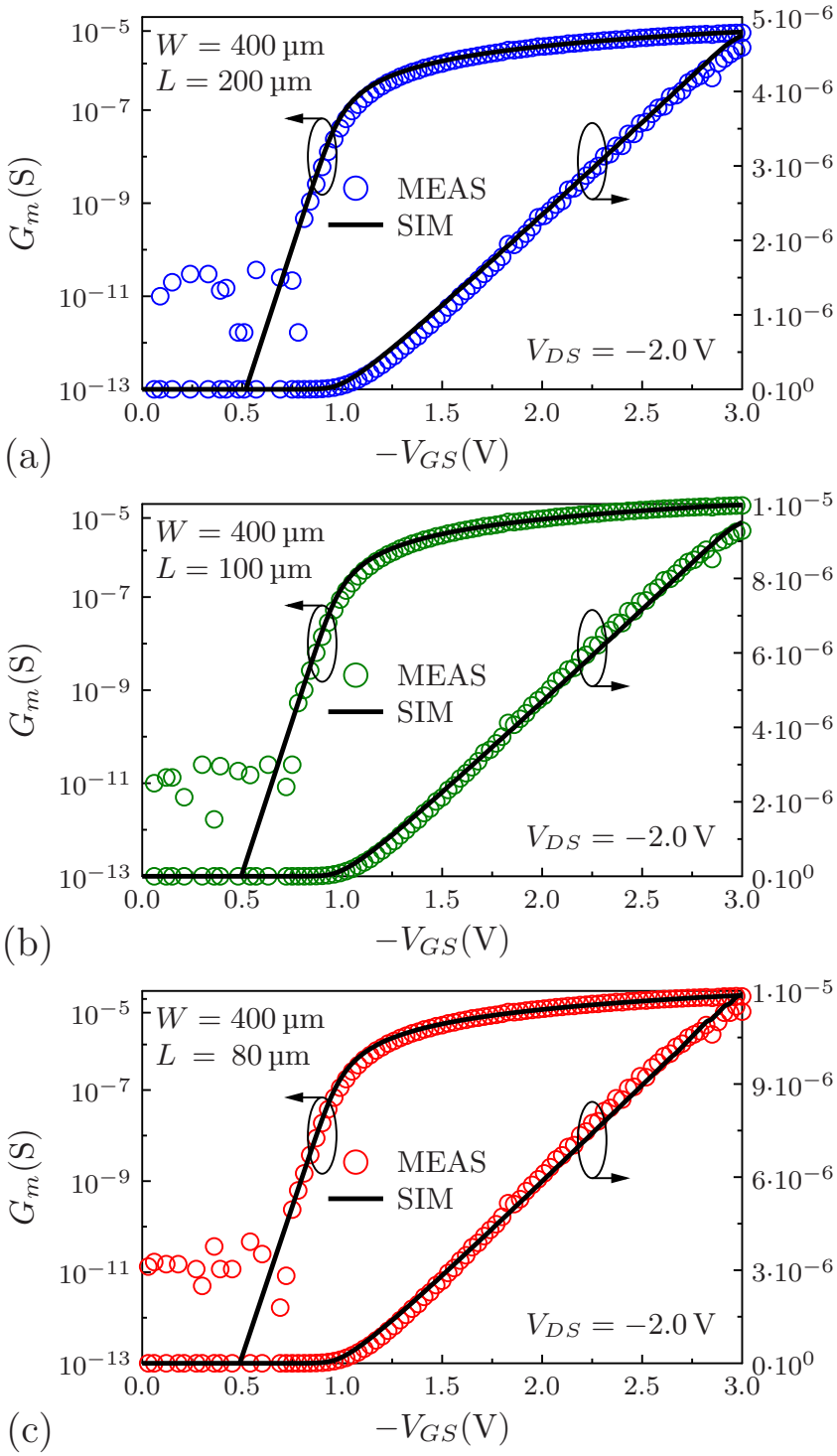


Figure A.6.: Gate transconductance G_m versus gate voltage V_{GS} of the fabricated p-channel DNTT TFTs with channel widths (W) of 400 µm and channel lengths (L) of (a) 200, (b) 100 and (c) 80 µm. Symbols: Measurements. Lines: Simulation results.

APPENDIX B

Layout Design of Silicon Stencil Masks for Variability Testing of Organic Thin-Film Transistor Based Circuits

B.1 Introduction

This Chapter provides an insight of the implementation of the Layout of the organic TFT based circuits that was presented in Chapter 4.

B.2 OTFT PDK Description

This section describes the properties of the process design kit (PDK), which is available for implementing OTFT layout designs in Cadence. The current PDK is oriented for layouts that include OTFTs of the bottom-gate/top-contact (inverted-staggered) configuration. Table B.1 summarizes the available layout layers and their corresponding materials. In the current design, only layers 1, 4, 5 and 8 are used. Layers 9 and 10 are employed in layouts that combine both organic and silicon based circuits. Note that the dielectric layers (AlO_x/SAM) and the flexible PEN substrate are not drawn layers. In Figure B.1 the corresponding color of each material is depicted.

Furthermore, the available PDK provides a Cadence Virtuoso [49] library that consists of the following five cells: n-channel OTFT, p-channel OTFT, resistor, capacitor-dielectric and gate-oxide cells. In the current study, only the p-channel OTFT cells are used. In Figure B.2, the drawn layouts of n-

Table B.1.: List of layout layers

Name	Material	Layer
L1_Gold_hoW (Bottom metal)	Gold	1st
L2_Alu_Conn	Aluminum	2nd
L3_Dielectric	-	3rd
L4_Alu_G (Bottom Gate)	Aluminum	4th
L5_Psemi (Semiconductor p-channel)	DNTT	5th
L6_Nsemi (Semiconductor n-channel)	-	6th
L7_Carbon	Carbon	7th
L8_Gold_veW_DS (Top metal)	Gold	8th
L9_Gold_Pad1	Gold	9th
L10_Gold_Pad2	Gold	10th
text	-	-

and p-channel TFTs with channel-width over channel-length ratio of $W/L = 50\,\mu m/5\,\mu m$ are shown. The transistor's layout can be adjusted by using the following parameters: channel-width, channel-length, number-of-fingers, number-of-dummys, gate-overlap and clearance.

Figure B.1.: PDK available layout layers and coloring.

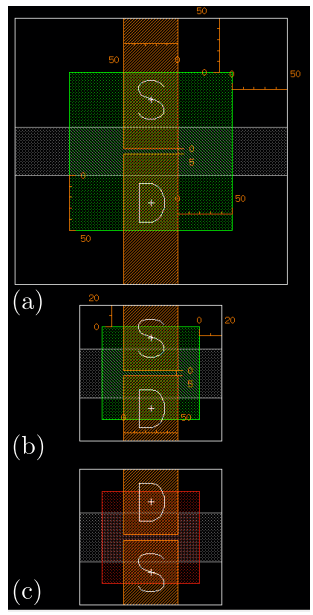


Figure B.2.: Layout of p-channel TFTs with channel-width over channel-length ratio of $W/L = 50\,\mu m/5\,\mu m$, overlap of $20\,\mu m$ and clearance of (a) $50\,\mu m$ and (b) $20\,\mu m$, respectively. (c) N-channel TFT of $W/L = 50\,\mu m/5\,\mu m$ (overlap=$20\,\mu m$, clearance=$20\,\mu m$).

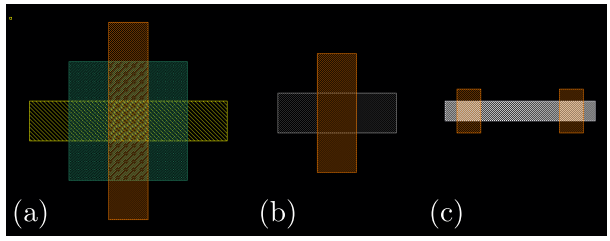


Figure B.3.: Layout of (a) capacitor-dielectric (b) gate-oxide and (c) resistor cells.

B.3 Circuits and Layouts for Variability Study

In this section the proposed circuits and layouts, that are expected to be used for the current variability study are described. The schematics of the basic topologies are depicted in Figure B.4 and consist of: a diode-loaded inverter (Driver: p-channel OTFT of $W/L = 50\,\mu m/5\,\mu m$, load: p-channel OTFT of

$W/L = 10\,\mu m/1\,\mu m^2$) and two different current mirror test circuits. Figures B.5 and B.6 show the layouts of the schematics depicted in Fig. B.4 (a) and (b), respectively.

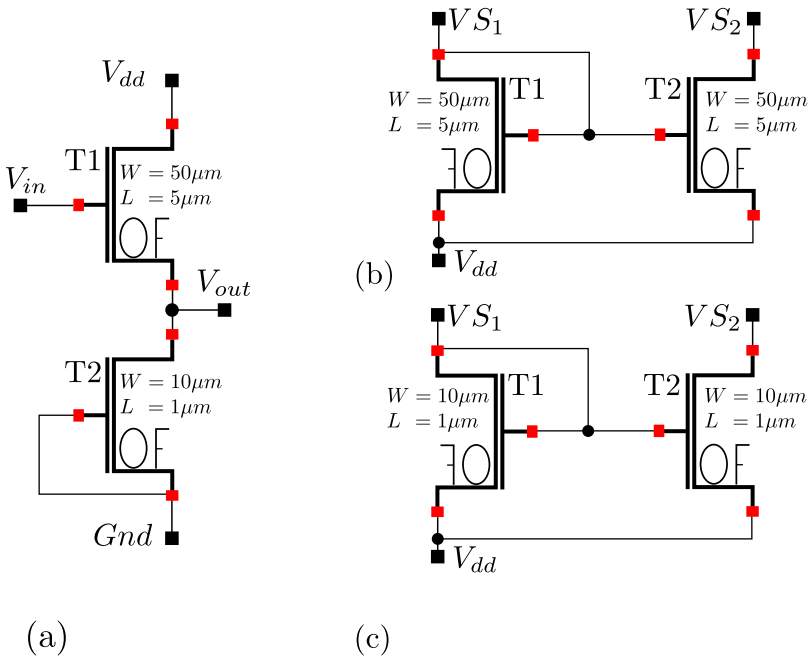


Figure B.4.: Schematics: (a) Diode-loaded inverter (Driver: p-channel OTFT of $W/L = 50\,\mu m/5\,\mu m$, load: p-channel OTFT of $W/L = 10\,\mu m/1\,\mu m^2$) and (b), (c) current mirror test circuits.

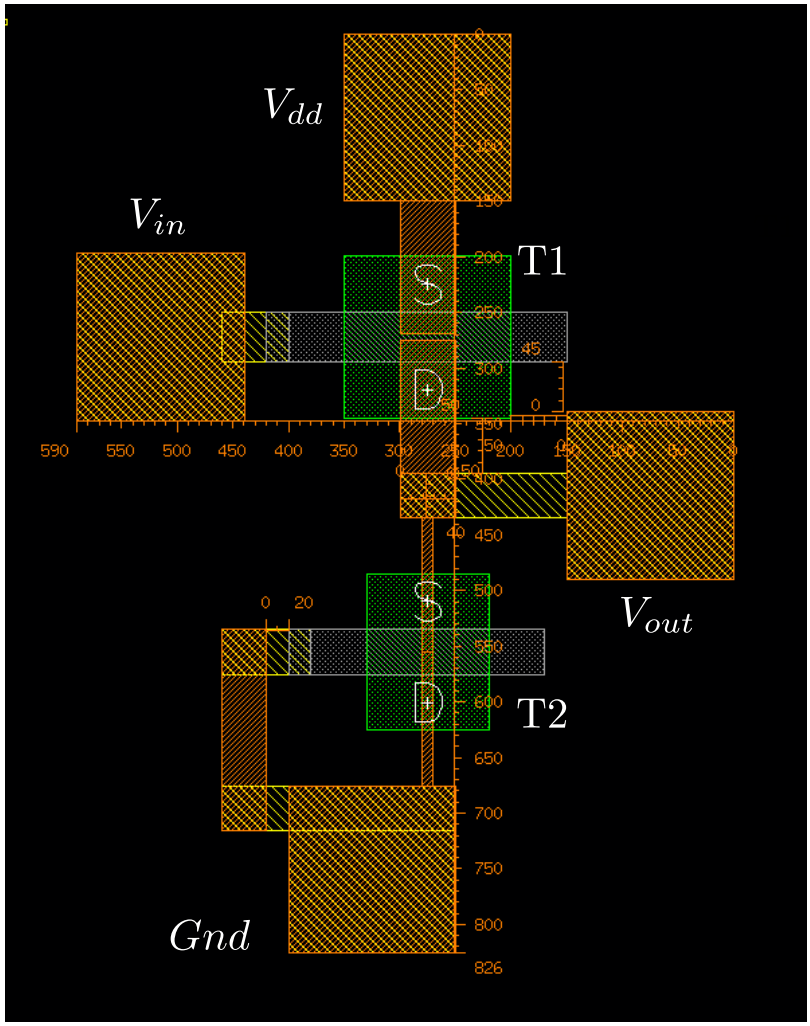


Figure B.5.: Layout of the diode-loaded inverter depicted in Figure B.4(a). Both driver and load transistors have an overlap of 20 µm and 50 µm clearance. The pads have an area of $150 \times 150 \mu m^2$, and consist of level-8 (top metal) gold on top of level-1 (bottom metal) gold. The vertical rooting line connecting T2 aluminum-gate with ground pad is of 40 µm width. Total area=$590 \times 826 \mu m^2$.

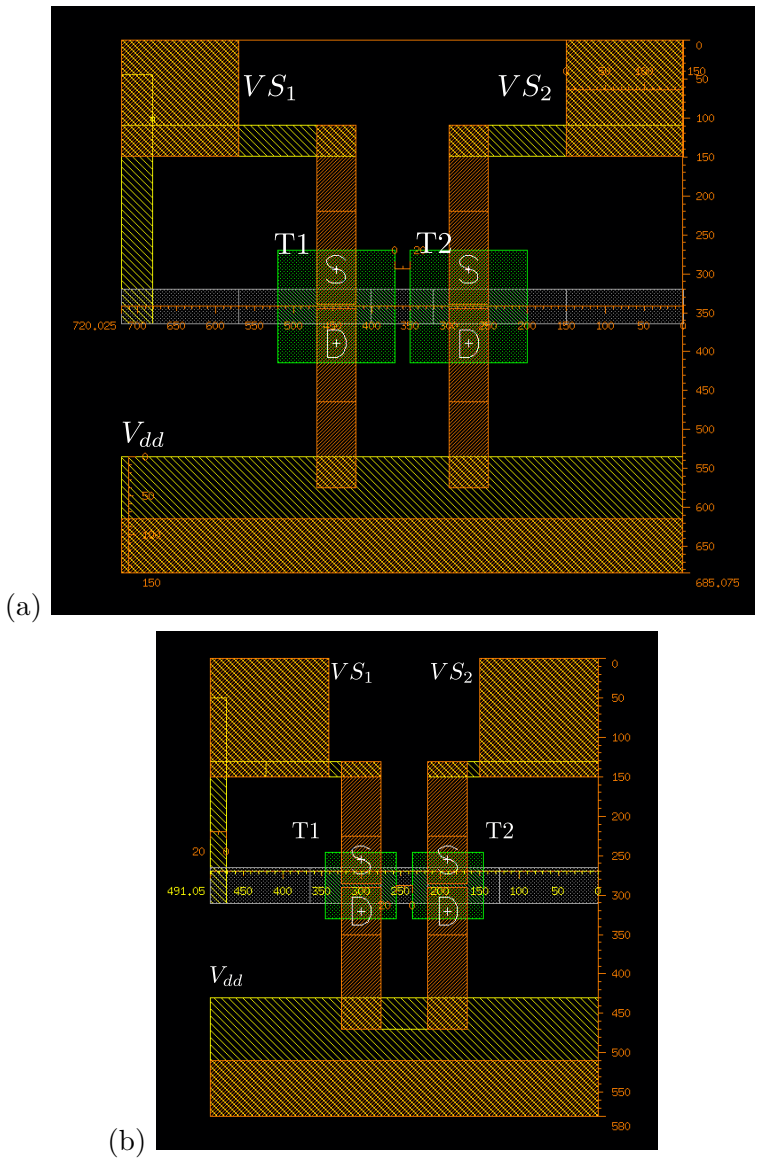


Figure B.6.: (a) Layout of the p-channel current mirror. OTFTs T1 and T2 have identical dimensions of $W/L = 50\,\mu m/5\,\mu m$, an overlap of $20\,\mu m^2$ and $50\,\mu m$ clearance. The level-1 gold rooting lines are of $40\,\mu m$ width. Total area=$720.025 \times 685.075 \mu m$. (b) Layout of the p-channel current mirror. T1 and T2 have identical dimensions and overlap as in (a). Here the clearance is of $20\,\mu m$ and the source-to-pad and source-to-vdd rooting lines are of $20\,\mu m$ (minimum) width, respectively. Total area=$491.05 \times 580 \mu m^2$. In both cases the Source-1 and Source-2 pads have an area of $150 \times 150 \mu m^2$. The vdd pad has dimensions 150 x maximum-layout-length μm^2 and this is because U-shape components should be avoided.

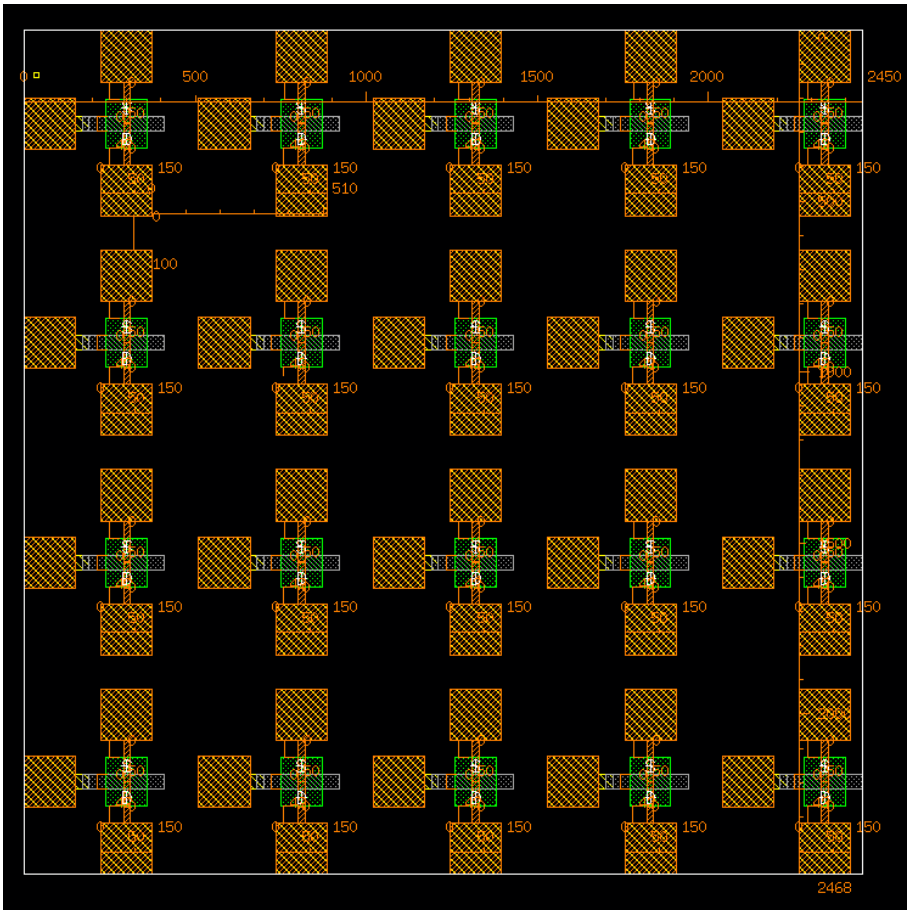


Figure B.7.: 5×4 array of identical p-channel TFTs with dimensions of $W/L = 20\,\mu m/2\,\mu m$, $20\,\mu m$ overlap and $50\,\mu m$ clearance. The pads have an area of $150 \times 150 \mu m^2$, and consist of level-8 (top metal) gold on top of level-1 (bottom metal) gold. The distance between devices is set to $100\,\mu m$. Total area=$2450 \times 2468 \mu m^2$.

B.4 Discussion

In order to have a complete variability analysis of the designed circuits, groups of stand-alone p-channel devices have to be included into the fabricated substrate in order to be characterized, e.g. as in Figure B.7 (both DC and variability characterization). Then the extracted model cards should be used to model the behavior of the OTFTs that comprise the designed circuits.

The choice of T2 with L=1um is risky. Therefore it is recommended to change with a bigger device of $W/L = 20\,\mu m/2\,\mu m$. Moreover, this choice will determine the dimensions of the "shorter channel" current mirror (Figure B.4(c)).

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