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Experimental and Design effort to understand a wider sense of memory application

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Abstract:

Magnetic Random-Access Memory (mRAM) is a more efficient, smaller, and less power-hungry memory device that can be implemented into computers. Using Magnetic Tunnel Junctions (MTJ) we store memory in devices that are far less complex than other types of memory with just the use of currents and magnetic fields changing the data.

In collaboration with the System-on-Chip Extension Technologies (SoCET) and Computing Advances by Probabilistic Spin Logic (CAPSL) groups, we have been working on using the characteristics of MTJs to characterize available commercial mRAM devices so we can have a better understanding of the thresholds of the MTJs. The SoCET teams develops chips using elements of the basic architecture and machine learning optimization. The CAPSL team creates probabilistic bits (p-bits) for probabilistic computing using MTJs and the Boltzmann Machine. Combining these two teams together I can work with mRAM to take the knowledge of computer architecture and knowledge of MTJ to better characterize and test the mRAM. To conduct the testing of commercial mRAM devices, a System Verilog code for a memory controller is being developed to input the data into the mRAM and read the data. To characterize mRAM we will test it by straining it multiple ways such as heat, high magnetic fields, and varying magnetic fields. We will be able to characterize it by comparing the data written into the device to the data read from the device after it has been strained.

Mentor(s):

Appenzeller

Johnson

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