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Optimization of an Embedded Phase Change Material Cooling Strategy Using Machine Learning

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Phase change materials (PCMs) have been widely investigated to function as a thermal buffer, particularly for components experiencing transient power loads. PCMs absorb some of the heat generated during periods of high-power dissipation and can enable longer periods of use before throttling of the processor or shut-off is required to prevent damage. Many studies with PCMs have focused on the functionality of PCM-laden heat sinks and, although these studies demonstrated extensions in high power operating times before the system overheated, the thermal pathway between the PCM-laden heat sink and heat source prevents their effective use as the heat generation rates increase. This study explores the concept of integrating PCMs at or near the silicon chip level near the heat source. Machine learning algorithms generate optimized patterns for balancing high heat storage zones and high thermal conductivity pathways within the embedded cooling layer on the backside of the silicon die. Reductions in both the hotspot temperatures and fluctuations in the transient temperature response highlights the effectiveness of embedded cooling and the machine learning algorithms provide a robust, efficient method for optimizing performance.

Keywords—Embedded Cooling, Phase Change Materials, Machine Learning

I. INTRODUCTION

Phase change materials (PCMs) have been widely investigated as a thermal buffering tool to mitigate temperature spikes in electronics experiencing transient power loads. By absorbing heat generated from the processor, they can extend operational time of the component before throttling or shut-off is required to prevent overheating. They can also provide thermal stability for components with cyclic power cycles. By melting and freezing during each on-off cycle, they can reduce the magnitude of temperature fluctuations.

Most PCM studies have focused on the functionality of externally packaged PCM heat sinks, and although these studies have demonstrated extensions in device operating times, numerous interfaces between the heat sink and heat source inhibit the effective usage of the PCM. An effective approach would be to integrate PCM at the silicon chip level near the heat source to eliminate resistance pathways that are otherwise present for external heat sinks. Soupermanien *et al.* explored the integration of metallic PCM within a power electronics structure and noted a hotspot temperature reduction of 28°C [1]. Similarly, Green, Federov, and Joshi embedded a composite PCM-heat spreader structure within the silicon die and saw an extension in device operating times by over 650% [2]. Shao *et al.* demonstrated the feasibility of an embedded PCM cooling strategy for computational sprinting [3]. Gurrum and colleagues tested a similar approach by etching PCM microchannels within a SiC die and observed temperature reductions of up to 25°C [4]. These works provide a foundation for embedding phase change materials within the chip for improved heat transfer performance.

Although such studies have highlighted the promise of embedded cooling, there is still a need to optimize the embedded heat sink geometry to achieve a balance of PCM heat storage zones and silicon thermal conductive pathways. Machine learning aided optimizations have been widely used in heat transfer to optimize microchannel heat sink geometries [5,6]. Boteler *et al*. investigated the use of Monte Carlo analysis to find optimal placements of copper, a metallic and an organic PCM to achieve temperature and weight objectives for a system [7].

This study introduces the use of a genetic algorithm to design an optimized embedded PCM cooling geometry within the silicon device layer. First, we briefly describe the modeling tools used to predict system performance and introduce the optimization approaches. Then, we discuss the effectiveness of the machine learning aided approach at predicting optimum geometries for three different heating cases.

II. METHODOLOGY

A. Modeling Tool

The system modeling and thermal analysis is performed using ParaPower, a MATLAB based simulation tool developed by the U.S. Army Research Laboratory to facilitate the design of electronic modules [8]. It uses a 3D thermal resistance network to calculate temperature evolution of the system and is noted to be up to 100X faster than standard finite element analysis (FEA) with temperature differences less than 2°C [9,10]. The simulation space is discretized into volumetric elements and PCM melting is computed via energy balance equations for each PCM element. A key difference compared to FEA models is that ParaPower assumes a constant melt temperature for the PCM, while many FEA simulation packages use the apparent heat capacity method modeling the phase change as a high heat capacity within a specified transition temperature range.

B. *Embedded Cooling System Geometry*

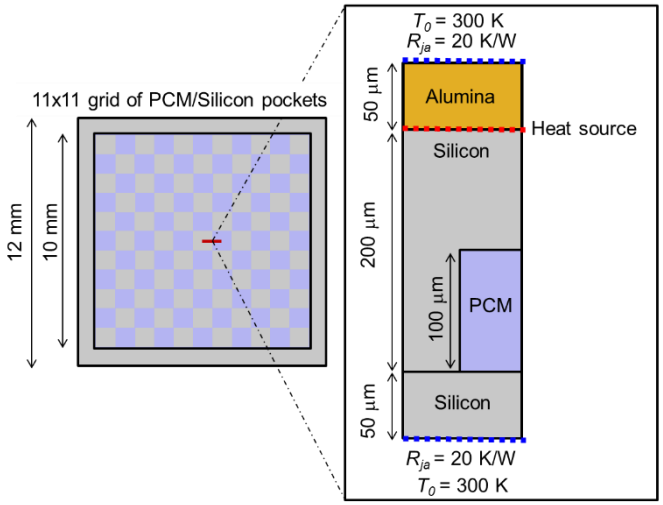

Fig. 1. A top-down schematic of the PCM layer consisting of PCM (purple) and silicon (gray) pockets. The inset illustrates a 2D cross-section that highlights the other device layers that span the entire chip area (12 x 12 mm). Heat is generated at the silicon-alumina interface with a square wave pattern with an on time of 0.5s. The top and bottom surfaces have a junction-to-ambient resistance of 20 K/W that is modeled with a heat transfer coefficient of 347 W/m^{2}K and an ambient temperature of 300 K.

For this study, we consider a 12 x 12 cm device that consists of a 100 µm embedded PCM layer etched in the backside of 200 µm silicon die (see Fig. 1). The PCM layer is capped with a 50 µm silicon sealing layer. The top surface of the silicon device layer generates heat and is electrically insulated with a 50 µm alumina layer. To emulate transient heat fluxes, the heat generation occurs as periodic square wave with an on/off time of 0.5 s. The top surface of the alumina and the bottom surface of the silicon layer have a junction-to-ambient resistance of R_{ja} = 20 K/W, which is similar to those observed in portable electronic devices. This is modeled with an equivalent heat transfer coefficient of 347 W/m^{2}K with an ambient temperature T_0 = 300 K.

The viable PCM layer cross section is designed to be 10 x 10 cm to allow for a 1 mm silicon containment edge. An 11 x 11 grid of PCM/silicon pockets is present within this layer. We have chosen a metallic composite with a melt temperature of 77°C as the embedded PCM [11]. The thermal conductivity, heat capacity, density, and latent heat of the PCM are: 32.3 W/mK, 642 J/kgK, 8490 kg/m^3, and 47730 J/kg.

This work uses a popular evolutionary algorithm called the genetic algorithm (GA). The GA solves optimization problems based on the concept of natural selection. After generating a randomized population set, it selects the best performing individual solutions and evolves them (by crossing over properties and introducing mutations) cyclically until an optimized solution is found [12, 13]. The strategic placement of the PCM/silicon pockets is optimized through the GA using two optimization approaches. In the first approach (called "GA Binary Optimization"), the GA cycles through a binary matrix representing PCM/Silicon placements. In the second approach (called "GA Integer Optimization"), the height of the PCM pocket can vary from 0 to 100 µm in 4 steps. Specifically, the GA cycles through an integer matrix representing the height of PCM placements in each pocket – a 0 denotes no PCM and a 3 denotes 100 µm. Both strategies have an optimization objective of reducing the overall maximum chip temperature $T_{o\text{-}max}$. Note that at a particular instant in time, the transient maximum chip temperature is referenced as T_{max}, while $T_{o\text{-}max}$ corresponds to the maximum temperature across all simulated timesteps. A second parameter of interest, which captures the stability of the system response, is the amplitude of the transient oscillation of the maximum chip temperature, T_{osc}. To efficiently optimize the design, system optimization is done for a simulation time of 20 seconds. After optimization, the simulations are run for longer durations to reach a quasi-steady state where melting and solidification happen each cycle of heating.

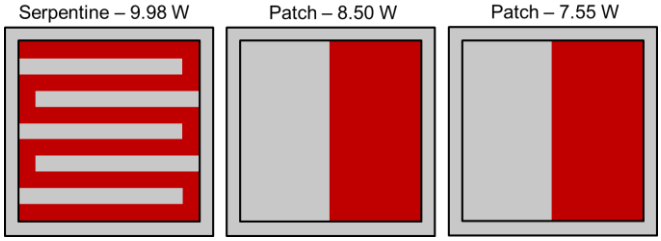

Fig. 2. Two heating patterns are explored for this study: a serpentine patter and a patch heating pattern. The serpentine heater is powered at 9.98W, and the patch heater has two power levels: 8.5 W and 7.55 W. The 8.5 W patch heater matches the power density of the serpentine pattern (170 kW/m^2), while the 7.55 W case has a reduced power density (151 kW/m^2). This reduced power density matches the overall maximum temperature for the baseline case (no PCM) in the serpentine heating pattern.

We explore three heating cases corresponding to two heating patterns: a serpentine pattern and a patch heater (see Fig. 2). The serpentine pattern has power density of 170 kW/m^2 corresponding to total heat dissipation of 9.98 W. The patch heating is a rectangular 5 cm x 10 cm heating patch that aligns with the edges of the viable PCM layer. The first case for the patch heater has a power density of 170 kW/m^2 producing heat dissipation of 8.50 W. The second case for the patch heater has a reduced power density (151 kW/m^2 corresponding to heat dissipation of 7.55 W). The reduced power density matches the overall maximum temperature of the reference case without PCM (bare silicon die) between the serpentine and patch heating patterns.

III. Results and Discussion

Table I and Table II show the overall maximum temperature $T_{o\text{-}max}$ and the amplitude of the thermal oscillations T_{osc} for the optimized PCM placements compared to 3 baseline configurations:

(a) **No PCM:** The entire die is silicon.

(b) **All PCM:** The entire 10 mm x 10 mm zone is filled with PCM.

(c) **Chip Overlaid PCM**: The PCM is placed directly above the heater pattern (matching the outlines in Fig. 2).

Table I shows the results for the time period of the optimization (20 seconds), while Table II shows the results after the systems have reached a quasi-steady state oscillation. Table II also includes the time to reach the quasi-steady state, Δt_{QS}. In both tables, T_{osc} is computed from the amplitude of the final simulated cycle of heating.

All cases with PCM outperform the bare silicon die ("no PCM" case) in terms of overall maximum temperature and the amplitude of the oscillations in temperature. For all configurations of the heater, the binary optimization and the integer optimization perform similarly. While $T_{o\text{-}max}$ is similar for the chip overlaid PCM and the optimized results, several of the optimized cases demonstrate reduced oscillations in the transient maximum temperature, even though that parameter was not a metric for the optimization. Although the metrics of system change slightly for the quasi-steady state compared to the shorter timescale used for optimization, the optimized designs perform well even for these longer durations.

A. *Serpentine Heating Pattern – 170 kW/m^2, 9.98 W*

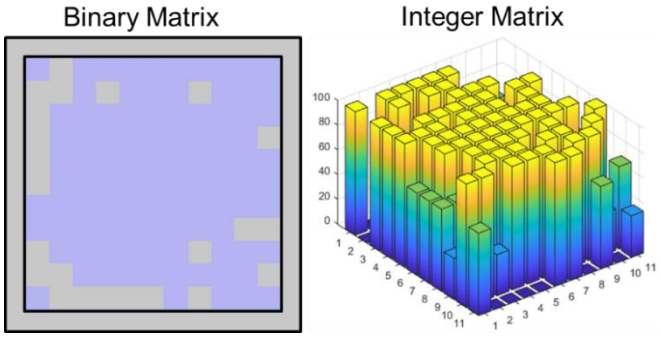

Fig. 3. Geometric representations for the GA optimized binary and integer matrices for the serpentine heating case. Both patterns place PCM in the majority of the available volume with the exception of some silicon pockets near the edges.

Fig. 3 shows the optimized placement of the PCM for the serpentine heating pattern with 9.98 W of heating. The binary matrix approach places PCM uniformly throughout the PCM/silicon layer with the exception of a few silicon pockets near the edges. The GA optimized integer matrix also fills the majority of the layer with PCM. Most of the PCM columns span the full height of the layer (100 μm) throughout the center with silicon pockets and partial PCM columns staggered near the edges. Fig. 4 compares the GA binary optimized pattern to the baseline cases, while Fig. 5 compares the binary optimization to the integer optimization for this heater configuration.

TABLE I. System Performance for 20 Seconds

Pattern	Serpentine 9.98 W		Patch 8.5 W		Patch 7.55 W	
	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)
No PCM	*94.86*	*32.61*	*103.12*	*44.59*	*94.61*	*39.61*
All PCM	*83.06*	*6.22*	*95.84*	*19.01*	*80.23*	*5.04*
Chip Overlaid PCM	*85.83*	*9.18*	*94.28*	*17.46*	*78.69*	*10.17*
GA Binary Matrix	*83.06*	*6.22*	*93.74*	*16.94*	*78.24*	*11.16*
GA Integer Matrix	*83.34*	*6.48*	*93.98*	*17.18*	*78.22*	*11.24*

TABLE II. System Performance at Quasi-Steady State

Pattern	Serpentine 9.98 W			Patch 8.5 W			Patch 7.55 W		
	Δt_{QS} (s)	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)	Δt_{QS} (s)	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)	Δt_{QS} (s)	$T_{o\text{-}max}$ (°C)	T_{osc} (°C)
No PCM	*8.5*	*94.86*	*32.61*	*8.5*	*103.12*	*44.59*	*7.5*	*94.61*	*39.61*
All PCM	*85.5*	*84.94*	*8.09*	*24.5*	*95.86*	*19.03*	*20.5*	*80.24*	*5.04*
Chip Overlaid PCM	*47.5*	*86.16*	*9.51*	*23.5*	*94.30*	*17.48*	*19.5*	*78.69*	*10.17*
GA Binary Matrix	*70.5*	*84.78*	*7.94*	*18.5*	*93.74*	*16.94*	*15.5*	*78.24*	*11.16*
GA Integer Matrix	*68.5*	*84.68*	*7.81*	*17.5*	*93.98*	*17.18*	*10.5*	*78.22*	*11.24*

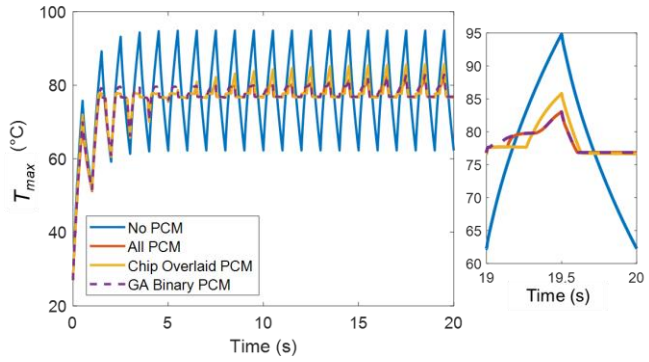

Fig. 4. Comparison of the transient maximum temperature of the system between the optimized binary approach and the baseline cases for the serpentine heater with 9.98 W. A zoomed-in view of the last heating cycle is provided on the right. The GA reduces the overall maximum chip temperature $T_{o\text{-}max}$ by 12%, from 94.86°C for an all silicon substrate to 83.06°C for an optimized substrate. For the given heating pattern and power density, an all-PCM layer performs similar to the GA optimized layer. The GA also reduces T_{osc} by 81%, from 32.61°C to 6.22°C.

Since heat generation is spread apart across the entire chip layer, the GA binary matrix pattern results in a transient system response similar to that of a completely filled PCM layer with slightly less PCM usage. Compared to an all-silicon substrate with a $T_{o\text{-}max}$ of 94.86°C, both the chip overlaid pattern and the GA binary optimization patterns reduce $T_{o\text{-}max}$ by ~12% to 83.06°C. The PCM layer has an additional benefit of significantly lowering T_{osc}. There is ample melting and re-solidification occurring at each cycle, thereby limiting transient fluctuations about 77°C. For the all-PCM and GA optimized layers, the oscillations reduce by 81% from 32.61°C to 6.22°C.

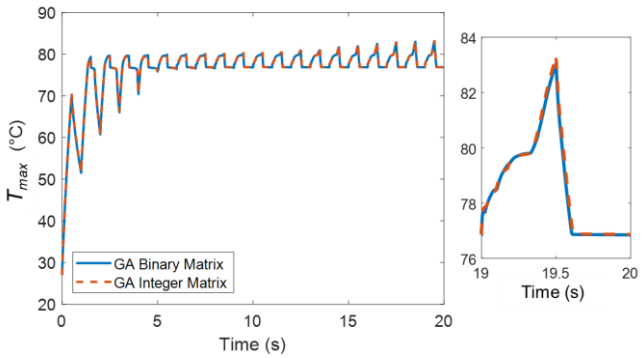

Fig. 5. Comparison between the transient maximum temperature of the system for the optimized binary and integer approaches with the serpentine pattern. A zoomed-in of the last heating cycle is provided on the right. Although the integer matrix has a similar performance to the binary matrix, this method has a larger computational expense.

Although both the binary and integer matrix geometries have similar performance, the integer matrix approach is significantly more computationally expensive. It takes longer per simulation and the GA fails to converge on a single geometry like the binary matrix. Instead, the GA terminates because of the generational limit set by the authors, resulting in a total computational time of ~58 hours compared to only ~12 hours needed for the binary matrix approach. It is hypothesized that the GA performed relatively poorly for this approach because of the reduced sensitivity to individual changes in the integer matrix compared to the binary matrix. For example, the $T_{o\text{-}max}$ change caused from adjusting the PCM column height from 66 μm to 100 μm is smaller than replacing a silicon column to a PCM one. Higher sensitivity to matrix changes might help guide the GA faster to the optimized solution.

This case study indicates that for power maps with uniform heating spread across the entire chip, it is beneficial to simply have an all-PCM layer since it will have similar performance to that of an optimized layer and does not have the additional complexity associated with manufacturing a hybrid PCM/silicon layer.

B. Patch Heating Pattern – 170 kW/m^2, 8.50 W

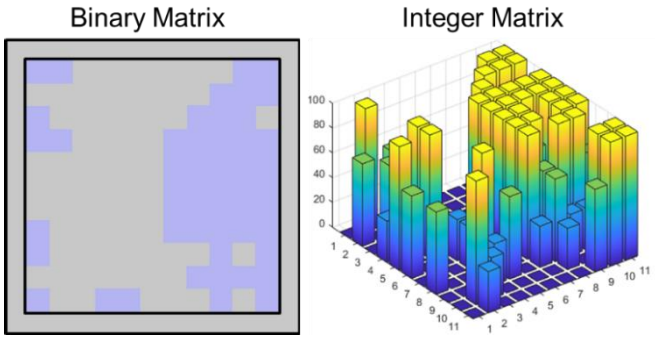

Fig. 6. Geometric representations for the GA optimized binary and integer matrices for the patch heating case (8.5 W). Both patterns place a majority of the PCM over the heat generation zone and share a resemblance of a curved inner boundary.

Fig. 6 shows the optimized placement of the PCM for the patch heating pattern with 8.5 W of heating. The binary matrix approach predominately places PCM over the heating pattern with a curved inner boundary. The GA optimized integer matrix produces geometry similar to the optimized binary matrix. Most of the 100 μm PCM columns are present above the heating patch in a curved inner boundary with other PCM columns present on the opposite end. Fig. 7 compares the performance of the GA binary optimized pattern to the baseline cases, while Fig. 8 compares the binary optimization to the integer optimization for this heater configuration.

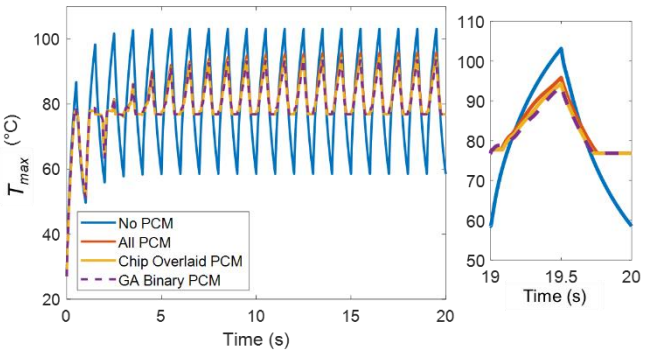

Fig. 7. Comparison of the transient maximum temperature of the system between the optimized binary approach and the baseline cases for the patch heater with 8.50 W. For the binary matrix method, the GA reduces the overall maximum chip temperature $T_{o\text{-}max}$ by 9%, from 103.12°C for an all silicon substrate to 93.74°C for an optimized substrate. Unlike the prior case

study, since the heating pattern is concentrated on one side, the GA matrix has a system performance that is much closer to the chip overlaid PCM rather than an all-PCM layer. The GA also reduces T_{osc} by 62 %, from 44.59°C to 16.94°C.

The optimized binary pattern reduces $T_{o\text{-}max}$ by 9% to 93.74°C. Similar to the prior case study, the PCM layer has the additional benefit of lowering system T_{osc}. For the GA optimized layer, the oscillations reduce by 62 % to 16.94°C. Compared to the serpentine heating case, the reduction in both parameters is relatively lower because the same PCM is used despite the higher system temperatures. There is insufficient re-solidification in relevant PCM pockets during the 'off' portion of the heating cycle (shown by shorter flat regions in the T_{max} response) and indicates that the PCM melt temperature needs to be higher to allow for a shorter time to re-solidification. For example, only 26% of the PCM in the chip overlaid PCM geometry re-solidifies and melts in the last few duty cycles.

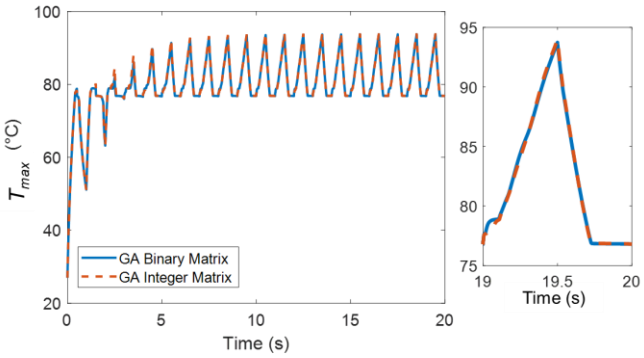

Fig. 8. Comparison between the transient maximum temperature of the system for the optimized binary and integer approaches with the patch heater(8.5 W). Like the prior heating case, although the integer matrix has a similar performance to the binary matrix, this method has a larger computational expense.

Similar to the previous case, algorithm termination for the GA integer matrix occurs because of the set generational limit, resulting in a computational time of ~58 hours. Although both the binary and integer matrix geometries have similar performances, it is advisable to opt for the binary matrix geometry to avoid the added manufacturing complexity of further dividing the PCM/silicon layer into 3 different layers needed for the integer matrix geometry.

The optimized patterns in this case study differ from those with prior study. The concentration of heat on one side of the chip only requires PCM placement above it unlike the serpentine heating pattern that spreads across the entire chip and requires PCM placement accordingly. Here, having PCM pockets in regions of no heat generation is detrimental to system performance and it is beneficial to have conductive silicon pathways there instead. Thus, for power maps with concentrated hotspots, GA strategies are effective at generating a PCM/silicon patterns that outperform intuitive ones. To ensure an effective PCM geometry, it is advisable to adjust the GA optimized geometry by removing noticeable outliers. For this heating case, the GA geometry was 'cleaned' by filling the inside of the curved boundary entirely with PCM and leaving only silicon outside of it. This ensures that all the PCM is only limited to the heat generation zone. This approach further reduces $T_{o\text{-}max}$ to 93.60°C and removes the manufacturing complexity associated with filling outlying PCM pockets.

C. Patch Heating Pattern – 151 kW/m^2, 7.55 W

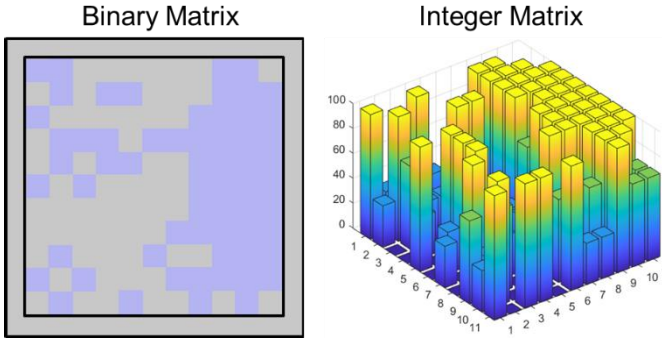

Fig. 9. Geometric representations for the GA optimized binary and integer matrices for the patch heater (7.55 W). Like the prior patch heating case, both patterns place a majority of the PCM above the heat generation zone. Although there is some resemblance of a curved innet boundary for the binary matrix, the intger matrix has a curved outer boundary on the edge of the PCM layer. Both patterns also place a larger amount of PCM outside the heat generation zone compared to the prior case.

Fig. 9 shows the optimized placement of the PCM for the patch heating pattern with 7.55 W of heating. The binary matrix approach predominately places PCM over the heating pattern like the prior patch heating case. However, unlike that prior patch heating case, there are a greater number of PCM pockets in regions of no heating. The GA integer matrix also terminates on a pattern with PCM concentration above the heating patch and greater number of PCM columns in regions of no heating. A key difference between the two matrix patterns is that the integer matrix has a curved outer boundary of 100 µm PCM columns on the edge of the PCM layer whereas the binary matrix has a resemblance of an curved inner boundary. Fig. 10 compares the performance of the GA binary optimized pattern to the baseline cases, while Fig. 11 compares the binary optimization to the integer optimization for this heater configuration.

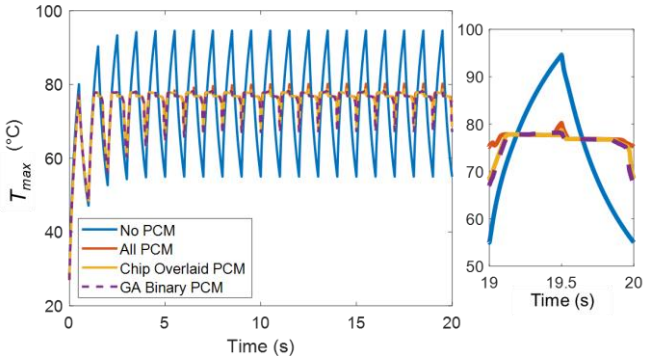

Fig. 10. Comparison of the transient maximum temperature of the system between the optimized binary approach and the baseline cases for the patch heater with 7.55 W. For the binary matrix method, the GA reduces the overall maximum chip temperature $T_{o\text{-}max}$ by 17%, from 94.61°C for an all silicon substrate to 78.24°C for an optimized substrate. Unlike the prior cases, the all-PCM layer has the largest improvement in T_{osc}, reducing it by 87% from 39.61°C to 5.02°C.

The GA binary matrix pattern reduces $T_{o\text{-}max}$ by 17% to 78.24°C. Unlike the prior patch heating case, there is ample PCM melting and re-solidification in each cycle and the system has a much better T_{osc} performance. For this optimized layer and an all-PCM layer, the oscillations reduce by 72% and 87% respectively. For an all-PCM layer, the melt fraction oscillation during the quasi-steady state is 1, indicating that the entire PCM block melts and re-solidifies during each cycle. The increased reduction in T_{osc} and $T_{o\text{-}max}$ compared to the prior patch heating case highlights the importance of the PCM melt temperature. This also explains the presence of more PCM pockets in this patch heating case despite a lower power density than the prior case. The GA places PCM locations only in regions that would benefit from the latent heat storage despite the loss of thermal conductivity resulting from the replacement of high conductivity silicon pockets. The PCM melt fraction oscillation of the GA pattern and the chip overlaid PCM pattern is more than double than those in the prior patch heating case. Thus, the available latent heat storage during each cycle (characterized by how much PCM solidifies during the off portion) is much higher. This allows the GA to replace more silicon pathways with the PCM.

In this case study, attempts at 'cleaning' the GA optimized pattern were ineffective and resulted in system performances that were slightly worse than the optimized pattern.

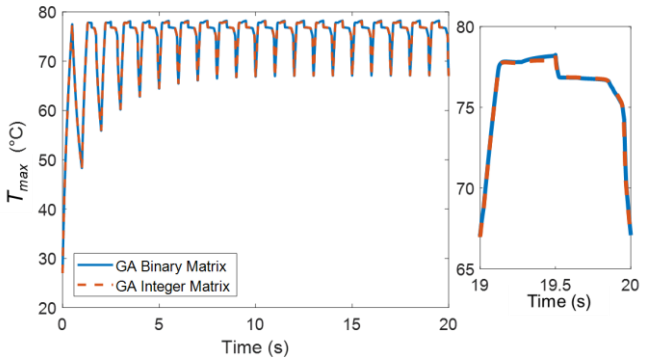

Fig. 11. Comparison between the transient maximum temperature of the system for the optimized binary and integer approaches with the patch heater (7.55 W). Although both geometries have similar performances, unlike the prior heating cases, the integer matrix slightly performs the binary matrix (by 0.02°C). However, the GA again terminates because of the generational limit and does not converge on a single pattern.

Like both the prior heating cases, the integer matrix approach is significantly more computationally expensive since it terminates because of the generational limit. However, this patch heating case is the only case where the integer matrix geometry slightly outperforms the binary matrix geometry (~0.02°C).

This study highlights an interesting trade-off that can be present in embedded PCM systems. As the $T_{o\text{-}max}$ for different PCM pattern reduces, the T_{osc} increases. Although using the GA binary PCM pattern further reduces $T_{o\text{-}max}$ by ~2°C compared to an all-PCM pattern, T_{osc} increases by ~6°C. The $T_{o\text{-}max}$ for the all-PCM pattern is higher because the PCM has a thermal conductivity that is an order of magnitude lower than that of silicon. Since the all-PCM pattern does not have the benefit of having conductive silicon pathways, its $T_{o\text{-}max}$ value is higher. However, the all-PCM pattern has the smallest T_{osc} value because all the PCM within the layer melts and re-solidifies during each heat pulse. Since the melt fraction oscillation for the GA optimized and chip overlaid patterns is less than 1, their T_{osc} values are higher. To ensure complete melting and re-solidification, these patterns would need to have a PCM melt temperature that is a few degrees lower than 77°C. This can also be concluded via zoomed-in view of the last heat pulse in Fig. 10. There is no kink in the curves for the two PCM patterns (GA binary and chip overlaid) at the 19.5 s mark indicating that not all the PCM has melted.

It is advisable to use an all-PCM layer since it has an improved T_{osc} response with only a relatively small $T_{o\text{-}max}$ trade-off. This layer also does not have the additional manufacturing complexity associated with a hybrid PCM/silicon layer.

IV. Conclusion

This study introduced the use of a genetic algorithm to design an optimized embedded PCM cooling geometry. The authors made use of a lightweight modeling tool called ParaPower to allow for faster computation and easier integration with machine learning approaches. Geometric optimization was performed for three different heating cases and compared to baseline cases (bare silicon, all PCM, and a PCM geometry matching the heater pattern).

The embedded PCM approach reduces the overall maximum chip temperature ($T_{o\text{-}max}$) by up to 17% and fluctuations in the transient maximum chip temperature (T_{osc}) by up to 87%. Of the two optimization approaches considered, the binary matrix approach resulted in improved system performances with a significantly lower computational cost. Ultimately, the PCM layer height may be too small for the integer approach to have a considerable impact. The integer matrix might be beneficial for larger systems where system performance is more sensitive to a sectioned PCM layer.

Results of the patch heating case at 7.55 W highlighted that embedded PCM systems can have a trade-off between $T_{o\text{-}max}$ and T_{osc}. Although an all-PCM layer had a $T_{o\text{-}max}$ that was ~2°C higher than the optimized PCM/silicon layer, it further reduced T_{osc} by ~6°C. Thus, if the all-PCM layer resulted in a $T_{o\text{-}max}$ value that was below than the required cut-off temperature, it is advisable to use this layer because of its relative simplicity in manufacturing and improved stability in the system response. In this regard, a recommended optimization approach for embedded systems that have a trade-off between $T_{o\text{-}max}$ and T_{osc} would be to generate a pareto front of the two parameters and select a layer that satisfies both parameter requirements and ensures easier manufacturability.

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