# ULTRA-LOW LOSSES SIC BASED SHUNT ACTIVE POWER FILTER FOR HARMONICS MITIGATION AND HARMONICS POWER RECOVERY IN INDUSTRIAL POWER SYSTEMS

RODRIGO GUZMAN ITURRA

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*If you want to find the secrets of the universe, think in terms of energy, frequency and vibration*

- Nikola Tesla

To my parents, to my wife-to-be

# Declaration

I declare that I have developed and written the enclosed thesis entitled 'Ultra-low losses SiC based Shunt Active Power Filter for Harmonics Mitigation and Harmonics Power Recovery in Industrial Power Systems' entirely by myself and have not used sources or means without declaration in the text. Any thoughts or quotations which were inferred from these sources are clearly marked as such.

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# Abstract

The classical method to suppress resonances in power systems is by installing passive dampers in parallel to the loads. However, observations indicate significant power losses due to harmonic currents flowing over passive dampers. Certainly, passive dampers absorb harmonic active power and dissipate this power as heat on their resistive elements leading to energy waste. On the other hand, the passive damper counterpart is the active damper. The latter is also known in technical literature as Voltage driven shunt active power filter (VSAPF). The active damper is a power-electronics-based system that emulates a virtual resistance at harmonic frequencies. Truly, very little was known about the harmonic power absorption on active dampers. Therefore, this dissertation delves into a profound analysis of the capability of an ultra-low losses active damper based on SiC semiconductor technology to process the harmonic power intake and perform harmonic power recovery. Harmonic power recovery in this context is understood as the process of transforming the harmonic active power absorbed into fundamental power that is injected back into the power system. The next topic that is addressed is the reduction in the fundamental power demanded by an industrial facility due to the recovery of harmonic active power. To this end, this dissertation analyzes the power balance flow of a distribution power system (e.g., industrial grid) that includes an ultra-low losses active damper. Arising out of the power balance flow analysis, it was found that the active damper with harmonic recovery function achieves a 1.4% reduction on the fundamental power demanded compared to a passive damper. Naturally, the lower the active damper´s power losses, the higher will be the amount of harmonic active power that can be recovered from the power system. Therefore, during this research work, various power electronics converters topologies are analysed to find the best possible design for the active damper with harmonic power recovery functionality. Arising out of this investigation, it was found that the conventional three-level neutral point piloted converter (3L-TNPC) and the asymmetrical three-level converter (3L-ASYM) are the most suitable power circuit topologies for the ultra-low losses active damper. The former topology, the 3L-TNPC, exhibits the lowest power losses for switching frequencies up to 60 kHz. And then, the 3L-ASYM topology presents the lowest losses among all the studied power circuits for switching frequencies beyond 70 kHz. Furthermore, as an active damper forms a closed loop between harmonic voltages and compensating currents, its stability must be ensured. Thus, a careful design of the VSAPF control system and its inner current controllers is essential. On account of this, this dissertation proposes using the Ragazzini method to design the VSAPF's inner current controllers. Furthermore, the direct design of the inner current controllers on the discrete domain using the Ragazzini method increases the current controllers' bandwidth by a factor of three compared to the controllers' design with conventional methods. Consequently, the increased current controller's bandwidth achieved through the Ragazzini method pushes the stability limit of the active damper forward compared with traditional current controller designs.

# Acknowledgments

First, I would like to thank my director of studies, Prof. Dr.-Ing. Peter Thiemann, for allowing me to carry out my PhD studies in his laboratory and within his research group. I am very grateful for all the trust that Prof. Thiemann put in me to carry out research and development within the European project "SIMON - Simulation OHMscher Netze". Besides, I need to thank him for all the support he has given me since day one. Support not only in regards to all the equipment and material that I needed to perform my research. But also for giving me the opportunities to visit different conferences, seminars, and workshops where I could grasp new concepts and build all the necessary skills to finish my PhD work. Indeed, it has been a pleasure and an honor to work for you Prof. Thiemann; I have learned so many things from you.

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*Thank you*
*Rodrigo Guzman Iturra*

# Abbreviations

| | |
|---|---|
| PV | Photovoltaic Arrays |
| IRENA | International Renewable Energy Agency |
| ASD | Adjustable Speed Drives |
| UPS | Uninterruptible Power Supplies |
| IE | Efficiency Class |
| ASM | Asynchronous Motors |
| ZVEI | German Electrical and Electronic Manufacturers Association |
| PCC | Point of Common Coupling |
| NLL | Nonlinear Loads |
| SAPF | Shunt Active Power Filter |
| VSAPF | Voltage-driven shunt active power filter |
| DSP | Digital Signal Processors |
| FPGA | Field-programmable Gate Arrays |
| THD | Total Harmonic Distortion |
| VSC | Voltage Source Converter |
| CSC | Current Source Converter |
| WBG | Wide Band Gap |
| SiC | Silicon Carbide |
| PWM | Pulse Width Modulator |
| SRF | Synchronous Reference Frame |
| FFT | Fast Fourier Transform |
| MPP | Molybdenum permalloy |
| SSC | Solid-state synchronous series compensator |
| HPF | High Pass Filter |
| PLL | Phase-Locked-Loop |
| ESR | Equivalent Series Resistor |
| SBD | Schottky Barrier Diode |

| | |
|---|---|
| HEMT | High Electron Mobility Transistors |
| ZVS | Zero Voltage Switching |
| MLT | Mean Length Turn |
| FOM | Figures-of-merit |
| CC | Current Controller |
| MPZ | Pole-zero matching |
| ZOH | Zero-Order-Hold |
| DPWM | Digital PWM |
| FF | Feedforward compensation |
| PFC | Power Factor Correction |

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# 1 Introduction

## 1.1 BACKGROUND

Power grids are large and complex systems that consist of many inductive elements, capacitive components, and power converters highly interconnected. For instance, shown in Fig.1.1 is a modern power grid with a significant number of power electronics converters connected to the system. In such a power grid, elements with an inductive behavior include distribution lines, feeders, and the leakage inductance of distribution transformers [1, 2]. In addition, capacitive components can be found in shunt compensators for power factor correction and in the output filters of power converters [3, 4, 5]. Undeniably, inductive and capacitive components play a significant role in shaping the impedance frequency response of a particular power system [6]. On the other hand, the efficient processing of electrical energy made by power converters has been the reason why the adoption of such devices has been continuously increasing. Truly, power converters have been extended in many applications across different segments in the renewable energy, transportation, and industry sectors [7, 8]. Certainly, a problem of concern is that power converters could excite resonances produced by inductive and capacitive components within the power system [2, 3].

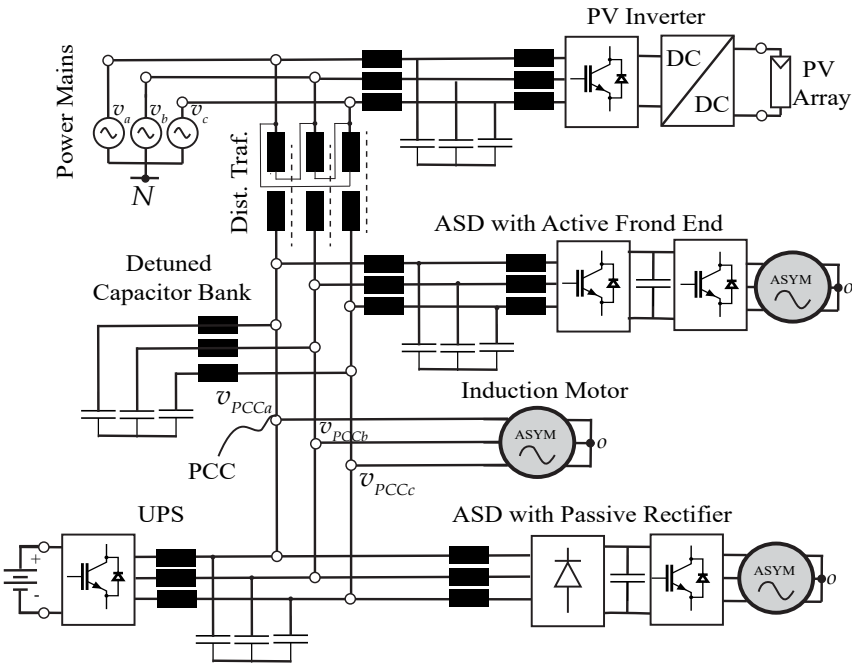


**Fig. 1.1:** Distribution power system consisting of many power converters, inductive and capacitive components connected to the point of common coupling (PCC).

### 1.1.1 *Power grids dominated by power converters*

Arguably, we are heading towards power grids dominated by power converters. Power converters are essential to address the challenges related to the increasing energy demand and the integration of renewable energy systems.For this reason, it is expected that the utilization of power converters will continue to grow, especially in the segments of generation and consumption of electrical energy [9, 10, 11]. Certainly, in the generation segment, power converters are indispensable to interface solar Photovoltaic Arrays (PV) and wind turbines with the power system. Because power converters transform the power produced by clean energy sources into electrical energy that can be stored in batteries or that can be fed directly into the power grid [12]. As an illustration, Fig.1.2 to Fig. 1.4 show the growth of power converters in the generation segment. In particular, Fig. 1.2 and 1.3 show the growth of global installed generation capacity for wind power and for photovoltaic power respectively. Notice that Figs. 1.2 and 1.3 are based on

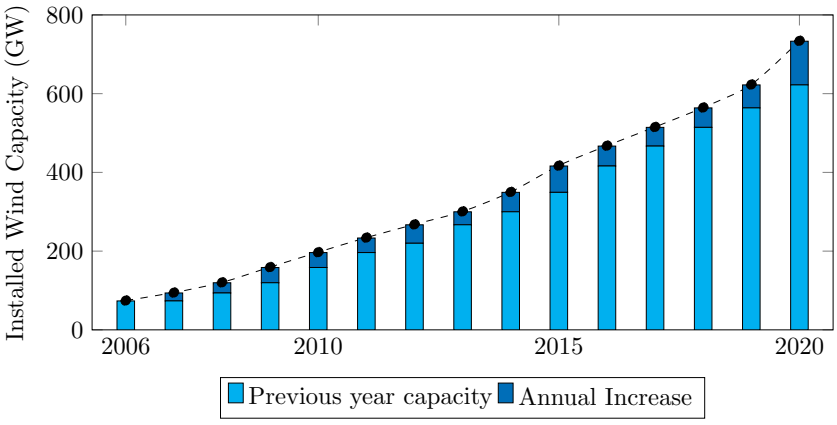


**Fig. 1.2:** Global installed Wind Power Capacity (2006- 2020). Reported by the International Renewable Energy Agency (IRENA) on "Renewable Capacity Statistics 2021" [13].

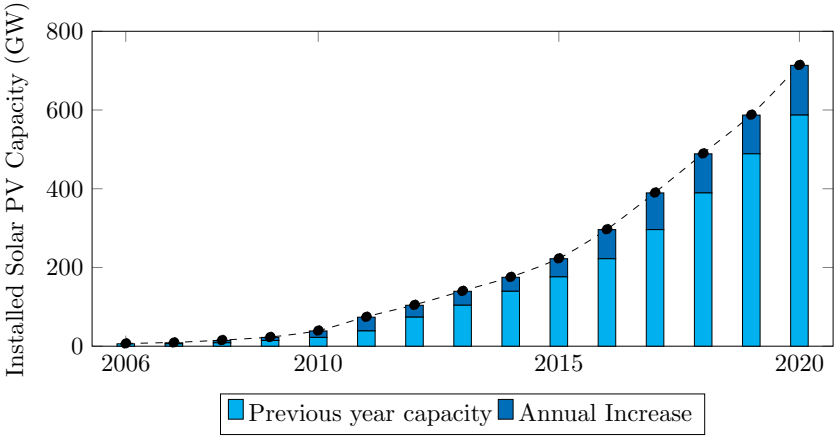


**Fig. 1.3:** Global installed Solar PV Power Capacity (until 2020). Reported by the International Renewable Energy Agency (IRENA) on "Renewable Capacity Statistics 2021" [13].

information published by the International Renewable Energy Agency (IRENA) [13] and

were presented by Blaabjerg in [14]. As can be seen, the figures cover the years 2006 to 2020 and show that the installed capacity for wind and solar power has been growing steadily without interruptions. Moreover, Fig. 1.4 shows the annual growth rate for different technologies of renewable electricity generation for the same time span [14, 15]. From the figure, it can be seen that the average annual growth for wind power has been around 12%, whereas for photovoltaic power, the average annual growth rate has been in the order of 22%. It turns out that wind and solar power technologies exhibit the largest growth among all the renewable energy sources.

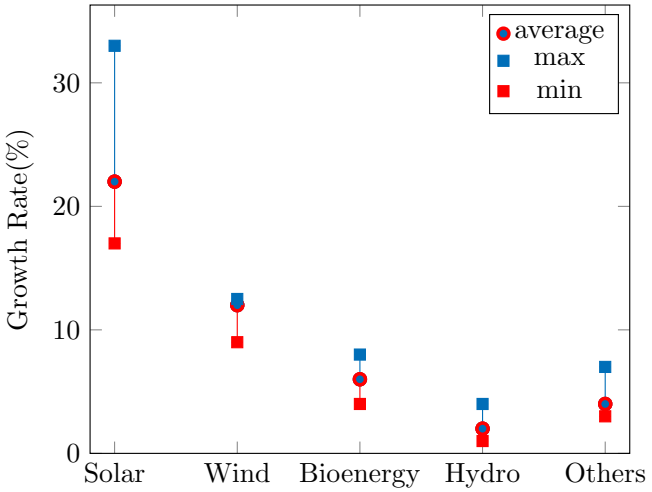


**Fig. 1.4:** Renewable Energy Generation - Annual growth rate of global installed capacity for type of clean energy source between 2006 and 2020 [15] (as reported in [14])

Conversely, in the consumption segment, power converters enable the efficient control of electrical power in loads such as lighting devices, Adjustable Speed Drives (ASD) and Uninterruptible Power Supplies (UPS) [16, 17]. These fully controllable loads will be essential in future power systems within the consumption segment for two important reasons. First, as electricity generation has to match the load demand and renewable energy systems produce power in a fluctuating manner, smart loads that shut down themselves at peak hours and turn on when there is a surplus of renewable energy will become necessary [18]. The latter will ensure an optimum supply of electricity to final users exploiting at the same time the full potential of renewable energy sources. Second, final users in the consumption segment (e.g., industrial users) will increase the number of power converters within their applications to increase the efficiency and flexibility of their processes [16]. As an illustration, Fig. 1.5 shows the number of ASD installed in the United States (U.S.) in 2016 and a forecast made for the year 2024 [19]. This information was generated by the market research company Global Market Insights and published in 2018. In particular, the 2024's forecast shown in Fig. 1.5 indicates that the number of installed ASD will increase in applications such as conveyors, compressors, and extruders in comparison with the year 2016. Particularly, an important boost in new units can be seen for pumps and fans, where significant energy savings can be achieved using adjustable speed drives for the flow's control of fluids or gases [20]. As is explained by Mohan in [21], only in the U.S. adjustable speed drives have the potential to reduce electrical energy consumption between 3.3 % to 8.9% in the process industry. On the other hand, in the European context, any asynchronous-motor drive in the range 0.12

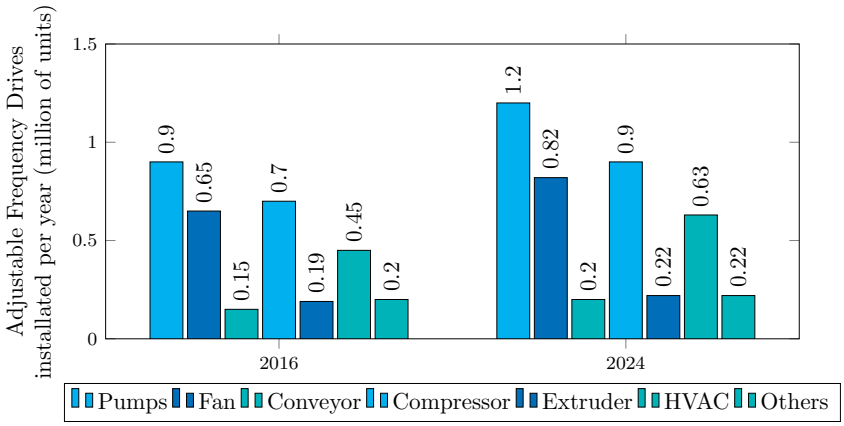


**Fig. 1.5:** Number of Adjustable speed drives installed by application in the United States. Data gathered for the year 2016 and estimated for the year 2024 by the research company Global Market Insights [19].

kW - 1000 kW introduced into the market between 2015 and 2021 needed to fulfill the EU Motor Regulation 640/2009 [22]. In detail, the EU 640/2009 regulation establishes that Asynchronous Motors (ASM) introduced in the market as products for the first time need to comply with a specific Efficiency Class (IE). The efficiency class had to be either IE3 (premium efficiency) when the ASM was meant to direct operation with the grid or could be reduced to IE2 (high efficiency) if it was meant to be driven by an ASD. Consequently, the regulation EU 640/2009 translated into a significant increase in the number of installed ASD within the EU between 2015 and 2021, according to the German Electrical and Electronic Manufacturers Association (ZVEI). In fact, ZVEI estimated that the number of variable-speed drives within the EU has doubled since 2012 [23]. Finally, Fig. 1.6 shows the number of cumulative shipments of AC servo motors made by the Japanese manufacturer Yaskawa [24]. Indeed, AC servo motors can be optimally driven only by power electronics converters. Specifically, by power converters that are a combination of rectifier, DC-Link and inverter, with the last one digitally controlled. In essence, Fig. 1.6 provides further evidence of the sustained increase in the number of power converters in the consumption segment. On the whole, Fig. 1.2 to Fig. 1.6 show the steady growth in

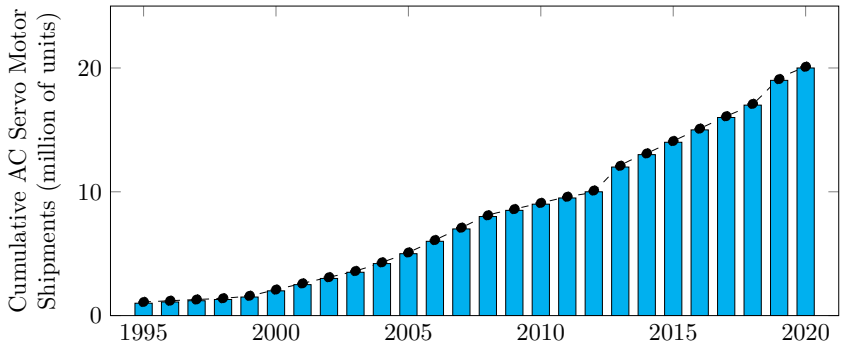


**Fig. 1.6:** Cumulative AC Servo Motor Shipments of the japanese manufacturer Yaskawa. The company reached 20 million units shipped in 2020 [24].

the number of power converters connected to the power grid. Above all, the statistics have shown a clear path towards a power grid dominated by power converters.

### 1.1.2 *Power quality problems caused by power converters*

As shown in the previous section, the number of power converters connected to power systems is steadily increasing. This large number of power converters affects the nature and functioning of power grids. In particular, the operation of power converters deteriorates the power quality of the power system they are connected to. Even though there is not a universal consensus on the definition of power quality among electrical engineers [25], for AC supply systems, power quality is mostly assessed in terms of voltage, current, and frequency deviations from an ideal condition [1, 26]. Even most people associate the term power quality directly with the term voltage quality [27]. Bollens in [25] points out that voltage quality relates to the discrepancy between the actual voltage and an ideal voltage waveform. Although Bollens argues that what constitutes an ideal voltage waveform can be largely discussed and debated, he claims that a straightforward solution is to define an ideal voltage as a pure sinusoidal voltage waveform with constant amplitude and frequency—both the same as their nominal values. Thus, if the actual voltage deviates to a great extent from an ideal voltage waveform, it is possible to say that the voltage quality is poor and there are power quality problems. As an illustration, Fig.1.7 **a)** shows the ideal voltage waveform that is expected in an industrial distribution system. This ideal voltage waveform exhibits a sinusoidal shape, a fixed frequency (typically 50 Hz in Europe), and a RMS value between two phases of 400 V. Furthermore, Fig.1.7 **b)** shows the equivalent circuit of a three-phase distribution system that consist of three voltage sources ($v_S$), the equivalent impedance of the grid ($L_G$) and a conventional three-phase resistive load. Examples of other conventional loads include induction motors, light bulbs, and capacitor banks. Obviously, in Fig.1.7 **b)**, the voltage sources represent the voltage supplied by the utility to the user's transformer. In addition, the equivalent impedance of the grid takes into account the inductive part of the distribution network and the leakage impedance of the distribution transformer, all refereed to the transformer's secondary side [17]. If a conventional load is connected to the secondary of the transformer, namely the Point of Common Coupling (PCC), sinusoidal currents with the same frequency as the voltages will be drawn from the mains (see Fig.1.7 **a)**). In simple terms, in the latter case, we have an exclusive linear relationship between the amplitude of the voltages at the PCC ($v_{PCC}$) and currents ($i$) that is defined by the load characteristic impedance [28]. For this reason, conventional loads are also known as linear loads in technical literature [1]. Naturally, with only linear loads connected, the voltages at the PCC contain only a single component $v_1$ at the nominal frequency.

In contrast to linear loads, power converters are based on switching mode operation, and in consequence, their voltage/current characteristic is nonlinear [28, 29]. For this reason, these loads are known in general as Nonlinear Loads (NLL)s. Even if NLLs are supplied with pure sinusoidal voltages, these loads will draw currents with high harmonic content [30]. In effect, the currents drawn by nonlinear loads can be highly discontinuous as is shown in Fig.1.7 **c)** and Fig.1.7 **e)**. Such a discontinuous current is the typical phase current drawn by a passive rectifier, which produces low-frequency harmonics at integer multiples of the nominal/fundamental frequency, at the 5th, 7th,11th,13th, etc. [31]. On the other hand, the currents drawn can also have a harmonic content related to the switching frequency operation of the power converter. The latter is the case on PV inverters and power converters that interface wind turbines [14, 32]. It follows that

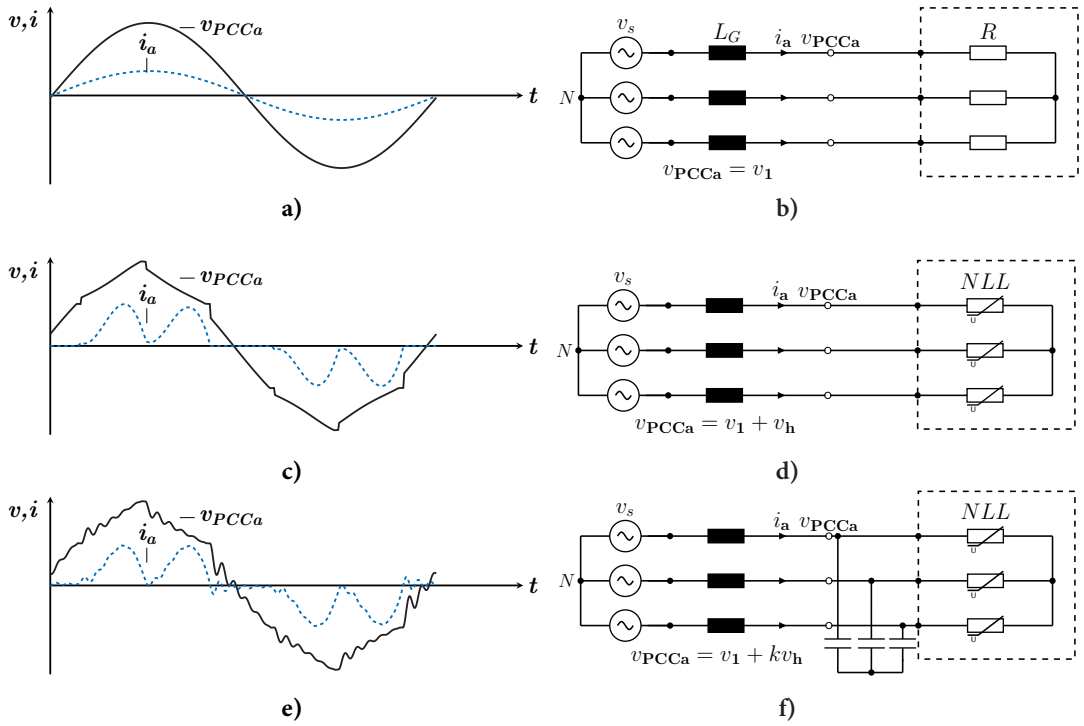


**Fig. 1.7:** Power distribution circuits and electrical waveforms. Power system with a linear load,with a nonlinear load and with nonlinear load under resonance condition. **a)** Voltage at the PCC and mains current (one phase) for distribution system with only a resistive linear load connected. **b)** Three-phase equivalent circuit of power distribution system with solely resistive linear load connected. **c)** Voltage at the PCC and mains current (one phase) for distribution system with passive rectifier connected. **d)** Three-phase equivalent circuit of power distribution system with passive rectifier as nonlinear load connected. **e)** Voltage at the PCC and mains current (one phase) for distribution system with resonance excited by harmonic currents. **f)** Three-phase equivalent circuit of power distribution system with passive rectifier as nonlinear load and capacitor bank connected.

harmonic currents drawn by power converters create harmonic voltage distortion in the power grid at the PCC [3] because the flow of harmonic currents causes a harmonic voltage drop ($v_h$) in the equivalent impedance of the power grid [1, 17]. An illustration of the latter can be seen in Fig.1.7 **d)**. Consequently, the voltage at the PCC will contain not only the single component $v_1$ but also additional harmonic components at different frequencies. Indeed, harmonic voltage distortion degrades the efficiency of the power system, and it could also lead to the heating and malfunctioning of the electrical devices connected [3, 17]. In fact, the most sensitive devices to harmonic distortion are precisely power electronics-based converters [30]. It follows that the voltage distortion caused by harmonics currents needs to be kept below certain limits. Only in this case high power quality and high reliability can be guaranteed in the power grid [17].

### 1.1.3 *Harmonics amplification due to resonances*

Without a doubt, voltage distortion created by harmonic currents increases even further under resonance conditions (see Figss. 1.7 **e)** and 1.7 **f)**). Consider the simplified distribution power system depicted in Fig.1.8 **a)**. The circuit consists only of a nonlinear

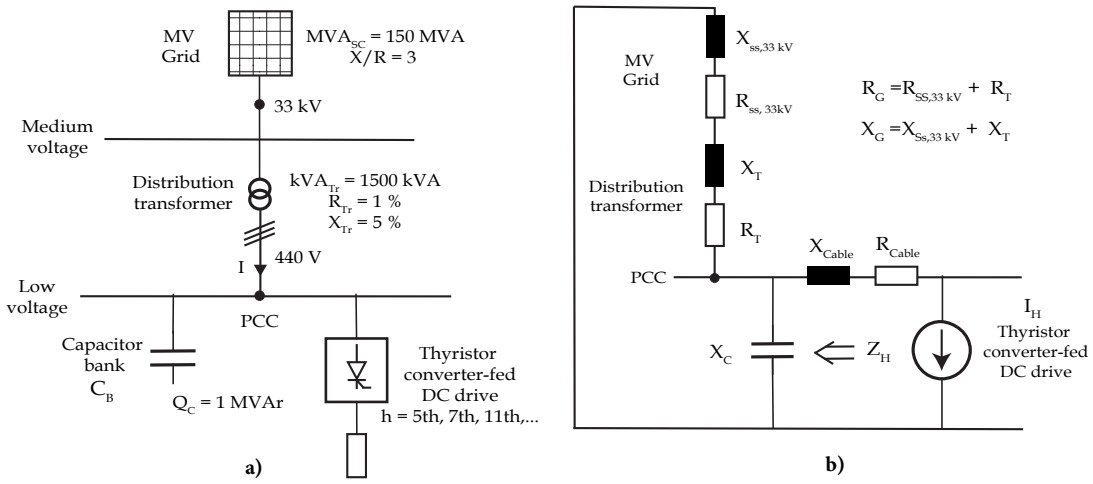


**Fig. 1.8:** Simplified power distribution system and equivalent circuit. Based on [33][34].

load (i.e. three-phase thyristor converter fed DC drive) and a capacitor bank ($C_B$). Furthermore, the per-phase equivalent circuit of this simplified distribution power system can be seen in Fig.1.8 **b)**, where the characteristic impedance of the grid $\underline{Z_G}$ is modeled through the elements $R_G$ and $X_G$. Put simply $\underline{Z_G} = R_G + jX_G$. Notwithstanding, the equivalent reactance of the power grid $X_G$ is proportional to the power grid equivalent inductance $L_G$ according to the relationship $X_G = \omega L_G = 2\pi f L_G$. In contrast the equivalent impedance of the capacitor bank $\underline{Z_C}$ is equal to $\underline{Z_C} = \frac{-j}{\omega C_B} = \frac{-j}{X_C}$. Moreover, the harmonic currents injected by the nonlinear load are modeled through the current source $I_H$. Actually, the total impedance $\underline{Z_H}$ seen by the nonlinear load consists of the grid´s impedance, capacitor´s impedance, and the impedance of the cable between power converter and PCC. Specifically [17][34]:

$$\underline{Z_H} = (\underline{Z_G}||\underline{Z_C}) + \underline{Z_{Cable}} = \frac{(R_G + j\omega L_G)(\frac{-j}{\omega C_B})}{R_G + j\omega L_G - \frac{j}{\omega C_B}} + (R_{Cable} + j\omega L_{Cable}) \tag{1.1}$$

On account of this, when the grid's reactance and capacitor bank's impedance become equal at a particular frequency, the denominator of $(\underline{Z_G}||\underline{Z_C})$ reaches a minimum value [1]. At this frequency, known as the system's resonance frequency $f_R$, the magnitude of the total impedance $\underline{Z_H}$ reaches a very high value. In fact, the resonance frequency of the system can be calculated according to [3]:

$$f_R = \frac{1}{2\pi}\sqrt{\frac{1}{L_G C_B} - \frac{R_G^2}{L_G^2}} \approx \frac{1}{2\pi}\sqrt{\frac{1}{L_G C_B}} \tag{1.2}$$

Altogether, Fig.1.9 shows the impedance of the different elements in the equivalent circuit depicted in Fig.1.8 **b)** and the total impedance $\underline{Z_H}$ seen by the nonlinear load. It can be seen from Fig.1.9 that a resonance results in $\underline{Z_H}$ when the impedances of the grid and the capacitor bank meet at the resonance frequency [33]. Certainly, other resonances could arise in the total impedance seen by the nonlinear load. For example, between the impedance of the distribution transformer and the capacitance of the connecting cables to the medium voltage (MV) grid. According to Mombauer in [34], these resonances are often seen in distribution power systems and are most of the time not damped. Indeed, the situation that is troublesome is when parallel resonances are excited by power

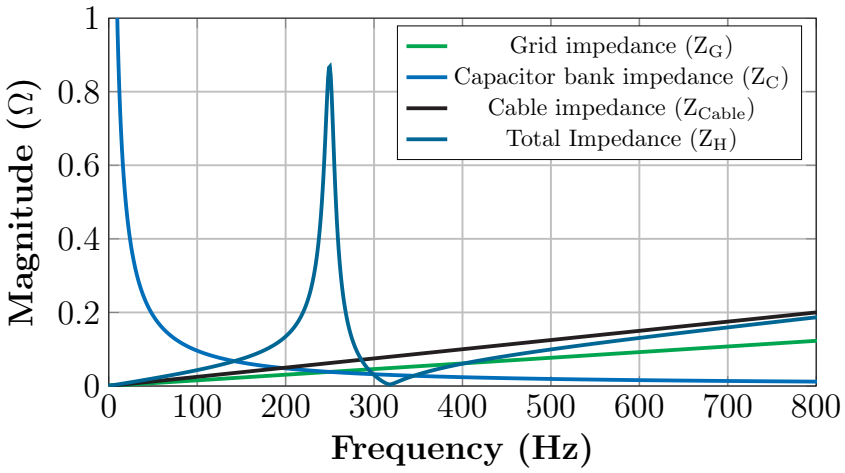


**Fig. 1.9:** Frequency response of the simplified power distribution system depicted in Fig.1.8. Based on [33][34].

converters or nonlinear loads (see Fig.1.7 **f)**). The latter occurs when nonlinear loads generate harmonic currents $I_H$ at or near of the system's resonance frequency. In such a case, harmonic currents and voltages are magnified (e.g. by a factor $k$) in several orders of magnitude as shown in Fig.1.7 **e)**. This amplification of harmonic voltages and currents degrades even further the efficiency of the power system, can cause unwanted tripping in protection devices, and disturbances or interferences in electronics and communication equipment [17]. Even in the worst-case scenario, the harmonics amplification can destroy the electrical devices connected, as happens when capacitor banks are overloaded [1, 35]. As a matter of fact, resonances were not a big problem in the past because the resistive part of conventional linear loads provided enough damping to suppress resonances. However, the situation has drastically changed as power converters have replaced many conventional loads in the last time. For instance, induction motors have been replaced by ASD and light bulbs have been replaced by LED lighting. Moreover, the problem of resonances produced by passive elements is further aggravated by the active control present in modern power electronics systems [36].

Recent scientific work has shown that the interaction between control loops in power converters can lead to self-generated resonance harmonic problems [37]. Take for example the grid-connected power converter depicted in Fig.1.10 **a)**. In the figure, the power converter consists of a two-level Voltage Source Converter (VSC) interfaced to the grid through an LCL filter. Also, the equivalent circuit of the grid-connected converter can be seen in Fig.1.10 **b)**. Obviously, the grid inductance $L_2$ and the ripple filter capacitor $C_F$ form part of the equivalent circuit [38]. Furthermore, the two-level converter, the coupling inductor $L_1$ and the associated control system can be modeled through a current controlled source with transfer function $G_{Cl}(s)$ and an output parallel admittance $Y_{Cl}(s)$ [39]. In fact, the output admittance of the converter $Y_{Cl}(s)$ and the transfer function $G_{Cl}(s)$ depend on the parameters of the converters' inner and outer controllers. In other words, the structure and tuning procedure of the different controllers, namely inner current controller, DC-Bus voltage controller and AC voltage controller will shape the transfer functions $G_{Cl}(s)$ and $Y_{Cl}(s)$. In fact, the real part of the transfer function $Y_{Cl}(s)$ can take a positive, a negative, or a zero value depending on the controllers' parameters. In particular when the real part of $Y_{Cl}(s)$ takes a positive value, the entire system represented by the equivalent circuit in Fig.1.10 **b)** becomes an stable system. In the latter case, the power converter operates in the long term without problems. In

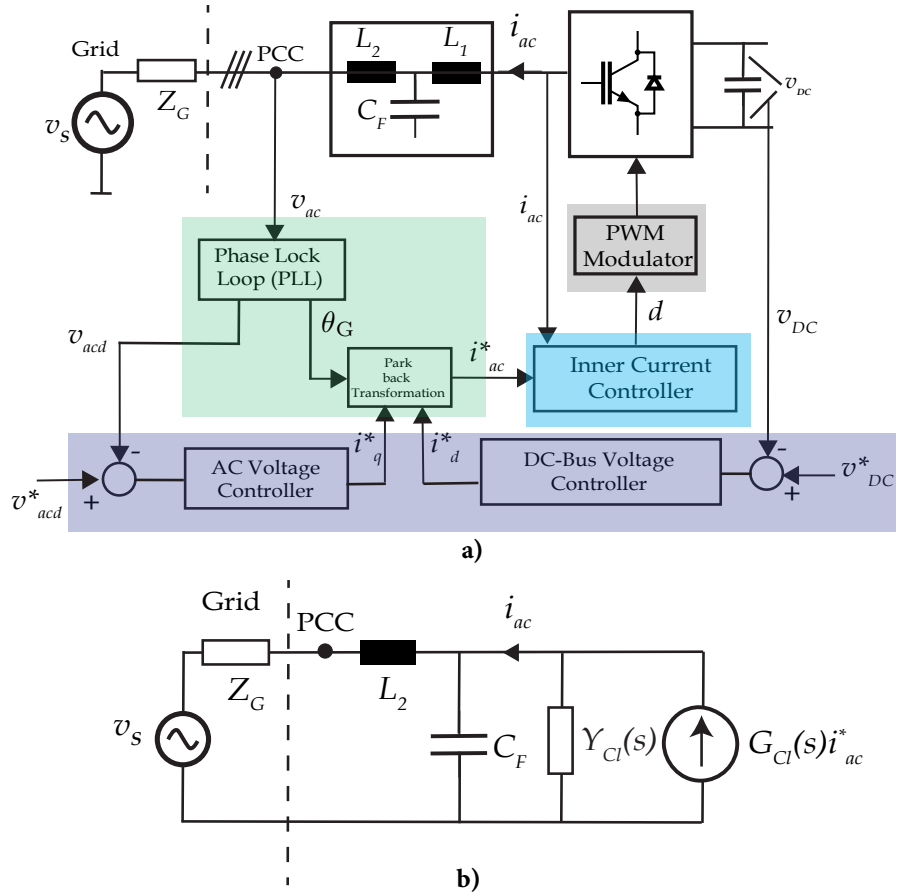


**Fig. 1.10:** Grid connected power converter and equivalent circuit based on specific control loops. Based on [40].

contrast, the entire system will be critically stable if the real part of $Y_{\mathrm{Cl}}(s)$ becomes zero or comes close to zero. Under this circumstance, it is said that the power converter produces a resonance in the power system that could be excited by the power converter itself (through the equivalent current source $G_{\mathrm{Cl}}(s)$) or by other power converters connected to the system. Certainly, the real part of $Y_{\mathrm{Cl}}(s)$ can turn negative as well, which will lead to a totally unstable system (i.e. harmonic instability [39]). In this case, the power converter will be disconnected from the power system by the tripping action of the protection devices. On this basis, Wang and Blaabjerg in [40] studied the root cause of abnormal frequencies measured at the output of a power converter and related those frequencies to the individual controllers. As a result, they found the relations stated in Table 1.1. For instance, the current controller structure and its parameters can produce harmonic oscillations in a frequency range between three times the fundamental frequency ($3f_1$) and half of the switching frequency of the converter ($f_{\mathrm{Sw}}/2$). Likewise, the Phase-lock-loop (PLL) structure and parameters can produce oscillations between the fundamental frequency and three times the fundamental frequency.

On this basis, numerous studies have reported harmonic resonances caused by the active control of power electronics converters. For example, Ackermann et al. in [41] studied a PV farm consisting of six identical string PV inverters. They found out that if the PV farm is connected to a weak grid (e.g. $L_G$ = 315 $\mu$H), and for certain constellation of current controller parameters, the six PV inverters can generate and trigger a harmonic resonance at 549 Hz as it is shown in Fig. 1.11. Similarly, Zou et al. in [42] studied a

**Table 1.1:** Correlation between abnormal frequencies produced by a power converter and individual control loops. (Nomenclature $f_1$: Fundamental frequency, $f_s$: Converter´s switching frequency)

| Denomination | Low frequency boundary | High frequency boundary | Control Loop responsable |
|---|---|---|---|
| Sub-synchronous oscillations | $< f_1$ | $f_1$ | DC-Bus Voltage Controller AC Voltage Controller |
| Near-synchronous oscillations | $f_1$ | $3f_1$ | Phase Lock Loop (PLL) |
| Harmonics oscillations | $3f_1$ | $f_{Sw}/2$ | Inner current controller |
| Sideband oscillations | $f_{Sw}/2$ | $f_{Sw}$ | PWM modulator |

harmonic instability incident produced in a MMC-HVDC converter at the HVDC station in Luxi, Yunnan, China. Actually, the harmonic instability event reported in [42] can be seen in Fig. 1.12 where the authors measured a 1270 Hz resonance induced by the inner current controller of the MMC-HVDC converter. In the latter case, the inherent delay in the closed current control loop caused the resonance. To put it differently, the control delay in the current controller caused negative damping triggering a resonance in the entire power system. Finally, Buchhagen et al. in [43] reported resonances at 451 Hz in an MMC-HVDC converter that interfaces the North Sea wind farm with continental Germany. In the latter case, the 451 Hz resonance was triggered by the interaction of the control loops and new cables connected to the wind farm. All in all, the interaction between control loops could produce zero or even negative damping worsening preexisting resonances in the power system.

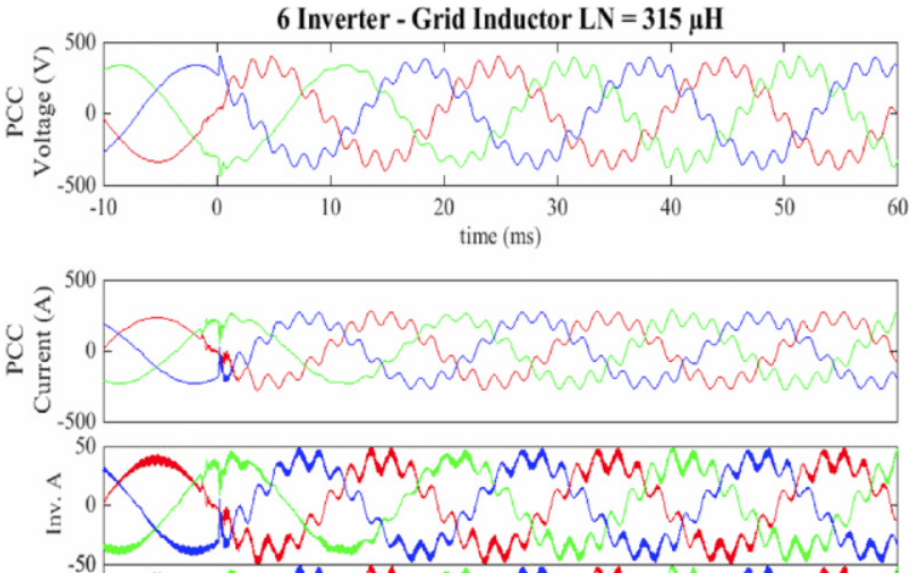


**Fig. 1.11:** Oscillations in PV system with harmonic resonances [41]. IEEE copyright ©2016 (Reproduced with permission of IEEE)

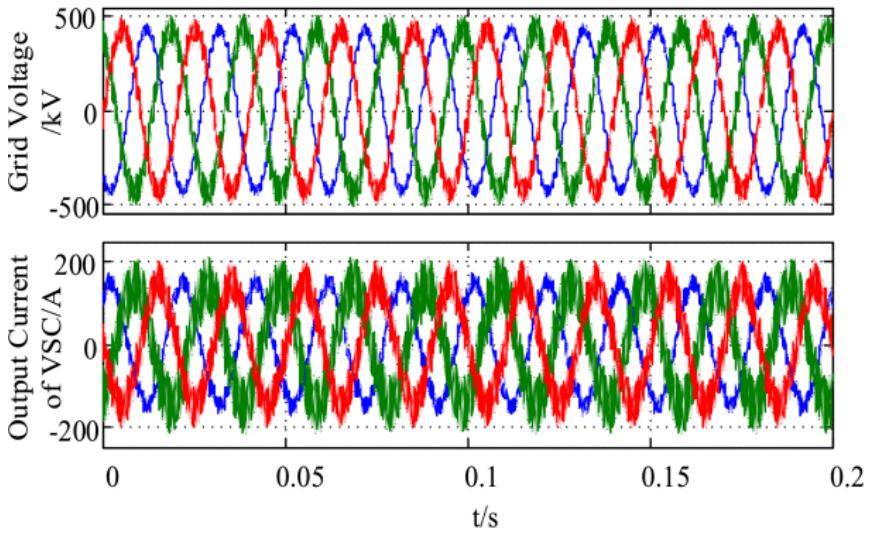


**Fig. 1.12:** Harmonic instability phenomena with MMC-HVDC in the Southern Power Grid,China [42]. IEEE copyright ©2018 (Reproduced with permission of IEEE)

## 1.2 MOTIVATION FOR RESEARCH

Connecting elements with resistive or ohmic behaviour adds damping to power systems. Therefore, harmonic resonances can be suppressed by connecting resistive elements as dampers to the power grid [1]. In detail, the additional damping can be provided either by passive dampers or active dampers installed in parallel to the loads [44]. In particular, Fig. 1.13 shows the power circuits of two second-order passive dampers and their frequency response. Both passive dampers are very simple and can be built using an inductor $L_1$, which exhibits an inherent resistance $R_1$, a capacitor $C_1$, and a damping resistor $R_S$. Actually, the passive damper depicted in Fig. 1.13 **a)** is denominated parallel-resonant damper [45]. The parallel-resonant damper is constituted by the series connection of a resonant tank, formed by $L_1$ and $C_1$, and the resistor $R_s$. The resonance tank blocks the flow of currents at the nominal frequency (e.g. 50 Hz) on the resistor $R_s$. On account of this, only currents at harmonic frequencies circulate over the resistor $R_s$, and currents at the nominal frequency (e.g., 50 Hz) do not flow over the resistor $R_s$. For this reason, power losses over the resistor $R_s$ are exclusively due to harmonic currents. Clearly, the resonant tank prevents unnecessary losses in the resistor $R_s$ that otherwise will be caused by currents at the nominal frequency. After all, a passive damper should exhibit resistive behavior only at harmonic frequencies. Naturally, the element $R_s$ determines completely the passive damper impedance at harmonic frequencies as can be seen in Fig. 1.13 **b)**. On the other hand, the passive damper depicted in Fig. 1.13 **c)** is denominated as series-resonant damper [44]. The latter is formed by the parallel connection of two circuit branches. The first branch is constituted only by the damping resistor $R_S$. Moreover, the second branch consists of the series connection of the elements $R_1$, $L_1$ and $C_1$. In fact, $L_1$ and $C_1$ are tuned so that their impedance cancel each other out at the nominal or fundamental frequency. Thus, at the nominal or fundamental frequency, the effective impedance of the second branch is determined exclusively by $R_1$. If $R_1$ is smaller than $R_S$, as is normally the case, the current at the nominal frequency (i.e. fundamental current) will flow mainly over the lower branch. Thus, losses due to the nominal or fundamental frequency will be avoided over the damping resistor $R_S$.

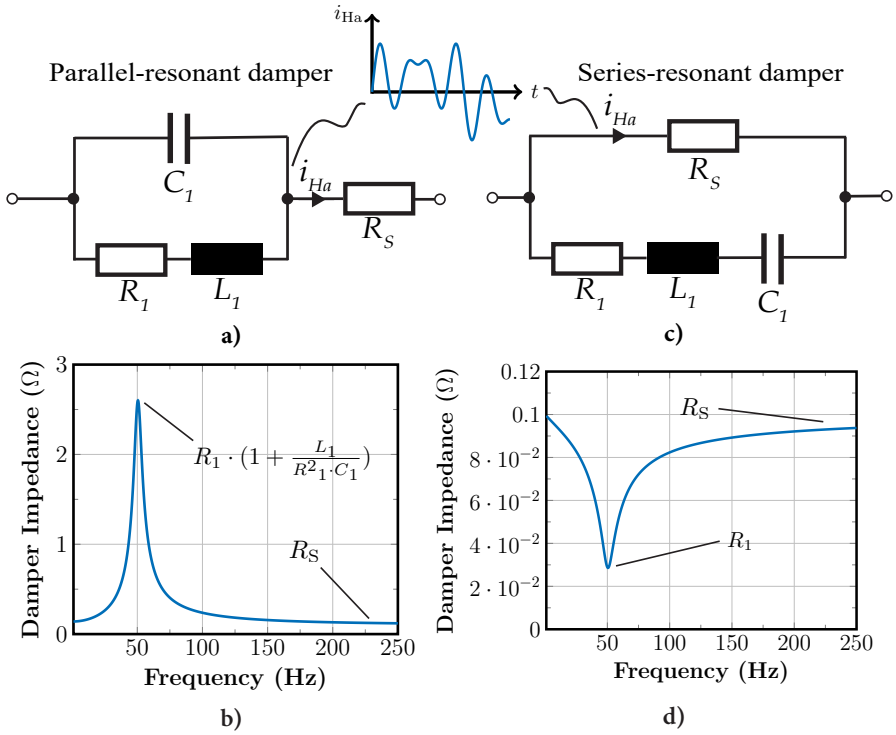


**Fig. 1.13:** Second-order passive dampers where only one-phase of the power circuit is shown **a)** Power circuit of second-order parallel-resonant damper. **b)** Impedance-frequency plot of parallel-resonant damper. **c)** Power circuit of second-order series-resonant damper. **d)** Impedance-frequency plot of series-resonant damper. Based on [45][44].

Moreover, just like the parallel-resonant damper, the impedance of the series-resonant damper at harmonic frequencies is defined by $R_S$ too. It follows that if the parallel-resonant damper or series-resonant damper are installed in parallel to the loads, they will provide enough damping to suppress harmonic resonances that could arise in the power system [44, 45]. For example, suppose that the parallel-resonant damper depicted in Fig. 1.13 **a)** is connected next to the power converter on the power system depicted in Fig. 1.8. In that case, the frequency response of the simplified power distribution system (see Fig. 1.9) will change. In particular, the parallel-resonant damper will reshape the frequency response depicted in Fig. 1.9 as in Fig. 1.14. In detail, Fig.1.14 shows the total impedance $Z_H$ seen by the power converter in the power circuit shown in Fig.1.8 with and without passive damper. Specifically, the $Z_H$´s frequency response that includes a parallel-resonant damper connected to the PCC for three different values of damping resistor has been plotted. In other words, the behavior of the total impedance´s frequency response including the passive damper was analyzed for three different magnitudes of $R_s$. From Fig. 1.14, it can be concluded that the resonance is damped out from the total impedance frequency response by the passive parallel-resonant damper. In fact, it can be inferred that the smaller the damping resistor $R_s$ is, the larger is the damping introduced into the system. Although passive dampers effectively suppress harmonic resonances, passive dampers suffer from two main problems. First, passive dampers are not flexible solutions, and they might lose their damping properties if grid conditions change. Second and particularly troublesome is that passive dampers exhibit significant power losses due to the flow of harmonic currents through $R_s$ [17, 36]. In fact, passive dampers absorb harmonic active power from the power system in the form of $P_H = 3R_s I^2_{Ha}$ [46][47]. Certainly, the problem of concern is that passive dampers dissipate the absorbed harmonic

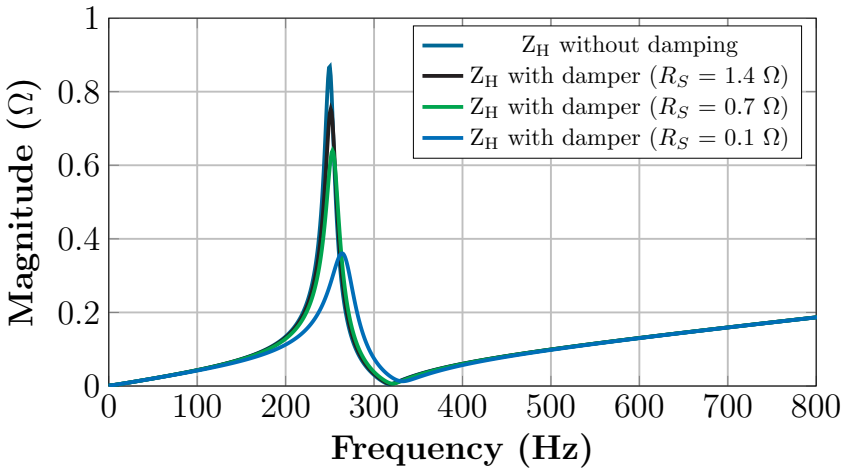


**Fig. 1.14:** Frequency response of the simplified power distribution system in Fig.1.8 with different values of damping resistor in the passive damper.

power as heat on their resistive elements leading to energy waste. The alternative to a passive damper is its active counterpart, the active damper. The active damper is also known in scientific literature as Voltage-driven shunt active power filter (VSAPF) [48], and in this dissertation, both names are used interchangeably. In detail, an active damper is a power electronics system (see Fig. 1.15 **a)**) based on a VSC with a self-supporting DC-Bus connected to the power mains through coupling inductors. It emulates a virtual resistance of $R_s$ ($\Omega$) at harmonic frequencies by drawing harmonic currents $i_{CH}$ that are proportional and in phase to the harmonic voltages $v_{PCCH}$ at the PCC following the control law $i_{CH} = \frac{v_{PCCH}}{R_s}$ [48]. To this end, the average output voltage of the VSC is adjusted, considering in the process the actual voltage at the PCC, in such a way that the currents flowing over the inductors resemble the shape of the harmonic currents that a pure resistor would draw (see Fig. 1.15 **b)**). Although the capability of active dampers to suppress resonances has been widely studied and discussed in literature [49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62], very little is known about the harmonic power absorption that takes place on active dampers. In fact, only a couple of scientific papers [63][64] made statements about the absorbed harmonic active power and its potential transformation (i.e., harmonic power recovery) to avoid the energy waste. On this basis, Table 1.2 lists all the relevant scientific publications related to voltage-driven

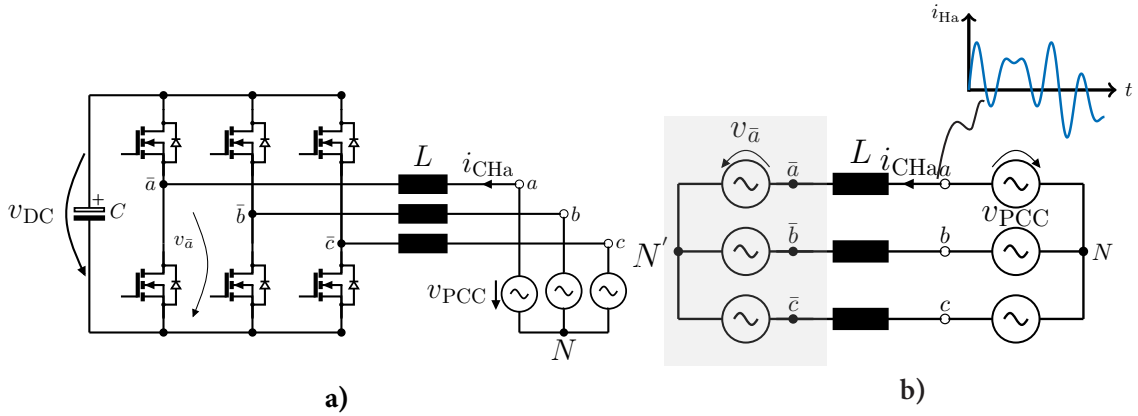


**Fig. 1.15:** Power circuit of active damper or VSAPF **a)** Power electronics circuit of the active damper. **b)** Equivalent circuit of the active damper. [31][48].

shunt active power filters (e.g., [49]- [62]) up to the year 2022. Furthermore, Table 1.2 shows very briefly the contribution made by each scientific publication and indicates if the resonance suppression or the harmonic power recovery feature of the VSAPF has been investigated therein.

**Table 1.2:** Summary of literature review about active dampers

| | | Resonance supression investigation | | Harmonic power transformation investigation | |
|---|---|---|---|---|---|
| Ref. | Contributions | Type of Analysis | Verification | Type of Analysis | Verification |
| [49] | Active damper technology was introduced by Kawahira et al. in 1983; however, the first scientific publication in English that discussed the damping of harmonic resonances using an active damper or VSAPF was this contribution by Akagi. Contributions:<br>1.- Analog control structure for the VSAPF was presented.<br>2.- VSAPF´s stability analysis with simplified power grid dynamics was carried out.<br>3.- Investigation of the best place for the VSAPF´s installation in a radial distribution system was performed. | Qualitative Quantitative | Through computer simulations | No analysis performed | Not performed |
| [50] | A selective harmonic control structure for SAPFs is proposed in this paper. The selective compensation scheme can be used with the load current, supply current, and voltage detection control strategies to command a SAPF. | Qualitative | Computer simulations and experimental validation | No analysis performed | Not performed |

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Table 1.2 – continued from previous page

| | | Resonance supression investigation | | Harmonic power transformation investigation | |
|---|---|---|---|---|---|
| Ref. | Contributions | Type of Analysis | Verification | Type of Analysis | Verification |
| [51, 52] | 1.- Digital control structure to command the VSAPF is presented. 2.-Implementation of automatic resistance adjustment in dependency of the grid conditions. | Qualitative Quantitative | Experimental validation | No analysis performed | Not performed |
| [53] | The harmonic resonance damping capability was added to a boost power factor correction (PFC) converter. To this end, a modified control structure for the PFC converter was introduced and validated through experiments. | Qualitative | Experimental validation | No analysis performed | Not performed |
| [54] | The harmonic resonance damping functionality was added to inverter-based distributed generators with adaptive resistance adjustment under peak fundamental power demand. | Qualitative | Experimental validation | No analysis performed | Not performed |
| [55] | Analysis of the capability of an active damper or VSAPF to mitigate harmonic propagation due to parallel and series resonance conditions. Verification that the best place to install an active damper is at the end of the supply feeder . | Qualitative | Through computer simulations | No analysis performed | Not performed |

Continued on next page

Table 1.2 – continued from previous page

| | | Resonance supression investigation | | Harmonic power transformation investigation | |
|---|---|---|---|---|---|
| Ref. | Contributions | Type of Analysis | Verification | Type of Analysis | Verification |
| [56] | Selective harmonics damping was added as ancillary functionality to an inverter-based distributed generator. In contrast with the work presented in [54], which dealt with broadband resonance damping, a selective harmonics damping scheme is proposed in this contribution. The proposed scheme was validated through experiments. | Qualitative Quantitative | Computer simulations and experimental validation | No analysis performed | Not performed |
| [57] | The harmonic resonance damping functionality was implemented in a hybrid active power filter. The latter combines a passive filter with an active power filter in series connection. This is done with the goal to reduce the power rating of the power quality conditioner. | Qualitative Quantitative | Computer simulations and experimental validation | No analysis performed | Not performed |
| [58] | An active damper that contains current resonant controllers within its control structure is proposed and validated through experiments. | Qualitative Quantitative | Computer simulations and experimental validation | No analysis performed | Not performed |
| [59] | A shunt active power filter that combined the load current and voltage detection control strategies was proposed. The proposed compound scheme was validated through experiments in a real industrial facility. | Qualitative Quantitative | Experimental validation | No analysis performed | Not performed |

Continued on next page

Table 1.2 – continued from previous page

| | | Resonance supression investigation | | Harmonic power transformation investigation | |
|---|---|---|---|---|---|
| Ref. | Contributions | Type of Analysis | Verification | Type of Analysis | Verification |
| [60] | Similar to [59], a shunt active power filter that combines the load current and voltage detection control strategies is proposed in this contribution. However, in this scientific work, the proposed compound scheme was validated only through computer simulations. | Qualitative Quantitative | Through computer simulations | No analysis performed | Not performed |
| [61] | A shunt active power filter based on voltage detection without grid-voltage sensors (Grid-Voltage Sensorless) is proposed. The grid voltages are calculated using only the currents measured at the output of the VSAPF. | Qualitative Quantitative | Computer simulations and experimental validation | No analysis performed | Not performed |
| [62] | The stability of an active damper is analyzed using the 2-Norm small-gain stability criterion. Furthermore, in case that instability on the active damper is detected, a stabilization algorithm is also proposed in this contribution. | Qualitative Quantitative | Through computer simulations | No analysis performed | Not performed |

Continued on next page

Table 1.2 – continued from previous page

| | | Resonance supression investigation | | Harmonic power transformation investigation | |
|---|---|---|---|---|---|
| Ref. | Contributions | Type of Analysis | Verification | Type of Analysis | Verification |
| [63] | The installation of an active damper in series with a capacitor bank is proposed in this contribution. Consequently, any possible resonance caused by the interaction between the capacitor bank and the grid impedance in a distribution system can be suppressed. Further, this publication analyzed in detail the VSAPF's damping capability and discussed only qualitatively the harmonic power absorption in the active damper. | Qualitative Quantitative | Computer simulations and experimental validation | Qualitative | Not performed |
| [64] | The harmonic resonance damping capability was added to a single phase AC-DC converter. This paper suggested very roughly that harmonic active power can be transformed to fundamental power but provided no further details. | Qualitative | Experimental validation | Qualitative | Not performed |

In particular, Shen et al. in [63] stated that the absorbed harmonic active power could be used to compensate for a fraction of the active damper's power losses. On the other hand, Ryckaert et al. in [64] mentioned somehow ambiguously that the absorbed $P_H$ could be converted into fundamental power $P_1$ and returned to the power system (i.e., harmonic power recovery). However, only vague qualitative statements were made in the former two studies, neither rigorous mathematical analysis nor experimental results demonstrating the recovery of harmonic active power were presented. Therefore, to the best of the author's knowledge, an exhaustive examination of the VSAPF's capability to transform the absorbed $P_H$ and experimental validation of the harmonic power recovery concept were not carried out in the mentioned publications or elsewhere. Thus, the precise mechanisms of $P_H$ processing through active dampers remain unclear and constitute a research gap in this area that should be further investigated.

## 1.3 PROBLEM STATEMENT

Inductive and capacitive elements connected to a power grid shape the frequency response of the power system. Moreover, a parallel resonance in the frequency response of the power system arises when the inductive and capacitive impedances become equal at a particular frequency. If the parallel resonance matches the frequency of a harmonic current generated by a power converter connected to the grid, the harmonic current and voltage are magnified by several orders of magnitude, causing many problems (e.g., overloading of capacitors, heating, and destruction of devices). The conventional method to suppress such resonances is introducing passive dampers made of resistive elements into the grid. However, this solution is not flexible and exhibits high harmonic power losses leading to energy waste. In detail, observations indicate significant power losses due to harmonic currents passing through passive dampers. Indeed, passive dampers absorb harmonic active power and dissipate it as heat on their resistive elements leading to energy waste. On the other hand, the passive damper counterpart is the active damper. The active damper is a power electronics-based system that emulates a virtual resistance at harmonic frequencies. Generally speaking, power electronics technology deals with the conversion and control of electrical power. In this regard, very little is known about the harmonic power absorption in active dampers, and it is not known if active dampers can transform the harmonic power absorbed and avoid energy waste. The purpose of this Ph.D. research is to investigate and to understand how an active damper can process harmonic power, perform harmonic power recovery and whether it contributes to reduce power consumption in an industrial facility. On this basis, Fig. 1.16 illustrates the relationship between the practical problem and the research problem addressed in this dissertation.

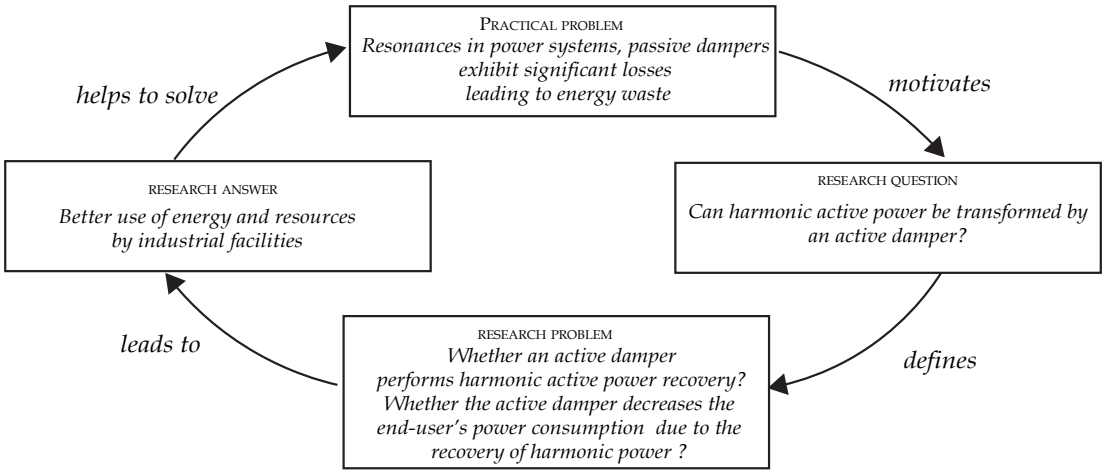


**Fig. 1.16:** Relationship between the practical problem and the research problem addressed in this Ph.D. work.

Furthermore, Table 1.3 summarizes the relevant publications found during the literature review (see Table 1.2) and contrasts them with the research carried out in this Ph.D. dissertation. In detail, Table 1.3 states whether a particular scientific work has addressed the harmonic mitigation or harmonic power recovery characteristics of VSAPFs qualitatively or quantitatively. Moreover, Table 1.3 also indicates if simulation results, experimental results, or both were presented in each publication. From the table, it can be seen that almost all the previous scientific work was focused on the harmonic mitiga-

tion capability of voltage-driven shunt active power filters where qualitative, quantitate analysis and experimental validation were carried out. Only two scientific publications addressed the subject of harmonic active power transformation, namely Shen et al. in [63] and Ryckaert et al. in [64]. However, the last two publications only qualitatively discussed the harmonic power recovery concept and provided no experimental results. It follows that, the harmonic power recovery characteristic of VSAPF was investigated neither in a quantitate manner (mathematical analysis) nor experimentally verified previous to this Ph.D. work as seen in Table 1.3.

**Table 1.3:** Comparison between this existing literature and this Ph.D. research work

| Ref. | Harmonics distortion/Resonance mitigation investigation | | | | Harmonic power transformation investigation | | | |
|---|---|---|---|---|---|---|---|---|
| | Qualitative Analysis | Quantitative Analysis | Simulation validation | Experimental validation | Qualitative Analysis | Quantitative Analysis | Simulation validation | Experimental validation |
| [49] | ✓ | ✓ | ✓ | X | X | X | X | X |
| [50] | ✓ | X | ✓ | ✓ | X | X | X | X |
| [51, 52] | ✓ | ✓ | X | ✓ | X | X | X | X |
| [53] | ✓ | X | X | ✓ | X | X | X | X |
| [54] | ✓ | X | X | ✓ | X | X | X | X |
| [55] | ✓ | X | ✓ | X | X | X | X | X |
| [56] | ✓ | ✓ | ✓ | ✓ | X | X | X | X |
| [57] | ✓ | ✓ | ✓ | ✓ | X | X | X | X |
| [58] | ✓ | ✓ | ✓ | ✓ | X | X | X | X |
| [59] | ✓ | ✓ | X | ✓ | X | X | X | X |
| [60] | ✓ | ✓ | ✓ | X | X | X | X | X |
| [61] | ✓ | ✓ | ✓ | ✓ | X | X | X | X |
| [62] | ✓ | ✓ | ✓ | X | X | X | X | X |
| [63] | ✓ | ✓ | ✓ | ✓ | ✓ | X | X | X |
| [64] | ✓ | X | X | ✓ | ✓ | X | X | X |
| This work | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

## 1.4 HYPOTHESIS

An active damper that exhibits power losses smaller than the harmonic active power intake (i.e., an ultra-low losses VSAPF) will recover a significant amount of harmonic active power. Besides, the ultra-low losses VSAPF will decrease the power consumption in a distribution power system.

## 1.5 RESEARCH OBJECTIVES

This Ph.D. thesis aims to investigate how an active damper can process the harmonic active power intake and perform harmonic power recovery. Harmonic power recovery in this context is understood as the process of transforming the harmonic power absorbed into fundamental power that is injected back into the power system. The last question addressed in this work is to investigate whether the mentioned transformation process contributes to reduce the power consumption of an industrial facility. In brief, the main objective of this dissertation is to study and develop a VSAPF to perform harmonic

distortion mitigation and harmonic power recovery. The main focus is to answer questions regarding the VSAPF's harmonic power recovery capability and its contribution to reduce power consumption in a distribution power system. The last two aspects have not been addressed in the past and are the novelties brought by this Ph.D. research work. In detail, the Ph.D. research objectives are defined as follows:

- To obtain knowledge about the state-of-the-art of SAPFs.
  - To study the system control structures commonly used in SAPFs.
  - To study the converter topologies commonly used in SAPFs.
- To investigate the interaction between the voltage-driven shunt active power filter (VSAPF) and the power grid from a power exchange point of view.
  - To analyse the harmonic active power absorption made by the VSAPF.
  - To examine how the harmonic active power absorbed by the VSAPF can be converted and injected back into the power grid as fundamental active power.
  - To study the power balance flow of a distribution system that has a VSAPF with harmonic power recovery capability connected to it.
- To investigate and compare different VSAPF converter topologies, control strategies, and operation parameters in terms of power losses. Furthermore, to determine which combination of these is the most promising solution to maximize the harmonic active power recovery.
- To develop current controllers for the inner control loop of the VSAPF, with the aim to improve the VSAPF's stability.
- To develop and validate the VSAPF for harmonics mitigation and harmonic power recovery in computer simulations and hardware experiments.

### 1.5.1 *Specific Research Questions*

In order to reach the objectives set on this Ph.D. work, the following research questions have been formulated:

1. What is the state-of-the-art of shunt active power filters? (addressed in Chapter 2)
2. Does an active damper perform harmonic power recovery ? (addressed in Chapter 4)
   a) What happens with the harmonic active power absorbed by the VSAPF during the virtual resistance emulation? (addressed in subsections 4.4.1 and 4.4.2, and in sections 4.6 and 4.7)
   b) How can the VSAPF transform the absorbed $P_H$ to $P_1$ and perform harmonic active power recovery? Which are the transformation mechanisms? (addressed in subsections 4.4.3, 4.4.4, and 4.4.5 and in section 4.6)
3. An active damper with harmonic power recovery functionality, does it reduce the fundamental power demanded by the end-user in comparison with a passive damper? (addressed in Chapter 5)
4. What is the most suitable VSAPF topology to maximize the harmonic active power recovery? (addressed in Chapter 6)

5. What factors influence the stability of the VSAPF when it is connected to the power system or power grid? (addressed in Chapter 7 and Appendix A)

## 1.6 RESEARCH METHODOLOGY AND FRAMEWORK

### 1.6.1 *Approach and Research Methodology*

The methodology used in this research project is mathematical theoretical analysis, numerical simulations, and experimental verification. Regarding the mathematical analysis, this research work investigated the active damper and power system interaction from a power exchange point of view. This interaction was described mathematically starting from the basic physics law of energy conservation, the energy stored in capacitors and inductors, and the active damper's working principles. Furthermore, the mathematical models derived were verified through computer simulation models. In particular, the electromagnetic-transient programs MATLAB/Simulink and PLECS were employed to perform the simulations. First, the simulation models were used to study the harmonics mitigation effectiveness and the capability of the VSAPF to transform harmonic active power. Naturally, the simulation models enabled the possibility of studying the power balance at different frequencies between the VSAPF and the power system. The simulation results confirmed the solutions of the differential equations proposed in this dissertation to explain mathematically the mechanism of harmonic active power recovery. Second, different power circuit topologies for the VSAPF were also evaluated via computer simulations. In particular, different power topologies at different operating points were simulated. The overall VSAPF's power losses were estimated on each simulation using accurate models for power semiconductors and inductive components. With all these results, it was possible to conduct a comparative evaluation among the power topologies in terms of power losses. Arising out of this comparative evaluation, it was possible to determine which power topology produced the lowest power losses or, differently said, it was possible to determine the most promising VSAPF's power circuit to maximize the recovery of harmonic active power. Third, simulation models were also used to investigate the factors influencing the active damper's stability. From the simulations, it was found that the performance of the inner current controller plays a significant role in the active damper's stability. On this basis, and similar to the power circuit topologies, different current controller structures were implemented and compared through computer simulations. From the current controllers' comparative evaluation, it was found that the larger the bandwidth of the VSAPF's current controller is, the better is the VSAPF's stability for low values of emulated resistance. Finally, the harmonic power recovery feature of VSAPFs was experimentally verified in two different hardware setups. The first hardware setup used a dSPACE MicroLab-Box as VSAPF's controller and a SEMIKRON SEMITEACH two-level inverter as VSAPF's power circuit. This first setup was built in the laboratory. It was used to validate the VSAPF's control system developed in this dissertation and to verify the absorption of harmonic active power in the VSAPF. The second hardware setup was an 82 kVA two-level SiC-based VSAPF installed in a test bench in the facilities of our research partner Condensator Dominit GmbH. Indeed, this second hardware setup was used to validate experimentally the recovery of harmonic active power through a VSAPF.

### 1.6.2 *Theoretical and empirical framework*

The theoretical framework used in this research includes instantaneous power theory [48] for the control of active power filters, power flow under non-sinusoidal conditions, and advanced design of power electronics based systems. On the other hand, the empirical framework of this research is constituted by observations of significant harmonic power losses on passive dampers. Those observations were made by the personnel of Condensator Dominit GmbH. In addition, the empirical framework is reinforced by the fact that power electronics technology can be used to condition and process electrical power energy from one form to another.

## 1.7 LIMITATIONS

### 1.7.1 *Balanced power systems*

As was mentioned in section 1.1.2, nonlinear loads draw harmonics currents from the AC mains, which degrade the efficiency of the distribution system and can cause malfunctioning of the electrical devices connected to it. Additionally, nonlinear loads can produce unbalance in power systems [17]. For example, if two-phase nonlinear loads (i.e., nonlinear loads supplied only with two of the three phases) are connected to three-phase three-wire power systems, or if single-phase nonlinear loads are connected to three-phase four-wire power systems, load balancing problems could arise [65]. In short, if unbalanced nonlinear loads are connected to a distribution system, harmonics and unbalance will degrade power quality even more than sole harmonics produced by balanced nonlinear loads [66, 67]. Consider, for example, a three-phase four-wire power system with balanced nonlinear loads. In the latter case, the $h$th harmonic voltage of phase $b$, will lag $h$ times 120° behind the $h$th harmonic voltage of phase $a$. On the same note, the $h$th harmonic voltage of phase $c$ will lag behind the $h$th harmonic of phase $a$ by $h$ times 240° [47]. Moreover, harmonics that are multiples of three times the nominal frequency (i.e., triplen harmonics) have a phase shift of three times 120° or three times 240° degrees. It follows that if three phases are considered altogether, triplen harmonics result in co-phasial phasors that are known as zero sequence components [1, 68]. In contrast, harmonics that are not triplen harmonics have either positive or negative sequences, and they cancel out if the three phases are considered as a whole [69, 70]. It turns out that in case of balanced nonlinear loads in a three-phase four-wire power system, all the triplen harmonics generated are summed up at the neutral conductor producing its overheating and forcing the oversizing of its conduction area [71, 72]. The latter situation worsens in case of unbalanced nonlinear loads, where residual currents due to the unbalance of positive and negative sequence components will also be added to the zero components in the neutral conductor aggravating the neutral cable overheating [70]. Moreover, Nicolae et al. in [73] claim that unbalance can also cause voltage sags and affect the magnetization currents of transformers within distribution power systems.

Furthermore, to analyze unbalanced nonlinear loads, it is necessary to resort to the symmetrical components method [71, 72],[74] and to the theory of three-phase systems with non-sinusoidal waveforms [47]. The latter combination of theoretical frameworks makes the study of unbalanced nonlinear loads very complex and difficult to handle [75, 69]. On this basis, and since this dissertation aims to investigate the power exchange between VSAPF and the power grid for the first time, only balanced linear and nonlinear loads are considered in this research. The latter was done for simplicity in this exploratory

quantitative research about harmonic power recovery through VSAPFs. Additionally, only a balanced VSAPF (i.e, a VSAPF that emulates the same virtual resistance on each phase) was considered in this dissertation. With this in mind, per-phase equivalent circuits were used for a large portion of the circuital analysis and circuits equations developed in this Ph.D. work. Altogether, this research work is limited to three-phase balanced systems, and the study of the power exchange between the VSAPF and an unbalanced power system is suggested as future work.

### 1.7.2 *Three phase three-wire distribution power systems*

This research work is limited to three-phase three-wire distribution power systems (e.g., power grids in industrial facilities). Because nonlinear loads are increasing rapidly in distribution power systems, harmonic pollution at the distribution level is considerable. Therefore, it is in this type of power system where a significant amount of harmonic active power can be absorbed and processed through active dampers. Although harmonic voltage distortion also exists on other levels, such as at the transmission level, the harmonic voltage distortion at this level is commonly low (< 5%) [1]. Therefore, it can be inferred that the amount of harmonic active power is negligible at the transmission level, and thus no harmonic energy recovery would be possible. For this reason, this research work has focused solely on distribution power systems.

### 1.7.3 *Mitigation of parallel resonances created by capacitive loads in distribution systems*

This Ph.D. research work only studied distribution power systems with parallel resonance problems. As mentioned in subsection 1.1.3, parallel harmonic resonances arise due to the interaction of capacitive loads and the distribution system impedance. Examples of capacitive loads in distribution systems include capacitor banks and ripple filters of grid-tie power converters. Furthermore, the distribution transformer and feeder impedances form the distribution system impedance. With this in mind, this dissertation only covered the mitigation of parallel resonances produced by capacitive loads and the distribution system impedance through an active damper. In addition, this research work also examined the mitigation of the harmonic distortion fed from outside the distribution power system. The latter was regarded as background harmonic distortion in the secondary side of the distribution transformer that supplies the distribution system in the mathematical analysis carried out in this investigation. In contrast, neither the suppression of series resonances nor resonances upstream of the distribution system feeder (i.e., parallel resonances at the transmission level) were considered in this dissertation.

## 1.8 THESIS OUTLINE AND ORIGINAL CONTRIBUTIONS

This Ph.D. Thesis is organized in 8 chapters, where each chapter addresses one particular question of the research questions stated in section 1.5.1. In particular, original contributions are provided in chapters 2, 4, 5, 6, and 7. Furthermore, in the following, an overview of the content of each of the chapters in this dissertation is given:

- **Chapter 1** describes the context and background of the Ph.D. topic, states the research problem, and defines the research questions of this dissertation. In brief, this chapter describes the practical problem tackled by this thesis and explains from where this problem comes. Put it simply, the practical problem that is addressed in

this work is the energy waste produced by passive dampers. Certainly, there was a call for research because a lack of knowledge existed regarding the capability of the passive damper's counterpart, the active damper, to process harmonic active power and avoid the energy waste.

- **Chapter 2** provides a comprehensive review of the state-of-art for SAPFs. First, this chapter contrasts the different control strategies to command a SAPF, namely the voltage-based and the current-based control strategies. On this basis, this chapter deeps into a profound study of the effectiveness of each of the control strategies to perform harmonic voltage mitigation at the PCC. Actually a comparative evaluation of the effectiveness of each of the control strategies was not carried out in the past, and it is a novelty brought by this chapter. Second, this chapter gives a rough overview of the different SAPF harmonics detection techniques that are available nowadays. Finally, this chapter describes common power circuit topologies and efficiency figures encountered on modern SAPFs.

- **Chapter 3** walks through a key technology that enables the ultra-low losses active damper solution. In particular, this chapter discusses the characteristics of SiC semiconductors and highlights their physical advantages against pure silicon devices. In addition, the benefits of high switching frequency operation and loss reduction at the converter system-level brought by SiC technology are also discussed in this chapter.

- **Chapter 4** presents the analysis of the power exchange between active damper and the distribution power system. In particular, this chapter discusses the harmonic active power absorption on the active damper and the mechanisms of harmonic power recovery. In other words, this chapter explains in a mathematical way how the transformation of the absorbed harmonic active power takes place within the active damper. In addition, as the harmonic recovery feature is enabled by an ultra-low losses VSAPF, this chapter also presents the design of an ultra-low losses VSAPF based on SiC semiconductors that allows the recovery of harmonic active power. The mathematical analysis made in this chapter is accompanied by simulation and experimental results.

- **Chapter 5** presents the power balance flow study of a power system that includes the ultra-low losses active damper. Specifically, the power balance flow is analyzed under non-sinusoidal conditions according to the Buchholz-Emmanuel power theory. Based on the definitions of this theory, the impacts of the passive and active dampers in the fundamental power demanded by the distribution power system are compared. This comparative evaluation found that the active damper with harmonic recovery function achieves a 1.4% reduction in the fundamental active power demanded from the utility compared with the passive damper. Additionally, two Figures-of-merit (FOM) to evaluate the capabilities of harmonic mitigation and power demand reduction of a particular power quality conditioner are proposed in this chapter.

- **Chapter 6** presents the comparative evaluation of four different power circuit topologies for the active damper all SiC based. In particular, this chapter compares three conventional topologies and one non-conventional topology in terms of power losses. The objective was to find out which topology exhibits the lowest losses. It is granted that the lower the power losses on the active damper, the higher will be

the amount of harmonic active power that can be recovered from the power grid. Arising out of the comparative evaluation in this chapter, it was found that the 3L-TNPC topology and the non-conventional asymmetrical (3L-ASYM) topology exhibit the lowest losses among all the topologies. In consequence, this chapter concludes that the 3L-TNPC and 3L-ASYM topologies are the most suitable ones to maximize the recovery of harmonic active power through an active damper. Furthermore, this chapter also illustrates the importance of computer-aided design of power electronics converters and converter optimization techniques to realize an ultra-low losses SAPF.

- **Chapter 7** pioneers the design of current controllers using the Ragazzini method. One of the conclusions reached during this research work was that the inner current control loop plays a significant role in the VSAPF´s stability. In other words, the current closed loop´s bandwidth determines very much the stability limit of the active damper. Therefore, and given that most current controllers are implemented nowadays in digital form, this chapter explores the direct discrete design of current controllers using the Ragazzini method. This chapter shows that the current controller's bandwidth can be increased three times using the Ragazzini method in comparison with conventional controller design techniques.

- **Chapter 8** presents the main conclusions of this dissertation and summaries the work carried out. Furthermore, this chapter presents some ideas for future research work.

## 1.9 LIST OF PUBLICATIONS

The research findings of this thesis have already been presented and published in different international scientific journals, conference proceedings, and technical workshops. The publications related to the topic of this thesis are as follows:

### 1.9.1 *Journal Articles*

[J1] R. Guzman Iturra and P. Thiemann, "Asymmetrical Three-Level Inverter SiC-Based Topology for High Performance Shunt Active Power Filter," Energies, vol. 13, no. 1, p. 141, Dec. 2019,
**DOI:10.3390/en13010141**

[J2] R. Guzman Iturra, M. Cruse, K. Figge, P. Thiemann and C. Dresel, "Ultra-Low Losses SiC-Based Active Damper for Industrial Power Systems: Mitigating Harmonic Distortion and Maximizing Harmonic Power Recovery," in IEEE Transactions on Energy Conversion, vol. 37, no. 4, pp. 2926-2940, Dec. 2022,
**DOI:10.1109/TEC.2022.3208772**

[J3] R. Guzman Iturra and P. Thiemann: "Discrete State-Space Current Control: Robust Tracking Control with Additional Dynamics ", Institute of Engineering and Technology (IET) Journal of Engineering (JoE), March 2023. Refereed from the IET Power Electronics Journal.
**DOI:Under Review**

### 1.9.2 *Conference Papers*

The following IEEE Conference articles were published in some of the most selective conferences for power electronics, all of them receiving at least 3 peer reviews:

[P1] R. Guzman Iturra and P. Thiemann, "Stability Analysis of Shunt Active Power Filter Based on Voltage Detection: A Delay Margin-Based Approach," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, Italy, 2018, pp. 1-8,
**DOI: 10.1109/COMPEL.2018.8459983**

[P2] R. G. Iturra, M. Cruse, K. Muetze, P. Thiemann and C. Dresel, "Shunt Active Power Filter for Harmonics Mitigation with Harmonic Energy Recycling Function," 2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC), Budapest, Hungary, 2018, pp. 938-945,
**DOI: 10.1109/EPEPEMC.2018.8521979**

[P3] R. G. Iturra, M. Cruse, K. Mütze, C. Dresel, I. Soleimani and P. Thiemann, "Model Predictive Control for Shunt Active Power Filter with Harmonic Power Recycling Capability," 2018 International Conference on Smart Energy Systems and Technologies (SEST), Seville, Spain, 2018, pp. 1-6,
**DOI: 10.1109/SEST.2018.8495890**

Outstanding presentation award received for paper **P4**:

[P4] R. Guzman Iturra, M. Cruse, K. Muetze, P. Thiemann and C. Dresel, "Power Balance of Shunt Active Power Filter based on Voltage Detection: a Harmonic Power Recycler Device," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 1835-1842,
**DOI: 10.1109/APEC.2019.8722037**

[P5] R. Guzman Iturra and P. Thiemann, "A Simple SiC MOSFETs Three Level Inverter Topology for High Performance Shunt Active Power Filter," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1-P.10
**DOI: 10.23919/EPE.2019.8914843**

[P6] R. Guzman Iturra and P. Thiemann, "Discrete Current Controller Design using Ragazzini Method for Active Damper," 2020 5th IEEE Workshop on the Electronic Grid (eGRID), Aachen, Germany, 2020, pp. 1-8,
**DOI: 10.1109/eGRID48559.2020.9330366**

[P7] Iturra R.G., Thiemann P. (2021) "Limits of Harmonic Power Recovery by Power Quality Conditioners in Three-Phase Three-Wire Systems Under Non-Sinusoidal Conditions". In: Afonso J.L., Monteiro V., Pinto J.G. (eds) Sustainable Energy for Smart Cities. SESC 2020. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol 375. Springer, Cham.
**DOI: 10.1007/978-3-030-73585-22**

[P8] Iturra R.G., Thiemann P. (2021) "Design of Current Controllers for Three Phase Voltage PWM Converters for Different Modulation Methods". In: Afonso J.L., Monteiro V., Pinto J.G. (eds) Sustainable Energy for Smart Cities. SESC 2020. Lecture Notes

of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol 375. Springer, Cham.
**DOI: 10.1007/978-3-030-73585-21**

[P9] R. Guzman Iturra and P. Thiemann, "Feed-forward Compensator Design with countermeasures against the non-realizable modulation delay inversion for Current Control of PWM converters," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Florence, Italy, 2021, pp. 1-8,
**DOI: 10.1109/CPE-POWERENG50821.2021.9501181**

[P10] R. Guzman Iturra and P. Thiemann, "Internal Model Control based Non-Interactive Feed-forward Compensator for Current Control of PWM Converters," 2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Florence, Italy, 2021, pp. 1-8,
**DOI: 10.1109/CPE-POWERENG50821.2021.9501221**

[P11] R. Guzman Iturra and P. Thiemann, "Comparative Evaluation of Control Strategies for Shunt Active Power Filters in Industrial Power Systems", Power and Energy Student Summit and Power Electronics Student Summit PESS & PELSS 2022, Kassel, Germany, November 2022,pp. 1-6.
**Print ISBN: 978-3-8007-6013-8**

### 1.9.3 *Technical Workshops*

Moreover, I have received the "Best Pitch Award" for outstanding presentation of Ph.D. topic in the technical workshop: "Mind the Wide-band Gap: Infineon Summer School 2021" organized by Infineon Technologies AG (Austria).

[W01] R. Guzman Iturra, ” Ultra-low losses SiC Shunt Active Power Filter based on Voltage Detection for Harmonics Energy Recovery in Industrial Power Systems”, Infineon Summer School 2021, August 2021, held Online.

### 1.9.4 *Further Scientific Contributions*

Some further scientific contributions not related with this Ph.D. thesis were also published in conference proceedings:

[P12] R. G. Iturra and P. Thiemann, "Sensorless Field Oriented Control of PMSM using Direct Flux Control with improved measurement sequence," 2021 XVIII International Scientific Technical Conference Alternating Current Electric Drives (ACED), Ekaterinburg, Russia, 2021, pp. 1-6,
**DOI: 10.1109/ACED50605.2021.9462276**

[P13] R. G. Iturra and P. Thiemann, "Sensorless Rotor Position detection of Synchronous Machine using Direct Flux Control – Comparative evaluation of rotor position estimation methods," 2021 XVIII International Scientific Technical Conference Alternating Current Electric Drives (ACED), Ekaterinburg, Russia, 2021, pp. 1-6,
**DOI: 10.1109/ACED50605.2021.9462301**

and as journal articles:

[J4] R. G. Iturra and P. Thiemann, "Sensorless Field Oriented Control of Synchronous Machines for Low and High Speeds with Space Vector Modulation-Based Direct Flux Control Measurement Sequence," Electronics, vol. 12, no. 6, p. 1382, Mar. 2023,
**DOI: 10.3390/electronics12061382**

# 2

# Shunt Active Power Filters: State-of-the-Art

Shunt active power filters (SAPFs) have been developed to combat the problems of harmonic voltage distortion caused by nonlinear loads in power systems. SAPFs are highly dynamic power quality conditioners formed by power semiconductors; and capacitors and inductors as passive energy storing elements. Indeed, SAPFs come in smaller sizes, are more flexible, and provide better harmonic filtering than shunt passive power filters [76]. Since their introduction by Gyugyi in 1976 [77], SAPF technology has improved tremendously due to the advent of modern semiconductor devices and digital control systems [30] [78]. On the one hand, the high computational power brought by modern digital processing units as Digital Signal Processors (DSP)s and Field-programmable Gate Arrays (FPGA)s is used within the SAPF's controller for the real-time calculation of the SAPF's compensating currents. As a result, these compensating currents can be adapted very quickly to changes in the harmonic currents drawn by nonlinear loads or to changing conditions in the power system. Above all, the ultimate goal of the compensating currents is to decrease the harmonic voltage distortion at the PCC [48]. On the other hand, modern semiconductor technology enables the construction of SAPF's power circuits that are fast enough to generate the compensating currents demanded by the SAPF's controller with a reasonable degree of accuracy [66]. At the same time, the rapid switching transitions of semiconductor devices and their outstanding static characteristics allow the realization of SAPF's power circuits with a low amount of power losses [17]. Finally, besides the mitigation of harmonic voltage distortion, SAPFs can also be utilized for reactive power compensation, voltage regulation, and load balancing [65][79].

Shunt active power filters can be conceived as controlled current sources that inject compensating currents $i_C$ to the power grid. As an illustration, Fig.2.1 shows a SAPF installed in an distribution power system and connected in parallel to the loads. Furthermore, the structure of such SAPF can be conceptually divided into two parts. The first part is the SAPF´s controller. The SAPF´s controller processes the harmonic voltages and currents, and based on those, it generates the references for the compensating currents $i^*_C$ [48]. The second part of the SAPF´s is formed by the power converter and its current controller. The latter two are in charge of the power processing or, differently said, they are in charge of the generation of the compensating currents as demanded by the SAPF´s controller. It follows that, in order to describe the current boundaries in SAPF technology, particularly the boundaries for VSAPFs, the state-of-the-art will be discussed in two parts. First, this chapter presents an overview of the state-of-art control strategies for SAPFs. Second, this chapter describes the most common power circuit topologies found in modern SAPFs. In fact, during the literature review carried out, a comparative analytical evaluation among the SAPF's control strategies was not found. On this basis, this chapter presents a profound mathematical analysis of the effectiveness of each of

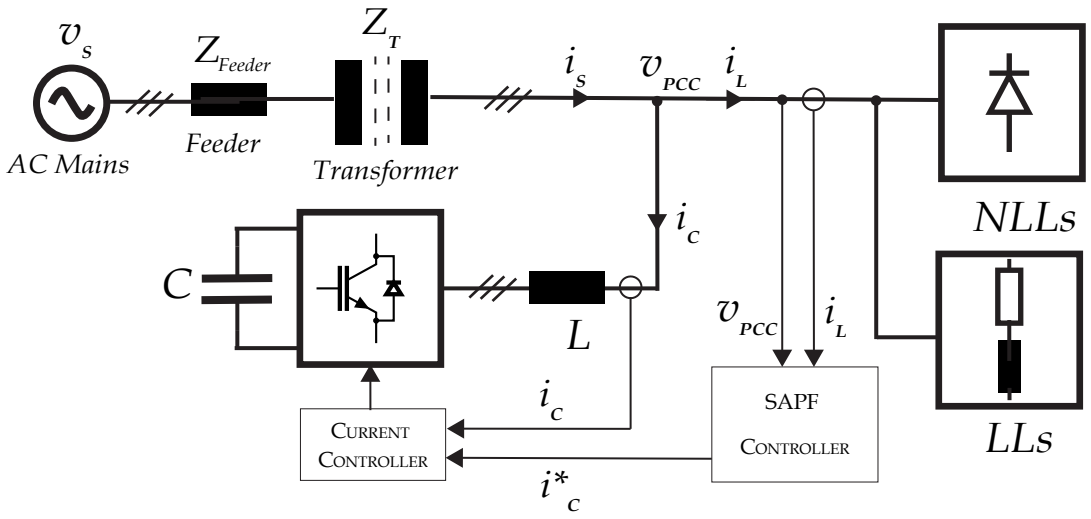


**Fig. 2.1:** Basic structure of a shunt active power filter connected to a distribution power system (e.g., industrial facility distribution system). The distribution power system consists of a distribution transformer, linear loads (LLs) and nonlinear loads (NLLs). Furthermore, the SAPF is formed by two main parts: the SAPF's controller that performs the reference generation and signals processing and a power processor formed by the power converter and current controller. The figure is based on [48].

the SAPF's control strategies to mitigate the voltage distortion at the PCC. Based on this mathematical analysis, this chapter critically compares the different SAPF's control strategies and highlights advantages and disadvantages of each of them. To the best of the author's knowledge, this mathematical analysis was not carried out in the past and thus represents another humble contribution to the body of knowledge. These findings were also published in:

- R. Guzman Iturra and P. Thiemann, "Comparative Evaluation of Control Strategies for Shunt Active Power Filters in Industrial Power Systems", Power and Energy Student Summit and Power Electronics Student Summit PESS & PELSS 2022, Kassel, Germany, November 2022,pp. 1-6.

## 2.1 SHUNT ACTIVE POWER FILTERS

### 2.1.1 *Distribution power system: Equivalent Circuit*

Before diving into the details of the state-of-the-art control strategies, it is necessary to define the nomenclature and conventions that will be used in the discussion. For this purpose, let us draw the per-phase equivalent circuit of Fig.2.1 as in Fig.2.2. Indeed, in the equivalent circuit, the NLL is modeled as a current source $i_{NL}$. The current source $i_{NL}$ draws currents at the fundamental frequency and harmonic frequencies, ($i_{NL1}$) and ($i_{NLh}$) respectively, from the grid. Although the representation of the nonlinear load as a pure current source is the simplest model possible as it is very commonly used, a more precise model of the nonlinear load is obtained using a Norton equivalent model [66]. The Norton equivalent model includes, in parallel to the harmonic current source, an impedance that depends on the parameters of the nonlinear load for a specific operating point. For the incoming discussion, the impedance $Z_L$ will include the equivalent parallel impedance of the linear loads and the parallel impedance of the Norton model without loss of generality.

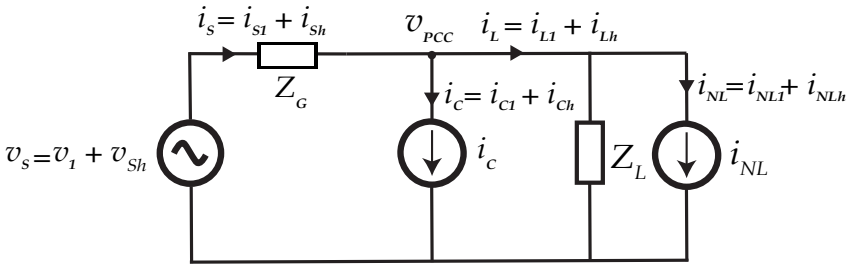


**Fig. 2.2:** Equivalent circuit of simplified distribution power system with SAPF connected. The figure is based on [48].

All in all, the current draw by linear and nonlinear loads is $i_L = i_{\mathrm{L1}} + i_{\mathrm{Lh}}$. Furthermore, the SAPF is considered in the equivalent circuit as a controlled current source that injects compensating currents $i_C$ into the PCC. In reality, the SAPF is subject to time delays in the control system and power circuit. Thus, the compensating currents generated by the SAPF's power circuit exhibit some phase lag with respect to their references [80]. The mentioned phase lags are taken into account in the mathematical modelling through the SAPF´s transfer function $G(s)$, similar to the approach taken by Peng in [81]. It is important to highlight that the transfer function $G(s) = \frac{I_C(s)}{I^*_C(s)}$ has units $A/A$ which lead to the conclusion that $G(s)$ is dimensionless. Moreover, for some frequencies where the harmonic compensation takes place, $G(s)$ can be considered as unity with a negligible phase lag. The latter is especially true for those harmonic frequencies that lie one decade below the bandwidth of the current controller [30]. Furthermore, the voltages provided by the utility can also contain a certain amount of harmonic background distortion or voltage distortion $v_{Sh}$. The background voltage distortion on the supply is produced by harmonic currents generated outside of the user's facility. Harmonic currents causing the background voltage distortion might be generated by nonlinear loads connected to the feeder's vicinity or by resonance conditions that involve the supply's feeder. The background voltage distortion $v_{Sh}$ causes the flow of supply harmonic currents $i_{Sh}$ over the grid impedance $\underline{Z_G} = R_G + j \cdot L_G \cdot \omega_{\mathrm{h}}$, specially when this impedance is low. Notice that the term $\omega_{\mathrm{h}}$ is defined as $\omega_{\mathrm{h}} = 2 \cdot \pi \cdot f_{\mathrm{h}}$ where $f_{\mathrm{h}}$ stands for any harmonic frequency $h$. From the loads perspective, the power grid impedance $Z_G$ is formed by the impedance of the feeder $Z_{Feeder}$ that connects the industrial facility with the mains, and the impedance of the transformer $Z_T$ (see Fig.1.8 **b)**). In particular, the impedance of the feeder $Z_{\mathrm{Feeder}}$ consist of two elements $R_{\mathrm{SS}}$ and $X_{\mathrm{SS}}$. The former two can be calculated based on the short-circuit capacity of the feeder ($MVA_{Sc}$) in MVA , the feeder X/R ratio ($\frac{X_{\mathrm{SS}}}{R_{\mathrm{SS}}}$) and the nominal feeder voltage $kV_{LL}$ in kV as follows [17][82]:

$$R_{\mathrm{SS}} = \frac{kV^2{}_{\mathrm{LL}}}{MVA_{\mathrm{SC}}} cos\left(tan^{-1}(\frac{X_{\mathrm{SS}}}{R_{\mathrm{SS}}})\right) \tag{2.1}$$

$$X_{\mathrm{SS}} = \frac{kV^2{}_{\mathrm{LL}}}{MVA_{\mathrm{SC}}} sin\left(tan^{-1}(\frac{X_{\mathrm{SS}}}{R_{\mathrm{SS}}})\right) \tag{2.2}$$

Furthermore, $R_{\mathrm{SS}}$ and $X_{\mathrm{SS}}$ can be referred to the secondary of the transformer dividing the results of (2.1) and (2.2) by the factor $(\frac{n_1}{n_2})^2$, where $n_1$ stands for the number of turns in the primary of the transformer and $n_2$ stands for the number of turns in the secondary of the transformer. Also [17]:

$$R_{\mathrm{Feeder}} = \frac{R_{\mathrm{ss}}}{(\frac{n_1}{n_2})^2} \tag{2.3}$$

$$X_{\text{Feeder}} = \frac{X_{\text{ss}}}{(\frac{n_1}{n_2})^2} \tag{2.4}$$

Similarly, the elements of the equivalent impedance of the transformer can be calculated based on its power rating ($kVA_{Tr}$) in kVA, its short circuit impedance ($R_{Trpu}$ and $X_{Trpu}$) in percent, and its voltage rating ($kV_{Tr}$) in kV. Thus, the following equations apply:

$$R_T = R_{\text{Trpu}} \frac{kV^2{}_{\text{Tr}}}{kVA_{\text{Tr}}} \tag{2.5}$$

$$X_T = X_{\text{Trpu}} \frac{kV^2{}_{\text{Tr}}}{kVA_{\text{Tr}}} \tag{2.6}$$

Altogether the power grid impedance, as seen by the loads, it is found as the series combination of the feeder impedance referred to the secondary of the transformer and transformer impedance:

$$R_G = R_{\text{Feeder}} + R_T \tag{2.7}$$

$$X_G = X_{\text{Feeder}} + X_T \tag{2.8}$$

It follows that the inductive part of the power grid is defined by:

$$L_G = \frac{X_{\text{G}}}{2\pi f_1} \tag{2.9}$$

Industrial grids normally lie on the deepest part of the distribution level. Thus the impedance of the service or user's transformer dominates over the impedance of the feeder [1]. This is because all the parameters of the power system and feeder are referred to the secondary side of the transformer, and thus the factor $(\frac{n_1}{n_2})^2$ drastically diminishes the feeder impedance's influence over the total impedance seen by the loads. Moreover, for transformers with power ratings between 1 MVA up to tens of MVAs, typical values for the short circuit impedance are $R_{Trpu}$=1% and $X_{Trpu}$=5% [17]. Because of this difference of a factor of 5 between $R_{Trpu}$ and $X_{Trpu}$, in general, the impedance of service transformers is considered mainly inductive.

## 2.2 SAPF CONTROL STRATEGIES

There are three control strategies to generate the references for the SAPF´s compensating currents. In particular, the control strategies are known as load current detection, supply current detection, and voltage detection [49]. The following subsections will discuss each control strategy in detail. Truly, the derivations that follow are based on the work presented by Peng in [81]. However, the circuital analysis carried out in the original Peng's work was focused only on the supply currents and was made only for the load current detection method. Thus, the following subsections expand the circuital analysis carried out by Peng to the harmonic voltages at the PCC and are performed for the three SAPF's control strategies.

### 2.2.1 *Load Current Detection Strategy*

The load current detection strategy is also known in technical literature as as open loop control strategy [83]. Also, on the load current detection strategy, the SAPF's controller measures the voltage $v_{PCC}$ and the load current $i_L$. Afterwards, the harmonic components $i_{Lh}$ are extracted from $i_L$ using time-domain or frequency-domain techniques. Those techniques are going to be briefly summarized in the next section. Based on the obtained currents $i_{Lh}$ and taking into account the equivalent circuit presented in Fig.2.2, the load current detection strategy defines the following control law for the compensating currents at harmonic frequencies:

$$i^*_{\mathrm{Ch}} = -i_{\mathrm{Lh}} \tag{2.10}$$

In simple terms, the load current detection strategy dictates that the compensating currents must be equal in amplitude to the load harmonic currents $i_{Lh}$ but with a phase shift of 180° with respect to the them [84]. Therefore, in the ideal case, the SAPF cancels out completely the harmonic currents generated by the nonlinear load. Furthermore, in order to analyze this control strategy in detail, let us apply the Kirchhoff's current law (for harmonic frequencies) on the circuit presented in Fig. 2.2 at the node PCC. We obtain that:

$$i_{\mathrm{Sh}}(s) - i_{\mathrm{Ch}}(s) - i_{\mathrm{Lh}}(s) = 0 \tag{2.11}$$

By definition:

$$i_{\mathrm{Sh}}(s) = \frac{v_{\mathrm{Sh}}(s) - v_{\mathrm{PCCh}}(s)}{Z_{\mathrm{G}}(s)} \tag{2.12}$$

$$i_{\mathrm{Lh}}(s) = \left( \frac{v_{\mathrm{PCCh}}(s)}{Z_{\mathrm{L}}(s)} + i_{\mathrm{NLh}}(s) \right) \tag{2.13}$$

thus replacing (2.12) and (2.13) in (2.11) leads to:

$$\frac{v_{\mathrm{Sh}}(s) - v_{\mathrm{PCCh}}(s)}{Z_{\mathrm{G}}(s)} - i_{\mathrm{Ch}}(s) - \left( \frac{v_{\mathrm{PCCh}}(s)}{Z_{\mathrm{L}}(s)} + i_{\mathrm{NLh}}(s) \right) = 0 \tag{2.14}$$

considering that in reality:

$$i_{\mathrm{Ch}}(s) = G(s) i^*_{\mathrm{Ch}}(s) = -G(s) i_{\mathrm{Lh}}(s) \tag{2.15}$$

replacing (2.15) in (2.14) and solving for the PCC voltage $v_{PCCh}$ in function of the background harmonic distortion $v_{Sh}$ and the nonlinear load harmonic currents $i_{NLh}$ yields to:

$$v_{\mathrm{PCCh}}(s) = \frac{\frac{Z_{\mathrm{L}}(s)}{1-G(s)} v_{\mathrm{Sh}}(s)}{Z_{\mathrm{G}}(s) + \frac{Z_{\mathrm{L}}(s)}{1-G(s)}} - \frac{Z_{\mathrm{L}}(s) Z_{\mathrm{G}}(s) i_{\mathrm{NLh}}(s)}{Z_{\mathrm{G}}(s) + \frac{Z_{\mathrm{L}}(s)}{1-G(s)}} \tag{2.16}$$

If for a particular set of harmonic frequencies $h$ the magnitude of the SAPF's transfer function approximates one or if the impedance of the load $|Z_L|$ is much larger than the impedance of the source $|Z_G|$, in other words if the following inequality holds:

$$\left| \frac{Z_{\mathrm{L}}(s)}{1 - G(s)} \right| >> |Z_{\mathrm{G}}(s)| \tag{2.17}$$

the expression (2.16) can be simplified as follows:

$$v_{\mathrm{PCCh}}(s) = v_{\mathrm{Sh}}(s) - Z_{\mathrm{G}}(s)[1 - G(s)] i_{\mathrm{NLh}}(s) \tag{2.18}$$

From this result, it can be concluded that if the SAPF's transfer function $G(s)$ equals one, the harmonic currents generated by the nonlinear load ($i_{NLh}$) do not flow over the grid impedance. Therefore, harmonic voltage distortion at the PCC due to the currents generated by the nonlinear load is avoided. It turns out, that the load current detection strategy is very effective for the compensation of harmonic currents generated at the load side. In addition, as this strategy is an open loop control scheme, the power system could not turn unstable due to the operation of the SAPF. Therefore, in this control strategy, delays in the control system or SAPF´s power circuit can not cause instabilities. However, the load current detection strategy does not diminish the impact of the background voltage distortion $v_{Sh}$ over $v_{PCCh}$ as is demonstrated by (2.18). In fact, if the background voltage is considerable, this voltage distortion will be immediately translated to the PCC despite the SAPF's operation. Moreover, if the conditions stated by (2.17) do not hold, the harmonics compensation performance of the SAPF deteriorates. For instance, if the load impedance is comparable to or even smaller than the grid impedance, the inequality stated by (2.17) is no longer valid. Indeed, the former is the case when capacitors are connected on the load side or when the parallel impedance of the Norton equivalent of the nonlinear load is small in magnitude. Similarly, if the SAPF's gain differs from unity at frequencies of interest, the inequality (2.17) is also affected. Consequently, the filtering performance of the SAPF under the load detection strategy depends heavily on the transfer function $G(s)$. One last disadvantage is that a load current driven SAPF could also excite resonances produced by the grid and load impedances interaction in the power system [85]. On the whole, it can be concluded that the load detection control strategy is the most effective when the SAPF's is installed immediately next to the nonlinear load that is generating the harmonic currents [86][87]. Otherwise, its filtering performance is heavily influenced by the ratio between the load and grid impedances [30][81].

### 2.2.2 *Supply Current Detection Strategy*

The supply current detection strategy uses the voltages at the PCC and the supply currents $i_S$ to generate the references for the compensating currents. Once again, the harmonic components $i_{Sh}$ are extracted from the signal $i_S$ through signal-processing techniques, either in the time domain or in the frequency domain. Further, taking into consideration the circuit presented in Fig.2.2, the supply current detection strategy dictates that the compensating current are proportional to the supply harmonic currents as follows:

$$i^*_{\mathrm{Ch}} = k_{\mathrm{C}} \cdot i_{\mathrm{Sh}} \tag{2.19}$$

where the factor $k_{\mathrm{C}}$ is dimensionless and chosen by the SAPF's designer [87][88]. The supply current detection strategy implies a closed loop between compensating currents and supply currents. This is the reason why this control strategy is also known as closed loop control strategy in technical literature [83]. As in practice the compensating currents lag their references in dependency of the SAPF's transfer function, the following holds:

$$i_{\mathrm{Ch}}(s) = G(s) i^*_{\mathrm{Ch}}(s) = k_{\mathrm{C}} G(s) i_{\mathrm{Sh}}(s) \tag{2.20}$$

Certainly, the working principle of the supply current detection strategy can be understood replacing (2.20) in (2.14) which yields:

$$v_{\mathrm{PCCh}}(s) = \frac{Z_{\mathrm{L}}(s) v_{\mathrm{Sh}}(s)}{Z_{\mathrm{L}}(s) + \frac{Z_{\mathrm{G}}(s)}{1+k_{\mathrm{C}}G(s)}} - \frac{\frac{Z_{\mathrm{G}}(s)Z_{\mathrm{L}}(s)}{1+k_{\mathrm{C}}G(s)} i_{\mathrm{NLh}}(s)}{Z_{\mathrm{L}}(s) + \frac{Z_{\mathrm{G}}(s)}{1+k_{\mathrm{C}}G(s)}} \tag{2.21}$$

$$v_{\mathrm{PCCh}}(s) = \frac{Z_{\mathrm{L}}(s)[1 + k_{\mathrm{C}}G(s)]v_{\mathrm{Sh}}(s)}{Z_{\mathrm{L}}(s)[1 + k_{\mathrm{C}}G(s)] + Z_{\mathrm{G}}} - \frac{Z_{\mathrm{L}}(s)Z_{\mathrm{G}}(s)i_{\mathrm{NLh}}(s)}{Z_{\mathrm{L}}(s)[1 + k_{\mathrm{C}}G(s)] + Z_{\mathrm{G}}} \tag{2.22}$$

if $k_{\mathrm{C}}$ is selected sufficiently large, we obtain the following relationship between the magnitudes in the denominators:

$$\left| Z_{\mathrm{L}}(s)[1 + k_{\mathrm{C}}G(s)] \right| >> |Z_{\mathrm{G}}(s)| \tag{2.23}$$

and (2.22) can be simplified as follows:

$$v_{\mathrm{PCCh}}(s) = v_{\mathrm{Sh}}(s) + \frac{Z_{\mathrm{G}}(s)i_{\mathrm{NLh}}(s)}{[1 + k_{\mathrm{C}}G(s)]} \tag{2.24}$$

If the factor $k_{\mathrm{C}}$ is sufficiently large and $G(s)$ is close to the unity, the supply current detection strategy will avoid the flow of the harmonic load currents upstream of the PCC. More importantly, the voltage drop provoked by $i_{NLh}$ over the grid impedance can be decreased by choosing the appropriate factor $k_{\mathrm{C}}$ independent of the ratio between the grid and load impedances. The supply current detection method is recommended when the SAPF should compensate for an entire cluster of linear and nonlinear loads [86][87]. For example, when the SAPF is intended to compensate for several linear and nonlinear loads, all connected in parallel, the supply detection method will produce better results than the load current detection strategy [83]. Nevertheless, similar to the load current detection strategy, the supply current detection strategy does not mitigate for the background harmonic voltage $v_{Sh}$ impact over $v_{PCCh}$ and does not eliminate resonances. Furthermore, as the supply current detection method implies a feedback loop between supply and compensating currents, instabilities in the overall closed loop could arise. In fact, phase lags and time delays within the SAPF and a large $k_{\mathrm{C}}$ factor can lead to an unstable operation of the SAPF [80]. A SAPF's unstable operation could produce harmonic voltage distortion at the PCC even larger than the original harmonic voltage distortion that existed prior to the operation of the SAPF.

### 2.2.3 *Voltage Detection Strategy*

A SAPF driven by the voltage detection strategy (VSAPF) measures only the voltages at the PCC. On this basis, the VSAPF injects harmonic compensating currents $i_{Ch}$ that are proportional to the harmonic voltages $v_{PCCh}$ present at PCC. In short, a VSAPF follows the control law $i^{*}_{\mathrm{Ch}} = \frac{v_{\mathrm{PCCh}}}{k_{\mathrm{V}}}$, where $1/k_V$ is the proportionality factor. Under these circumstances the VSAPF behaves or emulates a virtual harmonic resistor of $k_V$ ($\Omega$). Considering that in reality the compensating currents produced by the VSAPF depend on the transfer function $G(s)$, it follows that:

$$i_{\mathrm{Ch}}(s) = G(s)i^{*}_{\mathrm{Ch}}(s) = G(s)\frac{v_{\mathrm{PCCh}}}{k_{\mathrm{V}}} \tag{2.25}$$

Let us analyze the voltage detection strategy resorting once again to the circuit depicted in Fig.2.2 and equation (2.14). Thus, replacing (2.25) in (2.14) leads to:

$$v_{\mathrm{PCCh}}(s) = \frac{\frac{v_{\mathrm{Sh}}(s)}{Z_{\mathrm{G}}(s)}}{\frac{Z_{\mathrm{G}}(s)+Z_{\mathrm{L}}(s)}{Z_{\mathrm{L}}(s)Z_{\mathrm{G}}(s)} + \frac{1}{k_{\mathrm{V}}G(s)}} + \frac{i_{\mathrm{NLh}}(s)}{\frac{Z_{\mathrm{G}}(s)+Z_{\mathrm{L}}(s)}{Z_{\mathrm{L}}(s)Z_{\mathrm{G}}(s)} + \frac{1}{k_{\mathrm{V}}G(s)}} \tag{2.26}$$

$$v_{\mathrm{PCCh}}(s) = \frac{Z_{\mathrm{G}}(s)v_{\mathrm{Sh}}(s)}{\frac{1}{Z_{\mathrm{G}}} + \frac{1}{Z_{\mathrm{L}}} + \frac{1}{k_{\mathrm{V}}G(s)}} + \frac{i_{\mathrm{NLh}}(s)}{\frac{1}{Z_{\mathrm{G}}} + \frac{1}{Z_{\mathrm{L}}} + \frac{1}{k_{\mathrm{V}}G(s)}} \tag{2.27}$$

if $k_{\mathrm{V}}$ is chosen sufficiently small such that the admittance $\frac{1}{k_{\mathrm{V}}G(s)}$ is larger than the admittances $\frac{1}{Z_{\mathrm{L}}(s)}$ and $\frac{1}{Z_{\mathrm{G}}(s)}$, namely:

$$\left|\frac{1}{k_{\mathrm{V}}G(s)}\right| >> \left|\frac{1}{Z_{\mathrm{L}}(s)} + \frac{1}{Z_{\mathrm{G}}(s)}\right| \tag{2.28}$$

then (2.27) can be simplified as:

$$v_{\mathrm{PCCh}}(s) = \frac{k_{\mathrm{V}}G(s)}{Z_{\mathrm{G}}(s)}v_{\mathrm{Sh}}(s) + k_{\mathrm{V}}G(s)i_{\mathrm{NLh}}(s) \tag{2.29}$$

On the whole, if the factor $k_{\mathrm{V}}$ is made sufficiently small and $G(s)$ is close to the unity, the virtual resistor emulated by the VSAPF offers a path of lower impedance in relation to the equivalent impedance of the grid and the linear load. Consequently, the harmonic currents generated by the nonlinear load flow into the grid impedance to a lesser extent, the harmonic voltage drop over the grid impedance is reduced, and thus the voltage distortion at the PCC is decreased. Besides, the VSAPF will damp any resonance that could arise by the interaction of inductive impedances in the grid (e.g. transformers, transmission lines) and capacitors (e.g. capacitor banks, converters' output filters ) that could be connected in the load side. Therefore, the VSAPF drastically reduces any possibility of harmonic amplification in the system. A substantial difference with the SAPFs based on current detection is that this control strategy decreases the impact of the background voltage distortion over the PCC. In short, the influence of background distortion over the $v_{PCCh}$ can be tempered by the proper choice of $k_{\mathrm{V}}$.

Altogether, the harmonic voltage distortion at the PCC cannot be entirely eliminated by the VSAPF. The latter will signify a factor $k_{\mathrm{V}}$ infinitesimal small and therefore a compensating current infinitely large, which is not possible in practice. Nonetheless, VSAPFs can be used to maintain the harmonic voltage distortion below the limits permitted in distribution power systems, given for example, by the standard EN61000-2-4, if $k_{\mathrm{V}}$ is selected appropriately. But, of course, there are limits about how small $k_{\mathrm{V}}$ can be selected. As a VSAPF implies a closed feedback loop between measured harmonic voltages and compensating currents, time and phase delays contribute to the degradation of the filter performance and can lead ultimately to its instability, specially if $k_{\mathrm{V}}$ is chosen to small. A more detailed analysis of the stability of the VSAPF was carried out and can be found in Appendix A.

### 2.2.4 *SAPF Control Strategies - Comparative Evaluation*

In order to compare the control strategies discussed in the previous subsections, Table 2.1 summarizes the main features of each control strategy. First, Table 2.1 shows the type of control loop formed between the SAPF and the distribution power system for each compensation method. Among the three control strategies, the load current detection is the only open loop control strategy. It, therefore, is not subject to stability problems due to delays within the SAPF's control system and power circuit. Moreover, the supply current detection strategy and the voltage detection strategy are closed loop control strategies with loop gains $k_{\mathrm{C}}$ and $\frac{1}{k_{\mathrm{V}}}$ respectively. It is granted that if these gains become too large, stability problems will arise due to the phase lags or delays introduced by

**Table 2.1:** SAPF Control Strategies - Comparative Evaluation

| Feature | Load Current Detection | Supply Current Detection | Voltage Detection |
|---|---|---|---|
| Control type | Open Loop | Closed Loop | Closed Loop |
| Nr. Current Sensors | 6 | 6 | 3 |
| Nr. Voltage Sensors | | 3 | |
| Direct $THD_V$ Control | | Yes | |
| Direct $THD_I$ Control | Yes | Yes | No |
| Harmonic Currents Isolation | Yes | No | No |
| Resonance Damping | No | No | Yes |
| Background Distortion Mitigation | No | No | Yes |
| Recommended place of installation | Close proximity to polluting NLL | Central installation at PCC | Central installation at PCC |
| Filter Gain | - | $k_C$ | $\frac{1}{k_V}$ |
| Prone to instability (due to large gains or delays) | No | Yes | Yes |

$G(s)$. Second, Table 2.1 shows that the current based control strategies (load and supply current detection) require six current sensors in contrast to the three current sensors required by the voltage detection method. Obviously, three current sensors are needed for the internal current control of the compensating currents in all the control strategies. In this regard, closed-loop Hall effect current sensors are commonly used for the SAPF´s inner current control. Those exhibit an accuracy in the order 1% to 5% up to the 200 kHz range that suffices for current closed loop regulation [89]. Moreover, the current based detection strategies require in addition three external current sensors placed on the grid, either on the load or on the supply side. These external current sensors are installed outside of the SAPF and are normally conventional current transformers. Those exhibit an accuracy between 0.1% to 5% for currents up to 2 kHz at a relative low cost [65][89]. Of course, the placement of these external current sensors makes the installation of current based SAPFs more complex and more expensive. However, the external current sensors enable the possibility to add extra functionalities to the SAPF besides harmonic compensation [83]. For instance, Table 2.2 shows some additional functionalities that can be added to each SAPF's control strategy. Indeed, the voltage detection strategy is the less suitable for incorporating extra functionalities. Third, Table 2.1 shows that all the control methods directly influence the harmonic voltage distortion at the PCC. The harmonic distortion in voltage and current are typically measured in terms of the Total Harmonic Distortion (THD) index. Thus, the $THD_V$ can be reduced using all the three control strategies. However, the voltage detection strategy can only indirectly reduce the current distortion of the supply current measured by the $THD_I$. Clearly, the effectiveness of a VSAPF to decrease the $THD_I$ on the supply currents depends very much on the impedances of the grid and the load. In contrast, the current based SAPFs directly control the harmonic currents that flow upstream of the PCC. Thus, if for example, the industrial facility needs to comply with the IEEE Standard 519-2014 that imposes limits on both the

**Table 2.2:** SAPF Control Strategies - Additional functionalities

| Feature | Load Current Detection | Supply Current Detection | Voltage Detection |
|---|---|---|---|
| PCC Voltage Regulation | | Yes | |
| Power Factor Correction/ Reactive power compensation | Yes | Yes | No |
| Flicker Compensation | Yes | Yes | No |
| Load Balancing | Yes | Yes | No |

$THD_V$ and $THD_I$, the requirements will be easier to fulfill by applying current based SAPFs than VSAPFs. Finally, Table 2.1 shows that the strengths of the VSAPF are its unique abilities to suppress resonances and to mitigate the influence of the background voltage on the PCC.

It is granted that it is possible to combine two control strategies within the SAPF´s control system. Although to the best of the author's knowledge such combinations of control strategies have not been seen in industrial applications yet, academic publications have already addressed this topic. For example, Wang et. al in [90] have discussed the combination of the load and supply current detection methods. Furthermore, Chen et al. in [91] and [92] and Liu et al. in [59] have studied the combination of load current detection strategy in conjunction with the voltage detection strategy in what they name compound control strategy. The latter of course exhibits the advantages of the load current and voltage detection methods at the same time. In particular, the latter combination will bring several advantages and almost no drawbacks to practical applications. As Matthes explains in [85], in case a resonance is detected when the SAPF is driven by the load detection strategy, the SAPF simple stops to inject harmonic compensating currents in a narrow range in the vicinity where the harmonic resonance was detected. The latter diminishes the effectiveness of the active power filter if it uses the load detection strategy. But, if the compound control strategy is applied, the voltage detection strategy could be applied to the harmonic frequency range where the resonance was detected. Thus resonances will be suppressed, and the rest of the harmonic currents will be blocked by the SAPF. All the harmonic currents outside of the resonance range will be contained within the nonlinear load terminals by the compensating currents injected according to the load current detection strategy. The only possible drawback of the compound strategy is that instabilities in the power system could arise if the voltage detection gain $\frac{1}{k_V}$ is chosen too large.

## 2.3 HARMONICS EXTRACTION METHODS

The last section discussed the three control strategies that are available to generate the SAPF´s reference currents. One key and common aspect among the three control strategies is that separation of the fundamental component from the harmonic components needs to be carried out. The mentioned separation is performed over the load or supply currents for the current based control strategies or over the PCC voltage for the voltage detection strategy. In fact, different methods on the time or frequency domain are available to separate the fundamental component from the harmonic components. Certainly, it is beyond the scope this dissertation to describe every single one of the methods available and compare them. However, at least a summary of the available methods is given.

Indeed, Fig. 2.3 presents an overview of most relevant harmonic extraction techniques that exist in scientific literature. Actually, Asiminoaei et al. in [93] walked through some of the time and frequency domain methods and compared them. Actually, the comparison was carried out in terms of the processing power required, transient response time, and a steady state accuracy. They have concluded that the Harmonic DQ frame theory and the PQ theory techniques are the most advantageous in terms transient response time, steady state accuracy, and robustness against unbalanced voltages and currents. Moreover, in [93], Harmonic DQ frame theory is recommended to perform selective harmonic compensation whereas PQ theory is the recommended technique to compensate harmonics in a wide frequency range. Finally, a more exhaustive discussion about harmonics separation or extraction techniques for SAPFs can be found in [94] and [95].

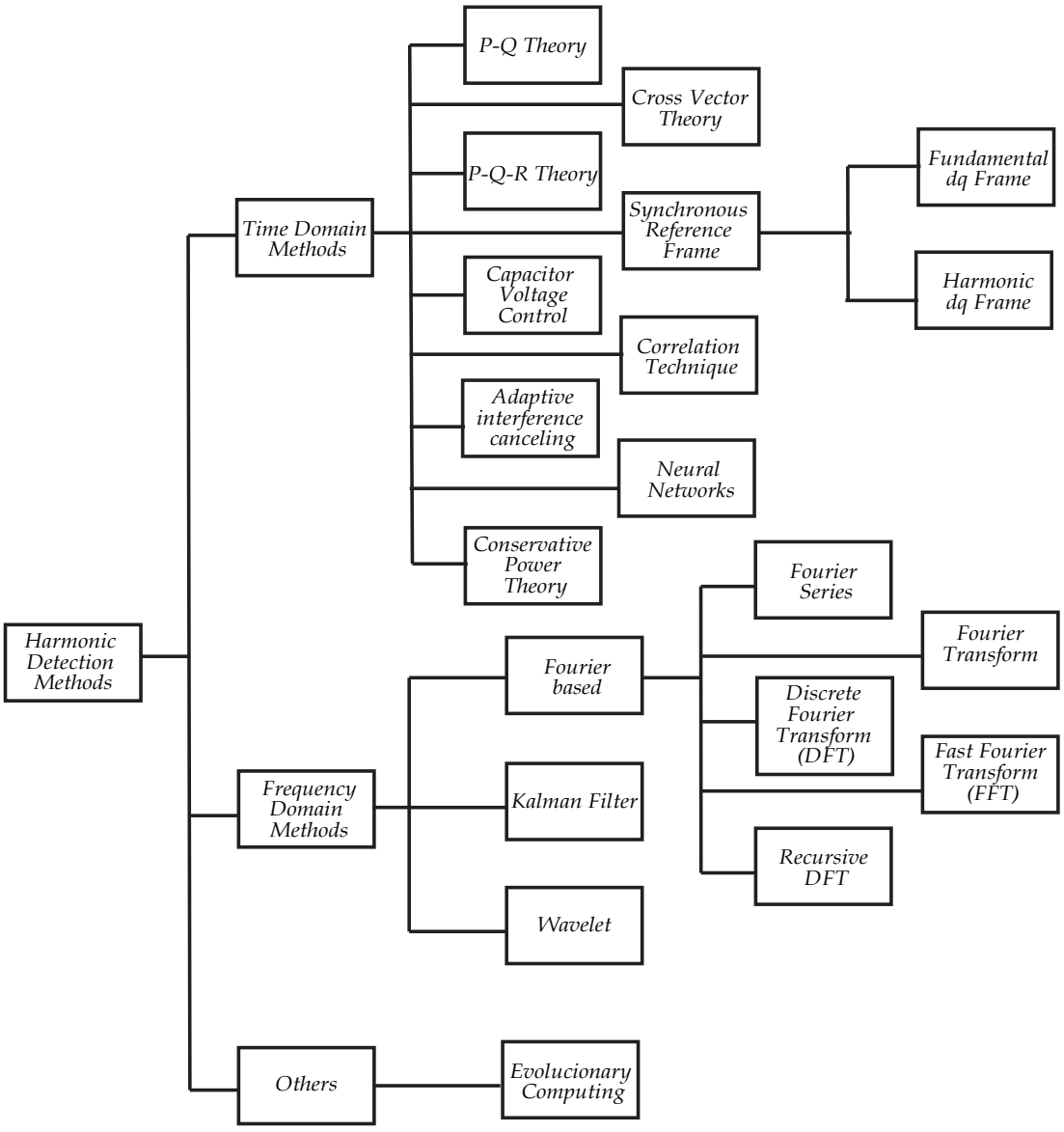


**Fig. 2.3:** Harmonic Detection Strategies - Overview. Based on [30],[93][94]

## 2.4 POWER CIRCUITS FOR SHUNT ACTIVE POWER FILTERS

SAPFs are in essence controllable current sources and their realization can be achieved using two types of power circuits, either VSC or Current Source Converter (CSC) [48]. Both types of power circuits are illustrated by Fig.2.4 and Fig.2.5 respectively. In fact, Monteiro et al. in [96] compared the harmonic filtering performance of both topologies and concluded that their performances were very similar. Thus, other factors need to be considered for the selection of one of these two topologies. On the hand, the VSC topology has a capacitor as energy storage on its DC side and uses bidirectional current and unidirectional blocking voltage switches. On the other hand, the CSC topology has an inductor as energy storage on its DC side and uses unidirectional current and bidirectional blocking voltage switches [30]. Indeed, the advantages of the CSC topology are its ruggedness, simple open loop current control, and lower power losses than the VSC topology below the nominal operating point [97]. Still, the CSC topology's drawbacks are the bulky DC inductor [97] and the need for an additional clamping circuit to protect the switches against overvoltages [98]. Above all, the most notorious disadvantage of the CSC is that it needs unidirectional current and bidirectional blocking voltage switches (e.g. reverse blocking IGBTs) which are not widely available in the market [99]. On the other hand, the VSC topology exhibits lower power losses than the CSC topology at the nominal operating point and comes as well in smaller sizes [48]. The difference lies in the DC side of both topologies. Truly, the energy density in capacitors is factor 1000 times larger than the energy density in inductors for voltage ratings up to 1000 V [100]. Therefore, a power converter based on the VSC topology comes in smaller size and volume than a power converter based on the CSC topology. More importantly, VSCs can be built with power MOSFETs or with IGBTs with antiparallel diodes, which are widely available in the market. By their very nature, the mentioned devices exhibit the bidirectional current

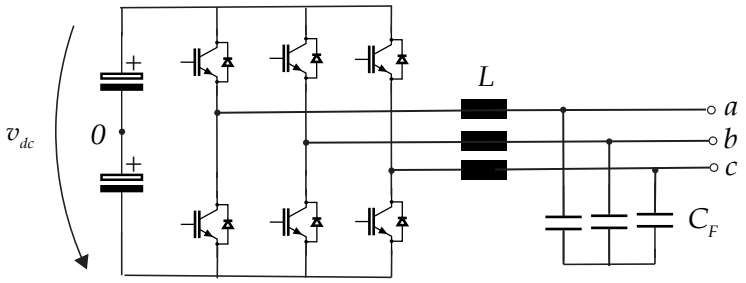


**Fig. 2.4:** Two-level voltage source converter (2L-VSC) with LC output filter. VSC built with silicon IGBTs and silicon diodes Based on [96]

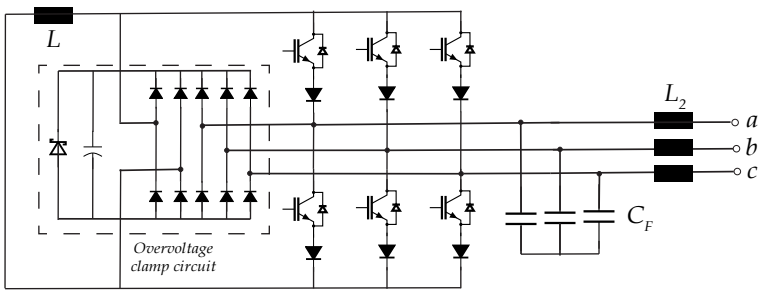


**Fig. 2.5:** Current Source Converter (CSC) power circuit. Based on [98]

and unidirectional blocking voltage capabilities required by a VSC [101]. This has been the main reason why SAPFs are predominantly based on voltage source converters up to now [17, 48, 99].

### 2.4.1 *Voltage Source Converter based SAPFs: State-of-the-art*

In distribution power systems, where the AC voltage levels typically lie below 690 V, two structures of VSC for SAPFs are commonly found. The simplest structure is the two-level voltage source converter (2L-VSC) built with silicon IGBTs and silicon diodes (see Fig. 2.4). As the SAPF needs to inject harmonic currents into the grid, the voltage at the DC side of the VSC should be higher than the voltage on the grid side for a good current controllability. In fact, a factor of two times the AC peak voltage is recommended for the DC-Bus voltage [17]. With this in mind, if a two-level based SAPF is going to be connected to a 400 V distribution power system, it should operate with a DC-Bus voltage of at least 700 V. It follows that the power switches used to construct the 2L-VSC power circuit should be rated at 700 V plus some margin to sustain overvoltages due to the *di/dt* over the stray inductance of the DC-Bus [99]. For this reason, IGBT power switches with a blocking voltage of 1200 V are typically used in 2L-VSC based SAPF that are going to be connected to 400 V power grids. On the same note, if a 2L-VSC based SAPF is going to be connected to a 690 V distribution power system, the SAPF's DC-Bus voltage should be selected as 1200 V, and the IGBT power switches must be selected with a blocking voltage of 1700 V. Indeed, several studies [102][103] have shown that the three-level voltage source converter structure (3L-VSC) exhibits many advantages over the 2L-VSC structure for low-voltage utility applications. Such advantages are lower power losses, higher compactness, and better EMI behavior [99][104]. In consequence, nowadays, the design of state-of-the-art SAPF is made using the three-level neutral point clamped (3L-NPC) topology [79]. Fig. 2.6 shows the power circuit of a 3L-NPC power converter entirely based on silicon semiconductors as an illustration. In terms of AC filters, the state-of-the-art SAPFs use LCL filters as output filters. Indeed, LCL filters are preferred to LC filters because they provide a better attenuation of the current ripple and diminish the possibility of introducing resonances to the power system [105][106].

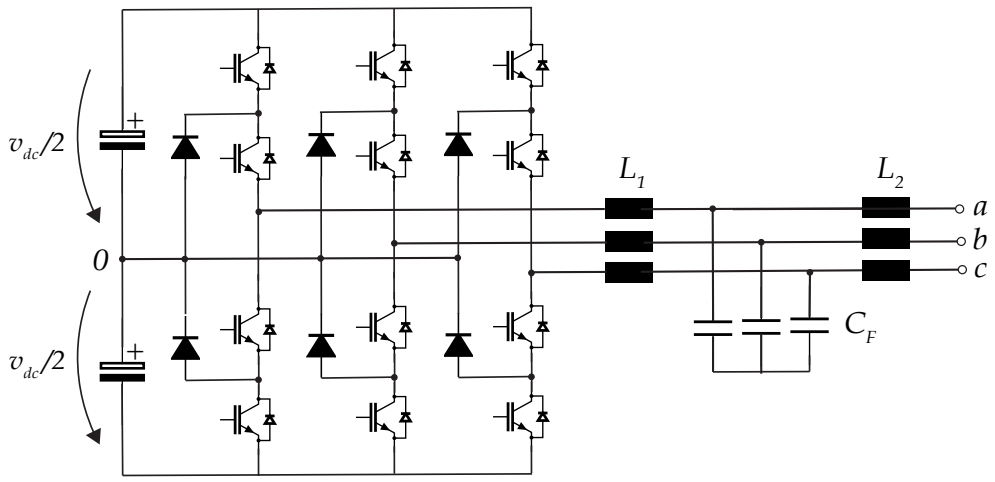


**Fig. 2.6:** Three-level voltage source converter neutral-point clamped (3L-NPC) with LCL output filter. VSC built with silicon IGBTs and silicon diodes

### 2.4.2 *SAPFs Efficiency and power losses figures*

In order to describe the current boundaries of SAPFs technology, a survey of industrial and commercially available active power filters was carried out. SAPFs designed to work on 400 V low-voltage power grids with nominal RMS currents close to 120 A were the specific target of the survey. Table 2.3 and Table 2.4 show the results of the survey where the supplier and model of each of the SAPF included are specified. In particular, Table 2.3 shows the SAPFs nominal current, the maximum harmonic order that can be compensated, and the control strategies available in each SAPF. The control strategies that can be chosen are the load current based control strategy or open current control (OCC), the supply current based control strategy or closed current loop control (CCC), and the voltage based control strategy (VCS). From Table 2.3, it can be seen that the majority of SAPFs work with the current based control strategies, either in open or closed loop. However, only a few power filters, like those from the companies COMSYS and Maschinenfabrik Reinhausen GmbH, can work with the voltage-based control strategy. This fact highlights the specialty of the voltage detection control strategy. Moreover, most active power filters can compensate up to the 50th harmonic order or up to 2.5 kHz. The reason is that the most relevant power quality standards, namely the IEC 61000-2-4 and the IEEE 519-2014 standards, set the limit for the voltage harmonic distortion in power grids only until the 49th harmonic. Truly, for the frequency interval between 2.5 kHz to 150 kHz, the so called supraharmonics range, no official limits for the voltage distortion that could take place in power systems exist yet. However, the standard IEC 610000-4-30, currently under development, will attempt to fulfill this gap in the near future [107]. Furthermore, Table 2.4 shows the power circuits' characteristics of the commercially active power filters included in the survey. Specifically, Table 2.4 includes the VSC topology, the output filter arrangement and the switching frequency used by each of the SAPF included in Table 2.3. The 3L-NPC topology and the LCL output filter are the most popular power circuit configurations among the active power filters. The latter is mostly due to the higher efficiency of the 3L-NPC topology over the two-level topology. For example, consider

**Table 2.3:** Commercially available SAPF by some of the largest active power filter producers around the world - Nominal ratings for low-voltage shunt active power filters

| Supplier | Model | Grid Voltage (V) | Nominal Current (A) | Control Strategy possible | Maximum Harmonic (Order) |
|---|---|---|---|---|---|
| COMSYS[108] | P200 | 400 | 120 | VCS | 100 |
| COMSYS[109] | P300 | 400 | 120 | OCC/CCC/VCS | 49 |
| Maschinenfabrik Reinhausen Gmbh (MR)[110] | Gridcon ACF | 400 | 125 | OCC/CCC/VCS | 51 |
| MERUS[111] | A2 | 400 | 100 | OCC/CCC | 50 |
| Danfoss[112] | AAF006 D | 400 | 120 | OCC/CCC | - |
| ICAR[113] | FA43 W | 400 | 120 | OCC/CCC | 49 |
| Sinexcel[114] | AHF 100 | 400 | 100 | OCC/CCC | 50 |
| Schaffner[115] | Ecosine | 400 | 120 | OCC/CCC | 50 |
| Enerdoor[116] | FINHRMA | 400 | 90 | OCC/CCC | 50 |
| EPCOS[117] | PQS | 400 | 120 | OCC/CCC | 50 |

**Table 2.4:** Commercially available low-voltage SAPF by some of the largest active power filter producers around the world - Power circuit characteristics

| Supplier | Model | VSC Topology | Output Filter | Switching Frequency (kHz) | Peak Efficiency (%) | Power Losses at peak eff. (W) |
|---|---|---|---|---|---|---|
| COMSYS[108] | P200 | 2L | LC | 7.2 - 20 | 98.5 | 1200 |
| COMSYS[109] | P300 | 2L | LCL | 10 | 96.7 | 2725 |
| MR[110] | Gridcon ACF | 3L-NPC | LCL | 10 | 97.8 | 1888.92 |
| Merus[111] | A2 | 3L-NPC | - | 20 | 97.7 | 1579 |
| Danfoss[112] | AAF006 D | 2L | LCL | 3.0 - 4.5 | 98 | 1648 |
| ICAR[113] | FA43 W | 3L-NPC | LCL | 24 | 97.8 | 1800 |
| Sinexcel[114] | AHF 100 | 3L-NPC | LCL | 20 -35 | 97 | 2060 |
| Schaffner[115] | Ecosine | 3L-NPC | LCL | 16 | - | - |
| Enerdoor[116] | FINHRMA | 2L | - | 20 | 97 | 1854.57 |
| EPCOS[117] | PQS | 3L-NPC | LCL | - | 98 | 1800 |

the Gridcon ACF and P300 power filters. Both have the same output filter, the same switching frequency and the same nominal compensating current. However the Gridcon ACF, which is a three-level based active power filter, exhibits a higher peak efficiency and lower power losses at the peak efficiency than the P300, which is a two-level based active power filter. Furthermore, although most active power filters share the 3L-NPC topology with LCL output filter, there is a great disparity in the switching frequencies among the different SAPF solutions. Regarding three-level based SAPFs working with a fixed switching frequency, the maximum switching frequency found is 24 kHz. Conversely, the minimum fixed switching frequency encountered in three-level based SAPFs is 10 kHz. Further, for SAPFs working with variable switching frequencies, the higher limit and lower limit found are 35 kHz and 3 kHz respectively. Furthermore, the SAPFs' peak efficiency is calculated as one minus the quotient between the power losses and the apparent power of the SAPFs. On this basis and resorting to Table 2.4, which shows the data provided by SAPFs' manufacturers, the maximum peak efficiency found among the industrial SAPFs was 98.5 % which corresponds to the COMSYS P200. In contrast, the minimum peak efficiency found was 97 % which corresponds to the peak efficiency of the AHF 100 and FINHRMA filters. Interestingly, the COMSYS P200 exhibits the highest efficiency among the SAPFs despite of the fact that the P200 is a two-level based SAPF. Nevertheless, the high efficiency of the P200 can be explained by the control strategy implemented in this filter. In particular, the P200 works with the voltage detection control strategy. Therefore, the P200 absorbs a substantial amount of harmonic active power from the power system which compensates for part of its internal power losses. Certainly, the efficiency exhibited by each SAPF is of great importance for studying the harmonic power recovery feature. The higher the efficiency of a particular SAPF, the higher the probability that it has to recover harmonic active power from the grid. In other words, the lower the power losses exhibited by a SAPF for a particular operating point, the higher the amount of harmonic active power that it can recover. Thus, from the survey of commercially available SAPFs, it becomes clear that the current boundary for the SAPFs' efficiency reaches the 98 % limit.

Next, a survey on scientific literature was carried out to contrast the state-of-the-art of industrial SAPFs with those of academia. The survey target was scientific publications

dealing with SAPFs where the efficiency or power losses achieved were reported. Although several scientific publications targeted SAPFs, few of those studies mention power losses or efficiency figures. Table 2.5 summarizes the results of a survey carried out in the IEEE Xplore database. Unfortunately, it was only possible to find four research papers dealing with SAPFs where the SAPF's efficiency was reported. It can be inferred from Table 2.5 that academic papers reported a maximum SAPF's efficiency achieved of 97.86 % for low-voltage power grids. In fact, the SAPF's efficiency of 97.86 % is reached by Kolar et al. in [118] using a 3L-NPC power circuit consisting of IGBT power switches and Silicon Carbide (SiC) antiparallel and clamping diodes. In sum, the larger SAPF's efficiencies encounter for state-of-the-art SAPFs can be seen in Fig. 2.7. Altogether, the efficiency that can be reached by a SAPF reaches the 98 % limit according to the information provided by industry and academia.

**Table 2.5:** Power circuit characteristics of SAPF from scientific literature that published figures of efficiency and power losses

| Author | Grid Voltage (V) | Nominal Current (A) | VSC Top. | Output Filter | Switching Frequency (kHz) | Peak Efficiency (%) |
|---|---|---|---|---|---|---|
| dos Santos[119] | 144 | 5.74 | 2L | LC | 10 | 88 |
| Kolar[118] | 400 | 17 | 3L NPC | LC | 48 | 97.86 |
| Wang[120] | 10k | 150 | MMC | LC | 5 | 98 |
| Orts [121] | 123 | 4 | 2L | LC | 19.2 | 80 |

## 2.5 SUMMARY

The state-of-the-art of SAPF technology has been discussed in this chapter. In particular, the discussion about the current technical boundaries in SAPF's technology was carried out in two parts. The first part dealt with the control strategies for the command of SAPFs. The state-of-the-art control strategies are open current control, closed current loop control, and the voltage based control strategy. The characteristics of each of these control strategies were described, and their advantages and disadvantages were highlighted. Truly, the open current control strategy is the recommended strategy when the objective is to compensate a single nonlinear and to contain the harmonics currents within the nonlinear load terminals. In contrast, the closed current loop control strategy is recommended when the objective is to compensate for the harmonic currents generated by several nonlinear loads or clusters of nonlinear loads. Indeed, additional functionalities such as power factor correction, load balancing, and flicker compensation can be easily added to the open or closed current control strategies. However, the current based control strategies are not the recommended techniques when the objective is to compensate for the background harmonic distortion or suppress resonances. In addition, the current based control strategies cannot be applied if external current sensors can not be installed in the power grid. In the latter cases, the voltage control strategy is the recommended control technique. A SAPF driven by the voltage control strategy, namely a VSAPF, suppresses resonances, mitigates the harmonic background distortion impact in the PCC, and reduces the distortion at the PCC due to harmonic currents generated by nonlinear loads. Nevertheless, the voltage control strategy is prone to instabilities

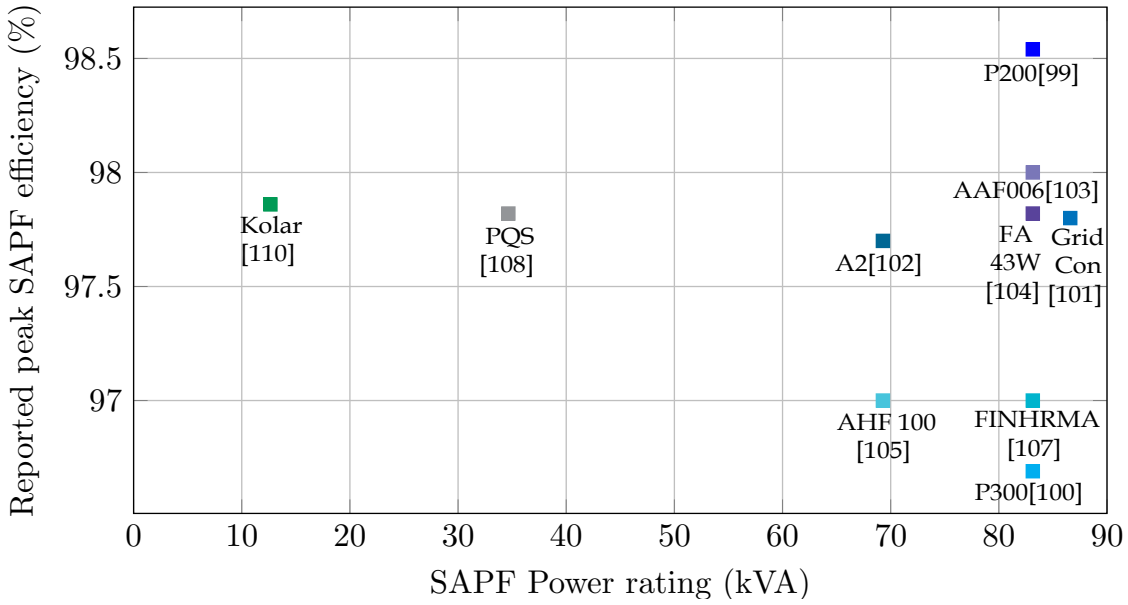


**Fig. 2.7:** Comparison of efficiency figures for state-of-art shunt active power filters. Based on [108, 109, 110, 111, 112, 113, 114, 116, 117, 118]

due to delays on the SAPF's control system and SAPF's power circuit. Also, additional functionalities such as load balancing and power factor correction can not be easily added to a VSAPF. The latter, at least not without installing first supplementary current sensors on the grid or load side. All in all, as the survey on state-of-the-art industrial SAPFs presented in this chapter has shown, most of SAPF work with the open or closed current control strategies. On the other hand, only a handful of industrial SAPF can be configured with the voltage detection strategy, a fact that highlights the specialty of this control strategy. Moreover, the detection of harmonic voltage and current components is common to all the SAPF's control strategies. In other words, each control strategy relies on a signal processing method that separates the fundamental component from the harmonic components of current or voltage signals, or both. Although several signal processing techniques to perform the harmonic extraction exist (see Fig. 2.3), the most common detection techniques used are the PQ theory [48] and the Harmonic DQ frame theory [93]. In sum, the Harmonic DQ frame theory is the favored harmonic extraction method for selective harmonic compensation. In contrast, the PQ theory is the suggested method to perform harmonic compensation on a wide frequency range. Both of these harmonic extraction methods exhibit fast transient response times, high steady-state accuracy, and robustness against unbalance voltages and currents [94].

Finally, this chapter discussed the second part of the technology boundaries for SAPFs, namely the power electronics circuits. For low-voltage power grids where the line-to-line voltages lie between 400 V and 690 V, 2L and 3L VSC based SAPF are commonly found in industrial applications and in academia. On the one hand, the advantages of the 2L topology are its simplicity, lower number of components and higher reliability. On the other hand, 3L NPC based SAPFs exhibit higher efficiencies, higher compactness and better EMI behavior than 2L based SAPFs. Furthermore, from the literature review presented in this chapter, it can be concluded that state-of-the-art SAPFs for distribution power systems are constructed with the 3L-NPC topology. In other words, the 3L-NPC power circuit topology is the preferred choice in state-of-the-art SAPFs. This trend can be seen in active power filters investigated by academia and industrial SAPFs available in

the market. Moreover, the switching frequencies for state-of-the-art SAPF's power circuits can be found between 10 and 35 kHz with efficiencies at full-load in the range of 97 % to 98 %. Thus, an efficiency of 98 % will be considered the benchmark for the efficiency of state-of-the-art SAPFs for future discussions.

# 3

# Silicon Carbide Power Devices Technology

In the last chapter, it was shown that state-of-the-art high efficient SAPFs solutions are based on three-level power circuits. Those three-level power circuits are built in modern SAPF with pure silicon semiconductors devices such as silicon IGBT and diodes. However, new technologies in the form of Wide Band Gap (WBG) semiconductors have recently stepped into the power electronics field. In particular, SiC MOSFET technology is the recommended WBG technology for applications that manage hundreds of amperes and require power devices with blocking voltages larger than 600 V [122]. On these high voltage applications (>600 V), SiC MOSFETs outperform their silicon IGBTs counterparts since SiC MOSFETs are unipolar devices that have no stored charges that need to be removed during the switching process [123]. Thus, power converters that use SiC MOSFETs can be driven at increased switching frequencies with low switching losses and can be implemented with smaller AC filters [124]. Therefore, SiC based two-level converters operating at high switching frequencies can reach efficiencies comparable to or superior to pure silicon-based 3L converter solutions due to the low switching losses and low AC filter losses [99, 124]. As it was already pointed out in section 1.4, a critical aspect of the harmonic power recovery is an ultra-low losses SAPF's power circuit. In simpler terms, harmonic power recovery employing a VSAPF is only possible if the VSAPF's power losses are lower than the harmonic active power intake. Therefore, if the aim is to recover a significant amount of harmonic active power, we are interested in the SAPF's solution that exhibits the lowest power losses possible. On this basis, this chapter focuses on SiC semiconductors as enabler technology to achieve an ultra-low losses SAPF solution. Specifically, some of the essential aspects of SiC MOSFETs will be addressed and explanations about how these devices can be used to reduce the SAPF's power losses will be given.

## 3.1 Power Losses on Shunt Active Power Filters

The entire VSAPF´s power losses are distributed between the power semiconductors and the passive output filter. According to Kuhnhenne in [125], 66 % of SAPF´s power losses are caused by the switching operation of the power semiconductors, and the remaining 34 % is caused by the harmonic compensating currents flowing over the output filter. Obviously, the core and winding losses on the SAPF´s coupling inductors are responsible for a large share of the power losses in the passive output filter. Indeed, using SiC power switches can help decrease the SAPF´s power losses not only in the power semiconductors but also in the passive output filter.

### 3.1.1 *Power Semiconductor Losses*

The most significant power losses that occur in a particular power semiconductor are distributed between static losses or on-state conduction losses ($P_{\text{Cond}}$) and switching losses ($P_{\text{Sw}}$) [126]:

$$P^{\text{Semi}}{}_{\text{Losses}} = P_{\text{Cond}} + P_{\text{Sw}} \tag{3.1}$$

The on-state losses are defined by the output characteristic of a particular power switch. For example, for bipolar power devices (e.g. Si based IGBT and diodes), the average conduction power losses over an evaluation period $T$ can be calculated using the following expression [127]:

$$P^{\text{IGBT}}{}_{\text{Cond}}\left(i_{\text{ce}}(t), T_{\text{j}}, V_{\text{gate}}\right) = \frac{1}{T}\int_0^T V_{\text{ce(sat)}}\left(i_{\text{ce}}(t), T_{\text{j}}, V_{\text{gate}}\right) \cdot i_{\text{ce}}(t)dt \tag{3.2}$$

where $V_{\text{ce(sat)}}$ stands for the voltage between collector-to-emitter in the IGBT and $i_{\text{ce}}$ stands for the current flowing over the IGBT device. Obviously, $V_{\text{ce(sat)}}$ depends on the junction temperature $T_{\text{j}}$, the gate voltage $V_{\text{gate}}$, and the current $i_{\text{ce}}$. Furthermore, the evaluation period $T$ is generally taken as one period of the grid voltage. On the other hand, for unipolar power devices such as SiC power MOSFETs, the conduction losses are entirely characterized by the ohmic characteristic of the power switch ($R_{\text{ds,on}}$). In fact, the conduction losses in a unipolar device can be calculated according to [128]:

$$P^{\text{FET}}{}_{\text{Cond}}\left(i_{\text{ds}}(t), T_{\text{j}}, V_{\text{gate}}\right) = \frac{1}{T}\int_0^T R_{\text{ds,on}}\left(i_{\text{ds}}(t), T_{\text{j}}, V_{\text{gate}}\right) \cdot i^2{}_{\text{ds}}(t)dt \tag{3.3}$$

where $i_{\text{ds}}$ stands for the current flowing over the drain and source terminals. Clearly, it can be seen that the resistance $R_{\text{ds,on}}$ depends on the junction temperature $T_{\text{j}}$, the gate voltage $V_{\text{gate}}$, and the drain-to-source current $i_{\text{ds}}$. Moreover, the switching losses that occur in a particular semiconductor can be expressed mathematically as [128]:

$$P_{\text{Sw}}(I_{\text{on}}, I_{\text{off}}, V_{\text{on}}, V_{\text{off}}, T_{\text{j}}) = \frac{1}{T}\sum_{i=1}^{N_{\text{sw,on}}} E_{\text{on}}(I_{\text{on,i}}, V_{\text{on,i}}, T_{\text{j}}) + \sum_{i=1}^{N_{\text{sw,off}}} E_{\text{off}}(I_{\text{off,i}}, V_{\text{off,i}}, T_{\text{j}}) \tag{3.4}$$

where $E_{\text{on}}$ and $E_{\text{off}}$ are the switching loss energies for switching-on and switching-off transitions, $V_{\text{on,off}}$ and $I_{\text{on,off}}$ are the voltage and currents on the power switch prior to the switching transition, and where $N_{\text{sw,on}}$ and $N_{\text{sw,off}}$ are the number of turn-on and turn-off transitions happening within the time interval $T$. Although (3.2) to (3.4) are the correct mathematical expressions to calculate the power losses produced in a power semiconductor, it is very common to use simpler mathematical expressions to calculate the power losses during the design of a power electronics circuit [129]. If it is assumed that $V_{\text{gate}}$ is constant and time invariant, and that the output characteristic of a power semiconductor can be approximated by a straight line, and that the forward voltage (if it exists) can be taken as constant [127], equations (3.2) to (3.4) can be simplified. As result the following mathematical expressions can be used to estimate the conduction power losses [130][131]:

$$P^{\text{IGBT}}{}_{\text{Cond}}(i_{\text{Avg}}, i_{\text{rms}}, T_{\text{j,Avg}}) = V_{\text{CEo}}(T_{\text{j,Avg}})i_{\text{Avg}} + R_{\text{ce}}(T_{\text{j,Avg}})i^2{}_{\text{rms}} \tag{3.5}$$

$$P^{\text{Diode}}{}_{\text{Cond}}(i_{\text{Avg}}, i_{\text{rms}}, T_{\text{j,Avg}}) = V_{\text{fd}}(T_{\text{j,Avg}})i_{\text{Avg}} + R_{\text{fd}}(T_{\text{j,Avg}})i^2{}_{\text{rms}} \tag{3.6}$$

$$P^{\text{FET}}{}_{\text{Cond}}(i_{\text{Avg}}, i_{\text{rms}}, T_{\text{j,Avg}}) = R_{\text{ds,on}}(T_{\text{j,Avg}})i^2{}_{\text{rms}} \tag{3.7}$$

where $R_{ce}$ is the collector-to-emitter equivalent resistance on an IGBT, $R_{fd}$ is the equivalent on-resistance of a power diode, and $R_{ds,on}$ is the drain-to-source equivalent resistance on a power MOSFET. Additionally, $T_{j,Avg}$ stands for the average value of the junction temperature, and $i_{Avg}$ and $i_{rms}$ are the average and RMS values of the current flowing through the power device. Notice that $i_{Avg}$ and $i_{rms}$ are different from the average and RMS values of the converter´s phase output current. The latter is because the phase current commutates among the different power switches within the power circuit depending on the modulation method and the control strategy during the evaluation period $T$ [131]. On the other hand, the switching power losses equation presented in (3.4) can be simplified by assuming an output phase current that has a sinusoidal shape with peak value $I_{Peak}$. Under such assumption, the switching power losses can be estimated by [127, 132]:

$$P^{IGBT}{}_{Sw} = \frac{1}{\pi} \cdot f_{Sw} \cdot E_{on\,+\,off} \cdot \left(\frac{I_{Peak}}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{dc}}{V_{ref}}\right)^{K_v} \tag{3.8}$$

$$P^{FET}{}_{Sw} = f_{Sw} \cdot \left[\left(\frac{1}{\pi} \cdot E_{on\,+\,off} \cdot \left(\frac{I_{Peak}}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{dc}}{V_{ref}}\right)^{K_v}\right) + (C_{OSS} \cdot V^2{}_{dc})\right] \tag{3.9}$$

$$P^{Diode}{}_{Sw} = \frac{1}{\pi} \cdot f_{Sw} \cdot E_{rr} \cdot \left(\frac{I_{Peak}}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{dc}}{V_{ref}}\right)^{K_v} \tag{3.10}$$

where $f_{Sw}$ stands for the switching frequency, $V_{dc}$ is the DC-Bus voltage of the circuit, and $C_{OSS}$ is the output capacitance of the power MOSFET switch. Moreover $V_{ref}$ and $I_{ref}$ are the references for the switching energies $E_{on}$ and $E_{off}$ given in the power semiconductor's datasheet. In any case, the coefficients $K_i$ and $K_v$ ensure a better fitting of the energies $E_{on}$ and $E_{off}$ taken from datasheet with the specific circuit values $V_{dc}$ and $I_{Peak}$ [127]. The typical and recommended values for the fitting coefficients $K_i$ and $K_v$ lie between 1 and 1.4 [129]. It is granted that equations (3.91) to (3.10) are valid only for output currents with a sinusoidal shape. Nevertheless, these equations serve as indicator to show that the switching losses are directly proportional to the switching loss energies. Of course, this is going to be also the case for the SAPF.

Moreover, it can be seen from (3.5) and (3.7) that SiC power MOSFETs show a clear advantage over Si IGBT power switches in terms of conduction losses. Because power SiC MOSFETs do not exhibit the forward voltage drop $V_{CEo}$ (typically 0.7 V on Si IGBT) and therefore power losses due to the $V_{CEo} \cdot i_{Avg}$ term do not take place using unipolar SiC MOSFETs. Furthermore, from (3.5) and (3.7), it can be concluded that power semiconductors exhibiting small $R_{ce}$ and $R_{ds,on}$ will have a positive influence reducing the conduction losses. Truly, SiC MOSFET switches can be designed with very low values of $R_{ds,on}$ due to the properties of the SiC material as will be explained in section 3.3. On the other hand, from (3.9) and (3.10) it may be inferred that the semiconductor's parameters that influence the switching losses are the $E_{on\,+\,off}$ loss energies in case of power switches and the $E_{rr}$ recovery loss energy in case of the power diodes. It is granted that the lower the switching loss energies on the power semiconductors, the lower will be the switching losses. Certainly, SiC MOSFETs exhibit lower $E_{on\,+\,off}$ energy losses than Si IGBTs because no stored carriers need to be removed on the on-off switching transition, and thus no tail currents take place on unipolar SiC MOSFETs. In addition, SiC MOSFETs have smaller capacitances than Si IGBT allowing them to have very fast switching transitions leading to small $E_{on\,+\,off}$ energies. Furthermore, SiC Schottky Barrier Diode (SBD)s exhibit almost zero $E_{rr}$ recovery loss energy and clearly outperform Si bipolar diodes in terms of switching losses. On the whole, the benefits of SiC power switches over Si power switches are lower conduction losses, lower switching losses, and lower gate driving

losses [123]. These benefits can be explained in terms of the physical properties of SiC as semiconductor material and its impact on the semiconductor device's design. The latter will be discussed in the next section.

### 3.1.2 *Output Filter Power Losses*

On a VSC, the SAPF´s output filter is meant to eliminate the frequency components on the compensation currents that arise due to the switching process. Put it simply, the output filter should eliminate the current ripple which exhibits frequencies around integer multiples of the switching frequency. In its simplest form, the output filter is of the LC type and is formed only by coupling inductors and a ripple filter. Generally speaking, the ripple filter is designed to behave as a first-order High Pass Filter (HPF) with a cut-off frequency of half of the switching frequency [17]. In particular, the ripple filter is formed by the damping resistors $R_F$ and the ripple capacitors $C_F$ (see Fig. 3.1). Even though the value of $C_F$ can be selected arbitrarily depending on the reactive power requirements or impedance of the grid, the value of the series damping resistors can be calculated based on the $C_F$ value as follows:

$$R_{\mathrm{F}} = \frac{1}{2 \cdot \pi \cdot \frac{f_{\mathrm{Sw}}}{2} \cdot C_{\mathrm{F}}} \tag{3.11}$$

Clearly, the power losses on the damping resistors are directly proportional to the value of $R_F$. Likewise, power losses do occur on the Equivalent Series Resistor (ESR) of the ripple capacitor. However, these losses are not significant due to the low values of ESR exhibited by modern power capacitors and can be disregarded [133]. Truly, the more significant losses on the output filter occur on the coupling inductors $L_{2\mathrm{L}}$. In fact, the coupling filter inductors are designed to limit the maximum current ripple $\Delta I_{\mathrm{pp}}$ to a specific value. In this regard, it is very typical to limit the maximum current ripple to 20 % of the nominal current of the active power filter [118]. Therefore, for 2L-VSC based power converters, the minimum inductance necessary to achieve $\Delta I_{\mathrm{pp}}$ can be calculated as [35]:

$$L_{2\mathrm{L}} = \frac{V_{\mathrm{DC}}}{8 \cdot f_{\mathrm{Sw}} \cdot \Delta I_{\mathrm{pp}}} \tag{3.12}$$

where $V_{DC}$ is the DC-Bus voltage. In fact, (3.12) implies that the coupling inductor $L$ can be made smaller if the switching frequency is increased while maintaining the current ripple constant. Namely, working at higher switching frequencies, the current ripple can be maintained constant for smaller values of the coupling inductor. Smaller

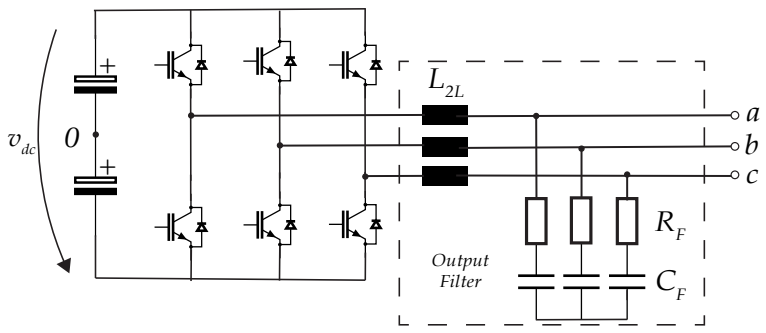


**Fig. 3.1:** Output filter for two-level based SAPF. The output filter is formed by the coupling inductors $L_{2\mathrm{L}}$, ripple filter capacitor $C_{\mathrm{F}}$ and damping resistor $R_{\mathrm{F}}$. Based on [17]

coupling inductors are advantageous because the inductor's power losses and inductor's volume are reduced. In fact, Kolar et al. in [134] and [135] investigated the relationship between the inductor's power losses and the switching frequency for a two-level based converter. Although the Kolar's research was focused on rectifiers for telecommunication applications, a similar pattern will arise between the inductor's power losses and the switching frequency on SAPFs. It follows that for active rectifiers, the power losses on the coupling inductor can be approximated by the following mathematical expression [135]:

$$P_{\mathrm{L}} = K_{\mathrm{Core}} \cdot {V_{\mathrm{L}}}^{\frac{4(2-\beta)}{3(2+\beta)}-\frac{1}{3}} \cdot {f_{\mathrm{Sw}}}^{\frac{2(\alpha-\beta)}{2+\beta}} \cdot {I_{\mathrm{RMS}}}^{\frac{2\beta}{2+\beta}} \cdot {V_{\mathrm{DC}}}^{\frac{2\beta}{2+\beta}} \tag{3.13}$$

where $V_{\mathrm{L}}$ is the volume of the coupling inductor, and $K_{\mathrm{Core}}$ depends of core material used to build the inductor. Moreover, $\alpha$ and $\beta$ are constants that correspond to the parameters of the Steinmetz equation. Indeed, the Steinmetz equation is used to calculate the inductor's core losses analytically. Furthermore, the Steinmetz parameters depend on the material used for the inductor's core. For instance, if nanocrystalline Vitroperm 500F is selected as core material for the coupling inductor, the Steinmetz parameters become $\alpha = 1.32$ and $\beta = 2.1$ [136]. Thus, the power losses of an inductor made of Vitroperm 500F, according to (3.13), become:

$$P_{\mathrm{L}} = K \frac{V_{\mathrm{DC}} \cdot I_{\mathrm{RMS}}}{{f_{\mathrm{Sw}}}^{\frac{19}{50}} \cdot {V_{\mathrm{L}}}^{\frac{9}{20}}} \tag{3.14}$$

From (3.14), it can be seen that increasing the switching frequency will reduce the inductor's power losses. All in all, increasing the switching frequency will decrease the power losses in the coupling inductor, the same as the power losses in the damping resistors $R_F$ as can be seen in (3.14) and (3.11) respectively. In other words, increasing the converter's switching frequency by means of SiC MOSFET semiconductors will reduce the power losses in the VSAPF's output filter. Of course, the higher the switching frequency, the higher the switching losses in the converter as can be seen in (3.9) and (3.10). On account of this, in any converter design, a compromise between the reduction of power losses in the output filter and the increase in switching losses needs to be found. Typically, there is an optimal switching frequency where the overall losses of the power converter become minimum [137]. This optimal frequency will depend on the power rating of the power converter, the topology used, and other parameters in the power circuit such as DC-Bus voltage, core materials and others [4]. For the specific case of the SAPF, the trade-offs between output filter losses and semiconductors switching losses are discussed in Chapter 6. Besides, in the same chapter, an analysis for the switching frequency that leads to minimum SAPF 's power losses is performed for two-level and three-level power circuits.

## 3.2 WIDE BAND GAP (WBG) MATERIALS

SiC is a compound semiconductor that consists of two materials of the Group IV of the periodic table: silicon and carbon. Indeed, SiC semiconductor material exhibits high thermal conductivity, high chemical stability, and high hardness due to the strong chemical bonding between silicon and carbon atoms [138]. Furthermore, the SiC semiconductor material has outstanding electrical properties as a larger band gap ($E_g$) and a higher saturated electron velocity than silicon (see Table 3.1 [139] [140]). Certainly, the material's band gap has a direct correction to the material's critical field $E_{\mathrm{Cri}}$. Furthermore, Table 3.1 shows the Gallium Nitrite (GaN) and Diamond materials in addition to SiC. Truly,

**Table 3.1:** Material Properties comparison between Si, SiC, GaN and Diamond

| Parameter | Unit | Silicon (Si) | 4H-SiC | GaN | Diamond |
|---|---|---|---|---|---|
| Band gap $E_g$ | eV | 1.12 | 3.26 | 3.39 | 5.47 |
| Critical Field $E_{\mathrm{Cri}}$ | MV/cm | 0.23 | 2.2 | 3.3 | 5.6 |
| Relative Permitivity $E_{\mathrm{r}}$ | | 11.8 | 9.7 | 9.0 | 5.7 |
| Electron Mobility $\mu_{\mathrm{n}}$ | $\mathrm{cm}^2/\mathrm{Vs}$ | 1400 | 950 | 1500 | 1800 |
| Sat. Electron Velocity | $10^7\mathrm{cm/s}$ | 1.0 | 2.0 | 2.5 | - |
| Thermal Conductivity | W/cmK | 1.5 | 3.8 | 1.3 | 20 |
| Intr. Concentration $n_{\mathrm{i}}$ | $cm^{-3}$ | $1.4 \cdot 10^{10}$ | $8.2 \cdot 10^{-9}$ | $1.9 \cdot 10^{-10}$ | $1 \cdot 10^{-22}$ |

GaN and Diamond are also wide band gap materials and are included in Table 3.1 only for comparison purposes. Table 3.1 shows that SiC has a band gap three times higher than silicon and a critical field almost ten times bigger. Moreover, SiC has a thermal conductivity 2.5 times larger than silicon, which means that SiC conducts heat out of the semiconductor structure much better than silicon. Due to its high thermal conductivity and low intrinsic concentration, before 2001, SiC was mainly used on applications that needed electronic devices operating at high temperatures (e.g. in military equipment). Indeed, the first studies that recognized the huge potential of SiC as material for power semiconductors were carried out by Baliga and his group in General Electric in 1985 [141]. They derived the theoretical models that predicted significant reductions in the specific on-resistance of unipolar devices (e.g. SiC MOSFETs and SBD) if SiC was used as material for the semiconductor's drift region. According to this analysis, the first 4H-SiC SBD device with high-voltage capabilities was demonstrated by Kimoto et al. in 1995 [142]. Based on the work presented in [142], Infineon performed improvements and optimizations on the 4H-SiC SBD design that led finally to the first commercial SiC SBD product in 2001 [138]. In any case, this first commercial available SiC SBD was designed to be used as power diode in power factor correction circuits [143]. Clearly, SiC semiconductors bring many technical advantages compared to silicon-based semiconductors such as lower specific on-resistance, lower switching losses, and high temperature operation. However, SiC is a material that is rarely found in nature. Thus, the production of SiC semiconductors is expensive due to the complex technology required to grow SiC crystals, and epitaxial layers [144][145]. Even today, and despite the technological advances in semiconductor manufacturing technology, the price of SiC semiconductors is four times higher than the price of Si semiconductors [130]. For this reason, SiC semiconductors are used only in applications where a significant improvement in performance or cost reduction (e.g. smaller magnetics, reduced cooling, smaller footprint) can be achieved at the system level ([146] as cited in [143]).

On the other hand, if we observe Table 3.1, it can be seen that GaN exhibits better properties than SiC as semiconductor material. In particular, GaN exhibits a larger band gap and higher critical field than SiC. However, GaN devices are relatively young and have a completely different semiconductor structure than unipolar SiC devices. Actually, state-of-the-art GaN devices, namely GaN High Electron Mobility Transistors (HEMT), are lateral semiconductor devices in contrast to SiC MOSFETs, which hold a vertical structure. Indeed, the blocking voltage capability of a GaN HEMT transistor is limited by the distance between its drain and gate contacts as can be seen in Fig. 3.2 [122]. Therefore, if the goal is to block high voltages with a GaN lateral device, the spacing between gate and drain contacts must be large. The latter will imply a larger drift region, a larger cell pitch, and in consequence an impractical high on-resistance [147]. For this

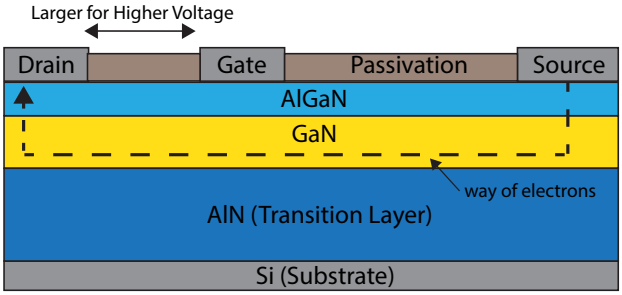


**Fig. 3.2:** Lateral GaN HEMT basic structure. Based on [147]

reason, GaN HEMT transistors are not typically used in applications beyond 600 V [145]. Of course, this would change if GaN HEMT transistors with vertical structures make it to the market. In fact, GaN transistors with vertical structures have been under research since 2016. However, they are not viable in practice yet due to reliability concerns, high defect density, and still high costs [148, 149]. For example, high electric fields produced by high voltages will affect the gate-oxide interface, leading to the destruction of GaN transistors. Nonetheless, this situation may change in the incoming 5 to 10 years, when probably GaN transistors will compete with SiC MOSFETs in high-voltage applications. In the following section, it is explained how the SiC material's properties are translated into advantages on the power switch realization.

## 3.3 SILICON CARBIDE MOSFETS

From (3.7), it can be inferred that the conduction losses in a unipolar device are heavily influenced by the parameter $R_{ds,on}$. Moreover, the parameter $R_{ds,on}$ is determined by the different layers that form the structure of a unipolar power device. In other words, each layer of the device's structure contributes to the overall resistance of the power switch. Take, for instance, a unipolar planar SiC MOSFET whose vertical structure is depicted in Fig. 3.3. The total $R_{ds,on}$ resistance of the unipolar MOSFET depicted in Fig. 3.3 can be expressed as [150]:

$$R_{ds,on} = R_{s*} + R_{n+} + R_{Ch} + R_a + R_{JFET} + R_{Drift} + R_{Sub} \tag{3.15}$$

where $R_{s*}$ is the resistance of package, $R_{n+}$ is the N-type Source resistance dependent on source doping, $R_{Ch}$ is the channel resistance of the MOSFET in the on-state, $R_a$ is the resistance of p-body edge and the gate, $R_{JFET}$ is the Resistance of the JFET region of the MOSFET, $R_{Drift}$ is the resistance of voltage blocking drift region and $R_{Sub}$ is the N-type drain resistance dependent on drain doping [151]. It turns out that the elements that contribute the most to the total on-state resistance are the channel resistance $R_{Ch}$ and the drift region resistance $R_{Drift}$ [150][151]. In particular, the drift resistance in a unipolar device is equal to [152]:

$$R_{Drift} = \frac{L_{drift}}{q \cdot \mu_n \cdot N_D \cdot A} \tag{3.16}$$

where $L_{drift}$ is the length of the drift region, $q$ stands for the net charge of an electron ($1.6 \cdot 10^{-19}$ C), $\mu_n$ is the electron mobility of the drift region material, $N_D$ is the number of electrons on the volume, and $A$ is the active area of the drift region.

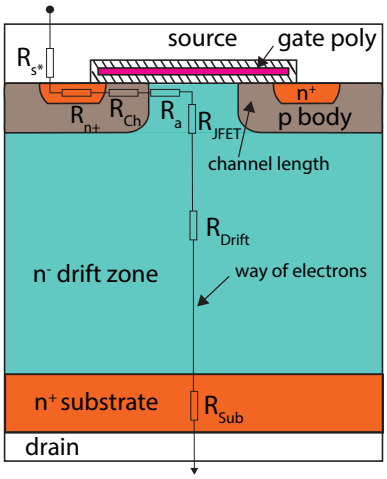


**Fig. 3.3:** Planar MOSFET basic structure. Based on [150]

### 3.3.1 *Breakdown voltage and Drift region*

Generally speaking, the maximum voltage that a power switch can sustain is denominated breakdown voltage $V_{BR}$. If a voltage beyond $V_{BR}$ is applied to the power switch, impact ionization occurs within the power switch. In such a case, the power switch device enters into breakdown avalanche and loses its voltage blocking capabilities [153]. Specifically, the breakdown voltage is related with $L_{drift}$ and $E_{Cri}$ according to [154]:

$$V_{BR} = \frac{1}{2} \cdot L_{drift} \cdot E_{Cri} \tag{3.17}$$

Table 3.1 shows that the critical field $E_{Cri}$ of SiC is ten times higher than the critical field of silicon. Therefore, equation (3.17) implies that $L_{drift}$ can be made smaller for the same $V_{BR}$ if SiC is used as crystal instead of silicon. Of course, a smaller $L_{drift}$ has a very positive impact decreasing the on-resistance of the drift region as can be inferred from (3.16). This is an advantage in favor of the SiC material because pure silicon MOSFETs are not used beyond 600 V due to the large $L_{drift}$ that will be necessary. In the latter case, a very large $L_{drift}$ will imply a very high $R_{Drift}$ that will lead ultimately to unacceptable high on-state losses for silicon MOSFET with blocking voltages beyond 600 V[130]. As an illustration, Fig. 3.4 shows the semiconductor structures of a Si MOSFET and a SiC MOSFET as presented by Zhang in [155]. Both devices are designed for a $V_{BR}$ of 1200 V. From the figure, it can be seen that the length of the drift region needs to be 120 $\mu$m large if silicon is used as material for the drift region. In contrast, if SiC is used as drift region's material, the drift region can be thinner. In effect, only 12 $\mu$m on the drift layer are needed to block 1200 V using SiC. In addition, due to the thinner layer on a SiC MOSFET, the doping on the drift region can be increased. Actually, Zhang in [155] states that the doping of the drift region in a SiC MOSFET can be made 100 times higher than the doping that is possible with pure silicon. Specifically, the drift region's doping in a Si MOSFET is only $1 \cdot 10^{14}\ cm^{-3}$ in comparison with the $1 \cdot 10^{16}\ cm^{-3}$ in a SiC MOSFET [157]. Due to the higher doping, the $R_{Drift}$ on a unipolar SiC MOSFET decreases even further compared to the $R_{Drift}$ in a unipolar silicon MOSFET. Actually, according to Friedrichs in [156], the dimensioning and the design of a MOSFET using SiC for 1200 V is very comparable to the design of a silicon MOSFET meant for 50 V. Moreover, due to the high critical field, SiC MOSFETs can be used in high voltage applications (e.g. 1200 V), achieving reasonable small on-resistances without the need to add a p+ back emitter

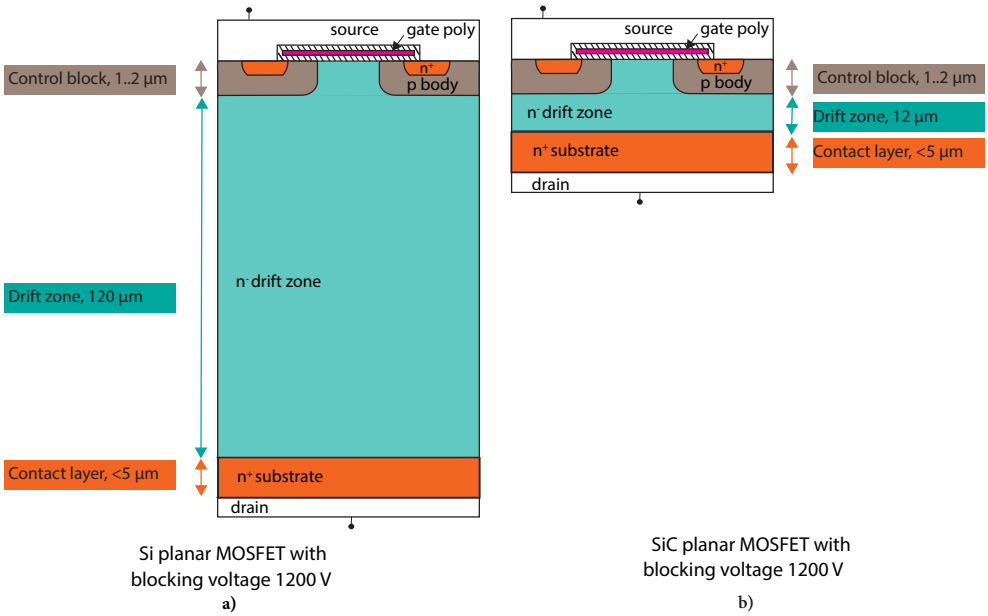


**Fig. 3.4:** Si and SiC Planar MOSFETs structures with blocking voltage 1200 V. Based on [155][156]

layer as is the case on silicon IGBTs [123]. The latter can be seen in Fig. 3.5 which shows the structure of a silicon Punch Through (PT) IGBT and a SiC MOSFET. Once again both devices are rated for a blocking voltage of 1200 V. Although the length of the drift region of the IGBT is thicker than the drift region of the SiC MOSFET, the electron-hole plasma produced by the p+ back emitter layer improves the overall on-state voltage drop in the IGBT. Thus, the p+ back emitter layer helps to reduce the conduction losses in the PT IGBT [157]. On this basis, it may be possible that the silicon IGBTs and SiC MOSFETs reach the same conduction losses at high temperatures. However, SiC MOSFETs will always exhibit faster switching transitions and thus lower switching losses than silicon IGBTs. This is because no stored charges need to be extracted during the turn-on and turn-off transitions [158]. Even, Schletz in [159] claims that the commercial limit for SiC unipolar MOSFET will lie between 3.3 kV to 4.5 kV, and just beyond these voltages, a device such as a SiC-based IGBT will be necessary.

### 3.3.2 *Specific on-resistance*

From (3.16), it can be seen that the chip area plays an important role in the overall $R_{\text{Drift}}$. At the same time, the chip's area also plays an important role in the production costs of the power semiconductor. On the one hand, it is possible to make the $R_{\text{Drift}}$ resistance very small by choosing a very large chip's area. On the other hand, the latter situation will be very disadvantageous for semiconductor manufacturers because a large chip's area increases the production costs dramatically. Therefore, during the chip's design, a trade-off between production costs and chip's area needs to be made. In this regard, the concept of specific on-resistance and the Figure-of-Merit (FOM) of semiconductor materials serve to quantify the mentioned trade-off. From (3.17), it can be inferred that if the drift region is brought under the electrical field $E_{\text{Cri}}$, this field must be supported by a concentration of electrons along the drift region [153][154]. Actually, the total electrons'

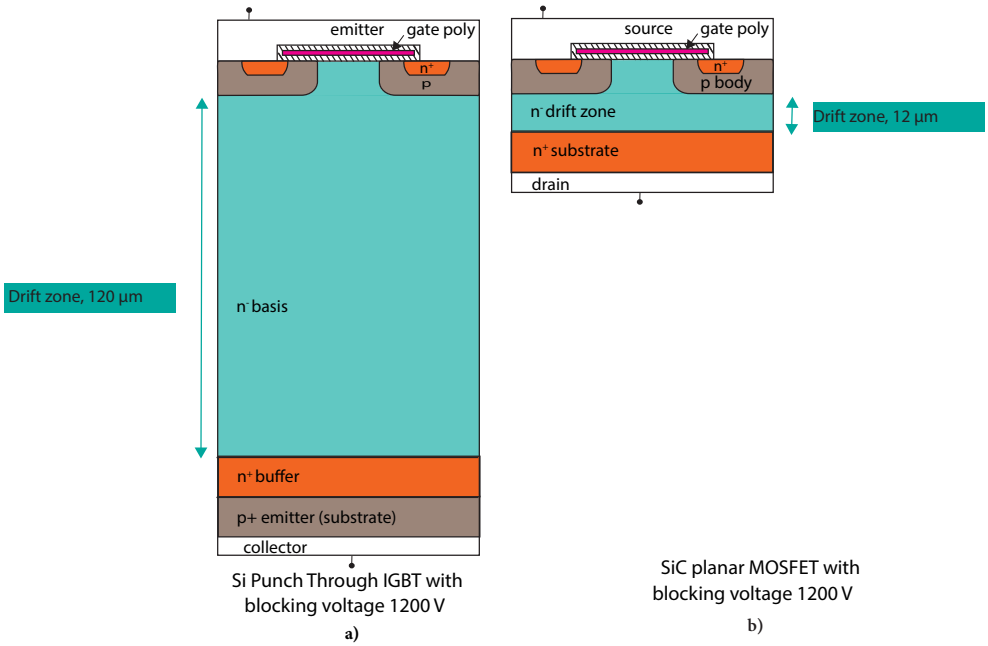


**Fig. 3.5:** Planar SiC MOSFET and PT Si IGBT structures with blocking voltage 1200 V. Based on [158]

charge ($q \cdot N_D$) in the drift region that supports the field $E_{Cri}$ can be calculated using the Poisson's equation [140]:

$$q \cdot N_D = \frac{E_r \cdot E_o \cdot E_{Cri}}{L_{drift}} \tag{3.18}$$

where $E_o$ is the permeability of the vacuum $1.26 \cdot 10^{-6}\, H/m$, and $E_r$ is the relative permeability of the drift material. From (3.16), the theoretical on-resistance per area or specific-resistance for unipolar devices can be calculated as:

$$R_{Drift} \cdot A = \frac{L_{drift}}{q \cdot \mu_n \cdot N_D} \tag{3.19}$$

combining (3.17) and (3.18) with (3.19) leads to:

$$R_{Drift} \cdot A = \frac{4 \cdot V^2_{BR}}{E_r \cdot E_o \cdot \mu_n \cdot E^3_{Cri}} = \frac{4 \cdot V^2_{BR}}{BFOM} \tag{3.20}$$

where $BFOM = E_r \cdot E_o \cdot \mu_n \cdot E^3_{Cri}$ is the so-called Baliga's Figure-of-Merit (BFOM) [141]. In this regard, Table 3.2 shows the BFOM normalized against the BFOM of silicon for the different materials mentioned in Table 3.1. Moreover, the specific on-resistance is related to the breakdown voltage $V_{BR}$ and the inverse of the BFOM as it can be seen from (3.20). Therefore, at least theoretically, SiC-based semiconductor dies can be made 500 times smaller in area than Si dies, achieving the same specific on-resistance for the same breakdown voltage. It follows that the high BFOM of SiC material allows semiconductor manufacturers to design SiC MOSFETs following essentially two approaches. Namely, the high-performance approach and the cost reduction approach [155]. In the high-performance approach, the SiC die is designed with the same area as a silicon die, leading to a SiC MOSFET with much lower $R_{ds,on}$ than a silicon MOSFET. On the other hand, in the costs reduction approach, the SiC die is made smaller in area than the silicon die and designed to achieve a comparable or slightly smaller $R_{ds,on}$ resistance. Commonly,

**Table 3.2:** Baliga´s Figure-of-Merit (BFOM) related to silicon material

| Parameter | | Silicon (Si) | 4H-SiC | GaN | Diamond |
|---|---|---|---|---|---|
| BFOM | $E_r \cdot E_o \cdot \mu_n \cdot E^3_{Cri}$ | 1 | 500 | 2400 | 9000 |

semiconductor manufacturers take the latter approach due to the high costs involved in SiC semiconductors production. Furthermore, as the thermal management on a 500 times smaller semiconductor die is complicated, semiconductor manufacturers normally design SiC dies to have the same loss density as silicon dies. Thus, in practice, SiC semiconductor dies are designed with an area factor $\sqrt{BFOM} = 22$ smaller than silicon semiconductor dies [140]. Nevertheless, this area reduction already leads to a smaller $R_{ds,on}$ and to a smaller die form factor. A smaller die form factor is positive because it reduces the SiC MOSFET capacitances. In other words, the reduction of the semiconductor die area reduces its parasitic capacitances allowing high-frequency operation and smaller passives on the power converter [147]. In addition, lower conduction and switching losses are beneficial because a smaller cooling system can be used. Finally, the lower intrinsic concentration on SiC makes them more suitable for operation at high temperatures, which helps to reduce the cooling system even further. To summarize, Fig. 3.6 shows how the properties of SiC are translated into advantages in a power converter at the system level.

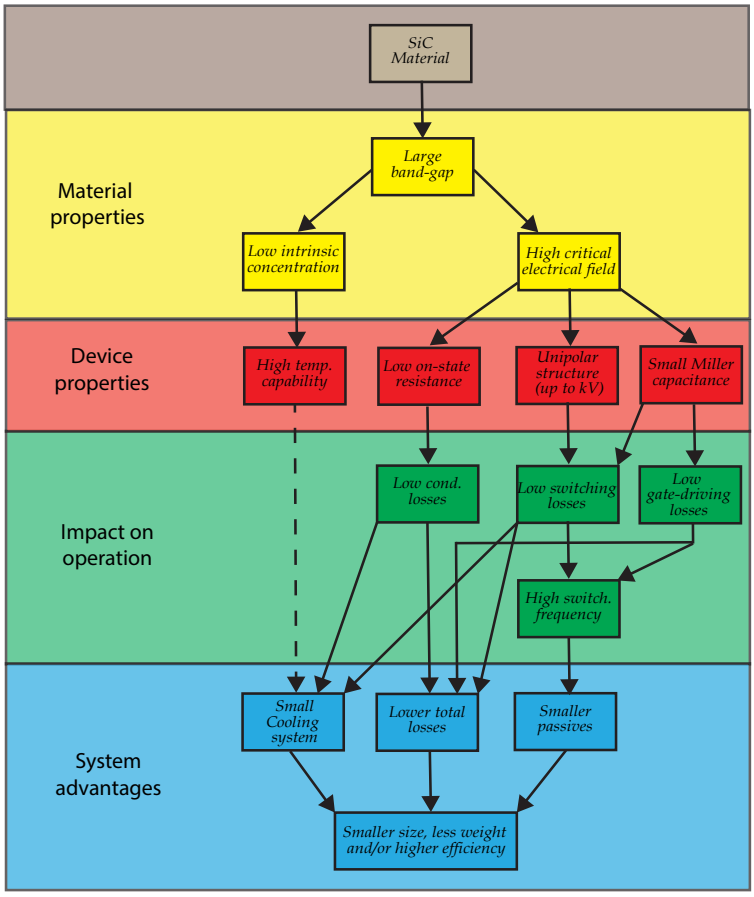


**Fig. 3.6:** Benefits brought by SiC to power converters at the system level. Based on [160]

## 3.4 SILICON CARBIDE SCHOTTKY DIODES

When IGBTs are used as power switches, antiparallel diodes are needed to conduct the current in the reverse direction. In this regard, Fig.3.7 shows the structures of the most commonly used power diodes: the bipolar Si PiN diode and the SiC based SBD. Furthermore, Si based PiN diodes are bipolar devices on which the current flow is formed by electrons and holes due to the PN junction. Therefore, PiN diodes achieve low on-resistances at high voltages due to a high-density electron-hole plasma formed on the drift region during conduction mode [154]. However, on the switching-on to switching-off transition, stored charges need to be extracted from the drift region, which leads to the appearance of a diode reverse recovery current that increases the switching losses [151]. As an illustration, Fig. 3.8 shows the turn-off characteristics of a 650 V bipolar Si PiN diode and a 650 V SiC based SBD. The transition shown in Fig. 3.8 was measured by Heckel in a half-bridge circuit by turn-on of the bottom silicon MOSFET and reported in [161]. Furthermore, the voltage used in the DC-Bus during the measurement is 400 V. Truly, the diode reverse recovery current in a PiN diode becomes larger at higher temperatures which is of course an additional disadvantage [162]. In contrast, SiC based SBD are unipolar devices whose current flow is exclusively due to the flow of electrons or majority carriers. Therefore, no stored charges need to be removed during the switching-on to switching-off transition. In consequence, the on-off transition happens very quickly. Therefore, SiC based SBDs exhibit virtually no reverse recovery current and thus an almost neglectable reverse energy charge $E_{rr}$ as can be seen in Fig. 3.8. Furthermore, and in contrast to Si PiN diodes, this very small reverse energy charge does not change with temperature [162] as can be seen in Fig. 3.8 as well. Although SiC MOSFETs exhibit an inherent body diode that conducts in reverse direction, the forward voltage drop on SiC MOSFET's body diodes is 3 V in contrast to the 0.7 V of silicon MOSFET's body diodes [154]. Due to this undesirable characteristic of SiC MOSFETs, many manufacturers place a SiC based SBD as antipallel diode to bypass the SiC MOSFET's body diode with the objective to reduce the conduction losses when the current reverses.

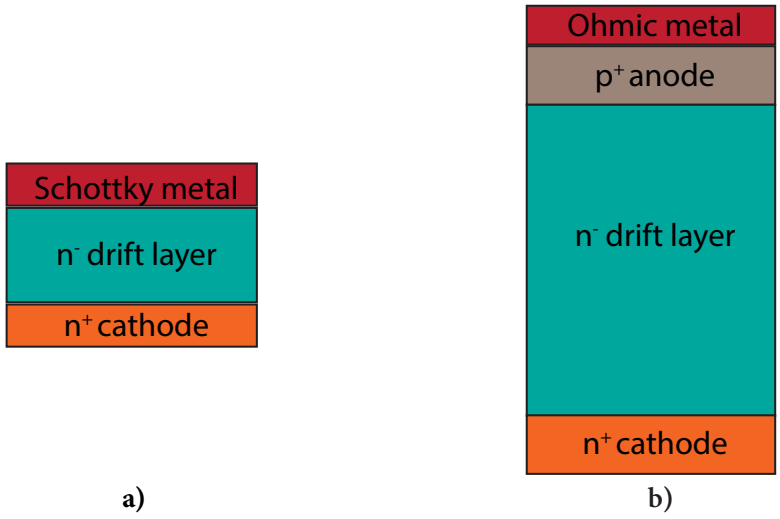


**Fig. 3.7:** PiN Diode and Schottky diode basic structures. **a)** SiC Schottky diode structure. **b)** PiN Si Diode structure. Based on [151]

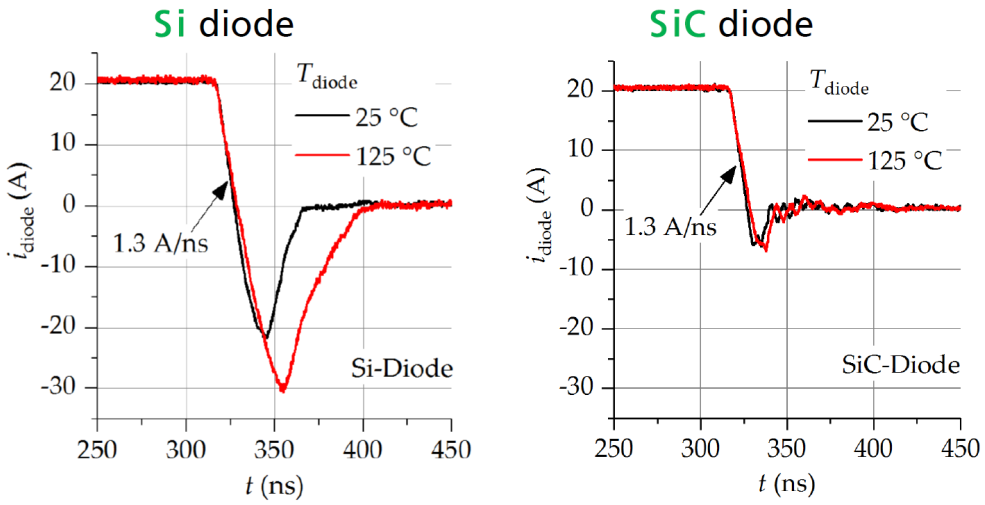


**Fig. 3.8:** Reverse recovery current on silicon PiN Diode and SiC Schottky diode. Extracted from [161]

## 3.5 SILICON CARBIDE MOSFETS AND SILICON IGBTS AT 1200 V - COMPARATIVE EVALUATION

In order to give a concrete example of the advantages of SiC MOSFETs over state-of-the-art silicon IGBT, let me compare two 1200 V half-bridge power modules. The first module SKM300GB12F4 [163] is constructed with Trench Field Stop Si IGBTs optimized with low switching losses and meant for high switching frequency operation (>15 kHz). In addition, the module SKM300GB12F4 uses fast recovery Si diodes as antiparallel diodes. The second module, a CAS300M12BM2 [164] module, consists of planar SiC MOSFETs equipped with SiC SBD antiparallel diodes. Both modules are rated for a continuous current of approximately 300 A and a maximum junction temperature of 150 °C. Furthermore, the key parameters of the Si and SiC modules can be found in Table 3.3 and Table 3.4. From Table 3.3, for a drain current of 300 A and a temperature of 25 °C, it can be seen that the voltage drop over the SiC MOSFET is $V_{DS} = 1.7\,V$. In contrast, for a collector current of 300 A and 25 °C, the entire voltage drop over the Si IGBT is $V_{CE(sat)} = 2.2\,V$. Thus, conduction losses at temperatures below 150 °C are lower using a SiC MOSFET than the Trench IGBT. Nevertheless, the SiC MOSFET and the Si IGBT produce the same voltage drop around 2.6 V, meaning $V_{CE(sat)} = V_{DS} = 2.8\,V$, for a collector/drain current of 300 A at 150 °C. It follows that at high temperatures, in the order of 150 °C, the conduction losses will be comparable. Moreover, if we take a closer look at the semiconductors' parasitic capacitances, the gate to emitter capacitance $C_{GE}$ in the IGBT seems to be comparable to the gate to source $C_{GS}$ capacitance of the SiC MOSFET. However, the Miller capacitance $C_{GD}$ in the SiC MOSFET is ten times smaller than the IGBT's Miller capacitance $C_{GC}$. As the Miller capacitance defines the dv/dt on the semiconductor during the switching transition and influences its input capacitance [151], the SiC MOSFET will exhibit a much faster switching behavior than the IGBT. Certainly, this faster switching behavior can be seen observing the turn-on and turn-off times, where the SiC planar MOSFET is ,on average, two times faster than the IGBT during the turn-on and turn-off transitions. Consequently, the switching energies $E_{on}$ and $E_{off}$ are smaller in the SiC MOSFET than in the Si IGBT as can be verified on

**Table 3.3:** Key parameters: Trench Field Stop silicon IGBT in SKM300GB12F4 module and SiC MOSFET in CAS300M12BM2 module

| Parameter | SKM300GB12F4 | CAS300M17BM2 |
|---|---|---|
| Technology | Trench Field Stop Si IGBT | SiC Planar MOSFET |
| Maximum $V_{CE}/V_{DS}$ | 1200 V | 1200 V |
| DC Continuous current | 300 A | 345 A |
| Maximum Pulse $I_C/I_D$ | 600 A | 1500 A |
| Typical $V_{GE}/V_{GS}$ | +20/-20 V | +20/-5 V |
| Short circuit time | 10 $\mu$s | 3 $\mu$s |
| $V_{CE(sat)}/V_{DS}$ at 300 A for 25 °C/150 °C | 2.06 V/2.6 V | 1.7 V/2.5 V |
| $C_{GE}/C_{GS}$ | 16.7 nF | 19.4 nF |
| $C_{CE}/C_{DS}$ | 0.2 nF | 2.4 nF |
| $C_{GC}/C_{GD}$ | 940 pF | 113 pF |
| Typical Gate Threshold Voltage | 5.8 V | 2.4 V |
| Gate Charge $Q_g$ (-5 V to 20 V) | 1.7 $\mu$C | 1.03 $\mu$C |
| Turn on time at 300 A, 600 V and 150 °C | 170 ns | 80 ns |
| Turn off time at 300 A, 600 V and 150 °C | 469 ns | 175 ns |
| $E_{On}$ at 300 A, 600 V and 150 °C | 16.5 mJ | 3.0 mJ |
| $E_{Off}$ at 300 A, 600 V and 150 °C | 24 mJ | 3.4 mJ |
| Thermal Resistance Junction-Case | 0.11 °C/W | 0.070 °C/W |

**Table 3.4:** Key parameters: Soft freewheeling silicon diode in SKM300GB12F4 module and SiC Schottky Barrier diode in the CAS300M12BM2 module

| Parameter | SKM300GB12F4 | CAS300M17BM2 |
|---|---|---|
| Technology | Soft freewheeling Si diode | SiC Schottky Barrier diode |
| Maximum blocking voltage | 1200 V | 1200 V |
| DC Continuous current | 300 A | 547 A |
| Maximum Pulse $I_F$ | 600 A | 1500 A |
| $V_F$ at 300 A and 150 °C | 2.3 V | 2.1 V |
| $t_r$ at 300 A, 600 V and 150 °C | 45 ns | 27 ns |
| $E_{rr}$ at 300 A, 600 V and 150 °C | 16 mJ | 2.17 mJ |
| Thermal Resistance Junction-Case | 0.17 °C/W | 0.073 °C/W |

Table 3.3. Additionally, as the Miller capacitance in a SiC MOSFET is smaller, a smaller gate charge $Q_g$ is needed to drive the SiC MOSFET in comparison with the gate charge that is needed to drive a Si based IGBT. Hence, the SiC MOSFET will exhibit lower gate driving losses than the Si based IGBT. Last but not least, the thermal resistance is also smaller in the SiC MOSFET than in the Si based IGBT, partly due to the better thermal conductivity of the SiC die. Furthermore, Table 3.4 shows the characteristics of the antiparallel diodes that are built in the modules SKM300GB12F4 and CAS300M12BM2. Although the SiC SBD is more current capable, it exhibits a forward voltage drop of 2.1 V, slightly smaller than the forward voltage drop of the soft Si freewheeling diode in the module SKM300GB12F4. Thus, the conduction losses on the SiC SBD are going to

be just slightly smaller than the conduction losses of the soft Si freewheeling diode of the IGBT. However, the switching characteristics of the SiC SBD are much better than the characteristics of the soft Si freewheeling diode. First, the recovery time $t_r$ is reduced almost by a factor 2 in the SiC SBD. Second, the energy recovery loss is reduced by a factor of 7 if the SiC SBD is used. Finally, the thermal resistance is also smaller on the SiC MOSFET once again due to the better thermal conductivity of the SiC SBD die.

## 3.6 CHAPTER SUMMARY

State-of-the-art SAPFs use classical Si IGBT and PiN diodes semiconductors arranged in a 3L-NPC topology as a power circuit. Although voltages in industrial power grids only reach values between 400 V to 690 V, the 3L topology is used in SAPFs as power circuit to achieve low power losses. However, recently, new semiconductor devices such as SiC MOSFETs and SiC SBD have stepped in. Indeed, SiC material exhibits a band gap three times higher than silicon and almost two times better thermal conductivity. Moreover, as there is a direct correlation between the band gap and the critical field in a semiconductor, a larger band gap in SiC is translated into a critical field ten times higher than silicon. Consequently, the drift layer in SiC based power switches can be thinner compared to Si-based power switches for the same breakdown voltage. It is granted that a thinner drift layer leads to smaller $R_{ds,on}$ resistance. Therefore conduction losses can be made smaller using SiC power switches using simple unipolar power device concepts. Indeed, there is no need to use bipolar devices concepts or conductivity modulation techniques using SiC unless the target is to reach a blocking voltage of 3.3 kV or 4.5 kV. On the other hand, SiC based power switches can be made smaller in area than silicon based power switches, reaching even smaller $R_{ds,on}$ resistances. In other words, although the chip's area of a SiC power switch is smaller than the chip's area of a silicon power switch, the $R_{ds,on}$ resistance of the SiC device reaches smaller values. Consequently, the miller capacitance of a SiC power switch, namely the $C_{GD}$ capacitance, is smaller than the miller capacitance of a silicon power switch. For this reason, SiC power switches exhibit faster switching transitions, and thus lower switching energies than silicon power switches for devices rated at the same blocking voltage. As a result, SiC power switches produce lower switching losses due to the lower switching energies. On account of this, SiC power switches can be used in power converters at higher switching frequencies without producing significant power losses. Furthermore, it is granted that at higher switching frequencies, the passive components on the ripple filter and the coupling inductors can be smaller, maintaining constant the current ripple. As a result, power converter topologies can be simplified from 3L to 2L. Indeed, SiC-based 2L power converters are built with a lower number of semiconductor components than Si-based 3L power converters. Moreover, although SiC-based 2L power converters work with higher switching frequencies than Si-based 3L power converters, SiC-based 2L power converters achieve comparable power losses and even smaller than the power losses produced by Si-based 3L power converters. Subsequently, SAPFs based on SiC-based 2L power converter will produce lower losses and thus higher efficiencies than state-of-the-art SAPFs based on the Si 3L-NPC topology. Then, it can be inferred that using SiC semiconductors, a VSAPF power circuit exhibiting ultra-low losses can be achieved. Accordingly, it can be said that with SiC technology the amount of harmonic active power that can be recovered through VSAPFs will be maximized.

# 4

# Ultra-low losses Active Damper for Harmonic Power Recovery

This chapter summarizes the most relevant findings related to the harmonic active power absorbed by an active damper and the mechanisms of harmonic power recovery. In addition, as the harmonic recovery feature is enabled by an ultra-low losses VSAPF, this chapter also describes the design of an ultra losses VSAPF's power circuit based on SiC MOSFETs. These findings were also published in:

- R. Guzman Iturra, M. Cruse, , K. Muetze , C. Dresel, K. Muetze, P. Thiemann, "Shunt Active Power Filter for Harmonics Mitigation with Harmonics Energy Recycling Function," in *2018 IEEE-PEMC 18th International Conference on Power Electronics and Motion Control (PEMC)*, Budapest, Hungary, August 2018, pp. 938-945.

- R. Guzman Iturra, M. Cruse, K. Muetze, P. Thiemann, C. Dresel, "Power Balance of Shunt Active Power Filter Based on Voltage Detection: a Harmonic Power Recycler Device," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, California, 2019, pp. 1835-1842.

- R. Guzman Iturra, M. Cruse, K. Figge, P. Thiemann and C. Dresel, "Ultra-Low Losses SiC-Based Active Damper for Industrial Power Systems: Mitigating Harmonic Distortion and Maximizing Harmonic Power Recovery," in IEEE Transactions on Energy Conversion, vol. 37, no. 4, pp. 2926-2940, Dec. 2022.

## 4.1 INTRODUCTION

It is already well known that passive resistors draw currents in phase with the supplied voltage in AC circuits. Thus, passive resistors only draw active or real power from an AC circuit. In a straight analogy with passive resistors, the operation of the VSAPF as a virtual harmonic resistor inherently involves the absorption of harmonic active power ($P_H$). The existence of $P_H$ has been acknowledged in [46, 47, 165, 166] and it has to be highlighted that it is a quantity that has a unequivocal physical interpretation. In other words, harmonic active power is not just a "computational quantity" linked to a particular power theory. Rather it is a real physical quantity. Furthermore, $P_H$ is very often disregarded as it is usually small when compared with the active power at the nominal frequency (e.g. $f_1$=50 Hz) referred in the present chapter as $P_1$. Nonetheless,

a previous study [64] about converters behaving as harmonic resistors suggested that the absorbed $P_H$ can be used to compensate for part of the converter losses. Even, Ryckaert et al. in [64] mentioned very roughly that $P_H$ can be converted into $P_1$ if the power converter is considered ideal. However, the mentioned authors made only these qualitative statements and did not perform a profound analysis of the $P_H$ conversion. Therefore, the precise mechanisms of $P_H$ conversion through an active damper or VSAPF constitute a research gap in the field of power electronics. On this basis, this chapter aims to describe mathematically how the transformation of the absorbed $P_H$ into $P_1$ takes place within the VSAPF. In particular, this chapter shows that if VSAPF's power losses are smaller than the $P_H$ intake, the difference between the $P_H$ absorbed and the losses can be converted to $P_1$ and returned to the power grid. In other words, a VSAPF can perform as a harmonic active power recovery device.

## 4.2 ACTIVE DAMPER'S CONTROL LAW

A SAPF driven by the voltage detection strategy or active damper measures only as external signals the voltages at the PCC ($v_{PCC}$). Subsequently, the harmonic components $v_{PCCh}$ are extracted from the signal $v_{PCC}$ through signal-processing techniques (see subsection 2.3). On this basis, the VSAPF's controller generates the reference for the compensating currents $i^*_{Ch}$ according to the following control law [49]:

$$i^*_{\mathrm{Ch}} = \frac{v_{\mathrm{PCCh}}}{R_s} \tag{4.1}$$

where $1/R_s$ is a proportionality factor. Under these conditions the VSAPF is commanded to behave or to emulate a virtual harmonic resistor of $R_S$ ($\Omega$).

## 4.3 ACTIVE DAMPER'S CONTROL SYSTEM

The active damper control system is formed by two outer loops and one inner control loop. To illustrate, Fig. 4.1 shows the active damper's control system, which is fundamentally based on the structure that Akagi proposed in [48]. On the one hand, the inner control loop contains the current controllers that feed the duty cycles to the Pulse Width Modulator (PWM). In fact, assuming that the distribution power three-phase system is balanced, each phase of the VSAPF can be controlled independently [167]. Actually, the duty cycles are calculated so that the currents flowing over the coupling inductors $L$, namely the currents $i_C$, follow closely the references $i^*_C$ dictated by the outer loops. In other words, the current controllers adjust the average voltage at the VSC terminals in such a way that $i_C$ tracks $i^*_C$ considering in the calculation the actual value of the PCC voltages [168]. In any case, the three current controllers used in this chapter are proportional-resonant controllers with delay compensation. Specifically, the resonant controllers are tuned around the typical harmonic frequencies (e.g. 5th,7th,11th,13th,17th, etc.) to ensure a good tracking of the reference currents. In addition, the proportional term in the current controllers takes care of the tracking in the inter-harmonic frequencies range. Moreover, in this chapter, the three current controllers are designed and tuned according to [169]. On the other hand, the outer loops define the compensating currents that will be drawn at the fundamental and harmonic frequencies. In simpler terms, the two outer loops together form the VSAPF's controller. The first outer control loop is the harmonics controller, which defines the reference for the harmonic compensating currents $i^*_{\mathrm{Ch}}$. For this purpose, the harmonics controller extracts the harmonic components of

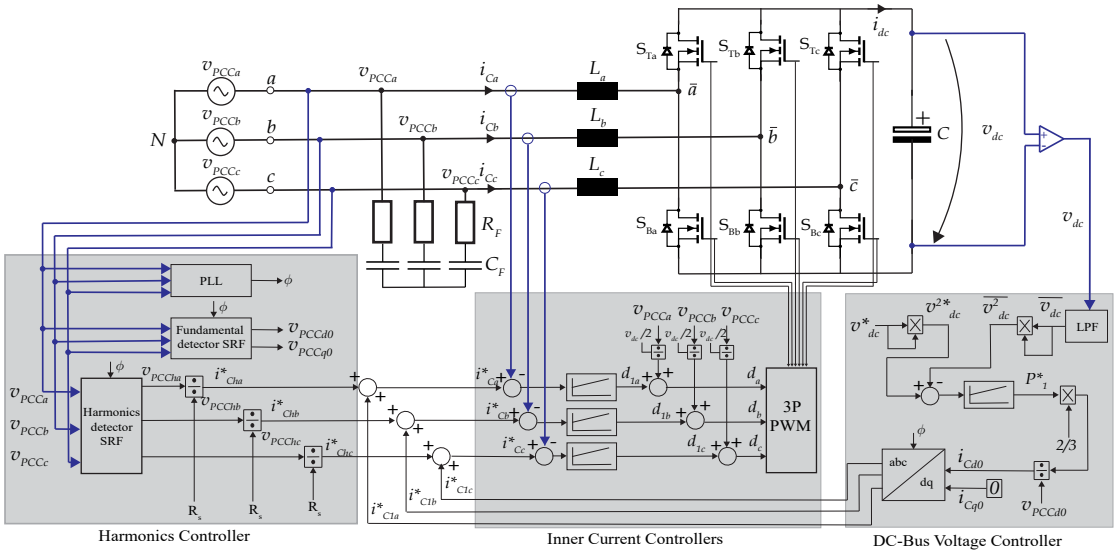


**Fig. 4.1:** Control system of the active damper. Based on [48]

$v_{PCC}$, namely the voltages $v_{PCCh}$, for each phase. Specifically, in this chapter, the harmonics detection process is realized by resorting to the Synchronous Reference Frame (SRF) theory [93]. Afterwards, and as it is stated by the control law defined in (4.1), the value $v_{PCCh}$ is scaled by the factor $1/R_s$. The scaled value of $v_{PCCh}$ for each phase constitutes the first component of the current references. Furthermore, the second outer loop is the DC-Bus voltage controller. The DC-Bus voltage controller indirectly commands the reference for the fundamental component of the compensating currents $i^*_{C1}$. As the VSAPF is meant with a self-supporting DC-Bus, the currents $i^*_{C1}$ are calculated based on the fundamental active power $P_1$ demanded by the DC-Bus voltage controller. The DC-Bus controller sets the amount of $P_1$ that the VSAPF should exchange with the power grid according to the following. If the DC-Bus voltage $v_{DC}$ is below its reference $v^*_{DC}$, the DC-Bus controller absorbs $P_1$ from the grid in order to charge the DC-Bus capacitor. In contrast, if the DC-Bus voltage is above its reference, the DC-Bus controller releases the energy stored on the DC-Bus capacitor injecting $P_1$ into the power system. In any case, the DC-Bus voltage controller used in this research work is designed according to [170]. Finally, the sum of the partial references $i^*_{C1}$ and $i^*_{Ch}$ is passed as overall reference to the inner current controllers.

## 4.4 ANALYSIS OF THE POWER EXCHANGE BETWEEN VSAPF AND THE DISTRIBUTION POWER SYSTEM

In this section, the analysis of the power exchange between VSAPF and the distribution power system is carried out. The study is performed under the assumption that the distribution power system is balanced. The latter can be justified by the fact that VSAPFs are most of the time installed on balanced power systems. Notice that VSAPFs are not used to combat unbalance in distribution power systems [83]. To perform load balancing, measurements of the currents drawn by linear and nonlinear loads are necessary [66]. However, the voltages at the PCC are the only electrical quantities that a VSAPF measures from the power system. It follows that VSAPFs are not equipped with the necessary instrumentation (i.e., current sensors) to combat load-balancing problems. VSAPFs are mainly used to suppress resonances, mitigate harmonic distortion, and provide voltage

support by injecting reactive power. Therefore, it is granted that if the goal is to solve load balancing problems, SAPFs based on the load current detection are the recommended solution [17, 83]. Furthermore, consider a distribution power system that contains nonlinear loads as the one illustrated in Fig. 4.6. In such a distribution system, the voltages at the PCC ($v_{PCC}$) contain components at different frequencies. Naturally, the voltages at the PCC contain a component with a frequency equal to the nominal frequency of the power distribution system, namely $v_{PCC1}(t)$. In addition, and due to the presence of nonlinear loads, the voltages at the PCC also contain components at harmonic frequencies labeled in the following as $v_{PCCh}(t)$. With this in mind, for the incoming mathematical analysis, instantaneous quantities are named with lowercase letters, and RMS or effective quantities are named with capital letters. In addition, $\omega = 2\pi f_1$ is regarded as the nominal frequency or the power system's frequency. It follows that the voltages at the PCC can be mathematically expressed as follows [1]:

$$v_{\mathrm{PCCa}}(t) = v_{\mathrm{PCC1a}}(t) + v_{\mathrm{PCCha}}(t) = \sum_{h=1}^{\infty} \sqrt{2} V_{\mathrm{h}} \sin(h\omega t + \alpha_{\mathrm{h}}) \tag{4.2}$$

$$v_{\mathrm{PCCb}}(t) = v_{\mathrm{PCC1b}}(t) + v_{\mathrm{PCChb}}(t) = \sum_{h=1}^{\infty} \sqrt{2} V_{\mathrm{h}} \sin(h\omega t + \alpha_{\mathrm{h}} - h\frac{2\pi}{3}) \tag{4.3}$$

$$v_{\mathrm{PCCc}}(t) = v_{\mathrm{PCC1c}}(t) + v_{\mathrm{PCChc}}(t) = \sum_{h=1}^{\infty} \sqrt{2} V_{\mathrm{h}} \sin(h\omega t + \alpha_{\mathrm{h}} + h\frac{2\pi}{3}) \tag{4.4}$$

Moreover, the VSAPF injects compensating currents into the grid not only at harmonic frequencies $i_{\mathrm{Ch}}(t)$ but also at the nominal frequency (i.e., fundamental frequency) $i_{\mathrm{C1}}(t)$. Specifically,

$$i_{\mathrm{Ca}}(t) = i_{\mathrm{C1a}}(t) + i_{\mathrm{Cha}}(t) = \sum_{h=1}^{\infty} \sqrt{2}\ I_{\mathrm{h}}\ \sin(h\omega t + \beta_{\mathrm{h}}) \tag{4.5}$$

$$i_{\mathrm{Cb}}(t) = i_{\mathrm{C1b}}(t) + i_{\mathrm{Chb}}(t) = \sum_{h=1}^{\infty} \sqrt{2}\ I_{\mathrm{h}}\ \sin(h\omega t + \beta_{\mathrm{h}} - h\frac{2\pi}{3}) \tag{4.6}$$

$$i_{\mathrm{Cc}}(t) = i_{\mathrm{C1c}}(t) + i_{\mathrm{Chc}}(t) = \sum_{h=1}^{\infty} \sqrt{2}\ I_{\mathrm{h}}\ \sin(h\omega t + \beta_{\mathrm{h}} + h\frac{2\pi}{3}) \tag{4.7}$$

As an active damper should emulate a virtual harmonic resistor, the compensating currents must be in phase with the harmonic voltages at the PCC. It follows that, if the current controller bandwidth is high enough, the following relationship between the angles of $v_{PCC}$ and $i_C$ for $h > 1$ holds:

$$\alpha_{\mathrm{h}} \approx \beta_{\mathrm{h}} \tag{4.8}$$

and the difference between the angles tends to be zero:

$$\theta_{\mathrm{h}} = \alpha_{\mathrm{h}} - \beta_{\mathrm{h}} \approx 0 \tag{4.9}$$

In addition, the active damper´s compensating currents are proportional to the harmonic voltage at the PCC according to (4.1). Thus for $h > 1$, it holds:

$$I_{\mathrm{h}} \approx \frac{V_{\mathrm{h}}}{R_{\mathrm{s}}} \tag{4.10}$$

### 4.4.1 *Harmonic Active Power at the active damper terminals*

Considering (4.2) and (4.5), it is possible to calculate the instantaneous power for one phase of the VSAPF. Specifically, the instantaneous power at the VSAPF's terminal $a$ can be written as [47]:

$$p_a = v_{PCCa} i_{Ca} = (v_{PCC1a} + v_{PCC2a} + v_{PCC3a} + ....)(i_{C1a} + i_{C2a} + i_{C3a} + ....) \tag{4.11}$$

$$p_a = (v_{PCC1a} i_{C1a}) + \sum_{h=2}^{\infty} v_{PCCha} i_{Cha} + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} v_{PCCma} i_{Cna} \; ; with \; m \neq n \tag{4.12}$$

It is granted that the instantaneous power in the other two phases have similar expressions. Moreover, the instantaneous power in (4.31) can be further expressed as the sum of three terms [3]:

$$p_a = p_{1a} + p_{hha} + p_{mna} \tag{4.13}$$

The term $p_{1a}$ is related with power exchange at the nominal frequency between the VSAPF and the grid for the phase $a$. The term $p_{mna}$ contains only cross terms of different frequencies which do not contribute to a net transfer of energy because it involves only oscillating quantities making $p_{mn}$ to have an average value equal to zero. The term $p_{hha}$ contains only terms products of harmonic currents and voltages at the same frequency for phase $a$ [3, 47]:

$$p_{hha} = v_{PCC2a} i_{C2a} + v_{PCC3a} i_{C3a} + v_{PCC4a} i_{C4a} + ... \tag{4.14}$$

In particular, the product of a single harmonic current and a harmonic voltage at the same frequency produces:

$$v_{PCCha} i_{Cha} = P_h - P_h \cos(2h\omega t - 2\alpha_h) - Q_h \sin(2h\omega t - 2\alpha_h) \tag{4.15}$$

With:

$$P_h = V_h I_h \cos(\theta_h) \tag{4.16}$$

$$Q_h = V_h I_h \sin(\theta_h) \tag{4.17}$$

The constant term $P_h$ in (4.15) is the active power of the $h$-order harmonic. On the other hand, the intrinsic harmonic power $P_h \cos(2h\omega t - 2\alpha_h)$ and the harmonic reactive power $Q_h \sin(2h\omega t - 2\alpha_h)$ both also of order $h$ do not contribute to the net transfer of energy and have an average value of zero. Based on (4.16), the harmonic active power absorbed through phase $a$ in (4.12) considering all the harmonic frequencies at once can be expressed as:

$$P_{Ha} = \sum_{h=2}^{\infty} P_h = \sum_{h=2}^{\infty} V_h I_h \cos(\theta_h) \tag{4.18}$$

Likewise, if a similar analysis is carried out for the other two phases, it can be found that the harmonic active power absorbed through phases $b$ and $c$ is equal to:

$$P_{Hb} = P_{Hc} = P_{Ha} = \sum_{h=2}^{\infty} P_h = \sum_{h=2}^{\infty} V_h I_h \cos(\theta_h) \tag{4.19}$$

Equations (4.11) to (4.19) imply that when a VSAPF is connected to the PCC, its operation implies inherently the consumption of harmonic active power. The phenomena can be explained with the help of Fig. 4.2. Specifically, the figure shows an distribution power system that consists of a nonlinear load and a capacitor bank. In fact, nonlinear loads

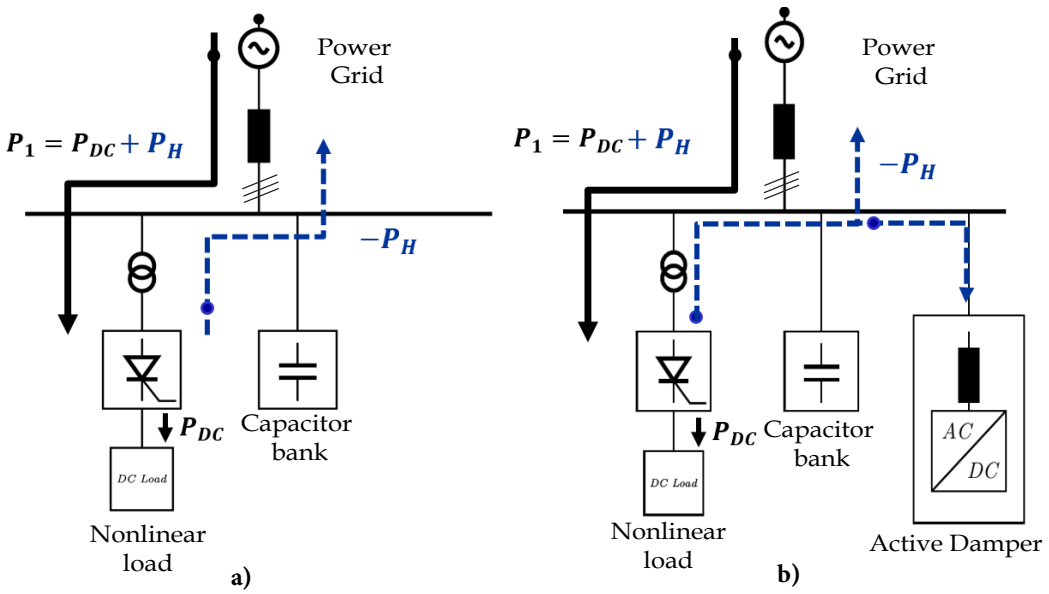


**Fig. 4.2:** Harmonic active power flow on an distribution power system **a)** Distribution power system with nonlinear load and capacitor bank. **b)** Distribution power system with nonlinear load, capacitor bank, and active damper.

absorb a large amount of fundamental power $P_1$ from the utility through the fundamental current drawn by the nonlinear load. A large amount of the absorbed fundamental power $P_1$ is converted by the nonlinear load, for example, to DC power $P_{\mathrm{DC}}$. However, not all the fundamental power absorbed is converted to $P_{\mathrm{DC}}$. Actually, a small part of the fundamental power supplied is injected back into the distribution system again in the form of $P_H$ (see Fig. 4.2 **a)**). The harmonic active power injected by the nonlinear load is injected back at different harmonic frequencies through harmonic currents. If an active damper is connected to PCC, the active damper will absorb part of the harmonic active power that is fed back to the distribution power system by the nonlinear load, as can be seen in Fig. 4.2 **b)**.

### 4.4.2 *Harmonic Active Power Absorbed by the VSAPF*

Three different mathematical expressions can be derived to calculate the amount of harmonic active power absorbed during the operation of the VSAPF. These mathematical expressions are in function of the currents injected by the VSAPF, the emulated resistance $R_{\mathrm{S}}$, and the voltage total harmonic distortion ($THD_V$) at the PCC. In fact, if we assume that the angle $\theta_{\mathrm{h}}$ is sufficiently small for all harmonics frequencies, the active power $P_{\mathrm{h}}$ at each individual frequency expressed by (4.16) can be approximated by:

$$P_{\mathrm{h}} = V_{\mathrm{h}} \cdot I_{\mathrm{h}} \cdot cos(\theta_{\mathrm{h}}) \approx \frac{{V_{\mathrm{h}}}^2}{R_{\mathrm{s}}} \tag{4.20}$$

This assumption implies that the VSAPF draws only active power at each harmonic frequency. Additionally, considering all the harmonics at once and a three-phase symmetrical system, the total amount of harmonic active power that can be absorbed by the VSAPF ($P_H$) can be calculated as:

$$P_{\mathrm{H}} = P_{\mathrm{Ha}} + P_{\mathrm{Hb}} + P_{\mathrm{Hc}} = 3 \cdot \sum_{h=2}^{\infty} P_{\mathrm{h}} \tag{4.21}$$

Recall that the $THD_V$ index is defined as [171]:

$$THD_V = \frac{V_H}{V_1} = \frac{\sqrt{\sum_{h=2}^{\infty} {V_h}^2}}{V_1} \tag{4.22}$$

It follows that the total absorbed harmonic active power $P_H$ can be written in terms of the $THD_V$ at the PCC, the RMS value of the fundamental component $V_1$ and the emulated resistance $R_s$ replacing (4.22) and (4.20) in (4.21) as follows [172]:

$$P_H \approx 3 \cdot \sum_{h=2}^{\infty} \frac{{V_h}^2}{R_s} = 3 \cdot \frac{\sum_{h=2}^{\infty} {V_h}^2}{R_s} = 3 \cdot \frac{(V_1 \cdot THD_V)^2}{R_s} \tag{4.23}$$

Equation (4.23) is the first equation found to predict the amount of $P_H$ absorbed by the VSAPF. On the other hand, (4.21) can be written in function of the currents injected by the VSAPF replacing (4.10) in (4.20) leading to:

$$P_H = 3 \cdot \sum_{h=2}^{\infty} P_h \approx 3 \cdot \sum_{h=2}^{\infty} {I_h}^2 \cdot R_S = 3 \cdot R_S \cdot \sum_{h=2}^{\infty} {I_h}^2 \tag{4.24}$$

Actually, the total RMS value of the compensating currents can be calculated as the sum of the RMS values of all individual components [66]:

$$I_C = \sqrt{{I_1}^2 + {I_H}^2} = \sqrt{{I_1}^2 + \cdot \sum_{h=2}^{\infty} {I_h}^2} \tag{4.25}$$

Typically in VSAPFs, the fundamental compensating current $I_1$ is much smaller than the RMS value of the harmonic components. Arising out of this, the RMS value of the compensating currents can be approximated by:

$$I_C \approx I_H = \sqrt{\sum_{h=2}^{\infty} {I_h}^2} \tag{4.26}$$

Replacing (4.26) in (4.24), leads to the second mathematical expression that can be used to calculate the amount of $P_H$ that is absorbed by the VSAPF:

$$P_H \approx 3 \cdot R_S \cdot {I_C}^2 \tag{4.27}$$

Finally, a third mathematical expression to calculate the amount of absorbed harmonic active power was derived by Cruse in [95]:

$$P_H \approx 3 \cdot (V_1 \cdot THD_V) \cdot I_C \tag{4.28}$$

All in all, either (4.23), or (4.27), or (4.28) can be used to estimate the amount of harmonic active power drawn during the VSAPF's operation.

### 4.4.3 *Power Balance Equation of the VSAPF*

In order to demonstrate how the VSAPF performs the transformation of $P_H$ into $P_1$, it is necessary to investigate the interaction between the active damper and the power system from a power exchange point of view. On this basis, the energy exchange

interaction between the VSAPF and the grid can be mathematically described starting from the basic physics law of conservation of energy, the energy stored in capacitors and inductors, and the working principles of the active damper. In order to illustrate the mathematical description, let me to take a simplified version of Fig. 4.1 as in Fig. 4.3. On the simplified circuit, the ripple filter is not considered because the ripple filter plays a role only at multiples of the VSAPF's switching frequency. Thus, for frequencies below 2 kHz where the harmonic active power is significant, Fig. 4.3 shows a reasonably accurate representation of the power exchange between the VSAPF and the power grid. Furthermore, the simplified circuit includes the resistors $R_a, R_b, R_c$ in series with each coupling inductor that serve to model the inherent resistance of the inductor's windings and inductor's core losses. Furthermore, and based on Fig. 4.3, we denominate $p_c(t)$ to the DC-bus capacitor instantaneous power, $P_{LossVSC}$ to the total power losses in the VSC (conduction and switching losses) and $p_{ac}(t)$ to the instantaneous power at the VSC AC-side terminals. Certainly, the law of conservation of energy states that the energy's rate of change on the VSC AC-side terminals should match the energy's rate of change on the VSC's DC-side minus the VSC's power losses. In simple terms, the so-called power balance equation of a power converter [170, 173, 174], for the particular case of the VSAPF can be formulated as:

$$p_c(t) = \frac{d}{dt}\left(\frac{C}{2}v^2_{DC}(t)\right) = p_{ac}(t) - P_{LossVSC} \tag{4.29}$$

The instantaneous power at the VSC AC-side terminal (see Fig. 4.3) can be expressed as:

$$\begin{aligned} p_{ac}(t) \quad &= v_{PCCa}(t)i_{Ca}(t) + v_{PCCb}(t)i_{Cb}(t) + v_{PCCc}(t)i_{Cc}(t) - \\ &- R_a i^2_{Ca}(t) - R_b i^2_{Cb}(t) - R_c i^2_{Cc}(t) - \\ &- \frac{d}{dt}\left(\frac{L_a}{2}i^2_{Ca}(t)\right) - \frac{d}{dt}\left(\frac{L_b}{2}i^2_{Cb}(t)\right) - \frac{d}{dt}\left(\frac{L_c}{2}i^2_{Cc}(t)\right) \end{aligned} \tag{4.30}$$

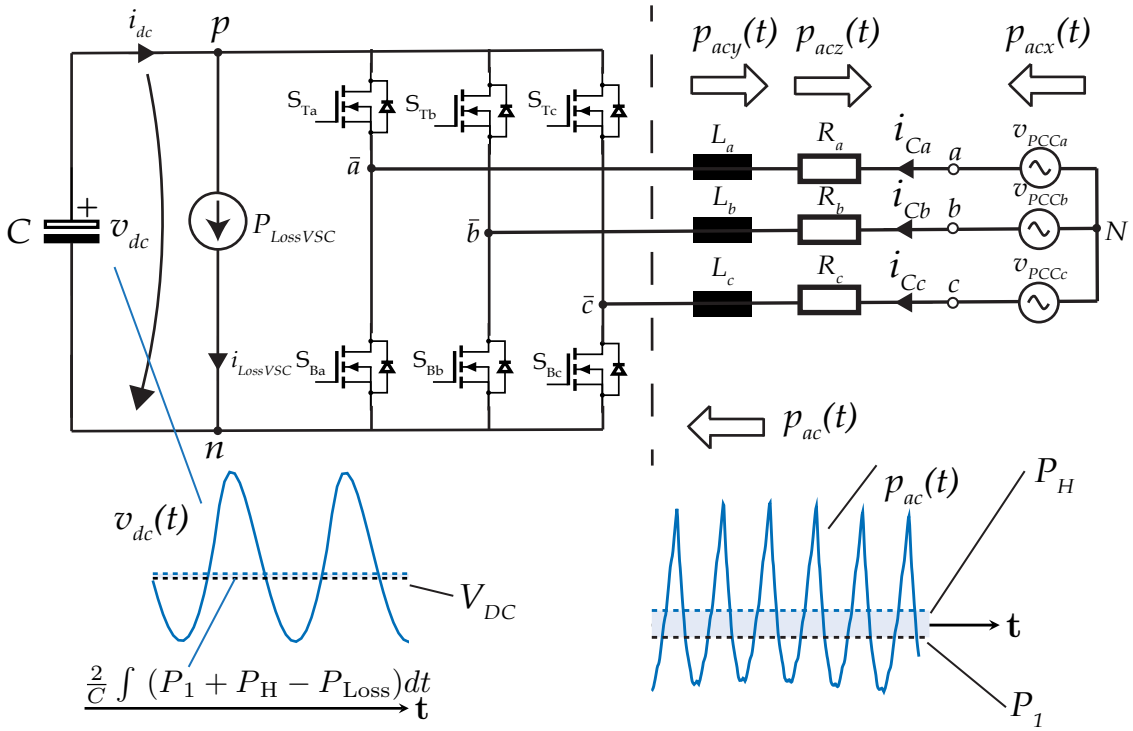


**Fig. 4.3:** Harmonic active power processing through VSAPF. Illustration of the VSAPF power balance equation.

Furthermore, and to maintain the incoming mathematical expressions simple, $p_{ac}(t)$ is further written as:

$$p_{ac}(t) = p_{acx}(t) - p_{acy}(t) - p_{acz}(t) \tag{4.31}$$

where $p_{acx}(t)$ is the instantaneous power supplied to the VSAPF, $p_{acy}(t)$ is the instantaneous power taken by the resistors $R_a, R_b, R_c$ and $p_{acz}(t)$ is the instantaneous power taken by coupling inductors (see Fig. 4.3). In other words:

$$p_{acx}(t) = v_{PCCa}(t)i_{Ca}(t) + v_{PCCb}(t)i_{Cb}(t) + v_{PCCc}(t)i_{Cc}(t) \tag{4.32}$$

$$p_{acy}(t) = R_a i^2_{Ca}(t) + R_b i^2_{Cb}(t) + R_c i^2_{Cc}(t) \tag{4.33}$$

$$p_{acz}(t) = \frac{d}{dt}\left(\frac{L_a}{2} i^2_{Ca}(t)\right) + \frac{d}{dt}\left(\frac{L_b}{2} i^2_{Cb}(t)\right) + \frac{d}{dt}\left(\frac{L_c}{2} i^2_{Cc}(t)\right) \tag{4.34}$$

Truly the typical case is that $R_a = R_b = R_c = R_i$ and $L_a = L_b = L_c = L_i$. Moreover, inspecting (4.2) to (4.7), it can be concluded that $p_{ac}(t)$, as expressed in (4.30), contains cross product terms of the form $V_m \cdot I_n$ and $I_p \cdot I_q$ for each phase that involve components at different frequencies ($m$,$n$,$p$,$q$). However, in a balanced three-phase circuit, the combinations that produce $(m+n)$, $(m-n)$,$(p+q)$ or $(p-q)$ expressions that are not multiples of three, sum to zero. Hence, just considering pairs $(m,n)$ and $(p,q)$ such that:

$$(m+n) = 3k_1, (p-q) = 3k_2 \mid k_1,\ k_2\ \in\ \mathbb{Z} \tag{4.35}$$

(4.32) to (4.34) can be expressed as in (4.36) to (4.38):

$$\begin{aligned} p_{acx}(t) \quad &= 3V_1 I_1 \cos(\theta_1) + 3\sum_{h=2}^{\infty} V_h I_h \cos(\theta_h) - \\ &-3\sum_{m=2}^{\infty}\sum_{n=2}^{\infty} V_m I_n \cos[(m+n)\omega t + (\alpha_m + \beta_n)] + \\ &+3\sum_{p=2}^{\infty}\sum_{q=2}^{\infty} V_p I_q \cos[(p-q)\omega t + (\alpha_p - \beta_q)] \end{aligned} \tag{4.36}$$

$$\begin{aligned} p_{acy}(t) \quad &= 3R_i\sum_{h=1}^{\infty} I^2_h - 6R_i\sum_{m=2}^{\infty}\sum_{n=2}^{\infty} I_m I_n \cos[(m+n)\omega t + (\beta_m + \beta_n)] + \\ &+6R_i\sum_{p=2}^{\infty}\sum_{q=2}^{\infty} I_p I_q \cos[(p-q)\omega t + (\beta_p - \beta_q)] \end{aligned} \tag{4.37}$$

$$\begin{aligned} p_{acz}(t) \quad &= -3L_i\sum_{m=2}^{\infty}\sum_{n=2}^{\infty}\{I_m I_n \cos[(m+n)\omega t + (\beta_m + \beta_n)](m+n)\omega\} + \\ &+3L_i\sum_{p=2}^{\infty}\sum_{q=2}^{\infty}\{I_p I_q \cos[(p-q)\omega t + (\beta_p - \beta_q)](p-q)\omega\} \end{aligned} \tag{4.38}$$

Furthermore, in a conventional balanced three-phase three-wire system with nonlinear loads connected, the harmonic frequencies encounter in the power system are typically within the range $m,n,p,q \in [1,5,7,11,13,...]$. As a consequence, only expressions $(m+n)$,$(m-n)$,$(p+q)$, $(p-q)\ \in\ [6,12,18,24,...]$ remain in equations (4.36) to (4.38). Furthermore in (4.36), the term:

$$P_1 = 3V_1 I_1 \cos(\theta_1) \tag{4.39}$$

is the power exchanged at the nominal frequency between the VSAPF and the grid. Moreover,

$$P_{\mathrm{H}} = 3\sum_{h=2}^{\infty} P_{\mathrm{h}} = 3\sum_{h=2}^{\infty} V_{\mathrm{h}} I_{\mathrm{h}} \cos(\theta_{\mathrm{h}}) \tag{4.40}$$

is the total absorbed harmonic active power by the VSAPF. Moreover, in (4.37), the following term:

$$P_{\mathrm{LossRi}} = 3R_{\mathrm{i}} \sum_{h=1}^{\infty} I^2{}_{\mathrm{h}} \tag{4.41}$$

represents the overall losses in the inductors $L_i$ which for this analysis include core and winding losses. The VSAPF's total losses ($P_{\mathrm{Loss}}$) comprise theVSC's power losses ($P_{\mathrm{LossVSC}}$) and the power losses on the coupling inductors $P_{\mathrm{LossRi}}$. Specifically:

$$P_{\mathrm{Loss}} = P_{LossVSC} + P_{LossRi}. \tag{4.42}$$

### 4.4.4 *DC-Bus Capacitor Voltage*

The capacitor voltage expression can be obtained integrating both sides of (4.29). This yields:

$$\frac{C}{2} v^2{}_{\mathrm{dc}}(t) = \int \Big( p_{\mathrm{ac}}(t) - P_{\mathrm{LossVSC}} \Big) dt \tag{4.43}$$

$$v_{\mathrm{dc}}(t) = \sqrt{\frac{2}{C}\int p_{\mathrm{ac}}(t)dt - \frac{2}{C}\int P_{\mathrm{LossVSC}} dt} \tag{4.44}$$

For an operating point in steady state, the overall VSAPF's losses $P_{Loss}$, the absorbed harmonic active power $P_H$ and the fundamental active power $P_1$, are all constant. By observing the oscillatory terms in (4.36) to (4.38), it is clear that terms pulsating at multiples of six times the nominal frequency are involved in $p_{\mathrm{ac}}(t)$ (see Fig. 4.3). Therefore, terms pulsating at multiples of six times the nominal frequency will be involved also in (4.44) as can be seen in Fig. 4.3. In consequence, it is possible to express the DC-Bus voltage as constant term $\overline{v_{\mathrm{DC}}}$ plus an oscillatory term $\widetilde{v_{\mathrm{DC}}}$ around it. Hence:

$$v_{\mathrm{dc}}(t) = \sqrt{\overline{v_{\mathrm{DC}}} + \widetilde{v_{\mathrm{DC}}}} \tag{4.45}$$

Where:

$$\overline{v_{\mathrm{dc}}} = \frac{2}{C}\int (P_1 + P_{\mathrm{H}} - P_{\mathrm{Loss}}) dt \tag{4.46}$$

$$\widetilde{v_{\mathrm{dc}}} = \frac{2}{C}\int (p_{\mathrm{ac}}(t) - P_1 - P_{\mathrm{H}} + 2P_{\mathrm{LossRi}}) dt \tag{4.47}$$

Similar to the approach taken in [174], equation (4.45) can be well approximated by the first two terms of its Taylor Series expansion around a particular operating point. In other words, (4.45) can be linearized around an operating point with DC value $V_{\mathrm{DC}}$ as follows:

$$v_{\mathrm{dc}}(t) = (V_{\mathrm{DC}} + \overline{v_{\mathrm{DC}}}) + \frac{1}{2V_{\mathrm{DC}}}\widetilde{v_{\mathrm{DC}}} \tag{4.48}$$

$$v_{\mathrm{dc}}(t) = V_{\mathrm{DC}} + \frac{2}{C}\int (P_1 + P_{\mathrm{H}} - P_{\mathrm{Loss}}) dt + \frac{1}{2V_{\mathrm{DC}}}\widetilde{v_{\mathrm{DC}}} \tag{4.49}$$

Equation (4.49) relates the DC-bus voltage to the harmonic active power absorbed, the active power exchanged between the VSAPF and the power system at the fundamental/nominal frequency, and the overall VSAPF's losses.

### 4.4.5 *Harmonics Active Power Conversion*

To understand how the conversion of $P_H$ to $P_1$ takes place, we need to observe the VSAPF's control system depicted in Fig. 4.1. It is granted that the DC-Bus controller is relatively slow due to the fact that as an outer loop, the DC-Bus controller needs to be ten times slower than the inner current control [170]. For this reason, the DC-Bus controller is meant only to regulate the average DC-Bus voltage $V_{DC} + \overline{v_{dc}}$. As a consequence, the DC-Bus controller will not react to high frequency components due to reactive or distortion powers in the VSC AC-terminals. Furthermore, the DC-Bus voltage controller output is the reference for the fundamental component of the compensating currents $i_{C1}$. Indeed, depending if the DC-Bus voltage is below or above its reference, the DC-Bus controller sets the three-phase currents $i_{C1}$ indirectly in order to absorb/release $P_1$ from/to the power system. From (4.49), it can be inferred that if $P_H$ is higher than $P_{Loss}$, the DC-Bus controller needs to command $P_1$ with a negative sign leading to the VSAPF releasing fundamental power to the grid. The latter is done to ensure the system's power balance and the equilibrium of the $v_{DC}(t)$ voltage. Otherwise, the DC-bus voltage term $\overline{v_{dc}}$ and therefore $v_{DC}(t)$ will increase monotonically since the integral of a positive constant is a ramp. The latter can be seen in Fig. 4.4 that shows the computer simulation results of an ultra-low losses VSAPF that does not exchange $P_1$ with the power system. Furthermore, another fact that highlight the correctness of the mathematical modelling carried out in this chapter is the expression $\widetilde{v_{dc}}$. As was explained in subsection 4.4.3, $\widetilde{v_{dc}}$ in (4.49) contains only oscillatory terms related with $p_{ac}(t)$ at frequencies $[6 \cdot 50Hz, 12 \cdot 50Hz, 18 \cdot 50Hz, ...]$. The latter can be confirmed by observing the Fast Fourier Transform (FFT) results performed over the simulated $v_{dc}(t)$ of the ultra-low losses VSAPF. Actually, the FFT of the simulated $v_{dc}(t)$ can be also seen in Fig. 4.4 below the signal $v_{dc}(t)$. In addition, equation (4.49) can be interpreted in the following manner: as the VSAPF behaves as a virtual harmonic resistor, it absorbs a

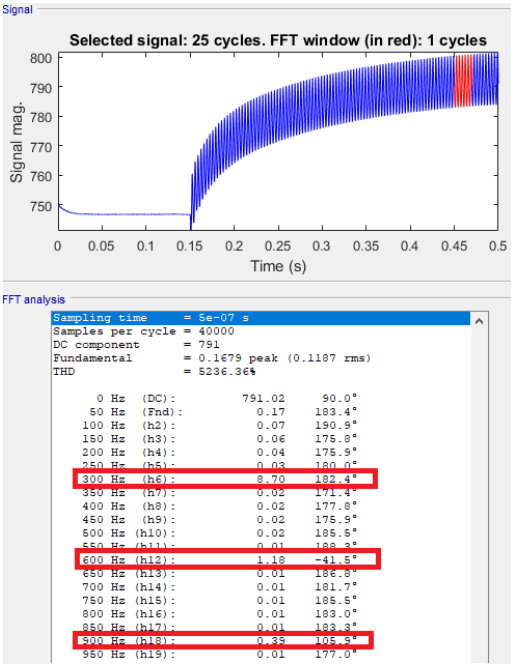


**Fig. 4.4:** Ultra-low lossless VSAPF's DC-bus voltage without P1 release (P1 = 0 W). Actually, the VSAPF harmonic resistance emulation is activated at $t = 0.15\ s$.

certain amount of harmonic active power. If the VSAPF's power losses are smaller than the harmonic active power intake, this power's difference over time will be stored as energy in the DC-bus capacitor. This is because the VSAPF itself is a non-dissipative circuit. It follows that the stored energy in the DC-bus capacitor can be transformed into fundamental active power and returned to the power system. In other words, it means a VSAPF acting as a harmonic power recovery device. In effect, the explained harmonic power recovery concept is protected under the European patent EP3118961 [175]. Although Wu et al. in [63] provided somehow a similar qualitative description of the harmonic power recovery concept as explained in this section, the description was backed neither by mathematical equations nor by simulation results. In addition Wu et al. always considered an ideal and loss-less active damper in their discussion and thus they did not introduce the necessary conditions for harmonic power recovery. Indeed, the theoretical implication of (4.49) is that the harmonic energy recovery process occurs through the DC-Bus voltage regulation, and it is only possible if the active damper's power losses are smaller than the harmonic active power intake (necessary condition). If $P_H < P_{\text{Loss}}$, harmonic power recovery is not possible, and the DC-Bus voltage controller draws fundamental power from the mains. In this latter case, the VSAPF acts as a load at the nominal frequency from the power grid perspective. Therefore, it can be inferred that the sole presence of a DC-Bus controller in an active damper power circuit does not ensure harmonic power recovery; the DC-Bus controller must be accompanied by an active damper with power losses smaller than the harmonic power intake if harmonic power recovery is to be performed. In the past, VSAPFs built with silicon semiconductors were just too lossy, leading to VSAPF power losses larger or equal than the harmonic active power absorbed. Thus, in practice, harmonic active power recovery was hardly possible. However, nowadays, WBG semiconductors technologies such as silicon carbide (SiC) and nanocrystalline material give the means to construct active dampers with ultra-low losses [144, 176].

## 4.5 ULTRA-LOW LOSSES SIC BASED ACTIVE DAMPER

The active damper power circuit displayed in Fig. 4.1 is physically built with 62mm power modules rated for 1.2 kV that contain 9.5 mΩ SiC MOSFETs and SBD. Specifically, three SEMIKRON SiC modules SKM350MB120SCH17 [177] are used to construct the three legs of the two-level power circuit for the active damper. As an illustration, the active damper prototype constructed in conjunction with the partner company of this project, namely Condensator Dominit, can be seen in Fig. 4.5 **a)**. Furthermore, SKYPER 42LJR drivers are used to command the three half-bridges that form the converter legs. Additionally, the cooling system is formed by the heatsink P16-200-16B and the cooling fan SKF 16A-230-01 also from the company SEMIKRON. Moreover, the VSAPF's coupling inductors are built with nanocrystalline material (SU114b), with bobbins 2x UI114B, and with high-frequency Litz wire with a total conduction area of 50 mm². Actually, a picture of the utilized coupling inductor can be seen in Fig. 4.5 **b)**. Moreover, each coupling inductor has nominal values $R_i$ = 2.1 mΩ (DC resistance at 20°C) and nominal inductance $L_i$ = 100 $\mu$H.

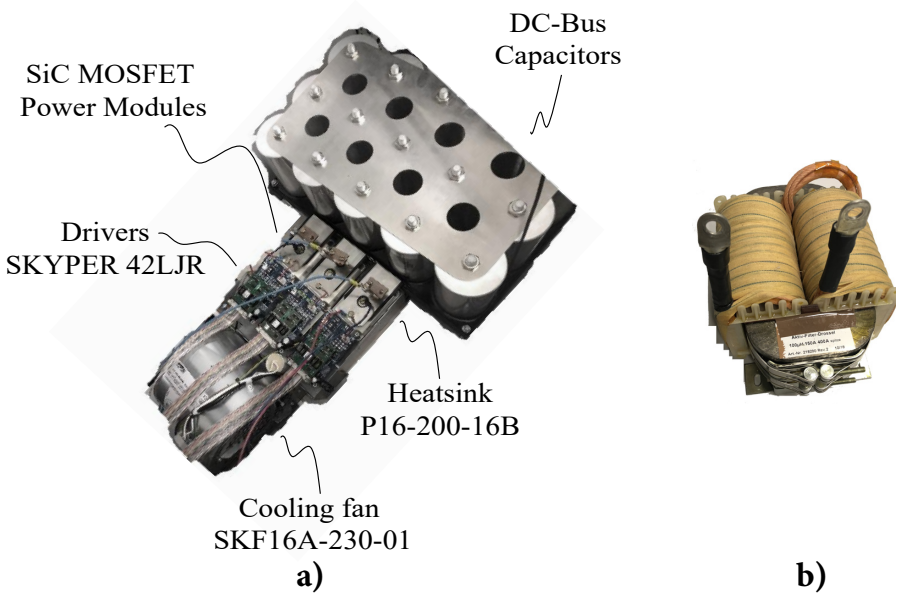


**Fig. 4.5:** Two-level SiC VSC power circuit of the active damper. **a)** Power circuit built with 9.5 mΩ SiC MOSFETs with antiparallel SiC Barrier Schottky diodes as power switches **b)** Coupling inductor of 100 $\mu$H built with nanocrystalline material and Litz-wire.

## 4.6 HARMONICS ACTIVE POWER RECOVERY

### 4.6.1 *Simulation Validation*

First, computer simulations were conducted to evaluate the harmonic active power recovery through an ultra-low losses active damper. In particular, Simulink and PLECS are used as software platforms upon which the active damper and the power system depicted in Fig. 4.6 are simulated. On the one hand, the control system depicted in Fig. 4.1 was implemented in Simulink. On the other hand, PLECS was chosen as software tool for the power circuit and thermal behavior simulation of the SiC based power circuit shown in Fig. 4.5.

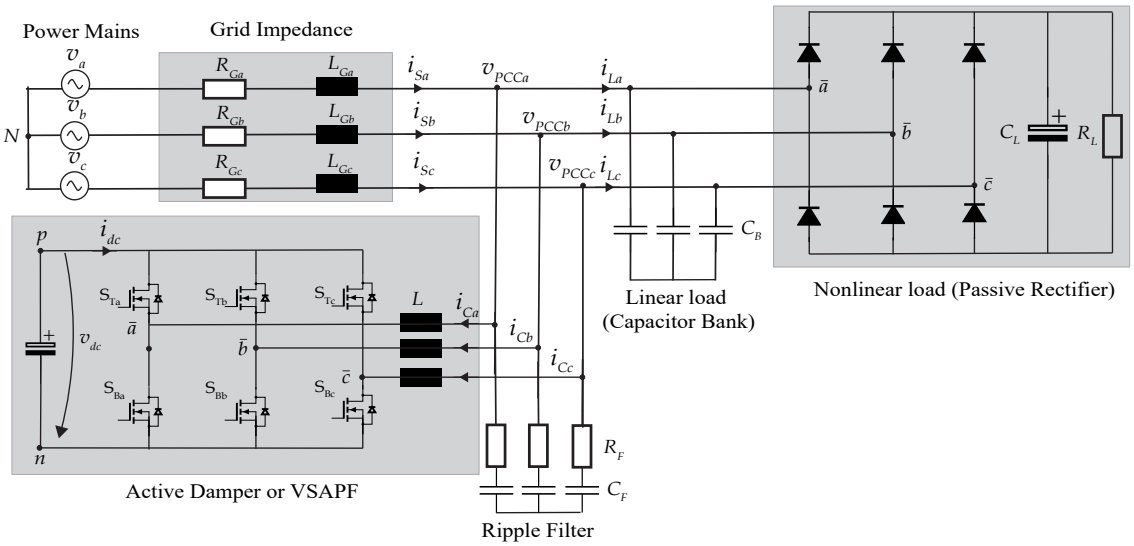


**Fig. 4.6:** Simulation Scenario - Active damper connected to a distribution power system that contains a capacitor bank $C_B$ and a passive diode rectifier as nonlinear load.

Certainly, the most important feature of PLECS is that it allows us to obtain accurate estimations of semiconductor losses using only a simulation environment. In detail, PLECS uses the datasheet information of the semiconductors, the power circuit states, the currents flowing over semiconductors, and the blocked voltages across the power switches to perform losses calculations. In addition, the power loss dependency of the temperature on the semiconductors can also be taken into account within PLECS. To this end, the entire thermal network from the junction to the ambient was implemented in PLECS according to the thermal impedance characteristics of the heatsink P16-200-16B with the fan SKF 16A-230-01. With all these features in mind, it is possible to infer that a highly accurate estimation of the power losses produced by the power circuit can be obtained in PLECS. Last but not least, PLECS also allows to simulate unique characteristics that belong to SiC power switches, such as the third quadrant characteristic of the SiC MOSFETs. Indeed, the scenario simulated is defined by the parameters written in Table 4.1.

**Table 4.1:** Simulation Parameters

| Description | Value |
|---|---|
| Power System | 400V (L-L),50 Hz<br>5th Background distortion 2% (250 Hz)<br>7th Background distortion 2% (350 Hz) |
| Medium Voltage<br>(MV) Grid | 150 MVA,<br>X/R = 3 |
| Power Transformer | 1 MVA,<br>Impedance 5%,<br>X/R = 20 |
| Nonlinear Load | 288 kW<br>(DC Side constant load) |
| Coupling Inductors<br>(DC Res. at 20°C) calc. | $L$ = 100 $\mu$H ,<br>$R$ = 2.1 m$\Omega$, |
| Ripple filter | $C_F$ = 250$\mu$F,<br>$R_F$ = 45m$\Omega$ |
| Switching Frequency<br>Sampling Frequency | 20 kHz<br>40 kHz |
| DC-Bus Voltage | 750 V |
| DC-Bus Capacitor | 10 mF |
| Capacitor Bank | $C_B = 150\mu F$ |

Additionally, the active damper is set to mimic a harmonic resistance of $R_s = 80\ m\Omega$ at $t$ = 0.25 s. Beforehand, the active damper is deactivated in order to benchmark the initial condition of the power system. Moreover, the behavior of the grid voltages at the PCC can be seen in Fig. 4.7. Likewise, the compensating currents performed by the active damper can be seen in Fig. 4.8. The $THD_V$ without active damper is 8.21 %. Such high voltage distortion arises from the interaction between the capacitance in the system ($C_B + C_F$) and the grid inductance $L_G$ that produce a resonance around 1.43 kHz. The latter is excited by harmonics currents drawn by the nonlinear load. Moreover, when the active damper is activated at $t$=0.25 s, the active damper injects compensating currents with an RMS value of 155.49 A per phase amid the emulation of the harmonic resistor $R_s$.

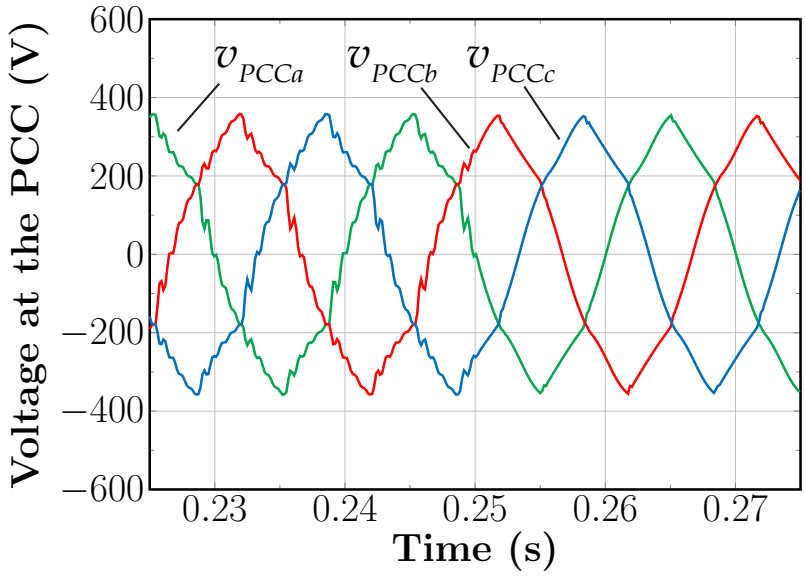


**Fig. 4.7:** VPCC line-to-neutral voltages. The VSAPF is activated at $t$=0.25 s. The $THD_V$ without VSAPF is 8.21 % . When the VSAPF is activated the $THD_V$ is reduced to 5.3 %.

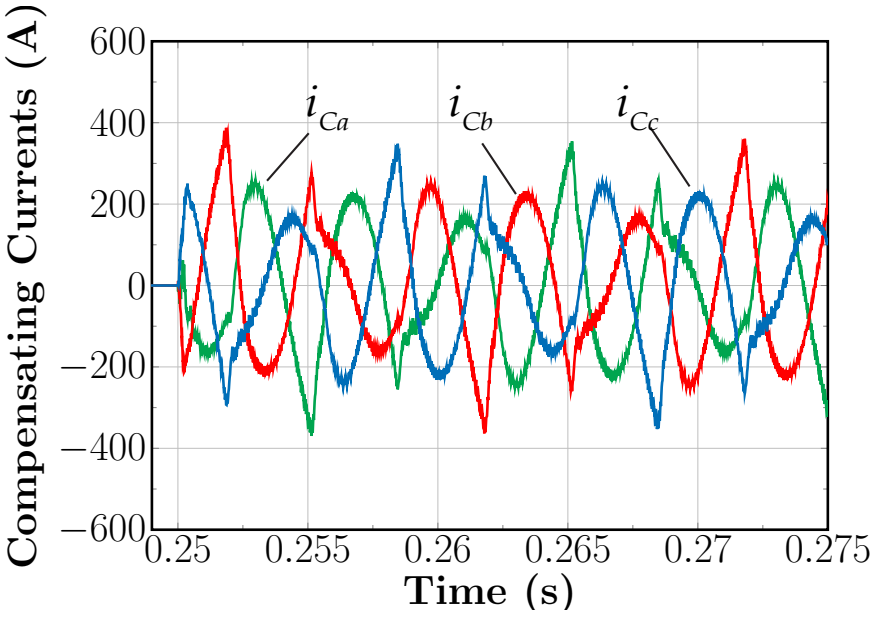


**Fig. 4.8:** VSAPF compensating currents $I_C$. The VSAPF is activated at $t$=0.25 s. The RMS current of the compensating currents is measured as 155.49 A. Moreover, the maximum ripple measured is 40 A peak to peak.

Indeed the active damper suppresses the resonance created by $(C_B + C_F)$ and the grid inductance $L_G$ and mitigates the background harmonic distortion. Thereby, the active damper decreases the $THD_V$ from 8.21% to 5.35% in compliance with the standard IEC 61000-2-4 compatibility class 2. In addition, the VSAPF provides an alternative to the distribution system impedance for harmonic currents produced by the nonlinear load. Hence, the VSAPF deflects a large amount of the load harmonic currents and decreases the harmonic voltage drop over the grid impedance. Also, the harmonic active power absorbed by the active damper can be calculated according to (4.23):

$$P_H \approx 3 \cdot \frac{(V_1 \cdot THD_V)^2}{R_s} = 3 \cdot \frac{(229.71\ \text{V} \cdot 0.0535)^2}{80\ \text{m}\Omega} = 5.63\ \text{kW} \tag{4.50}$$

or resorting to (4.27):

$$P_{\mathrm{H}} \approx 3 \cdot R_{\mathrm{S}} \cdot {I_{\mathrm{C}}}^2 = 3 \cdot 80\ \mathrm{m\Omega} \cdot (155.49\ \mathrm{A})^2 = 5.79\ \mathrm{kW} \tag{4.51}$$

and of course can be estimated using (4.28) as well:

$$P_{\mathrm{H}} \approx 3 \cdot (V_1 \cdot THD_{\mathrm{V}}) \cdot I_{\mathrm{C}} = 3 \cdot (229.71\ \mathrm{V} \cdot 0.0535) \cdot (155.49\ \mathrm{A}) = 5.72\ \mathrm{kW} \tag{4.52}$$

Furthermore in order to confirm these theoretical estimations made for the harmonic active power absorbed by the active damper, an FFT analysis is performed over the $v_{PCCa}$ voltage and $i_{Ca}$ current. The time window chosen for evaluating these two signals is 40 ms. Indeed, the magnitudes and phase difference between $v_{PCCa}$ and $i_{Ca}$ for harmonic frequencies of interest were measured and the results written in Table 4.2. From the table, it is possible to conclude that the VSAPF behaves as a virtual resistor of 80 $m\Omega$ at harmonic frequencies. Evidence of such a fact are the values $R_s \approx 80m\Omega$ and the small phase angle difference $\theta_h < 30^\circ$ reached at the harmonic frequencies 5th, 7th, 11th,and 13th.

**Table 4.2:** VSAPF performance as virtual harmonic resistance (Phase a).

| h | $VPCC_h$(V) | $I_{Ch}$(A) | $R_s(m\Omega)$ | $\theta_h(^\circ)$ | $3P_h(W)$ |
|---|---|---|---|---|---|
| 1 | 229.71 | 7.13 | 32212.7 | -179.21 | -4913.59 |
| 5 | 11.56 | 145.63 | 79.4 | 1.46 | 5050.50 |
| 7 | 3.43 | 45.78 | 75.1 | 7.18 | 468 |
| 11 | 0.83 | 11.64 | 71 | 32.59 | 24.51 |
| 13 | 1.37 | 20.1 | 69 | 24.13 | 75.64 |
| 2..∞ | | | | | 5644.387 |
| 1..∞ | 230.1 | 155.49 | | | |

Moreover, recall that PLECS uses ideal switches as power switches; therefore, the power circuit simulation is almost lossless. Actually, the only losses on the simulation's power circuit are the losses due to the resistance of the coupling inductors. Because, the semiconductors' switching and conduction losses are calculated just apart in the PLECS environment. In consequence, in the FFT analysis carried out in Table 4.2, almost the complete harmonic power intake $P_{\mathrm{H}} \approx$ 5.6 $kW$ (close to the value calculated on (4.50),(4.51) and (4.52)) is released as fundamental active power $P_1 \approx -4.9\ kW$. On the other hand, the overall VSAPF 's power losses were estimated using electrical and thermal models implemented in PLECS and GeckoMagnetics. The semiconductor electrical models are based on the SiC modules datasheet information and implemented in PLECS. Besides the thermal impedance of the SiC modules, and heatsink with cooling system were included in the semiconductor losses estimation assuming an ambient temperature of 40 °C. In this regard, Table 4.3 summarizes the overall losses for this specific operating point. For the calculation of the losses in the ripple filter damping resistors $R_{\mathrm{F}}$, the current passing through them was measured, and an RMS value of $I_{\mathrm{RF}} = 32.01\ A$ per phase was obtained. Thus, the losses in the resistors $R_{\mathrm{F}}$ are simply calculated as ${I^2}_{\mathrm{RF}} R_{\mathrm{F}}$. From Table 4.3, the VSAPF´s total losses for this particular operating point reach the value of $P_{Loss} = 1.16\ kW$. For the operation point simulated, it can be seen that $P_H = 5.6\ kW$ is larger than $P_{Loss}$ as it is graphically depicted in Fig. 4.9. It follows that in reality, the difference between the $P_{\mathrm{H}}$ absorbed and the VSAPF's power losses can be injected back into the power system as $P_1$. In brief, for the simulated operating point, the VSAPF will

continuously release $P_1 \approx 5.6\ kW - 1.16\ kW \approx 4.44\ kW$ back to the power system as it is shown in Fig. 4.10. Altogether, it means that an ultra-low losses VSAPF can perform as harmonic active power recovery device.

**Table 4.3:** SiC based active damper - Estimated Losses during simulation

| Description | Calculation Method | Individual Losses (W) | Quantity | Total Losses(W) |
|---|---|---|---|---|
| MOSFET Switching Losses ($P^{FET}{}_{Sw}$) | PLECS | 45.15 | 6 | 270.9 |
| MOSFET Conduction Losses ($P^{FET}{}_{Cond}$) | PLECS | 60.79 | 6 | 364.74 |
| Schottky Diode Conduction Losses ($P^{Diode}{}_{Cond}$) | PLECS | 7.85 | 6 | 47.1 |
| Coupling Inductor $L_i$ Winding Losses | GeckoMagnetics | 59 | 3 | 177 |
| Coupling Inductor $L_i$ Core Losses | GeckoMagnetics | 5 | 3 | 15 |
| $R_F$ Losses | By Hand | 46 | 3 | 138 |
| Fan-PMax Losses | Datasheet | 140 | 1 | 140 |
| Driver (per 2 channels) Losses | By Hand | 2 | 6 | 6 |
| Total Losses | | | | 1158.74 |

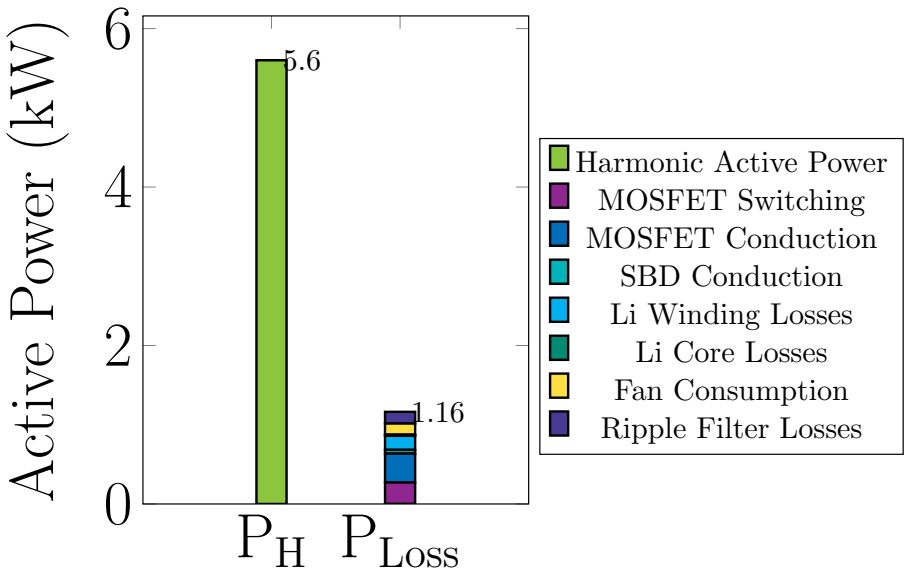


**Fig. 4.9:** Losses estimation: semiconductors (PLECS), Inductors (Gecko Magnetics) and others (hand calculations) for the operating point simulated.

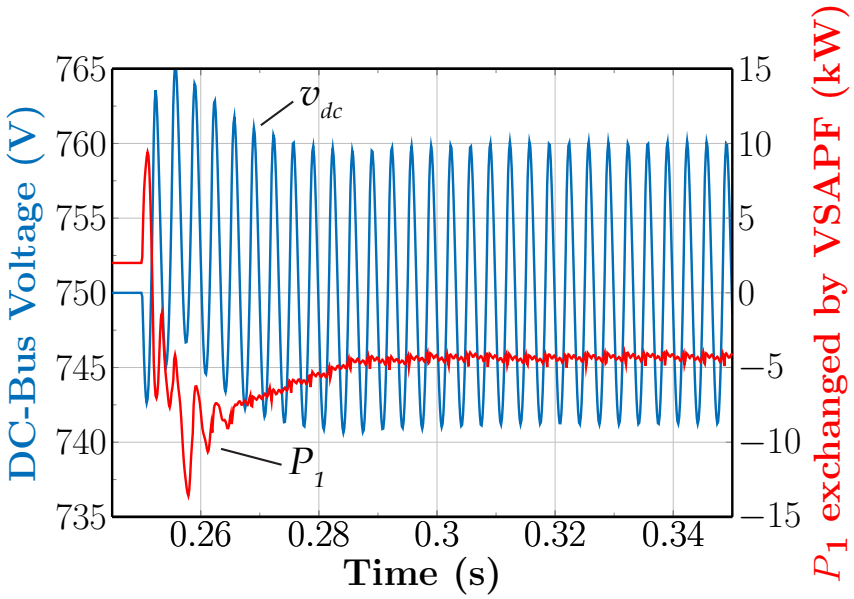


**Fig. 4.10:** DC-bus voltage (blue) and $P_1$(red) exchanged between the VSAPF and the power grid. The VSAPF behaves as a virtual harmonic resistor and absorbs harmonic active power. The DC bus controller senses the increase in the DC-bus voltage $v_{\mathrm{DC}}(t)$ approximately at $t = 0.25$ s due to the absorption of $P_H$ and later on releases $P_1 \approx -5.6kW + 1.16kW \approx -4.44kW$ to the grid in order to regulate $v_{\mathrm{DC}}(t)$ to 750 V.

### 4.6.2 *Harmonic Power Recovery: Comparative evaluation between SiC and Si based active dampers*

The main conclusion reached in section 3.5 is that SiC semiconductors offer a massive reduction of power losses compared to conventional silicon semiconductors. Of course, such reduction in power losses is advantageous to maximize the amount of harmonic active power that an active damper can recover. Thus, in order to compare the impact that both types of semiconductor technologies have on the amount of harmonic active power that a VSAPF can recover, a comparative evaluation between the SiC based active damper proposed in section 4.5 and a silicon based active damper was carried out. On this basis, and taking advantage of the PLECS software, the same scenario described by Fig. 4.6 and Table 4.1 was simulated a second time. However, instead of SiC modules SKM350MB120SCH17 in the PLECS model, in the second simulation, Infineon IGBT4 silicon modules FF200R12KE4 [178] were considered for the power circuit. Such IGBT modules are recommended for high switching frequency applications (> 15 kHz) [150], and thus these IGBT4 modules are suitable for a SAPF's power circuit operating at 20 kHz. Additionally, instead of the coupling inductors based on nanocrystalline material depicted in Fig. 4.5, coupling inductors based on the conventional powered-iron Molybdenum permalloy (MPP) material were considered. Coupling inductors made of this material are very commonly found in industrial SAPFs such as the P200 [108], P300 [109] and A2 [111] filters. The reason being is that MPP inductors offer a good compromise between price and losses for serial production of power electronics systems [179]. Finally, all the other simulation parameters and models for the cooling system and ripple filter were kept constant in the second simulation. On the one hand, the silicon-based active damper's filtering performance is very similar to the one achieved by the SiC based active damper at a switching frequency of 20 kHz. On the other hand, a significant difference in the power losses between both power converters can be observed. In effect, Table 4.4 shows

the results of losses estimated on the silicon based active damper, the one that uses the FF200R12KE4 modules. If we compare the results of Table 4.4 with the results presented in Table 4.3, it can be seen that the total losses in the active damper are reduced if SiC technology and nanocrystalline inductors are used. In particular, the switching losses are reduced by 91 % if SiC MOSFETs are used instead of IGBTs as power switches and if SBDs are used as freewheeling diodes instead of silicon diodes as can be seen in Fig. 4.11 **a)**. This is because SiC MOSFETs exhibit much smaller parasitic capacitances than IGBTs allowing them to have faster-switching transitions and thus smaller switching losses (see section 3.5). In addition, silicon anti-parallel diodes exhibit important switching losses due to the reverse recovery charge, which contributes significantly to the overall switching losses. On the contrary, SBDs exhibit a negligible recovery charge, and thus the switching losses produced by SBDs can be considered as zero. Furthermore, the conduction losses are reduced by 31% if SiC power switches are used instead of silicon power switches as can be seen in Fig. 4.11 **b)**. The latter can be explained in short because SiC MOSFETs exhibit a much smaller voltage drop for the same current level than silicon IGBTs. Thus ohmic losses are in general smaller in SiC MOSFETs than in silicon IGBTs [162]. Furthermore, Fig. 4.12 **a)** shows the total power losses in the coupling inductors for the SiC and Si based active damper. If we recall (3.13), the power losses in an inductor are directly proportional to the constant $K_{\text{Core}}$ that depends on the time-average core loss per unit of volume ($P_{\text{Fe}}$) for the core material used. Actually, $P_{\text{Fe}}$ is 312 $mW/cm^3$ for nanocrystalline material and equal to 1032 $mW/cm^3$ for powdered iron (at 0.2 T and 10 kHz) [136]. Additionally, the relative permeability of nanocrystalline material is 15000 in contrast with the MPP's relative permeability of 75. Thus, less turns are needed in the nanocrystalline inductor than in the MPP coupling inductor to reach the same

**Table 4.4:** Silicon based active damper - Estimated Losses during second simulation

| Description | Calculation Method | Individual Losses (W) | Quantity | Total Losses(W) |
|---|---|---|---|---|
| IGBTs Switching Losses ($P^{\text{Sw}}{}_{\text{IGBT}}$) | PLECS | 380 | 6 | 2280 |
| IGBTs Conduction Losses ($P^{\text{Cond}}{}_{\text{IGBT}}$) | PLECS | 54.25 | 6 | 325.3 |
| Silicon Diode Switching Losses ($P^{\text{Sw}}{}_{\text{Diode}}$) | PLECS | 126 | 6 | 756.04 |
| Silicon Diode Conduction Losses ($P^{\text{Cond}}{}_{\text{Diode}}$) | PLECS | 46.38 | 6 | 278.28 |
| Coupling Inductor $L_i$ Winding Losses | GeckoMagnetics | 140 | 3 | 420 |
| Coupling Inductor $L_i$ Core Losses | GeckoMagnetics | 30 | 3 | 90 |
| $R_F$ Losses | Theoretical calculation | 46 | 3 | 138 |
| Fan-PMax Losses | Datasheet | 140 | 1 | 140 |
| Driver (per 2 channels) Losses | Theoretical calculation | 2 | 6 | 6 |
| Total Losses | | | | 4431.72 |

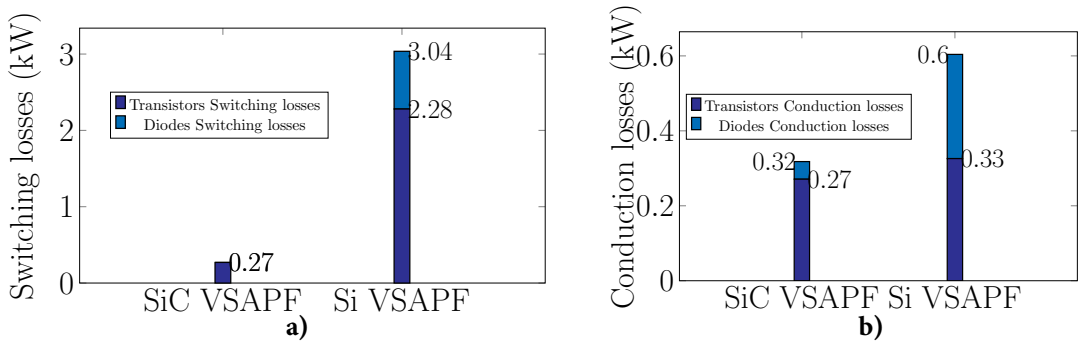


**Fig. 4.11:** SiC and Si based active damper semiconductor losses comparison **a)** Switching Losses **b)** Conduction Losses

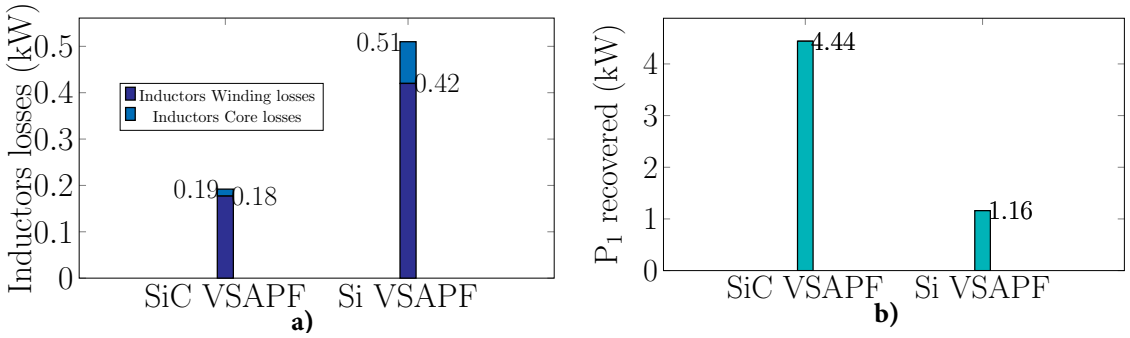


**Fig. 4.12:** SiC and Si based active damper harmonic active power recovered comparison **a)** Inductors Losses **b)** Harmonic active power recovered

nominal inductance. The latter of course plays in favor of the nanocrystalline material because a smaller number of turns implies smaller conduction losses in the inductor's windings. In sum, due to the differences in the time-average core loss constants and the relative permeabilities between nanocrystalline and MPP, the SiC based active damper exhibits 62 % smaller losses in the coupling inductors than the silicon based active damper. Altogether, the SiC based active damper produces only 1.158 kW losses, whereas the silicon based active damper produces 4.431 kW amid the emulation of the 80 $m\Omega$ resistance. On this basis, if the amount of harmonic active power that can be recovered from the absorbed 5.6 kW of harmonic active power (see equation (4.50)) is computed, the SiC based active damper recovers 4.44 kW of harmonic active power. In other words, 80 % of the absorbed harmonic active power is injected back into the power grid by the SiC based active damper. In contrast, the silicon based active damper recovers only 1.16 kW of the absorbed active power. Thus only a 20 % of the absorbed harmonic active power goes back to the grid if silicon semiconductors are used (see Fig. 4.12 **b)**). It is this factor of four times higher amount of harmonic power that can be recovered using SiC technology that makes the recovery of harmonic active power interesting for practical applications.

### 4.6.3 *Experimental Validation*

The active damper in Fig. 4.5 was connected to a three-phase 400 V/50 Hz test bench consisting of a 350 kVA distribution transformer and a 300 kVA Solid-state synchronous series compensator (SSC). Truly, Fig. 4.13 shows the power circuit of the test bench utilized to gather the experimental results and Fig. 4.14 shows a photograph of the test-bench

implementation. In essence, the VSAPF's parameters are the same as in the numerical simulation and can be seen in Table 4.1. However, the test bench for the experiment does not include a nonlinear load. Rather, the SSC is used as a source of harmonic voltages that are added to the fundamental voltage provided by the 350 kVA transformer. This approach is similar to the method used in [180] where a second power electronics system was used alongside the SAPF under test to validate the power filtering functionalities of the latter. In particular, the SSC was used to increase the voltage distortion targeting the 5th, 7th, 11th,13th,17th and 19th harmonics orders. Indeed, the PCC line-to-line voltage $v_{\mathrm{PCCab}}$ was measured through a differential probe TESTEC TT-SI/9110 at the beginning of the experiment with the VSAPF deactivated. The oscilloscope capture of such measurement can be seen in Fig. 4.15. The figure shows the $v_{\mathrm{PCCab}}$ voltage behavior

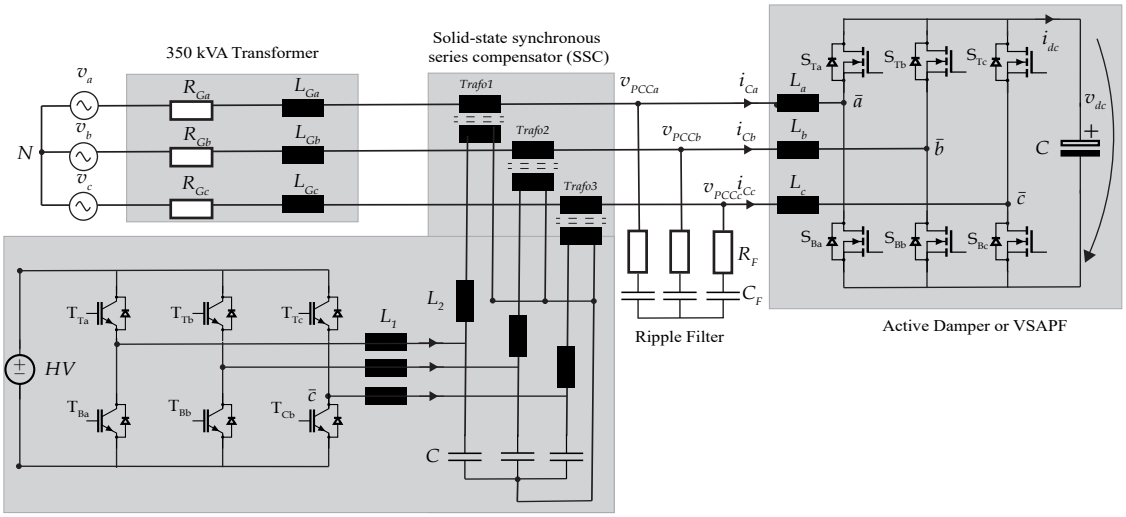


**Fig. 4.13:** Power circuit of the test-bench used for the experimental validation. Active damper connected to an industrial power system that contains a 350 kVA distribution transformer and a SSC as harmonic voltages generator.

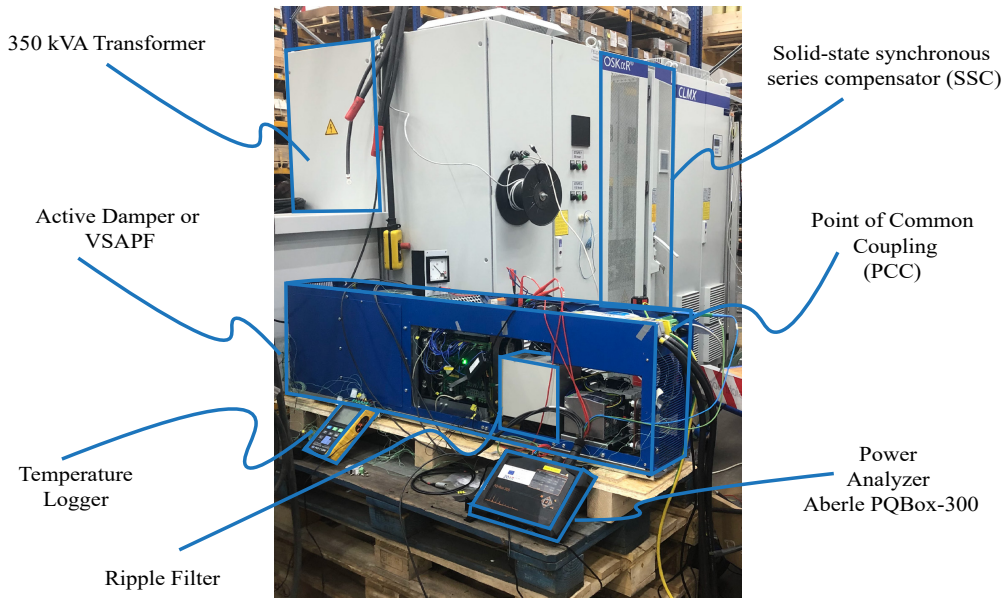


**Fig. 4.14:** Photograph of the test-bench used for the experimental validation. The test-bench was implemented in the facilities of Condensator Dominit GmbH in Brilon,Germany.

over time along with its frequency spectrum. From Fig. 4.15, it is possible to confirm that harmonic distortion is produced by the SSC on the PCC. In addition to the scope measurements, power measurements were carried out using a power quality analyzer PQBox-300 from the company A-Eberle [181]. Also, the PQBox-300 was connected to the test-bench and it measured the three-phase voltages at the PCC ($v_{PCC}$) and the three-phase compensating currents $i_C$ drawn by the VSAPF. Using the PQBox-300, the $THD_V$ at the PCC without VSAPF compensation was measured as 16.3%. Afterwards, the VSAPF is activated with the command to emulate a virtual harmonic resistor of $R_s = 250\ m\Omega$. In this regard, Fig. 4.16 shows the behavior of the PCC line-to-line voltage $v_{PCCab}$ and the behavior of the compensating currents during the VSAPF's activation. From the figure, it

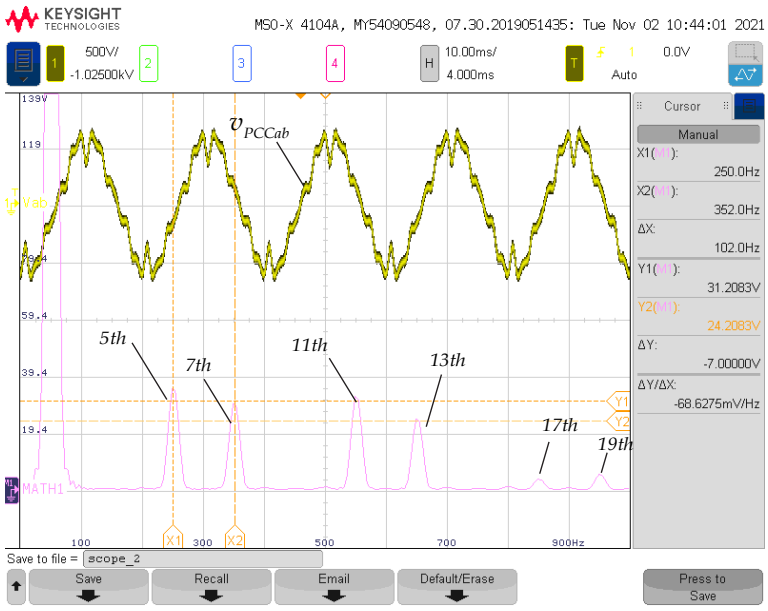


**Fig. 4.15:** Voltage line-to-line $v_{PCCab}$ measured with the VSAPF deactivated. The $v_{PCCab}$ behavior over time is shown in yellow and the frequency spectrum of $v_{PCCab}$ is depicted in pink.

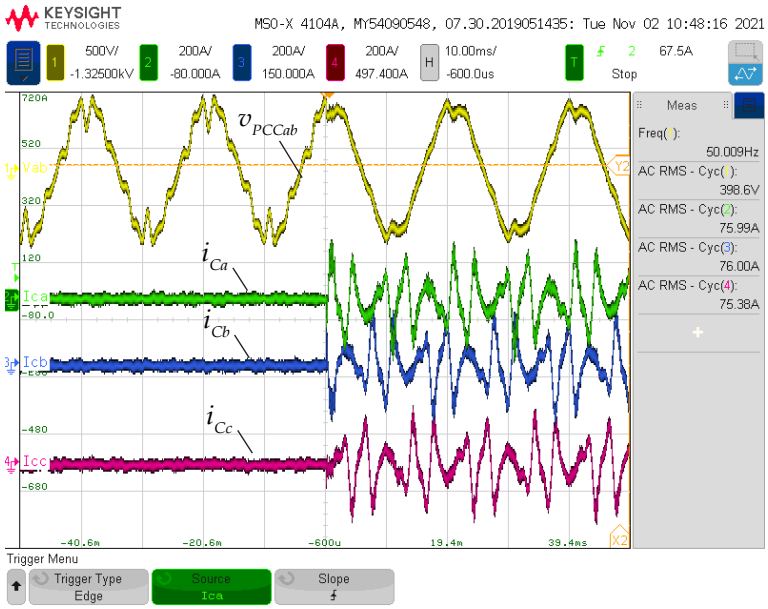


**Fig. 4.16:** Voltage $v_{PCCab}$ and compensation currents measured during the VSAPF´s activation.

is possible to see the fundamental component of the $v_{PCCab}$ voltage has a frequency of 50.009 Hz and an RMS value of 398.6 V. Moreover, from the same figure, it is possible to infer that the VSAPF draws 75 A per phase for the emulation of the $R_s = 250\ m\Omega$ harmonic resistor. After the VSAPF is activated, the $THD_V$ of the voltages at the PCC is decreased from 16.3% to approximately 7.81% as can be seen from measurements extracted from the PQBox-300 and depicted in Fig. 4.17. In addition, Fig. 4.18 shows the oscilloscope capture of the voltage $v_{PCCab}$ and its frequency spectrum measured with the VSAPF activated. Comparing Fig. 4.15 and Fig. 4.18, it is possible to conclude that the

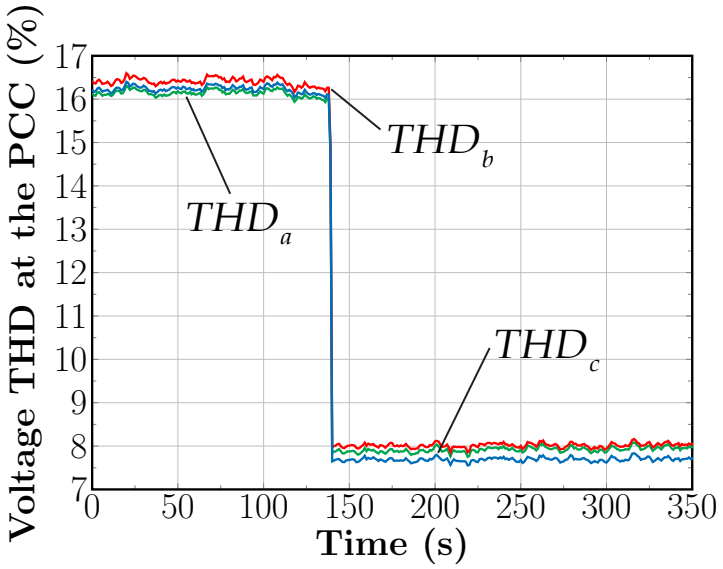


**Fig. 4.17:** Time plot of $THD_V$ (%) for phase a,b,c measured during the experiment. Without VSAPF operation, the $THD_V$ at the PCC is 16.3%. Once the VSAPF is activated with $R_s = 250\ m\Omega$ the $THD_V$ is decreased to 7.81 % due to the VSAPF compensation.

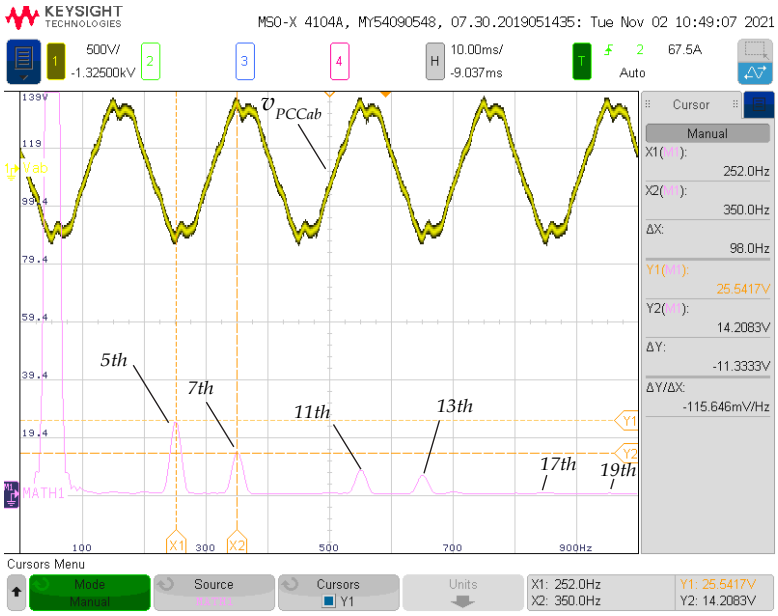


**Fig. 4.18:** Voltage line-to-line $v_{PCCab}$ and its frequency spectrum during the VSAPF operation with reference $R_s = 250\ m\Omega$. The $v_{PCCab}$ behavior over time is shown in yellow and the frequency spectrum of $v_{PCCab}$ is depicted in pink.

voltage harmonic distortion at the 5th, 7th, 11th,13th,17th and 19th harmonics orders are decreased by the action of the VSAPF. Specifically, Fig. 4.19 shows the amount of harmonic voltage distortion before and after the VSAPF activation for each frequency. This information was extracted from the PQBox-300 power analyzer. For example, it is possible to see that the harmonic distortion in the 5th order is decreased from 8.95 % to 6.48 %. Likewise, the voltage distortion in the 19th order was decreased from 1.26 % to 0.18 %. Altogether, the results presented in Fig. 4.15 to Fig. 4.19 show the effectiveness of the VSAPF prototype to mitigate harmonic voltage distortion. Furthermore, the PQBox-300 power analyzer was used during the experiment to measure the harmonic active power absorbed by the active damper at each frequency. The results of such measurement can be seen in Fig. 4.20. First, notice that the PQBox-300 measures the voltage phase angle $\alpha_h$ of the PCC voltages and the current phase angle $\beta_h$ of the compensating currents. On this basis, the PQBox-300 calculates the harmonic phase angle $\theta_h$ as the difference of $\alpha_h$ and $\beta_h$. From Fig. 4.20, it can be seen that the VSAPF´s harmonic phase angle for the harmonic orders 5th, 7th,11th, and 13th was very small, actually less than 4°. Therefore, it can be inferred that the VSAPF achieved ohmic behavior at these harmonic frequencies. Additionally, the PQBox-300 calculated the harmonic active power absorbed at each of the individual frequencies. From Fig. 4.20, the harmonic active power absorbed at the 5th harmonic was:

$$P_5 = P_{5a} + P_{5b} + P_{5c} = 876\ \text{W} + 875\ \text{W} + 819\ \text{W} = 2571\ \text{W} \tag{4.53}$$

Likewise, the absorbed $P_h$ for the 7th and 11th harmonics can be read from Fig. 4.20:

$$P_7 = P_{7a} + P_{7b} + P_{7c} = 256\ \text{W} + 299\ \text{W} + 291\ \text{W} = 846\ \text{W} \tag{4.54}$$

$$P_{11} = P_{11a} + P_{11b} + P_{11c} = 154\ \text{W} + 165\ \text{W} + 163\ \text{W} = 482\ \text{W} \tag{4.55}$$

leading to a total absorbed $P_H$ of:

$$P_H = P_5 + P_7 + P_{11} = 3899\ \text{W} \tag{4.56}$$

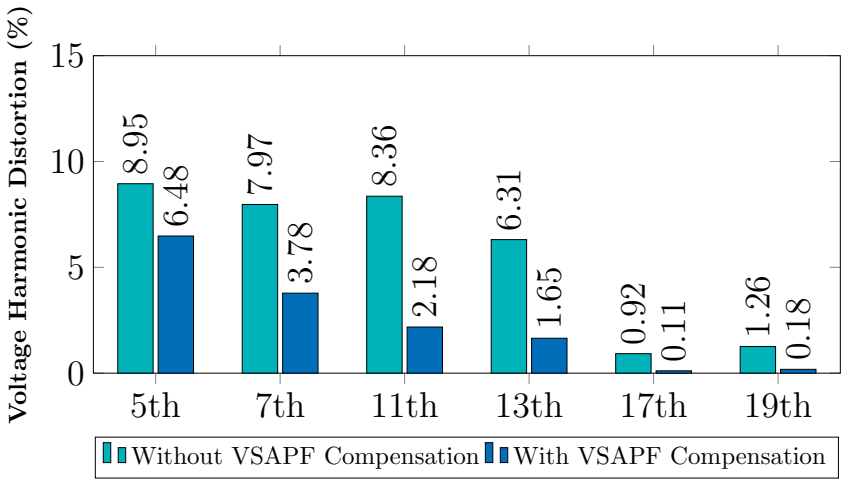


**Fig. 4.19:** Voltage harmonic distortion ($THD_V$) for individual harmonics for phase a. The voltage distortion without VSAPF compensation is shown in light blue and with VSAPF compensation in dark blue. Data extracted from the PQBox-300.

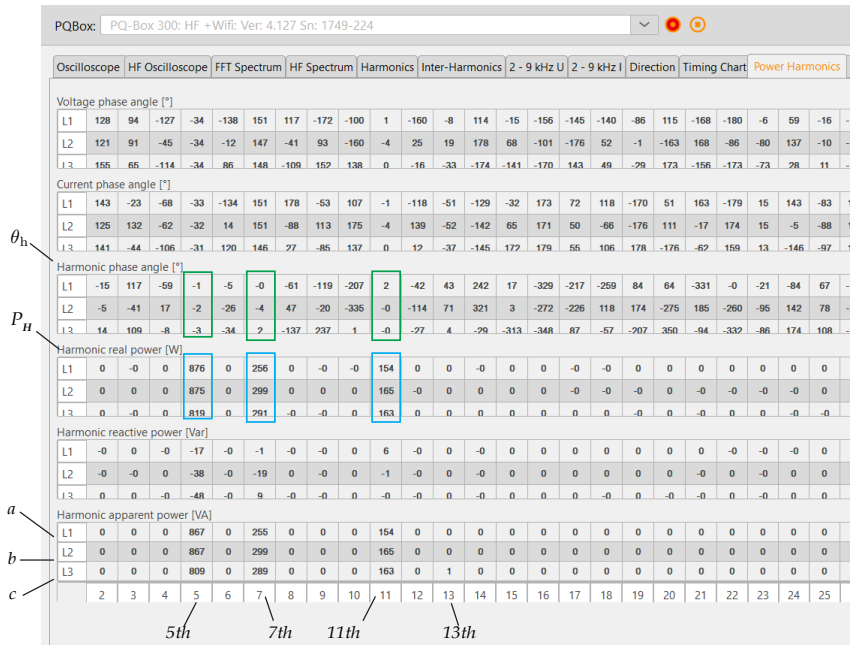


**Fig. 4.20:** Harmonic active power intake on the VSAPF measured during the experimental measurements. PQ-Box 300 measurement results (for harmonics 2nd to 25th). The items measured appear in this order: $v_{PCC}$ phase angle, $i_C$ phase angle, phase angle difference between $v_{PCC}$ and $i_C$, Harmonic Active Power, Harmonic Reactive Power, Harmonic Apparent Power.

In fact, (4.23) can be used to confirm the amount of harmonic active power absorbed:

$$P_{\mathrm{H}} \approx 3 \cdot \frac{(230\ \mathrm{V} \cdot 0.0781)^2}{250\mathrm{m}\Omega} = 3932\ \mathrm{W} \tag{4.57}$$

Notice that there is a good agreement between the measured value of $P_H$ written in (4.56) and the theoretical value calculated in (4.57). Moreover, the fundamental active power $P_1$ exchanged between the VSAPF and the power grid is also measured with the PQBox-300 (see Fig. 4.21). From the figure, it can be observed that when harmonic resistor emulation is deactivated, the VSAPF only draws 70 W of fundamental power from the grid. These 70 W are drawn to compensate for the active damper internal losses and to regulate the DC-Bus voltage to 750 V. Later on, when the VSAPF starts to emulate the harmonic resistor and starts to draw harmonic active power $P_H$, the VSAPF injects fundamental active power back to the power system in order to keep the average value of the DC-voltage constant. Clearly, for this particular operating point, the VSAPF was able to recover 3254 W from the 3899 W absorbed as harmonic active power as seen in the measurement depicted in Fig. 4.21. It follows that during the harmonic resistance emulation, the VSAPF´s overall losses reached the value of $3899\ W - 3254\ W = 645\ W$. In the final analysis, 3254 W are returned back to the power grid as fundamental power confirming the harmonic active power recovery feature by experimental measurements. Finally, the voltage at the DC-Bus was also measured during the operation of the VSAPF. These measurements of the DC-Bus voltage were carried out setting a reference of $R_s = 350\ m\Omega$ for harmonic orders bigger than the 13th order (> 650 Hz) and $R_s = 5\ m\Omega$ for the harmonic orders 5th, 7th, 11th, and 13th. Moreover, for such commanded values, the VSAPF drawn an RMS current of 92.86 A per phase with a peak-to-peak phase current equal to 475 A. In fact, an oscilloscope picture of such measurement can be seen in Fig. 4.22. From the figure, and looking at the frequency spectrum of $v_{\mathrm{dc}}$, it is possible to observe the

frequencies 300 Hz, 600 Hz, 900 Hz, and 1200 Hz on the voltage $v_{dc}$. Those frequencies were predicted by the power balance equation presented in section 4.4.3 and serve to confirm once again the theoretical power analysis made for the VSAPF. In conclusion, the experimental results shown in Fig. 4.22 validate the models proposed in this dissertation to explain the harmonic power recovery through an active damper.

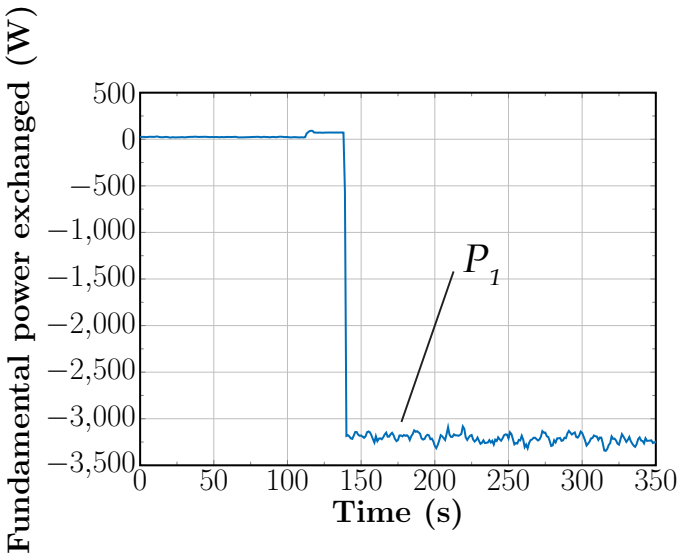


**Fig. 4.21:** Fundamental active power exchanged by the VSAPF and the power grid. Negative $P_1$ means fundamental power been injected back to the grid. Fundamental power measured during the experimental measurements through the PQBox-300 power analyzer.

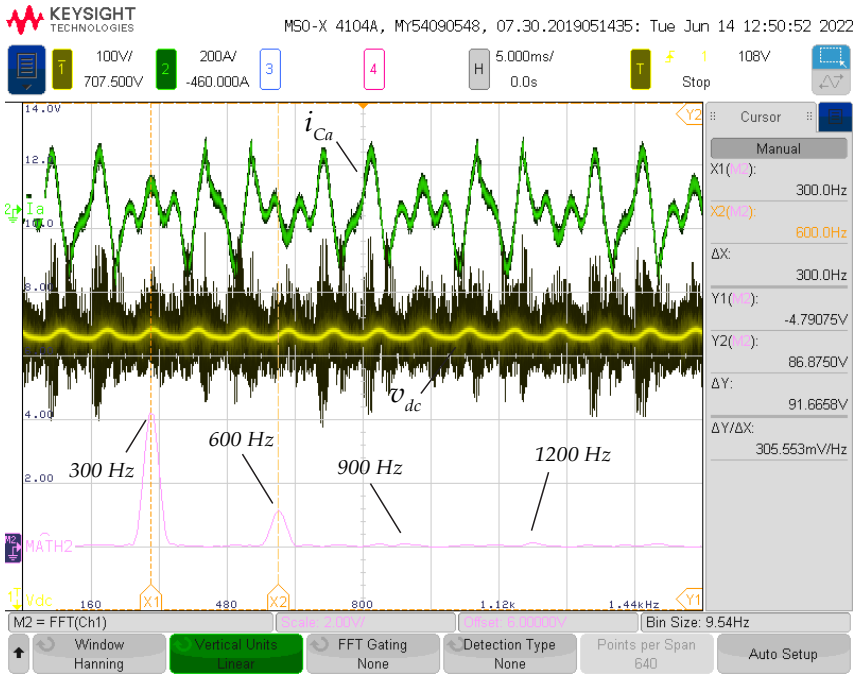


**Fig. 4.22:** Current for phase a and DC-Bus voltage $v_{dc}$ measured during VSAPF compensation. The $i_{Ca}$ behavior over time is shown in green, the DC-Bus voltage is shown in yellow and the frequency spectrum of $v_{dc}$ is depicted in pink.

## 4.7 ULTRA-LOW LOSSES ACTIVE DAMPER EFFICIENCY FIGURES

Using the PQBox-300 power analyzer, the SiC based active damper prototype depicted in Fig. 4.5, and the test-bench of Condensator Dominit illustrated by Fig. 4.14, it was possible to measure the efficiency of the ultra-low losses active damper studied in this chapter. In particular, the efficiency of the active damper was calculated as:

$$\eta = (1 - \frac{P_{\text{Losses}}}{3 \cdot V_{\text{L-N}} \cdot I_{\text{C}} \cdot cos(\phi)}) \cdot 100\% = (1 - \frac{P_{\text{H}} - P_{1}}{S_{\text{SAPF}}}) \cdot 100\% \tag{4.58}$$

Actually, the PQBox-300 automatically calculates the apparent power of the filter $S_{\text{SAPF}}$ as the sum of the product of RMS voltage and current for each phase in the active damper. Indeed, the values $P_H$, $P_1$ and $S_{\text{SAPF}}$ are all provided by the PQBox-300 power analyzer. On this basis, the efficiency of the VSAPF was measured for different compensating currents values. Specifically, 10 measurements were performed setting different setpoints for the emulated resistance, leading to 10 different values of the compensation currents. The results of these measurements can be seen in Table 4.5. From the table, it is possible to infer that the minimum efficiency is 97.72 % when the active damper is entirely inactive. The latter occurred when the reference for the harmonic resistance was set equal to $R_s = 50\,\Omega$ in all the frequency range. In this case, the VSC draws hardly any currents from the power system, and the only currents that can be measured are those that flow from the power system through the ripple filter. Furthermore, the maximum efficiency reached by the active damper is equal to 98.43 %. The peak efficiency occurs when the emulated resistance is set equal to $R_s = 350\ m\Omega$ for harmonic orders bigger than the 11th order (> 550 Hz) and $R_s = 100\ m\Omega$ for the harmonic orders 5th, 7th, and 11th. At this operation point of maximum efficiency (i.e. peak efficiency), the active damper draws an RMS current of 80.68 A per phase, exhibits only 876 W of power losses and has an apparent power of 55.7 kVA. Moreover, it is possible to compare the peak efficiency achieved by the SiC based active damper with the peak efficiency of the state-of-the-art SAPF presented in Fig. 2.7. In this regard, the VSAPF's peak efficiency found from the results presented in Table 4.5 was superimposed to the efficiency figures presented in Fig. 2.7 to produce Fig. 4.23. From Fig. 4.23, it can be seen that the peak efficiency of the SiC based active damper is superior almost by 0.5 % to the peak efficiency reported for state-of-the-art SAPFs. Notice, however, that the P200 was excluded from the comparison

**Table 4.5:** Efficiency measured in the ultra-low losses SiC based active damper for different values of compensating currents

| $R_s$ (mΩ) for h > 650 Hz | $R_5$ (mΩ) | $R_7$ (mΩ) | $R_{11}$ (mΩ) | $R_{13}$ (mΩ) | $V_{\text{L-N}}$ (V) | $I_C$ (A) | $P_{\text{Losses}}$ (W) | $S_{\text{SAPF}}$ (kVA) | $\eta$ (%) |
|---|---|---|---|---|---|---|---|---|---|
| 50k | 50k | 50k | 50k | 50k | 231.62 | 25.07 | 399.5 | 17.5 | 97.72 |
| 900 | 900 | 900 | 900 | 900 | 232.01 | 33.77 | 483.9 | 23.5 | 97.94 |
| 600 | 600 | 600 | 600 | 600 | 232.04 | 43.11 | 555 | 30.4 | 98.17 |
| 450 | 450 | 450 | 450 | 450 | 231.9 | 49.68 | 614.1 | 35.2 | 98.26 |
| 350 | 350 | 350 | 350 | 350 | 231.74 | 56.54 | 660 | 39.3 | 98.33 |
| 350 | 100 | 100 | 100 | 350 | 231.2 | 80.68 | 876 | 55.7 | 98.43 |
| 350 | 5 | 5 | 5 | 350 | 231.1 | 90.45 | 1150 | 64 | 98.2 |
| 350 | 2 | 2 | 2 | 350 | 230.96 | 99.06 | 1330 | 69.8 | 98.09 |
| 350 | 2 | 2 | 2 | 100 | 231.23 | 103.29 | 1420 | 72.2 | 98.03 |
| 350 | 5 | 5 | 5 | 3 | 231.4 | 106.44 | 1390 | 75 | 98.15 |

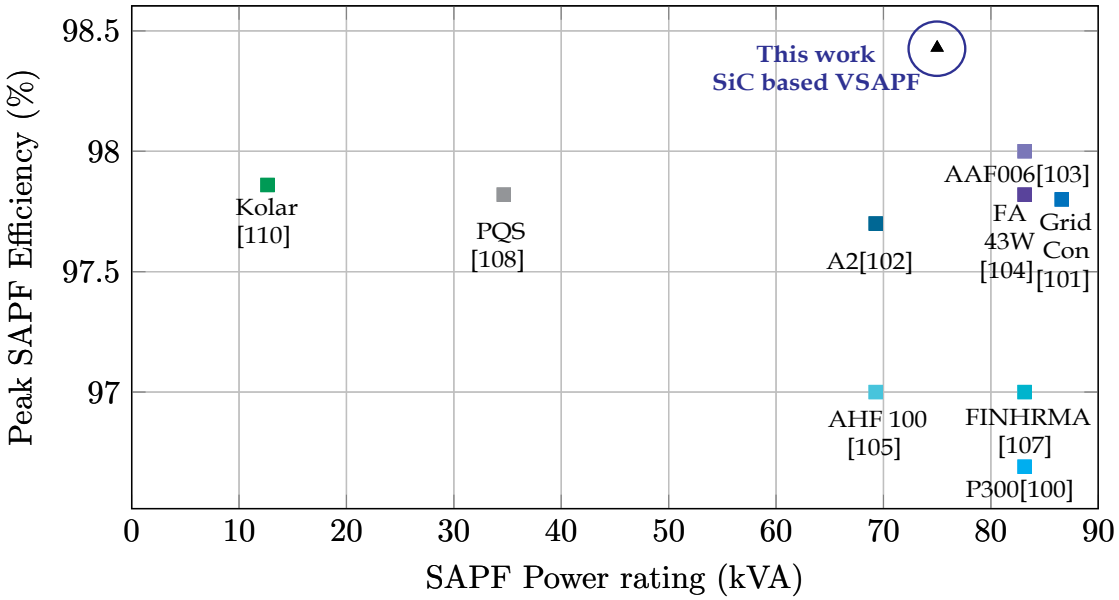


**Fig. 4.23:** Comparison of efficiency figures for state-of-art shunt active power filters and SiC based active damper studied in this dissertation. Based on [109, 110, 111, 112, 113, 114, 116, 117, 118]

presented in Fig. 4.23. Although the P200's peak efficiency was reported in [108], we had in the facilities of Condensator Dominit at our disposal a P200 power filter. Therefore, it was much better to perform a direct comparison under the same conditions between the SiC based active damper and the P200 in the test bench shown in Fig. 4.14. Recall that the P200 was the SAPF reporting the highest peak efficiency in the survey's results presented in Fig. 2.7 and probably it is the active filter with the highest efficiency among the state-of-the-art SAPFs. Therefore, it makes sense to compare not only the peak efficiency of the P200 and the SiC based active damper but also the efficiency in a broader range of compensating currents. With this in mind, the P200's efficiency was measured for compensating currents between 30 A and 106 A using the PQBox 300. Actually, the results of these measurements can be seen in Fig. 4.24. From the figure, it can be seen that the P200 only reaches a peak efficiency of 97.42 % on the test bench. In effect, the peak efficiency is achieved by the P200 when it injects compensating currents with an RMS value of 75 A. Differently said, the P200 reaches its peak efficiency when it exhibits 52.8 kVA of apparent power. At this particular operating point, the P200 was configured to emulate a virtual harmonic resistor of 0.1 Ω in all the frequency range. Furthermore, for compensating currents bigger than 30 A, the SiC based active damper outperforms the P200 in terms of efficiency. Altogether, on the operating range measured from 21 kVA to 75 kVA, the SiC active damper exhibits an average efficiency 0.86 % higher than the P200. The latter means that the amount of harmonic active power that the SiC active damper can recover is almost doubled compared with the P200.

## 4.8 CHAPTER SUMMARY

This chapter presented an ultra-low losses three-phase active damper which performs harmonic active power recovery. Indeed, the purpose of this chapter was to illustrate how an active damper can process the harmonic active power intake and perform harmonic power recovery. Harmonic power recovery in this context is the process of transforming

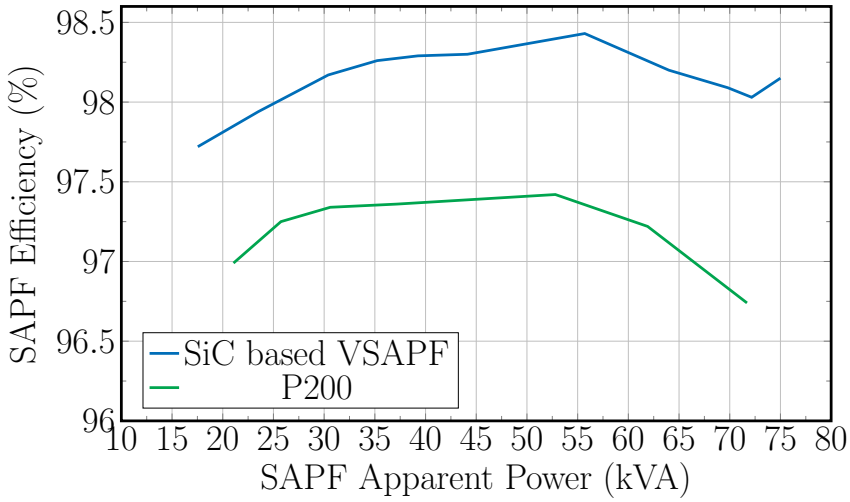


**Fig. 4.24:** Experimental Efficiency Comparison - SiC based active damper and P200 [108] efficiency measured for different values of compensating current and apparent power

the harmonic power absorbed into fundamental power that is injected back into the power system. To the best of the author's knowledge, this aspect of active dampers was not analyzed mathematically in the past and was not proven experimentally. On this basis, the VSAPF power balance equation and the equation's simulation and experimental validations are the main contributions to the body of knowledge brought by this dissertation. Fundamentally, power-electronics technology deals with the transformation and processing of electrical power [182]. In the case of the ultra-low losses VSAPF, it means the transformation of useless harmonic active power that produce just losses and heat into fundamental power that can be used by electrical devices once again. Moreover, it is essential to highlight that the key feature that enables the recovery of a significant amount of harmonic active power is an ultra-low losses VSAPF solution. As any power electronics system, the VSAPF generates power losses amid its operation during the injection of compensating currents all along the virtual harmonic resistance emulation. These power losses include conduction and switching losses in the semiconductors, core and windings losses in the coupling inductors, losses in the DC-Bus capacitors, and many others. Therefore, it is granted that if the target is to recover a significant portion of the absorbed harmonic active power, these power losses should be much lower than the harmonic active power intake. In fact, in the past, VSAPFs built with silicon semiconductors and powdered iron coupling inductors were just too lossy, leading to VSAPF power losses equal to or only slightly smaller than the harmonic active power absorbed. Thus, in practice harmonic active power recovery was hardly possible. In contrast, nowadays, WBG semiconductors technologies such as silicon carbide, and coupling inductors built with nanocrystalline material enable the construction of power electronics systems with ultra-low power losses. It is granted that other works such as [183, 184] dealt with SiC-based SAPF. However, the mentioned works addressed exclusively SAPFs based on the load current detection strategy and mainly were focused on the control design. They have neither discussed nor presented experimental results of harmonic power absorption, conversion, or any other similar concept. Altogether, this chapter covered the design of an ultra-low losses SiC based shunt active power filter based on voltage detection that performs harmonic power recovery and simultaneously reduces the total harmonic voltage distortion in a distribution power system. In particular, the filter emulates a resistance at harmonic frequencies leading to absorption of harmonic active power. As

the filter performs this function, exhibiting ultra-low losses, a significant portion of the harmonic power absorbed is converted to fundamental active power that is injected back into the power system leading to the recovery of harmonic energy.

# 5

# Ultra-low losses active damper impact over the power system: Power Exchange studies under Non-sinusoidal Conditions

Chapter 4 has shown that an ultra-low losses active damper can recover harmonic active power. The question that arises is whether the active damper would reduce the fundamental power consumption as a result of the harmonic power recovery. In order to answer this question, it is necessary to study the overall power exchange among the utility, linear and nonlinear loads, and the ultra-low losses active damper with harmonic power recovery capability. It is granted, that the power exchange among the utility, linear and nonlinear loads, and active damper need to be assessed considering harmonic components in voltages and currents. In other words, the power exchange among all the elements needs to be studied under non-sinusoidal conditions. Caramia et al. in [46] denominated as power balance flow studies the power exchange's studies between utility and power converters under non-sinusoidal conditions . On this basis, the term power balance flow study is adopted in this chapter. In effect, this chapter shows the power balance flow study of a distribution power system (e.g., industrial grid) that includes the active damper presented in section 4.6.1 alongside with liner and nonlinear loads. This study is carried out based on the Buchholz-Emmanuel power theory, which is the base for the IEEE Standard 1459-2010 [171]. This theory highlights and recognizes the importance of the fundamental active power and harmonic active power on the overall power exchange. For this reason, the Buchholz-Emmanuel power theory constitutes the theoretical framework and the supportable theory of this PhD work. Arising out of the power studies under non-sinusoidal conditions, it was found that the active damper with harmonic recovery function achieves a 1.4% reduction in the fundamental active power demanded to the power mains compared with the passive damper. These findings were also published in:

- Iturra R.G., Thiemann P. , "Limits of Harmonic Power Recovery by Power Quality Conditioners in Three-Phase Three-Wire Systems Under Non-Sinusoidal Conditions," in *Sustainable Energy for Smart Cities. SESC 2020. Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering*, vol 375. Springer, Cham.

## 5.1 INTRODUCTION

Due to the enormous proliferation of loads of the nonlinear type, nowadays, the most common voltage distortions encountered in power systems are related to harmonics, inter-harmonics, notching and noise [17, 30]. Indeed, the primary function of power quality conditioners such as passive and active dampers is to protect the electrical devices from waveform distortions in the supplied voltage. Nevertheless, power quality conditioners can also bring some economic benefits to end users. These economic benefits imply some energy savings but mostly embrace savings related to the minimization of production downtimes and damage reduction in electrical equipment [17]. However, assigning a hard value to the last two mentioned savings is complicated. Consequently, they are considered as soft savings and usually end users assign a non-tangible value to them. For this reason, many power filter representatives promote energy's cost reductions rather than the protection feature as a sales strategy to sell power filters [185]. Power quality solutions that advertise the return of investment in some finite amount of time make a particular power quality conditioner device easier to sell. Thus, very often, return of investment figures are used as arguments to convince financial officers to accept the acquisition of a particular power quality conditioner. Unfortunately, many vendors of harmonic mitigation solutions embellish or inflate the energy savings that can be achieved to secure a contract. Sometimes energy savings in the range of 20% to 30% are claimed, when the truth is that the energy savings are much smaller [186].

Consequently many power filters vendors use the kVA metric instead of the kW metric to make claims about significant energy reductions [185]. Equipment that improves or reduces the $THD_V$ or $THD_I$ can reduce the kVA demanded but have minimal effect on the kWs consumed by the facility from the utility point of view [47]. In fact, real energy savings mean a reduction in the real kW or kWh that a particular industrial facility demands [187]. Specifically, the energy required to do actual work (e.g. mechanical, heating, etc.) cannot be eliminated from the electrical costs unless a second energy source is installed locally [186]. Thus, if a device states to save energy on a power system, the only energy that can be saved is the energy wasted in power losses through the power system. Indeed, an important part of the power losses that occur in a power system are related to harmonic currents, namely harmonic power losses. The mentioned power losses arise due to the harmonic active power dissipation produced in resistive elements (e.g. the line resistance, linear loads, passive filters) due to the flow of harmonics currents [3, 17]. Actually, $P_H$ is produced by nonlinear loads and power converters and injected into the power system as was illustrated in Fig. 4.2 [47]. On the one hand, the ultra-low losses active damper acts as a virtual resistor at harmonic frequencies and absorbs the harmonic active power generated by nonlinear loads. On the other hand, the ultra-low losses active damper behaves as a current source that delivers power at the fundamental frequency. Therefore, in practice, the ultra-low losses active damper acts as a secondary power source at the fundamental providing active power recovered from harmonic components. In this chapter, the overall power exchange among the utility, linear and nonlinear loads, and an active damper within a distribution power system (i.e., industrial grid) is investigated. Specifically, the power balance studies were done according to the Buchholz-Emmanuel power theory. Indeed, this theory was used to quantify the amount of fundamental active power that can be saved if an ultra-losses VSAPF with harmonic power recovery functionality transforms the harmonic active power produced by nonlinear loads. Furthermore, based on the $THD_V$ metric, the $THD_I$ metric, and the fundamental power demanded to the power mains, two FOMs are proposed in

order to compare the performance of power quality conditioners. The FOMs reflect in one indicator the capability that a power quality conditioner has to mitigate harmonic distortion and reduce the fundamental power demand from the power mains at the same time.

## 5.2 STUDIED POWER SYSTEM

In order to investigate the energy savings potential due to the processing and recovery of harmonic active power, the distribution power system depicted in Fig. 4.6 was studied using numerical computer simulations. Only for the sake of convenience and clarity, the power system depicted in Fig. 4.6 is redrawn as in Fig. 5.1 in this chapter. Indeed, Fig. 5.1 shows unmistakably how the different currents and voltages are defined for the incoming power balance flow studies. Furthermore, and similar to section 4.6.1, the studied circuit in Fig. 5.1 is a three-phase symmetrical power system supplied by the utility. The utility, in this case the power mains, supplies the industrial grid through a feeder and a distribution transformer. Again, the equivalent impedance of the connecting feeder and transformer referred to the secondary of the transformer is represented by the equivalent components $R_G$ and $L_G$ [17]. Furthermore, the nominal voltage at the secondary of the transformer is $V_1$=230 V RMS, 50 Hz with a background distortion at the 5th harmonic $V_5$ and 7th harmonic $V_7$. On the other hand, the loads in the considered industrial grid are three-phase balanced loads. The loads consist of a capacitor bank formed by capacitors $C_B$ and the ripple filter of the SAPF. In addition a three-phase passive diode rectifier with smoothing DC-Link capacitor is included as nonlinear load and connected to the PCC.

### 5.2.1 *Definition of voltages and currents*

In section 4.4, the instantaneous power at the terminals of the active damper was analyzed. In this section, and to study the apparent power on each of the elements in the power

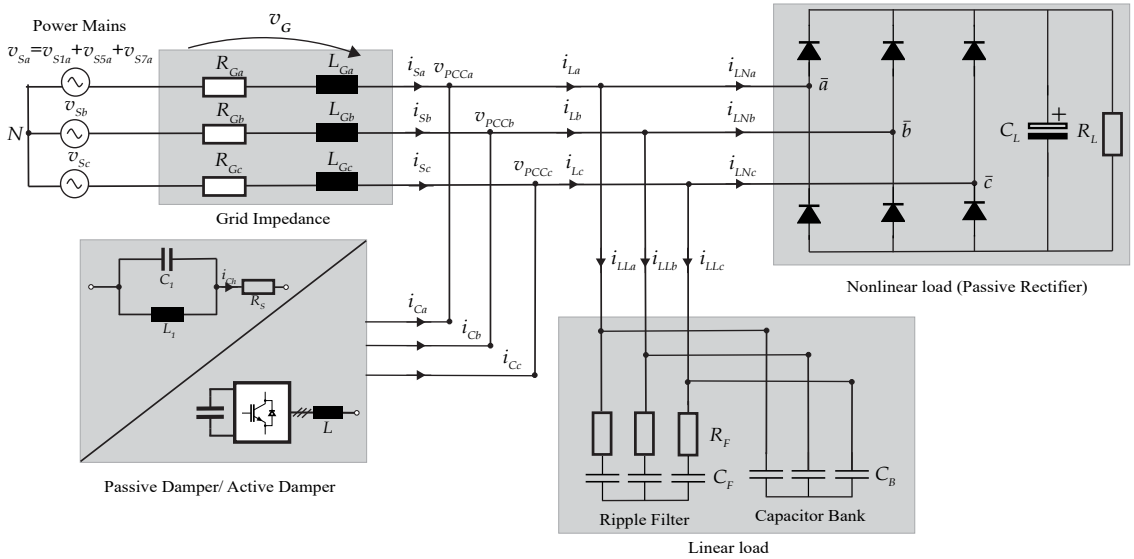


**Fig. 5.1:** Scenario for the power balance flow studies - Power quality conditioners, namely passive damper or active damper connected to an industrial grid that contains a capacitor bank $C_B$, ripple filter and a passive diode rectifier as nonlinear load.

system depicted in Fig. 5.1, it is necessary to generalize the definitions of voltage and current presented in (4.2) to (4.7) to any element **X**. Thus, in the presence of nonlinear loads in the power system, the voltage at the terminals of any element **X** referred to the neutral point $N$ will contain a fundamental and harmonic components. With this in mind, the generic voltage $v_X$ at the phase terminal of any element **X** (e.g. nonlinear load, linear load, passive damper, active damper, grid impedance) under non-sinusoidal conditions can be mathematically written as (5.1) to (5.3).

$$v_{\text{a-X}} = v_{1\text{a-X}} + v_{\text{ha-X}} = \sqrt{2} \cdot V_{1\text{-X}} \cdot \sin(\omega t + \alpha_1) + \sum_{h=2}^{\infty} \sqrt{2} \cdot V_{\text{h-X}} \cdot \sin(h\omega t + \alpha_{\text{h}}) \tag{5.1}$$

$$v_{\text{b-X}} = v_{1\text{b-X}} + v_{\text{hb-X}} = \sqrt{2} \cdot V_{1\text{-X}} \cdot \sin(\omega t + \alpha_1 - \frac{2\pi}{3}) + \sum_{h=2}^{\infty} \sqrt{2} \cdot V_{\text{h-X}} \cdot \sin(h\omega t + \alpha_{\text{h}} - h\frac{2\pi}{3}) \tag{5.2}$$

$$v_{\text{c-X}} = v_{1\text{c-X}} + v_{\text{hc-X}} = \sqrt{2} \cdot V_{1\text{-X}} \cdot \sin(\omega t + \alpha_1 + \frac{2\pi}{3}) + \sum_{h=2}^{\infty} \sqrt{2} \cdot V_{\text{h-X}} \cdot \sin(h\omega t + \alpha_{\text{h}} + h\frac{2\pi}{3}) \tag{5.3}$$

Where the terms expressed with capital letters $\text{V}_{\text{h-X}}$ denote the RMS voltage value of the element **X** at the frequency component $h$. The total RMS voltage $\text{V}_{\text{X}}$ of each phase considering all the components (fundamental and harmonics) was defined by Emanuel in [171] following the approach of Buchholz [188] as:

$$V_{\text{X}} = \sqrt{(V_{1\text{-X}})^2 + (V_{\text{H-X}})^2} = \sqrt{(V_{1\text{-X}})^2 + \sum_{h=2}^{\infty} (V_{\text{h-X}})^2} \tag{5.4}$$

Where the total harmonic voltage contribution $V_{\text{H-X}}$ is:

$$V_{\text{H-X}} = \sqrt{\sum_{h=2}^{\infty} (V_{\text{h-X}})^2} \tag{5.5}$$

The current passing over each element $i_X$ will have the same frequency components as the voltages over the elements, thus the three-phase currents can be expressed as in (5.6) to (5.8):

$$i_{\text{a-X}} = i_{1\text{a-X}} + i_{\text{ha-X}} = \sqrt{2} \cdot I_{1\text{-X}} \cdot \sin(\omega t + \beta_1) + \sum_{h=2}^{\infty} \sqrt{2} \cdot I_{\text{h-X}} \cdot \sin(h\omega t + \beta_{\text{h}}) \tag{5.6}$$

$$i_{\text{b-X}} = i_{1\text{b-X}} + i_{\text{hb-X}} = \sqrt{2} \cdot I_{1\text{-X}} \cdot \sin(\omega t + \beta_1 - \frac{2\pi}{3}) + \sum_{h=2}^{\infty} \sqrt{2} \cdot I_{\text{h-X}} \cdot \sin(h\omega t + \beta_{\text{h}} - h\frac{2\pi}{3}) \tag{5.7}$$

$$i_{\text{c-X}} = i_{1\text{c-X}} + i_{\text{hc-X}} = \sqrt{2} \cdot I_{1\text{-X}} \cdot \sin(\omega t + \beta_1 + \frac{2\pi}{3}) + \sum_{h=2}^{\infty} \sqrt{2} \cdot I_{\text{h-X}} \cdot \sin(h\omega t + \beta_{\text{h}} + h\frac{2\pi}{3}) \tag{5.8}$$

Where capital letters $I_{h\text{-}X}$ denote the current RMS value of the element **X** at the frequency component $h$. The effective current of each phase considering the fundamental and harmonic frequencies can be calculated with an expression similar to (5.4) leading to:

$$I_X = \sqrt{(I_{1\text{-}X}{}^2) + (I_{H\text{-}X})^2} = \sqrt{(I_{1\text{-}X})^2 + \sum_{h=2}^{\infty}(I_{h\text{-}X})^2} \tag{5.9}$$

$$I_{H\text{-}X} = \sqrt{\sum_{h=2}^{\infty}(I_{h\text{-}X})^2} \tag{5.10}$$

The total harmonic voltage and current distortion at the element's terminals are defined as [171]:

$$THD_{V\text{-}X} = \frac{V_{H\text{-}X}}{V_{1\text{-}X}} = \sqrt{(\frac{V_X}{V_{1\text{-}X}})^2 - 1} \tag{5.11}$$

$$THD_{I\text{-}X} = \frac{I_{H\text{-}X}}{I_{1\text{-}X}} = \sqrt{(\frac{I_X}{I_{1\text{-}X}})^2 - 1} \tag{5.12}$$

## 5.3 APPARENT POWER RESOLUTION FOR NON-SINUSOIDAL CONDITIONS

### 5.3.1 *Total Apparent Power*

As each element of the system depicted in Fig. 5.1 is subject to voltages and currents at harmonic frequencies, the apparent power of each element **X** will depend on the RMS current $I_X$ and the RMS voltage drop $V_X$ over the element. Thus, the three-phase apparent power of each of the elements in Fig. 5.1 can be expressed as:

$$S_{eX} = 3 \cdot V_X \cdot I_X \tag{5.13}$$

The apparent power can be squared and expanded as in [189]:

$$\begin{aligned}
S_{e\text{-}X}{}^2 &= 9 \cdot V^2{}_X \cdot I^2{}_X = 9 \cdot (V^2{}_{1\text{-}X} + V^2{}_{H\text{-}X}) \cdot (I^2{}_{1\text{-}X} + I^2{}_{H\text{-}X}) = \\
&= 9 \cdot (V^2{}_{1\text{-}X} \cdot I^2{}_{1\text{-}X}) + 9 \cdot (V^2{}_{1\text{-}X} \cdot I^2{}_{H\text{-}X}) + 9 \cdot (V^2{}_{H\text{-}X} \cdot I^2{}_{1\text{-}X}) + 9 \cdot (V^2{}_{H\text{-}X} \cdot I^2{}_{H\text{-}X}) = \\
&= (9 \cdot V^2{}_{1\text{-}X} \cdot I^2{}_{1\text{-}X}) + (9 \cdot V^2{}_{1\text{-}X} \cdot I^2{}_{H\text{-}X}) + (9 \cdot V^2{}_{H\text{-}X} \cdot I^2{}_{1\text{-}X}) + +(9 \cdot V^2{}_{H\text{-}X} \cdot I^2{}_{H\text{-}X}) = \\
&= (9 \cdot S^2{}_{1\text{-}X}) + (9 \cdot D^2{}_{I\text{-}X}) + (9 \cdot D^2{}_{V\text{-}X}) + (9 \cdot S^2{}_{H\text{-}X}) = \\
&= (3 \cdot S_{1\text{-}X})^2 + (3 \cdot D_{I\text{-}X})^2 + (3 \cdot D_{V\text{-}X})^2 + (3 \cdot S_{H\text{-}X})^2 = \\
&= (S_{e1\text{-}X})^2 + (D_{eI\text{-}X})^2 + (D_{eV\text{-}X})^2 + (S_{eH\text{-}X})^2 = \\
&= (S_{e1\text{-}X})^2 + (S_{eN\text{-}X})^2
\end{aligned} \tag{5.14}$$

### 5.3.2 *Components of the Total Apparent Power*

Equation (5.14) can be written as:

$$S_{e\text{-}X}{}^2 = S_{e1\text{-}X}{}^2 + S_{eN\text{-}X}{}^2 \qquad [V^2 \cdot A^2] \tag{5.15}$$

The first term in (5.15) is the square of the fundamental (50 Hz) apparent power $S_{e1}$:

$$S_{e1\text{-}X} = 3 \cdot S_{1\text{-}X} = 3 \cdot V_{1\text{-}X} \cdot I_{1\text{-}X} \tag{5.16}$$

$$S_{e1\text{-}X} = 3 \cdot \sqrt{(P_{1\text{-}X})^2 + (Q_{1\text{-}X})^2} \tag{5.17}$$

$$S_{e1\text{-}X} = 3 \cdot \sqrt{\{V_{1\text{-}X} \cdot I_{1\text{-}X} \cdot cos(\beta_1 - \alpha_1)\}^2 + \{V_{1\text{-}X} \cdot I_{X1} \cdot sin(\beta_1 - \alpha_1)\}^2} \qquad [V \cdot A] \tag{5.18}$$

The second term in (5.15) is the square of the non-fundamental apparent power $S_{eN\text{-}X}$, defined as following [190]:

$$S_{eN\text{-}X} = \sqrt{(D_{eI\text{-}X})^2 + (D_{eV\text{-}X})^2 + (S_{eH\text{-}X})^2} \qquad [V \cdot A] \tag{5.19}$$

Where:

$$D_{eI\text{-}X} = 3 \cdot D_{I\text{-}X} = 3 \cdot V_{1\text{-}X} \cdot I_{H\text{-}X} \qquad [VAr] \tag{5.20}$$

is the total current distortion power. The current distortion power results from the product of the voltage at the fundamental and currents at different harmonic frequencies. The expression contains only oscillatory terms with an average value of zero. Therefore $D_{eI\text{-}X}$ produces only reactive power and its units are fundamentally VAr. Actually, most of the times the distortion power $D_{eI\text{-}X}$ makes the largest contribution to the magnitude of $S_{eN\text{-}X}$. Furthermore,

$$D_{eV\text{-}X} = 3 \cdot D_{V\text{-}X} = 3 \cdot V_{H\text{-}X} \cdot I_{1\text{-}X} \qquad [VAr] \tag{5.21}$$

is the total voltage distortion power. The voltage distortion power is the product of harmonic voltages at different frequencies and the current at the fundamental frequency. It follows that $D_{eV\text{-}X}$, as $D_{eI\text{-}X}$, produces only reactive power leading to VAr as a unit. Finally, the smallest of all the terms in (5.19) is the total harmonic apparent power $S_{eH\text{-}X}$,

$$S_{eH\text{-}X} = 3 \cdot S_{H\text{-}X} = 3 \cdot V_{H\text{-}X} \cdot I_{H\text{-}X} \qquad [V \cdot A] \tag{5.22}$$

In detail, the harmonic apparent power can be characterized by two important components [190]:

$$S_{eH\text{-}X}{}^2 = P_{H\text{-}X}{}^2 + D_{eH\text{-}X}{}^2 \qquad [V^2 \cdot A^2] \tag{5.23}$$

where the active power is equal to the average value of the harmonic apparent power $S_{eH\text{-}X}$ over time (e.g over a time averaging window of one fundamental period). It is granted that if we consider a three-phase system, the contribution of each phase to the active power needs to be considered. With the last arguments in mind, the total harmonic active power over the element **X**, namely $P_{H\text{-}X}$, is formally defined as [47]:

$$P_{H\text{-}X} = \int_0^{\frac{1}{f_1}} \Big\{ (v_{ha\text{-}X} \cdot i_{ha\text{-}X}) + (v_{hb\text{-}X} \cdot i_{hb\text{-}X}) + (v_{hc\text{-}X} \cdot i_{hc\text{-}X}) \Big\} dt \tag{5.24}$$

$$P_{H\text{-}X} = 3 \cdot \sum_{h=2}^{\infty} V_{h\text{-}X} \cdot I_{h\text{-}X} \cdot cos(\alpha_h - \beta_h) \qquad [W] \tag{5.25}$$

Which has an average value different from zero due to the product of currents and voltages at the same frequency. Actually, this one is the only one component of the apparent power than can be processed later to recover energy from the harmonics present in the power system. The term $D_{eH\text{-}X}$ is defined as harmonic distortion power and results from the product of harmonic voltages and currents at different frequencies. As a consequence the term $D_{eH\text{-}X}$ contains only oscillatory terms and thus produces only reactive power and it is equal to:

$$D_{eH\text{-}X} = \sqrt{(S_{eH\text{-}X})^2 - (P_{H\text{-}X})^2} \qquad [VAr] \tag{5.26}$$

On the other hand, the expression for $D_{eH\text{-}X}$ can also be written in terms of the harmonic reactive power $Q_H$ and the cross-product of harmonic voltages and currents at different frequencies $G_H$. Put it simple:

$$D_{eH\text{-}X} = \sqrt{(Q_{H\text{-}X})^2 + (G_{H\text{-}X})^2} \qquad [V \cdot A] \tag{5.27}$$

where:

$$Q_{H\text{-}X} = 3 \cdot \sum_{h=2}^{\infty} V_{h\text{-}X} \cdot I_{h\text{-}X} \cdot sin(\alpha_h - \beta_h) \qquad [VAr] \tag{5.28}$$

and:

$$G_{H\text{-}X} = 3 \cdot \sum_{m=1}^{v-1} \sum_{n=m+1}^{v} (V_{m\text{-}X} I_{n\text{-}X})^2 + (V_{n\text{-}X} I_{I\text{-}X})^2 - (2 V_{m\text{-}X} I_{n\text{-}X} V_{n\text{-}X} I_{I\text{-}X} cos(\theta_m - \theta_n)) \qquad [VAr] \tag{5.29}$$

Altogether, according to the Buchholz-Emmanuel power theory the apparent power $S_{e\text{-}X}$ can be solved in the components depicted in Fig. 5.2 [47].

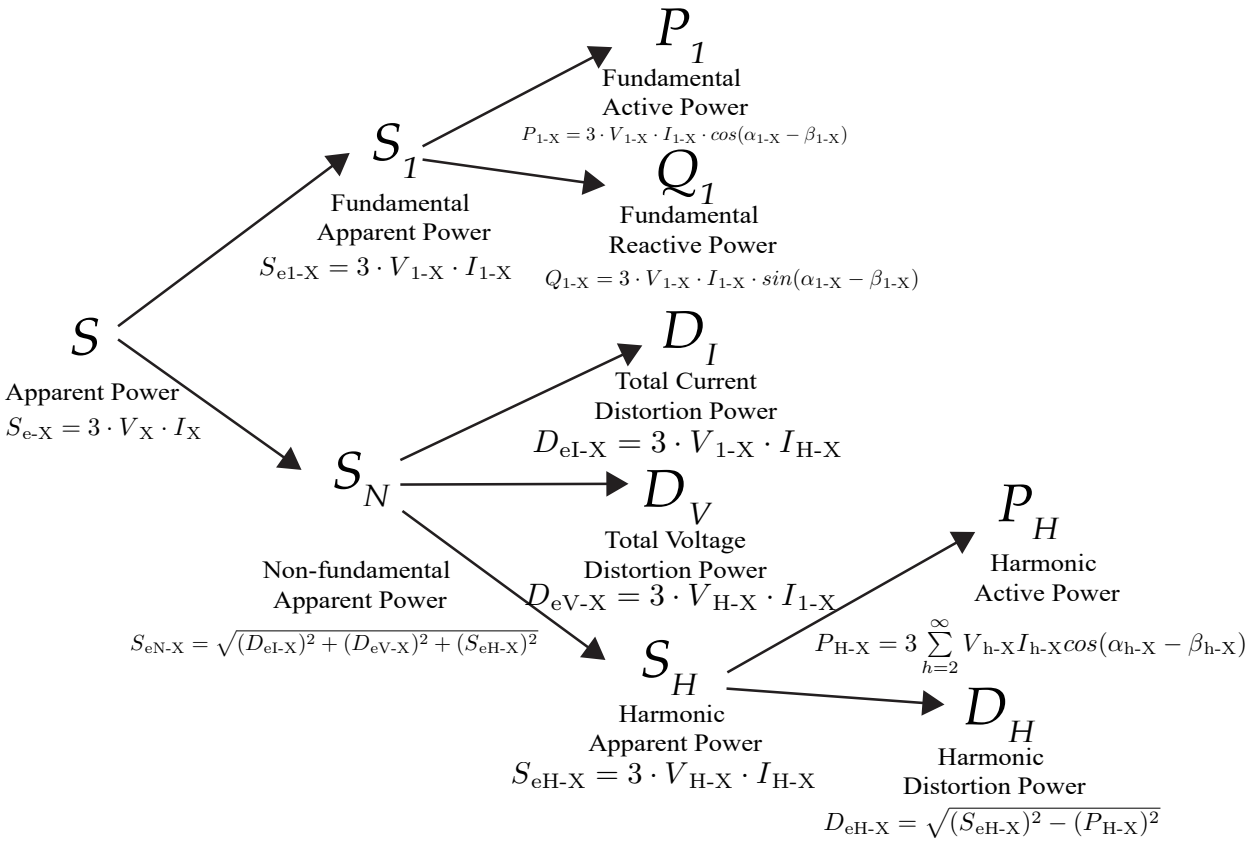


**Fig. 5.2:** Apparent power resolution according to Buchholz-Emmanuel power theory [47].

## 5.4 APPARENT POWER COMPONENTS AS FUNCTIONS OF THD

The different components that form the total apparent power (5.14) can be expressed as functions of the total harmonic voltage and current distortion $THD_{V\text{-}X}$ and $THD_{I\text{-}X}$ [47]. This can be achieved by multiplying and dividing each term by the factor $S_{e1\text{-}X}$. For instance, take the total current distortion power $D_{eI\text{-}X}$ in equation (5.20):

$$D_{eI\text{-}X} = 3 \cdot V_{1\text{-}X} \cdot I_{H\text{-}X} = S_{e1\text{-}X} \cdot \frac{3 \cdot V_{1\text{-}X} \cdot I_{H\text{-}X}}{3 \cdot V_{1\text{-}X} \cdot I_{1\text{-}X}} = S_{e1\text{-}X} \cdot \frac{I_{H\text{-}X}}{I_{1\text{-}X}} = S_{e1\text{-}X} \cdot THD_{I\text{-}X} \tag{5.30}$$

A similar procedure can be carried out with the total voltage distortion power $D_{eV\text{-}X}$ and the harmonic apparent power $S_{eH\text{-}X}$ leading to equations (5.31) and (5.32).

$$D_{eV\text{-}X} = 3 \cdot V_{H\text{-}X} \cdot I_{1\text{-}X} = S_{e1\text{-}X} \cdot \frac{3 \cdot V_{H\text{-}X} \cdot I_{1\text{-}X}}{3 \cdot V_{1\text{-}X} \cdot I_{1\text{-}X}} = S_{e1\text{-}X} \cdot \frac{V_{H\text{-}X}}{V_{1\text{-}X}} = S_{e1\text{-}X} \cdot THD_{V\text{-}X} \tag{5.31}$$

$$S_{eH\text{-}X} = 3 \cdot V_{H\text{-}X} \cdot I_{H\text{-}X} = S_{e1\text{-}X} \cdot \frac{3 \cdot V_{H\text{-}X} \cdot I_{H\text{-}X}}{3 \cdot V_{1\text{-}X} \cdot I_{1\text{-}X}} = S_{e1\text{-}X} \cdot THD_{V\text{-}X} \cdot THD_{I\text{-}X} \tag{5.32}$$

Replacing (5.30), (5.31) and (5.32) in (5.19) leads to:

$$S_{eN\text{-}X} = S_{e1\text{-}X} \cdot \sqrt{(THD_{I\text{-}X})^2 + (THD_{V\text{-}X})^2 + (THD_{V\text{-}X} \cdot THD_{I\text{-}X})^2} \quad [V \cdot A] \tag{5.33}$$

Substituting (5.33) in (5.15) results in:

$$S_{e\text{-}X} = S_{e1\text{-}X} \cdot \sqrt{1 + (THD_{I\text{-}X})^2 + (THD_{V\text{-}X})^2 + (THD_{V\text{-}X} \cdot THD_{I\text{-}X})^2} \quad [V \cdot A] \tag{5.34}$$

## 5.5 POWER EXCHANGE BETWEEN UTILITY, LOADS, AND ACTIVE DAMPER UNDER NON-SINUSOIDAL CONDITIONS

This section examines the power exchange among the utility, linear and nonlinear loads, and the ultra-low losses active damper with harmonic power recovery capability in a distribution power system. In other words, this section delves into the study of the power balance flow [46] of a distribution power system that contains an active damper that performs harmonic power recovery. Although it was not possible to derive final analytical solutions due to the nonlinear characteristics of the passive rectifier depicted in Fig. 5.1, numerical solutions backed by computer simulations were obtained. Therefore, based on the definitions of the Buchholz-Emmanuel power theory (see Fig. 5.2) , the apparent power and its components were analyzed for each element of the power system depicted in Fig. 5.1. In particular, the voltages and currents used to calculate the apparent power of each of the elements can be seen in Table 5.1. Moreover, and similar to the simulations carried out in section 4.6.1, the simulations for the power balance flow studies were carried out through a coupling-simulation between Simulink and PLECS with the parameters written in Table 4.1. Furthermore, three simulations and thus three power balance flow studies of the power circuit depicted in Fig. 5.1 were performed. Each simulation considered a specific scenario. First, a simulation was carried out without any passive or active damper connected to the distribution power system. This first scenario serves as benchmark for the comparison and it is named in the following discussion as

**Table 5.1:** Voltages and currents used for the apparent power resolution

| Element | Voltages (V) | Currents (A) |
|---|---|---|
| Nonlinear Load | $v_{PCCa}$,$v_{PCCb}$,$v_{PCCc}$ | $i_{LNa}$,$i_{LNb}$,$i_{LNc}$ |
| Linear Load | $v_{PCCa}$,$v_{PCCb}$,$v_{PCCc}$ | $i_{LLa}$,$i_{LLb}$,$i_{LLc}$ |
| Passive Damper/Active Damper | $v_{PCCa}$,$v_{PCCb}$,$v_{PCCc}$ | $i_{Ca}$,$i_{Cb}$,$i_{Cc}$ |
| Loads at PCC | $v_{PCCa}$,$v_{PCCb}$,$v_{PCCc}$ | $i_{Sa}$,$i_{Sb}$,$i_{Sc}$ |
| Grid Impedance | $v_{Ga}$,$v_{Gb}$,$v_{Gc}$ | $i_{Sa}$,$i_{Sb}$,$i_{Sc}$ |
| Power Mains | $v_{Sa}$,$v_{Sb}$,$v_{sc}$ | $i_{Sa}$,$i_{Sb}$,$i_{Sc}$ |

the *No compensation* scenario. Second, a simulation of the power system in Fig. 5.1 has been performed using the parallel-resonant damper (see Fig. 1.13 **a)**) with $R_s = 85\ m\Omega$ as power quality conditioner. This second scenario is referred as the *Passive Damper* scenario in the incoming discussion. Finally, the power balance flow study was performed for the same industrial facility as the previous scenarios, but the ultra-low losses active damper was considered as power quality conditioner. Obviously, in order to have a comparable situation for the evaluation of the power conditioners, the active damper was set to emulate a resistor of $R_s = 85\ m\Omega$. Lastly, in all scenarios, the load in the DC-side of the passive rectifier has been configured to behave as a constant power load that draws always 288 kW of average power.

### 5.5.1 *No compensation scenario*

Fig. 5.3 and Fig. 5.4 show the behavior of the voltages at PCC and the currents drawn from the power mains gathered during the computer simulation of the power system depicted in Fig. 5.1. Notice that in the simulation, neither the passive nor the active damper are activated prior to $t$ =0.25 s. Under this scenario, the passive rectifier excites the resonance produced by the capacitor bank and the grid inductance leading to a high voltage distortion at $t$ <0.25 s. On this basis, FFT analyses were carried out over the voltages and currents of each of the elements defined in Table 5.1. For the results presented in this subsection, the FFT analyses were performed at $t$ <0.25 s in order to study the power balance flow of the distribution power system under the *No compensation* scenario. Moreover, from the FFT results, the RMS values and THD values for voltages and currents in all the elements along the power system were calculated. Those results are summarized in Table 5.2. From the table, it can be seen that the $THD_V$ at the PCC without the passive damper is 8.21 %. In addition, the supply currents $THD_I$ was measured as 60.44 % without compensation. Moreover, the passive rectifier draws a current of 498.6 A from the PCC from which 433.24 A are due to the fundamental component. Also, the complete industrial grid draws phase currents of 501.64 A, from which 429.32 A are due to the flow of fundamental current. Naturally, it can be seen that the three-phase system is balanced and completely symmetrical because the values for the three-phase voltages and currents are practically the same among the three-phases. Furthermore, based on the values written in Table 5.2 and equations (5.13) to (5.34), some of the apparent power's

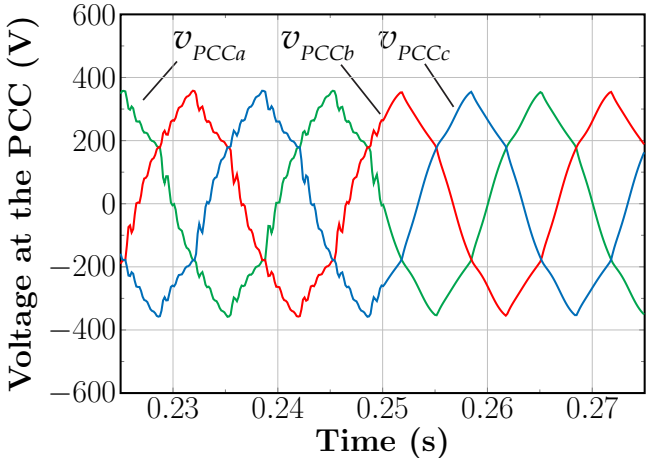


**Fig. 5.3:** VPCC line-to-neutral voltages for the three phases. Notice that the passive damper is connected to the system at $t$ = 0.25 s.

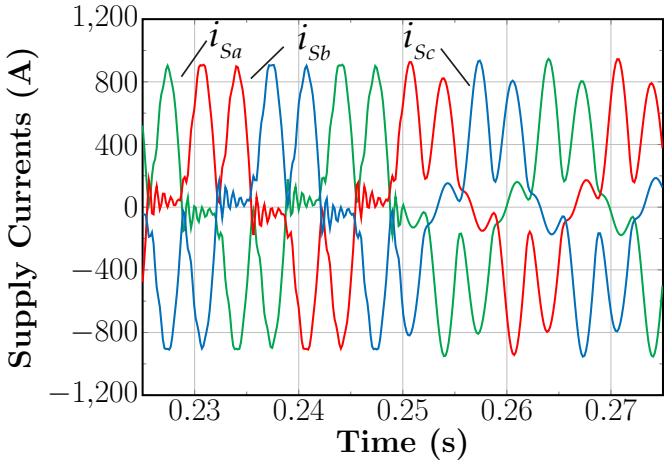


**Fig. 5.4:** Supply currents drawn from the mains. Compensation activated at $t$ = 0.25 s.

**Table 5.2:** RMS values and THD measured without power filter connected.

| Phase | $V_X$ (V) | $I_X$ (A) | $THD_{\text{V-X}}$ (%) | $THD_{\text{I-X}}$ (%) | $V_{1\text{-X}}$ (V) | $I_{1\text{-X}}$ (A) |
|---|---|---|---|---|---|---|
| Passive Rectifier | | | | | | |
| a | 230.08 | 498.60 | 8.21 | 56.96 | 229.31 | 433.24 |
| b | 230.08 | 498.59 | 8.21 | 56.96 | 229.31 | 433.24 |
| c | 230.08 | 498.59 | 8.21 | 56.96 | 229.31 | 433.24 |
| Linear Load | | | | | | |
| a | 230.08 | 47.65 | 8.21 | 131.71 | 229.31 | 28.82 |
| b | 230.08 | 47.65 | 8.21 | 131.71 | 229.31 | 28.82 |
| c | 230.08 | 47.65 | 8.21 | 131.71 | 229.31 | 28.82 |
| Loads | | | | | | |
| a | 230.08 | 501.65 | 8.21 | 60.44 | 229.31 | 429.33 |
| b | 230.08 | 501.65 | 8.21 | 60.44 | 229.31 | 429.32 |
| c | 230.08 | 501.64 | 8.21 | 60.44 | 229.31 | 429.32 |
| Grid Impedance | | | | | | |
| a | 17.82 | 501.65 | 420.13 | 60.44 | 4.13 | 429.33 |
| b | 17.82 | 501.65 | 420.13 | 60.44 | 4.13 | 429.32 |
| c | 17.82 | 501.64 | 420.13 | 60.44 | 4.13 | 429.32 |
| Power Mains | | | | | | |
| a | 230.09 | 501.65 | 2.83 | 60.44 | 230.00 | 429.33 |
| b | 230.09 | 501.65 | 2.83 | 60.44 | 230.00 | 429.32 |
| c | 230.09 | 501.64 | 2.83 | 60.44 | 230.00 | 429.32 |

components (see Fig. 5.2) for the different elements of the power system were calculated. In particular the total apparent power $S$, the fundamental apparent power $S_1$, the non-fundamental apparent power $S_N$, and the harmonic apparent power $S_H$ were calculated using (5.13),(5.16), and (5.19) to (5.22) respectively. In addition the active and reactive power at the fundamental and harmonic frequencies were calculated using (5.18), (5.25), and (5.28). The results of the mentioned calculations can be seen in Table 5.3. Certainly, the table shows the components of the apparent power resolution under non-sinusoidal conditions of the power system without any active power filter connected. Moreover, each phase's total apparent power and fundamental apparent power are added together in Table 5.3. The latter is done with the idea to obtain a reference for the total apparent

**Table 5.3:** Apparent power resolution under non-sinusoidal conditions for each element of power circuit depicted in Fig. 5.1 according to the Buchholz-Emmanuel power theory without power quality conditioner connected to the system.

| Phase | $S_X$ (kVA) | $S_{1\text{-}X}$ (kVA) | $S_{N\text{-}X}$ (kVA) | $S_{H\text{-}X}$ (kVA) | $P_{1\text{-}X}$ (kW) | $P_{H\text{-}X}$ (kW) | $Q_{1\text{-}X}$ (kVar) | $Q_{H\text{-}X}$ (kVar) |
|---|---|---|---|---|---|---|---|---|
| Passive Rectifier (NLL) | | | | | | | | |
| a | 114.72 | 99.35 | 57.36 | 4.65 | 97.83 | -1.29 | 17.29 | -3.60 |
| b | 114.72 | 99.35 | 57.36 | 4.65 | 97.83 | -1.29 | 17.30 | -3.60 |
| c | 114.72 | 99.35 | 57.36 | 4.65 | 97.83 | -1.29 | 17.29 | -3.60 |
| NLL | 344.15 | 298.04 | | | 293.49 | -3.86 | 51.88 | -10.81 |
| Linear Load (LL) | | | | | | | | |
| a | 10.96 | 6.61 | 8.75 | 0.71 | 0.04 | 0.06 | -6.61 | -0.54 |
| b | 10.96 | 6.61 | 8.75 | 0.71 | 0.04 | 0.06 | -6.61 | -0.54 |
| c | 10.96 | 6.61 | 8.75 | 0.71 | 0.04 | 0.06 | -6.61 | -0.54 |
| LL | 32.89 | 19.82 | | | 0.11 | 0.19 | -19.82 | -1.62 |
| Overall Loads | | | | | | | | |
| a | 115.42 | 98.45 | 60.25 | 4.89 | 97.87 | -1.22 | 10.69 | -4.14 |
| b | 115.42 | 98.45 | 60.25 | 4.89 | 97.87 | -1.22 | 10.69 | -4.14 |
| c | 115.42 | 98.45 | 60.25 | 4.89 | 97.87 | -1.22 | 10.69 | -4.14 |
| Loads | 346.26 | 295.35 | | | 293.60 | -3.67 | 32.06 | -12.43 |
| Grid Impedance | | | | | | | | |
| a | 8.94 | 1.77 | 8.76 | 4.50 | 0.09 | 0.03 | 1.77 | 3.89 |
| b | 8.94 | 1.77 | 8.76 | 4.50 | 0.09 | 0.03 | 1.77 | 3.89 |
| c | 8.94 | 1.77 | 8.76 | 4.50 | 0.09 | 0.03 | 1.77 | 3.89 |
| Grid Imp. | 26.82 | 5.32 | | | 0.27 | 0.10 | 5.31 | 11.66 |
| Power Mains | | | | | | | | |
| a | 115.43 | 98.75 | 59.77 | 1.69 | 97.96 | -1.19 | 12.46 | -0.26 |
| b | 115.43 | 98.74 | 59.77 | 1.69 | 97.96 | -1.19 | 12.46 | -0.26 |
| c | 115.42 | 98.74 | 59.77 | 1.69 | 97.96 | -1.19 | 12.46 | -0.26 |
| Mains | 346.28 | 296.23 | | | 293.87 | -3.57 | 37.37 | -0.77 |

power of each element (e.g. the passive rectifier, the linear loads, and the overall industrial grid as seen by the mains). On the other hand, according to the Buchholz-Emmanuel power theory, only the active powers $P_1$ and $P_H$ and the reactive powers $Q_1$ and $Q_H$ exhibit the additiveness property. For this reason, they are the only elements summed or added together for the three phases in Table 5.3 besides the apparent powers. Obviously, the additiveness property can be verified using the results presented in Table 5.3. Take for instance the fundamental power $P_1$. From the table, it is possible to see that the power mains supplies the industrial grid with 293.87 kW of fundamental power. From the 293.87 kW, 0.27 kW are dissipated in the resistive part of the grid impedance, and 0.11 kW are absorbed by the linear loads as fundamental active power. Finally, the difference 293.87 kW - 0.11 kW - 0.27 kW = 293.49 kW is absorbed as fundamental active power by the passive rectifier. Likewise, Table 5.3 shows that the passive rectifier as NLL absorbs 293.49 kW of fundamental power, transfers 288 kW to its DC-side and injects backwards to the power system 3.86 kW of harmonic active power. At this point, the power losses on the passive rectifier (i.e. the power losses on the diodes of the passive rectifier) reach the value of 0.73 kW. Furthermore, from the 3.86 kW of harmonic active power generated by

the nonlinear load, 0.19 kW are dissipated in the linear loads, namely in the resistors $R_F$, and 0.1 kW are dissipated in the resistive part of the grid impedance $R_G$. Meanwhile, the remaining harmonic active power of 3.57 kW flows upstream of the distribution power system to the power mains. Indeed, the remaining 3.57 kW will be dissipated in other resistive elements on the power mains side. In effect, this characteristic of the NLL as harmonic active power generator has been shown in several studies [46, 165, 166, 191]. Actually, Emanuel in [166] suggested that the negative harmonic active power measured at the terminals of the NLL is an indicator that this kind of load is polluting the power system with harmonics currents. Lastly, the additiveness property in $Q_1$ and $Q_H$ can be also verified by simple inspection of Table 5.3.

### 5.5.2 *Passive damper scenario*

In order to study the power exchanged among all the elements in the power circuit when the passive damper is connected to the system (*Passive Damper* scenario), FFT analyses were carried out over the magnitudes defined in Table 5.1 for $t > 0.25$ s. Arising out of the FFT analyses, the RMS and THD values on each of the elements of the power system with the passive damper connected were calculated. Those results can be seen in Table 5.4. In any case, Table 5.4 is equivalent to Table 5.2 but with the power system

**Table 5.4:** RMS values and THD measured for voltages and currents at each element of the power system depicted in Fig. 5.1 with the passive damper as power quality conditioner.

| Phase | $V_X$ (V) | $I_X$ (A) | $THD_{V\text{-}X}$ (%) | $THD_{I\text{-}X}$ (%) | $V_{1\text{-}X}$ (V) | $I_{1\text{-}X}$ (A) |
|---|---|---|---|---|---|---|
| Passive Rectifier | | | | | | |
| a | 230.04 | 519.44 | 5.68 | 66.24 | 229.67 | 433.06 |
| b | 230.04 | 519.40 | 5.68 | 66.24 | 229.67 | 433.01 |
| c | 230.05 | 519.43 | 5.68 | 66.24 | 229.68 | 433.05 |
| Linear Load | | | | | | |
| a | 230.05 | 30.48 | 5.68 | 33.97 | 229.68 | 28.86 |
| b | 230.04 | 30.48 | 5.68 | 33.97 | 229.67 | 28.86 |
| c | 230.04 | 30.48 | 5.68 | 33.97 | 229.67 | 28.86 |
| Passive Damper | | | | | | |
| a | 230.04 | 153.04 | 5.68 | 18218.55 | 229.67 | 0.84 |
| b | 230.04 | 153.07 | 5.68 | 19915.96 | 229.67 | 0.77 |
| c | 230.05 | 153.09 | 5.68 | 20973.83 | 229.68 | 0.73 |
| Loads + Passive Damper | | | | | | |
| a | 230.04 | 484.11 | 5.68 | 50.69 | 229.67 | 431.80 |
| b | 230.04 | 483.97 | 5.68 | 50.70 | 229.67 | 431.67 |
| c | 230.05 | 484.13 | 5.68 | 50.70 | 229.68 | 431.81 |
| Grid Impedance | | | | | | |
| a | 12.85 | 484.11 | 292.75 | 50.69 | 4.15 | 431.80 |
| b | 12.85 | 483.97 | 292.94 | 50.70 | 4.15 | 431.67 |
| c | 12.85 | 484.13 | 292.90 | 50.70 | 4.15 | 431.81 |
| Power Mains | | | | | | |
| a | 230.09 | 484.11 | 2.83 | 50.69 | 230.00 | 431.80 |
| b | 230.09 | 483.97 | 2.83 | 50.70 | 230.00 | 431.67 |
| c | 230.09 | 484.13 | 2.83 | 50.70 | 230.00 | 431.81 |

subject to the action of the passive damper. Similarly, Table 5.5 is the equivalent of Table 5.3 but with the passive damper connected to the power system. From Table 5.4 it can be seen that the $THD_V$ at the PCC with the passive damper is decreased from 8.21 % to 5.68 %. Likewise, the $THD_I$ on the supply currents is also improved, where a reduction from 60.44 % to 50.70 % was achieved. Interestingly, the fundamental active power demanded from the utility increases from 293.87 kW to 297.32 kW. The reason being is the nonlinear characteristic of the passive rectifier. When the passive damper is connected to the power system, the overall impedance seen by the passive rectifier changes due to the presence of the passive damper. It is granted that a passive rectifier with a smoothing DC-side capacitor is a NLL of the harmonic-voltage source type [30]. This type of nonlinear load is by far the most common on industrial grids [79]. Certainly,

**Table 5.5:** Apparent power resolution under non-sinusoidal conditions for each element of power circuit depicted in Fig. 5.1 according to the Buchholz-Emmanuel power theory with the passive damper connected.

| Phase | $S_X$ (kVA) | $S_{1\text{-}X}$ (kVA) | $S_{N\text{-}X}$ (kVA) | $S_{H\text{-}X}$ (kVA) | $P_{1\text{-}X}$ (kW) | $P_{H\text{-}X}$ (kW) | $Q_{1\text{-}X}$ (kVar) | $Q_{H\text{-}X}$ (kVar) |
|---|---|---|---|---|---|---|---|---|
| Passive Rectifier (NLL) | | | | | | | | |
| a | 119.49 | 99.46 | 66.23 | 3.74 | 99.11 | -2.76 | 8.38 | -2.36 |
| b | 119.48 | 99.45 | 66.22 | 3.74 | 99.10 | -2.76 | 8.38 | -2.36 |
| c | 119.49 | 99.46 | 66.23 | 3.74 | 99.11 | -2.76 | 8.37 | -2.36 |
| NLL | 358.47 | 298.38 | | | 297.32 | -8.28 | 25.14 | -7.09 |
| Linear Load (LL) | | | | | | | | |
| a | 7.01 | 6.63 | 2.29 | 0.13 | 0.04 | 0.00 | -6.63 | -0.12 |
| b | 7.01 | 6.63 | 2.29 | 0.13 | 0.04 | 0.00 | -6.63 | -0.12 |
| c | 7.01 | 6.63 | 2.29 | 0.13 | 0.04 | 0.00 | -6.63 | -0.12 |
| LL | 21.04 | 19.89 | | | 0.11 | 0.01 | -19.89 | -0.35 |
| Passive Damper | | | | | | | | |
| a | 35.21 | 0.19 | 35.21 | 2.00 | 0.01 | 1.99 | 0.19 | -0.13 |
| b | 35.21 | 0.18 | 35.21 | 2.00 | 0.01 | 1.99 | 0.18 | -0.13 |
| c | 35.22 | 0.17 | 35.22 | 2.00 | 0.01 | 1.99 | 0.17 | -0.13 |
| Pass. Damp. | 105.64 | 0.54 | | | 0.03 | 5.97 | 0.54 | -0.38 |
| Loads + Passive Damper | | | | | | | | |
| a | 111.37 | 99.17 | 50.67 | 2.85 | 99.15 | -0.77 | 1.95 | -2.61 |
| b | 111.33 | 99.14 | 50.66 | 2.85 | 99.12 | -0.77 | 1.93 | -2.61 |
| c | 111.37 | 99.18 | 50.67 | 2.85 | 99.16 | -0.77 | 1.91 | -2.61 |
| Loads | 334.07 | 297.49 | | | 297.43 | -2.30 | 5.79 | -7.82 |
| Grid Impedance | | | | | | | | |
| a | 6.22 | 1.79 | 5.96 | 2.66 | 0.09 | 0.02 | 1.79 | 2.61 |
| b | 6.22 | 1.79 | 5.95 | 2.66 | 0.09 | 0.02 | 1.79 | 2.61 |
| c | 6.22 | 1.79 | 5.96 | 2.66 | 0.09 | 0.02 | 1.79 | 2.61 |
| Grid Imp. | 18.66 | 5.38 | | | 0.27 | 0.07 | 5.37 | 7.82 |
| Power Mains | | | | | | | | |
| a | 111.39 | 99.31 | 50.45 | 1.42 | 99.24 | -0.74 | 3.74 | 0.0002 |
| b | 111.36 | 99.28 | 50.43 | 1.42 | 99.21 | -0.74 | 3.72 | 0.0002 |
| c | 111.39 | 99.32 | 50.45 | 1.42 | 99.25 | -0.74 | 3.70 | 0.0001 |
| Mains | 334.14 | 297.91 | | | 297.70 | -2.23 | 11.16 | 0.0004 |

in nonlinear loads of the harmonic-voltage source type, the shape of the currents drawn depend on the grid impedance. On account of this dependency of the nonlinear load currents to the grid impedance, the fundamental active power demanded by the industrial grid increases when the passive damper is connected to the power system, although the average power demanded at the DC-side of the passive rectifier is held constant at 288 kW. In summary, there is an increase of 3.45 kW in the fundamental power absorbed by the nonlinear load compared to the *No compensation* scenario. Furthermore, it can be seen that in presence of the passive damper, the NLL also generates more harmonic active power. Comparing Table 5.3 and Table 5.5, it can be seen that the harmonic active power generated by NLL increases from 3.83 kW to 8.28 kW. The latter implies an increase of 4.4 kW on the harmonic active power generated by the NLL. This fact directly correlates with the increase of fundamental active power absorbed due to the change in the overall impedance seen by the NLL. Besides, the power losses on the passive rectifier (i.e., losses on the power diodes of the passive rectifier) are decreased from 0.73 kW to 0.04 kW. The latter situation can be explained by the fact that the rectifier´s power diodes produce more losses under resonance conditions due to the high frequency currents drawn from the PCC. Moreover, the $P_H$ generated by the nonlinear load is reflected back to the power system. The $P_H$ is absorbed by the linear loads, but to a major extent by the passive damper. The latter dissipates 5.97 kW of the 8.28 kW of harmonic active power generated by the NLL. Finally, only 0.07 kW of harmonic active power are dissipated in the grid impedance, and 2.23 kW of harmonic power flow upstream to the power mains.

### 5.5.3 *Active damper scenario*

When the active damper is connected to the power system depicted in Fig. 5.1, the behavior of the voltages at PCC and the currents drawn from the power mains can be seen in Fig. 5.5 and Fig. 5.6 respectively. Notice that the active damper is connected to the PCC at $t$ =0.25 s, just as the passive damper simulation presented in the last subsection. Moreover, the voltages and currents defined in Table 5.1 are also studied through FFT analyses for this scenario (see Table 5.6). In effect, Table 5.6 shows the RMS and THD values of each of the elements of the power system with the active damper connected. Clearly, Table 5.6 is the counterpart of Table 5.4, but for the scenario of the

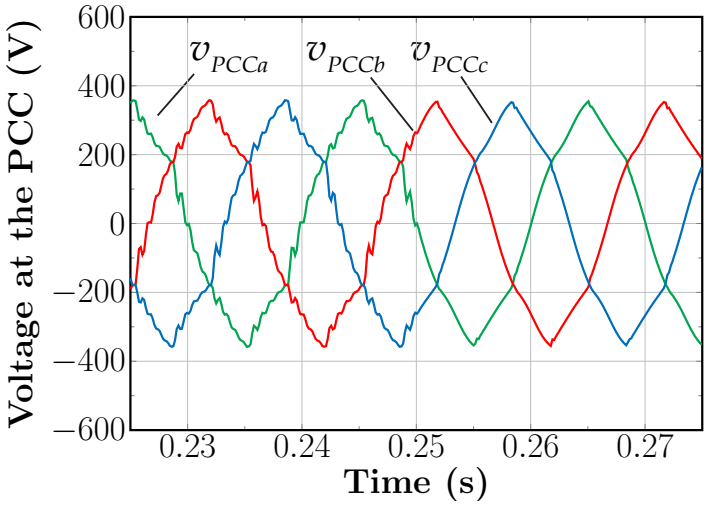


**Fig. 5.5:** VPCC line-to-neutral voltages for the three phases. The VSAPF is activated at $t$ = 0.25 s.

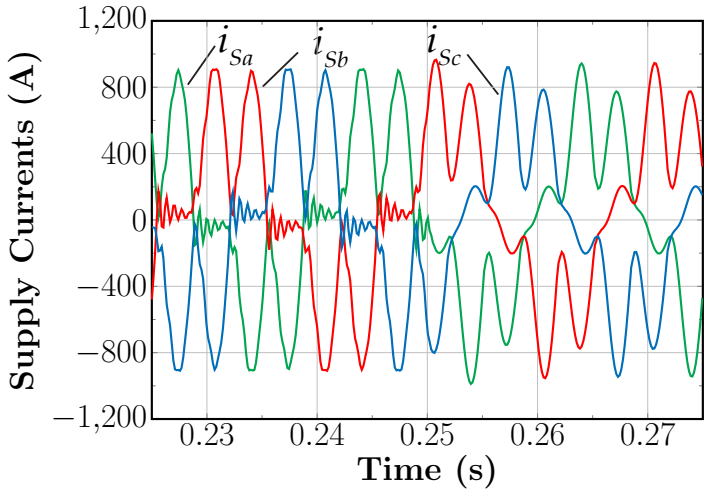


**Fig. 5.6:** Supply currents $i_{Sa}$,$i_{Sb}$,$i_{Sc}$ drawn from the power mains with the active damper connected at $t$ = 0.25 s.

**Table 5.6:** RMS values and THD measured for voltages and currents at each element of the power system depicted in Fig. 5.1 with the active damper as power quality conditioner.

| Phase | $V_X$ (V) | $I_X$ (A) | $THD_{V\text{-}X}$ (%) | $THD_{I\text{-}X}$ (%) | $V_{1\text{-}X}$ (V) | $I_{1\text{-}X}$ (A) |
|---|---|---|---|---|---|---|
| Passive Rectifier | | | | | | |
| a | 230.03 | 520.46 | 5.39 | 67.50 | 229.70 | 431.38 |
| b | 230.03 | 520.43 | 5.39 | 67.51 | 229.70 | 431.33 |
| c | 230.03 | 520.43 | 5.39 | 67.51 | 229.70 | 431.33 |
| Linear Load | | | | | | |
| a | 230.03 | 31.89 | 5.39 | 47.05 | 229.70 | 28.86 |
| b | 230.03 | 31.88 | 5.39 | 46.97 | 229.70 | 28.86 |
| c | 230.03 | 31.90 | 5.39 | 47.07 | 229.70 | 28.86 |
| Active Damper | | | | | | |
| a | 230.03 | 154.34 | 5.39 | 2415.88 | 229.70 | 6.38 |
| b | 230.03 | 154.33 | 5.39 | 2432.33 | 229.70 | 6.34 |
| c | 230.03 | 154.35 | 5.39 | 2430.02 | 229.70 | 6.35 |
| Loads + Active Damper | | | | | | |
| a | 230.03 | 474.16 | 5.39 | 49.00 | 229.70 | 425.80 |
| b | 230.03 | 474.15 | 5.39 | 49.00 | 229.70 | 425.79 |
| c | 230.03 | 474.16 | 5.39 | 49.00 | 229.70 | 425.79 |
| Grid Impedance | | | | | | |
| a | 12.37 | 474.16 | 285.20 | 49.00 | 4.09 | 425.80 |
| b | 12.37 | 474.15 | 285.15 | 49.00 | 4.09 | 425.79 |
| c | 12.37 | 474.16 | 285.17 | 49.00 | 4.09 | 425.79 |
| Power Mains | | | | | | |
| a | 230.09 | 474.16 | 2.83 | 49.00 | 230.00 | 425.80 |
| b | 230.09 | 474.15 | 2.83 | 49.00 | 230.00 | 425.79 |
| c | 230.09 | 474.16 | 2.83 | 49.00 | 230.00 | 425.79 |

active damper. Again, in the same way as in the analysis of the passive damper, Table 5.7 is constructed based on the results presented in Table 5.6. On the one hand, from

Table 5.6, it is possible to infer that the $THD_V$ at the PCC is decreased to 5.39 % by the active damper. On the other hand, from Table 5.7, it can be seen that the NLL absorbs 296.24 kW of fundamental active power, in contrast to the 293.49 kW absorbed in the absence of the active damper. Once more, this behavior corresponds to the change on the operating point of the NLL. From the 296.24 kW of fundamental active power absorbed, the NLL returns to the system 7.85 kW of harmonic active power. From these 7.85 kW of harmonic active power, 5.65 kW are absorbed by the active damper. Subsequently, the active damper transforms a portion of the absorbed 5.65 kW of harmonic active power and returns 4.4 kW of fundamental active power back to the system. The latter is, of course, due to the harmonic power recovery feature of the VSAPF.

**Table 5.7:** Apparent power resolution under non-sinusoidal conditions for each element of power circuit depicted in Fig. 5.1 according to the Buchholz-Emmanuel power theory with the active damper connected.

| Phase | $S_X$ (kVA) | $S_{1\text{-}X}$ (kVA) | $S_{N\text{-}X}$ (kVA) | $S_{H\text{-}X}$ (kVA) | $P_{1\text{-}X}$ (kW) | $P_{H\text{-}X}$ (kW) | $Q_{1\text{-}X}$ (kVar) | $Q_{H\text{-}X}$ (kVar) |
|---|---|---|---|---|---|---|---|---|
| Passive Rectifier (NLL) | | | | | | | | |
| a | 119.72 | 99.09 | 67.20 | 3.60 | 98.75 | -2.62 | 8.11 | -2.30 |
| b | 119.72 | 99.08 | 67.20 | 3.60 | 98.74 | -2.62 | 8.12 | -2.30 |
| c | 119.72 | 99.08 | 67.20 | 3.60 | 98.74 | -2.62 | 8.11 | -2.30 |
| NLL | 359.15 | 297.24 | | | 296.24 | -7.85 | 24.34 | -6.90 |
| Linear Load (LL) | | | | | | | | |
| a | 7.34 | 6.63 | 3.14 | 0.17 | 0.04 | 0.00 | -6.63 | -0.11 |
| b | 7.33 | 6.63 | 3.14 | 0.17 | 0.04 | 0.00 | -6.63 | -0.11 |
| c | 7.34 | 6.63 | 3.14 | 0.17 | 0.04 | 0.00 | -6.63 | -0.11 |
| LL | 22.01 | 19.89 | | | 0.11 | 0.01 | -19.89 | -0.32 |
| Active Damper | | | | | | | | |
| a | 35.50 | 1.47 | 35.47 | 1.91 | -1.47 | 1.88 | -0.03 | 0.12 |
| b | 35.50 | 1.46 | 35.47 | 1.91 | -1.46 | 1.88 | -0.03 | 0.12 |
| c | 35.50 | 1.46 | 35.47 | 1.91 | -1.46 | 1.88 | -0.02 | 0.12 |
| Act. Damp. | 106.51 | 4.38 | | | -4.38 | 5.65 | -0.08 | 0.37 |
| Loads + Active Damper | | | | | | | | |
| a | 109.07 | 97.80 | 48.28 | 2.58 | 97.79 | -0.72 | 1.47 | -2.32 |
| b | 109.07 | 97.80 | 48.28 | 2.58 | 97.79 | -0.72 | 1.47 | -2.32 |
| c | 109.07 | 97.80 | 48.28 | 2.58 | 97.79 | -0.72 | 1.47 | -2.32 |
| Loads | 327.21 | 293.41 | | | 293.38 | -2.17 | 4.40 | -6.97 |
| Grid Impedance | | | | | | | | |
| a | 5.87 | 1.74 | 5.60 | 2.44 | 0.09 | 0.02 | 1.74 | 2.38 |
| b | 5.86 | 1.74 | 5.60 | 2.43 | 0.09 | 0.02 | 1.74 | 2.38 |
| c | 5.87 | 1.74 | 5.60 | 2.44 | 0.09 | 0.02 | 1.74 | 2.38 |
| Grid Imp. | 17.59 | 5.23 | | | 0.26 | 0.06 | 5.22 | 7.14 |
| Power Mains | | | | | | | | |
| a | 109.10 | 97.93 | 48.08 | 1.36 | 97.88 | -0.70 | 3.21 | 0.0566 |
| b | 109.10 | 97.93 | 48.08 | 1.36 | 97.88 | -0.70 | 3.21 | 0.0566 |
| c | 109.10 | 97.93 | 48.09 | 1.36 | 97.88 | -0.70 | 3.21 | 0.0567 |
| Mains | 327.30 | 293.80 | | | 293.64 | -2.10 | 9.62 | 0.1700 |

### 5.5.4 *Power balance flow in presence of the power quality conditioners - Comparative Evaluation*

This section compares the harmonic mitigation performance and fundamental active power reduction achieved by the passive and active dampers. For this purpose, Table 5.8 is constructed based on the results presented in Table 5.5 and Table 5.7. Table 5.8 shows some of the components of the apparent power measured at the terminals of the passive damper and active damper during operation. Obviously, the advantage of Table 5.8 is that it allows to compare side by side the fundamental active power and the harmonic active power absorbed by each of the power quality conditioners, and it will serve as a starting point for the comparison. Table 5.8 shows that the apparent power rating of the passive and active damper equals approximately 106 kVA. Also, from the table, it may be inferred that the passive damper absorbs $P_H = 5.97\ kW$ of harmonic active power from the 8.28 kW of harmonic active power that the NLL returns to the power system. Similarly, from Table 5.8, it can be concluded that the VSAPF absorbs $P_H = 5.63\ kW$ of harmonic active power from the 7.85 kW of harmonic active power generated by the NLL. However, a substantial difference can be seen in the fundamental active power $P_1$ exchanged with the power system. Indeed, the passive damper absorbs only a minimal amount of fundamental active power from the power system, namely $P_1 = 0.03\ kW$, due to the passive damper´s resonant tank characteristics. In contrast, the active damper injects back 4.4 kW to the power system (as can be inferred from the value $P_1 = -4.4\ kW$) due to the harmonic active power recovery action. Moreover, in order to investigate the reduction on the fundamental power demanded by the end-user (i.e., industrial grid) to the power mains, Tables 5.9 and 5.10 are constructed from the results obtained in Table 5.2 to Table 5.5. In both tables, the first row shows the parameters of the power grid without compensation. It can be seen from Table 5.9 that with and without compensation, the RMS voltage at the PCC is around 230.08 V. Also, without compensation, the industrial facility draws RMS currents equal to $I_S$ = 501.65 A including the harmonic components. From Table 5.10, the $THD_V$ at the PCC without compensation is 8.21 % and the $THD_I$

**Table 5.8:** Components of the apparent power calculated for the passive damper and active damper amid their operation according to the Buchholz-Emmanuel power theory

| Quantity | Unit | Passive Damper | Active Damper |
|---|---|---|---|
| $S$ | kVA | 105.63 | 106.51 |
| $S_1$ | kVA | 0.54 | 4.38 |
| $P_1$ | kW | 0.03 | -4.38 |
| $Q_1$ | kVar | 0.54 | -0.08 |
| $P_H$ | kW | 5.97 | 5.65 |
| $Q_H$ | kVar | -0.38 | 0.37 |

**Table 5.9:** Comparative Evaluation - Losses over the grid impedance resistive part

| | $V_{PCC}$ RMS (V) | $I_S$ RMS (A) | $P_{Loss}$ over grid impedance (W) |
|---|---|---|---|
| No Compensation | 230.08 | 501.65 | 265.47 |
| Passive Damper | 230.04 | 484.11 | 268.64 |
| Active Damper | 230.03 | 474.15 | 260.66 |

**Table 5.10:** Comparative Evaluation - Harmonics Mitigation and Fundamental Power demanded

| | $S$ seen by the power mains (kVA) | $P_1$ demanded from the mains (kW) | $THD_V$ at PCC (%) | $THD_I$ at $I_S$ (%) |
|---|---|---|---|---|
| No Compensation | 346.27 | 293.87 | 8.21 | 60.43 |
| Passive Damper | 334.14 | 297.70 | 5.67 | 50.69 |
| Active Damper | 327.3 | 293.64 | 5.38 | 48.99 |

over the currents drawn from the mains ($I_S$) reaches the value of 60.43 %. Also, in the *No compensation* scenario, from the utility or power mains perspective, the industrial grid has an apparent power of 346.27 kVA and demands 293.87 kW of fundamental active power. Naturally, when the passive or active damper are connected to the system, the $THD_V$ at the PCC is reduced. The $THD_V$ is decreased to 5.67 % using the passive damper and to 5.38 % using the active damper. Similarly, the $THD_I$ on the current $I_S$ is reduced to 50.69 % using the passive damper and to 48.99 % using the active damper. Of course, as the passive and active damper provide a path of lower impedance in relation to the grid impedance, the harmonic content in the phase current $I_S$ is reduced and thus the RMS value is reduced, as can be seen in Table 5.9. In brief, both power filters decrease the RMS value of the phase currents $I_S$, the $THD_V$, and the $THD_I$ due to their harmonic mitigation capabilities. Consequently, the apparent power seen by the power mains is also reduced when any of the power filters are connected to the power system (see Table 5.10). This can be explained with the Buchholz-Emmanuel power theory, where the apparent power S can be expressed as (5.34), here rewritten for convenience:

$$S_{e\text{-}X} = S_{e1\text{-}X} \cdot \sqrt{1 + (THD_{I\text{-}X})^2 + (THD_{V\text{-}X})^2 + (THD_{V\text{-}X} \cdot THD_{I\text{-}X})^2} \qquad [V \cdot A] \quad (5.35)$$

From the latter equation, it can be seen clearly, that a reduction on the $THD_V$ and $THD_I$ will reduce the overall apparent power seen by the mains. Additionally, the power loss over the grid impedance or, differently said the power losses over the resistors $R_{Ga}$, $R_{Gb}$, $R_{Gc}$ depicted in Fig. 5.1 are reduced due to the action of the active damper. Nevertheless, the reduction in the power losses over the grid impedance is very small, only in the order of 5 W, as can be seen in Table 5.9. More important is the reduction of the fundamental active power $P_1$ demanded from the grid. In order to compare the reduction of fundamental active power demanded, the values of each column in Table 5.10 were normalized, taking as base the values of the *No compensation* scenario. The results of the normalization of the values in Table 5.10 can be seen in Table 5.11. The normalized table shows that the $THD_V$ is reduced by 30.88 % using the passive damper and by 34.41 % using the active damper. Likewise, the $THD_I$ on the $I_S$ currents is reduced by 16.13 % using the passive damper and by 18.94 % using the active damper. In effect, the grid impedance seen by the nonlinear load is modified by the action of the passive damper or active damper. On account of the nonlinear load behavior´s dependency on the grid impedance, the fundamental active power demanded increases by 1.3 % when the passive damper is used to suppress the resonance. On the other hand, when the active damper is used to suppress the resonance and due to the harmonic power recovery feature, the fundamental active power demanded by the end-user is reduced by 0.08 % compared with the *No Compensation* scenario. Of course, it can be argued that when it is necessary to install a power filter to solve resonance problems or to reduce the $THD_V$ at the PCC, an active damper equipped with harmonic active power recovery feature will

**Table 5.11:** Comparative Evaluation - Harmonics Mitigation and Fundamental Power demanded normalized against the No compensation scenario

| | $S$ seen by the power mains (%) | $P_1$ demanded from the mains (%) | $THD_V$ at PCC (%) | $THD_I$ at $I_S$ (%) |
|---|---|---|---|---|
| No Compensation | 100 | 100 | 100 | 100 |
| Passive Damper | 96.49 | 101.3 | 69.12 | 83.87 |
| Active Damper | 94.51 | 99.92 | 65.59 | 81.06 |

reduce the fundamental power demanded to the power mains in comparison with the passive damper. For the particular operating point simulated in this chapter, an overall reduction in the order of $1.3\% + 0.08\% \approx 1.4\%$ can be achieved in the fundamental active power demanded from the utility using the ultra-low losses active damper.

### 5.5.5 *Figures of merit for Power Quality Conditioners*

As can be seen in Table 5.10 and Table 5.11, the passive damper as power quality conditioner produces an increase on the fundamental power demanded from the power mains in comparison to the *No Compensation* scenario. On the other hand, the passive damper indeed decreases the $THD_V$ at the PCC and the $THD_I$ on the supply currents compared to the *No Compensation* scenario. Therefore, it may be inferred that there is a trade-off between fundamental active power reduction and harmonic distortion reduction that a particular power filter can achieve. Interestingly, there is a similar trade-off on unipolar devices in the semiconductor world. For example, in unipolar MOSFETs there is a trade-off between the $R_{ds,on}$ and the output capacitance $C_{OSS} = C_{DS} + C_{GD}$ of the device. Both quantities depend on the chip's area of the semiconductor device. On the one hand, the $R_{ds,on}$ is inverse proportional to the area of the semiconductor. On the other hand, the capacitance $C_{OSS}$ is directly proportional to the area of the semiconductor and it plays an important role in the switching losses as seen in (3.9). Thus, there is an inherent trade-off between switching and conduction losses concerning the semiconductor chip's area. On account of this, semiconductor manufacturers have proposed the FOM $R_{ds,On} \cdot Q_{OSS}$ as metric to compare different devices and evaluate the trade-off between switching losses and conduction losses [192, 193]. Of course, the output charge $Q_{OSS}$ is related with the output capacitance according to the relationship $Q_{OSS} = 2 \cdot C_{OSS} \cdot \sqrt{V_{DS} \cdot V_{DS,ref}}$ [194]. Actually, it is possible to borrow this concept of FOM from the semiconductor world and apply it to power quality conditioners. Thus, in order to quantify the trade-off between harmonics mitigation and reduction in the fundamental power demanded, the following figures-of-merit are proposed to evaluate the performance of a particular power filter:

$$FOM_{Filter1} = P_1 \cdot THD_V \tag{5.36}$$

$$FOM_{Filter2} = P_1 \cdot THD_I \tag{5.37}$$

Moreover, with information written in Table 5.10, the proposed FOMs are calculated for the three simulated scenarios and the results are presented in Table 5.12. Again, and for an easier comparison, the values written in Table 5.12 are normalized against the values of the *No Compensation* scenario. The results of this last normalization can be seen in Table 5.13. From the table, it may be inferred that if the reduction on the fundamental power demanded and reduction on the $THD_V$ must be considered at the same time, the

**Table 5.12:** Comparative Evaluation - FOM for the different power quality conditioners

| | $P_1$ demanded to the mains (kW) | $THD_V$ at PCC (%) | $THD_I$ at $I_S$ (%) | $FOM_{Filter1}$ $P_1 \cdot THD_V$ $(kW \cdot \%)$ | $FOM_{Filter2}$ $P_1 \cdot THD_I$ $(kW \cdot \%)$ |
|---|---|---|---|---|---|
| No Compensation | 293.87 | 8.21 | 60.43 | 24.13 | 177.61 |
| Passive Damper | 297.70 | 5.67 | 50.69 | 16.9 | 150.91 |
| Active Damper | 293.64 | 5.38 | 48.99 | 15.81 | 143.86 |

**Table 5.13:** Comparative Evaluation - Normalized FOM for the different power quality conditioners against the no compensation scenario

| | $P_1$ demanded to the mains (%) | $THD_V$ at PCC (%) | $THD_I$ at $I_S$ (%) | $FOM_{Filter1}$ $P_1 \cdot THD_V$ (%) | $FOM_{Filter2}$ $P_1 \cdot THD_I$ (%) |
|---|---|---|---|---|---|
| No Compensation | 100 | 100 | 100 | 100 | 100 |
| Passive Damper | 101.3 | 69.06 | 83.88 | 70.04 | 84.97 |
| Active Damper | 99.92 | 65.53 | 81.07 | 65.52 | 81 |

$FOM_{Filter1}$ and $FOM_{Filter2}$ are a better metric to compare power quality conditioners. For instance, if the $P_1 \cdot THD_V$ metric is used for the comparison, it can be concluded that the passive damper brings a 29.96 % improvement compared to the *No Compensation* scenario. By the same metric, the active damper is even better because the active damper brings a 34.48 % improvement compared with the *No Compensation* scenario. Of course, the active damper outperforms the passive damper by a 4.52 % in terms of the $FOM_{Filter1}$. Similarly, if the $FOM_{Filter2}$ is observed in Table 5.13, it can be seen that the active damper also outperforms the passive damper judging by the second metric $FOM_{Filter2}$. In brief, the active damper with ultra-low losses improves the harmonic distortion and, at the same time, reduces the fundamental active power demanded. In contrast, the passive damper only reduces the harmonic voltage distortion but increases the fundamental active power demanded by the end-user. For this reason, the passive damper exhibits worse $FOM_{Filter1}$ and $FOM_{Filter2}$ than the active damper.

## 5.6 CHAPTER SUMMARY

This chapter presented the power balance flow study of an distribution power system (e.g., industrial grid) with an ultra-low losses active damper operating as power quality conditioner. Specifically, the examination of the power exchange under non-sinusoidal conditions among the elements was carried out according to the Buchholz-Emmanuel power theory. This particular theory was selected because it highlights and recognizes the importance of the fundamental active power and harmonic active power on the overall power balance flow. Although it was not possible to derive a final analytical solution due to the nonlinear characteristics exhibit by the nonlinear load considered, numerical solutions backed by computer simulations were obtained. In fact, two computer simulations were carried out considering first a passive damper and later an active damper. Indeed, the computer simulations provided metrics of the power filters' performance as harmonic

voltage distortion, harmonic current distortion and apparent power seen by the mains. In addition, the computer simulation results were also used for examination of the power exchanged among the elements in the simulated system. Specifically, the power balance flow in the power system was studied considering the fundamental active power and the harmonic active power at each node of the simulated system. Indeed, the numerical simulation results support the case of this PhD thesis because the results demonstrate that it is possible to reduce the harmonic distortion and the power consumption in an industrial facility using an ultra-low losses active damper. In particular, for the distribution power system studied, it was possible to reduce the $THD_V$ by 2.83 % and the fundamental active power demanded to the grid by 1.4 % using the ultra-low losses active damper instead of the passive damper. Furthermore, it was found that when a power filter is used as a resonance damper, there is a trade-off between harmonic distortion reduction and fundamental active power reduction. In order to take into account both effects and compare the power quality conditioners fairly, two FOMs were proposed in this chapter. Both FOMs consider at the same time the capabilities of a particular resonance damper to reduce harmonic distortion and the fundamental power demanded to the power mains. According to the first FOM $P_1 \cdot THD_V$, for the distribution power system studied, the active damper outperforms in 4.52 % the passive damper. Finally, according to the second FOM $P_1 \cdot THD_I$, the active damper outperforms in 3.97 % the passive damper for the power system simulated in this chapter.

# 6

# Ultra-low losses active damper: Power Circuit Topologies

From chapter 4 it can be concluded that harmonic power recovery through an active damper is enabled by an ultra-low losses SAPF solution. Also, in chapter 3, it was made clear that SiC semiconductor technology outperforms Si technology regarding switching and conduction losses. Consequently, if the goal is to recover a significant amount of harmonic active power, it is straightforward to design the SAPF's power circuit with SiC semiconductors. However, the question that naturally arises is which one is the best power topology for the active damper. Put another way, the question is which is the active damper´s power topology that produces the lowest power losses amid the harmonic resistance emulation. In order to answer this question, this chapter delves into the investigation of different SiC based power circuit topologies for the active damper. In particular, the power topologies investigation covers conventional topologies, namely the two-level (2L), three-level T-type (3L-TNPC), and three-level neutral point clamped (3L-NPC) power circuits, all of them entirely SiC based. In addition, the investigation also includes a non-conventional topology proposed in this chapter: the SiC based asymmetrical three-level power circuit. This chapter essentially analyses the power losses produced by each power topology and performs a comparative evaluation of the power losses and efficiency figures obtained. Arising out of the comparative evaluation, the SiC based non-conventional topology proposed in this chapter seems to be a very promising power circuit topology for the active damper. Indeed, the proposed topology has power losses smaller than the power losses produced by conventional all-SiC 2L and 3L topologies for switching frequencies above 60 kHz. Further, for high current ratings, the proposed topology has the advantage that it can be built just by cascading two half-bridge power modules. The findings presented in this chapter were also published in:

- R. Guzman Iturra and P. Thiemann, "A Simple SiC MOSFET Three Level Inverter Topology for High Performance Shunt Active Power Filter," in 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe), 2 – 6 September, 2019, Genova – Italy.

- R. Guzman Iturra and P. Thiemann, "Asymmetrical Three-Level Inverter SiC-Based Topology for High Performance Shunt Active Power Filter," Energies, vol. 13, no. 1, p. 141, Dec. 2019.

## 6.1 INTRODUCTION

Nowadays, there is a steadily increasing demand for highly efficient and intelligent converter solutions in many energy-related applications. SAPFs, like many other power converters for power conditioning systems, must exhibit high compactness, acceptable EMI behavior, and low high-frequency harmonics besides low power losses. Currently, the design of compact and highly efficient power converters with the features described above is made following basically two approaches. The first approach uses multilevel converter topologies based on silicon semiconductors (IGBTs and diodes), and the second uses two-level circuits with WBG semiconductors. Actually, multilevel converters exhibit high efficiency at high switching frequencies mainly for two reasons. First, multilevel converters provide reduced switching losses at high switching frequencies since the semiconductors only need to block a fraction of the complete DC-Bus voltage. Second, the ripple filter losses are also reduced in multilevel converters. Because the AC filter size is reduced due to the reduced ripple produced by the different voltage levels available at multilevel converters' output terminals [99, 102, 104]. Furthermore, the second approach uses modern wide band gap (WBG) semiconductors such as SiC MOSFETs [122]. This technology offers significant technical advantages due to the unipolar semiconductor concept as was discussed in chapter 3. Consequently, simple full SiC MOSFET two-level converter structures with high switching frequency and reduced AC filter size achieve efficiencies comparable or superior to pure silicon-based multilevel converters [99, 124]. Certainly, the combination of multilevel circuit structures and SiC MOSFETs will lead to power converters with the highest efficiency and power density. This trend will be seen in the near future for applications requiring the highest performance. In fact, research carried out over the last three years has studied full SiC MOSFET based three-level (3L) three-phase converters for motor drives [195], grid-tie converters [196], and more electrical aircraft applications [197]. These studies have evaluated and compared the two-level (2L) (see Fig. 6.1 **a)**), three-level neutral point piloted or T-Type (3L-TNPC) (see Fig. 6.1 **b)**) and the three-level neutral point clamped (3L-NPC) (see Fig. 6.1 **c)**) topologies all SiC based. Arising out of these investigations, it was found that the T-Type circuit implementation produces the highest efficiency for the mentioned applications.

On this basis, this chapter proposes and analyzes a non-conventional three-level topology, namely the three-level asymmetrical topology, based entirely on silicon carbide (SiC) semiconductors as VSAPF's power circuit. However, it is important to emphasize that according to the literature review carried out, some key ideas of this non-conventional topology have been proposed already in [198, 199] for silicon IGBT-based PFC rectifier systems and in [200] for single-phase SAPFs. Indeed, these studies focused entirely on the design of inner current controllers, DC-Bus voltage balancing and digital control implementation. Furthermore, only reference [198] analyzed the topology's switching states. However, the latter analysis was made only for the single-phase Power Factor Correction (PFC) circuit built with silicon IGBTs and diodes. Actually, to the best of the author's knowledge, such topology has not been studied in three-phase SAPF nor as circuit topology built with SiC semiconductors. Therefore, this chapter extends the body of knowledge by analyzing the switching states and current commutations during transitions of the SiC-based asymmetrical topology. These are very different from those seen in the topology with silicon IGBTs due to the third quadrant characteristic of SiC MOSFET devices. In addition, in this chapter, the proposed topology is compared against other full-SiC-based conventional topologies in terms of efficiency and power losses. Truly, this comparison has not previously been carried out in the literature. In sum, this

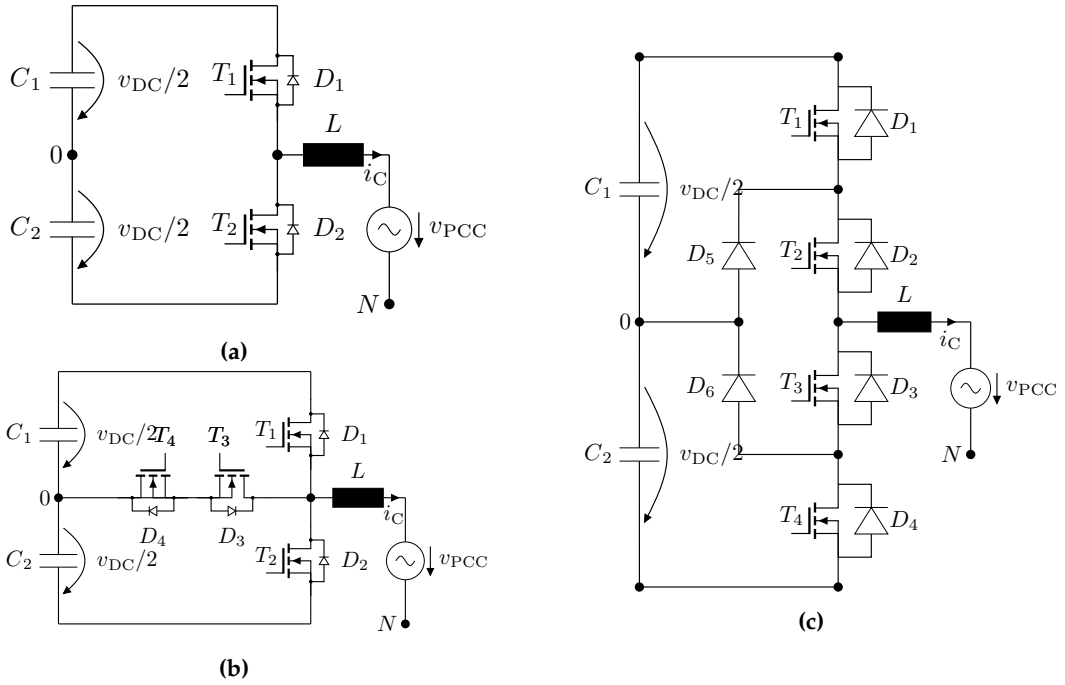


**Fig. 6.1:** Schematics of conventional converter topologies. Just one leg of the three phase converter is shown in all cases. (**a**) Two level (2L) topology. (**b**) Three level neutral-point piloted (3L-TNPC) or 3L T-Type topology. (**c**) Three level neutral-point clamped (3L-NPC).

chapter profoundly discusses the non-conventional topology power losses and efficiency and compares it against conventional 2L and 3L full-SiC-based topologies.

## 6.2 ASYMMETRICAL THREE LEVEL CONVERTER TOPOLOGY (3L-ASYM)

Fig. 6.2 shows one leg of the three-phase 3L non-conventional topology proposed as power circuit for the VSAPF. The non-conventional topology is named in this chapter as an asymmetrical three-level converter (3L-ASYM) for reasons that will become clear in subsection 6.2.3. It can be seen in Fig. 6.2 that the DC-Bus is constituted by two capacitors connected in series. Also, the neutral point arises from this series connection, located at the middle point of the DC-Bus. Furthermore switches *T1-T4* are selected to be SiC MOSFETs and the diodes *D1-D4* are selected to be SBD. Indeed, one advantage of the 3L-ASYM power circuit is that it can be constructed using only two-level commutation cells in a cascade connection. Differently said, the proposed topology can be built by cascading two SiC half-bridge modules, connecting the AC terminal of one module to the positive terminal of the second module.

### 6.2.1 *VSAPF's Control System for Three-level power circuits*

The VSAPF control system for the case of a three-level power circuit is depicted in Fig. 6.3. The control system in Fig. 6.3 has four main components. Specifically, two outer loops, one inner current control loop, and one DC-side voltage equalizer. The former three components are similar to the control system for the two-level VSAPF presented in section 4.3. Notice that three-level converters exhibit a voltage divider in their DC-side due to the capacitors in series. These DC-bus´s capacitors are subject to suffer from the

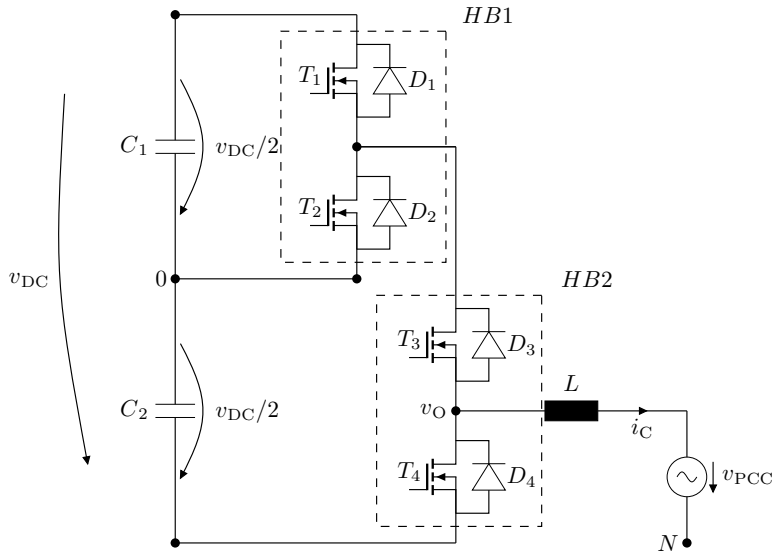


**Fig. 6.2:** Configuration of the proposed 3L asymmetrical topology (just one leg of the three phase converter is shown). One leg is formed by employing four controlled switches using a cascade connection of two single phase half-bridges (HB)

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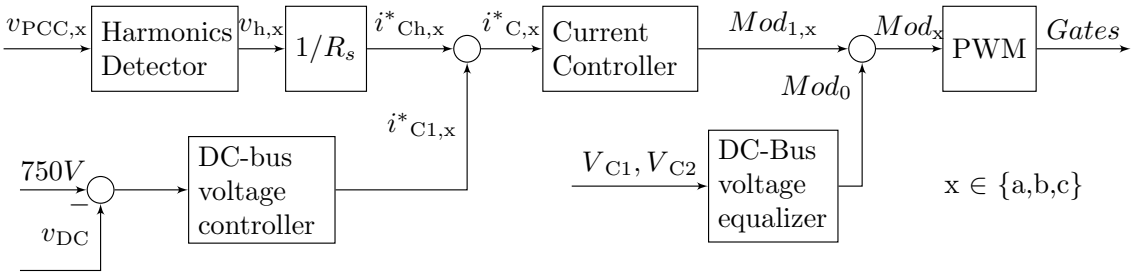


**Fig. 6.3:** Control system of the Shunt Active Power Filter based on voltage detection (VSAPF) with a three-level power circuit. Simplified block diagram.

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partial DC-side voltage drift phenomenon. The latter occurs when the voltage of both of the capacitors becomes unbalanced [170, 199]. Therefore, a DC-side voltage equalizer in the control system becomes necessary in three-level converters to maintain the voltage of the DC-Bus capacitors symmetric during operation through active adjustments of the duty cycles.

### 6.2.2 *Switching states 3L-ASYM topology*

On Fig. 6.2, the node that is taken as reference for the analysis of the output voltage formation is the neutral point *o*. Obviously, the potential of the positive rail *p* becomes $v_{DC}/2$ and the potential of the negative rail *n* becomes -$v_{DC}/2$. The voltage $v_o$ is defined as the output voltage. If *T1* and *T3* are switched ON, the output voltage takes the $v_{DC}/2$ potential. On the latter state, the *T2*'s voltage is half of the DC-Bus voltage $v_{DC}/2$ and the stress across *T4* is the full DC-Bus voltage $v_{DC}$. If *T2* and *T3* are ON, the output voltage takes the *o* potential. The voltage stress across *T1* is half of the DC-Bus voltage $v_{DC}/2$ and the stress across *T4* is also $v_{DC}/2$. If *T2* and *T4* are ON and *T3* is OFF, the output voltage assumes -$v_{DC}/2$ potential. The voltage stress across *T1* is half of the DC-Bus

voltage $v_{DC}/2$ and the stress across $T3$ is also $v_{DC}/2$. All the switching states of the VSAPF proposed topology can be seen in Table 6.1 and a summary of the voltage stress on the different switches can be seen in Table 6.2. From Table 6.2, it can be inferred that all the power switches with the exception of T4 and D4 have to be selected with a blocking voltage capability of half of the DC-Bus voltage. On the other hand, T4 and D4 have to be rated to sustain the complete DC-Bus voltage. Moreover when the switch $T1$ is ON, it is absolutely mandatory that the switch $T2$ is OFF. Otherwise shoot-through occurs in the capacitor $C_1$. Likewise, when the switch $T2$ is ON, it becomes necessary to command the switch $T1$ to OFF state. It is granted that when $T1$ or $T2$ are switched on, a blanking time becomes necessary in the same way as in two-level commutation cell. The same happens on the power switches $T3$ and $T4$ in order to avoid shoot-through of the capacitor $C_2$. Furthermore, level-shifted PWM modulation can be used as a modulation method for the proposed non-conventional, the 3L-TNPC and 3L-NPC topologies. In this modulation variant, the modulating signal *(Mod)* is compared with two high frequency triangular waveforms (*Vtri1* and *Vtri2*). Fig. 6.4 shows the behavior of the level-shifted PWM for the asymmetrical topology when the modulating signal is purely sinusoidal. It can be seen that the switches T1 and T2 change their only states during the positive semi-cycle of the modulating signal. In addition, during this positive semi-cycle, the switch T3 is continuously on. Conversely, during the negative semi-cycle, the switches T3 and T4 change their states, and the switch T2 is continuously on.

### 6.2.3 *Voltage levels generation and output current in the 3L -ASYM*

For the given topology, it is important to ensure that any desired output voltage, namely voltages $v_{DC}/2$, 0 , or $-v_{DC}/2$ can be generated for positive and negative currents. In other words, irrespective of the direction of the current, it should be possible to select any of the three levels at the output port. For example for $i_C > 0$, in order to connect the AC output port ($v_o$) of the converter to $v_{DC}/2$, the semiconductors $T1$ and $T3$ should carry the output current. In contrast, to generate an output voltage $o$ at the AC output port for $i_C > 0$, the semiconductors $T2$,$D2$ and $T3$ should carry the current. On the other hand, to connect the ac output port to $-v_{DC}/2$, for $i_C > 0$, the semiconductors $T4$ and $D4$ should carry the current. Arising out of this, the proposed non-conventional topology is

**Table 6.1:** Switching States for the 3L-ASYM topology

| Switching state | $T_1$ | $T_2$ | $T_3$ | $T_4$ | Output Voltage |
|---|---|---|---|---|---|
| $p$ | 1 | 0 | 1 | 0 | $v_{DC}/2$ |
| $o$ | 0 | 1 | 1 | 0 | 0 |
| $n$ | 0 | 1 | 0 | 1 | $-v_{DC}/2$ |

**Table 6.2:** Voltage stress across the switches for the 3L-ASYM topology at different switching states

| Switching state | Stress across T1/D1 | Stress across T2/D2 | Stress across T3/D3 | Stress across T4/D4 |
|---|---|---|---|---|
| $p$ | - | $v_{DC}/2$ | - | $v_{DC}$ |
| $o$ | $v_{DC}/2$ | - | - | $v_{DC}/2$ |
| $n$ | $v_{DC}/2$ | - | $v_{DC}/2$ | - |

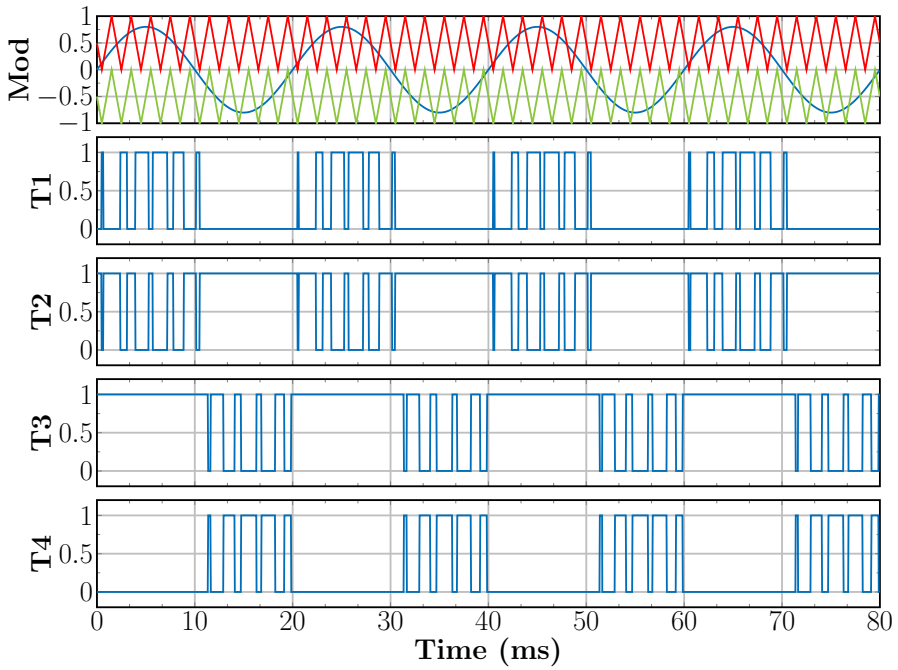


**Fig. 6.4:** PWM Generation waveforms. From top to bottom: reference voltage: modulation signal (blue), Triangular Carrier Signal 1 *Vtri1* (red), Triangular Carrier Signal 2 *Vtri2* (green). Gating signal for switch T1. Gating signal for switch T2. Gating signal for switch T3. Gating signal for switch T4

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named in this chapter as asymmetrical three level converter topology. Because there is an asymmetry on the number of semiconductors carrying the current at different output voltage levels. The details of the current commutations on each of the semiconductors in the different converter states will be discussed in the following subsections.

#### 6.2.3.1 *3L ASYM Commutation p - o for positive current*

Fig. 6.5 shows the transition between *o-p* for a positive current ($i_C > 0$). During the switching state *o*, the positive current flows out of the neutral point *o* through the diode *D2*, the transistor *T2* and the transistor *T3*. In this switching state the channel of *T2* is open and allows a reverse current (current flow from source to drain) to pass through the SiC MOSFET switch *T2*. This conduction mode is called third quadrant operation of the SiC MOSFET [201, 202]. Moreover, the current $i_C$ will be distributed between the SiC MOSFET T2 and the SBD diode D2. The current distribution depends on the on-resistance ($R_{ds,on}$) of the MOSFET, the forward voltage drop of the SiC SBD diode ($V_{fd}$) and the SiC SBD dynamic resistance ($R_{fd}$) [203]. Indeed the described switching operation is very different from what is seen in the three-level silicon based topology. The voltage blocked by *T1*,*D1*,*T4* and *D4* at this state is $v_{DC}/2$. During the blanking time interval between *T1* and *T2*, the current passes entirely through the diode *D2* and the transistor *T3*. Then, the converter is brought to the switching state *p* by turning the switch *T1* ON. The current conmutates from *D2* to *T1*. At this stage *T2* and *D2* block half of the DC-bus voltage and the semiconductors *T4* and *D4* block the full DC-Bus voltage. It has to be pointed out that SiC SBDs exhibit almost zero reverse current [204] which means that the increase in switching losses due to the current commutation from SBDx to Tx can be neglected at all times.

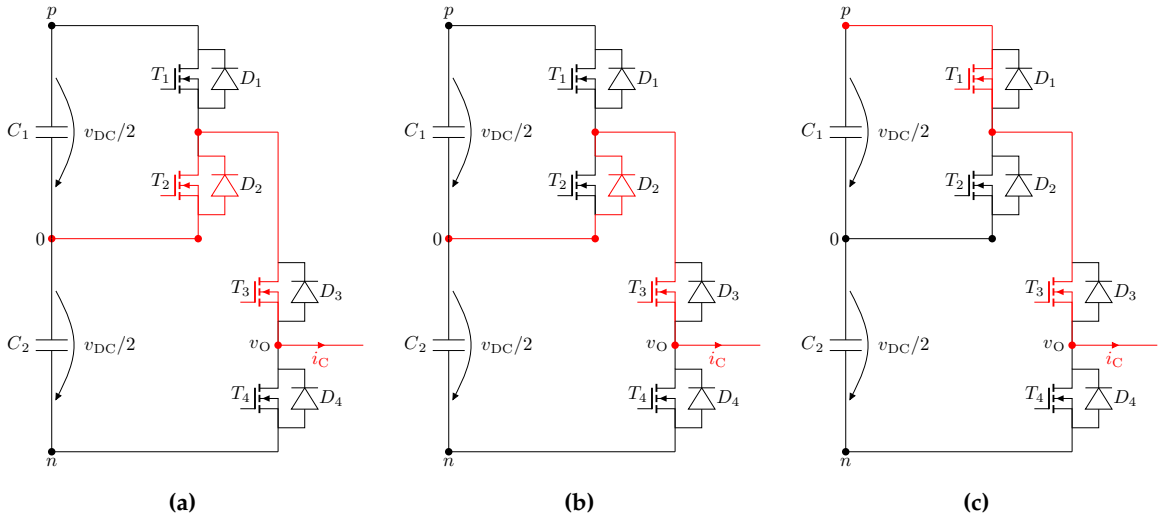



**Fig. 6.5:** Current commutation, transition from switching state *o* to *p* for $i_C > 0$. Current flow depicted in red. (**a**) Switching state *o*. (**b**) Blanking time (between T1 and T2) interval. (**c**) Switching state *p*.

#### 6.2.3.2 *3L ASYM Commutation p - o for negative current*

Fig. 6.6 shows the transition *o-p* for a negative compensating current ($i_C < 0$). At the switching state *o*, the current flows through *T2*,*T3*, and *D3*. The former two share the compensating current as *T3* operates in third quadrant. The devices *T1*,*D1*,*T4* and *D4* block half the DC-Bus voltage. During the blanking time between *T1* and *T2*, the diode *D1* conducts the current alongside with *T3* and *D3*. *T2* and *D2* hold the half of the DC-Bus voltage. In contrast *T4* and *D4* sustain the complete DC-Bus voltage. Finally once the blanking time has elapsed and the transistor *T1* is fully ON, the current passes through *T1*,*D1*,*T3* and *D3* with *T1* and *T3* in third quadrant operation. The devices *T2*,*D2*,*T4* and *D4* block the same voltage as previously stated. At this stage the transistor *T1* is turned on at almost Zero Voltage Switching (ZVS) [205, 206]. This comes inherently because

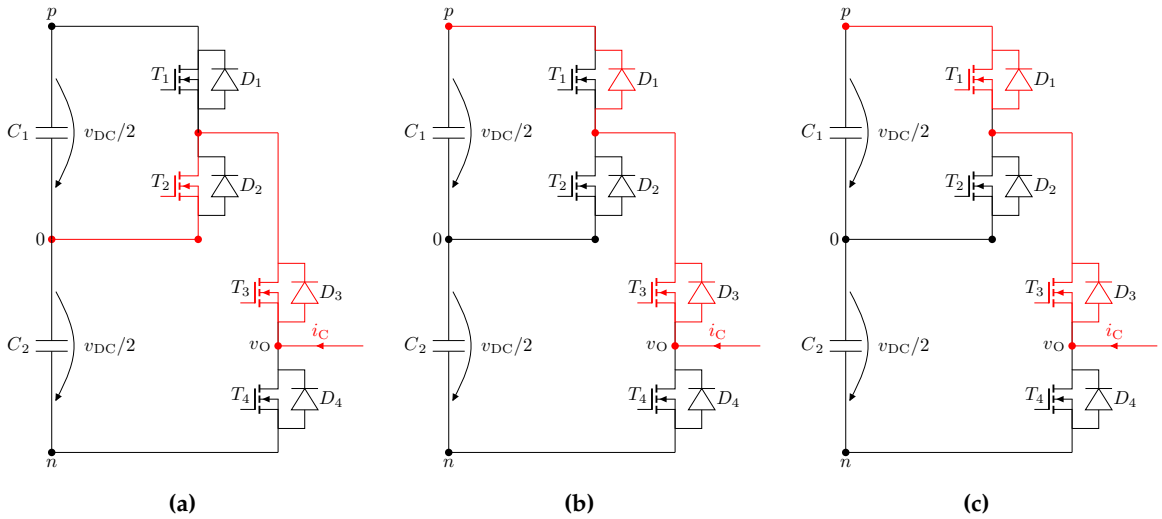



**Fig. 6.6:** Current commutation, transition from switching state *o* to *p* for $i_C < 0$. Current flow depicted in red. (**a**) Switching state *o*. (**b**) Blanking time (between T1 and T2) interval. (**c**) Switching state *p*.

the diode *D1* has been conducting the current since the beginning of the blanking time interval. The effective blocking voltage at the time of the switching ON transition of *T1* is just the voltage drop produced by $i_C$ over *D1* which is remarkable smaller than half of the DC-Bus voltage. Therefore, it is possible to say that *T1* is turned on partially at soft-switching, and this comes inherently due to the circuit nature. Therefore, there is no need for a special control loop or further control considerations to achieve partial soft-switching.

#### 6.2.3.3 *3L ASYM Commutation n - o for positive current*

Fig. 6.7 presents the transition *o-n* for a positive compensating current ($i_C > 0$). The semiconductors behavior for state *o* is the same as the one described in subsection 6.2.3.1. During the blanking time interval between *T3* and *T4*, the current commutates from *T2*/*D2* to the diode *D4*. As *T2* is in conduction state, *T1*,*D1* and *T4* block just half of the DC-Bus voltage. Finally the commutation concludes by turning *T4* ON almost at ZVS. As this point *T4* operates in third quadrant and $i_C$ is shared between *T4* and *D4*. *T1*,*D1* and *T4* block the same voltage as in the blanking time interval.

#### 6.2.3.4 *3L ASYM Commutation n - o for negative current*

Fig. 6.8 depicts the behavior of the *n* - *o* transition for $i_C < 0$. The switching state *o* transition is identical to the *o* state described in subsection 6.2.3.2. All along the blanking time interval between *T3* and *T4*, $i_C$ flows across *T2* and *D3*. *T1*,*D1*,*T4* and *D4* block just half of the DC-Bus voltage. In the final stage of the transition the switch *T4* is switched ON and the current commutates from *D3* to *T4*. As *T2* is in conduction state, *T1*,*D1*,*T3*,*D3* and *D4* block just half of the DC-Bus voltage.

## 6.3 POWER CIRCUIT DESIGN

SiC semiconductors can drastically reduce power losses due to lower switching losses, almost no reverse recovery, lower on-resistance, and lower gate charge compared with

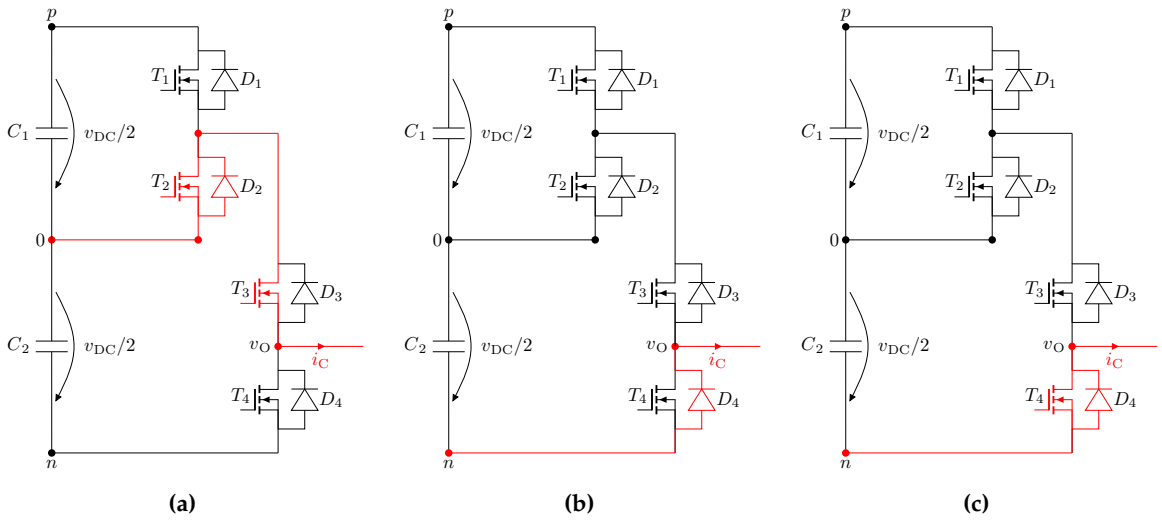



**Fig. 6.7:** Current commutation, transition from switching state *o* to *n* for $i_C > 0$. Current flow depicted in red. (**a**) Switching state *o*. (**b**) Blanking time (between T3 and T4) interval. (**c**) Switching state *n*.

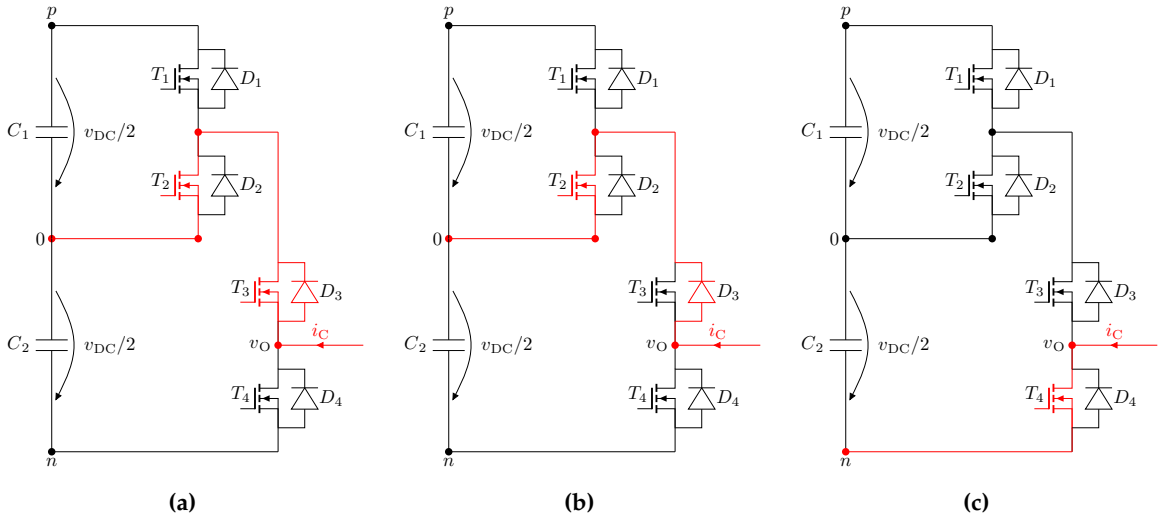



**Fig. 6.8:** Current commutation, transition from switching state *o* to *n* for $i_C < 0$. Current flow depicted in red. (**a**) Switching state *o*. (**b**) Blanking time (between T3 and T4) interval. (**c**) Switching state *n*.

their pure silicon counterparts [123]. However, to benefit from the SiC technology at the system level, the overall converter power losses (i.e. losses in semiconductors, inductors, ripple filter, etc.) should be minimized using the different degrees of freedom available for the design. Of course, there are many degrees of freedom in the design of a power converter. These degrees of freedom are circuit topology, modulation scheme, current ripple on the coupling inductors, switching frequency, etc. Additionally, different components and technologies can be selected to construct a particular power converter. The components's selection embraces decisions about the core material for the inductors, solid or Litz wire for the inductor windings, and power switches. Moreover, in order to compare the three-level topologies, a three-phase VSAPF with a power rating of 23.1 kVA (rated compensating current $I_C$ of 33.5 A) was designed and simulated. The reason is because PLECS models for 900 V/40 A SiC power switches where available directly from semiconductor manufacturers. On the contrary, PLECS models for switches rated at 900 V and currents higher than 40 A were not available at the time that this chapter was written. Although the power rating of the three-phase VSAPF designed in this chapter is smaller than the power rating of the VSAPF presented in Chapter 4.5 (100 kVA), it can be argued that the figures of power losses and efficiency will have a similar behavior. According to the literature, the design of power electronics systems in the range of 10 to 100 kVA exhibit similar efficiency figures [4]. For this reason, many universities and institutes design prototypes with small ratings at a reasonable cost and extrapolate their results to bigger power ratings up to 100 kVA. The latter can be seen in many scientific papers such as [31] and [99]. With this in mind, four different 23.1 kVA VSAPFs were designed using the circuit topologies 2L, 3L-TNPC, 3L-NPC, and 3L-ASYM considering a DC-bus voltage of 750 V, also $v_{DC}$ equal to 750 V. Actually, the semiconductors considered are discrete SiC MOSFETs and SBD which can be seen in Table 6.3. Moreover, the simulation software used for the power circuit, control system, thermal and power converter losses estimation is Simulink-PLECS as in chapter 4.5. In any case, the PLECS models of all the semiconductors stated in Table 6.3 were gathered from the official website of the manufacturer Wolfspeed [207].

**Table 6.3:** Parameters of the power semiconductors used in the comparative evaluation of the two-level and three-level power converters

| Topology | Component | Semiconductor Part | $V_{DS,Max}$ (V) | $I_{D,rated}$ (A) | $R_{ds,on}(m\Omega)$ $T_J$=175°C | $E_{Total}$ (mJ) $V_{DS}$=800 V |
|---|---|---|---|---|---|---|
| 2L | T1 | C2M0025120D | 1200 | 37 | 43 | 2.4 |
| | T2 | C2M0025120D | 1200 | 37 | 43 | 2.4 |
| | D1 | C4D30120D | 1200 | 43 | 110 | ≈0 |
| | D2 | C4D30120D | 1200 | 43 | 110 | ≈0 |
| 3L-TNPC | T1 | C2M0025120D | 1200 | 37 | 43 | 2.4 |
| | T2 | C2M0025120D | 1200 | 37 | 43 | 2.4 |
| | T3 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T4 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | D1 | C4D30120D | 1200 | 43 | 110 | ≈0 |
| | D2 | C4D30120D | 1200 | 43 | 110 | ≈0 |
| | D3 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D4 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| 3L-ASYM | T1 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T2 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T3 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T4 | C2M0025120D | 1200 | 37 | 43 | 2.4 |
| | D1 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D2 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D3 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D4 | C4D30120D | 1200 | 43 | 110 | ≈0 |
| 3L-NPC | T1 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T2 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T3 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | T4 | C3M0030090K | 900 | 30 | 37 | 0.66 |
| | D1 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D2 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D3 | C3D20065D | 900 | 26 | 89.8 | ≈0 |
| | D4 | C3D20065D | 900 | 26 | 89.8 | ≈0 |

## 6.4 COUPLING INDUCTORS DESIGN

GeckoMagnetics is the software used to design the coupling inductors and to calculate the inductors' power losses. To this end, the input given to GeckoMagnetics is the coupling inductor current spectrum obtained from the Simulink-PLECS simulation. The latter is done to have the same operating point in both simulation tools. Furthermore, the coupling inductors were designed according to a defined maximum current ripple in all the designs. If the maximum ripple is defined as $\Delta I_{pp}$, then the minimum inductance necessary to achieve $\Delta I_{pp}$ in a two-level converter can be calculated according to (3.12) which is here rewritten for the sake of convenience [35, 208, 209]:

$$L_{2L} = \frac{V_{DC}}{8 \cdot f_{Sw} \cdot \Delta I_{pp}} \tag{6.1}$$

Recall that $f_{Sw}$ stands for the switching frequency of the power converter. Therefore, the last equation implies that the inductance of the coupling inductor decreases as the

switching frequency increases. Moreover, if a three-level converter is designed in such a way that the same maximum current ripple $\Delta I_{pp}$ as in a two-level converter is to be obtained, the following applies [210, 211]:

$$L_{3L} = \frac{2 \cdot L_{2L}}{3} \tag{6.2}$$

With this in mind, the maximum current ripple was fixed at 20% of the rated current $\Delta I_{pp} = I_n \cdot (20\%) \cdot 2 = 13.4\ A$ and the $f_{Sw}$ was used as system's design parameter to maximize the overall efficiency of the VSAPF. The topologies were compared at different switching frequencies ranging from 10 to 120 kHz, and the inductors were sized according to (6.1) and (6.2) such that the maximum ripple was maintained at 13.4 A in all designs. Furthermore, the inductors were designed considering iron powder for the magnetic core. Specifically, cores made of high flux material on a toroidal shape from Magnetic Inc. were used for the magnetic's design. Furthermore, the inductors were designed using the area product method with the enhancements introduced by Hurley and Wölfle in [136] to select the core with the optimum effective permeability ($\mu_{r,opt}$):

$$\mu_{r,opt} = \frac{B_{Sat} \cdot l_C \cdot K_i}{\mu_o \sqrt{\frac{P_{Cu,max} \cdot N_L \cdot A_W}{\rho_W \cdot MLT}}} \tag{6.3}$$

Where $B_{Sat}$ is the maximum magnetic flux density of the powder iron material (1.5 T), $l_C$ is the length of the magnetic path of the toroidal core, and $K_i$ is the current crest factor. Furthermore, $P_{Cu,max}$ is the maximum dissipation possible in the inductor windings, $N_L$ is the number of winding turns, and $MLT$ is the Mean Length Turn (MLT). Finally, $\rho_W$ is the resistivity of the conductor and $\mu_o = 4 \cdot \pi \cdot 10^{-}7\frac{H}{m}$ is the free space's permeability. Regarding the inductor's windings, the conductor's section used in all designs is 3.2 $mm^2$ corresponding to AWG 8. The summary of the inductors design for the two-level and three-level converters at different $f_{Sw}$ can be seen in Tables 6.4 and 6.5 respectively. Furthermore, the inductor values for the two-level and three-level converters as function of the switching frequency can be seen in Fig. 6.9 **a)**. On the same note, the inductors' volume as a function of the switching frequency can be seen in Fig. 6.9 **b)**.

**Table 6.4:** Inductor design for the two-level (2L) converter

| $f_{Sw}$ (kHz) | L Desired ($\mu$H) at 50 A | $\mu_{r,opt}$ | Part Number Magnetics | $N_L$ (Turns) | L Achieved ($\mu$H) at 50 A |
|---|---|---|---|---|---|
| 10 | 650 | 40 | 58338 | 99 | 640 |
| 20 | 325 | 60 | 58339 | 53 | 321 |
| 30 | 217 | 60 | 58099 | 65 | 223 |
| 40 | 163 | 60 | 58099 | 49 | 167 |
| 50 | 130 | 60 | 58777 | 30 | 132 |
| 60 | 108 | 60 | 58777 | 26 | 108 |
| 70 | 93 | 60 | 58907 | 44 | 96 |
| 80 | 81.25 | 60 | 58867 | 50 | 85 |
| 90 | 72 | 60 | 58072 | 28 | 78 |
| 100 | 65 | 60 | 58072 | 25 | 68 |
| 110 | 59 | 60 | 58617 | 19 | 56 |
| 120 | 54 | 60 | 58617 | 18 | 51 |

**Table 6.5:** Inductor design for the three-level (3L) converters

| $f_{Sw}$ (kHz) | L Target ($\mu$H) at 50 A | $\mu_r$ | Part Number Magnetics | $N_L$ (Turns) | L Achieved ($\mu$H) at 50 A |
|---|---|---|---|---|---|
| 10 | 429 | 40 | 58338 | 77 | 425 |
| 20 | 215 | 60 | 58099 | 64 | 216 |
| 30 | 143 | 60 | 58737 | 31 | 140 |
| 40 | 107 | 60 | 58907 | 50 | 108 |
| 50 | 86 | 60 | 58907 | 43 | 86 |
| 60 | 72 | 60 | 58617 | 22 | 69 |
| 70 | 61 | 60 | 58617 | 20 | 60 |
| 80 | 54 | 60 | 58617 | 19 | 56 |
| 90 | 48 | 60 | 58617 | 18 | 47 |
| 100 | 43 | 60 | 58110 | 32 | 43 |
| 110 | 39 | 60 | 58110 | 27 | 38 |
| 120 | 36 | 60 | 58110 | 26 | 36 |

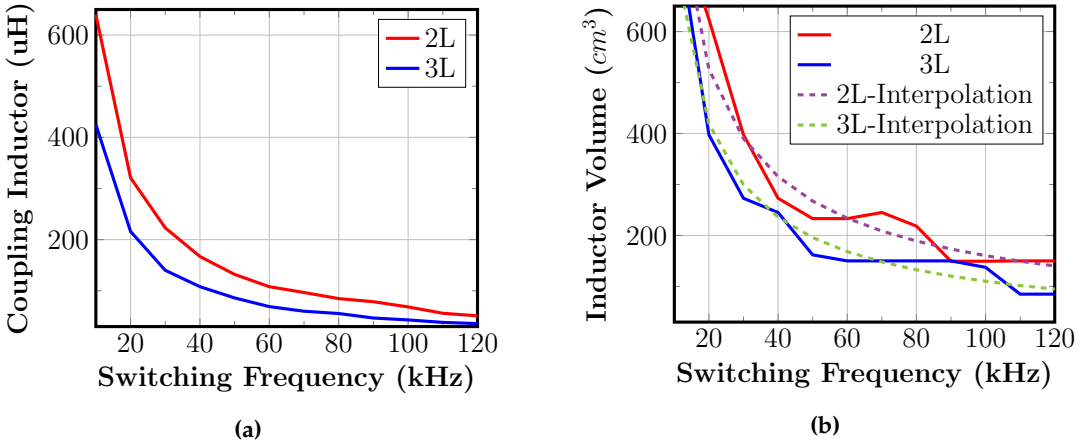
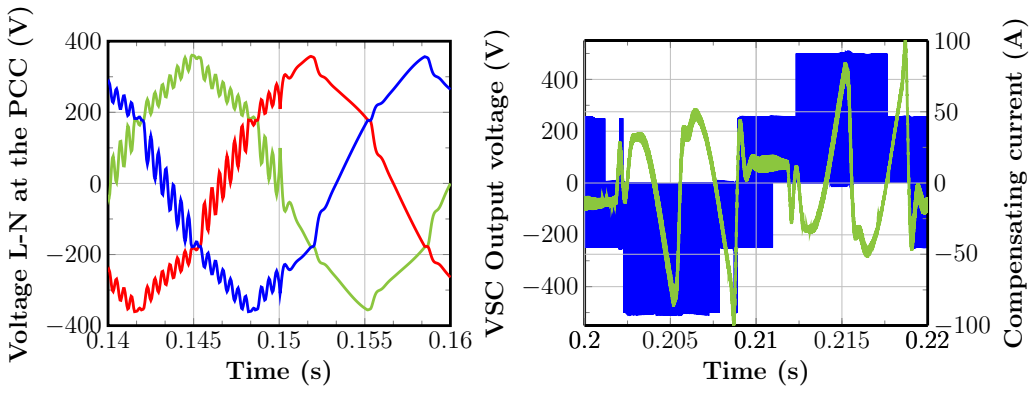



**Fig. 6.9:** (**a**) Coupling inductor value as function of the switching frequency for the 2L and the 3L topologies (**b**) Coupling inductor volume as function of the switching frequency for the 2L and the 3L topologies.

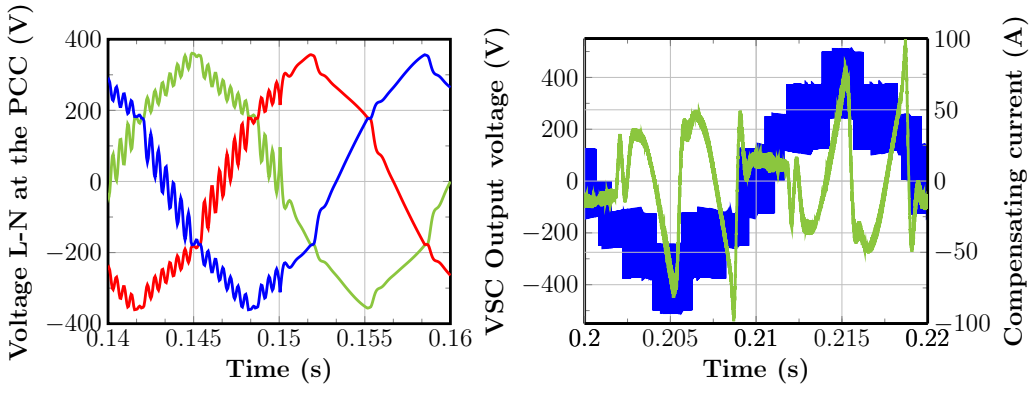
## 6.5 COMPARATIVE EVALUATION

In the same way as in chapter 4, in this chapter, the distribution system depicted in Fig. 4.6 was simulated with the parameters stated in Table 4.1. However, in the incoming simulations, the harmonic background distortion in the mains was equal to zero volts. Recall that a resonance condition is produced in the simulated scenario due to the capacitor bank's and grid's inductive impedance interaction. Indeed, the nonlinear load excites the mentioned resonance drawing currents in the vicinity of the resonance frequency. Obviously, for the simulations of the three-level converters presented in this chapter, the control system for the VSAPFs follows the structure described in section 6.2.1. It follows that under the described scenario, the 2L, 3L-TNPC, 3L-NPC, and 3L-ASYM topologies are simulated as VSAPF´s power circuits. In particular, the simulation results for the VSAPFs operating with a pulse frequency of 60 kHz and full compensation currents can be seen in Fig. 6.10 to Fig. 6.13. In all cases, the VSAPFs are activated at $t$=0.15 s



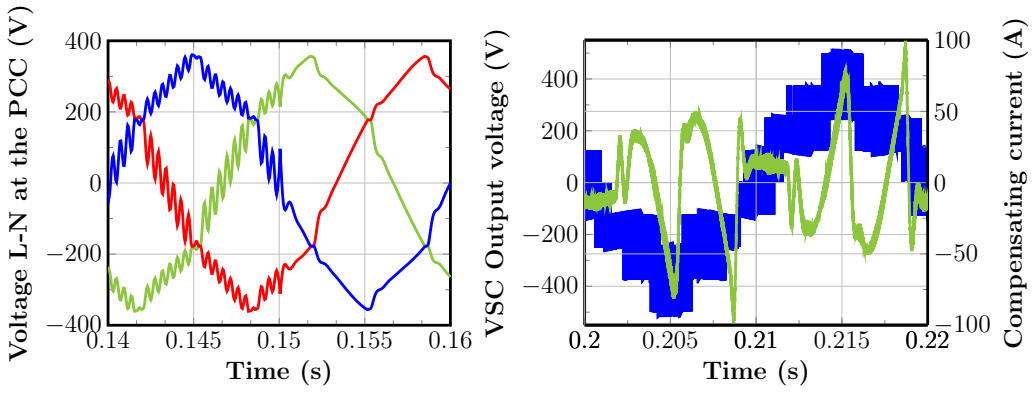

**(a)** **(b)**

**Fig. 6.10:** (**a**) $V_{PCC}$ behavior in presence of the 2L based VSAPF (**b**) 2L based VSAPF compensating current $i_C$ for the phase A (green) and converter output voltage $v_{o\text{-}N}$ for the same phase. VSAPF is activated at $t$ = 0.15 s. The $THD_V$ without VSAPF is 10.5% and with the VSAPF is reduced to 6.87%.



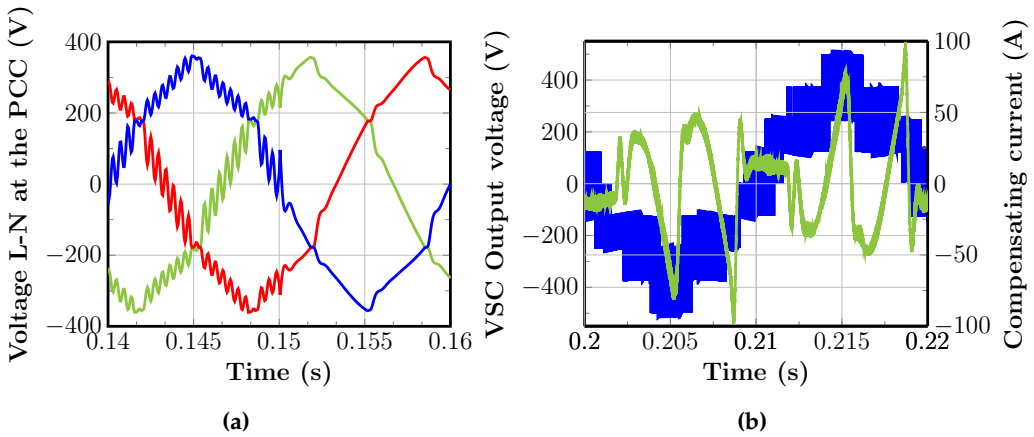

**(a)** **(b)**

**Fig. 6.11:** **a**) $V_{PCC}$ behavior in presence of the 3L-TNPC based VSAPF **b**) 3L-TNPC based VSAPF compensating current $i_C$ for the phase A (green) and converter output voltage $v_{o\text{-}N}$ for the same phase.




**(a)** **(b)**

**Fig. 6.12:** **a**) $V_{PCC}$ behavior in presence of the 3L-ASYM based VSAPF **b**) 3L-ASYM based VSAPF compensating current $i_C$ for the phase A (green) and converter output voltage $v_{o\text{-}N}$ for the same phase.




**(a)** **(b)**

**Fig. 6.13:** **a**) $V_{PCC}$ behavior in presence of the 3L-NPC based VSAPF **b**) 3L-NPC based VSAPF compensating current $i_C$ for the phase A (green) and converter output voltage $v_{o\text{-}N}$ for the same phase.

with the command to emulate a harmonic resistor of $R_s = 400\,m\Omega$. Before the VSAPFs activation, a $THD_V$ = 10.5% can be measured at the PCC since the resonance in the power system is excited by the nonlinear load. In fact, the effectiveness of all VSAPFs in reducing the harmonic voltage distortion at the PCC can be verified by observing Fig. 6.10 to Fig. 6.13. Specifically, the VSAPFs reduce the voltage distortion at the PCC reaching a $THD_V$ of 6.87% and eliminating the resonance in the power system. In effect, the standard IEC 61000-2-4 [212] defines the maximum voltage distortion limits for different power systems classes. Actually, the standard defines a maximum distortion of 8% for industrial power grids. The latter ones fall under the classification of compatibility level 2 or class 2. Indeed, the simulation results show that due to the action of the VSAPFs, the distortion levels in the simulated power system are below from those stipulated in the standard IEC 61000-2-4 for class 2 facilities. It is granted that when the switching frequency of the VSAPFs is increased and the coupling inductors are changed accordingly (see Fig. 6.9 **a)**), the same harmonics' filtering performance as in Fig. 6.10 to Fig. 6.13 is achieved. Moreover, Fig. 6.10b to Fig. 6.13b show the compensating currents injected by the VSAPFs in green, and the output voltage with respect to the neutral synthesized by each converter is depicted in blue. Obviously, the VSAPFs power circuits are isolated with respect to the neutral of the power system. For this reason, the two-level converter produces 5-levels in the output voltage, and the three-level converters produce 9-level in the phase output voltages, as shown in Fig. 6.10 **b)** to Fig. 6.13 **b)**.

### 6.5.1 *Efficiency Comparison*

Furthermore, for the same scenario mentioned before, all the different topologies for the VSAPFs were simulated with switching frequencies ranging from 10 to 120 kHz. From the simulation results, the overall power losses in the VSAPFs are calculated considering the conduction and switching power losses altogether:

$$P_{VSC} = N_{FET} \cdot P^{FET}{}_{Sw} + N_{FET} \cdot P^{Cond}{}_{FET} + N_{Diodes} \cdot P^{Cond}{}_{Diode} \tag{6.4}$$

where $N_{FET}$ and $N_{Diodes}$ stand for the number of SiC MOSFETs and diodes in each power topology. Moreover, the losses in the coupling inductors are labeled as $P_L$ and the losses in the ripple filter are labeled $P_{R_F}$. Truly, the mentioned losses are the most dominant

ones when we consider the complete SAPF converter system [125]. On this basis, Fig. 6.14 shows the overall power losses $P_{\text{Losses}} = P_{\text{VSC}} + P_{\text{L}} + P_{\text{R}_\text{F}}$ achieved by each of the topologies at different switching frequencies. Further, and based on the overall power losses, the efficiency of a particular VSAPF can be calculated using (4.58):

$$\eta = (1 - \frac{P_{\text{Losses}}}{3 \cdot V_{\text{L-N}} \cdot I_{\text{C}} \cdot cos(\phi)}) \cdot 100\% = (1 - \frac{P_{\text{VSC}} + P_{\text{L}} + P_{\text{R}_\text{F}}}{3 \cdot 230\,V \cdot I_{\text{C}} \cdot cos(\phi)}) \cdot 100\% \tag{6.5}$$

where it was considered $cos(\phi) = 1$ due to the fact that the VSAPF behaves as a pure resistive impedance at harmonic frequencies and that $i_C$ is formed mostly by harmonic components. Accordingly, the efficiency for each operating point was calculated for all the VSAPF power circuits simulated. In effect, the efficiency of the VSAPFs over the complete range of switching frequencies considered can be seen in Fig. 6.15 **a)**. First of all, notice that the two-level based VSAPF exhibits its highest efficiency when the converter's switching frequency is set equal to 20 kHz. This was the reason why 20 kHz was chosen as the switching frequency for the real VSAPF's prototype presented in chapter 4. Notice also that the highest efficiency for the two-level based VSAPF with 20 kHz simulated in this chapter is found around 98.5 %. Clearly, there is an excellent agreement with the peak efficiency of 98.43 % measured in the real VSAPF shown in section 4.7. Furthermore, it can be noticed that among all the topologies, the 3L-TNPC and the 3L-ASYM power circuits exhibit the highest efficiency in the switching frequency range evaluated. By observing Fig. 6.15 **a)**, the 3L-ASYM topology exhibits an efficiency slightly lower than the T-Type converter for switching frequencies below 60 kHz. And yet, the 3L-ASYM power circuit starts to be more efficient than the T-Type power circuit at switching frequencies greater than 70 kHz. Furthermore, as the highest efficiencies for the 3L-TNPC and 3L-ASYM power circuits were observed at 60 kHz, the VSAPFs' designs were evaluated at a switching frequency of 60 kHz for different values of the compensating (see Fig. 6.15 **b)**). The VSAPFs were simulated for different operating points by changing the reference $R_s$ leading to the RMS value of $I_C$ to vary from 11.57 A (34%) to 33.5 A (100%). The peak efficiency reaches the value of 98.99% at 60% of the rated compensating current for both 3L-TNPC and 3L-ASYM at 60 kHz switching frequency. The peak efficiency achieved by the proposed topology is remarkably higher than the 97.8% peak efficiency claimed to be held by state-of-the-art 3L-NPC based SAPFs [110]. On the other hand, power density improvements can also be expected in comparison

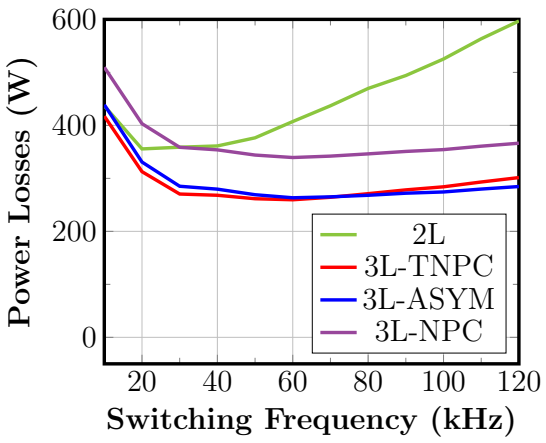



**Fig. 6.14:** VSAPF overall losses as function of the switching frequency. VSAPF injecting rated compensating current $i_C$ = 33.5 A (rated power rating 23.1 kVA).

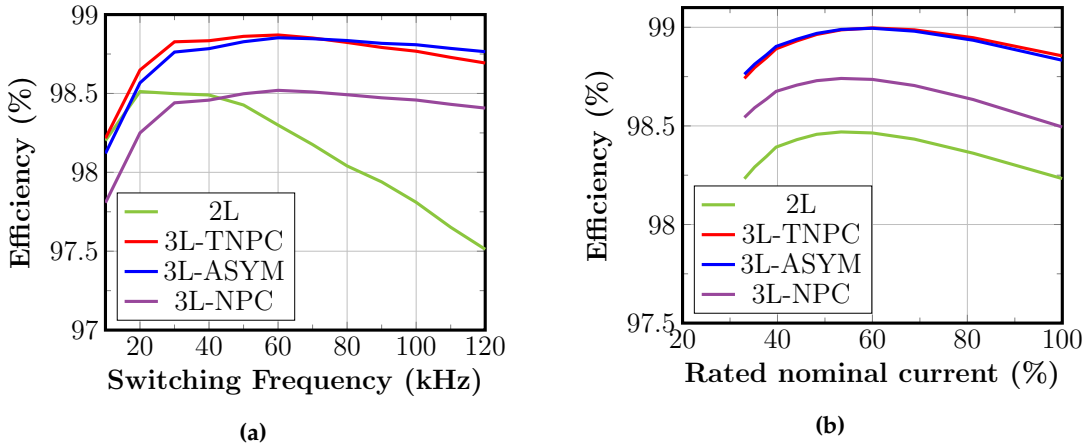



**Fig. 6.15: a**) VSAPF efficiency function of the switching frequency. VSAPF injecting rated compensating current $I_C$ = 33.5 A (rated power rating 23.1 kVA). **b**) VSAPF efficiency as function on the compensating current $I_C$ ($I_C$=33.5 A at 100%). The switching frequency was set as 60 kHz.

with state-of-the-art solutions. Take for instance three-phase PFC rectifier systems, where coupling inductors commonly take 33% of the total volume share of the converter [31]. It can be argued that a similar pattern would emerge for VSAPFs. Thus, from Fig. 6.9 **b)** it can be inferred that a three-level full SiC power circuit operating with a high switching frequency will significantly improve the volumetric power density (kVA/cm$^3$) of the VSAPF in comparison to full SiC 2L or 3L silicon-based power circuits.

### 6.5.2 *Efficiency Performance Discussion*

The following subsections address the performance regarding power losses of the two- and three-level power circuits only at the nominal rated current. With this in mind and to start the discussion about the VSAPFs´ efficiency, it is necessary to differentiate between two kinds of power losses. Specifically, there is power losses that are switching frequency dependent and there is power losses that are switching frequency independent. The losses independent of the switching frequency are the conduction losses in power transistors and diodes. The switching frequency dependent losses are the switching losses in the transistors, the inductor losses (when the inductor value is changed to maintain the ripple constant), and ripple filter losses.

#### 6.5.2.1 *Ripple Filter Losses*

From subsection 3.1.2, it can be inferred that the ripple filter is designed as a HPF tuned at half of the switching frequency. Indeed, for the simulated VSAPF's power circuits, the filter capacitors were held constant at $C_F = 350\,\mu F$. The latter ensures a stable operation of the VSAPFs for $R_s = 400\,m\Omega$ in the frequency range evaluated. For further details see Appendix A. It follows that if the filter capacitor is held constant and the switching frequency is changed, the damping resistor should be adapted to any change of the switching frequency of the power converter. Thus, according to (3.11) [17]:

$$R_F = \frac{1}{2\pi C_F \frac{f_{Sw}}{2}} \tag{6.6}$$

From the equation above, it is clear that $R_F$ is reciprocal to the switching frequency $f_{Sw}$. Therefore, the ripple filter losses in the form $P_{R_F} = R_F \cdot {I_F}^2$ , with $I_F$ is the current flowing through the ripple filter, decrease in the same proportion for all topologies as the switching frequency is increased. The latter can be seen in Fig. 6.16 where the curves of $P_{R_F}$ for each converter topology practically overlap each other all the time.

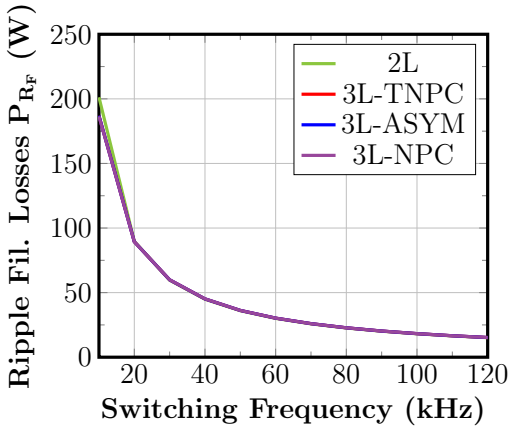



**Fig. 6.16:** Ripple filter losses as function of the switching frequency for the different topologies. The ripple filter is tuned at half of the switching frequency at each case maintaining the capacitor value fixed at 350 $\mu F$.

#### 6.5.2.2 *Coupling inductor losses*

The power losses in the coupling inductors are determined by the compensating currents injected by the VSAPF. Certainly, most of these power losses in the high-frequency range depend on the current ripple. It turns out that the current ripple depends on the power converter's topology and the switching frequency. In any case, all three-level converter topologies, namely the 3L-TNPC, 3L-ASYM, and 3L-NPC topologies, produce to a vast extent the same current ripple. Therefore, in the discussion carried out in this subsection, the inductor power losses produced by the three-level topologies are discussed in general. Furthermore, inductors' power losses are subdivided into core losses and winding or copper losses. The core losses, in turn, can be subdivided into hysteresis and eddy current losses. On soft magnetic materials such as powdered iron, the eddy current losses are minimal and can be neglected because the diameter of the iron particles forming the core is smaller than the skin depth of switching frequencies in the kHz range [136]. Furthermore, the overall core losses in a power inductor can be roughly estimated with the Steinmetz equation:

$$P_{Fe} = V_c \cdot K_c \cdot f^{\alpha} {B_{max}}^{\beta} \tag{6.7}$$

where $V_c$ is core volume, $B_{max}$ is the peak value of the flux density with sinusoidal excitation at frequency $f$, $K_c$, $\alpha$, and $\beta$ are constants that depend on the core material [136]. Clearly, from (6.7), it can be seen that the core losses are proportional to the inductor volume. With this in mind, and from the results presented in Fig. 6.9 **b)**, it can be concluded that the inductor's core losses in a three-level power circuit are going to be smaller than the inductor's core losses in a two-level power circuit. After all, the volume of a coupling inductor meant for a three-level based converter will be smaller than the volume of an inductor meant for a two-level based converter according to (6.2). The latter can be confirmed by observing Fig. 6.17 **a)**. The figure shows the core losses for a single inductor as a function of the switching frequency. These results were obtained from the

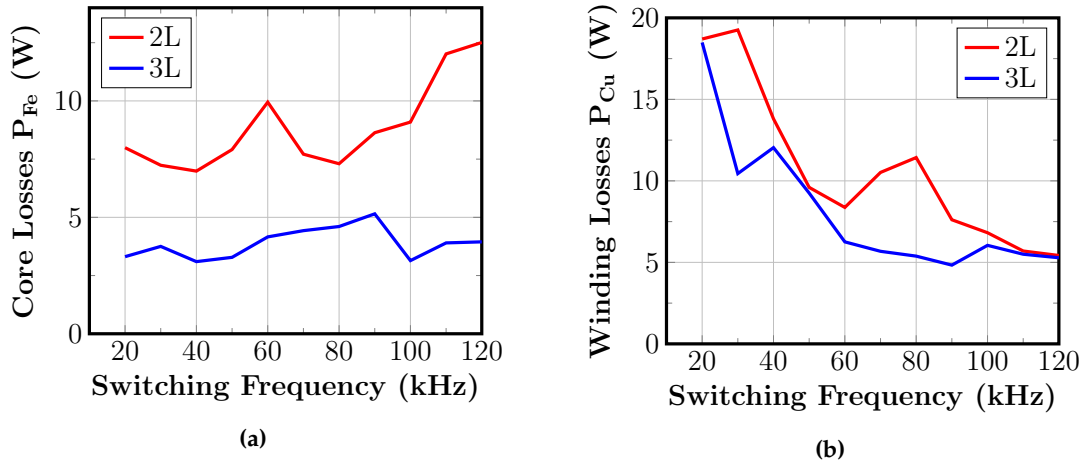



**Fig. 6.17:** **a**) Core losses of an individual coupling inductor as function of the switching frequency **b**) Winding losses of an individual coupling inductor as function of the switching frequency.

GeckoMagnetics's simulation. Clearly, Fig. 6.17 **a)** shows the extreme nonlinear core loss dependency on the switching frequency. This nonlinear behavior is related to the complex hysteresis losses mechanism (i.e. major hystesis loops, minor hysteresis loops, relaxation effects) which are handled and calculated by the simulation software GeckoMagnetics [213]. On the other hand, winding or copper losses ($P_{Cu}$) are proportional to the number of turns $N_L$. Generally speaking, the number of turns decreases as the target inductance value decreases [214]. Thus $P_{Cu}$ losses under the design's constraints in this chapter decrease as the switching frequency increases. The latter can be confirmed by resorting to Fig. 6.17 **b)** . The figure shows the winding losses for a single inductor calculated by GeckoMagnetics at different switching frequencies for the two- and three-level topologies. Altogether, taking into account core and winding losses, the total inductor losses can be calculated as follows:

$$P_L = 3 \cdot (P_{Fe} + P_{Cu}) \tag{6.8}$$

Using this equation, the total inductor losses obtained from the VSAPFs simulations can be seen in Fig. 6.18. From the coupling inductors losses perspective, three-level topologies offer significant advantages compared to the two-level converter, as shown in Fig. 6.18. Furthermore, and in regards to the three-level topologies, it can be seen that if the switching frequency is increased from 20 kHz to 60 kHz, there is a significant reduction in the inductor's power losses. However, increasing the switching frequency beyond 60 kHz produces only a slight reduction in the inductor's power losses as can be concluded from Fig. 6.17 **b)** and Fig. 6.18.

#### 6.5.2.3 *VSC Switching losses*

From Table 6.3, it can be inferred that SiC MOSFETs rated for 900 V exhibit lower switching losses than SiC MOSFETs rated for 1200 V. In other words, the lower the voltage class of a particular SiC MOSFET, the lower are the switching losses exhibit by the device. Accordingly, the two-level power circuit will exhibit the highest switching losses among the topologies evaluated in this chapter for two reasons. First, all the switches in the two-level topology are rated at 1200 V. Second, all the switches in the two-level circuit always commutate at full DC-Bus voltage of 750V. Conversely, the three-level topologies are constructed with a combination of 1200 V and 900 V rated power switches.

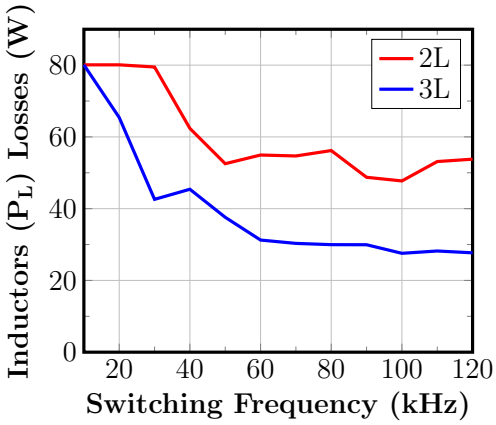



**Fig. 6.18:** Total inductor losses as function of the switching frequency. The design constrain was to maintain the current $\Delta I_{pp}$ constant to 13.4 A.

Also, some of the switches in the three-level power circuits commutate at only half of the DC-Bus voltage, namely 375 V. On this basis, the 3L-NPC and 3L-ASYM outperform the 3L-TNPC power circuit. The reason is that the 3L-NPC and 3L-ASYM circuits have more SiC MOSFETs rated at 900 V and more switches commutating at 375 V than the 3L-TNPC topology. Obviously, the 3L-NPC power circuit has one more switch rated at 900 V than the 3L-ASYM. Nonetheless, the switching losses performance of the 3L-ASYM and 3L-NPC are very similar as can be seen in Fig.6.19 **a)**. In effect, the switching losses exhibited by all topologies as a function of the switching frequency can be seen in Fig. 6.19 **a)**. Indeed, the performance of the 3L-TNPC from the switching losses perspective degrades as the switching frequency increases and becomes less and less attractive at high switching frequencies.

### 6.5.2.4 *VSC Conduction losses*

Fig. 6.19 **b)** summarizes the conduction losses for the VSAPFs when they inject a com-

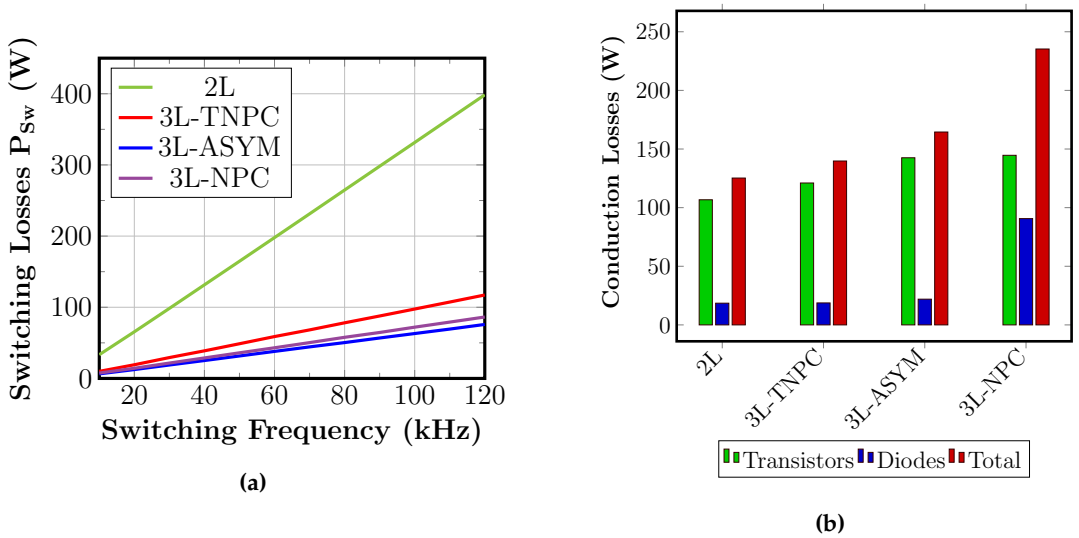



**Fig. 6.19: a**) Switching losses as function of the switching frequency for the 2L and the 3L topologies **b**) Conduction losses for the 2L and 3L at 100% compensating current.

pensating current of 33.5 A into the power grid. Indeed, all the topologies benefit from the third quadrant operation of SiC MOSFETs, where the current is shared between each SiC MOSFET and its antiparallel SBD. The latter is, of course, for currents flowing from source to drain, from the SiC MOSFETs perspective. The third quadrant operation effectively decreases the conduction losses as the effective total resistance is decreased as a consequence of the parallel connection of the $R_{ds,on}$ resistance of the SiC MOSFET and $R_{fd}$ resistance of the SBD. Moreover, it can be seen that the two-level based power converter exhibits the lowest conduction losses. This is because only one semiconductor carries the current at each output voltage level. Furthermore, the 3L-TNPC topology is the second one with the lowest conduction losses. Because only one semiconductor is used to connect the positive rail $p$ or negative rail $n$ to the output node. It is only when the neutral point $o$ is to be connected with the output node that two semiconductors are used in the 3L-TNPC power circuit. The third topology in the conduction losses classification is the 3L-ASYM. The topology uses two semiconductors to carry the current at the $p$ and $o$ output voltage levels. Further, the 3L-ASYM uses just one semiconductor to carry the current at the $n$ output voltage level. Finally, the 3L-NPC exhibits the worst performance from the conduction losses perspective since at each output voltage level $p$,$o$ or $n$ two semiconductors carry the current. The situation for the 3L-NPC is worsened because to output a voltage level $o$, the clamping diodes D5 and D6 are used. Those do not benefit from the third quadrant operation of any SiC MOSFET, and also their forward voltage $V_{fd}$ [205] not present in SiC MOSFETs, impacts the overall 3L-NPC conduction losses.

#### 6.5.2.5 *Total losses*

Considering the results presented in Figs. 6.18 and 6.19, it can be inferred that the three-level power topologies outperform the two-level power circuit due to the lower switching and lower inductors losses. However, among the three-level topologies, the 3L-NPC is the worst in terms of power losses. The main reason is the considerable conduction losses inherent to this power topology. Moreover, the power circuit proposed in this chapter, namely the 3L-ASYM topology, benefits from reduced switching losses in comparison with the 3L-TNPC and low conduction losses compared with the 3L-NPC. Consequently, regarding the power losses and efficiency, the 3L-ASYM power circuits stand precisely in the middle between these topologies. Even at high switching frequencies (in our case beyond 60 kHz), the proposed topology shows lower losses and thus higher efficiency than the other three-level circuit counterparts. In particular, the 3L-TNPC suffers from high switching losses at high switching frequencies, and the 3L-NPC suffers all the time from high conduction losses.

## 6.6 EXPERIMENTAL RESULTS

The original design for the 3L-ASYM power circuit presented in section 6.3, was initially carried out for a VSAPF of 23.1 kVA. However, for the experimental setup, the 3L-ASYM based VSAPF is scaled down in one order of magnitude from 23 kVA to 2 kVA. Further, the VSAPF is constructed with material available at the laboratory. In other words, the SiC MOSFETs, SiC SBD and inductors taken to build the 3L-ASYM power circuit are just taken from the stock available at the laboratory. The main idea of the experimental setup is to demonstrate the feasibility of the solution in a scaled-down prototype with reduced currents and voltages. Thus, a single leg of the 3L-ASYM converter was built using two

Wolfspeed evaluation boards 8020-CRD-8FF1217P-1 (see Fig. 6.20). Each board consists of two SiC MOSFETs C2M0080120D and two SBD diodes C4D20120D, all of them in a TO-247 package. Furthermore, each 8020-CRD-8FF1217P-1 was configured as a half-bridge, and later both evaluation boards were cascaded. Each SiC half-bridge is driven by a 2.5 A Avago gate driver (ACPL-W346) that is interfaced through optocouplers with the control system. A coupling inductor of 100 $\mu H$ is connected to the output port of the single leg in one extreme, and the other extreme is connected to the middle point of the DC-Bus, as can be seen in Fig. 6.20. The coupling inductor of 100 $\mu H$ is built with two UU93/60 cores of amorphous material (AMCC800A). Further, the windings consist of a square copper cable of 10mmx7.11mm, resulting in a total winding section of 71mm$^2$ with a total resistance at twenty degrees celsius of 1.6 $m\Omega$. A photograph of the experimental setup can be seen in Fig. 6.21. Furthermore, the DC-Bus voltage during the experiment was set as 100V, and the switching operating frequency was chosen to 40 kHz due to the availability of the 100 $\mu H$ coupling inductor (see Fig. 6.9a). Two electrolytic capacitors connected in series, each with a total capacitance of 2200 $\mu F$, are connected parallel to voltage sources of 50 V. The capacitors are inside two SEMITEACH-IGBT Stacks and connected to the Wolfspeed evaluation boards through cables. In this experiment, the converter was operated in standalone operation, in other words, without grid interaction. The control algorithm and the Level-shifted PWM modulation are implemented in a dSPACE system MicrolabBox DS1202.

The compensating current $i_C$ and the output voltage $v_O$ with respect to the negative rail of the converter measured during the experiment can be seen in Fig. 6.22 and a zoomed version in Fig. 6.23. The compensating current (signal in yellow color in Fig. 6.23) follows a reference far from a pure sinusoidal shape. It contains all the components stated in Table 6.6. The values in Table 6.6 were obtained from a Fourier analysis of the compensating current found in Fig. 6.12 **b)**, where the amplitude of the components was scaled down by a factor of 2. The value of the DC Bus voltage $v_{DC}$ is determined by the PCC line voltage of the grid where the VSAPF is going to be connected. If $v_{LL}$ is the

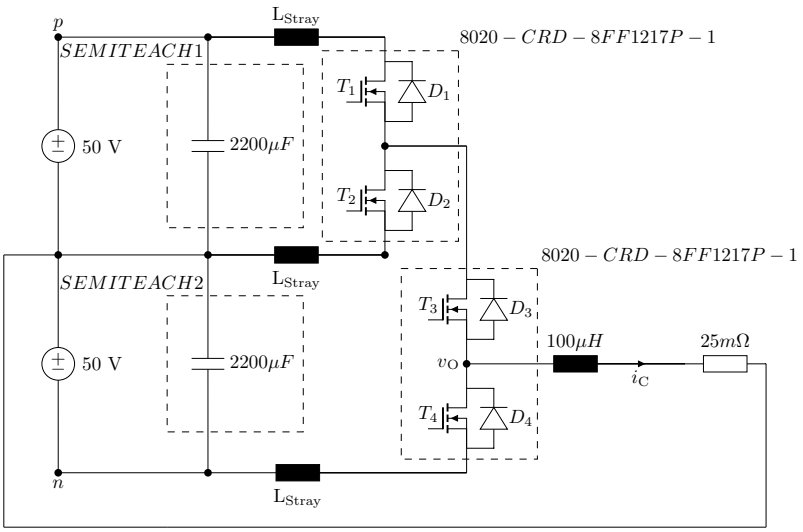
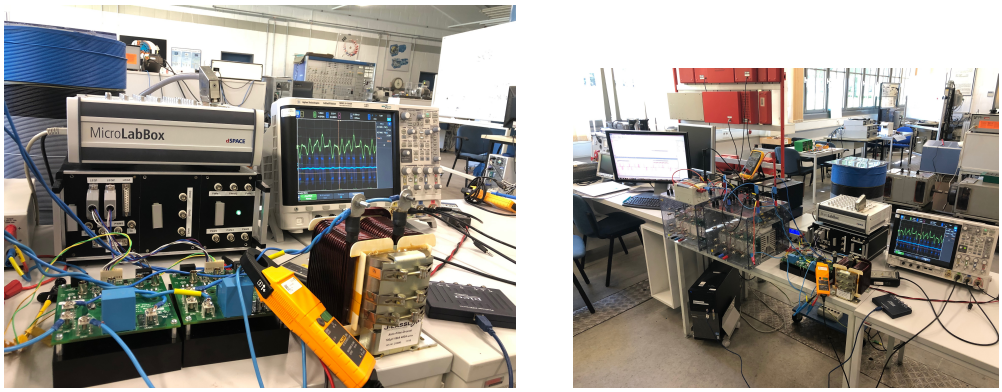



**Fig. 6.20:** Schematic of the 3L-ASYM power circuit used during the experiment. One leg of the 3L-ASYM is built by cascading two 8020-CRD-8FF1217P-1 boards.




**(a)** **(b)**

**Fig. 6.21:** Experimental implementation of the three level asymmetrical topology 3L-ASYM. (**a**) KIT8020-CRD-8FF1217P-1 boards connected to form one leg of the 3L-ASYM converter (**b**) Test bench.

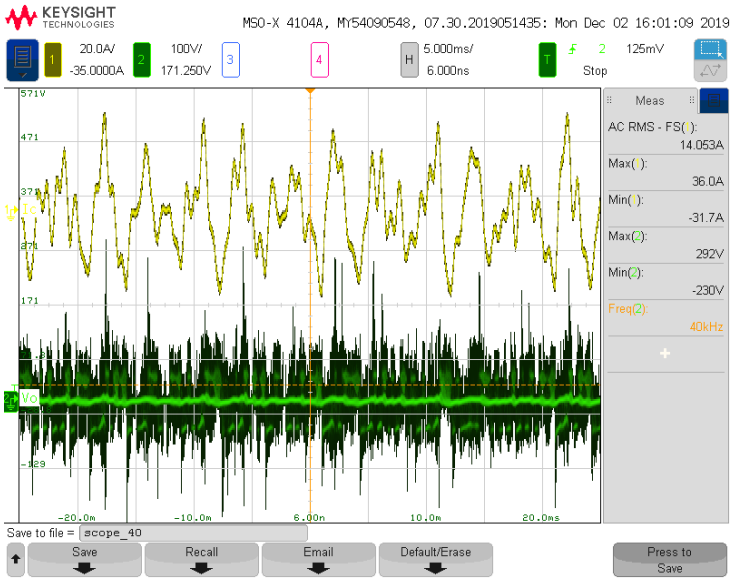



**Fig. 6.22:** Current and output voltage measured on the 3L-ASYM power circuit prototype. Compensating current $i_C$ (yellow) and output voltage $v_O$ (green). Current measurement done through Rogoswski Current Waveform Transducer CWTUM/6/B. Voltage measurement done through differential probe Pico TA042.

line voltage at the PCC of the power system, the following equation defines the relation between the VSAPF's DC-bus voltage and the RMS line voltage [17]:

$$v_{\mathrm{LL}} = \frac{\sqrt{3} \cdot v_{\mathrm{DC}}}{1.5 \cdot \sqrt{2}} \tag{6.9}$$

For a DC-bus voltage of $v_{DC}$= *100 V*, the VSAPF can be connected to a power grid with a line voltage of:

$$v_{\mathrm{LL}} = \frac{\sqrt{3} \cdot 100V}{1.5 \cdot \sqrt{2}} = 81.65V \tag{6.10}$$

The RMS value of the compensating current is around 14 A and it peaks at 34 A as can be seen in Fig. 6.22. It follows that the power rating of the experimental setup is:

$$S_{\mathrm{VSAPF}} = \sqrt{3} \cdot v_{\mathrm{LL}} \cdot i_{\mathrm{C}} = \sqrt{3} \cdot 81.65V \cdot 14A = 1.98\ kVA \tag{6.11}$$

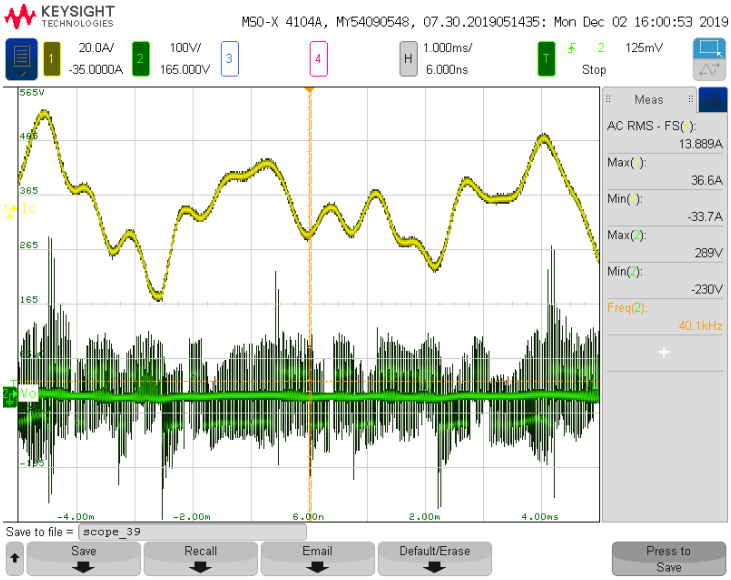



**Fig. 6.23:** Zoomed in version of the current and output voltage measured on the 3L-ASYM power circuit prototype. Compensating current $i_C$ (yellow) and output voltage $v_O$ (green). Zoomed version of Fig. 6.22.

**Table 6.6:** Compensating Current Reference - Harmonic Components

| Harmonic Number | Frequency (Hz) | Amplitude (A) | Phase (°) |
|---|---|---|---|
| 1 | 50 | 0.24 | -10.3 |
| 5 | 250 | 15.45 | 207.8 |
| 7 | 350 | 10.584 | -14.9 |
| 11 | 550 | 4.587 | -28.6 |
| 13 | 650 | 4.418 | 108 |
| 17 | 850 | 3.931 | 158.2 |
| 19 | 950 | 3.015 | 223 |
| 23 | 1150 | 3.477 | -72.1 |
| 25 | 1250 | 2.413 | -25 |
| 29 | 1450 | 2.726 | 48.1 |
| 31 | 1550 | 1.792 | 82 |

Three voltage levels in $v_O$ that correspond to +50 V, 0 V, -50 V can be seen in Fig. 6.22. Furthermore, the measurements in Fig. 6.23 confirm the 40 kHz on the output voltage, corresponding to the 40 kHz switching frequency set on the dSPACE control system. By inspecting Fig. 6.23, it is possible to observe some voltage peaks during the MOSFETs switching ON and OFF transitions. Such peaks sometimes reach the value of 292 V. This is due to the parasitics of our laboratory setup. The connection between the DC-bus capacitors (within the SEMITEACH-IGBT Stacks) and the evaluation boards is made using 2.5 mm² cable. They introduce considerable stray inductances into the power loop. Such stray inductances ($L_{Stray}$) produce voltage overshoots or voltages spikes ($\Delta V$) due to the *di/dt* (rising and falling currents) over the SiC transistors during the MOSFETs commutations according to [215]:

$$\Delta V = L_{\text{Stray}} \cdot \frac{di}{dt} \tag{6.12}$$

As SiC MOSFETs switch much faster than Si IGBTs, the *di/dt* (that sometimes reaches $6kA/\mu s$ for SiC MOSFETs) is also increased, and the stray inductances on the power loop play a more critical role in SiC MOSFET power circuits than in Si IGBT power circuits. Therefore, it is granted that if we redesign the experimental setup including all the DC-Bus capacitors in the same PCB as the SiC MOSFETs, stray inductances will be minimized, and voltage spikes will be avoided.

## 6.7 CHAPTER SUMMARY

In this chapter, different all-SiC based power topologies for the active damper have been evaluated and compared in terms of power losses. Specifically, the comparative evaluation included the 2L, 3L-TNPC, and 3L-NPC conventional topologies. In addition, an all-SiC non-conventional topology was also proposed in this chapter and compared against the conventional topologies. In particular, the proposed topology in this chapter is named three-level asymmetrical power circuit. On this basis, this chapter explored the switching states, voltage stress across the semiconductors, and the current commutation during switching states transitions for the proposed non-conventional topology. Furthermore, in order to exploit the SiC MOSFETs' features of low switching losses, almost no reverse recovery, and low gate charge, the pulse or switching frequency of the converter was used as design degree of freedom to maximize the overall efficiency of the VSAPF for all circuit topologies. On this basis, the comparative evaluation between the all-SiC asymmetrical and conventional topologies was carried out, sweeping the switching frequency from 10 to 120 kHz. The objective was to determine which power circuit among the studied topologies produced the lowest power losses. The comparative evaluation results show that the proposed asymmetrical 3L topology outperforms 2L and 3L conventional topologies (3L-TNPC and 3L-NPC) in terms of power losses for switching operating frequencies above 60 kHz, having its best performance at 70 kHz. As the bandwidth of the VSAPF is related to its switching frequency, it is a welcome product that the switching frequency for minimum losses is encountered at such a high value because a highly dynamic VSAPF solution can be realized. Furthermore, the high efficiency exhibited by the proposed three-level topology when it is operated at high switching frequencies is due to three main reasons. First, coupling inductors with small volume are used as interface with the power grid. Second, most of the time, the power switches commutate just at half of the DC-Bus voltage. Third, most of the converter's power switches are rated at 900 V. The latter reduces conduction and switching losses due to lower $R_{\text{ds, on}}$ resistance and lower total energy ($E_{Tot}$) of these switches compared to switches rated at 1200 V (see Table 6.3). Furthermore, one distinct feature of the proposed topology is that it can be formed by just two 2L commutation cells. This feature is important because currently, for high current ratings, there is no commercial availability of three-level modules in the market [197, 216]. Thus, the proposed topology is an interesting option for building a high-performance, high-current three-level converter with available half bridge power modules.

# 7

# Discrete Current Controller Design using Ragazzini Method for Active Damper

The active damper's capability to suppress resonances in a wide range of harmonics frequencies, including inter harmonics, depends massively on the tracking performance of its inner current controllers. Likewise, the active damper's stability depends on the current controllers' bandwidth. Although most current controllers are implemented digitally in a microcontroller or DSP nowadays, the conventional current controller design is still done in the continuous frequency domain. Later, the current controller discretization is carried out using transformation techniques (e.g. Tustin transformation, forward rule, and others). The disadvantage of such a methodology is that the current controller bandwidth is restricted to be ten times smaller than the PWM sampling frequency. This fact negatively affects the performance of the active damper and its stability, especially at small values of the emulated resistance. On this basis, this chapter deals with the direct design of current controllers in the discrete domain. Specifically, this chapter presents the design of discrete current controllers using the Ragazzini method. The result of such a design methodology is a closed-loop for the current control with a bandwidth three times higher than the bandwidth achieved by current controllers designed with traditional methods. The achieved higher bandwidth boosts the effectiveness of the active damper and pushes its stability limit forward. The findings presented in this chapter were also published in:

- R. Guzman Iturra and P. Thiemann, "Discrete Current Controller Design using Ragazzini Method for Active Damper," 2020 5th IEEE Workshop on the Electronic Grid (eGRID), 2020, pp. 1-8.

## 7.1 INTRODUCTION

An active damper can be conceived as a controlled current source that injects harmonic compensating currents $i_{\text{Ch}}$ into the grid. Such compensating currents are proportional to the harmonic voltages $v_{\text{PCCh}}$ measured at the PCC. Thus, the currents injected by the active damper obey the feedback law $i_{\text{Ch}} = \frac{v_{\text{PCCh}}}{R_s}$ [48]. If the proportionality factor is set as $\frac{1}{R_s}$, under the mentioned feedback law, the active damper behaves as a virtual shunt resistor of $R_s$ ($\Omega$) for all the harmonic frequencies as was explained in section 4.2. Furthermore, from section 2.4, it is known that state-of-the-art active dampers are formed by VSC with a self-supporting DC-Bus interfaced through the power system with coupling inductors. Actually, for the mathematical modeling that will be presented in this

chapter, an extended version of the VSC power circuit depicted in Fig. 2.4 is drawn as in Fig. 7.1 [17, 30]. Moreover, Fig. 7.2 shows a simplified version of the active damper control system presented in section 4.3. In effect, the simplified control system in Fig. 7.2 is more suitable for discussing the mathematical modeling and discretization of the current control loop. Moreover, the active damper's control system is implemented digitally on a microcontroller, or DSP in modern active power filters [168]. It is granted that the Current Controller (CC) 's aim is to track as accurately as possible the compensating current reference ($i_C{}^*$) generated by the outer loops. To this end, PWM modulators govern the VSC, providing the appropriate signals to the power semiconductors. In effect, the PWM produces the time average output voltage demanded by the current controller at the VSC's output terminals [168, 217]. Certainly, the active damper's capability to suppress resonances in a wide range of harmonics frequencies and its stability depend heavily

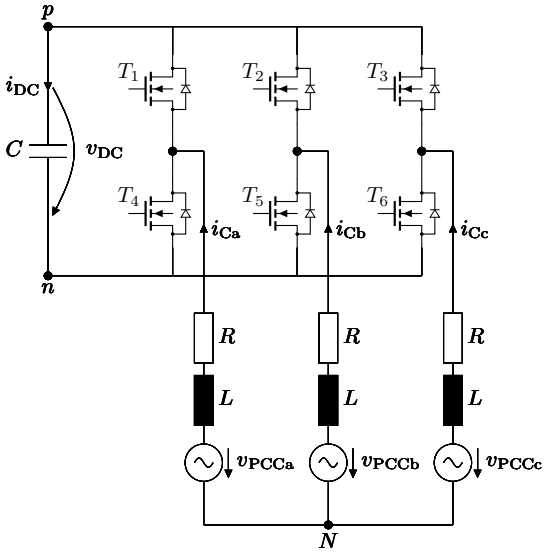



**Fig. 7.1:** Active Damper with self-supporting DC-bus consists of VSC, coupling inductors and DC-bus capacitor.

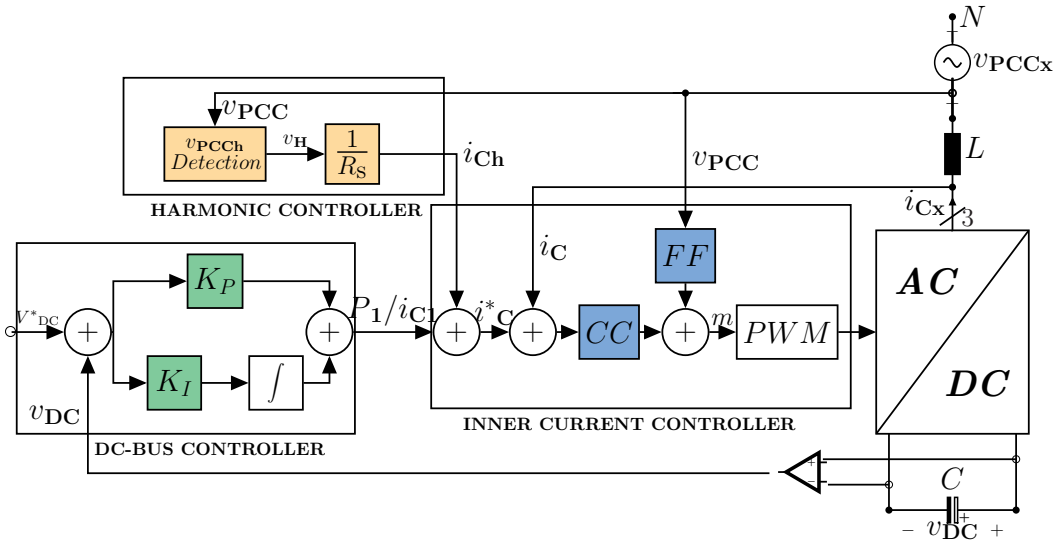



**Fig. 7.2:** Active Damper cascade control, harmonic resistance emulation and DC-Bus controller as outer loops.The inner loop is commanded by the current controller (CC).

on the tracking performance of its inner CC. Although nowadays, the majority of the CCs are implemented in a digital form, traditionally, the design of current controllers for grid-connected voltage source inverters is done in the continuous frequency domain, or s-domain [167, 168]. Afterwards, its discretization is carried out using transformation techniques, a procedure known as discrete design by emulation or s to z mapping [218]. Actually, the preferred transformation technique is the Tustin Method with prewarping [219]. The former retains the stability of the closed-loop achieved in the s-domain into the z-domain. Additionally, the prewarping feature minimizes the frequency response distortion caused by the transformation process and maintains, at the same time, the half-power frequency [220]. Nevertheless, such design methodology has as a consequence that the CC´s maximum bandwidth $w_c$ (related to the tracking capability of the current controller) achievable while guaranteeing a phase margin $\phi_m$ is around ten times smaller than the PWM sampling frequency [221]. This is because the PWM modulator and digital computational delay are approximated by a transport delay transfer function in the continuous domain. This forces designers to take a conservative approach to avoid instabilities in the CC´s design. However, such limitations on the $w_c$ are detrimental to the damping performance of the power electronics-based active damper. Furthermore, as the active damper forms a closed loop between the measured harmonic voltages and the compensating currents, a low CC´s bandwidth translates to a high phase shift between the performed compensating currents and their references, which could lead to the active damper instability, especially at low values of $R_s$ [222, 223].

The direct discrete design of the current controller in the less familiar z-domain can bring many advantages. In this regard, previous work has already dealt with the design of CCs entirely in the discrete domain. For instance, current controllers in state space based on full state feedback and with state estimators were designed in [224] and [225] respectively. Current Controller design based on Linear Quadratic Regulators (LQRs) and with Dahlin Control were presented in [221] and [226] respectively. Design of discrete PI current controllers are reported in [227, 228] and discrete current controllers with lead compensators were presented in [229]. It is necessary to highlight that conventional continuous controller forms (e.g. PI, PID, Lead Compensator) resulted from the limitations imposed by the pneumatic or electrical elements (resistors, amplifiers) that were available for the implementation of analog controllers in the past. Nowadays, however, many of these restrictions no longer apply to digital controllers [220]. The direct discrete design based on the Ragazzini method enables the possibility of designing current controllers with forms that diverge from conventional controllers and thus provides an opportunity to enhance the current controllers' bandwidth. To the best of the author's knowledge, the current controller design using this method has yet to be reported in the literature, and thus is the novelty brought by this chapter. The goal is to illustrate how the simple yet powerful Ragazzini method produces current controllers with a bandwidth higher than one-third of the PWM sampling frequency. The increased current controller bandwidth enhances the performance and stability of the active damper.

## 7.2 SYSTEM MODELING

Based on Fig. 7.1, the dynamics of the VSAPF's compensating currents injected into a balanced power system can be described in $\alpha$-$\beta$ coordinates as follows [217]:

$$v_{PCC\alpha}(t) = L\frac{di_{C\alpha}(t)}{dt} + Ri_{C\alpha}(t) + v_{\alpha}(t); \tag{7.1}$$

$$v_{PCC\beta}(t) = L\frac{di_{C\beta}(t)}{dt} + Ri_{C\beta}(t) + v_{\beta}(t) \tag{7.2}$$

where $v_{\alpha}(t)$=$m_{\alpha}\frac{Vdc}{2}$ and $v_{\beta}(t)$=$m_{\beta}\frac{Vdc}{2}$ are the voltages generated by the VSC. The voltages generated by the VSC can be controlled by the duty cycles $m_{\alpha}$ and $m_{\beta}$ respectively. Equations (7.1) and (7.2) lead to the block control diagram in Fig. 7.3 [168]. The actual compensating currents, reference compensating currents and grid voltages are acquired by the control system through Sample and Zero-Order-Hold (ZOH) blocks. The ZOHs are triggered and synchronized with the Digital PWM (DPWM) at twice the switching frequency ($f_{Sw}$). In other words, the sampling technique considered for the active damper in this chapter is PWM with double update [230]. In particular, this technique states that the sampling occurs at the positive and negative peaks of the triangular carrier. Such sampling process has the advantage that the average value of the compensating current can be obtained without current ripple and without the need to use low pass filters. Furthermore, Fig. 7.4 illustrates graphically the sampling process to measure the actual compensating currents without ripple [221]. The output voltage demanded by the current controller is expressed through the duty cycle value *m(k)*, which is calculated based on the currents measured one sampling period in the past, leading to a deadtime or transport delay of $\frac{1}{2\cdot f_{Sw}}$ in the control loop. Therefore a computation delay is added to the model due to the finite time that is needed to compute the next duty cycle after the ZOHs fetch a new value [231]. Furthermore, the Feedforward compensation (FF) of the current controller takes care of the disturbance rejection (rejection of the grid voltages) and decouples the CC from the major dynamics of the AC system [170]. Thus the current controller can be designed with a high emphasis on the reference tracking. From Fig. 7.3, it can be inferred that the continuous transfer function of the inductor plus inverter gain is [168]:

$$Q(s) = \frac{Vdc}{2}\frac{1}{Ls + R} \tag{7.3}$$

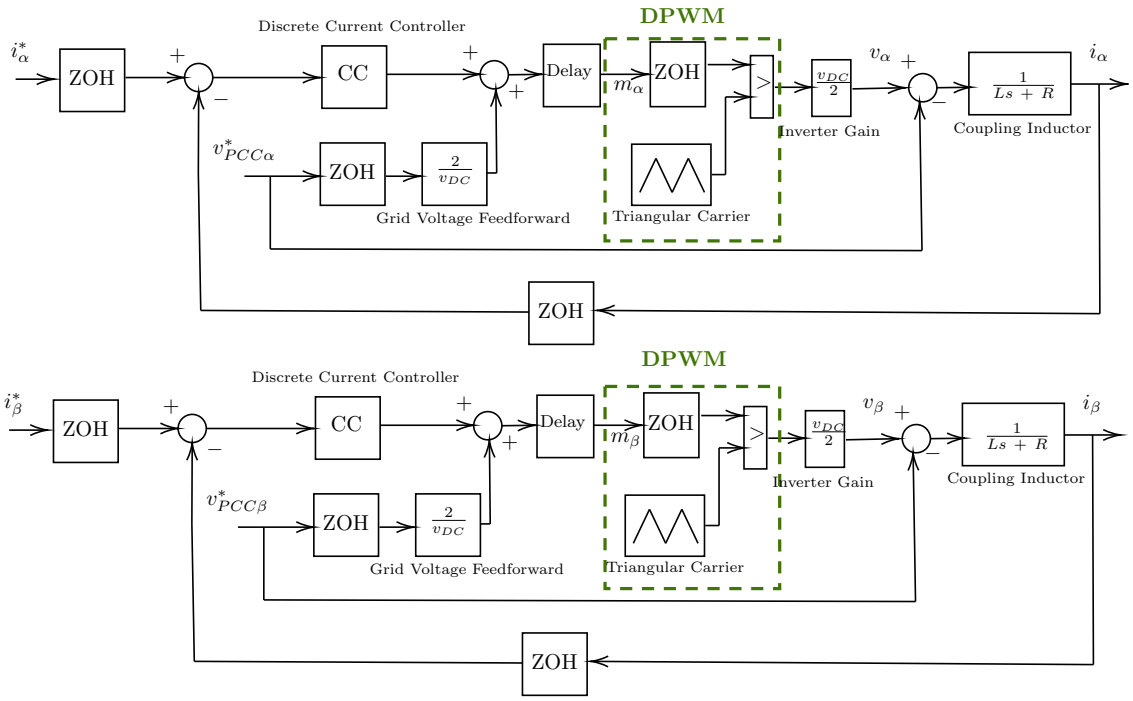



**Fig. 7.3:** Block diagram of the current controllers in $\alpha$-$\beta$ coordinates

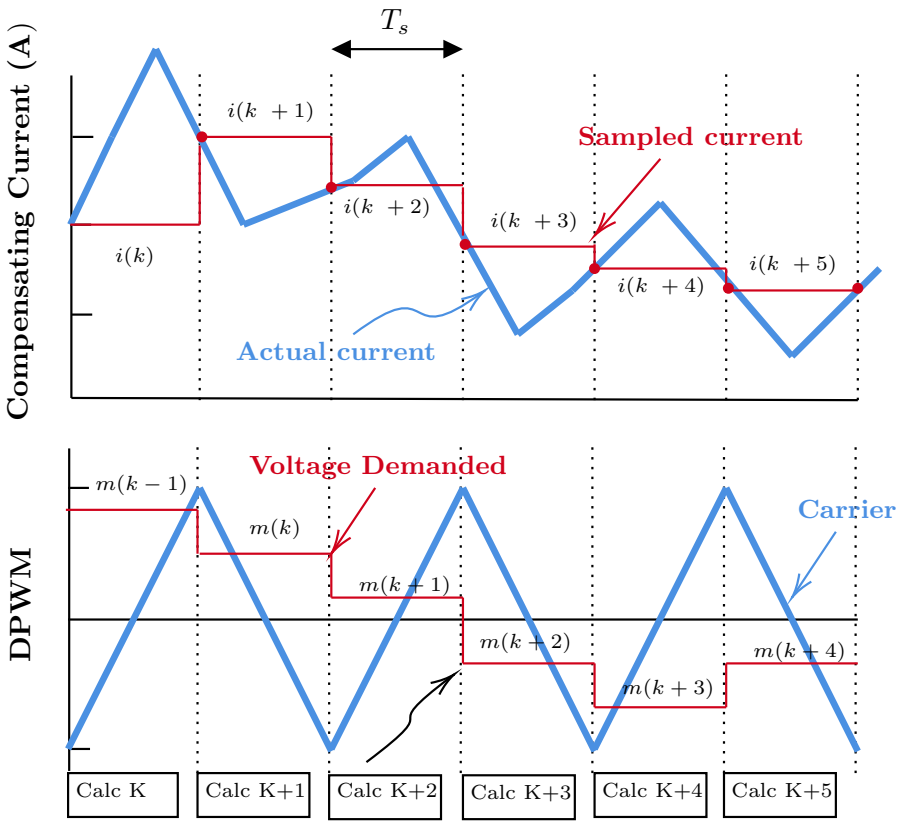



**Fig. 7.4:** Synchronous current sampling of PWM with double update

Equation (7.3) can be portrayed into the discrete frequency domain using the ZOH method [218] (chosen due to the nature of the DPWM sampling) which leads to [232]:

$$Q(z) = (1 - z^{-1})\mathcal{Z}\{\frac{Q(s)}{s}\} \tag{7.4}$$

$$Q(z) = \frac{V_{\text{dc}}}{2R}\frac{(1 - e^{-(R/L)T_{\text{s}}})z^{-1}}{1 - e^{-(R/L)T_{\text{s}}}z^{-1}} \tag{7.5}$$

$$Q(z) = \frac{V_{\text{dc}}}{2}\frac{bz^{-1}}{1 - az^{-1}} = \frac{V_{\text{dc}}}{2}\frac{b}{z - a} \tag{7.6}$$

where $a = e^{-(R/L)T_{\text{s}}}$ and $b = \frac{1-e^{-(R/L)T_{\text{s}}}}{R}$ with $T_{\text{s}} = \frac{1}{2 \cdot f_{\text{Sw}}}$ for double update. The computation delay can be modeled with an unit delay $z^{-1}$, thus the discrete plant seen by the CC is as follows:

$$P(z) = Q(z)z^{-1} = \frac{V_{\text{dc}}}{2}\frac{b}{z(z - a)} \tag{7.7}$$

## 7.3 CONTROLLER DESIGN USING RAGAZZINI METHOD

Let us assume that the FF perfectly rejects the voltage disturbances from the grid. It follows that we can focus solely on the output system response to the current reference. Accordingly, the simplified block diagram of the control system in the discrete domain, considering no influence of the disturbance on the system output $i(k)$, is shown in Fig. 7.5. The output-reference transfer function, also $G_{\text{Cl}}(z) = \frac{I(z)}{I^*(z)}$, of the discrete system shown in Fig. 7.5 can be expressed as (7.8). Furthermore, the Ragazzini method states that given

a desired closed-loop transfer function $G_{Cl}(z)$, the controller can be explicitly solved as in (7.9) [220].

$$G_{Cl}(z) = \frac{I(z)}{I^*(z)} = \frac{C(z)P(z)}{1 + C(z)P(z)} \tag{7.8}$$

$$C(z) = \frac{1}{P(z)} \frac{G_{Cl}(z)}{1 - G_{Cl}(z)} \tag{7.9}$$

The controller $C(z)$ must be designed to produce a stable closed-loop system, and at the same time, it should be a causal transfer function. The causality of $C(z)$ is ensured if $G_{Cl}(z)$ has a delay at least as long as the delay on $P(z)$. Differently said, $G_{Cl}(z)$ should have the same or a higher pole-zero deficit than $P(z)$ [220]. If $P(z)$ is stable, as in our discrete plant, the design is greatly simplified, and the big challenge is the selection of an appropriate target closed-loop transfer function $G_{Cl}(z)$. Although it will be possible to select the poles and zeros of $G_{Cl}(z)$ directly in the z-domain, a method to simplify the design process is to choose a continuous transfer function $G_{Cl}(s)$ with a particular set of characteristics that fulfill the specifications imposed over the closed-loop. Afterwards the transfer function $G_{Cl}(z)$ can be obtained by applying pole-zero matching transformation over $G_{Cl}(s)$ [233]. On account of this, it is feasible to select as template for the continuous transfer function $G_{Cl}(s)$ a second-order system with damping factor $\zeta = 0.6$ and natural frequency $w_n = 2\pi f_{Sw}$. Notice that we are pushing the bandwidth of the desired closed current loop very close to the limit dictated by the Nyquist frequency. At the same time, enough damping is provided by $\zeta = 0.6$ such that big overshoots will be avoided. Thereafter, the target transfer function $G_{Cl}(z)$ can be obtained using Pole-zero matching (MPZ) over $G_{Cl}(s)$. Notwithstanding, in order to meet the causality of $C(z)$, a unit delay $z^{-1}$ must be added to the desired transfer function. Altogether, the complete target closed-loop transfer function can be calculated as follows:

$$G_{Cl}(z) = MPZ\{G_{Cl}(s)\}z^{-1} \tag{7.10}$$

$$G_{Cl}(z) = MPZ\{\frac{{w_n}^2}{s^2 + 2\zeta w_n s + {w_n}^2}\}z^{-1} \tag{7.11}$$

$$G_{Cl}(z) = \frac{(Cz + J)z^{-1}}{z^2 + Dz + E} \tag{7.12}$$

where the coefficients $C$, $J$, $D$ and $E$ depend on the choice of $T_s$. The mentioned coefficients can be calculated using scientific software. For example using the command *c2d($G_{Cl}(s)$,Ts,'matched')* in MATLAB. Finally the controller transfer function can be found by replacing (7.7) and (7.12) in (7.9) which yields:

$$C(z) = \frac{1}{\frac{V_{dc}}{2}\frac{b}{z(z-a)}} \frac{\frac{(Cz+J)z^{-1}}{z^2+Dz+E}}{1 - \frac{(Cz+J)z^{-1}}{z^2+Dz+E}} \tag{7.13}$$

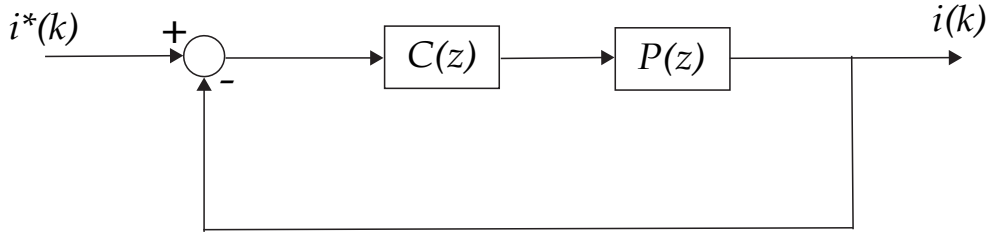



**Fig. 7.5:** Block diagram of the discrete control system

$$C(z) = \frac{2}{bV_{\mathrm{dc}}} \frac{Cz^3 + (J - aC)z^2 - (aJ)z}{z^3 + Dz^2 + (E - C)z - J} \tag{7.14}$$

## 7.4 FREQUENCY RESPONSE - COMPARATIVE EVALUATION

A comparative evaluation is carried out in terms of frequency response between a current controller designed with conventional methods and a current controller designed with the Ragazzini Method. For such comparison, two current controllers are designed. A coupling inductor of $L = 100\mu H$ with an internal resistance of $R = 1.6m\Omega$ and a VSC switching frequency of $f_{Sw}$ = 20 kHz are considered for the control design. In addition, the DC-Bus voltage $V_{\mathrm{dc}}$ is set as 750 V. Certainly, a switching frequency of 20 kHz leads to a PWM sampling frequency of 40 kHz and a sampling time equal to $T_s = 25\mu s$ when double update is considered.

### 7.4.1 *Current Control Design using the Conventional Method*

Indeed, the plant to be controlled can be modeled as a first order system with the transfer function presented in (7.3). In such a case, the optimal continuous current controller has the form of a PI controller $C_{\mathrm{PI}} = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s}$ [170]. With this in mind, it is possible to design a PI controller according to the approach suggested in [167]. This approach states that given a desired phase margin $\phi_{\mathrm{m}}$ (set as $\phi_{\mathrm{m}} = 60^\circ = \frac{\pi}{3}$ for the current design) the recommended cross over frequency can be calculated as:

$$w_{\mathrm{c}} = \frac{(\pi - 2\phi_{\mathrm{m}})}{3T_{\mathrm{s}}} = 13963\ rad/s \tag{7.15}$$

This cross over frequency can be achieved setting the proportional gain and integral gain as $K_{\mathrm{P}} = \frac{2w_{\mathrm{c}}L}{V_{\mathrm{dc}}} = 0.0037A^{-1}$ and $K_{\mathrm{I}} = \frac{w^2{}_{\mathrm{c}}L}{5V_{\mathrm{dc}}} = 5.199A^{-1}s^{-1}$ respectively. Subsequently, the discrete version of the PI controller can be obtained through the Tustin transformation with prewarping at the crossover frequency $w_{\mathrm{c}}$ which leads to:

$$C_{\mathrm{PI}}(z) = \frac{0.003789z - 0.003658}{z - 1} \tag{7.16}$$

### 7.4.2 *Current Control Design using the Ragazzini Method*

The second current controller for the comparison, namely the current controller based on the Ragazzini method, is designed using the procedure described in section 7.3. A sampling time of $T_s$ = 25 $\mu s$ and a switching frequency $f_{\mathrm{Sw}}$ of 20 kHz lead to the template transfer function $G_{\mathrm{Cl}}(s)$,defined in (7.11), as:

$$G_{\mathrm{Cl}}(s) = \frac{8.883e09}{s^2 + 1.131e05s + 8.883e09} \tag{7.17}$$

and coefficients $C = J = 0.6344$, $D = 0.2457$ and $E = 0.0231$ for the discretization. The controller defined by (7.14) becomes finally:

$$C_{\mathrm{Raga}}(z) = \frac{0.006769z^3 - (4.229e - 06)z^2 - 0.006764z}{z^3 + 0.2457z^2 - 0.6113z - 0.6344} \tag{7.18}$$

### 7.4.3 *Closed loop bandwidth discussion*

Considering the plant transfer function $P(z)$ as (7.7), the output to reference transfer function $G_{\text{Cl}}(z)$ as defined in (7.8) is calculated once with $C(z) = C_{\text{PI}}(z)$ leading to $G_{\text{PI}}(z)$ and once with $C(z) = C_{\text{Raga}}(z)$ leading to $G_{\text{Raga}}(z)$. The frequency response of both transfer functions can be seen in the Bode plot depicted in Fig. 7.6. Notice that the frequency response is just valid until 20 kHz. In other words, it is just valid until the Nyquist frequency of the sampled system. Recalling that the bandwidth of the closed-loop is defined as the frequency where the amplitude becomes -3 dB, the bandwidth of the resulting closed-loop response $G_{\text{PI}}(z)$ and $G_{\text{Raga}}(z)$ are 5.3 kHz and 13.5 kHz respectively. Here there is an improvement of 2.5 times in terms of bandwidth achieved by the Raggazini-based design. Moreover, by observing the phase plot, it is possible to see that the $G_{\text{Raga}}(z)$ controller provides a smaller phase lag than the $G_{\text{PI}}(z)$ controller, especially at high frequencies. Such reduction in the phase lag has a positive impact on the tracking capability of the current controller and ultimately on the stability of the active damper.

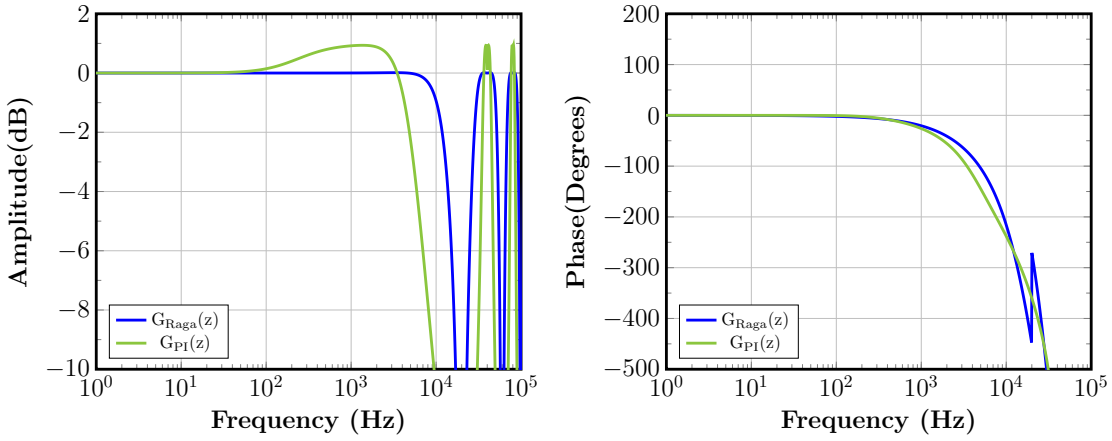



**Fig. 7.6:** Closed loop frequency response of the current loop. Process controlled by the PI with the conventional design in green and with the Ragazzini based current controller in blue.

## 7.5 SIMULATION VALIDATION

In order to assess and compare the performance of the current control designs, an active damper is simulated in Simulink with elements of the Simscape Specialized Library. Once again, the scenario is similar to the one depicted in Fig. 4.6. Likewise, the simulation's parameters are set as in Table 4.1. However, for the simulations in this chapter, the ripple filter capacitance was decreased from $C_F = 250\mu F$ to $C_F = 150\mu F$. This was done with the idea of minimizing the ripple filter capacitor as much as possible and improving the active damper's stability only through the current controller. Furthermore, in the simulations performed in this chapter, the active damper is activated and connected to the power system at $t$ = 0.15 s. Moreover, the first two simulations are carried out by setting a reference for the active damper of $R_s = 250\,m\Omega$. Next, the third and fourth simulations presented in this chapter were performed by setting $R_s = 120\,m\Omega$.

### 7.5.1 *Active damper driven by conventional PI controller*

The first simulation is performed using the PI controller defined in (7.16) as inner current controller, with one current controller for each phase. In this regard, the behavior of the grid voltages at the PCC obtained in the first simulation can be seen in Fig. 7.7. Likewise, the compensating currents performed by the active damper in the first simulation can be seen in Fig. 7.8. The $THD_V$ without active damper is 8.20 %. Such large voltage distortion arises due to the resonance condition produced by the inductive impedance of the grid and the capacitor bank. Indeed, this resonance is excited by the nonlinear load currents. When the active damper is activated, it injects compensating currents with a RMS value of 62.16 A per phase and decreases the $THD_V$ at the PCC to 6.21 %. Furthermore, the voltages at the PCC and the compensating currents $i_C$ injected by the active damper are measured and analyzed through Fourier analysis (FFT) to determine their amplitudes and the phase difference at the different harmonic frequencies. The results of the Fourier analysis are written in Table 7.1.

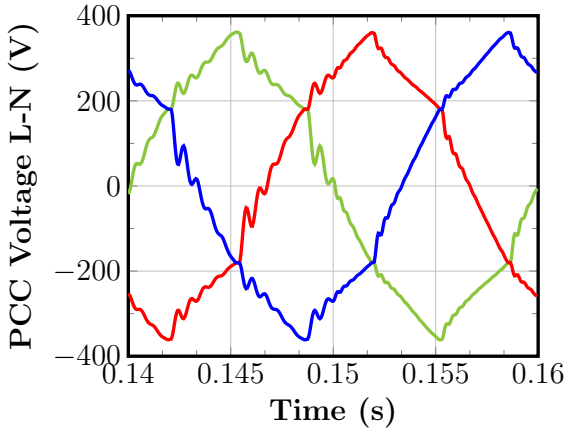



**Fig. 7.7:** $V_{PCC}$ measured, the active damper is activated at $t$=0.15 s. The active damper has a reference equal to $R_s = 250\,m\Omega$ and driven by $C_{PI}(z)$

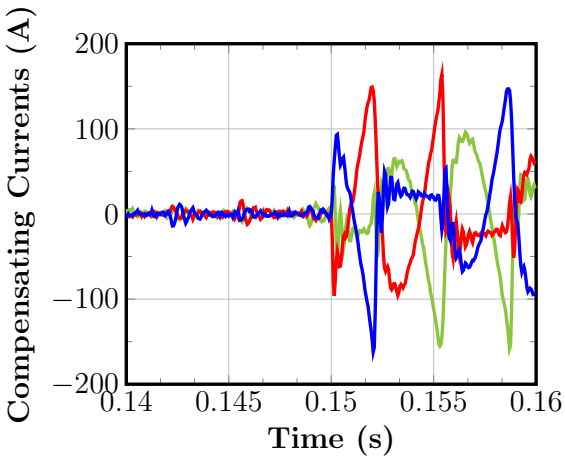



**Fig. 7.8:** Compensating currents $I_C$ injected by the active damper when the reference for the emulated resistance is set as $R_s = 250\,m\Omega$ and the CC is $C_{PI}(z)$

**Table 7.1:** Active damper driven by conventional current controller - Emulated harmonic resistance measured through FFT (Phase A)

| Harmonic Order | $V_{PCC}$(V) | $I_{Ch}$(A) | $R_s(m\Omega)$ | $\theta_h(^\circ)$ | $P_h(W)$ |
|---|---|---|---|---|---|
| 1 | 229.35 | 4.00 | 57000.36 | -148.18 | -779.17 |
| 5 | 10.51 | 45.00 | 230 | -0.10 | 473.06 |
| 7 | 7.79 | 34.47 | 230 | 3.46 | 268.15 |
| 11 | 2.57 | 11.52 | 220 | 19.36 | 27.97 |
| 13 | 2.67 | 12.49 | 210 | 18.64 | 31.59 |
| 17 | 1.56 | 6.26 | 250 | 31.55 | 8.33 |
| 19 | 1.41 | 7.20 | 200 | 33.51 | 8.46 |
| 23 | 1.09 | 4.08 | 270 | 43.26 | 3.25 |
| 25 | 0.95 | 4.83 | 200 | 49.31 | 2.99 |
| 31 | 0.77 | 3.85 | 200 | 63.42 | 1.33 |
| 35 | 0.82 | 2.38 | 350 | 50.61 | 1.25 |
| 37 | 0.69 | 3.25 | 210 | 77.69 | 0.48 |
| 41 | 0.83 | 2.63 | 320 | 56.62 | 1.21 |
| 43 | 0.73 | 2.92 | 250 | -272.15 | 0.08 |
| 47 | 0.82 | 2.62 | 310 | 57.88 | 1.14 |
| 49 | 0.69 | 2.80 | 250 | 92.68 | -0.09 |

### 7.5.2 *Active damper driven by Ragazzini-based current controller*

A second simulation is carried out with the active damper driven by the Ragazzini-based current controller defined in (7.18). For this simulation, Fig. 7.9 **a)** and Fig. 7.9 **b)** show the behavior of the PCC voltages and compensating currents respectively. In the second simulation, the active damper reduces the $THD_V$ at the PCC from 8.20 % to 6.19 %. Moreover, the compensating currents have an RMS value of 58.25 A. As in the previous subsection, Table 7.2 shows the Fourier Analysis results for the second simulation to

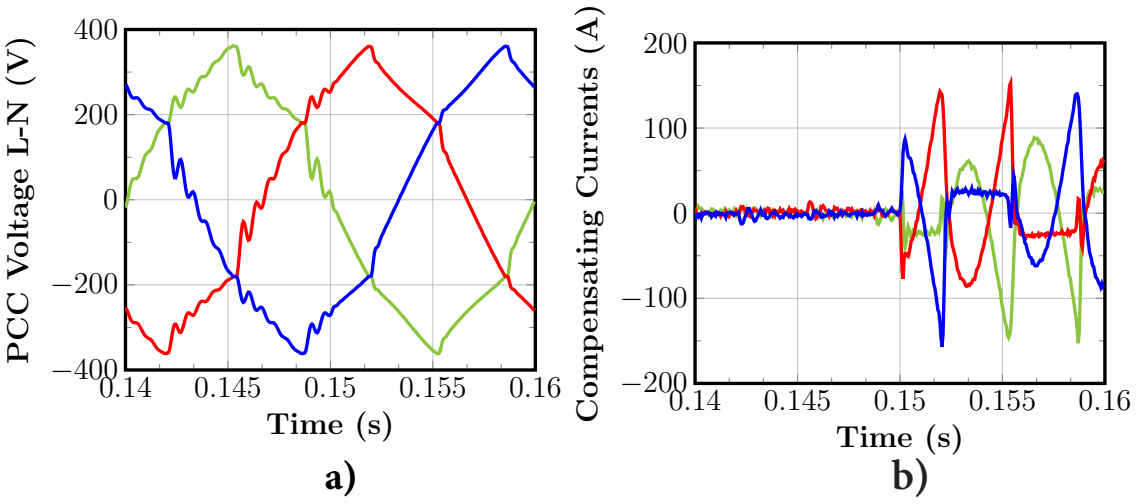



**Fig. 7.9: a)** $V_{PCC}$ measured, the active damper is activated at $t$=0.15 s. The active damper has a reference $R_s = 250\,m\Omega$ and driven by $C_{Raga}(z)$ **b)** $I_C$ injected by the active damper when the reference for the emulated resistance is set as $R_s = 250\,m\Omega$ and the current controller is $C_{Raga}(z)$.

evaluate the emulated resistance performed by the Ragazzini-driven active damper. If we compare the results of Tables 7.1 and 7.2, we can extract the magnitude and the phase of the emulated impedance achieved for each current controller. Such information is summarized in Fig. 7.10 **a)** for the impedance's magnitude and in 7.10 **b)** for the impedance's phase. From Fig. 7.10 **a)**, it can be seen that the Ragazzini-driven active damper performs an emulated resistance closer to the 250 $m\Omega$ reference set for many harmonic frequencies. The only exceptions are the harmonic orders 43rd and 47th, where the PI-driven active damper performs a little bit closer to the $R_s = 250\ m\Omega$ than the active damper implemented with the current controller designed with the Ragazzini Method. In terms of phase, resistive behavior is achieved if the phase of the emulated impedance tends to zero degrees. Fig. 7.10 **b)** shows that the active damper driven by the Ragazzini current controller always exhibits a smaller phase shift for all harmonics frequencies than the PI current controller driven active damper. Thus, the Ragazzini-driven active damper performs better as virtual harmonic resistance than its PI-driven active damper counterpart.

**Table 7.2:** Active damper driven by Ragazzini based current controller - Emulated harmonic resistance measured through FFT (Phase A)

| Harmonic Order | $V_{PCC}$(V) | $I_{Ch}$(A) | $R_s(m\Omega)$ | $\theta_h(^\circ)$ | $P_h(W)$ |
|---|---|---|---|---|---|
| 1 | 229.35 | 4.00 | 57000.36 | -148.18 | -779.17 |
| 5 | 10.50 | 42.42 | 250 | 1.77 | 445.21 |
| 7 | 7.89 | 32.23 | 240 | 4.63 | 253.50 |
| 11 | 2.66 | 10.57 | 250 | 15.62 | 27.07 |
| 13 | 2.79 | 11.70 | 240 | 16.58 | 31.28 |
| 17 | 1.68 | 6.35 | 270 | 26.24 | 9.59 |
| 19 | 1.53 | 6.60 | 230 | 27.02 | 8.97 |
| 23 | 1.24 | 4.30 | 290 | 34.23 | 4.41 |
| 25 | 1.00 | 4.53 | 220 | 39.77 | 3.49 |
| 31 | 0.76 | 3.45 | 220 | 49.65 | 1.70 |
| 35 | 0.86 | 2.71 | 320 | 45.51 | 1.63 |
| 37 | 0.66 | 2.91 | 230 | 58.19 | 1.01 |
| 41 | 0.79 | 2.25 | 350 | 49.68 | 1.15 |
| 43 | 0.57 | 2.57 | 220 | 65.01 | 0.62 |
| 47 | 0.70 | 2.09 | 340 | 53.44 | 0.87 |
| 49 | 0.54 | 2.35 | 230 | 75.96 | 0.31 |

### 7.5.3 *Stability limit assessment*

Next, two new VSAPF's simulations are performed with reference $R_s = 120\ m\Omega$ for the emulated resistance. The power system's initial $THD_V$ without active damper is 8.20 %. The results of the active damper driven by the $C_{PI}(z)$ as current controller can be seen in Fig. 7.11 **a)** and with the active damper driven by the Ragazzini-based current

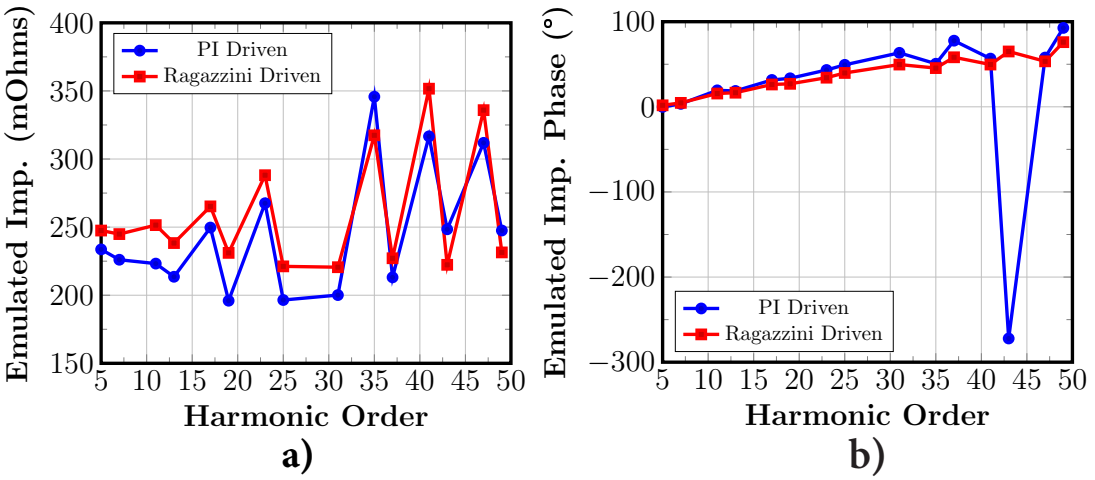



**Fig. 7.10:** Measured magnitude of the emulated impedance performed by the active damper driven by PI current and Ragazzini based current controllers

controller in Fig. 7.11 **b)**. From Fig. 7.11 **a)**, it can be seen that when the PI-based current controller drives the active damper, instabilities arise, and the voltage distortion is increased up to 16.94 %. In contrast, when the active damper is driven by $C_{\text{Raga}}(z)$ as current controller, the active damper suppresses the resonance successfully and decreases the $THD_{\text{V}}$ to 5.51 % as can be seen in Fig. 7.11 **b)**. Furthermore, other simulations have shown that the active damper driven by $C_{\text{PI}}(z)$ is stable only until $R_s = 200\ m\Omega$. On the other hand, in the case of the active damper driven by $C_{\text{Raga}}(z)$, the stability limit is found to be around $R_s = 100\ m\Omega$. Altogether, it can be concluded that the current controller designed according to the Ragazzini method pushes the stability limit of the active damper forward.

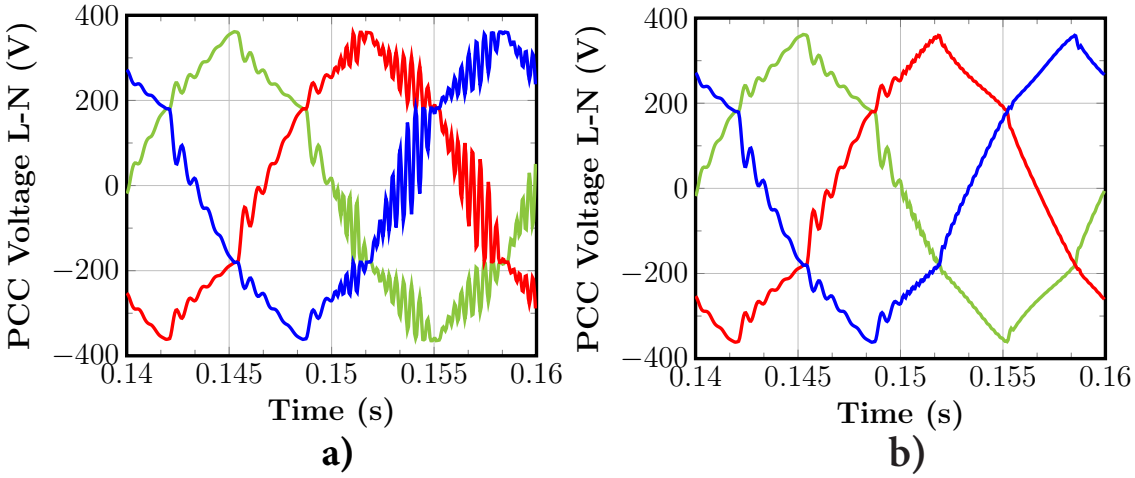



**Fig. 7.11:** $V_{\text{PCC}}$ measured in presence of the active damper with reference $R_s = 120m\Omega$ **a)**Active damper driven by $C_{\text{PI}}(z)$ **b)** Active damper driven by $C_{\text{Raga}}(z)$.

## 7.6 CHAPTER SUMMARY

This chapter has shown the design of current controllers with the Ragazzini method. The design leads to current closed-control loops with larger bandwidth than designs that use traditional PI controllers mapped to the z-domain. Naturally, the increased bandwidth is a welcome feature that enhances the active damper performance while pushing forward its stability limit. Truly, this chapter provided the details of the controller derivation using the Ragazzini method in a mathematical sense. In addition, a theoretical comparative evaluation in terms of frequency response between the proposed current controller and a conventional PI current controller was performed. It was shown that the closed current loop bandwidth is increased by three times when the Ragazzini Method is applied instead of the PI controller's conventional design method. Finally, simulation results confirmed the improved performance of the Ragazzini-driven active damper in terms of harmonic resistance emulation and stability.

# 8

# Conclusions and Outlook

Power grids are large and complex systems that consist of many linear and nonlinear loads highly interconnected. Indeed, many conventional loads have been replaced by power-electronics-based systems as final users pursue to improve the efficiency and controllability of their processes. The latter has led to a huge proliferation of nonlinear loads over the last time. Indeed, the problem of concern is that voltage distortion is created by the interaction of the harmonic currents drawn by nonlinear loads and the power system impedance. Certainly, the power system impedance is determined to a large extent by the inductive and capacitive elements connected to the power system. In this regard, it is well known that parallel resonances arise when the impedances of inductive and capacitive elements connected to the system become equal at a specific frequency. On the same note, recent studies found that the active control in power-electronics converters can also produce additional parallel resonances. Indeed, outer and inner controllers in converters' control systems and synchronization Phase-Locked-Loop (PLL)s influence these power electronics-generated resonances. In any case, the troublesome situation is when a resonance is aligned with the frequency of one of the harmonic currents generated by the nonlinear loads. If a parallel resonance is excited, harmonic currents and voltages are magnified by several orders of magnitude due to the resonance condition. This catastrophic amplification of harmonic voltages and currents degrades the efficiency of the power system and can potentially damage the electrical devices connected to it.

The conventional method to combat resonances in distribution power systems (e.g., industrial grids) is through passive dampers. These passive dampers are installed parallel to the loads in the power system to provide damping. In detail, passive dampers are formed by inductors and capacitors that reject currents at the nominal frequency and by an important share of resistive elements that dominate the passive damper impedance at harmonic frequencies. However, passive dampers are not flexible solutions, and observations indicate that they exhibit significant power losses due to the flow of harmonic currents. Indeed, passive dampers absorb harmonic active power from the power system at harmonic frequencies, and the problem of concern is that they dissipate this power as heat on their resistive elements leading to energy waste. On the other hand, the alternative to the passive damper is its power-electronics counterpart, the active damper. An active damper is a power converter that emulates a virtual resistance at harmonic frequencies. Indeed, very little was known about the harmonic power absorption on active dampers or VSAPFs. On account of this, this PhD dissertation has investigated the active damper regarding its harmonic power processing capability and analyzed in great detail the mechanisms of harmonic active power recovery. Moreover,

this thesis has also investigated potential power savings in an industrial facility brought by an active damper. In this regard, power balance flow studies under non-sinusoidal conditions were conducted to study the reduction in the fundamental power demanded by an industrial grid that has connected an active damper featuring harmonic power recovery.

Furthermore, this PhD thesis was organized in eight chapters. Truly, Chapter 1 introduced the background and the research problem tackled by this PhD work. Subsequently, Chapter 2 presented the state-of-the-art in shunt active power filters, and Chapter 3 presented a comprehensive description of SiC semiconductor technology. This technology has been proven to be fundamental for the recovery of harmonic active power and the enabler to achieve an ultra-low losses active damper. Moreover, the most important findings of this PhD thesis were presented in Chapters 4 to 7. Finally, due to the limits imposed on the length of this dissertation, other scientific findings in the area of control of power-electronics converters and VSAPF´s stability obtained along this PhD work are presented in the appendices.

## 8.1 MAIN FINDINGS

The main findings of this PhD thesis can be summarized as follows:

- **Chapter 4** has investigated the active damper and its interaction with the industrial grid from a power exchange point of view. In fact, this interaction was mathematically described based on the fundamental physics law of energy conservation, the energy stored in capacitors/inductors, and the working principles of the active damper. By working out all these elements, the power balance equation of the active damper was obtained. This equation is a mathematical model that describes how an active damper transforms harmonic active power and recovers harmonic power. Such an equation is a modest contribution to the body of knowledge. The theoretical implication of the power balance equation is that the harmonic power recovery process takes place inherently through the DC-Bus voltage controller. The latter adjusts the fundamental power delivered to the grid in function of the harmonic active power absorbed in order to maintain the DC-Bus equilibrium. Besides, the equation highlights an important practical implication: the harmonic power recovery feature is enabled by an ultra-low losses active damper. A second, even more modest contribution to the body of knowledge is the mathematical derivation of two prediction formulas. These formulas can be used to estimate the amount of harmonic power that is absorbed during the active damper´s operation. The validity of the power balance equation and the prediction formulas were tested first through numerical computer simulations. These computer simulations were carried out using the multi-domain software platforms MATLAB-Simulink, PLECS, and GeckoMagnetics. Additionally, a test bench was used to evaluate the performance of an active damper prototype constituted by a two-level SiC power circuit. It is granted that the test bench and the real prototype were developed in conjunction with the research partner Condensator Dominit. In effect, the power balance equation and prediction formulas were also validated experimentally by measurements obtained on the SiC active damper prototype. In any case, there is an excellent agreement between the computer simulation results and the experimental measurements in the active damper´s prototype. Altogether, the simulation and experimental results support the case of this PhD thesis and the mathematical anal-

ysis performed in this chapter. Lastly, this chapter proves the hypothesis that an active damper with ultra-low losses transforms and recovers a significant amount of harmonic active power.

- **Chapter 5** presented the study of the power balance flow of a distribution power system that included an ultra-low losses active damper with harmonic active power capability. Specifically, the study of the power exchange between utility, loads, and active damper under non-sinusoidal conditions was carried out according to the Buchholz-Emmanuel power theory and through computer simulations. The Buchholz-Emmanuel theory was selected because it highlights and recognizes the importance of harmonic and fundamental active powers on the overall power balance flow. Accordingly, the power balance flow was studied in three different power system scenarios. First, the simulation of an uncompensated distribution power system was carried out, and the power exchange among the different elements of the system was captured. This was done to obtain a benchmark for the comparative analysis. Second, a power balance flow study was carried out in the distribution power system subjected to the action of a passive damper. Third, the power balance flow study was performed for the same industrial grid as in the two previous scenarios, but an ultra-low losses active damper was considered in the simulation. The computer simulations have shown that the harmonic mitigation capability of passive and active dampers are very similar. In addition, the simulations have demonstrated that the nonlinear loads behavior change when either the passive or the active damper are connected to the system. Specifically, the nonlinear loads absorb more fundamental power than in the uncompensated case. Nevertheless, analyzing the power balance flow in the three scenarios, it can be concluded that the ultra-low losses active damper brings benefits in terms of fundamental active power reduction. In particular, it was found that the active damper with harmonic recovery function achieves a 1.4% reduction in fundamental active power demanded from the utility compared to the passive damper. Furthermore, and to quantify the effectiveness of a power filter to reduce harmonic distortion and fundamental power demanded from the mains simultaneously, two FOMs are proposed in this chapter. In particular, the metrics proposed are the products $FOM_1 = P_1 \cdot THD_V$ and $FOM_2 = P_1 \cdot THD_I$. In terms of the FOMs proposed in this chapter, the active damper outperforms the passive damper by a 4.52% when harmonic voltage distortion and fundamental active power reduction are considered simultaneously.

- **Chapter 6** addressed the question about which power circuit topology is the most suitable for the ultra-low losses active damper with harmonics power recovery functionality. In other words, the question was which power circuit topology exhibits the lower power losses amid the harmonic virtual resistance. To this end, Chapter 6 presented the comparative evaluation of four power circuit topologies, all full-SiC based, for the active damper. In particular, three conventional topologies and one non-conventional topology (3L-ASYM) were compared in terms of power losses in this chapter. It is granted that the lower the power losses on the active damper, the higher the amount of harmonic active power that can be recovered from the power system. In fact, in applications such as motor drives, and grid-tie inverters, other scientific studies found that the SiC based 3L-TNPC exhibits the highest efficiency among all the conventional topologies. However, in the case of the VSAPF application, the SiC based 3L-TNPC has a true competitor in the non-conventional SiC based 3L-ASYM topology. In effect, the comparative analysis

performed in this chapter revealed that the 3L-TNPC and 3L-ASYM topologies exhibit the lowest losses among all the SiC based topologies. In particular, the 3L-ASYM topology exhibits an efficiency slightly lower than the T-Type converter for switching frequencies below 60 kHz. And yet, the 3L-ASYM topology starts to be more efficient than the T-Type converter at switching frequencies greater than 70 kHz. On the other hand, for high current ratings, three-level SiC power modules are currently unavailable in the market. This is because it is always difficult for semiconductors manufacturers to justify the development of a new three-level converter module; they always need to look at the demand if there is a market big enough for such a development. The proposed non-conventional topology has the main advantage that it can be constructed cascading two-level commutation cells. In effect, the cascaded connection is made by connecting the AC terminal of one module to the positive terminal of the second module. Thus, converter manufacturers can have a stock of just half-bridge SiC MOSFETs to produce both classes of converters: two-level and 3L-ASYM converters. On the whole, the results presented in this chapter lead to the conclusion that the SiC based 3L-TNPC and 3L-ASYM topologies are the most suitable ones to maximize the recovery of harmonic active power through an active damper.

- **Chapter 7** presented the design of current controllers using the Ragazzini method. One of the conclusions reached in chapter 7, specifically in subsection 7.5.3, was that the inner closed-loop current controller plays a significant role in the VSAPF´s stability. In fact, the current closed loop´s bandwidth determines very much the stability limit of the active damper. Therefore, and given that most current controllers are implemented in digital form, this chapter explored the direct discrete design of current controllers using the Ragazzini method. Indeed, this chapter walked through the detailed design of a Ragazzini-based current controller and showed that the current controller's bandwidth is increased by a factor of three using this technique compared to traditionally designed PI controllers mapped to the z-domain. The increased bandwidth is a welcome feature that enhances the active damper performance while pushing forward its stability limit. All in all, this chapter and associated paper pioneered the design of current controllers using the Ragazzini method.

## 8.2 FUTURE RESEARCH

Indeed, the interaction between VSAPF and a power system is very complex. Although this PhD work has studied the interaction between a VSAPF and a balanced power system from an power exchange point of view, the dynamic interaction between VSAPF and the power grid in terms of stability remains largely unexplored. On this basis, there are three paths where further research on the active damper with harmonic power recovery capability can be carried out. First, the active damper's power circuit can be improved to minimize power losses to a major extent. By doing so, an even more significant amount of harmonic active power can be processed and recovered. Second, improvements in the active damper's control system can be made to enhance the active damper's stability further. Third, the study of the power exchange between the VSAPF and an unbalanced power system subject to harmonic pollution can be performed. More details about these three paths for future research are discussed in the following.

### 8.2.1 *Further power losses minimization in the active damper*

Regarding the active damper's power circuit, research can be carried out in power topologies that achieve lower losses than the topologies presented in this PhD work. It is granted that this PhD dissertation has mostly dealt with the two-level power circuit, although this topology is not the best in terms of power losses as can be seen in Fig. 6.14. The reason for this was the nature of the research project in which this PhD work was involved. Specifically, the industrial-academic research collaboration between the South Westphalia University of Applied Sciences and the company Condensator Dominit. On account of this, a conservative approach was taken in selecting the power topology for the active damper. Naturally, the industry perspective was to use a well-known, deeply understood, and among all, a field-proven power-electronics circuit for the product development. For this reason, most of the development and experimental results obtained in this thesis are related to the two-level topology. Nevertheless, other topologies can achieve better performance, as illustrated by the studies carried out in section 6.2.3. Truly, the three-level topologies 3L-TNPC and 3L-ASYM outperform the two-level power circuit in terms of power losses and probably in terms of power density as well. Obviously, multilevel topologies based on SiC MOSFETs or GaN HEMT semiconductors with more than three levels will reduce the power losses even further. Of course, the costs of a SiC multilevel active damper will increase as a higher number of WBG switches are needed to build a multilevel power circuit. Thus, it is still to be seen in which industrial applications WBG multilevel converters will be economically viable. Indeed, multilevel (> 3L) based SiC grid-tie-converter have been reported in [234]-[235] and with GaN HEMTs in [236, 237]. Still, there is much room for research regarding the power circuit. As new building elements in the form of WBG semiconductors are available for power-electronics engineers, it is possible to think of further innovations in power circuit topologies. The characteristics of WBG semiconductors would allow or enable new paradigms in power electronics circuit design.

For example, consider the CSC circuit discussed in Chapter 2.4. Due to the bulky inductor on the DC-side, the CSC was not so favorable in terms of power density. Also, an additional disadvantage was that nowadays, silicon bidirectional blocking switches are not widely available in the market. Nevertheless, recently, experimental WBG bidirectional blocking devices in the form of Monolithic GaN bidirectional Switches are being tested by Panasonic [238] and by Infineon [239]. If these Monolithic GaN bidirectional switches result successful and they are produced for high current capability (i.e. hundreds of amperes), they can be used to build a high switching frequency CSC´s power circuit for the VSAPF. In such a case, the DC-side inductor can be reduced, and the power density greatly improved compared to a silicon-based CSC power circuit. In addition, according to Jahn et al. in [240], it is expected that CSC power converters built with GaN bidirectional switches will exhibit better EMI behavior and higher temperature operation than SiC-based VSC. Furthermore, it is possible to investigate non-conventional modulation schemes to minimize power losses in VSC. For example, techniques to achieve soft-switching in all switches during current commutation in the entire operating range are thinkable to minimize power losses . In this regard, Lee et al. in [241, 242] are pioneering soft-switching techniques in WBG semiconductors for PFC circuits using interleaving, coupled inductors, and planar magnetics. It might also be possible to investigate these techniques in the VSAPF field. In the final analysis, multiple possibilities and degrees of freedom exist to develop new and improved power circuits for the VSAPF. These circuits can resort to WBG semiconductors to recover an even larger amount of

harmonic active power than the one recovered by the power circuits presented in this work.

### 8.2.2 *VSAPF Stability Improvement*

The VSAPF stability has been the greatest challenge encountered in this PhD work during the active damper's development. In contrast to the active damper, its passive counterpart does not suffer from stability issues. The reason being is that in a passive damper, harmonic currents in phase with the PCC harmonic voltages flow instantaneously through the passive damper. Indeed, in the passive damper's elements, the electrons vibrate back and forth at harmonic frequencies at the speed of light. Unfortunately, in the active damper this is not the case. Because the active damper itself is governed by a digital control system. The digital control system always needs some time to read the analog signals, for the A/D conversion, and for the calculation of the reference currents. In addition, once the references are calculated, the VSC needs some extra time to synthesize the compensating currents through PWM. Due to the described operation of the active damper, the compensating currents always have a phase shift with respect to the actual PCC voltages. For this reason, the active damper suffers from stability issues, specially if the emulated resistance is set to small. The stability of the active damper depends on many factors such as the magnitude of the emulated resistance, the VSC 's switching frequency, the size of the ripple filter capacitor, the equivalent grid impedance, and the loads impedance. For several reasons, a precise stability analysis of the active damper and the power grid is difficult to perform. First, the power grid itself is a time-variant system since loads are being connected and disconnected from the system constantly [243]. Also, the grid impedance is often not known exactly, and it varies with operations carried out on the utility side [1], for instance, by the connection or disconnection of vicinity feeders. Even more troubling is the presence of nonlinear loads. The net effect of these nonlinear loads on the active damper stability is complicated to assess. Useful mathematical models for conventional nonlinear loads such as passive rectifiers cannot be obtained for stability analysis [244]. Therefore, it is not easy to make general statements about the stability of the active damper when nonlinear loads such as passive diodes rectifiers, which do not have an exact transfer function, are involved. Actually, not only the stability of the active damper is a topic that is open for further research. In general, the stability of converters' clusters is a big research topic nowadays [14]. For example, stability analysis in PV and wind farms [41, 245, 246], in data centers [247], and in HVDC systems [43, 248] have been carried out. The cluster stability was analyzed for those particular power systems because all the elements in these power systems were very well known. However, it is not possible to make a general conclusion about the stability of a cluster of converters that varies along the time [14], and the stability needs to be analyzed on a case-by-case basis.

From the experience collected in this PhD thesis, the meaningful degrees of freedom to improve the active damper's stability are the VSC 's switching frequency and the inner current controller. On the one hand, a higher switching frequency makes the active damper more stable for two reasons. First, the higher the switching frequency, the smaller the time needed to synthesize the currents through a VSC. Second, high switching frequencies imply shorter sampling times in the digital control system; thus current references can be calculated more often and faster at high switching frequencies. Notwithstanding, this factor reinforces even more the proposed three-level topology. Because a three-level based VSAPF operating at a high switching frequency will not only

reduce the power losses on the overall active damper but also will improve the stability limit of the VSAPF. Finally, in the author's opinion, improved control schemes and control structures for the inner controller will positively influence the active damper's stability. It has been seen already in Chapter 7 that if the current controller bandwidth is increased, the stability of the active damper will be improved. On this basis, it would be possible to extend the controller's bandwidth by designing unconventional current controllers combining model-based control and data-driven control techniques, as shown by Schoellig in [249]. The latter could improve the current controller tracking and the overall stability of the active damper through an adaptative current controller that learns from a changing power grid environment. Altogether, open research regarding the active damper's stability is more precise models for the stability analysis and improved current controllers for the active damper.

### 8.2.3 *VSAPF's power exchange with unbalanced power system*

As stated in section 1.7.1, this research work was limited to studying the VSAPF's power exchange with a balanced power system subject to harmonic voltage distortion. However, more and more power distribution systems suffer in addition to harmonic voltage distortion from unbalance due to unsymmetrical loads [250]. On this basis, future research can study the interaction of a VSAPF and an unbalanced power system from a power exchange of view. Granted that VSAPFs are not the best solution to combat load balancing problems in power systems [83]. However, for the VSAPF's power exchange studies with an unbalanced power system, the VSAPF should be able to perform harmonic resistance emulation under unbalanced conditions. To this end, the VSAPF's power circuit and the VSAPF's control system presented in section 4.3 need to be modified and adapted. It follows that the investigation of the most suitable power circuit topology and control system for the VSAPF to cope with unbalanced conditions is yet to be performed and it is suggested as future work. Furthermore, the mathematical analysis in subsections 4.4.3 and 4.4.4 assumed a balanced power system. If the aim is to study the VSAPF's power exchange with an unbalanced power system, all the mathematical analysis carried out in subsections 4.4.3 and 4.4.4 needs to be redone. This future mathematical analysis should rework equations (4.30) to (4.49) using positive, negative, and zero sequence terms applying the method of symmetrical components [47, 70]. Arguably, under unbalanced conditions, the form of (4.49) derived in this PhD work will remain with only two particularities. First, the positive-sequence active power $P^{+}{}_{1}$ will appear instead of the fundamental active power $P_1$. Second, under unbalanced conditions, the frequencies involved in (4.36) to (4.38), in (4.47), and in Fig. 4.4 will differ from the frequencies $[6 \cdot 50Hz, 12 \cdot 50Hz, 18 \cdot 50Hz, ...]$ found in the analysis for balanced power systems performed in this dissertation. Of course, an exhaustive and detailed mathematical analysis considering unbalanced conditions must verify the latter statements. Finally, it is also left as future work to expand the power balance flow studies under non-sinusoidal conditions carried out in Chapter 5 to power balance flow studies under non-sinusoidal and unbalanced conditions. The latter investigation will reveal if a VSAPF with harmonic power recovery capability can also reduce the power consumption of an industrial-user under unbalanced conditions.

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## COLOPHON

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