Characterisation of Photodiodes in 22 nm FDSOI at 850 nm

Jelle H. T. Bakker, Mark S. Oude Alink, Jurriaan Schmitz, Bram Nauta
University of Twente, Enschede, The Netherlands, email: j.h.t.bakker@utwente.nl

ESSDERC 2023 - IEEE 53rd European Solid-State Device Research Conference (ESSDERC) | 979-8-3503-0423-7/23/$31.00 ©2023 IEEE | DOI: 10.1109/ESSDERC59256.2023.10268483

***Abstract*—We present the analysis and measurement results of photodiodes (PDs) fabricated in 22 nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology at a wavelength of 850 nm. To the best of our knowledge this is the first paper to give detailed information about PDs in 22 nm FDSOI. FDSOI has the unique opportunity to place a PD in SOI, which is potentially very fast, on top of bulk devices such as PNP-transistors for temperature sensors. Its measured responsivity is 4 µA/W at a bandwidth (BW) of 3.4 GHz. Several bulk PDs, including PW/NW/DNW, PW/DNW/PSUB, and NW/PSUB have also been characterised. They have responsivities between 6 mA/W and 207 mA/W and BWs between 23 MHz and 5.8 GHz. 22 nm FDSOI shows potential for fully-integrated high-speed optical receivers, as it combines ∼90 nm bulk CMOS PD performance with 22 nm RF and digital processing capabilities on a single die.**

***Index Terms*—22 nm FDSOI, 22FDX™, Bulk PDs, PIN-SOI PD, 850 nm PD characterisation**

I. Introduction

Silicon (Si) photodiodes (PDs) can detect 850 nm light, which is used in short-haul (<200 m) high-speed optical communications. Therefore it makes sense to monolithically integrate Si PDs in CMOS. Advantages of this include reduced cost and volume, and removal of an RF interface. Even so, predicting performance can be challenging due to the absence of process design kit models. Information on PDs in 180 nm, 130 nm, 65 nm, and similar CMOS technologies can readily be found [1]–[6], but this is not the case for GlobalFoundries' 22 nm Fully-Depleted Silicon-On-Insulator (FDSOI).

22 nm FDSOI (22FDX™) allows for the fabrication of bulk CMOS and SOI devices in one die. The process provides for quite a few different pn junctions that may be used to create PDs [7] as shown in Fig. 1. In 22 nm FDSOI, high-speed PDs can be combined with compact high-speed RF and digital circuits on the SOI layer. This makes the technology promising for high-speed monolithically integrated optical receivers. As FDSOI is one of the technologies that will be supported by the European chips act [8], its use in optical receivers may become very relevant.

22 nm FDSOI allows for the creation of the following types of PDs that are known for having a high bandwidth (BW): NW or DNW-based PDs without slow PSUB photocurrents [4], Spatially Modulated Light (SML) PDs where slow PSUB currents are measured separately and then cancelled by subtraction [1], avalanche PDs [2], PIN bulk PDs [6], and (potentially) PIN-SOI PDs. The NW or DNW, PIN-SOI PD, and a few other PD types are all designed complying to the standard Design Rule Checking (DRC) ruleset, fabricated, and characterised in this paper.

This project is financed by Bruco Integrated Circuits and Holland High Tech in a public-private-cooperation for research and development in the Hightech Systems & Materials topsector.

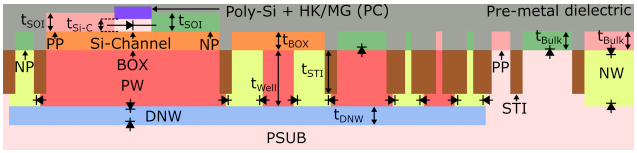


Fig. 1: Layer thickness definitions and p(i)n junctions in 22 nm FDSOI.

Blocking the slow PSUB photocurrent contribution with a NW or DNW is effectively a form of equalisation: it increases the intrinsic BW (BW_i) by reducing the low-frequency response, but without requiring any circuits, to reach BWs of ∼ 6 GHz [4]. Extra circuit-based equalisation at the higher frequencies potentially achieves BWs around ∼13 GHz [5] at low reverse bias voltages ($V_{RB} < 3$ V).

High supply voltages $(3 - 10\,\mathrm{V})$ are usually not readily available, which is important for cost-effective integration. The desired low V_{RB} is the main reason why the other PDs, except for the SML PDs, are not considered. The avalanche PDs have as extra disadvantage higher noise [9], which limits the advantage of a higher responsivity. Lastly, the SML PDs are covered in more metal than non-SML PDs in the same technology. This makes them less suitable for monolithic integration where responsivity is often an important limitation.

This paper is organised as follows: section II details PD considerations and dimensions, section III discusses the created PD layouts, section IV shows the measurement results and a discussion, and section V ends with conclusions.

II. Responsivity and Frequency Response Analysis

Two Figures of Merit (FoMs) are especially important in PDs: responsivity (R), and BW. The total BW (BW_t) is determined by BW_i and electrical BW (BW_e). The BW_i is the limiting factor as long as the PD junction capacitance (C_j) is sufficiently small such that the BW_e with a roll-off of 20 dB/dec does not become dominant. BW_i is determined by the photocurrent response of the PDs, which has a roll-off of 4 dB/dec to 10 dB/dec [6], [10]. The intrinsic photocurrent response is determined by the combination of fast drift currents from the depletion region and slow diffusion currents from the layers outside the depletion region. Depending on the exact PD layout, the used junctions, and assuming a V_{RB} below 3 V, a BW_i between 1 MHz to 6 GHz can be achieved [4], [10].

R is the ratio of photocurrent over optical input power [10]

$$R = \frac{I_{PD}}{P_{O,RX}} = \frac{q_e}{E_p}\eta_{EQE,PD} = \frac{q_e}{E_p}\eta_F\eta_M\eta_A\eta_Y\eta_C\ [\mathrm{A/W}]. \quad (1)$$

TABLE I: ESTIMATED THICKNESS AND CALCULATED η_A.

PD	Junction	Calculation	t [µm]	η_A
PD_1	(NW, DNW)/PW	$t = t_{Well} - t_{STI} + \frac{1}{2}t_{DNW}$	0.750	0.03
	(NW, DNW)/PSUB	$1 - \eta_A$ of upper junction		0.97
PD_2	(NW, DNW)/PW	$t = t_{Well} - t_{STI} + \frac{1}{2}t_{DNW}$	0.750	0.03
	(NW, DNW)/PSUB	$1 - \eta_A$ of upper junction		0.97
PD_3	PP/NW	$t = t_{Bulk} + \frac{1}{2}t_{Well}$	0.223	0.01
	NW/PSUB	$1 - \eta_A$ of upper junction		0.99
PD_4	NP/PSUB	$t = t_{Bulk} + t_{PSUB}$	375	1.00
PD_5	NW/PSUB	$t = t_{NW} - t_{STI} + t_{PSUB}$	375	1.00
PD_6	NP/Si/PP	$t = t_{SOI}$	0.013	0.0005

Here I_{PD} is photocurrent, $P_{O,RX}$ is optical input power, q_e is elementary charge, E_p is photon energy, $\eta_{EQE,PD}$ is external quantum efficiency, η_F is the fraction of $P_{O,RX}$ that is not reflected by permittivity changes in the Back End Of Line (BEOL) layers, η_M is the fraction of total PD area over the area not blocked by metal or other opaque layers, η_A is the fraction of absorbed power, η_Y is the number of Electron-Hole (EH)-pairs produced per absorbed photon (assumed to be 1 in non-avalanche mode [6]), and η_C is the fraction of charge carriers that did not recombine before reaching the metal contacts (assumed to be 0.9, based on calculations for a NW/PSUB PD in 0.18 µm CMOS [6]).

Using the simplified form of the Fresnel equations, on a simplified non-absorbing material stack in 22 nm FDSOI, η_F is estimated to be 0.72 for normal incident 850 nm light. This is reasonably in line with reported results for 250 nm (0.66), 180 nm (0.51), 130 nm (0.88), and 90 nm (0.78) CMOS [6].

η_A can be calculated by using $\eta_A = 1 - e^{-\alpha_{oa} \cdot t}$. Here α_{oa} is the absorption coefficient of Si at 850 nm $\left(\alpha_{oa} \approx 0.0382\,\mu m^{-1}\right)$ [6] and t is the thickness of the individual layers making up the PDs (Fig. 1). More detailed analysis requires process details which are not publicly available.

t_{BOX}, $t_{Si\text{-}C}$, t_{SOI}, t_{Bulk}, and t_{STI} are 20 nm, 6 nm [11], 13 nm, 20 nm, and 220 nm [7], [11], [12] respectively. A common rule of thumb for the NW and PW thicknesses is to take half their minimum lateral length [10]. MOSIS provides a set of rules that is compatible with many technologies, giving a good overview of what reasonable well dimensions are [13]. The geometric mean of the STI thickness ($t_{STI} = 220$ nm, lower boundary [7], [11], [12]) and maximum MOSIS Scalable CMOS well thickness (750 nm, upper boundary [13]) gives an estimate for t_{Well} of 406 nm. t_{DNW} is estimated to be 1.13 µm based on the PW and DNW ratio (2.78) from [14]. Table I shows the resulting estimated η_A. R is estimated to be in the order of 10 mA/W without and 100 mA/W with a PSUB photocurrent contribution for the bulk PDs, and 100 µA/W for the SOI PD.

III. PHOTODIODE LAYOUTS

All PD layouts shown in this section are fully compliant with the standard DRC rule set of 22 nm FDSOI. All six PDs are labelled as PD_i to prevent confusion.

The PSUB photocurrent has a very low BW_i (~10 MHz). PD_1 (PW/NW/DNW) shown in Fig. 2 is specifically designed for high BW_t by removing the PSUB photocurrent. This increases BW_t and decreases C_j at the cost of a lower R (at DC). This cost is not a problem when high overall BW (>10 GHz) is considered. In PD_1 the PW/NW finger width (0.6 µm in Fig. 2) is reduced as much as possible to reduce the travel distance of the charge carriers. Enough vias and wide metal layers are used to reduce series resistance to ~1 Ω, well below the 50 Ω input impedance of measurement equipment.

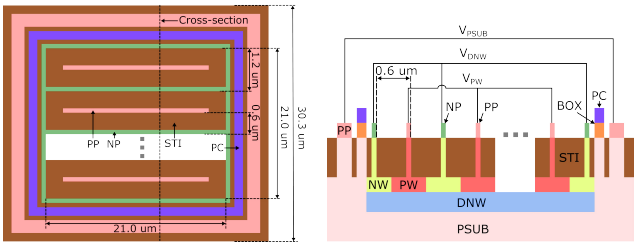


Fig. 2: PD_1 (PW/NW/DNW) layout: (left) top view and (right) cross-section.

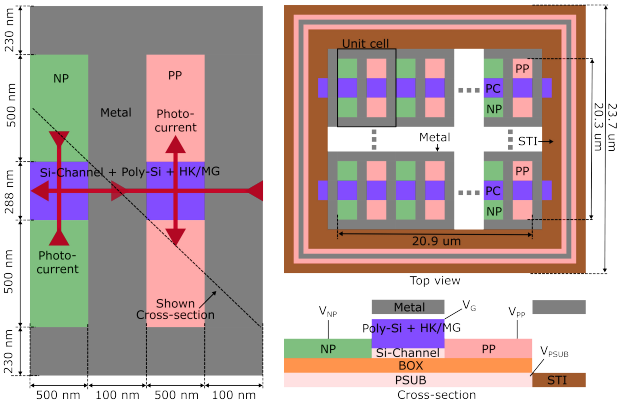


Fig. 3: PD_6 (PIN-SOI) layout: (left) unit cell top view and (right) PD top view and cross-section.

PD_2 (PW/DNW/PSUB) is the same as PD_1, but with only one PW finger to reduce wiring, thereby allowing for more light to reach the Si. This results in a higher responsivity at the cost of higher series resistance and longer travel times for the charge carriers. PD_3 (PP/NW/PSUB) and PD_4 (NP/PSUB) utilize some of the other available junctions.

PD_5 uses NW/PSUB. NW/PSUB PDs are extensively analysed in literature [6], [10], thus making them a good choice to compare technologies and find trends.

Finally, Fig. 3 shows the unit cell of the PIN-SOI PD_6 (NP/Si/PP). This PD allows for placing bulk devices like PNP transistors directly below the PIN-SOI PD. NP and PP are separated by a Si channel because DRC prohibits them from touching. Thus, this forms a PIN-diode, with the intrinsic Si-channel unfortunately blocked by the High-K Metal Gate (HK/MG). This results in photons generating EH-pairs only in the NP and PP regions. These charge carriers have a high recombination probability, due to traps introduced by the via required to connect to the NP and PP, and Auger recombination [15]. Photons will also be lost due to free-carrier absorption [16] caused by high doping levels needed to reduce the resistance in the NP and PP regions. The electric field will therefore also mostly be over the Si-channel, resulting in a reduced drift photocurrent contribution and thus significantly lower responsivity than calculated in section II.

Careful optimisation while staying DRC-compliant results

TABLE II: DC MEASUREMENT RESULTS.

PD	Junction	R [mA/W][a]	V_{BR} [V]	$I_{d,0}$ [A][a]	$I_{d,BR}$ [A][a]
PD_1	(NW, DNW)/PW	6.25	9.5	$6.4 \cdot 10^{-13}$	$1.4 \cdot 10^{-9}$
	(NW, DNW)/PSUB	123	9.8	$2.3 \cdot 10^{-13}$	$1.4 \cdot 10^{-7}$
PD_2	(NW, DNW)/PW	8.26	9.0	$2.7 \cdot 10^{-15}$	$3.9 \cdot 10^{-11}$
	(NW, DNW)/PSUB	199	10.0	$9.9 \cdot 10^{-14}$	$1.2 \cdot 10^{-10}$
PD_3	PP/NW	6.59	8.0	$5.2 \cdot 10^{-13}$	$1.0 \cdot 10^{-8}$
	NW/PSUB	170	10.0	$3.5 \cdot 10^{-13}$	$2.7 \cdot 10^{-9}$
PD_4	NP/PSUB	10.5	7.5	$3.7 \cdot 10^{-12}$	$2.0 \cdot 10^{-7}$
PD_5	NW/PSUB	186	9.5	$1.2 \cdot 10^{-13}$	$6.9 \cdot 10^{-8}$
PD_6	NP/Si/PP	0.0043	-[b]	$2.6 \cdot 10^{-12}$	-[b]

[a] R at $V_{RB} = 0\,V$, $I_{d,0}$ at $V_{RB} = 0.05\,V$, and $I_{d,BR}$ at V_{RB} is 9.4 V, 8.9 V, 7.9 V, 7.4 V, and 9.4 V for PD_1 to PD_5 respectively.
[b] Not measured.

in PD unit cells of approximately $21\,\mu m \times 21\,\mu m$. The PIN-SOI and bulk PDs have a η_M of 0.46 and $\sim$0.83, respectively.

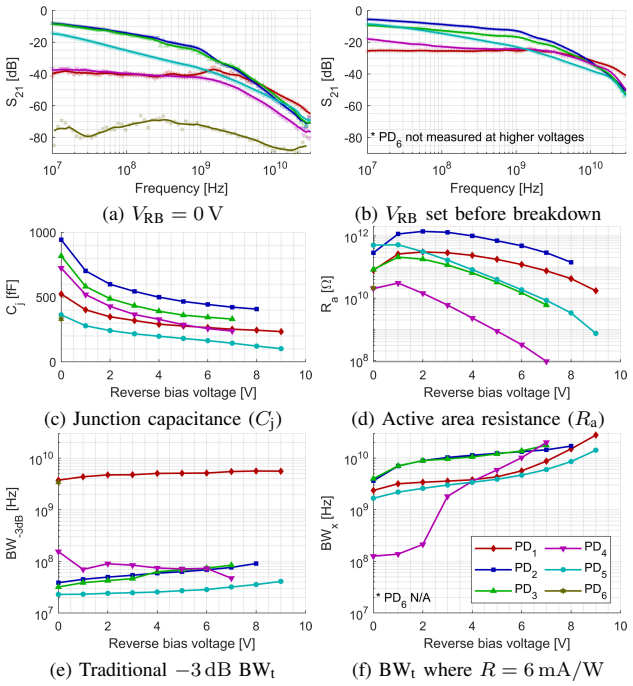
IV. MEASUREMENT RESULTS AND DISCUSSION

All measurements are done on a probe station; IV sweeps with a parameter analyser, responsivity measurements with a custom calibrated 850 nm light source, S-parameters of the bulk PDs with a network analyser and de-embedded Vertical Cavity Surface Emitting Laser (VCSEL), and S-parameters of the PIN-SOI PD with a signal generator and signal analyser due to the high dynamic range required with the low R. For all PDs the RF signal needle is connected to NP, NW, or DNW, except for PD_1 where it is connected to the PW.

Some bulk PDs have multiple junctions and thus multiple V_{BR} (Table II). For minimal dark current (I_d) and I_d/R it is best to use PD_2. The measured R is largely in agreement with the calculations from section II. PD_4 (NP/PSUB) has a shallow junction depth which will result in significantly more recombination in the PSUB below the depletion region plus its diffusion length than with the other bulk PDs.

PD_6 (PIN-SOI) shows lower R than the bulk PDs (Table II) due to 3.2× more opaque surface area and 17× to 75× thinner photon absorption thickness (t) than the bulk PDs. Likely additional factors for the low R are (1) surface recombination in the NP and PP layers due to the relatively many defects caused by the lower ratio between total Si volume and via contact area compared to the bulk Si PDs, (2) recombination in the Si-channel, and (3) the relatively high NP and PP doping concentrations compared to wells in the bulk, which might also result in free-carrier absorption [17].

S_{21} is defined as $S_{21} = \partial P_{E,out}/\partial P_{O,in}$, with $\partial P_{E,out}$ the change in electrical output power (generated current into a 50 Ω load) due to the change in optical input power ($\partial P_{O,in}$). Fig. 4a and 4b show that PD_2 and PD_3 generally have a higher S_{21} than all other PDs due to (1) the large PSUB photocurrent contribution and (2) a second junction which increases the fast drift photocurrent. PD_1 is the best choice (has the best R) at frequencies above 10 GHz. At these higher frequencies, PD_1 has as advantages that (1) the charge carriers have to travel less distance due to the closely-spaced NW and PW fingers and (2) it has a lower C_j as shown in Fig. 4c. R_a and C_j (Fig. 4c and 4d) are the parallel junction capacitance and active area resistance used in the electrical equivalent model. PD_2 to PD_5 are interesting due to their relatively high R. When combined with a circuit-based equaliser they are also candidates for high-speed optical receivers.



(a) $V_{RB} = 0\,V$ (b) V_{RB} set before breakdown
(c) Junction capacitance (C_j) (d) Active area resistance (R_a)
(e) Traditional $-3\,dB$ BW_t (f) BW_t where $R = 6\,mA/W$

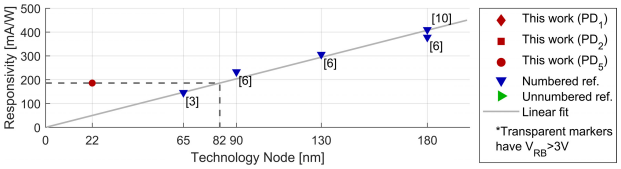
Fig. 4: In Fig. 4b, PD_1: $V_{RB} = 9\,V$, PD_2: $V_{RB} = 8\,V$, PD_3: $V_{RB} = 7\,V$, PD_4: $V_{RB} = 7\,V$, PD_5: $V_{RB} = 9\,V$. There will be an error in the absolute S_{21} between different PD measurements due to the lensed fibre optical probe placement above the PDs. See section III for PD definitions.

Fig. 4a shows that PD_6 (PIN-SOI) has some unexpected behaviour at frequencies below 100 MHz that we could not explain. The BW_{-3dB} of "only" 3.4 GHz is however explained by considering that almost the entire photocurrent is made up of slow diffusion current because the Si-channel is blocked. Although as a bare PD it has poor performance, the PIN-SOI PD may still have some useful applications due to the possibility of placing bulk devices like PNP transistors for temperature sensors directly below the PIN-SOI PD.

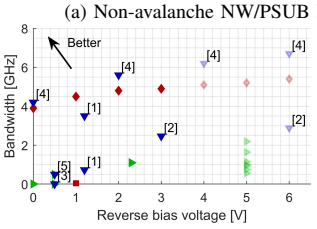
Fig. 4e gives the BW_{-3dB} where the S_{21} is 3 dB lower than the S_{21} at 10 MHz. However, circuit-based equalisation, which is usually always applied to PD-based high-speed receivers, makes the conventional BW_{-3dB} definition less useful. An estimate for input-referred noise current density of a transimpedance amplifier with a BW more than 10 GHz is $7\,pA/\sqrt{Hz}$ [18]. Assuming a 2 mW peak-to-peak optical signal swing, PAM-4 modulation, and a R of 6 mA/W (−40 dB in Fig. 4a and 4b) this results in an SNR of 19 dB for a BER of 10^{-12} [19]. This is why Fig. 4f gives the BW_x for which $S_{21} = -40\,dB$ (6 mA/W).

PD_5 (NW/PSUB) has a R of 186 mA/W. Assuming a linear relationship between the technology node and the R of NW/PSUB PDs (based on [3], [6], [10]), the interpolated equivalent technology node for 22 nm FDSOI is $\sim$90 nm bulk CMOS as shown in Fig. 5a.

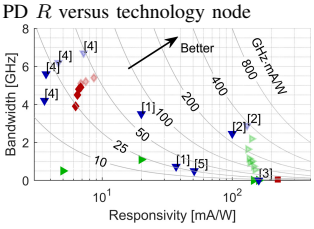
PD_1 is comparable to the best published PDs fabricated in standard CMOS technologies from a BW_{-3dB} and R perspective (Fig. 5 and Table III), but with the added benefit of being fabricated in a technology that is significantly better suited



(a) Non-avalanche NW/PSUB PD R versus technology node



(b) V_{RB} versus BW$_{-3dB}$



(c) R versus BW$_{-3dB}$

Fig. 5: (a) R trend of all NW/PSUB PDs found in literature. (b and c) State-of-the-art non-avalanche Si PDs fabricated in commercial technologies.

TABLE III: NON-AVALANCHE SI PDS FABRICATED IN COMMERCIAL CMOS TECHNOLOGIES.

Ref.	[1]	[2]	[3]	[4]	[5]	This Work PD_1	This Work PD_2
Year	2011	2013	2013	2014	2016	2023	2023
Tech.	180 nm CMOS	180 nm CMOS	65 nm CMOS	180 nm CMOS	65 nm CMOS	22 nm FDSOI	22 nm FDSOI
Junction	NW PSUB	PW NW PSUB	NW PSUB	NP PW	PW DNW	PW DNW	PW DNW PSUB
V_{RB} [V]	1.2	3	0.5	2	0.5	1.0	1.0
R [mA/W]	20	100	160	3.7	51	6.45	224
BW$_{-3dB}$ [GHz]	3.5	2.46	0.006	5.6	0.5	4.50	0.045
BW$_x$[GHz][a]	8.3	> 2.46	> 0.1	–	4.0	3.3	7.1
C_j [fF]	354	–	–	–	480	399	700
A_T [µm^2]	17× 17	50× 50	60× 60	10× 10	50× 50	21× 21	21× 21

[a] BW for which R is 6 mA/W. This R corresponds to -40 dB in Fig. 4.

for high-bandwidth transceivers and high-intensity digital processing. This opens the way to a tightly integrated high-speed optical receiver.

V. CONCLUSION

The responsivities (R) of different bulk PDs fabricated in 22 nm FDSOI are measured to be between 6 and 207 mA/W at a reverse bias of 0 V and the BW$_{-3dB}$ between 23 MHz and 5.7 GHz depending on the PD layout and applied bias. A PW/NW/DNW PD with a BW$_{-3dB}$ of 4.5 GHz and a reverse bias of 1 V shows potential for high-speed optical receivers, with heavy digital on-chip processing as if combining ∼90 nm bulk CMOS PD performance with 22 nm RF and digital processing capabilities on a single die. This PD is the best choice for BW $\gtrsim$ 10 GHz. A PW/DNW/PSUB PD with a R of 207 mA/W and 224 mA/W at reverse bias voltages of 0 V and 1 V is the best if maximal R and standard available bias voltage are required. A PIN-SOI PD in 22 nm FDSOI may have the promise to be ultra-fast (at the cost of R), but was found to be inferior to the bulk PDs with a R of 4 µA/W and BW$_{-3dB}$ of 3.4 GHz. However, it can be placed on top of bulk devices such as PNP-transistors for temperature sensors and therefore may still have some useful applications.

ACKNOWLEDGEMENTS

The authors would like to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program. We also want to thank Anne-Johan Annema, Arnoud Rop, Frans Segerink, Remco Sanders, Jeroen Korterik, Max Krakers, and the late Gerard Wienk (University of Twente) for help with the measurement setups, tape-out, and discussions and Gerard Voshaar, Paul Klatser, and Peter-Paul Vervoort (Bruco Integrated Circuits) for fruitful discussions.

REFERENCES

[1] Shih-Hao Huang, Wei-Zen Chen, Yu-Wei Chang, and Yang-Tung Huang, "A 10-Gb/s OEIC with Meshed Spatially-Modulated Photo Detector in 0.18 µm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1158–1169, May 2011.

[2] F.-P. Chou, G.-Y. Chen, C.-W. Wang, Z.-Y. Li, Y.-C. Liu, W.-K. Huang, *et al.*, "Design and Analysis for a 850 nm Si Photodiode Using the Body Bias Technique for Low-Voltage Operation," *J. Light. Technol.*, vol. 31, no. 6, pp. 936–941, Mar. 2013.

[3] W. Ahmad, M. Törmänen, and H. Sjöland, "Photodiodes in deep submicron CMOS process for fully integrated optical receivers," in *Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2013, pp. 135–138.

[4] K. Iiyama, T. Shimotori, R. Gyobu, T. Hishiki, and T. Maruyama, "10 GHz bandwidth of Si avalanche photodiode fabricated by standard 0.18 µm CMOS process," *Optoelectron. Commun. Conf. (OECC), Aust. Conf. Opt. Fibre Technol.*, pp. 243–244, Jul. 2014.

[5] Q. Pan, Y. Wang, Y. Lu, and C. P. Yue, "An 18-Gb/s Fully Integrated Optical Receiver With Adaptive Cascaded Equalizer," *IEEE J. Sel. Top. Quantum Electron.*, vol. 22, no. 6, pp. 361–369, Nov. 2016.

[6] F. Tavernier and M. Steyaert, "High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS," in 1st ed., New York, NY: Springer New York, 2011, ch. 3.

[7] R. Carter, J. Mazurier, L. Pirro, J.-U. Sachse, P. Baars, J. Faul, *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *IEEE Int. Electron Devices Meet.*, Dec. 2016, pp. 2.2.1–2.2.4.

[8] *European Chips Act: Staff Working document*, Brussels, May 2022.

[9] F.-P. Chou, Y.-C. Hsieh, C.-A. Huang, and Y.-M. Hsin, "Excess noise of 850-nm silicon avalanche photodiodes fabricated using CMOS process," in *IEEE Int. Symp. Next-Generation Electron.*, May 2014, pp. 1–3.

[10] S. Radovanovic, "High-speed photodiodes in standard CMOS technology," PhD Thesis, University of Twente, The Netherlands, 2005.

[11] T. Xie, Q. Wang, H. Ge, Y. Lv, Z. Ren, and J. Chen, "Characterization of 22 nm FDSOI nMOSFETs With Different Backplane Doping at Cryogenic Temperature," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 1030–1035, Oct. 2021.

[12] C. Schippel, S. Lehmann, S. Ong, A. Muehlhoff, I. Cortes, W. Chow, *et al.*, "A 22nm FDSOI Technology with integrated 3.3V/5V/6.5V RFLDMOS Devices for IOT SOC applications," in *IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf.*, vol. 1, Oct. 2018, pp. 1–3.

[13] MOSIS, *MOSIS Scalable CMOS (SCMOS)*, Revision 8. Marina del Rey, CA, 2009.

[14] J. G. Su, H. M. Hsu, S. C. Wong, C. Y. Chang, T. Y. Huang, and J. Y. C. Sun, "Improving the RF performance of 0.18 µm CMOS with deep n-well implantation," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 481–483, Oct. 2001.

[15] A. Richter, S. W. Glunz, F. Werner, J. Schmidt, and A. Cuevas, "Improved quantitative description of Auger recombination in crystalline silicon," *Phys. Rev. B*, vol. 86, no. 16, p. 165 202, Oct. 2012.

[16] D. Schroder, R. Thomas, and J. Swartz, "Free carrier absorption in silicon," *IEEE Trans. Electron Devices*, vol. 25, no. 2, pp. 254–261, Feb. 1978.

[17] L. Passari and E. Susi, "Recombination mechanisms and doping density in silicon," *J. Appl. Phys.*, vol. 54, no. 7, pp. 3935–3937, Jul. 1983.

[18] K. Lakshmikumar, A. Kurylak, R. K. Nandwana, B. Das, J. Pampanin, M. Brubaker, *et al.*, "A 7 pA/sqrt(Hz) Asymmetric Differential TIA for 100Gbs PAM-4 links with -14dBm Optical Sensitivity in 16nm CMOS," in *IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 66, Jan. 2023, pp. 206–207.

[19] M. N. Sakib and O. Liboiron-Ladouceur, "A Study of Error Correction Codes for PAM Signals in Data Center Applications," *IEEE Photonics Technol. Lett.*, vol. 25, no. 23, pp. 2274–2277, Dec. 2013.