Simulation Environment with Customized RISC-V Instructions for Logic-in-Memory Architectures

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Abstract—Nowadays, various memory-hungry applications like machine learning algorithms are knocking "the memory wall". Toward this, emerging memories featuring computational capacity are foreseen as a promising solution that performs data process inside the memory itself, so-called computation-in-memory, while eliminating the need for costly data movement. Recent research shows that utilizing the custom extension of RISC-V instruction set architecture to support computation-in-memory operations is effective. To evaluate the applicability of such methods further, this work enhances the standard GNU binary utilities to generate RISC-V executables with Logic-in-Memory (LiM) operations and develop a new gem5 simulation environment, which simulates the entire system (CPU, peripherals, etc.) in a cycle-accurate manner together with a user-defined LiM module integrated into the system. This work provides a modular testbed for the research community to evaluate potential LiM solutions and co-designs between hardware and software.

Index Terms-RISC-V, Logic-in-Memory, Simulation, Gem5

I. INTRODUCTION

The performance gap between memories and computing units, known as "the memory wall" has been a long-lasting issue in computing systems [18]. Along with the rise of application domains such as machine learning and the internet of things, this issue becomes exceedingly pressing in the conventional von Neumann computing paradigm. In addition to the ever-worsening performance gap, the data movement between these components consumes more than 60% of the total system energy [3]. To overcome this issue, several Computation-in-Memory (CiM) techniques have been proposed, and research from different computing layers is actively involved [21], [29]. Specifically, Logic-in-Memory (LiM) is one promising CiM solution [6], [5], where the computation can be performed by additional logic inside the memory array¹.

To utilize such CiM architectures, the CPU must be able to coordinate the corresponding operations and let the data processing perform by the memory itself. A few recent studies have shown that the custom encoding space of RISC-V



Fig. 1. Overview of the evaluation environment developed in this work. Our contributions are within the scope of the dashed block. The outputs of the environment include simulation logs and instruction execution logs.

Instruction Set Architectures (ISA) serves this purpose very well, in which additional instructions can be introduced and mapped to various functionalities provided by CiM architectures. For example, Lin et al. [17] propose specific instructions with the support of Tensor Virtual Machine (TVM) to aid Processing-in-Memory architectures for accelerating binarized neural network [4]. Considering the standard RISC-V core architecture [25], RISC-Vlim provides a general solution to enable the communication between the microprocessor and the LiM array without altering the bus interface [5]. With such customized instructions, the coordination of the computing process can be automated, and more optimizations are potentially allowed.

However, computing systems with the CiM capacities are still rarely available at the market. With commodity memories like DRAM, indeed some prominent examples have been emerging, e.g., Samsung's FIMDRAM [15], UPMEM architecture [9], SK Hynix's AiM [16]. Most researchers so far still rely on simulations to evaluate their approaches, based on detailed models at different layers. Under this context, the gem5 simulator [2] is widely used nowadays and serves several research directions, especially for emerging memories

¹The literature offers a wide range of LiM definitions [21], [22], and we follow the typology used in [22] and [5]. Nevertheless, this work's insight shall generally apply to memory architectures with specific computation capacities.



Fig. 2. LiM memory architecture, adapted from [5]

and HW/SW co-designs [10], [19], [11]. It is a cycle accurate full-system simulator, which provides the functional simulation of the underlying hardware. Many simulation tools are also possible to be integrated as modules or plugins with the gem5 simulator, such as NVMain2.0 [20] for non-volatile memories and RTSim [14] specifically for racetrack memories.

Our Contributions: In this work, we develop a new simulation environment, where the customized RISC-V instructions defined in [5] can be integrated into a C program via the inline assembly functions, and the developed gem5 simulator is able to run the generated executable and report the execution details, such as execution time in cycles and executed instructions logs. Figure 1 shows the overview of this work. In a nutshell, the contributions of this work are:

- Introducing the customized RISC-V instructions, defined by [5], into the standard GNU binary utilities, by which the inline assembly functions in the C program for LiM operations can be compiled (See Section II-C).
- The gem5 simulation setup with an enhanced decoder for the customized RISC-V instructions, which simulates the LiM operations with a user-defined LiM module on a functional level (See Section III).
- Evaluation of the developed simulation environment with real-world algorithms, in comparison to the simulation results derived from RISC-Vlim [5] (See Section IV).

The enhanced toolchains and the developed environment in this work will be publicly available once the paper is accepted.



Fig. 3. The considered system architecture, simulated in the developed gem5 simulation environment. As a proof of concept, we disable the cache hierarchy in this work and focus on the CPU and LiM modules.

II. SYSTEM ARCHITECTURE AND RISC-V INSTRUCTIONS

In this section, we introduce the system architecture and the customized RISC-V instructions considered in this work. We follow the insight of Coluccio et al. [5] to consider a standard memory interface, by which different LiM architectures are compatible, regardless of the underlying memory technologies.

A. System Architecture

Figure 2 shows the considered LiM memory design [5]. Noted that the CPU used in [5] ri5cy access instruction and data from the same memory, so the instruction flow is also considered in the memory design. Each memory cell is considered a LiM cell, while access data, bit-wise operations like **AND**, **OR**, and **XOR** will be operated with the mask data, which is from the register. All the LiM cells are connected with the MAX-MIN Logic, which determines the MAX or MIN value over the cells. In this simulation, we realize the functionality of range logic with its peripherals and LiM cells. MAX-MIN logic is considered as the future work.

Figure 3 illustrates the system architecture we considered in this work. Based on the default design of gem5, the communication over the hardware components as modules in the simulated system is implemented via packets and ports. The CPU has the instruction cache port and the data cache port connected with the memory bus, and the memory bus received data from CPU and control the LiM memory architecture. The corresponding portions of the LiM memory can then be activated via the information contained in the packet, such as opcode and offset of the memory address (introduced below). Any further interface modification, such as the memory interface, can also be easily introduced. Although gem5 has memory subsystems such as cache hierarchy, they are disabled in this work to avoid involving side effects, which are considered out of the scope.

B. Customized RISC-V Instructions for LiM Operations

For the completeness, we recap the customized RISC-V instructions introduced in [5], which support the LiM solution proposed in [27]. Since the LiM memory could also be utilized as a classic memory, two customized instructions are introduced for adjusting the status of the LiM memory cells, namely **STORE_ACTIVE_LOGIC** and **LOAD_MASK**, as shown in Figure 4. The original **STORE** instruction could also be involved in the operations of LiM process. If the memory region is activated for LiM operations, a normal store instruction will be interpreted as a logic store instruction.

There are three fields for **STORE_ACTIVE_LOGIC**: BASE_REG, RANGE_REG and MEM_OP. The BASE_REG field determines the base memory address, and the range size (i.e., RANGE_REG) of cells are active. The MEM_OP field gives the active operation type: NONE, AND, OR, XOR, NAND, NOR and XNOR. For **LOAD_MASK**, data from the BASE_REG field will be masked by the MEM_OP with the input mask in the SOURCE_REG field first. Afterward, the result is stored at the destination register DEST_REG. Note that **LOAD_MASK** must always be placed after the activation of the LiM operation, which is handled by compilation.

Here we give a running example to demonstrate the system behavior with the instruction **STORE_ACTIVE_LOGIC** with **STORE**. Suppose that every LiM memory cell has an initial status, **NONE**, meaning that this cell is inactivated for any LiM operation yet and data is merely loaded into the memory. As shown in Figure 5, **STORE_ACTIVE_LOGIC** executed with *BASE_REG* equal to 0x08, *RANGE_REG* equal to 0x03, and *MEM_OP* is *OR*. The LiM memory switches the cell status to *OR* for 3 cells starting from the address 0x08. The **STORE_ACTIVE_LOGIC** instruction must cooperate with a **STORE** instruction, which is treated as a logic store operation here. Note that the **BASE_REG** field must have the same value and the value of *IMME12* field must be zero. Therefore, the data from the *SOURCE_REG* then are operated with *MEM_OP* and written back to the same memory cell.

C. Enhancement of GNU Binary Utilities

Here we present how we generate the executable binary with the customized instructions via the enhancement of the GNU binary utilities. We consider an agile development flow with the usage of inline assembly functions to enable the LiM operations in a given program.

In a typical end-to-end compilation flow, the source code is first translated into the assembly code and converted into the object code by the assembler. Afterward, the linker binds and links runtime information to generate the executable binary. To serve the objective of this work, the enhancement of the assembler is sufficient without revamping all the steps above.

Figure 6 illustrates the compilation flow we adopted: Given an application source code, the LIM operations are enabled by users through inline assembly functions. To process the additional customized instructions, the new opcodes have to be registered in the assembler. The RISC-V GNU binary utilities provide the repository of RISC-V Opcode to reserve the opcodes for customized instructions in the repository:. Since there is no automatic detection for collisions, a potential pitfall here is that the introduced opcodes might overlap with the existing opcodes. With the auxiliary of the RISC-V opcode, we can introduce new instructions into the GNU binary utilities with unique opcodes.

III. GEM5 SIMULATION ENVIRONMENT

In this section, we present the design of our gem5 simulation environment, where the RISC-V decoder is extended to process additional instructions introduced previously. Figure 7 shows the overview, considering one LiM architecture in the simulated system suggested by [5].

A. RISC-V Decoder for LiM Instructions

To use the LiM memory architecture, at first two new customized instructions, **STORE_ACTIVE_LOGIC** and **LOAD_MASK** are additionally introduced into the RISC-V decoder of gem5. Under 32-bit RISC-V ISA, **STORE_ACTIVE_LOGIC** belongs to I-type, and **LOAD_MASK** is the SB-type [1]. Figure 8 shows the instruction format of RISC-V I type and SB type.

The ISA Parser (so-called decoder) adopts a nested structure to decode instructions, based on the code segments (i.e., the brackets in Figure 8). The format is defined from left to right and match the **QUADRANT**, **OPCODE**, and **FUNC3**. For all the instructions, the memory and the registers exchange data to each other. For **STORE_ACTIVE_LOGIC**, the activation size of memory stored in the *RANGE_REG* is sent to the memory via the packet, i.e., *Mem_ub* is assigned with *Rd_ub*. For the simplicity of presentation, the other detailed handling such as the memory address in **RANGE_REG** and the *MEM_OP* are not introduced here.

B. Design of LiM Module

Along with the convention of gem5, we introduce a module to describe the functionalities of the LiM memory architecture into the environment, as shown in Figure 3, where the CPU communicates with the memory controller through the packets. Based on the information contained in the packets, the memory controller modifies the state of the memory cells accordingly and updates the data stored in the memory.

Figure 7 illustrates the gem5 simulator, integrated with one LiM memory architecture. By the design of gem5, every hardware component, such as CPU, is considered as an object, and the objects communicate with each other via packets and signals. After decoding, all the information is packed into the LiM packet, and the CPU module sends this packet to the memory controller by the response port. Afterward, the memory controller alters the state of the LiM memory. Each cell inside the memory holds the current states of LiM memory as *NONE*, *AND*, *OR*, *XOR*, *NAND*, *NOR*, or *XNOR*. After the simulation, instruction count, simulation time, and detailed instruction log is obtained by the gem5.



Fig. 4. RISC-V customized instructions to use the LiM memory cells, adapted from [5].



Fig. 5. Running example for STORE_ACTIVE_LOGIC



Fig. 6. Overview from a given C program to the target code

IV. EVALUATION AND DISCUSSION

In this section, we present the required runtime for simulating the execution of benchmarks with the introduced customized instructions, in comparison to the RTL simulation environment provided by [5]. Please note that, the simulations conducted in [5] are based on Vsim (as known as ModelSim), where a hardware description language is utilized and waveforms for signals are generated for circuit validation. Once the designed architecture is proven to work well with the customized instructions, the gem5 simulation environment developed in this work can be utilized to efficiently evaluate the effectiveness of customized instructions and LiM architecture. The resulted speedup is thus expected and helpful.

A. Experimental Setup

Table I shows the details of experiment environment. We simulated a system with a LiM memory architecture in Gem5 v22.0.0.2. The customized instructions were introduced by the enhanced GNU Binutils 11.1.0 (see Section II-C). We compare the performance of the simulation environments with the same benchmarks adopted in [5], i.e., The source code with inline assemblies were provided by the repository², and we used the enhanced GNU Binutils to generate the target code in elf with the LiM operations as the input of the gem5 simulations.

Since the Vsim-based evaluation conducted in [5] merely simulates the hardware behavior, only the physical memory space is considered, and thus an actual physical address is given into the tested application, shown as Listing 1. However, our gem5-based simulation environment works with a virtual memory space towards the need of operating systems, where we adopt the *malloc* function to settle the virtual memory space, as shown in Listing 2.

```
int main(int argc, char* argv[]) {
    /* input variables declaration */
    int (*states)[4][4] = 0x30000;
    ...
    return EXIT_SUCCESS;
}
```

Listing 1. Address definition example for vsim

```
int main(int argc, char* argv[]) {
    /* Other variables */
    int i;
    /* input variables declaration */
    int row = 4, col = 4;
    int* states[row];
    for (i = 0; i < row; i++)
        states[i] = (int*)malloc(col * sizeof(int));
    ...
    return EXIT_SUCCESS;
}</pre>
```

Listing 2. Address definition example for Gem5

B. Experimental Results

Table II shows the required time of two simulation environments for running different benchmarks on average. For each simulation environment, we ran 20 times per benchmark. We

²https://github.com/vlsi-nanocomputing/risc-v-lim-architecture



Fig. 7. The developed gem5 simulation environment, integrated with the considered LiM memory architecture



Fig. 8. RISC-V instruction type and corresponding Gem5 decode format



Fig. 9. Gem5 decoder example for STORE_ACTIVE_LOGIC

Experiment environment		
Architecture	x86_64	
CPU(s)	24	
Model name	12th Gen Intel(R) Core(TM) i9-12900K	
CPU max MHz	6700	
CPU min MHz	800	
Main Memory Size	128 GiB	
Operating System	Ubuntu 22.04.1 LTS	

TABLE I Experiment environment

can see that for running software applications, the gem5-based environment is much efficient. For xnor_net.c, due to the limited time, we cannot finish all the experiments.

Overall, as long as the introduced customized instructions have been validated by, for example, the Vsim environment in [5], the gem5-based environment is more suitable for massive testing for capturing the numbers of memory accesses and the performance improvement.

V. RELATED WORK

Several CiM solutions have been proposed [21], [29], especially in recent years due to the emerging non-volatile memories [26], [30], [28]. Using customized RISC-V instructions to support various architectures such as accelerators has also been studied widely [17], [5]. RISC-V is conceived to be expandable so that unused opcodes can be introduced to accommodate custom extensions; some extensions become standard, while others can remain a specific feature of vendors. This characteristic allows RISC-V processors to have ad-hoc instructions while keeping compatibility with the global RISC-V ecosystem. This approach has been, for example, leveraged by the PULP processors [8] [24] [23].

While several instruction set simulators for RISC-V have been developed to speed up the functional verification, most of them can hardly be extended to support system-level use cases. Different full system simulators have been proposed to fill this gap, such as SoCRocket [7] and RISC-V VP [12], just to name a few. As one popular full system simulator, gem5 has been attractive to computing system researchers [2], [11], [13]. This work serves as the first step to support the customized RISC-V instructions in the gem5 fashion for LiM memory architectures, by which more LiM solutions, HW/SW co-designs and software automation can be evaluated.

VI. CONCLUSION

Towards the pressing issue of "the memory wall", various CiM solutions have been proposed in the literature. Recent research shows that utilizing the custom extension of RISC-V instruction set architecture (ISA) to support the coordination of CPU and CiM, especially for LiM architectures, is effective. In this work, we develop a new gem5 simulation environment to

Simulation time			
Benchmark	Gem5	Vsim	
aes128_arkey.c	0.0149s	53s	
bitmap_search.c	0.0148s	57s	
bitwise.c	0.013s	36s	
max_min.c	0.0232s	116s	
xnor_net.c	0.0886s	-	

TABLE II SIMULATION TIME COMPARISON

provide a cycle-accurate simulation to support such research. The results show that the gem5-based simulation can be used for massively testing the impacts of introduced instructions, and its flexibility provides foreseen potentials for testing CiM/LiM solutions. In the future, we plan to maintain this tool set and include, for example, more LiM architectures and customized instructions like reduction algorithms.

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