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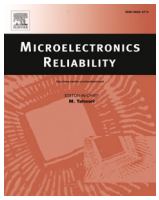

Modelling SiC MOSFET module threshold voltage (V_{TH}) and impact of parallel device ΔV_{TH} on short circuit robustness

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ABSTRACT

In SiC modules, where several power MOSFETs are connected in parallel for high current conduction capability, the issue of threshold voltage (V_{TH}) variation between individual devices can become problematic. In instances where the standard deviation of device V_{TH} is minimized by appropriate V_{TH} pre-screening, non-uniform V_{TH} shift under bias-temperature-instability can lead to increased V_{TH} dispersion and potentially poor current sharing. Although non-destructive for normal operation, V_{TH} dispersion in surge events like short circuits can cause premature module failure. In this paper, experimental investigations backed by theoretical models have been developed to explain the relationship between device V_{TH} dispersion and module V_{TH} shift. This is done for Si and SiC MOSFETs. Five Si/SiC MOSFETs are paralleled in a custom printed-circuit-board allowing individual V_{TH} and module V_{TH} measurements. It is shown that the module V_{TH} is typically between the smallest V_{TH} and the mean V_{TH}, depending on the V_{TH} standard deviation. Using empirical models for MOSFETs in weak inversion derived from the measured subthreshold gate transfer characteristics, the model can estimate module V_{TH} from a dispersion of individual MOSFET V_{TH}. It can also predict the impact of non-uniform V_{TH} shift between constituent devices on the overall module V_{TH}. Finally, the impact of V_{TH} mismatch on current sharing during short circuits in parallel connected SiC MOSFETs is presented. The results show that V_{TH} mismatch in parallel connected SiC MOSFETs reduces the short circuit withstand time from 5 μs to 4.5 μs compared to V_{TH} matched SiC MOSFETs.

1. Introduction

Threshold voltage drift from charge trapping and de-trapping is a well-known and studied reliability issue for SiC power MOSFETs [1–3]. Several investigations have been performed on the measuring threshold voltage shifts (ΔV_{TH}) under positive and negative gate voltage stress [4,5]. These have been done at different gate-source voltages (V_{GS}) frequencies, durations, and device junction temperatures. These investigations have typically involved single discrete devices. However, in high current applications where devices are connected in parallel for current sharing, measurement, and characterization of the module ΔV_{TH} is not straightforward. This is because the individual devices in the module may undergo different magnitudes of ΔV_{TH}. In module design, it is highly recommended to parallel devices within the same V_{TH} range to minimize the V_{TH} dispersion between the devices in the module. While in most cases, different SiC power MOSFETs of the same technology from the same manufacturer should undergo identical ΔV_{TH} under the same test conditions, the probabilistic nature of charge trapping and de-trapping means there may be some variation in ΔV_{TH} even between devices in the same V_{TH} bin [1]. This can have important reliability implications over the operation life of the module. For example, it has been shown that ΔV_{TH} between parallel devices reduces the short circuit robustness of the power module [6,7].

In this paper, the relationship between the module V_{TH} and the V_{TH} dispersion of the constituting devices is investigated. A model is developed that allows the prediction of module V_{TH} given the spread of V_{TH} of the constituting devices. The model is based on the application of weak inversion MOSFET equations on experimentally measured devices and can be used to predict the impact of ΔV_{TH} between parallel connected MOSFETs on the module V_{TH}. A custom designed PCB that allows the parallel connection of discrete devices was developed. This PCB allows the measurement of individual device V_{TH} and the module V_{TH}. Section 2 introduces the experimental set-up and measurements. Section 3 describes the development of the model. Section 4 discusses model

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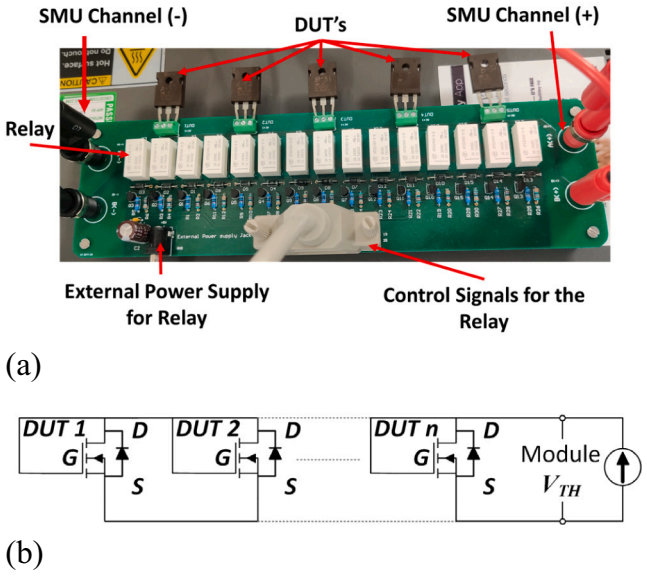


Fig. 1. (a). Custom-designed PCB for evaluation of V_{TH} in parallel connected MOSFETs.
(b). Equivalent of PCB in V_{TH} measurement mode.

Table 1
Individual and Module V_{TH} for Si and SiC MOSFETs.

	Si M1	Si M2	Si M3	SiC M1	SiC M2	SiC M3
V_{TH1}	4.191	2.966	4.201	4.086	3.767	3.912
V_{TH2}	4.243	3.243	3.259	4.106	4.131	4.405
V_{TH3}	4.064	3.100	4.102	4.021	3.800	3.889
V_{TH4}	4.125	3.000	4.141	4.084	3.681	3.910
V_{TH5}	4.185	2.920	4.192	4.036	4.151	4.359
Module	**4.158**	**2.965**	**3.438**	**4.107**	**3.893**	**4.035**
Mean	4.162	3.046	3.979	4.067	3.906	4.095
SD (%)	1.655	4.227	10.172	0.885	5.608	6.411

validation, Section 5 presents the impact of threshold voltage variation on short circuit measurements while Section 6 concludes the paper.

2. Experimental measurements

There are different methods of measuring the threshold voltage of a MOSFET [8]. However, in industrial settings, V_{TH} is typically measured by shorting the gate of the MOSFET to the drain, forcing a defined current (usually 1 mA) and measuring the drain-source voltage, which should be equal to the gate-source voltage [9]. The advantage of this technique is that it yields a point measurement, instead of a gate-sweep. When there are parallel connected MOSFETs with different V_{TH}, and this technique is used, the forced current is shared between the parallel devices. If the devices have identical V_{TH}, then the forced current is equally shared and if not, there is a current divider based on the V_{TH} difference.

Fig. 1(a) shows a picture of the custom designed PCB for the evaluation of the V_{TH} of parallel connected devices. Fig. 1(b) shows the equivalent circuit diagram of the PCB in V_{TH} measurement mode where the gate and drain of the devices are shorted and a forcing current is passed through. A source-measurement-unit (SMU from Keithley Model 2602B) is used to measure the module V_{TH}.

The circuit in Fig. 1 was used to measure the module V_{TH} of 5 parallel connected silicon and SiC MOSFETs. The V_{TH} of the individual devices and that of the module are measured. The measurement results are shown below in Table 1 for 3 silicon and 3 SiC modules with different V_{TH} dispersion (standard deviation) between constituent devices. The

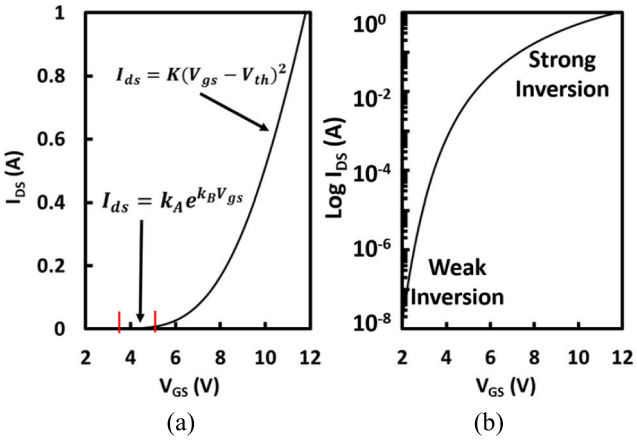


Fig. 2. Gate transfer characteristics of 650 V SiC MOSFET with (a) linear and (b) logarithmic axes $V_{DS} = 1$ V.

V_{TH} standard deviation in the module is varied between 1 and 10 % (of the average V_{TH}) in the silicon devices and 0.8 and 6.4 % in the SiC devices. In silicon module M1, the SD is low. In Si module M2, one of the 5 devices has a higher V_{TH} while in silicon module M3, one of the devices has a low V_{TH}. The results in Table 1 show that the module V_{TH} is between the minimum device V_{TH} and the average V_{TH} for all cases. In cases where the standard deviation is large (M3), the module V_{TH} is closer to the minimum V_{TH}, however, in modules where the V_{TH} standard deviation is low (M1), the module V_{TH} is closer to the average V_{TH}. In the next section, a model that uses experimental transfer characteristics of individual devices to predict the module V_{TH} will be introduced.

3. Model development

The model developed for correlating device V_{TH} dispersion (between individual devices) to module V_{TH} uses the equation for the MOSFET in weak inversion. As the V_{GS} is swept between off-state and on-state, the MOSFET channel goes from accumulation (holes in the channel) to depletion (channel is free of carriers), to weak inversion (low electron concentration) and then to strong inversion (high electron concentration). The threshold voltage is defined as the V_{GS} bias point at which the channel goes from weak inversion into strong inversion i.e., the electron concentration in the channel is equal to the background p-doping concentration used to set the threshold voltage.

$$V_{TH} = V_{FB} + \varphi_S + \frac{\sqrt{qN_A\varepsilon_{Si}2\varphi_S}}{C_{OX}} \tag{1}$$

where V_{FB} is the flat-band voltage, φ_S is the semiconductor surface potential, N_A is the p-body doping, ε_{Si} is the dielectric constant of the semiconductor and C_{OX} is the oxide capacitance density of the gate dielectric. The V_{TH} also corresponds to the V_{GS} bias at which the surface potential is equal to the bulk potential as shown in Eq. (2).

$$\varphi_S = 2\frac{kT}{q}ln\left(\frac{N_A}{n_i}\right) \tag{2}$$

Before strong inversion in the channel, the relationship between V_{GS} and the drain-source current I_{DS} is exponential. This equation is given by

$$I_{DS} = \beta\phi_{th}^2(n-1)e^{\frac{V_{GS}}{n\phi_{th}}} \tag{3}$$

where ϕ_{th} is the thermal voltage, n is the body factor and β is the gain constant. Eq. (3) can be simplified into Eqs. (4) and (5) corresponding for two parallel MOSFETs. The exponential pre-factor and constants k_{A_1}, k_{A_2}, k_{B_1} and k_{B_2} are determined by curve fitting from experimental measurements.

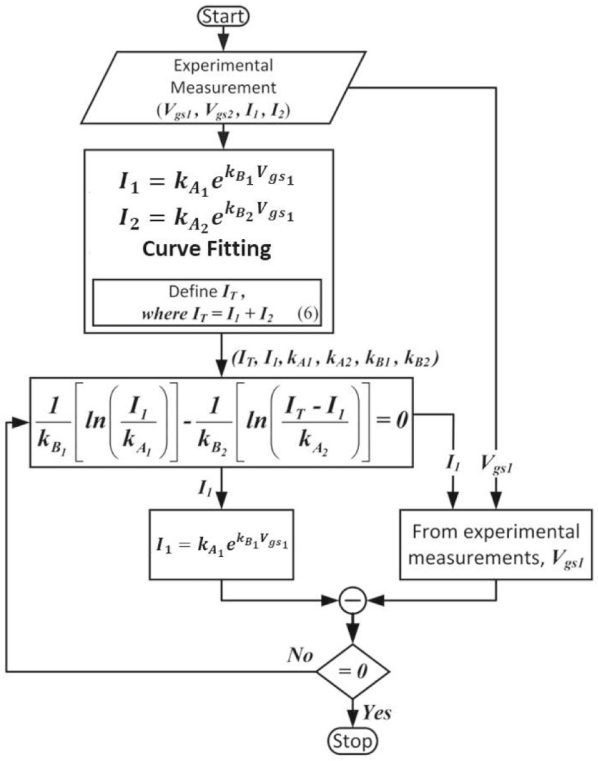


Fig. 3. Process for module V_{TH} determination from individual MOSFET gate transfer characteristics.

$$I_1 = k_{A_1} e^{k_{B_1} V_{gs_1}} \tag{4}$$

$$I_2 = k_{A_2} e^{k_{B_2} V_{gs_2}} \tag{5}$$

Fig. 2 shows the measured gate transfer characteristics of a typical 650 V SiC MOSFET with the drain current plotted on linear and logarithmic axes. The drain-source voltage was 1 V. Fig. 2(b) clearly identifies the transition point between weak and strong inversion on the logarithmic axes where the drain current characteristics move from linear to saturation.

As the V_{GS} is swept for 2 parallel connected MOSFETs, the measured current is the sum of the individual MOSFET currents as shown in Eq. (6) below.

$$I_T = I_1 + I_2 \tag{6}$$

As the V_{GS} is equal for both devices, rearranging Eqs. (4) and (5) yields Eq. (7).

$$\frac{1}{k_{B_1}}\left[ln\left(\frac{I_1}{k_{A_1}}\right)\right] - \frac{1}{k_{B_2}}\left[ln\left(\frac{I_T - I_1}{k_{A_2}}\right)\right] = 0 \tag{7}$$

Eqs. (6) and (7) can be used to predict module V_{TH} given a range of device V_{TH} under parallel connection.

Fig. 3 shows the process of module V_{TH} determination (from 2 parallel devices) using the equations presented. First, an SMU is used to measure the subthreshold gate transfer characteristics of the devices. Then using curve fitting, the parameters k_{A_1} and k_{B_1} are extracted from the measurements. These parameters are used to determine I_1 such that equation7 holds true under the constraint of Eq. (6). It is an iterative process implemented in MATLAB. Once the I_{DS} point in the subthreshold gate transfer characteristics are found (at which both Eqs. (6) and (7) are satisfied), the corresponding gate voltage is calculated (using Eq. (4)) and then compared with the measured V_{GS} corresponding to the I_{DS} calculated from Eq. (7). The calculated and measured V_{GS} values should be equal otherwise the process is repeated. The V_{GS} obtained from this process is the combined V_{TH} of the parallel devices.

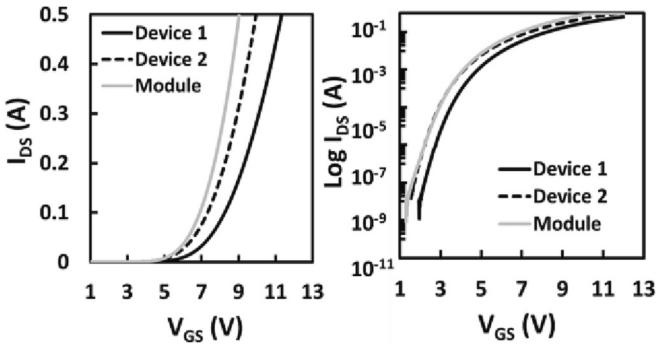


Fig. 4. Gate transfer characteristics of individual SiC MOSFETs and in parallel as a module.

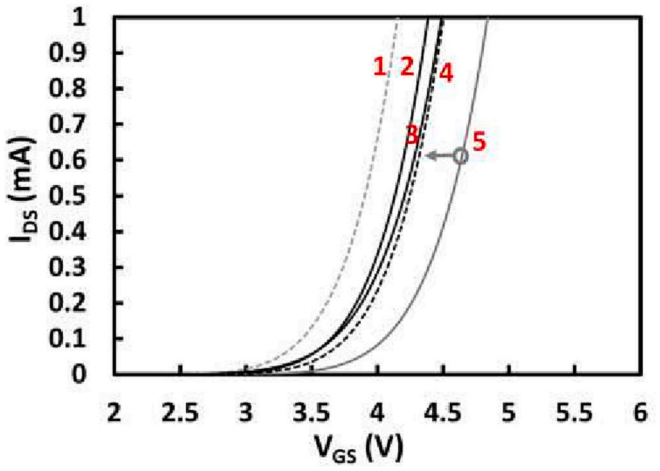


Fig. 5. Gate transfer characteristics of 5 SiC MOSFETs.

4. Model validation

In this section of the paper, experimental threshold voltage measurements have been performed on parallel connected 1.2 kV SiC MOSFETs from ST with datasheet reference SCT10N120AG. V_{TH} was measured using a 2-channel SMU. One channel of the SMU was used for defining the drain source voltage (1 V) and the other channel was used for sweeping gate source voltage (0 V to 12 V). Fig. 4 shows the measured gate transfer characteristics for both devices measured singularly as well as the combined characteristics. The individual V_{TH} of the device 1 and device 2 are 4.33 V and 3.68 V respectively at 0.25 mA drain-source current. After implementing curve-fitting, the parameters obtained were,

$$k_{A_1} = 3.298e^{-9}, \quad k_{A_2} = 9.905e^{-7}$$
$$k_{B_1} = 4.272 \quad , \quad k_{B_2} = 3.367$$

Using the algorithm proposed in Fig. 3, a combined V_{TH} of 3.8705 V is predicted, assuming a total current of 0.5 mA drain to source for two devices in parallel. Measurements of the parallel connected devices show a combined V_{TH} of 3.8803 V at 0.5 mA drain-source current in agreement with the prediction of the model shown in Fig. 3.

One main application of the model is its ability to predict module V_{TH} shift in a condition when one of the constituting devices is undergoing V_{TH} shift from negative or positive gate voltage stress. Ideally, all devices should undergo identical shift under the same stress. However, the probabilistic nature of charge trapping (related to oxide interface and fixed oxide defect density) means it is possible for there to be V_{TH}

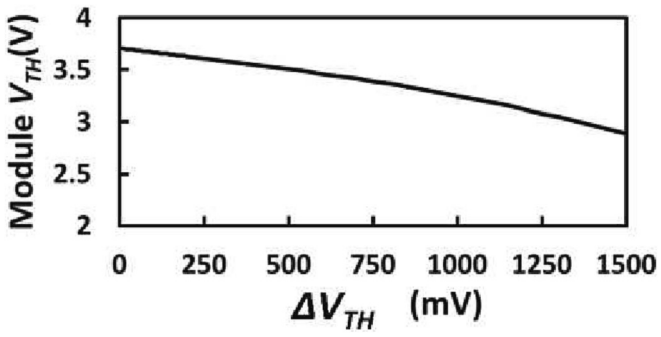
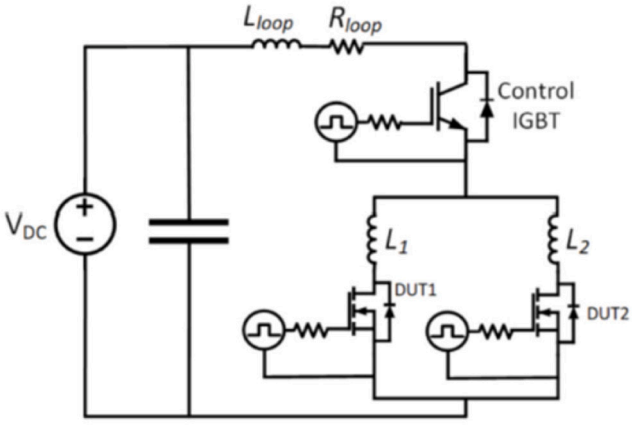
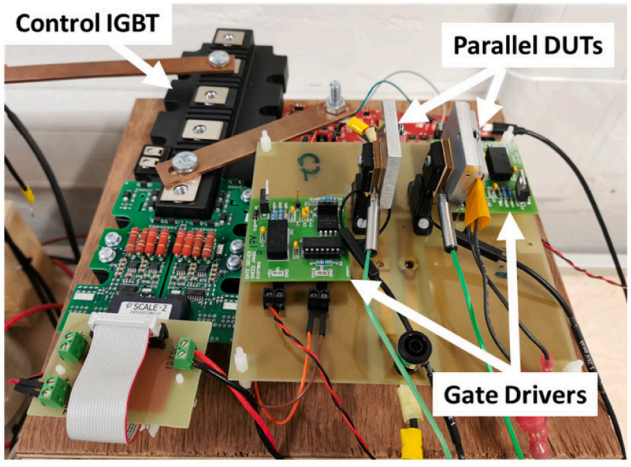


Fig. 6. Module Vth as a function of ΔV_{TH} of device 5.



(a)

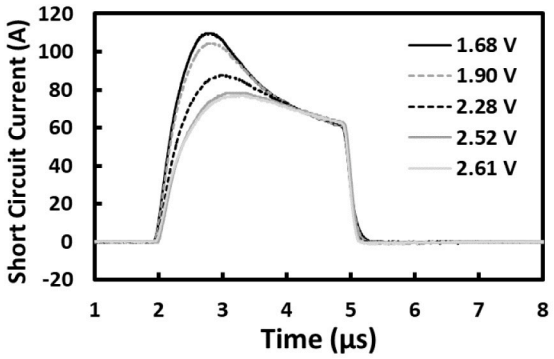


(b)

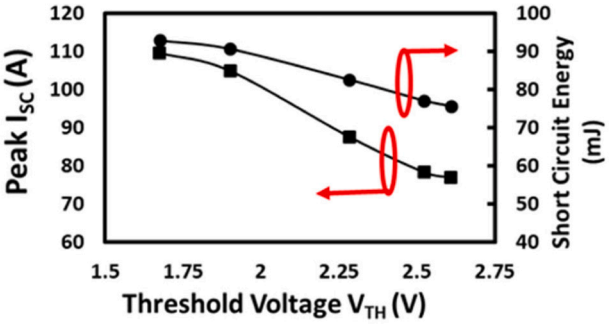
Fig. 7. (a). Circuit Diagram of the short circuit test system.
(b). Short circuit PCB for testing of parallel SiC MOSFETs.

variation between parallel devices as a result of differences in the rate of charge trapping under V_{GS} stress [1,2].

Fig. 5 shows the measured subthreshold gate transfer characteristics of five different 1.2 kV SiC MOSFETs from the ST. To emulate negative V_{TH} shift from negative gate bias, the transfer curve of device 5 is moved leftwards with respect to that of the others. The algorithm in Fig. 3 is used to compute the impact of this on module V_{TH} shift. Although the algorithm in Fig. 3 is shown for 2 parallel devices, it can be extended to V_{TH} prediction for 5 parallel devices. This is done iteratively by combining the subthreshold characteristics of 2 devices into a single device and then repeating until all devices are combined. Hence, if there



(a)



(b)

Fig. 8. (a). Measured short circuit current for SiC MOSFETs with different threshold voltages V_{DS} = 400 V.
(b). Measured short circuit current for SiC MOSFETs with different threshold voltages V_{DS} = 400 V.

are n parallel devices, the algorithm is run n-1 times until a single subthreshold characteristic is derived. The results of this process are shown in Fig. 6, where the module V_{TH} is plotted as a function of the V_{TH} shift of device 5. Fig. 6 shows that the negative shift of the V_{TH} of a single device (ΔV_{TH}) in parallel connection with 4 other devices results in an overall module $V_{TH\text{-}M}$ shift according to Eq. (8) below

$$V_{TH-M} = -0.0008 \bullet \Delta V_{TH} + 3.95 \quad (8)$$

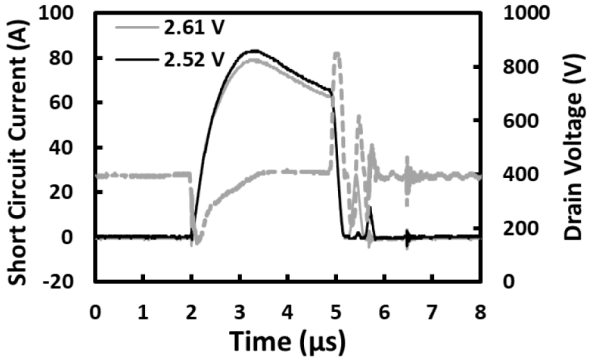
Note from Eq. (8), that the module V_{TH} ($V_{TH\text{-}M}$) is 3.95 V, when there is no V_{TH} shifting from device and the module $V_{TH\text{-}M}$ reduces with the V_{TH} of device 5.

5. Threshold voltage mismatch and short circuit performance

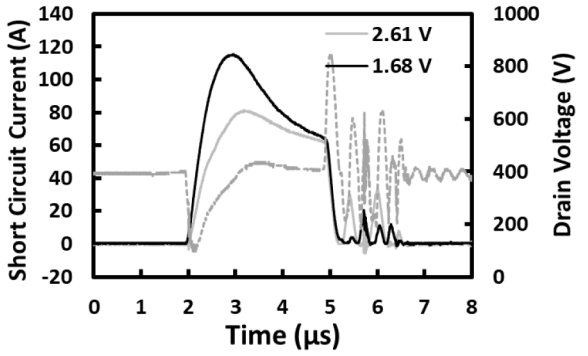
The short circuit performance of a power device is an important robustness metric [10,11]. In this section, a thorough analysis of the impact of V_{TH} on the SC performance of single and parallel devices is performed. For parallel connected devices, the impact of V_{TH} variation on SC current sharing and withstand time is investigated. Fig. 7(a) shows the circuit diagram of the short circuit test system [12]. The measurements were performed with a DC link voltage of 400 V. Fig. 7(b) shows the picture of the short circuit PCB with the parallel SiC MOSFETs. The capacitor is pre-charged and used to discharge its energy into the DUTs. The control IGBT is a 1.2 kV/1000 A Silicon IGBT from Infineon with datasheet reference FF1000R17IE4. As the IGBT module has a much higher output capacitance compared to the SiC MOSFET DUTs, all of the DC link voltage falls across the DUTs [12,13].

5.1. Impact of V_{TH} on peak SC currents

In this section, short circuit measurements have been performed on SiC MOSFETs with different threshold voltages so as to investigate the



(a)



(b)

Fig. 9. (a). Measured short circuits for parallel connected SiC MOSFETs with V_{TH} difference of 0.09 V.
(b). Measured short circuits for parallel connected SiC MOSFETs with V_{TH} difference of 0.93 V.

impact of threshold voltage on the peak short circuit current.

Fig. 8(a) shows short circuit measurements performed on 5 different 650 V/120 mΩ SiC MOSFETs with different threshold voltages. The measurement was performed at ambient temperature 25 °C. The measurements in Fig. 8(a) show that the peak short circuit current is highly sensitive to the threshold voltage with the peak current reducing from 109.6 A with V_{TH} = 1.68 V to 76.9 A with the V_{TH} = 2.61 V. Fig. 8(b) shows the measured peak short circuit current and short circuit energy (in mJ) as a function of device V_{TH}. The short circuit energy is calculated by integrating the short circuit power over the duration of the short circuit. In this case the short-circuit duration is 3 µs. The calculations show that the short circuit energy increases from 75.59 mJ to 93 mJ as the V_{TH} reduces from 2.61 V to 1.68 V. This increase in SC energy is due to the increase in the peak short circuit current.

The short circuit current in a MOSFET is comprised of 2 phases. The first phase determines the peak of the short circuit current and is highly dependent on the device V_{TH} and parasitic inductance in the current path. The 2nd phase is determined by the short circuit resistance of the MOSFET and its temperature coefficient. As can be seen in Fig. 8(a), after 2 µs into the short circuit, all the currents converge to the same value regardless of the MOSFET V_{TH} and peak SC current. Similar results are seen and explained in [12].

Since the short circuit currents of all devices, regardless of V_{TH}, converge to the same value (about 60 A) after 2 µs, it can therefore be assumed that the short circuit resistance and its temperature coefficient are independent of V_{TH}.

5.2. Impact of V_{TH} mismatch on SC performance of parallel SiC MOSFETs

In this subsection, the impact of V_{TH} variation on short circuit current sharing is investigated. Short circuit measurements were performed on parallel connected SiC MOSFETs with 4 different magnitudes of threshold voltage difference. Fig. 9(a) shows the measurements on the parallel DUTs for the lowest V_{TH} difference while Fig. 9(b) shows the measurements for the parallel DUTs with the highest V_{TH} difference. The results in Fig. 9 shows that the difference in the peak currents is proportional to the V_{TH} difference between the parallel DUTs. Fig. 10 shows the peak SC current difference (ΔI_{peak}) and short circuit energy difference (ΔE_{SC}) as a function of the V_{TH} difference between the DUTs for 4 different measurements. The equations relating ΔI_{peak} and ΔE_{SC} to ΔV_{TH} are given below.

$$\Delta I_{peak} = 38.38 \bullet \Delta V_{TH}$$

$$\Delta E_{SC} = 23.17 \bullet \Delta V_{TH}$$

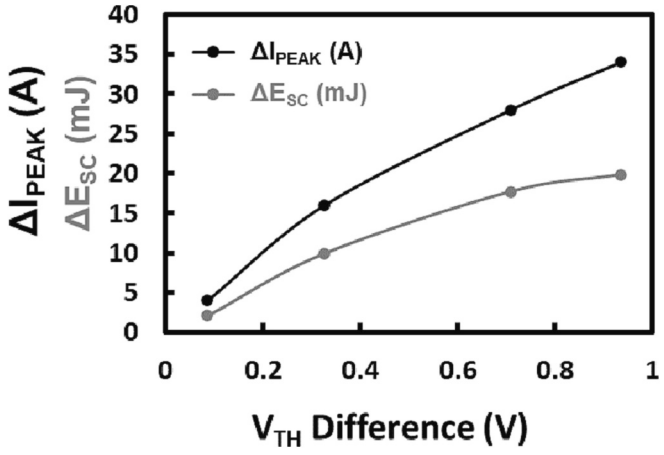


Fig. 10. Peak short circuit current difference as a function of threshold voltage difference between the parallel DUTs.

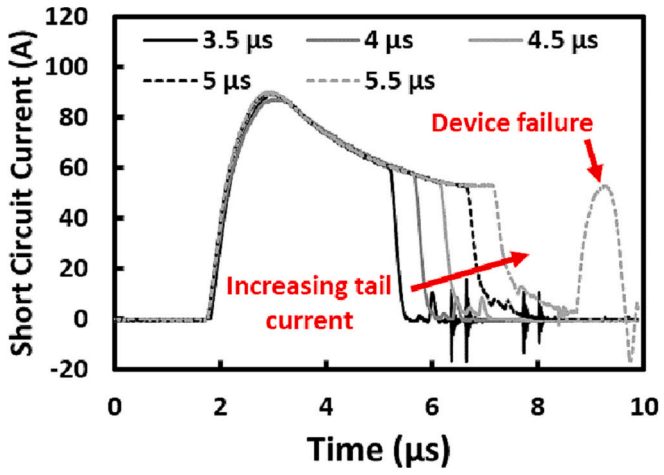


Fig. 11. Short circuit currents for different durations.

5.3. Impact of V_{TH} mismatch on short-circuit withstand time

This subsection investigates the impact of ΔV_{TH} on the short circuit withstand time (SCWT) of the parallel connected MOSFETs with different V_{TH} mismatches. This has been done at 400 V. The SCWT is determined by increasing the short circuit duration in steps of 0.5 µs until the device fails, as done in [13]. In the first case, we investigate the performance of two parallel devices of similar V_{TH}. DUT 1 and DUT 2 with V_{TH} = 2.51 V. Fig. 11 shows the measured short circuit current for V_{TH} matched parallel connected SiC MOSFETs for different short circuit

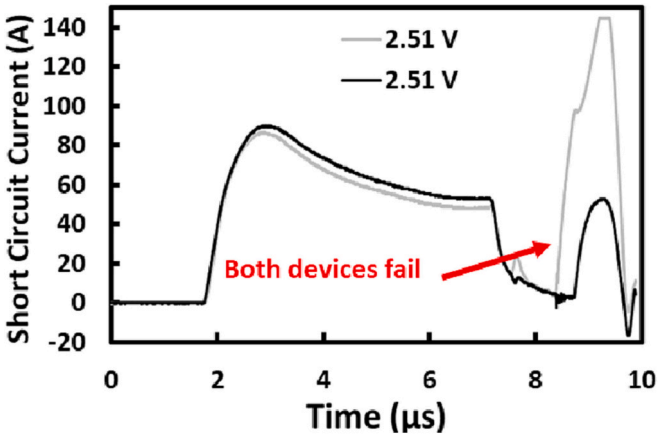


Fig. 12. Short circuit currents for parallel connected SiC MOSFET with V_{TH} matching. SCWT is 5.5 µs.

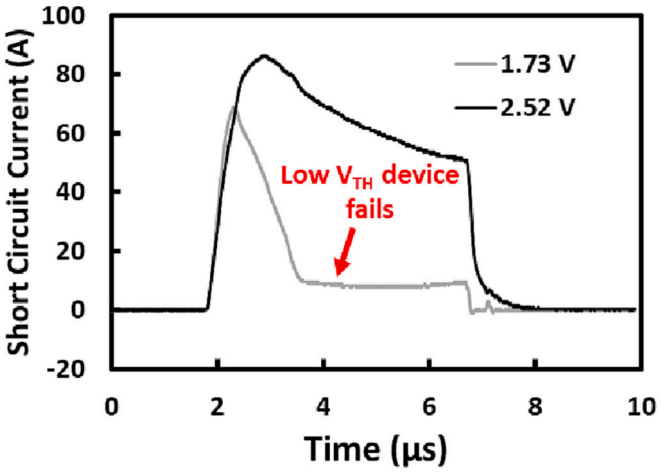


Fig. 13. Short circuit currents for parallel connected SiC MOSFET with V_{TH} mismatching of 35.63 %.

durations. As the short circuit duration is increased, as shown in Fig. 11, there is increased tail current resulting from rising junction temperatures. The measured SCWT for the parallel connected devices is 5 µs, which is comparable to measurements made on similar rated devices in other investigations [14–17]. Two origins have been attributed for tail current (a) increased hole injection from the p-body into the drift region [10]. (b) Channel conduction due to reduced V_{TH} as a result of high lattice temperature [18].

Fig. 12 shows the failure measurement of the parallel connected SiC MOSFETs with very similar V_{TH} (less than 0.1 % difference) failing after 5.5 µs of short circuits meaning that the SCWT is 5 µs, as this was the last pass measurement. Fig. 12 shows that both devices fail simultaneously in a clear case of delayed failure [19], as the devices fail during the tail current phase when the gate is turned off. This results in a hard failure [20]. Subsequent failure analysis showed that both devices exhibited shorted source/drain and gate/source terminals.

Fig. 13 shows similar SCWT measurements for V_{TH} mismatched MOSFETs with a V_{TH} difference of 35.63 % with respect to the higher V_{TH} device. (DUT 3 with $V_{TH} = 1.73$ V and DUT 4 with $V_{TH} = 2.52$ V.) The SC duration in Fig. 13 is 5 µs, hence the SCWT is 4.5 µs.

It should be noted, that for the SCWT measurements for the V_{TH} mismatched SiC MOSFETs in Fig. 13, the MOSFET with the lower V_{TH} (DUT 3) fails while that with the higher V_{TH} (DUT 4) remains fully operational. Subsequent failure analysis showed that the failed device is still capable of blocking a drain source voltage thereby indicating a case

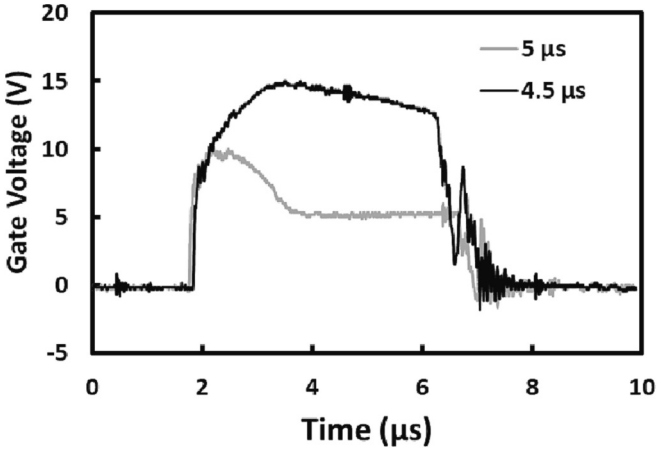


Fig. 14. Gate voltage transients of the failed device for the last pass and failure.

of soft failure [11,20]. The device was unable to turn-on as the gate-source was shorted thereby indicating a breakage in the gate oxide from thermal induced rupture. Fig. 14 shows the gate voltage of the DUT 3 during the last pass test (4.5 µs) and the failure measurement (5 µs). The last pass shows a reduction of the effective gate voltage caused by the increasing gate leakage current during the SC [21].

6. Conclusion

SiC modules comprise of parallel connected SiC MOSFETs that may have some variation in their threshold voltages. In this paper, a program has been developed that is capable of estimating module V_{TH} as a function of the V_{TH} of the constituting devices. It has been shown that the module V_{TH} lies between the smallest V_{TH} in the parallel connection and the mean V_{TH}. When the V_{TH} standard deviation between the constituent devices is low, the V_{TH} is closer to the mean V_{TH} and when the standard deviation is high, it lies closer to the minimum V_{TH}. The model is based on parameter extraction from curve fitting of the subthreshold transfer characteristics where I_{DS} and V_{GS} have an exponential relationship. The model has been validated using parallel connected devices. The model has also been used to demonstrate the impact of differential negative V_{TH} shift between parallel connected devices on the overall module V_{TH}. The impact of V_{TH} mismatch in parallel connected SiC MOSFET on the peak short circuit current and SCWT has been assessed experimentally. The results show that SCWT is reduced from 5 µs in V_{TH} matched devices to 4.5 µs in V_{TH} mismatched devices (with $\Delta V_{TH} =$ 35.63 %).

CRediT authorship contribution statement

A. Deb: Data curation, Formal analysis, Software. **J. Ortiz Gonzalez:** Investigation, Methodology. **S. Jahdi:** Conceptualization. **M. Taha:** Project administration. **P.A. Mawby:** Funding acquisition. **O. Alatise:** Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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