A Rad-hard On-chip CMOS Charge Detector with High Dynamic Range

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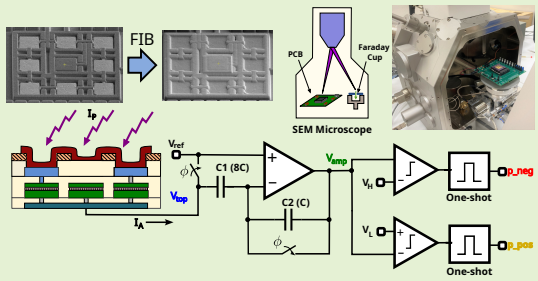
***Abstract*— This article introduces a CMOS charge detector tailored for measuring ionizing radiation in a wide range of fluences. It represents an entirely on-chip solution based on capacitive sensing. It was fabricated using a standard 0.18 μm CMOS process and employs Metal-insulator-Metal (MiM) capacitor arrays to attain high matching, low leakage, and minimal process variations. The sensing area was rad-hardened with a post-CMOS layer of metal deposited with a Focus Ion Beam (FIB) that removes the use of external metallic plates. Experimental testing under the electron beam of a scanning electron microscope (SEM) demonstrated radiation hardness at energies up to 10 keV, with a very high dynamic range of up to 138 dB (externally adjustable), and with a sensitivity of 1.43 μV/e⁻. By harnessing the detection of relative charge variations instead of relying on absolute values, this approach proves highly suitable for particle event detection and facilitates future integrations compatible with the Address Event Representation (AER) communication protocol.**



***Index Terms*— Charge sensing, Rad-hard, Semiconductor Detectors, AER, Dynamic Range, Electron Microscopy**

I. Introduction

IONIZING radiation detection is at the core of instrumentation used in numerous scientific disciplines (e.g., high energy physics, materials science, chemistry, and biology) [1], in medical diagnostic devices [2], or industrial inspection tools [3]. The design of a detector for radiation depends on the incident kinetic energy, fluence, and the type of particles to be sensed, such as photons, neutrons, electrons, ionized molecules, etc. [4], [5].

Indirect sensing is frequently used when high dynamic range, radiation hardness, and sensitivity are needed, like in photomultipliers or PMTs with a scintillator for converting energetic particles into low-energy photons. Direct sensing, on the other hand, is based on absorbing the radiation in photodiodes or by direct charge (current) measurement with a conducting electrode acting as input to the detection electronics, also known as Faraday detection [6]. High-aspect-ratio (depth/width) cup geometries or Faraday cages are prevalent and serve to capture ions while minimizing scattering losses efficiently [7]. In imaging applications, the detectors are formed by pixelated arrays, sometimes called focal-plane arrays, that must be protected against radiation damage. In X-ray radiography, imagers are often made of the combination of a pixelated scintillator that is optically coupled to a photodiode array using CMOS/CCD technology [8].

There is great interest in developing direct image sensors that are rad-hard without using scintillators. The reason is that they can produce high-quality images from ionizing radiation with higher sensitivity and speed compared to indirect sensing approaches. Many devices are frequently built using CMOS rad-hardened arrays of photodiodes [1]. An area of great interest is the case of image sensors for electron microscopes [3], [9], [10]. In electron microscopes, a sample material is irradiated with a beam of primary electrons using kinetic energies between 1 keV and 300 keV [11], [12]. The electrons, after interacting with the material being investigated, are focused on a pixelated array to form an image of the sample. In electron microscopy, low fluences are commonly used to minimize sample damage when imaging biological materials, while higher fluences are preferred for imaging inorganic materials. In the case of performing electron diffraction techniques, the images have extremely high dynamic range and sometimes must be acquired at very high speed [13]. Therefore, direct imagers for electron microscopy would benefit from high dynamic range, high sensitivity, linearity, and speed.

The two main approaches for making image sensors rad-hard are back-thinning and flip-chip fabrication [14]. The most paradigmatic case of the latter is the *Medipix* family of image sensors built with hybrid technology, which are prominent in applications like electron microscopy, X-ray imaging, or environmental dosimetry [15]. Flip-chip fabrication involves stacking a pixelated semiconducting layer that makes electrical contact with the readout circuitry placed on a die beneath. The thickness of the semiconductor layer must be optimized for the

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type and energy of the radiation in the final application. The fill factor is close to 100 % with this approach. Unfortunately, this form of vertical integration remains expensive as it necessitates die post-processing at various stages, leading to increased fabrication time. Additionally, the minimum pixel size is restricted to approximately 55 µm × 55 µm. Although such sensors can exhibit sensitivity to single particles in certain applications, they suffer from non-linearity issues and have a limited dynamic range.

Regarding the sensor latency of imagers, classic synchronous readout logic is inefficient for operating at high speed because all the pixel's data have to be read out sequentially, even for the pixels that do not detect charge variations. Thus, more advanced readout circuitry has been explored [16]. Still, those implementations use digital counters to encode digital values representing the total dose of accumulated charge. Thus, the amount of time that charge can be gauged is limited by the counters' number of bits. Moreover, counters penalize the integration area and, therefore, the pixel pitch.

The Address Event Protocol (AER) is a communication scheme widely adopted to read out pixel arrays with asynchronous operation [17], [18]. It can convey the data of pixel arrays off-chip at high speed without penalizing the pixel fill factor a lot because the logic required to be incorporated in each pixel to communicate with the AER protocol is simple. To the best of our knowledge, direct charge sensing asynchronous pixels compatible with the AER protocol have not been explored yet.

In this work, we investigate a CMOS asynchronous pixel conceived to directly sense ionizing radiation (fluence and sign). It could be integrated, with more development, as the unit pixel of a focal-plane array, compatible with the AER communication protocol and operational within a range of energies of interest for electron microscopy. The prototype was tested using a Scanning Electron Microscopy (SEM) microscope, confirming the proper operation of the circuit with a high dynamic range and low latency.

II. Proposed Sensor

A. Operation principle

The proposed circuit for charge detection is shown in Fig. 1(a). The input is a floating metal layer electrically connected to the electrode of the coupling capacitor C_1. This layer is metallic and has two purposes, first, being the absorbing layer of the radiation, and secondly, acting as a shield of the readout circuitry. When the floating electrode is irradiated with radiation (for example, with a beam of electrons), a net electric charge accumulates at C_1 that is amplified (see Section II-C). The net charge is a balance between the charged particles that are absorbed and those that are re-emitted by the layer. [11].

The amplifier, in conjunction with the negative feedback capacitor C_2 and C_1, forms an inverting stage with an AC gain of approximately -C_1/C_2 for voltages [6], [19]. Alternatively, the configuration can be viewed as a Charge Sensitive Amplifier (CSA) with its transfer equation given by:

$$\Delta V_{amp} = -\frac{\Delta Q_A}{C_2} \tag{1}$$

where ΔQ_A is the net-absorbed charge on the top plate of C_1. To achieve a precise gain in the differencing circuit, capacitors C_1 and C_2 can be arranged in a common-centroid layout to match their electrical characteristics [20]. This is achieved by selecting C_1 as mC and C_2 as nC, where m and n are integers and C is a designated unit capacitance. According to Eq. 1, by minimizing the capacitance C_2, charge to voltage conversion is maximized. Nevertheless, this can result in a reduced pixel pitch and impact sensitivity to fluence. To maintain the appropriate pixel pitch while still achieving the desired Q/C transfer, utilizing values of $m > n$ is advisable.

Fig. 1(b) depicts the operation of the circuit shown in Fig. 1(a). The circuit starts by asserting the $reset$ signal that activates ϕ, and the electrode voltage V_{top} and the amplifier output voltage V_{amp} get properly initialized to a voltage reference V_{REF}. After that, the electrode is charged (or discharged) based on the total charge deposited by the incident radiation in C_1, which causes V_{top} to increase (or decrease) accordingly. The voltage V_{amp} is proportional to the temporal variation of charge on the electrode, with a constant of proportionality $-1/C_2$.

Using threshold voltages V_H and V_L, two comparators detect temporal differences and polarity of the CSA's output voltage V_{amp}. The detection limits are defined by the relationship $V_H > V_{REF} > V_L$, with V_{REF} being a DC bias voltage. By adjusting these voltages, the measurement can be more or less sensitive to a particular particle fluence. Once an amount of charge Q_A is deposited after a time T_{Q_A}, the comparators are triggered, generating a pulse p_{neg} or p_{pos} at the output of the one-shots circuits. Subsequently, the circuit is reset by the output ϕ of the NOR gate, and both the electrode and the amplifier output voltage return to V_{REF} for a duration T_r, as dictated by the one-shot circuit, to prevent glitches and allow proper stabilization. The pixel is fully compatible with AER communication in a pixel array by substituting the delay elements with transistors that activate row and column petitions through a shared bus [21], [22]. For the pixel implementation reported, the period of the positive or negative pulses, T_{pos} or T_{neg}, respectively, is determined by the variation of the deposited charge on the electrode at that moment and is lower for greater variations of the charge. Thus, the frequency of these pulses $f_{p,n}$ can be expressed by the equation:

$$f_{p,n} = \frac{1}{T_{Q_A} + T_r + T_d} \approx \frac{1}{T_{Q_A} + T_r} \tag{2}$$

where T_{Q_A} is the time elapsed to deposit a charge $Q_A = \Delta V_{p,n} C_2$, with $\Delta V_{p,n} = V_{H,L} - V_{REF}$; T_r is the retention time of the one-shot circuit; and T_d is the comparator's delay. For values commonly used in this work $T_r = 1\ \mu s$, and $T_{Q_A} > 5\ \mu s$, T_d can be neglected. T_{Q_A} is related to the total absorbed current for the electrode I_A and the input leakage current, I_{leak}, which models the charge loss on the top MiM capacitor plate as:

$$T_{Q_A} = \frac{\Delta V_{p,n} \cdot C_2}{I_A - I_{leak}} \tag{3}$$

After substituting Eq. (3) in Eq. (2), the sensitivity or gain $K_{p,n}$ of the sensor can be defined as the ratio of the pulse

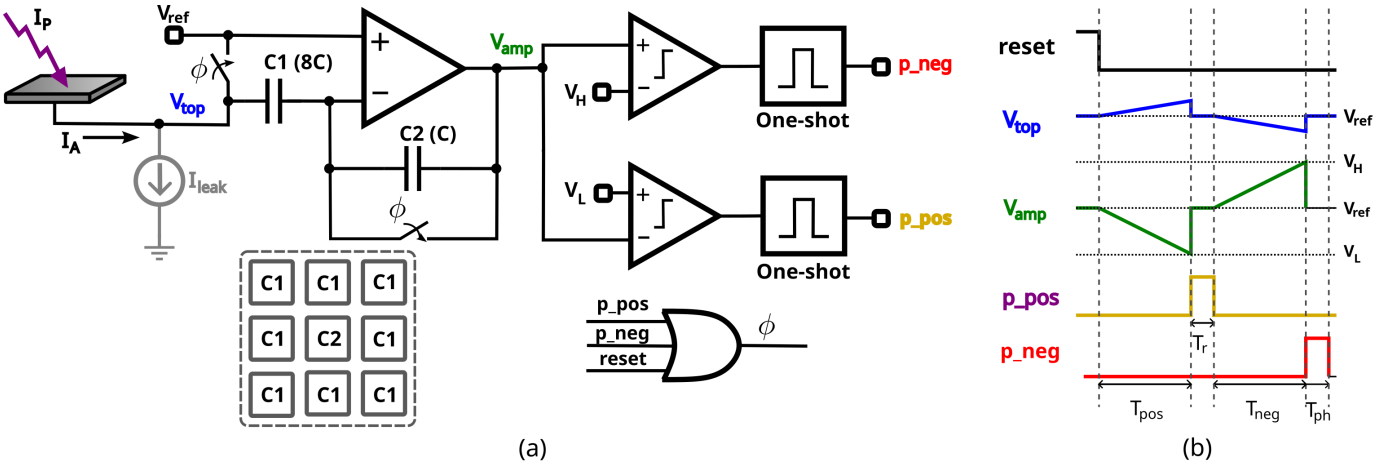

Fig. 1: (a) Schematic of the proposed sensor using the floating metal plate for charge sensing. (b) Waveforms indicating the behavior of the circuit for positive/negative charge detection.

frequency (for positive or negative charges to the absorbed current I_A. It is calculated using the following formula:

$$K_{p,n} = \frac{f_{p,n}}{I_A} = \frac{\left(1 - \frac{I_{leak}}{I_A}\right)}{\Delta V_{p,n} \cdot C_2 + T_r \cdot (I_A - I_{leak})} \tag{4}$$

Upon visual inspection of the curve of sensitivity in Fig. 2, $K_{p,n}$ is a nonlinear function of I_A with three distinct regions given by the following expressions:

$$K_{p,n} = \begin{cases} -\dfrac{I_{leak}}{\Delta V_{p,n} \cdot C_2 \cdot I_A} & I_A \ll I_{leak} \\ \dfrac{1}{\Delta V_{p,n} \cdot C_2} & I_{leak} < I_A < \dfrac{\Delta V_{p,n} \cdot C_2}{T_r} \\ \dfrac{1}{T_r \cdot I_A} & I_A \gg \dfrac{\Delta V_{p,n} \cdot C_2}{T_r} \end{cases} \tag{5}$$

The circuit exhibits high linearity, with constant sensitivity $1/(\Delta V_{p,n} \cdot C_2)$ for a range of absorbed current I_A. The linear range is bounded by a lower limit of I_{leak} and the upper limit given by the largest non-saturating current $I_{max} = (\Delta V_{p,n} \cdot C_2)/T_r$. Consequently, for this range, we can define the Dynamic Range (DR) of the sensor as the ratio between the maximum and minimum detectable currents, including noise components, expressed as:

$$\text{DR} = 20 \cdot \log_{10}\left(\frac{I_{max}}{I_{min}}\right) = 20 \cdot \log_{10}\left(\frac{\Delta V_{p,n} \cdot C_2}{T_r \sqrt{I_{leak}^2 + \sigma_{I_n}^2}}\right) \tag{6}$$

where I_{min} is the minimum detectable current and is a function of the leakage current I_{leak} and σ_{I_n}, the Input Referred Noise (IRN) under dark conditions as defined in [23]. It is worth mentioning that the dynamic range DR can be fine-tuned externally by configuring the voltages V_H and V_L.

The retention time T_r was generated with the one-shot circuit depicted in Fig. 3, which was implemented with logic gates and using a capacitor C_H to retain the pulse for the necessary time defined by:

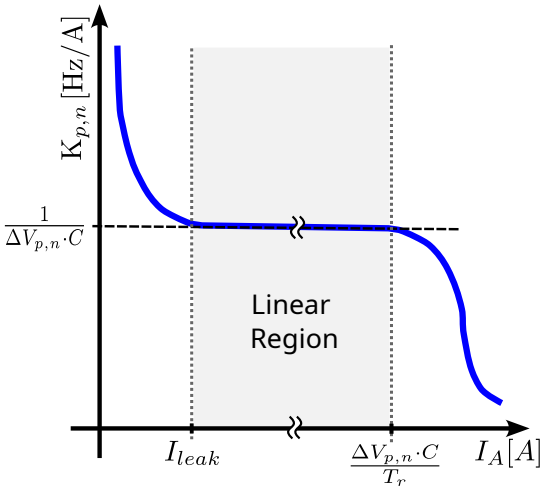

Fig. 2: Sensor's sensitivity ($K_{p,n}$) vs. absorbed current (I_A) highlighting the linear region of operation.

$$T_r = \frac{V_M \cdot C_H}{I_{REF}} \simeq \frac{V_{DD} \cdot C_H}{2 I_{REF}} \tag{7}$$

where I_{REF} is an externally programmable reference current and V_M is the trip point of the inverter cell. The minimum value of T_r is primarily constrained by the charging/discharging time of capacitors C_1 and C_2 through TGs, which is set to be 1 µs based on corner simulations. There is a trade-off between the leakage current in the TGs' off-state and the circuit's settling time, which makes it impractical to use minimum-length MOS devices [24].

B. Circuit layout

The top view of the pixel layout with the MiM capacitors C_1 and C_2 is illustrated schematically in Fig. 4(a). It consists of the feedback capacitor C_2 with a unit capacitance C, and the sensing capacitor C_1 made of eight unit capacitors connected in parallel, with an equivalent capacitance of $8C$. With this configuration, the amplifier has an absolute voltage gain of $C_1/C_2 = 8C/C = 8$.

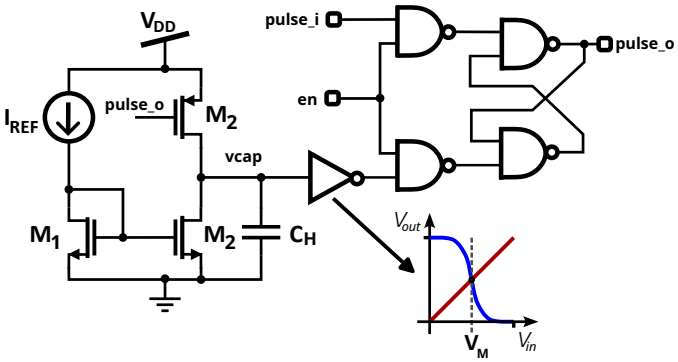

Fig. 3: One-shot circuit implemented using an external current I_{REF}, a latch and a MOS capacitor C_H.

The nine capacitors form a 3 × 3 array where the eight capacitors of C_1 are arranged symmetrically around the central capacitor C_2 to match their electrical characteristics, hence, to achieve a precise gain in the differencing circuit [20]. The connection in parallel of the eight capacitors of C_1 is achieved as follows. First, an intermediate-layer metallization (Metal 5) interconnects the lower electrodes of the capacitors, as depicted in the cross-section view of Fig. 4(c). Then, the circuit is fabricated without a passivation layer above the top electrodes (Metal Top) of the capacitors of C_1 which leaves them exposed. Finally, the eight electrodes are short-circuited with deposited metal on the top, as explained in the next section.

The CMOS ASIC was fabricated with UMC 0.18 µm technology and using a 3.3 V analog/digital supply. The chip was wired bonded in a PGA package. The cover lid was removable so the sensor could be exposed to radiation. Fig. 5 shows a microphotograph capturing a single test structure of the chip, showing the 3 × 3 array of MiM capacitors and adjacent circuitry. The area of the array is 55 µm × 55 µm, and the dimensions of the capacitors of the array are all the same as 10.9 µm × 10.9 µm. The capacitance per unit area of the MiM capacitor available is 1 fF/µm^2, and the actual capacitance values for the capacitors are C_1 = 952 fF and C_2 = 119 fF. The amplifier is a simplified version of the self-biased folded-cascode differential pair proposed in [25]. Two-stage comparators with input rail-to-rail capability were also used as discriminators and TGs with 600 nm length. The analog circuitry was protected by the top metal layer.

C. Rad hardening

After CMOS fabrication, we added a thick metallic layer on top of the capacitor array using a TESCAN SOLARIS UHR FESEM electron microscope equipped with a Focus Ion Beam (FIB). The layer is shown schematically in cross-section in Figs. 4(b) and (c). Fig. 4(d) is an actual SEM image of the capacitor array after the deposition of a platinum layer using the FIB. This layer fulfills several functions: i) It acts as a floating electrode of C_1 that absorbs the incident radiation as long as its energy is below a certain value that depends on the thickness of the metal; ii) It interconnects the top electrodes of the eight capacitors of C_1; iii) It00 shields any device placed beneath against radiation damage; iv) Finally, its safeguards the passivation oxide layer of C_2 from electrostatic charging due to exposure to direct electron irradiation.

The thickness of the deposited metal layer and the nature of the particles play a crucial role in determining the radiation-hardening specifications for the pixel. In the context of this setup, it is important to understand the nature of the electron-matter interaction between the incident electrons and the metallic layer. The collision of an electron with any material causes elastic and inelastic interactions, which primarily produce secondary electrons (SEs) and backscattered electrons (BSEs). The probability of occurrence of these events is quantified by the parameters (yields) η and δ, respectively, which depend on the material and also on the energy of the primary electrons of the electron probe. Therefore, the net current I_A (also referred to as the specimen current) that is absorbed by the top electrode of C_1 differs from the beam probe current I_P hitting the electrode. It can be mathematically defined with the equation:

$$I_A = I_P \cdot (1 - \sigma) \tag{8}$$

where $\sigma = \eta + \delta$ is the total electron emission yield [26].

Fig. 6(a) shows Monte Carlo simulations of the scattering losses occurring when primary electrons impact on the metallic electrode of the sensor using the software CASINO [27]. Some electrons escape from the surface of the electrode as BSEs and SEs, while others become trapped in the metal. The electrons travel in the material with a random path and can reach a maximum depth, Z_{max}, that depends on their initial kinetic energy and the type of metal. Fig. 6(b) shows three curves of the dependence of Z_{max} as a function of the energy of the electrons for three metals, platinum, tungsten, and aluminum. Given the deposited material's non-uniform attributes, it is advisable to uphold a sufficient thickness margin; we validated reliable operation at energies up to 10 keV using 1.2 µm of platinum.

III. SENSOR TESTS

A. Beam irradiation in an SEM

The circuit was tested by irradiating the top metal of the capacitive array with the electron beam of an SEM TESCAN VEGA 4 with a tungsten filament. The electron beam current I_P and the landing energy can be adjusted between 1 pA and 2 nA, and between 200 eV and 30 keV, respectively. Nominal I_P can be calibrated accurately at any time using a picoamperemeter Faraday Cup (FC) available inside the vacuum chamber of the SEM.

The ASIC was soldered to a PCB and interfaced with an FPGA (an Artix-7 Opal Kelly Board) used to control the chip, as displayed in Fig. 7(a). The PCB containing the ASIC was inserted in the vacuum chamber of the SEM as shown in Fig. 7(b), and a feedthrough provided access to the board with a USB 3.0 connection for interfacing with an external PC. Data acquisition and ASIC control were made using a Python interface.

For testing the sensor with electrons, we proceeded as follows: we fixed a value of the energy of electrons to 3 keV; the electron beam, which can be focused to a probe size

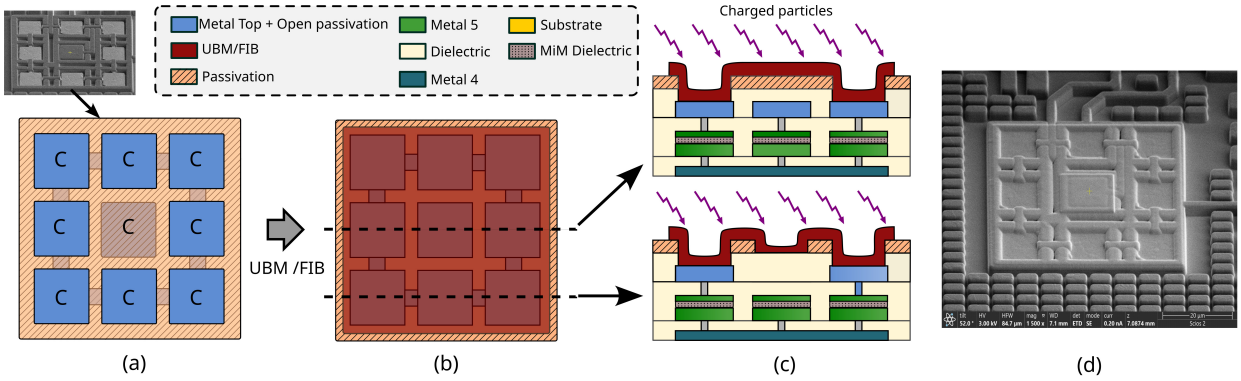

Fig. 4: (a) Top-view of the capacitor array post-CMOS fabrication.(b) Top-view of the capacitor array post-metal deposition via FIB/UBM. (c) Cross-sectional view of the sensor arrangement illustrating the connection with the top metal and MiM capacitors.(d) Microscope image of the capacitor array after 1.2 µm Pt deposition with FIB.

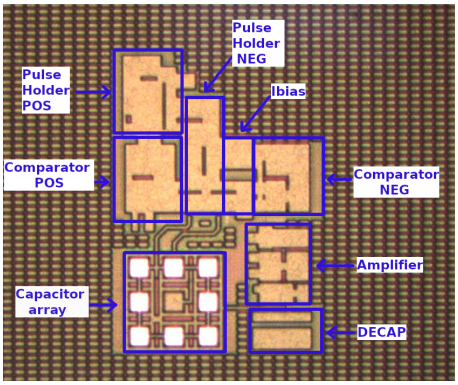

Fig. 5: Light microscope photograph of the die portion containing the single pixel. Dimensions: Capacitor Array (55 µm × 55 µm), Amplifier (30 µm × 48 µm), Comparator (56 µm × 56 µm), Ibias (20 µm × 22 µm), Pulse Generator (22 µm × 46 µm), and DECAP capacitors (29.6 µm × 25 µm).

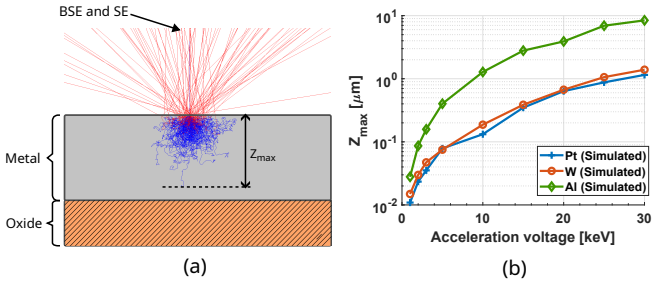

Fig. 6: (a) Electron-metal interaction of a SEM beam, highlighting the maximum reached depth Z_{max}. (b) Z_{max} vs. beam energy for three different materials (Pt, W, and Al).

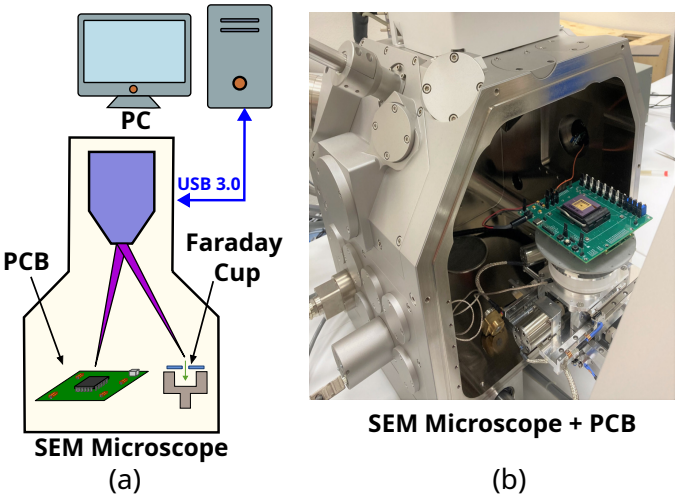

Fig. 7: (a) Primary configuration of the experimental setup employing a SEM with an internal FC and a PC connection. (b) Photography of the PCB with the ASIC inside the SEM's chamber.

diameter smaller than 10 nm, was centered on the capacitor array of the circuit; we measured the signal $f_{p,n}$ generated by the circuit at nine different probe currents I_P in the range between 1 pA and 10 nA. We then repeated the same steps with electrons of 10 keV and with four probe currents within the same range. For each current step, I_P was independently calibrated using the FC.

IV. Experimental Results

A. Sensitivity

Fig. 8 shows the frequency measurements f_n with different probe currents, I_P, and at 3 and 10 keV. As previously stated, the frequency depends on I_A, the actual net current at the input electrode. By employing calculations derived from (2) using the values of I_P and I_A separately, it becomes possible to extract the values of σ in the model presented in Eq. (8). At higher energies, discrepancies between the results and calculations begin to emerge. One possible explanation for this disparity is the non-uniform nature of the deposited platinum, which can be attributed to deposited metal contamination with other elements from the precursor gas and residual molecules in the chamber [28].

Table I shows the estimates for the input current leakage I_{leak} derived from pulse frequency measurements with no input stimulus at a junction temperature of T_j = 25 ^oC. The expression in Eq. (2) for $\Delta V_{p,n}$ = 0.2 V was utilized to derive these estimates. Additionally, these values can be utilized to calculate the dynamic range. The positive pulses observed for all measured samples indicate that the leakage current was mostly injected from V_{REF} through TGs.

Using the frequency measurements obtained with 3 keV, it is possible to construct the plot of the sensitivity $K_{p,n}$ using the Eq. (4). Fig. 9 illustrates the K_n as a function of I_P. The plot includes the minimum and maximum bounds for sensitivity obtained through simulations considering process variations. These results were compared with the theoretical model described in Eq. (4), and by treating I_{leak} as a fitting

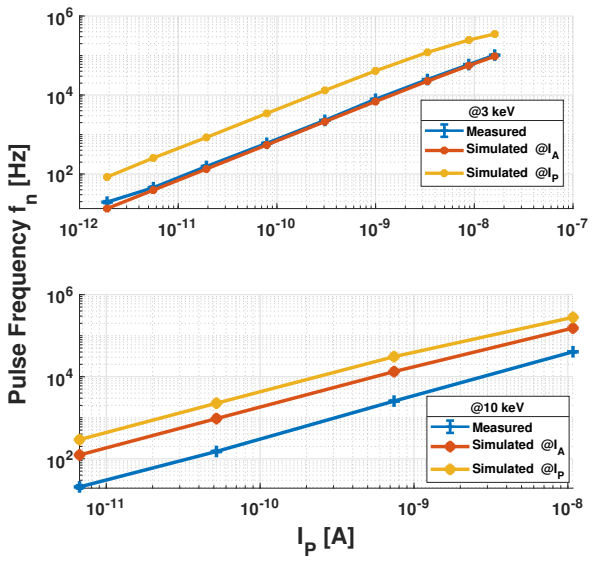

Fig. 8: Relationship between pulse frequency and the current probe I_P for negative charges at two different energy levels (3 and 10 keV).

TABLE I: Measurement results for the leakage in four different samples and estimation of DR using Eq. (6).

Parameter	Sample			
	#1	#2	#3	#4
I_{leak} $^{(a)}$	5.0 fA	4.7 fA	7.5 fA	13.2 fA
DR $^{(b)}$	119 dB	119 dB	119 dB	118 dB
$^{(a)}$ Measured at T_j = 25 ^{o}C.				
$^{(b)}$ Estimated for $\Delta V_{p,n}$ = 0.2 V.				

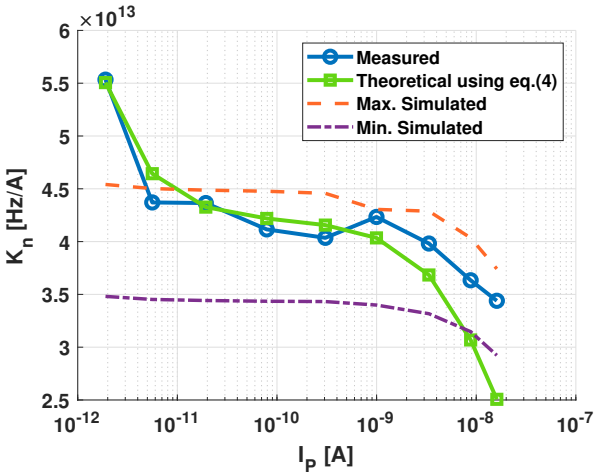

Fig. 9: Sensitivity K_n as a function of different current probes I_P, obtained from measurement results, theoretical expressions, and simulation values.

parameter, we obtained a value of -590 fA. This value is higher than measured under typical conditions and shown in Table I due to the very poor thermal dissipation inside the vacuum chamber of the SEM. During prolonged tests lasting over 30 minutes, junction temperatures exceeding 65 ^{o}C were observed. This highlights the need for new strategies to manage the heat generated by the electronics, which may involve allocating the FPGA and main regulators outside the vacuum chamber.

Finally, Fig. 10 shows an extrapolation of the yield (σ)

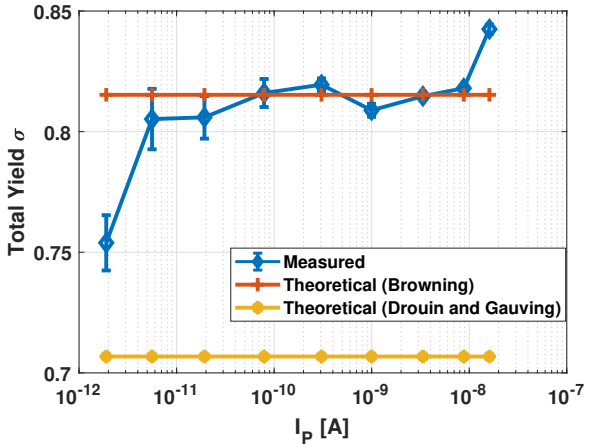

Fig. 10: Total electron emission yield (σ) as function of different current probes I_P obtained from measured data, Browning [11] and Drouin and Gauving [29] models.

based on the pulse frequencies obtained using the energy of 3 keV and the Eq. (8). This value was compared with two different theoretical models of σ (Browning [11], and Drouin and Gauving [29]) through simulations using CASINO [27]. Based on the measured data, the Browning model was found to be the best fit.

B. Noise

The noise characterization was conducted under dark conditions (no beam exposure) while varying the voltages V_H and V_L around V_{REF}. First, it is necessary to consider the offset (V_{OS}) of the amplifier and the comparator. This can be achieved by performing a coarse adjustment until pulses are observed in both positive and negative directions. The imbalances between both sensitivities will indicate the sign of V_{OS}. The subsequent stage entails a fine adjustment of the threshold associated with the offset direction (V_H or V_L). We employed the least significant bit (LSB) voltage (805 µV) from a 12-bit DAC, specifically the TI DAC124S085 part [30], as the incremental step for sweeping. The average frequency of the pulses was recorded until it reached the reference voltage (V_{REF}), as depicted in Fig. 11. Using the measured data, we can estimate the offset voltage of the combined comparator and amplifier setup ($V_{OS} \approx 4.6$ mV). By displacing the data by V_{OS} and converting the values to input-referred current, we calculated the Input-Referred Noise (IRN). The resulting value for σ_{I_N} is 24.8 fA$_{rms}$. This value also includes the noise from the voltage threshold references, which was not disclosed in the datasheet. Future improvements should focus on enhancing reference controllability through on-chip implementation to achieve lower noise and improved signal integrity.

V. Discussion and Benchmarking

Table II compares the specifications of the implemented sensor with other works focused on charge detection. Medipix [16] is a commercial focal-plane array that relies on vertical integration, i.e., the radiation is absorbed in a semiconductor layer that is connected with a flip-chip assembly to the readout

TABLE II: Comparative analysis of State-of-the-Art approaches.

Parameter	This work	Sakamoto (2012) [31]	Medipix (2013) [16]	Song (2020) [6]	Song (2022) [32]
Technology	0.18 µm CMOS	0.2 µm CMOS	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Manufacturing	Planar (On-chip)	Planar (On-chip)	3D Integration (Flip-Chip)	External FC (PCB)	External FC (PCB)
Supply Voltage	3.3 V	3.3 V / 1.5 V	1.5 V	1.8 V	1.8 V
Power Consumption (per pixel)	161 µW	ND	9 µW	5.5 mW	2.2 mW
Rad Hard	Yes (Low Energy)	Yes (Low Energy)	Yes (Hybrid)	Yes	Yes
Conversion Gain	1.43 $\mu V/e^-$	150 μV/ion	11.4 $\mu V/e^-$	8.9 $\mu V/e^-$	15.0 $\mu V/e^-$
Dynamic Range	118 dB$^{(a)}$	70 dB	ND	ND	ND
IRN	7031 e^-rms	3 ions$^{(b)}$	80 e^- to 175 e^-	475 e^-rms	221 e^-rms
Sensing Area	55 µm × 55 µm	7 µm × 7 µm	55 µm × 55 µm	1 cm × 1 cm	ND
Complexity	96 transistors	4 transistors	~ 1600 transistors	> 23 transistors	ND
Latency	1 $\mu s^{(c)}$	1 μs	491 µs/ frame	NA	NA
Dark Current	7.6 fA$^{(d)}$	ND	−10 nA to +20 nA	30 pA	ND

$^{(a)}$ Measured at $\Delta V_{p,n}$ = 0.2 V. It could reach up to 138 dB using $\Delta V_{p,n}$ = 1.6 V.
$^{(b)}$ Measured at T = 181 K.
$^{(c)}$ In a closed-loop configuration utilizing a one-shot circuit. The delays of logic cells and collisions constrain the effective latency in AER implementations.
$^{(d)}$ Mean value with σ = 3.9 fA.

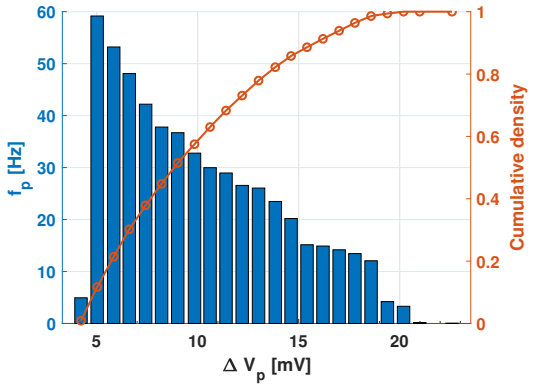

Fig. 11: Frequency of the positive pulses varying V_H near to V_{REF} ($\Delta V_p = V_H - V_{REF}$) for a sampling duration of 300 s.

circuit placed beneath in a different die. This technology is rad-hard and has high sensitivity due to the intrinsic amplification mechanism given by absorbing the energy of the incoming radiation that is converted into free electron-hole pairs. On the other hand, it has several limitations: i) vertical integration is costly, has low yield, and requires advanced fabrication nodes; ii) the sensitivity is non-linear with energy and with fluency; and iii) the thickness of the sensing layer must be adjusted carefully for the energy range used.

The detector proposed in this work measures the net charge accumulating in a capacitor, which depends on the total scattering yield σ. The yield is close to one, meaning it does not amplify the signal, resulting in much lower sensitivity. Nevertheless, a sensor based on charge sensing can be competitive in terms of dynamic range, linearity, latency, and power consumption. The dynamic range is much higher (when operating in integration mode) than other technologies (see Table II) for two reasons: Firstly, the proposed pixel conveys its information with asynchronous logic, assuring fast operation to track quick charge variations. Secondly, the minimum detectable current, which is limited by the INR is very low, and it can be used for the detection of radiation with very low kinetic energy, something that can be much more difficult with flip-chip sensors [33].

The proposed sensor here is compatible with standard CMOS planar integration. This design was conservative and future versions of the circuitry in Fig. 5 can be positioned to fit beneath the sensing array of capacitors, with some blocks needing further optimization. This can transform the test structure into a rad-hard pixel to be used as the sensing unit of a focal-plane array with a high fill ratio. Using the common-centroid distribution of capacitors for the sensing part offers an advantage as it minimizes offsets between adjacent pixels, leading to a reduction in Fixed Pattern Noise (FPN). Pixels can be arranged in a pixel matrix connected to AER arbitration circuitry, and in that case, one-shot circuits will no longer be needed. Modern AER readout circuitry channels can cope with pixel event rates up to 100 Meps [21], [22]. That is enough to render images with pixelated sensors that convey pixel information using Pulse Density Modulation (PDM) encoding [34].

The compactness and high sensitivity of such an imager design would qualify it for its use in electron microscopy but also for other charge detection applications, such as mass spectrometry and space radiation detectors, or in sensors based on electrostatic induction for bio-sensing [2], [35]. FIB deposition is not scalable to large pixel arrays; therefore, alternative approaches must be investigated to make such a rad-hard focal-plane array. Vertical integration technologies offer Top Surface Metallurgy (TSM) to implement vertical interconnections. This extra metalization layer can harden the pixels against radiation without requiring a costly flip-chip hybridization process after fabrication [36].

VI. Conclusions

We have designed a charge-sensitive sensor that is compatible with integration in any modern CMOS technology. It can be used for measuring ionizing radiation impacting the electrode of an input capacitor that was made rad-hard by depositing a 1.2 μm thick platinum layer on top of it. The sensor has been tested by irradiating it with electrons in a scanning electron microscope, SEM, displaying high dynamic range, rad-hardness, and linearity at beam currents between 1 pA-10 nA and kinetic energies between 3 keV and 10 keV. The gain and noise performance have been characterized, and the results show good agreement with simulations. The circuit features are competitive in terms of dynamic range and latency. With further development, it can be integrated as part of a focal-plane array that conveys output data off-chip with the AER asynchronous protocol. Future work will be carried out to integrate the circuitry beneath the capacitor array.

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