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ABSTRACT

ARIEL is an ESA mission whose scientific goal is to investigate exoplanetary atmospheres. The payload is composed by two instruments: AIRS (ARIEL IR Spectrometer) and FGS (Fine Guidance System).

The FGS detection chain is composed by two HgCdTe detectors and by the cold Front End Electronics (SIDECAR), kept at cryogenic temperatures, interfacing with the F-DCU (FGS Detector Control Unit) boards that we will describe thoroughly in this paper. The F-DCU are situated in the warm side of the payload in a box called FCU (FGS Control Unit) and contribute to the FGS VIS/NIR imaging and NIR spectroscopy.

The F-DCU performs several tasks: drives the detectors, processes science data and housekeeping telemetries, manages the commands exchange between the FGS/DPU (Data Processing Unit) and the SIDECARs and provides high quality voltages to the detectors.

This paper reports the F-DCU status, describing its architecture, the operation and the activities, past and future necessary for its development.

Keywords: Exoplanets atmospheres, NIR spectroscopy, Infrared radiation, Infrared telescopes, Remote sensing, Photometry, FGS-Fine Guidance Sensor

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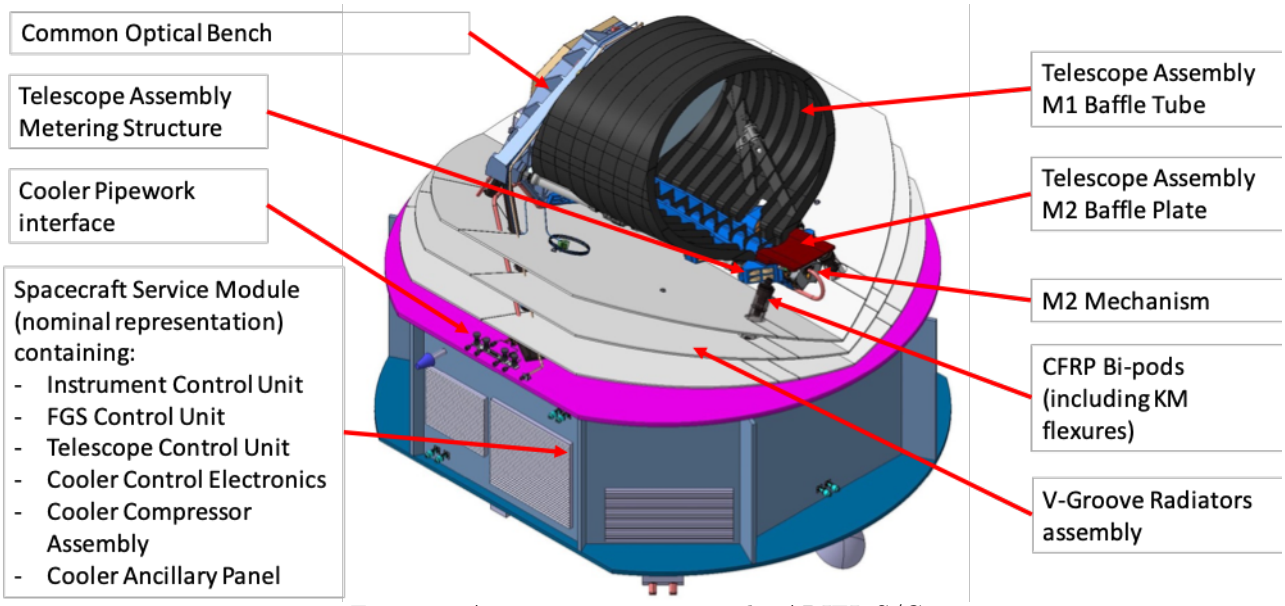


Figure 1: An image representing the ARIEL S/C.

1. INTRODUCTION

ARIEL (Atmospheric Remote-sensing InfraRed Large-survey)[1] is a medium-class mission of the European Space Agency, part of the Cosmic Vision program (M4), whose launch is foreseen by early 2029.

ARIEL aims to study the composition of exoplanet atmospheres, their formation and evolution by performing infrared spectroscopy of a large number of transiting exoplanets with temperatures from $\sim 500\ K$ to $\sim 3000\ K$. During its 6 years of mission (4 nominal and 2 extended), ARIEL will observe about 1000 planets with one or more of the following methods: transit, eclipse and phase-curve spectroscopy.

The ARIEL spacecraft[2] hosts an off-axis Cassegrain infrared (IR) telescope[3,4] with a $1\ m \times 0.7\ m$ primary mirror, built in solid Aluminium and feeding two instruments:

- AIRS (ARIEL InfraRed Spectrometer) that will perform IR spectrometry in two wavelength ranges: between 1.95 and 3.9 µm (with a spectral resolution $R > 100$) and between 3.9 and 7.8 µm, with a spectral resolution $R > 30$.
- FGS (Fine Guidance System)[5] , an instrument with three narrow-band from visible to near-infrared photometer channels (two of them used as guidance sensors as well as for science) and a low-resolution near-infrared spectrometer, that will be further described in Section 2.

This paper presents the F-DCU design status and an overview of its development prior the PDR (Preliminary Design Review) and just before the MRR (Manufacture Readiness Review) that represents the start of the production of the first three Engineering Model (EM) samples. In Section 2 we describe the FGS instrument, in Section 3 we go in detail with its internal architecture and in Section 4 we illustrate the functions that the F-DCU shall provide, including interactions with the other boards composing the FCU: the Data Processing Unit (DPU) and the Power Supply Unit (PSU).

Section 5 describes the activities related to F-DCU production (analyses, tests, etc.) and, finally, Section 6 draws the conclusions.

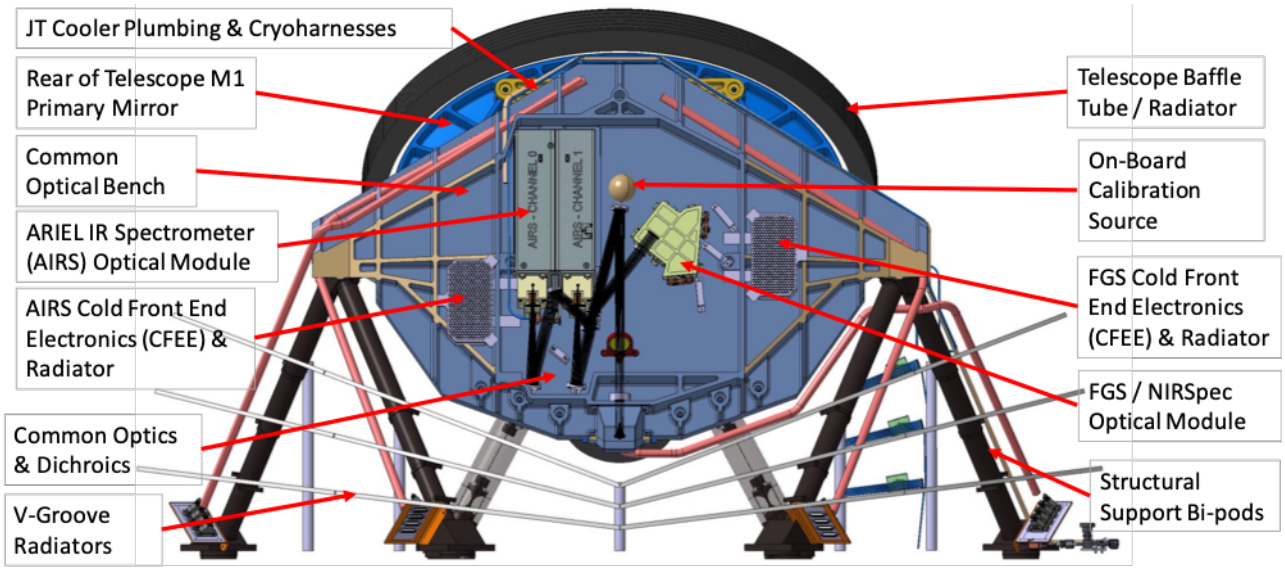


Figure 2: A view of the Telescope Optical Bench with the instruments' cold boxes. The On-Board Calibration Source is not in the baseline anymore.

2. FGS INSTRUMENT

The Fine Guidance System main task, as suggested by its name, is to provide information on changes of the telescope's Line of Sight (LoS) to the S/C AOCS (Attitude and Orbit Control System) with a cadence of 10 Hz and with the goal of reaching a 0.02 arcsec pointing accuracy for brighter targets. The AOCS combines the information on the LoS provided by the FGS with the inputs coming from the gyroscopes and from the star trackers and provides these data to the control loop, stabilizing the spacecraft actuating the reaction wheels and the thrusters to obtain the required stability.

Beyond ensuring centering, focusing and guidance to the satellite, FGS also provides high precision astrometry and photometry of the target star that can be used for de-trending and science data analysis on ground. To meet its goals for guiding and photometry, the ARIEL telescope[67] feeds four spectral bands (see Figure 4b) to FGS:

- FGS-1: 0.8-1.0 µm;
- FGS-2: 1.0-1.2 µm;
- VIS-Phot: 0.50-0.55 µm;
- NIR-Spec: 1.25-1.95 µm, low resolution spectrometer ($R > 10$).

FGS-1 and 2 are the primary and redundant FGS channels. The four spectral bands (and the light feeding AIRS, too) are selected using dichroic mirrors from D1 to D5, mirrors and filters (see Figure 4b).

2.1 FGS structure

The FGS instrument is composed of:

1. Two metallic enclosures situated in the cold part of the payload (@ 55 K) in the instrument bay, a cavity carved in the Telescope Optical Bench (TOB):
   (a) The FGS Optical Module containing the final part of the optics and two H2RG (Teledyne) detectors;

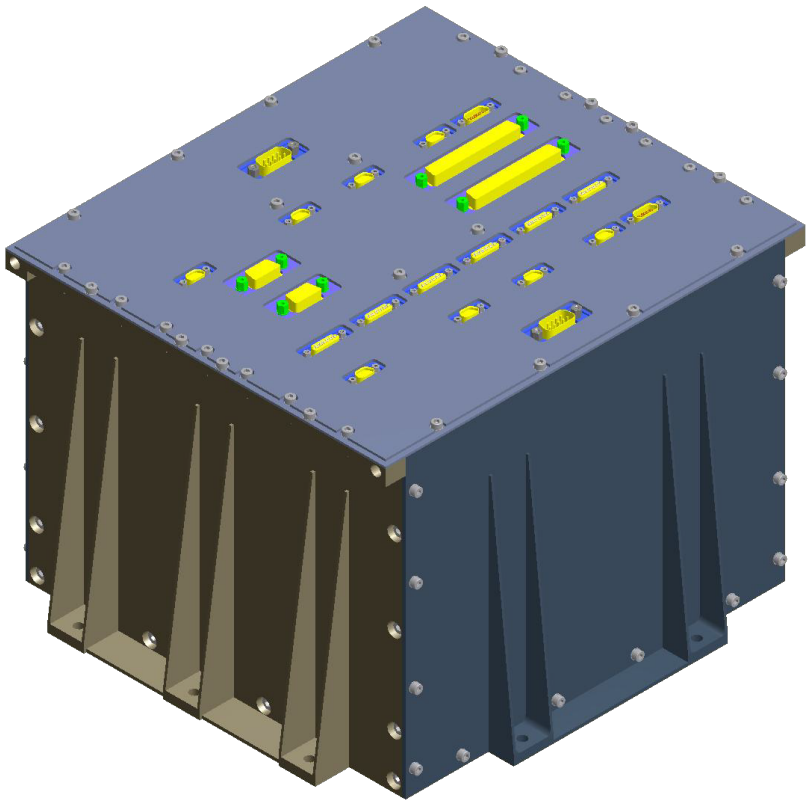


Figure 3: FCU box mechanical drawing.

(b) The Focal Plane Electronics (FPE) hosting the cold Front End Electronics (SIDECAR) and whose cover acts as a radiator.

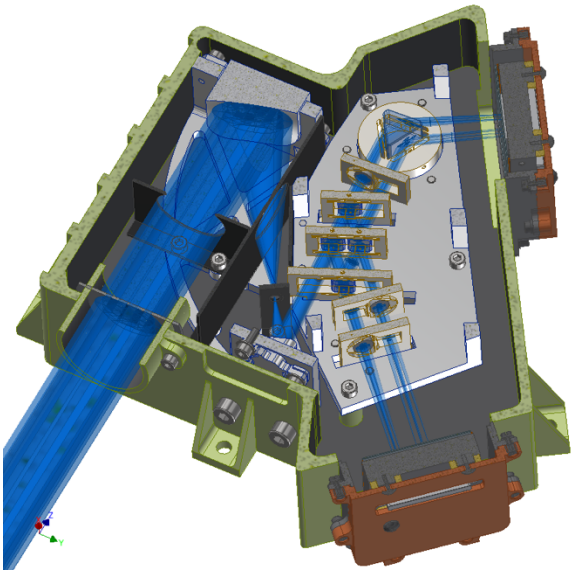
2. The FCU (FGS Control Unit):[8] an electronic box accommodated in the "warm" side of the spacecraft,[4] at a temperature of about 300 K. The FCU hosts the F-DCU modules (warm Front-End Electronics) that control and read the detectors and carry out the data processing for centroid calculation and image processing.

SIDECAR (System Image, Digitizing, Enhancing, Controlling, And Retrieving) is an ASIC (Application Specific Integrated Circuit) produced by the same Company (Teledyne) supplying the detectors. It has been used in NISP instrument on-board Euclid mission interfacing with the Focal Plane and providing output digitization.

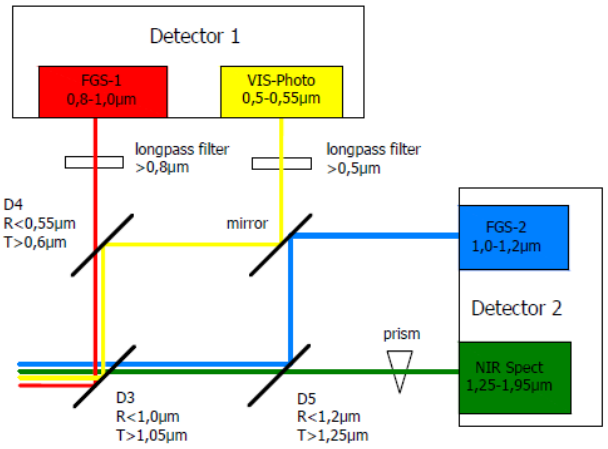
Inside the FCU, beyond F-DCUs, are also hosted other five boards:

- Two Data Processing Units (DPU)[9] – working in cold redundancy scheme
- Two Power Supply Units (PSU) – working in cold redundancy scheme
- One F-TCU (FGS Thermal Control Unit) – not redundant

The detectors and the associated Front End Electronics (SIDECAR and F-DCUs) work in "warm" redundancy, meaning that they are permanently switched on. On the contrary, DPU and PSU operate in "cold" redundancy, meaning that only the nominal ones are normally active and that the redundant pair is switched-on only in case of a failure of the first one.



(a) The FGS Optical Module, showing the light paths.



(b) Schematic of dichroic splitting of channels within the FGS.

Figure 4: FGS optical path.

2.2 FGS key requirements

In normal operation both FGS-1 and FGS-2 work simultaneously, such that the first channel is used for guiding purposes and the second can provide photometric measurements. FGS-1 detector and VIS-Phot channel require smaller windows (e.g. 30×30 pixels each). Anyway, full window size is required at the beginning during the phase of searching predefined star and to start the guiding procedure. When the star reaches the optical axis of the ARIEL telescope, the window can be reduced and a simplified procedure for data transfer can be adopted.

In tracking mode, the star coordinates measurement error across the LoS (at 10 Hz) shall be lower than 20 mas (milli-arcsec) for bright targets and 150 mas for fainter targets.

The focal plane array (FPA), hosts two HgCdTe detectors HAWAII-2RG (2048×2048) from Teledyne Imaging Scientific (TIS)

1. One for imaging in 0.5-0.55 µm and in 0.8-1.0 µm bands;
2. One for imaging in 1.0-1.2 µm band and low-resolution spectroscopy in the NIR range 1.2-1.95 µm.

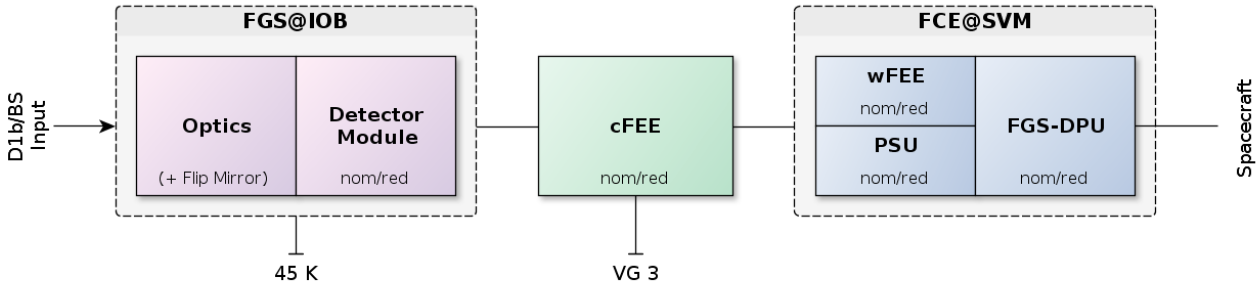


Figure 5: FGS Top-level architecture. The V-groove #3 is at an intermediate temperature of about 130 K.

2.2.1 Readout

The FGS collects images (and spectra) from the two detectors, as well as housekeeping telemetries, and sends them to the SVM (Service Module) to be further addressed to ground. The F-DCU receives from each SIDECAR packets containing from 1 to 4 consecutive complete rows (2048 pixels each) at 16 bits. The image processing consists in the extraction of up to 2 crop zones from the packets. Each crop zone is then elaborated by a Finite State Machine on the F-DCU, reordered and temporarily buffered into the SDRAM memory. As soon as the crop zone to be sent as first is completely received, the DMA (Direct Memory Access) block starts the upload of the image to the DPU through the SpaceWire connection.

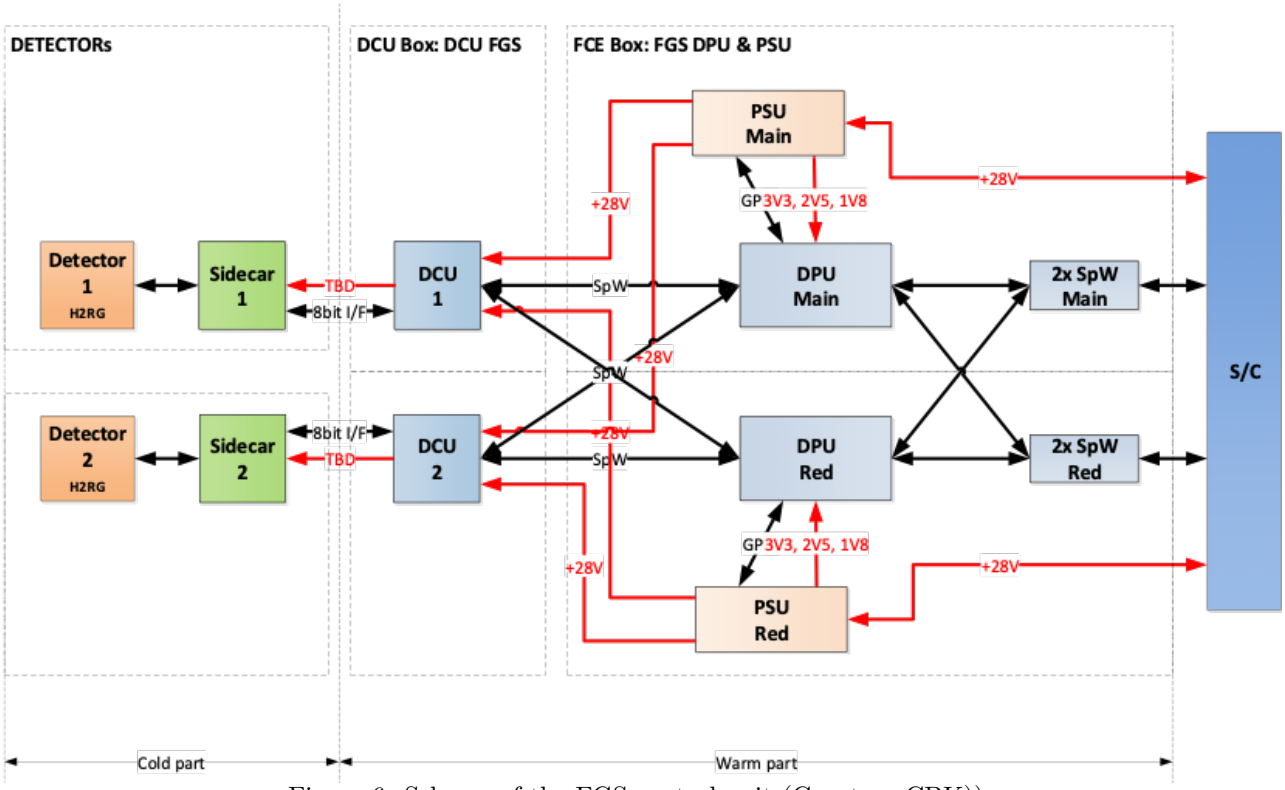


Figure 6: Scheme of the FGS control unit (Courtesy CBK)).

2.2.2 Data rate

The overall telemetry contribution of the FGS depends on the parameter configuration; anyway, it is less than 4 kbit/s if no images are sent and less than 79 kbit/s in measurement mode.

3. DETECTOR CONTROL UNIT: DESIGN DESCRIPTION

The F-DCU,[10] controlled by the DPU electronics, acquires and processes science data. Its architecture is illustrated in Figure 7 and can be split in two parts: a digital section (Paragraph 3.1), hosting the logic (FPGA), the memory (SDRAM) and the communication interfaces, and three isolated sections (Paragraph 3.2) dedicated to the production of the secondary voltages needed to operate the cold Front End Electronics and the detectors.

3.1 Digital section

The F-DCU digital section consists of the following main blocks:

1. Power conditioning;
2. Logic (FPGA);

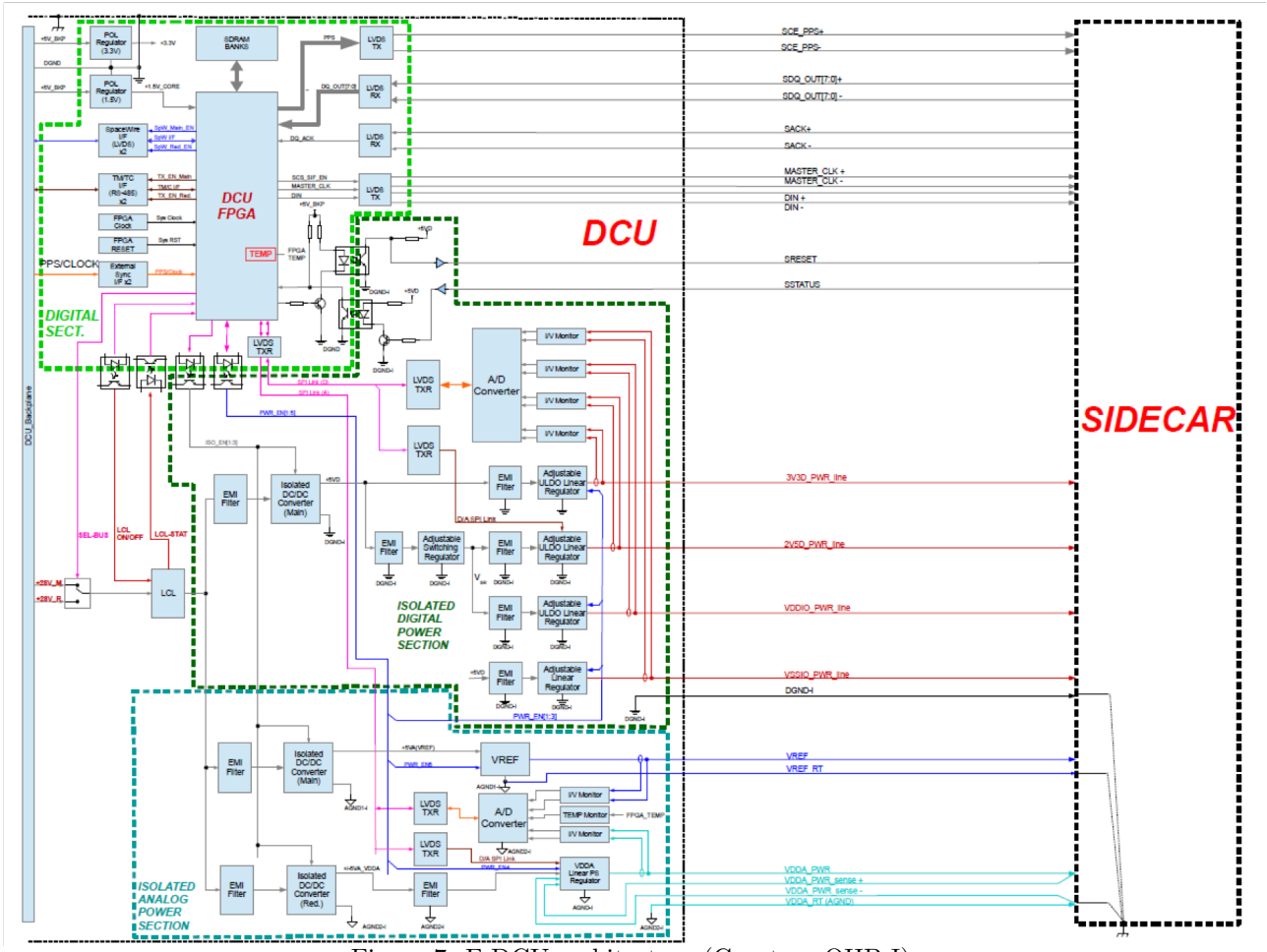


Figure 7: F-DCU architecture (Courtesy OHB-I).

3. SDRAM memory banks;
4. LVDS interfaces for data exchange with the SIDECAR;
5. SpaceWire I/F for data exchange with the DPU.

Each of these blocks has been further detailed in the following paragraphs.

3.1.1 Power

The digital section is powered by a single +5V line provided by the PSU. This voltage is converted to +3.3V and lower voltages (necessary to supply the FPGA core) by means of high efficiency buck switching regulators.

3.1.2 FPGA

The logic on-board the F-DCU is in charge of a FPGA (Microsemi RT ProASIC3), whose duties are: control the SIDECAR, process science data, manage SDRAM memory and communicate with the DPU. Figure 8 describes its internal architecture.

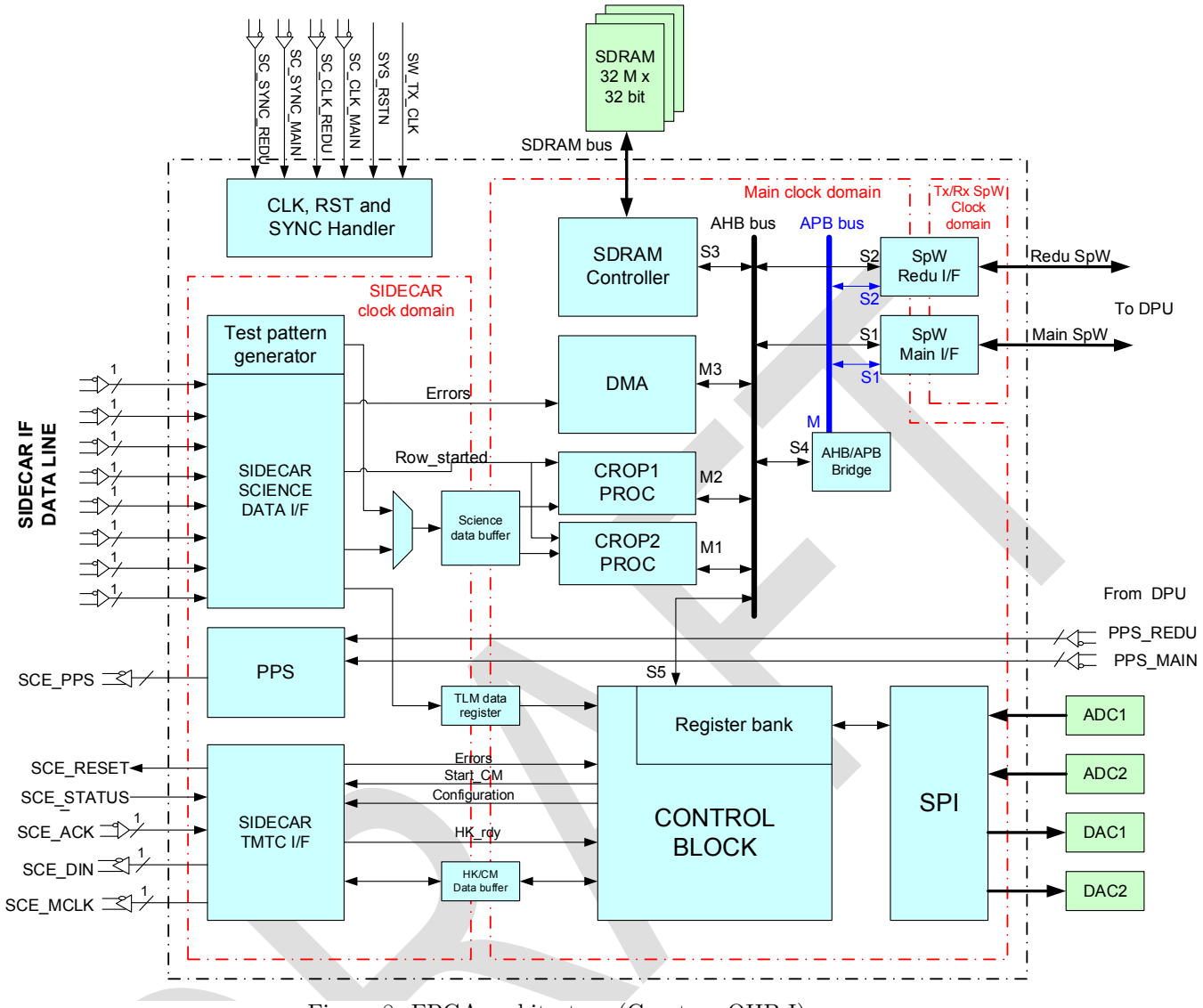


Figure 8: FPGA architecture (Courtesy OHB-I).

3.1.3 SDRAM

The F-DCU implements buffering of the images by means of an external SDRAM memory whose total dimension is $32M \times 32bit$ (1Gbit) and that is protected from radiation-induced events with an EDAC (Error Detection And Correction) system. The SDRAM memory is connected to the FPGA via a dedicated bus and can be accessed by the DPU using a DMA engine, implemented to rapidly transfer the cropped data from the SDRAM buffer using standard SpW packets. The link between the F-DCU and the DPU is implemented with two SpaceWire connections working at a frequency of 60MHz and a maximum data rate of 48Mb/s.

3.1.4 LVDS interfaces

The F-DCU communicates with the SIDECAR by means of two different links:

1. The scientific and telemetry data produced by the SIDECAR during normal operations are delivered in parallel (through 8× LVDS interfaces, described in Paragraph 4.1.1) to the F-DCU electronics;

2. A serial LVDS line (described in Paragraph 4.1.2) is used to set register values on the SIDECAR and for communicating housekeeping requests from the DPU.

3.1.5 SpW interfaces

For redundancy reasons, the FPGA implements two SpaceWire connections that connect the F-DCU board to two different DPU (Nominal and Redundant).

3.2 Isolated power sections

The F-DCU includes three distinct isolated power conditioning sections providing several different power supply voltages in order to satisfy SIDECAR needs:

1. Digital voltages (3V3D, 2V5D, VDDIO/VSSIO);
2. Analog voltage (VDDA);
3. Reference voltage (VREF).

These sections share some common characteristics, such as:

- Each section is provided with isolated DC/DC converters;
- Each DC/DC converter is supplied via LCL (Latched Current Limiter) blocks that act as power switches;
- They are controlled from FPGA by means of optically decoupled discrete signals;
- There are EMI filters to reduce the output ripple voltage.

The transmission of housekeeping telemetries (temperatures, voltages and currents), acquired by A/D converters, are performed using LVDS transceivers. Also the use of latching relays allows to isolate both hot and return lines of the inactive bus, thus preventing formation of ground loops.

3.2.1 Grounding scheme

All the precautions to avoid ground loops are adopted because they could pick electromagnetic disturbs from the surroundings, then representing possible noise sources. The F-DCU sections dedicated to producing the SIDECAR power lines are fully isolated with respect to the FCU, so the communications internal to the F-DCU are performed using either optically isolated or balanced (LVDS) interfaces. The F-DCU digital section has the same digital ground (DGND) of the whole FCU. DGND is distributed by the FCU backplane and is connected to the chassis and from this to the S/C structure. On SIDECAR side, the analogue and digital grounds are connected together in star-point and referred to the chassis via dedicated connection.

In general (with the exception of VDDA), the primary voltage is transformed from +28V to an intermediate level, using a switching buck regulator (so to enhance power conversion efficiency), before to be fed to the low drop-out (typically 500mV) linear post regulators.

3.2.2 SIDECAR Digital voltages

3V3D:

This power line, used by the SIDECAR digital section complies with the following specifications:

- 3.3V nominal value;
- Output voltage accuracy over line, load and temperature: +2.0%

2V5D:

This programmable voltage regulator is based on a digitally controlled current source. The main specifications are:

- 2.5 V nominal value;
- Maximum nominal load current: 24 mA
- A soft-start mechanism, that limits the inrush current within two times the maximum nominal load current.

VDDIO/VSSIO:

These power lines are driven by two linear regulators: one sourcing current to the load and the second sinking the same current.

3.2.3 VDDA

This extremely controlled voltage has two wires for load sensing to ensure accurate regulation in correspondence of the SIDECAR board. It is finely adjusted using a D/A converter piloted by the F-DCU FPGA via a SPI interface and protected against out-of-range events.

3.2.4 VREF (3.3V)

The VREF generation is based on the use of a low noise band-gap voltage reference, providing a very stable and highly accurate output voltage with the following specifications:

- 3.3 V ±0.05% reference voltage
- Accuracy over temperature: ±0.15%
- Accuracy over radiation: ±0.25%

4. F-DCU OPERATIONS

The F-DCU manages the SIDECAR and the corresponding H2RG detector, performing the following tasks:

1. Provides to SIDECAR telecommands and acquires telemetries and 8-bit parallel science;
2. Processes data (image cropping + HK extraction), these functions are implemented in a reprogrammable RT ProASIC FPGA;
3. Supplies several very low noise power voltages with power sequencing, voltage adjustment via DAC and return current isolation, overvoltage and overcurrent protections and a very clean grounding scheme.

From the DPU side, the F-DCU board is controlled via SpW RMAP link and provides science data on the same link through autonomous SpW packet transmission.

4.1 Control & TM/TC

The F-DCU receives commands from the DPU and translates them into SIDECAR or local (e.g. FPGA read/write) commands. This is done through a set of registers and memory areas that allow the DPU to monitor, command and configure both F-DCU and SIDECAR functions.

The F-DCU performs also SIDECAR error detection (invalid transmission checksum, missed command, wrong line/frame and power supply fault) and error register implementation.

- Implementation of some synchronous serial interfaces
- SIDECAR power supply monitoring in real-time and handling of power up and power down sequencing;

The front-end interface that connects the F-DCU to the SIDECAR is split into 2 main sections: science data interface and TM/TC interface. The first is used to receive science data and extract the telemetry values while the second provides a serial bidirectional path to write/read configuration data or dump internal registers. Only the scientific data stream is allowed to transmit autonomously.

4.1.1 Science data IF

The packet transmission is initiated, On this interface, by the SIDECAR, after having received an exposure command. Science data is transmitted in parallel on a 8× LVDS interface in packets containing 1 to 4 detector rows ($2048 \times 2Bytes$ each). The packet used by the transmission protocol includes a header, the data cargo and a CRC16 checksum at the end. The FPGA science data I/F splits this packet and provides the telemetries to the control logic and the science data to the processing logic. The image pre-processing is operated by a Finite State Machine into the FPGA, the cropped zones extracted from the packets are reordered and downloaded into the SDRAM memory in a temporary image buffer. When the next cropped zone is complete, the Direct Memory Access module starts the image upload towards the DPU through the SpaceWire connection .

4.1.2 TM/TC IF

This interface is used to read and write internal registers or memory areas of the SIDECAR. No autonomous transmissions from the SIDECAR are allowed on this interface and only the F-DCU can perform read/write operations.

When the DPU wants operate on the SIDECAR, it must configure the SIDECAR register area present on the F-DCU and then raise a "send" command to the F-DCU to execute the desired operation. In this way, the DPU can access all SIDECAR functionalities.

4.2 Data Processing

The data pre-processing (image cropping and HK extraction) is implemented in the FPGA. After the reception of the data stream from SIDECAR and the pixel de-serialization, the F-DCU extracts a maximum of 2 crop area from each stripe and buffers the telemetries in the local SDRAM. The telemetries are separated from scientific data and the values are used by the control logic to generate a 128 entries TM table stored in SDRAM and accessible to the DPU via RMAP.

4.3 Power Control

The F-DCU supplies several very low noise power lines and a voltage reference. More details are given in paragraphs from 3.2.2 to 3.2.4 describing the Power supply section design. Monitoring in real time of the power supplies and of the overvoltage and overcurrent protections is provided as well as the handling of power-up and power-down sequencing. The power consumption is very low ($< 3.5\ W$)

5. F-DCU DEVELOPMENT

5.1 Heritage

The design of the F-DCU boards proposed for the ARIEL mission rely on the heritage of the DCU board developed for the NISP instrument adopted by the Euclid mission. The reuse of the project has been done with only minor modifications limited to the PCB and the reprogrammable FPGA.

5.2 F-DCU Model Philosophy

The F-DCU Model Philosophy, comprises the following models:

1. **Engineering Model (EM)**, functional and electrical representative of flight standard, used to verify the F-DCU functionalities inside the FCU and for Application SW development;
2. **Engineering Qualification Model (EQM)**, flight representative in form, fit and functions, i.e. including electrical, printed circuit boards, thermal, mechanical fidelity;
3. **Avionics Verification Model (AVM)**, EM build standard, functionally representative and with flight representative interfaces. Contributes to the payload AVM campaign;
4. **Flight Model (FM)**, final model for integration in FCU FM and launch;

Figure 9: An image of the Euclid DCU board (Courtesy OHB-I)

5. **Flight Spare (FS)**, flight spare, ready to substitute one of the FM boards in case of major problems.

In particular, concerning the EQM, military grade or lower-level parts can be used instead of high reliability parts, provided they are procured from the same manufacturer with the same packaging. Use of FM proto devices is also admitted. Manufacturing will be performed using the same processes that will be applied on the FM. Full traceability of changes, if any, between EQM and FM will be provided. One of the EQM boards (EQM1) is subject to a complete qualification campaign at board level. The remaining EQM boards are integrated in FGS model, perform the qualification and then delivered to RAL for integration in the EM model.

Table 1: F-DCU models utilization summary.

Model	#	Phase	Purpose	Notes
EM	3	B2	to reduce the risks on the EQM and FM models	not deliverable to RAL
EQM	3	C/D	EQM1 subj. to compl. tests at board level	
AVM	1	C/D	contributes to AVM camp. at RAL	EQM1 to be reused in AVM
FM	2	C/D	complete acceptance tests at board level	integrated in FGS PFM model
FS	1	C/D	limited acceptance tests at board level	

5.3 Verification and tests

The various models, foreseen by the model philosophy described in paragraph 5.2, are subject to a series of tests at board and FCU unit level. Furthermore, the FCU will be tested in the instrument chain at PL level and at SC level. A summary of the tests is given in Table 2.

Table 2: Tests to be performed on the different F-DCU models.

Test description	EM	EQM	AVM	FM & FS
Interface Verification	Y	Y	Y	Y
Functional Tests		Y	Y	Y
Performance Verification		Y		Y
Physical & Mass Properties	Y	Y	Y	Y
Sine Vibration	Q	Q		A
Random Vibration	Q	Q		A
Shock	Q	Q		
Thermal Vacuum/Balance		Q		A
Electrical Interfaces		Y	Y	Y
Conducted Emissions		Y		Y
Radiated Emissions		Y		Y
Conducted Susceptibility		Y		Y
Radiated Susceptibility		Y		Y
ESD		Y		Y

Notes: Q is qualification level, A is acceptance level.

5.4 FPGA Development Plan

OHB-I will perform simulations of the FPGA code in order to obtain confidence that the VHDL design complies, under all conditions, the given performance and functional requirements. The worst conditions are considered taking into account all possible parameters, including environmental conditions (temperature range, TID) and power supply levels. Simulations are performed by means of a dedicated tool and validated test benches.

5.5 Analyses

As the design progresses, several types of analysis and mathematical models (FEM, TMM, etc.) must be provided as part of the accompanying documentation. A list of these is given in the following paragraphs with a description and an assessment of the maturity stage.

5.5.1 FEM

OHB-I provided a structural model and performed a FEM (Finite Element Method) analysis on the F-DCU board mechanical design. The F-DCU FEM model contributes as a subsystem to the FEM analysis at FCU box level (see Figure 10).

5.5.2 FMEA/FMECA

The Failure Modes Effects and Criticality Analysis has been performed according to the guidelines given in ECSSQ-ST-30-02C. The FMECA identifies all failures and modes of failure that can occur at F-DCU level and shall be used as input for higher level analysis at FCU level.

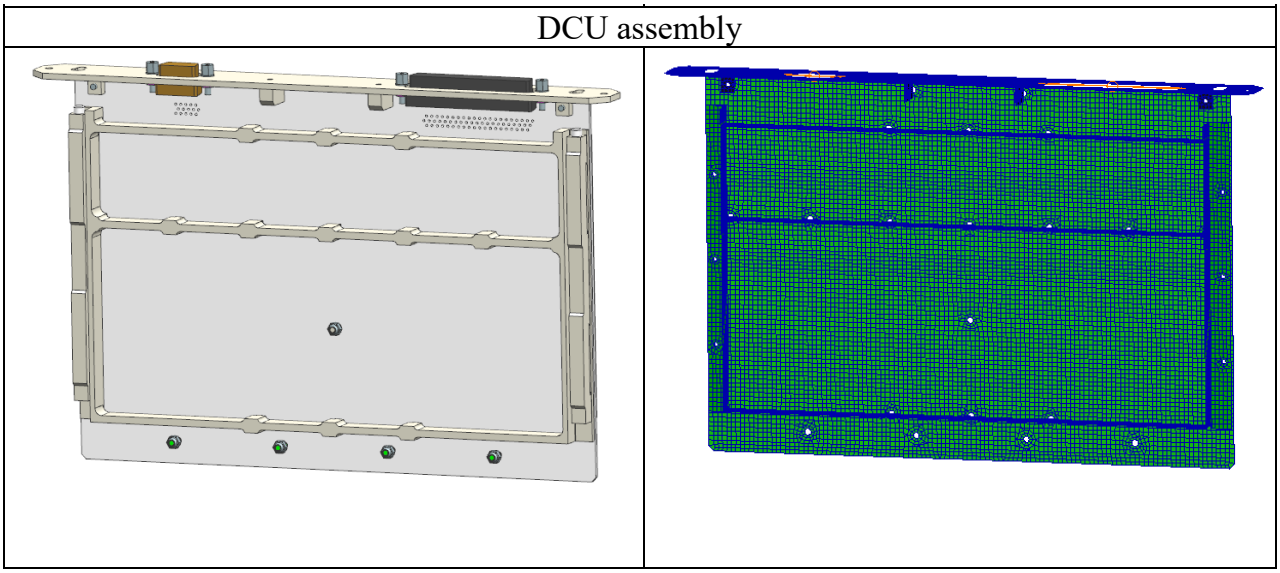


Figure 10: An image of the F-DCU FEM.

5.5.3 WCA

Worst case analysis (ECSS-Q-HB-30-01A) on the critical circuits (e.g. protection circuits) have been performed to proof that the design meets the required performance under worst conditions. The worst conditions are defined taking into account all possible parameters, including environmental conditions both during AIT activities and in-orbit (nominal duration + extended mission). The Monte Carlo and RSS (Root Sum Squared) methods are used for the F-DCU worst case analysis. The WCA have been performed using the Cadence PSPICE simulator. The parameters degradation used in the WCA are here below listed:

- Initial tolerance;
- Temperature drift, assuming a maximum temperature on the PCB board of 82.15 $°C$;
- Ageing, considering an in-orbit lifetime of 6.25 yrs;
- Radiation, with a TID (Total Integrated Dose) inside the FCU box = 7.8 krad.

The WCA results show that the outcoming values are compliant with the required limits.

5.5.4 PSA

This analysis aims to verify the respect of the ECSS (ECSS-Q-ST-30-11C) derating rules of all the EEE parts used on the F-DCU board. No noncompliances have been found during the analysis.

5.5.5 Thermal analysis

Two different types of materials have been considered in the TMM (Thermal Mathematical Model):

1. Metallic structures, all in Aluminium type 6082 (thermal conductivity: 170 $W/m \cdot K$);
2. The PCB (12 layers) that is composed, in turn, of dielectric and conductive layers and of electronic components:
   - Polyimide ARLON 35N (150 µm thick);
   - Copper (17 µm thick);
   - Only critical electronic components (2 nodes models) were considered.

The equivalent in-plane thermal conductivity of the PCB resulted: 14.79 $W/m \cdot K$. The thermal analysis show that in both Acceptance and Qualification cases there is a positive margin in terms of maximum temperatures that can be reached, also because about half of the heat is rejected by radiation to the environment. This contributes to keep all the boards and components at a sufficiently low temperature.

6. SUMMARY AND CONCLUSIONS

ARIEL payload and its subsystems will face the PDR (Preliminary Design Review) in the second half of this year (2022).

The detailed design of the F-DCU board is consolidated and its mechanical dimensions with respect the FCU enclosure are defined. Due to the maturity of the project several representative analyses (electrical, structural-FEM and thermal) have already been performed.

After the MRR (Manufacturing Readiness Review), to be held in autumn, OHB Italy will begin the construction of the first three EM (Engineering Model) boards.

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