OPTIMIZACIJA PARAMETARA SINTEROVANJA DEBELOSLOJNIH OTPORNIKA NA BAZI $Bi_2Ru_2O_7$ SLOJNE OTPORNOSTI 10 kΩ/sq

OPTIMIZATION OF 10 kΩ/sq $Bi_2Ru_2O_7$ THICK-FILM RESISTORS SINTERING PARAMETERS

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Development of new and improvement of existing energy-saving electronic components are supporting transition from traditional to renewable energy sources and contributing to energy efficiency. Thick- film resistors are passive components that are often being used in energy-saving smart home appliances, LED lighting, air conditioning management, electric scooters, battery management systems etc. For these reasons, this paper will deal with optimization of 10 kΩ/sq $Bi_2Ru_2O_7$ thick-film resistors sintering parameters.

Key words: *energy efficiency; thick-film resistors; sintering parameters*

Razvoj novih i unapređenje postojećih elektronskih komponenti koje doprinose smanjenju potrošnje električne energije pogoduju prelasku sa tradicionalnih na obnovljive izvore energije i doprinose energetskoj efikasnosti. Debeloslojni otpornici su pasivne komponente koje se sve više koriste u pametnim energetski štedljivim kućnim uređjima, LED osvetljenju, upravljanju klima uređajima, električnim trotinetima, sistemima za upravljanje baterijama itd. Zbog toga će u ovom radu biti reči o uticaju parametara sinterovanja na formiranje strukture najčešće korišćenih debeloslojnih otpornika na bazi $Bi_2Ru_2O_7$ slojne otpornosti 10 kΩ/□.

Ključne reči: *energetska efikasnost; debeloslojni otpornici; parametri sinterovanja*

1 Introduction

Having in mind the current global energy demand, saving energy through innovation and technology is a promising concept for years to come. Energy efficiency has increased considerably over the past few decades as a response to energy price increases, government policies regarding the environmental impact of CO_2 emissions and technology improvements. Nowadays, the world is facing dramatic increase in energy prices because of the concern for the general energy security. Governments are encouraging the use of renewable energy systems because these systems are sustainable and can be used locally.

Development of new energy-saving electronic components and improvement of existing ones are contributing to energy efficiency and supporting the transition from traditional to renewable energy sources [1-3]. Passive components that are often being used in energy-saving smart home appliances, LED lighting, air conditioning management, electric vehicles, battery management systems etc. are thick-film resistors. Their excellent performances, laser trim stability, power handling, overall reliability and cost advantages justify their use in energy-saving devices. The key process responsible for formation and performances of these complex structures is the sintering process. For these reasons, this paper will deal with optimization of sintering parameters for 10 kΩ/sq $Bi_2Ru_2O_7$ thick-film resistors.

2 Experimental

In order to optimize thick resistive film sintering parameters, several groups of thick-film resistors of identical sheet resistances (10 kΩ/sq) and geometries (resistor length: 21 mm; width: 3 mm) were realized and exposed to different sintering conditions (Figure 1).

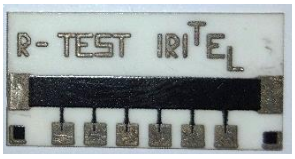

Figure 1. 10 kΩ/sq thick-film resistors used in the experiment

Test samples used in the experiment were screen-printed on pure alumina (96% Al_2O_3) substrates using commercially available $Bi_2Ru_2O_7$ resistor composition. Contact pads were formed using Pd/Ag conductor composition. The major thick resistive film screen printing and drying parameters are given in Table 1.

Table 1. Processing parameters prior to sintering

Stainless steel mash count	200	Dry layer thickness	25 μm
Emulsion thickness	10-12 μm	Levelling	15 min/21 °C
Wet layer thickness	36-38 μm	Infrared drying cycle	10 min/150 °C

For experimental purposes five different sintering profiles were chosen. Primary 60 min sintering profile with peak temperature of 850 °C and 10 min dwelling time, recommended by the composition manufacturer [4], was used as a referent one. For the referent profile, sintering phases and processes are given in table 2. Two additional sintering profiles with lower (825 °C) and higher peak (875 °C) temperatures were examined in combination with 10 min dwelling time, as well as two profiles with two different dwelling times of 5 min and 15 min at peak temperature of 850 °C.

Table 2. Primary sintering profile

Sintering phase	**Temperature**	**Process**
Rise to peak temperature	400 - 500 °C	Burnout of the organic constituents in the film
Rise to peak temperature	500 - 850 °C	Borosilicate glass melting
Dwelling at the peak temperature	850 °C	Thick resistive film structure formation
Fall from the peak temperature	850 - 400 °C	Glass solidification phase
Fall from the peak temperature	< 400 °C	Relaxation of the thick resistive film

For all chosen sintering profiles sufficient time was allowed for the belt furnace to reach and stabilize pre-set temperatures in all 9 temperature zones in order to achieve desired sintering profile. To maintain the equilibrium conditions, the belt was uniformly loaded at all times during the sintering process, the sample transit rate was uniform and the sintering profile was checked using control thermocouples attached to the dummy loads. The measured stabilized primary sintering profile is given in Figure 2.

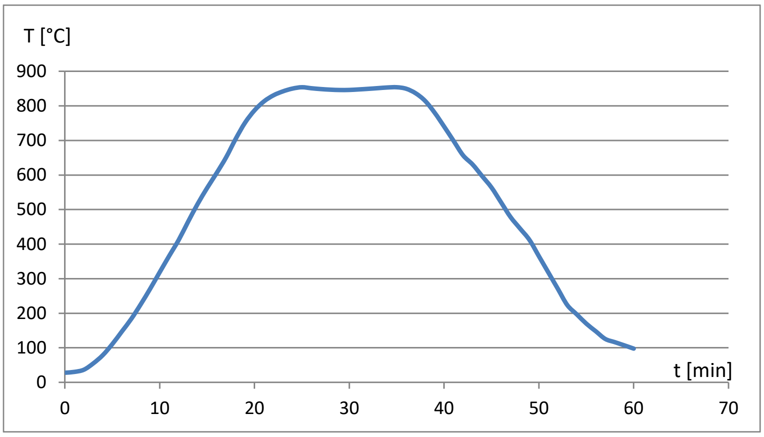

Figure 2. The primary sintering profile recorded using the control thermocouple.

3 Results and discussion

When recommended peak temperature of 850 ºC with 10 min dwelling time is in question, main requirements for successful structure formation were met and measured resistance values were used as the reference values. During the sintering process, spatially uneven insulating and conductive phase distribution occurred resulting in formation of conductive network that consists of multiple conducting chains and glass areas. Therefore, conducting mechanisms present in 10 kΩ/sq resistors are tunnelling through glass barriers present between some of the neighboring conducting particles and metallic conduction through clusters of conductive particles and sintered contacts between them [5].

Sintering profile with peak temperature of 825 ºC resulted in thick-film resistors with resistances slightly lower than the reference one. For samples with reference value of 16.7 kΩ/sq, lower peak temperature resulted in -3% resistance change. This means that conducting phase did not achieve complete immersion in the insulating glass matrix and a greater number of conducting chains was formed allowing direct conduction or tunnelling through thin glass barriers.

Sintering profile with peak temperature of 875 ºC resulted in thick-film resistors with resistances slightly higher than the reference one. The change in the resistance value was +3%. Due to the higher peak temperature glass viscosity was reduced causing the greater immersion of conducting particles into the glass matrix. Because of the increased number of glass barriers that formed between adjacent conducting particles the number of conducting chains in the conductive network was reduced.

Effect of peak temperature on resistance of 10kOhm/sq thick resistive film is shown in Figure 3.

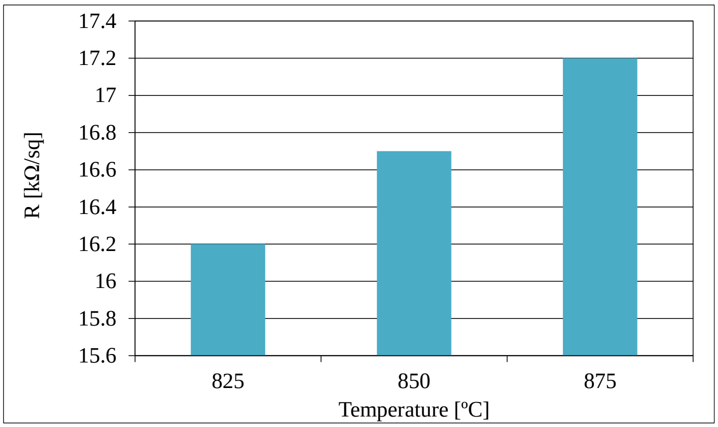

Figure 3. Resistivities of 10 kΩ/sq thick resistive films sintered at peak temperatures of 825 ºC, 850 ºC and 875 ºC. for 10 min.

Variations in dwelling time had similar effect (Figure 4). For all examined test samples dwelling time of 5 min at the recommended peak temperature of 850 ºC was insufficient to allow optimum immersion of the conducting phase in the insulating glass matrix. For samples with reference value of 5.5 kΩ/sq, shorter dwelling time resulted in -9 % resistance change because a greater number of conducting chains was formed allowing direct conduction or/and tunnelling through thin glass barriers.

Longer dwelling time (15 min) allowed further spatial distribution of the conducting phase within the glass matrix and resulted in reduced number of conducting chains in the matrix due to thicker glass barriers between adjacent conducting particles. For samples with reference value of 5.5 kΩ/sq, longer dwelling time resulted in +3.6 % resistance change.

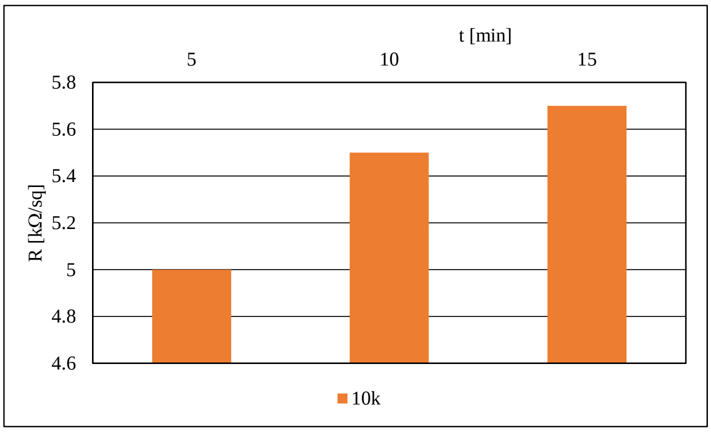

Figure 4. Resistivities of 10 kΩ/sq thick resistive films sintered at the peak temperature of 850 ºC for 5 min, 10 min and 15 min.

4 Conclusion

Test resistors of 10 kΩ/sq sheet resistivity were sintered at three different peak temperatures (825 ºC, 850 ºC and 875 ºC) with 10 min dwelling time and with three different dwelling times (5 min, 10 min and 15 min) at peak temperature of 850 ºC to examine influence of sintering parameters on structure-related changes in resistance.

Peak firing temperature of 850 ºC with 10 min dwelling time is the sintering profile recommended by the composition manufacturer and measured resistance values were used as reference ones.

It was observed that resistance increases with both increase in peak temperatures and in dwelling times due to the thick resistive film microstructure evolution during the high-temperature treatment. The reduction of glass phase viscosity with the increase in temperature or dwelling time led to greater immersion of conducting phase in to the glass matrix thus reducing the number of conducting chains and increasing the number of glass barriers that take part in the tunneling conduction.

Observed effects can be used in defining optimum sintering profiles when fine tuning of resistance values is necessary. Slight decrease or increase in resistance (up to a few percent) can be achieved by decrease or increase in peak temperature or dwelling time. This is of the greatest importance in cases when trimming process is not available because of the resistor size and/or position, especially in cases when buried resistors are being incorporated in thick- film multilayer structures.

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5 References

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