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# Arm current reversal-based modular multilevel DC-DC converter

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**Abstract**

Nowadays, most of the converters used in high-power high-voltage (HV) applications are the conventional modular multilevel converters (MMC). However, in the case of DC-DC conversion, an imbalance of the capacitor voltages occurs and the conventional MMC fails to operate correctly. This paper introduces an arm current reversal-based modular multilevel DC-DC converter, which successfully provides balance among the capacitor voltages while operating in DC-DC conversion. The proposed configuration is used in medium voltage DC grids to feed DC loads or to interconnect between two DC grids of different voltage levels. The proposed converter is a two-stage DC-DC modular converter, which consists of a single-phase half-bridge MMC with half-bridge submodules (HBMMC) followed by a single-phase H-bridge MMC with half-bridge submodules (SMs). The operational concept of the proposed converter is based on reversing the arm current direction and reversing the output terminals with the help of the H-bridge MMC stage, which ensures the same direction of the voltage at the load terminals. The proposed converter provides a high conversion ratio, bidirectional power flow, simple architecture, and a simple control scheme. Detailed illustrations, analysis, and design of the proposed converter are presented. Besides, MATLAB-based and Opal RT-based simulation results and experimental results are presented to validate the proposed configuration claims.

## 1 | INTRODUCTION

The modular multilevel converter (MMC) has shown promising potential in HV high-power applications due to its astonishing benefits, which include redundancy, modularity, and scalability [1–4]. Each leg in the conventional MMC comprises two arms, where each arm consists of series-connected submodules (SMs). The most common SM used is the half-bridge SM (HBSM), which consists of two IGBTs and a DC capacitor. The HBSMs can output zero or positive voltages according to the IGBTs gating signals. There is also a full-bridge SM (FBSM) that can output zero, positive, and negative voltages. The main issue of the conventional MMC is operating with balanced and bounded capacitors voltages, which is inherently guaranteed in the case of DC-AC operation with relatively high output frequency thanks to the bipolar arm currents. Operating with bipolar arm currents allows periodic charging and discharging of the SMs capacitors. The corresponding voltage ripples of the capacitors increase when the output current rises and/or the output frequency decreases [5, 6]. Hence in low-frequency applications, the capacitors suffer from high-ripple voltage unless hardware/software solutions have been added to the converter or even bulky capacitors have been used. In the case of the DC-DC conversion process, energy drift occurs between the upper and lower arms of the conventional MMC due to the unipolar arm currents, which results in operating with unbalanced capacitor voltages [7].

In the literature, different approaches based on hardware/software modifications have been presented to overcome the capacitor voltage imbalance issue during the DC-DC conversion process. One of the software-based approaches is the injection of the AC circulating current to the conventional MMC, where it allows charging and discharging of the arm capacitors. Hence, a successful DC-DC conversion is achieved. However, an optimization technique should be applied on the injecting current as presented in [8], because high circulating current leads to excessive current stresses on the involved IGBTs in addition to higher operational losses, which decreases the converter efficiency. On the other hand, special HBSMs-based modular DC-DC converter topologies with

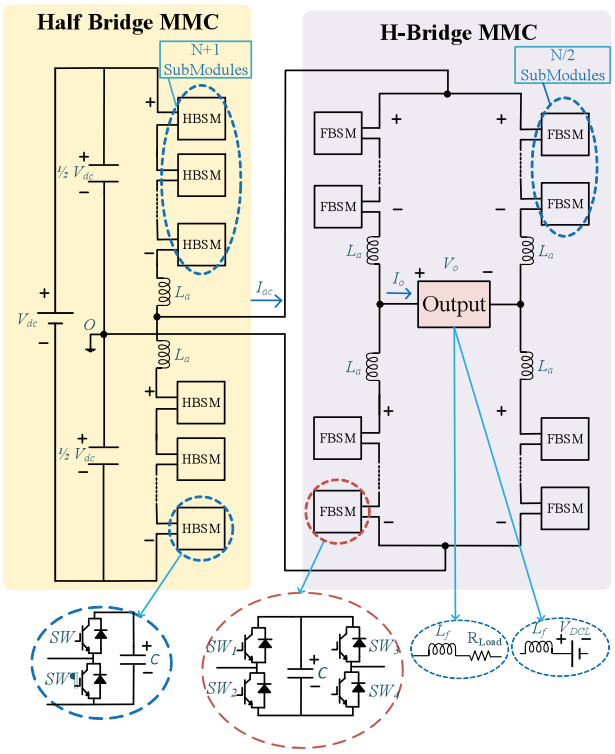


**FIGURE 1** The architecture of the existing DC-DC converter presented in [21]

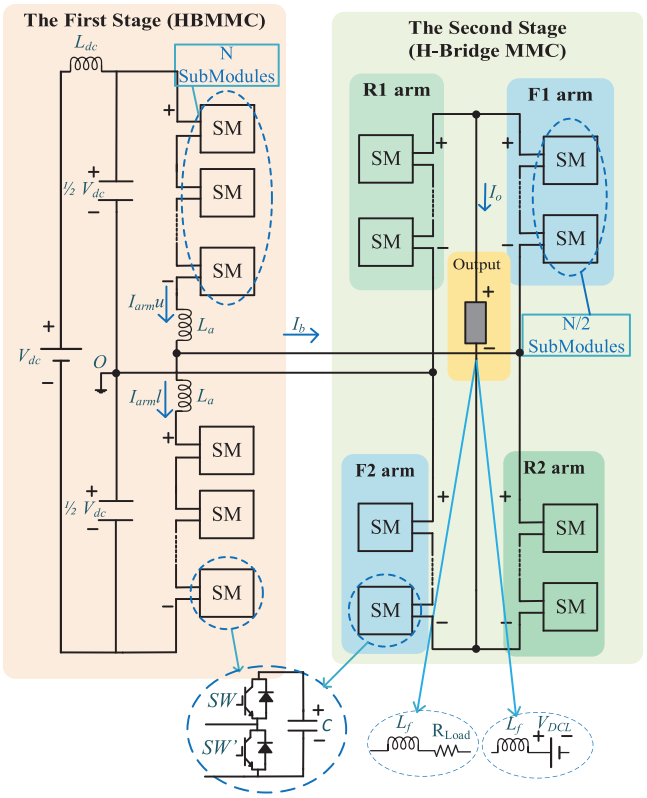


**FIGURE 2** The architecture of the proposed DC-DC converter

cross-connected capacitances [9] and cross-connected arms [10] were presented in the literature. In these topologies, to ensure the operation with balanced capacitor voltages, an AC voltage injection is used. The number of switches in these configurations is relatively high. A similar concept with HBSMs as well as FBSMs has been proposed for bipolar DC systems in [11]. Some researchers suggested employing the conventional MMC in DC-DC operation with an additional hardware circuit, which is named energy equalizing modules (EEMs) [12–16]. The EEMs ensure arms energy balance where balanced capacitor voltages are achieved. Using EEMs needs many semiconductor devices, EEMs controllers, and transformers, which increases system complexity and cost. Alternatively, hybrid modular DC-DC converters that use high-voltage valve(s) in addition to HBSMs and/or FBSMs are proposed in the literature [17–20]. The high-voltage valve in these converters consists of a series-connection of IGBTs and is operated under zero-voltage switching.

Recently, a modular DC-DC converter, which is based on the arm interchange concept, was proposed in the literature [21], where the upper and lower arms are exchanging their positions during operation to ensure balanced capacitor voltages in DC-DC conversion. This presented topology is comprised of a two-stage modular DC-DC converter. The first stage consists of a half-bridge single phase MMC with HBSMs while the second stage consists of an H-bridge single phase MMC with FBSMs as shown in Figure 1. Therefore, it has a relatively complex architecture and control scheme.

In this paper, an arm current reversal-based modular DC-DC converter is presented, which successfully achieves balanced capacitor voltages in DC-DC conversion. The proposed topology consists of a two-stage modular DC-DC converter. The first stage is a half-bridge single-phase HBSM-based MMC (HBMMC), while the second stage is an H-bridge single-phase HBSM-based MMC. The first stage generates the required output voltage, but only in half of a predetermined periodic time and its negative value in the other half. The capacitors are charging in only half of the periodic time and are discharging in the other half, because the arm current is reversed, that is, operating with bipolar arm currents. The second stage is the rectification stage, where it is controlled, such that its output is the required DC voltage for the whole period. Hence, a successful DC-DC conversion with balanced capacitor voltages is achieved by employing the proposed arm current reversal concept. The proposed DC-DC converter shown in Figure 2 may fit in medium-voltage medium power applications as single leg-based MMC with relatively bulky DC-link capacitances is employed, where the size of capacitors increases with the increase of converter power rating. For the proposed converter to be used in high voltage high power applications, the first stage is replaced by an H-bridge MMC instead of the half-bridge MMC as shown in Figure 3.

The detailed operational concept of the arm current reversal-based modular DC-DC converter is presented along with capacitor voltage ripples analysis and passive components design. To clarify the proposed approach's pros and cons, a comparison has been made between the proposed topology and other different topologies of modular DC-DC converters in the literature.

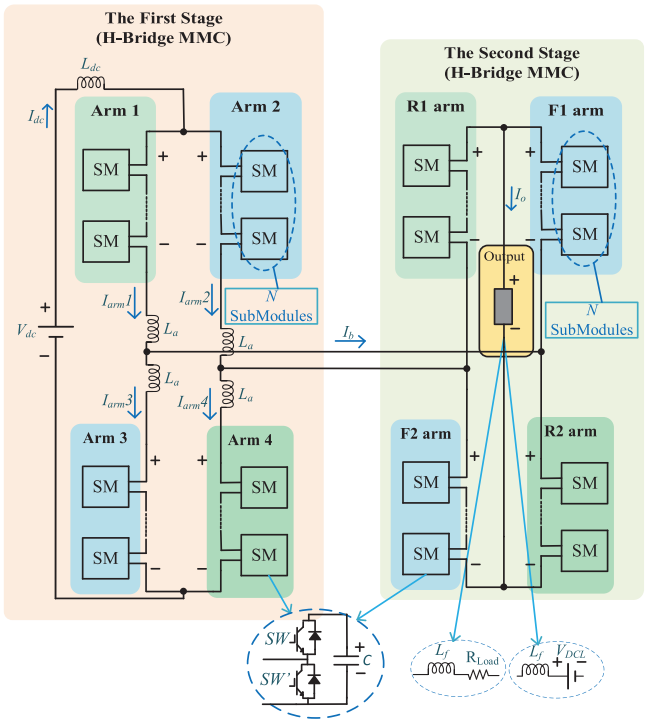


**FIGURE 3** The architecture of the proposed DC-DC in high voltage high power applications

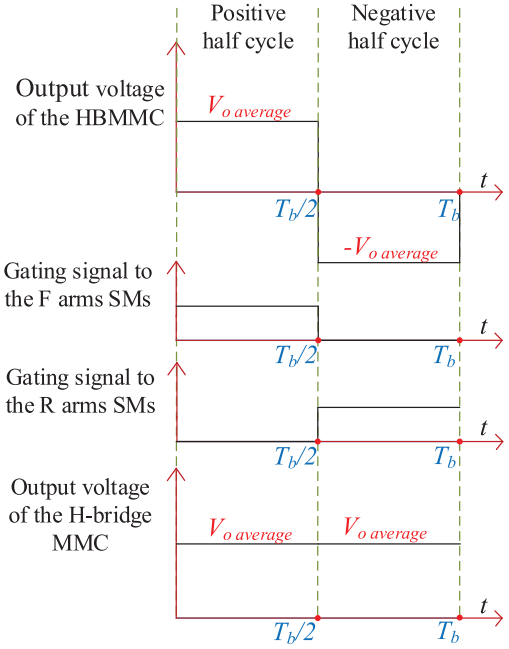


**FIGURE 4** The operational concept of the proposed MMC

Finally, to validate the proposed approach, simulation, as well as experimental results, are demonstrated achieving successful DC-DC conversion with balanced capacitor voltages.

The main contributions of the presented approach can be summarized as follows.

- The arm current reversal-based modular DC-DC converter is proposed where a successful DC-DC operation with balanced capacitor voltages has been realized.
- The proposed configuration provides a bidirectional power flow, high conversion ratio, low current stresses, low number of IGBTs, simple architecture, and simple control scheme.

## 2 | THE PROPOSED CONFIGURATION

To overcome the challenge of the SMs capacitor voltages unbalances in conventional MMCs in the case of DC-DC operation, a new arm current reversal-based modular multilevel DC-DC converter is proposed. In the proposed configuration, there is no need for injecting high AC circulating current nor using special modular topologies.

The main concept of this configuration is the inversion of the arm current direction while keeping the output current unchanged.

The proposed configuration is a two-stage modular DC-DC converter, which comprises a half-bridge single-phase MMC with half-bridge SMs (HBSMs) followed by an H-bridge single-phase MMC with HBSMs connected to its output as illustrated in Figure 2. In the first stage, the output voltage of the HBMMC is controlled, such that it generates the desired output voltage ($V_o$) only in half of a predetermined periodic swapping time ($T_b$), which can be named, the positive half cycle. While the HBMMC generates the negative value of the desired output voltage ($-V_o$) in the other half, which can be named, the negative half cycle. In the second stage, in the positive half cycle, the SMs of the H-bridge arms F1 and F2 will be deactivated, which acts as a short circuit, while the other arms R1 and R2 will have their SMs activated. Alternatively, in the negative half cycle, the situation is reversed, where the two arms' SMs R1 and R2 will be deactivated, while the arms F1 and F2 will have their SMs turned on producing the same desired output voltage during the whole period as shown in Figure 4.

In other words, as seen in Figure 5, in the positive half cycle, the number of activated SMs in the lower arm of HBMMC is larger than that of the upper arm hence, the lower SMs capacitors are discharging, while the upper SMs capacitors are charging. Nevertheless, in the negative half cycle, the number of activated SMs in the upper arm is larger than that of the lower arm leading to the arm currents reversal, so the upper SMs capacitors are discharging while the lower SMs capacitors are charging. However, the same output DC voltage is maintained in the whole period thanks to the H-bridge MMC. By continuous swapping between the positive and negative cycles with proper swapping periodic time ($T_b$), low ripple voltage in the capacitors is achieved.

It has to be noted that the number of submodules in each arm of the HBMMC stage is $N$, while the number of submodules in each arm of the H-bridge MMC is $N/2$, where the output voltage of the HBMMC ranges from $-V_{dc}/2$ to $V_{dc}/2$. Any modulation technique can be used to extract the number of SMs to be activated in each arm for the given arm reference voltages. In this paper, the employed modulation technique is

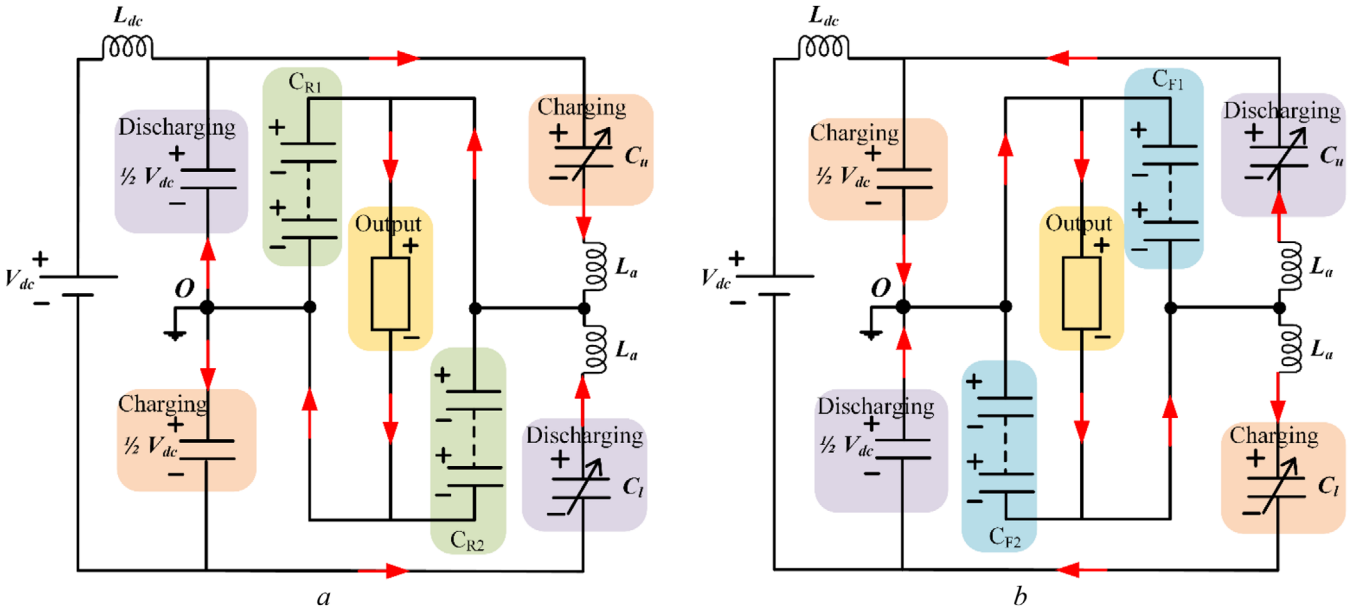


**FIGURE 5** The proposed modular DC-DC converter. (a) The operation in the positive half cycle where the number of activated SMs in lower arm is greater than that of the upper arm, (b) the operation in the negative half cycle where the number of activated SMs in upper arm is greater than that of the lower arm

the phase-shifted carrier PWM (PSC-PWM) where it results in evenly distributed stresses on the involved switches [22] and a conventional voltage-balancing algorithm is applied [23]. It is worth noting that the voltage conversion ratio ($V_o/V_i$) of the proposed DC-DC converter ranges from 0.5 down to 0 without any restrictions, it is simply changed by modifying the reference output voltage.

## 3 | MATHEMATICAL ANALYSIS

### 3.1 | Modelling

The simplified MMC model with equivalent capacitors presented in [24] is used in this work to study the dynamic performance of the proposed modular multilevel DC-DC converter. The equivalent circuit of the proposed approach is shown in Figure 6. This simplified model replaces the series-connected submodules with an equivalent capacitor, whose capacitance depends on the number of connected submodules. The $C_u$ and $C_l$ in Figure 6 represent the equivalent capacitances in the upper and lower arms respectively, which are defined in Equations (1) and (2), where $C$ is the nominal capacitance of the SMs capacitors in the HBMMC, while $u$ and $l$ are the number of activated submodules in the upper and lower arms respectively.

$$C_u = \frac{C}{u} \tag{1}$$

$$C_l = \frac{C}{l} \tag{2}$$

The number of activated SMs in the upper and lower arms of HBMMC is defined in Equations (3) and (4) respectively as a function of the output voltage modulating signal ($v_m$), which is

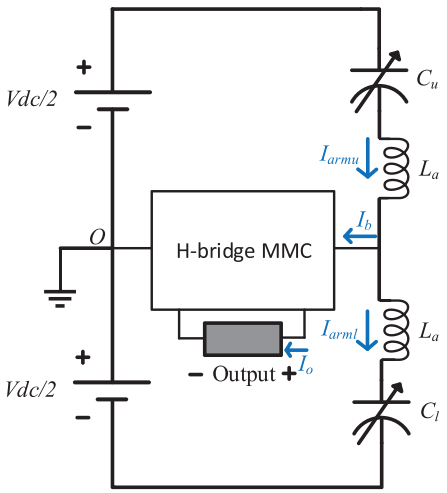


**FIGURE 6** A simplified model of the proposed architecture with the equivalent capacitors

the reference signal that ranges in the interval [-1, 1].

$$u = N\frac{1 - v_m}{2} \tag{3}$$

$$l = N\frac{1 + v_m}{2} \tag{4}$$

Based on Figure 6, assuming no arm inductance ($L_a = 0$), the upper and lower arm currents are given by;

$$I_{armu} = I_b \frac{C_u}{C_u + C_l} = I_b \frac{l}{u + l} = I_b \frac{l}{N} \tag{5}$$

$$I_{arml} = -I_b \frac{C_l}{C_u + C_l} = -I_b \frac{u}{u + l} = -I_b \frac{u}{N} \tag{6}$$

where ($I_b$) is the output current of the HBMMC stage, substituting Equations (3) and (4) into Equations (5) and (6), the arm currents will be

$$I_{armu} = I_b \frac{1 + v_m}{2} \tag{7}$$

$$I_{arml} = -I_b \frac{1 - v_m}{2} \tag{8}$$

The modulating signal ($v_m$) in the proposed DC-DC converter is defined by;

$$v_m = \begin{cases} \frac{V_o}{V_{dc}/2}, & 0 < t < \frac{T_b}{2} \\ -\frac{V_o}{V_{dc}/2}, & \frac{T_b}{2} < t < T_b \end{cases} \tag{9}$$

where $V_o$ is the desired DC output voltage level.

## 3.2 | HBMMC capacitor voltage ripple calculation

The change in the voltage of each submodule capacitor in the upper and lower arms of HBMMC is given by;

$$\Delta V_{cu} = \frac{1}{C} \int_0^t I_{armu} \times \left(\frac{u}{N}\right) dt \tag{10}$$

$$\Delta V_{cl} = \frac{1}{C} \int_0^t I_{arml} \times \left(\frac{l}{N}\right) dt \tag{11}$$

By substituting Equations (7) and (8) into Equations (10) and (11), the change in the capacitor voltage in upper and lower arms are expressed by Equations (12) and (13) respectively.

$$\Delta V_{cu} = \frac{1}{C} \int_0^t I_b \frac{1 + v_m}{2} \times \frac{1 - v_m}{2} dt \tag{12}$$

$$\Delta V_{cl} = -\frac{1}{C} \int_0^t I_b \frac{1 - v_m}{2} \times \frac{1 + v_m}{2} dt \tag{13}$$

Taking into consideration that ($v_m$) is a DC value in both halves of the periodic time, then the change in the upper and lower capacitor voltages can be calculated as follows.

$$\Delta V_{cu}(t) = \frac{1}{C} \times I_b \frac{1 - {v_m}^2}{4} t \tag{14}$$

$$\Delta V_{cl}(t) = -\frac{1}{C} \times I_b \frac{1 - {v_m}^2}{4} t \tag{15}$$

Assuming a smoothing reactor (low-pass filter) is used at the load terminals, then the half-bridge MMC (HBMMC) output current ($I_b$) can be defined as

$$I_b(t) = \begin{cases} I_o, & 0 < t < \frac{T_b}{2} \\ -I_o, & \frac{T_b}{2} < t < T_b \end{cases} \tag{16}$$

where ($I_o$) is the DC load current.

Taking into consideration ($v_m$) mentioned in Equation (9), the corresponding change in the capacitor voltage in the upper arm is given by

$$\Delta V_{cu}(t) = \begin{cases} \frac{1}{C} \times I_o \frac{1 - \left(\frac{V_o}{V_{dc}/2}\right)^2}{4}(t), & 0 < t < \frac{T_b}{2} \\ -\frac{1}{C} \times I_o \frac{1 - \left(\frac{V_o}{V_{dc}/2}\right)^2}{4}\left(t - \frac{T_b}{2}\right), & \frac{T_b}{2} < t < T_b \end{cases} \tag{17}$$

Similarly, for the change in the lower arm capacitor voltages. Finally, the capacitor voltage ripple is given by:

$$V_{ripple} = \Delta V_{cu}\left(\frac{T_b}{2}\right) - \Delta V_{cu}(0) \tag{18}$$

$$V_{ripple} = \frac{1}{C} \times I_o \frac{1 - \left(\frac{V_o}{V_{dc}/2}\right)^2}{4}\left(\frac{T_b}{2}\right) \tag{19}$$

Based on Equation (19), it must be noted that the ripple voltage in the capacitors decreases with decreasing the swapping time ($T_b$) and/or decreasing the output current ($I_o$).

## 3.3 | DC-link capacitors voltage ripple calculation

By applying Fourier analysis for the bridge current $I_b(t)$ given by Equation (16), the fundamental component of the current $I_b(t)$ is given by:

$$I_{b1}(t) = \frac{4I_o}{\pi} \sin\left(\frac{2\pi}{T_b} t\right) \tag{20}$$

The fundamental component of the DC-link capacitor current ($I_{CF}$) is half of $I_{b1}(t)$.

$$I_{CF} = \frac{I_{b1}(t)}{2} = \frac{2I_o}{\pi} \sin\left(\frac{2\pi}{T_b} t\right) \tag{21}$$

The peak-to-peak voltage ripple of the DC-link capacitors due to the current $I_{CF}$, namely, $V_{r\,p\text{-}p}$ is given by Equations (22) and (23), where $I_{CF\,pk}$ and $X_c$ are the peak of the capacitor

fundamental current and fundamental capacitive reactance of DC-link capacitor respectively.

$$V_{r\,p-p} = 2\,I_{CF\,pk}\,X_c \tag{22}$$

$$V_{r\,p-p} = \frac{2I_oT_b}{\pi^2 C_s} \tag{23}$$

where $C_s$ is the capacitance of the DC-link capacitors. Since the converter output power ($P_o$) is equal to $V_o \times I_o$, the ripple voltage $V_{r\,p\text{-}p}$ can be written as a function of the converter output power as follows.

$$V_{r\,p-p} = \frac{2P_oT_b}{\pi^2 C_s V_o} \tag{24}$$

## 4 | ASSESSMENT OF THE PROPOSED DC-DC CONVERTER

### 4.1 | Losses calculations of the proposed converter

To estimate the losses in the proposed converter, both the conduction and the switching losses of both stages of the proposed converter should be calculated. Assume that each IGBT/diode has an on-state voltage ($V_{on}$) and on-state resistance ($R_{on}$). Also, each IGBT has a turning on time ($t_{on}$) and a turning off time ($t_{off}$).

Regarding the conduction losses of the first stage (HBMMC), by substituting Equations (16) and (9) in Equation (7), the upper arm current is given by:

$$I_{arm_u} = \begin{cases} I_o\dfrac{1+\frac{V_o}{V_{dc}/2}}{2}, & 0 < t < \dfrac{T_b}{2} \\ -I_o\dfrac{1-\frac{V_o}{V_{dc}/2}}{2}, & \dfrac{T_b}{2} < t < T_b \end{cases} \tag{25}$$

Then the conduction losses of each switch in the upper arm can be given by:

$$p_{c_{sw_u}} = \left(\left|I_{arm_{u_{1_{avg}}}}\right| + \left|I_{arm_{u_{2_{avg}}}}\right|\right) \times V_{on} + \left(I^2_{arm_{u_{1_{rms}}}} + I^2_{arm_{2_{rms}}}\right) \times R_{on} \tag{26}$$

where $|I_{arm_{u_{1_{avg}}}}|$ and $|I_{arm_{u_{2_{avg}}}}|$ are the absolutes of the average upper arm current in the first and second half-cycles, respectively, while $I_{arm_{u_{1_{rms}}}}$ and $I_{arm_{u_{2_{rms}}}}$ are the RMS values of the upper arm current in the first and second half-cycles, respectively. Since one semiconductor is conducting per SM at any instance and each arm consists of $N$ SMs, then the conduction losses of the first stage (HBMMC) can be estimated as follows;

$$p_{c_{HBMMC}} = \frac{NI_o}{2}\left(2V_{on} + I_o\left(1 + \left(\frac{V_o}{V_{dc}/2}\right)^2\right) \times R_{on}\right) \tag{27}$$

Alternatively, for calculation of the switching losses of the HBMMC stage, the switching losses of each IGBT can be calculated as follows;

$$P_{sw\,IGBT} = \frac{1}{4}\,\frac{V_{dc}}{N} \times I_o \times f_s \times \left(t_{on} + t_{off}\right) \tag{28}$$

Since there are two switches in each SM, if the current passes through the IGBT of one of the switches before the switching instance, then after it the current passes through the diode of the other switch and vice versa. Therefore, for switching losses calculations, only one IGBT per SM is considered. The switching losses of the HBMMC stage can be calculated as follows, taking into consideration that HBMMC consists of two arms and each arm comprises $N$ SMs

$$P_{sw\,HBMMC} = 0.5 \times V_{dc} \times I_o \times f_s \left(t_{on} + t_{off}\right) \tag{29}$$

On the other hand, regarding the conduction losses of the second stage (H-bridge MMC) and because the output current passes in each arm for only half of the periodic time, then the conduction losses of each switch can be calculated as follows:

$$p_{c_{sw}} = \frac{I_o}{2} \times V_{on} + \frac{I_o^2}{2} \times R_{on} \tag{30}$$

Since the second stage consists of four arms where each arm consists of $N/2$ SMs then the conduction losses of the second stage can be estimated as follows:

$$p_{c_{H-Bridge}} = NI_o\left(V_{on} + I_o \times R_{on}\right) \tag{31}$$

Regarding the switching losses of the H-bridge MMC, the switching losses of each IGBT can be given by;

$$P_{sw\,IGBT} = 0.5 \times \frac{V_o}{N/2} \times I_o \times f_b \left(t_{on} + t_{off}\right) \tag{32}$$

where $f_b$ is the switching frequency of the IGBT in the second stage that equals $(1/T_b)$. Therefore, the switching losses of the H-bridge stage can be calculated as follows;

$$P_{sw\,H-bridge} = 2 \times V_o \times I_o \times f_b \left(t_{on} + t_{off}\right) \tag{33}$$

### 4.2 | Numerical example

For the proposed DC-DC converter with $V_{dc}$ = 10 kV, $T_b$ = 0.01 s, $N$ = 4, and $V_o = 0.25 \times V_{dc}$ = 2.5 kV. Based on Equation (19), the capacitor voltage ripple of HBMMC capacitances is given by Equations (34) and (35). Figure 7 shows the corresponding 3D plot of the voltage ripple percentage of the HBMMC capacitors with the output current and the HBMMC

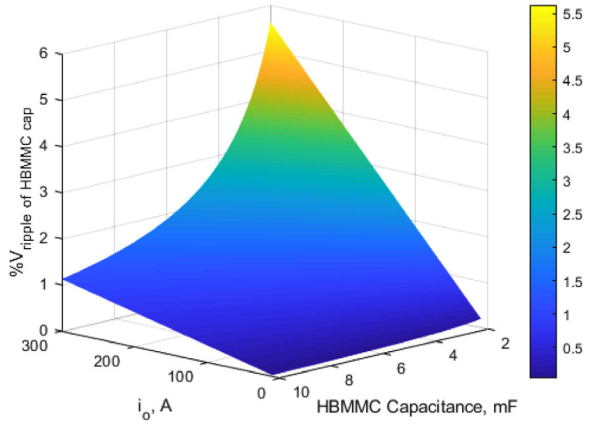


**FIGURE 7** 3D plotting of the HBMMC capacitor voltage ripple percentage with the output current and the HBMMC SMs capacitance for the given numerical example

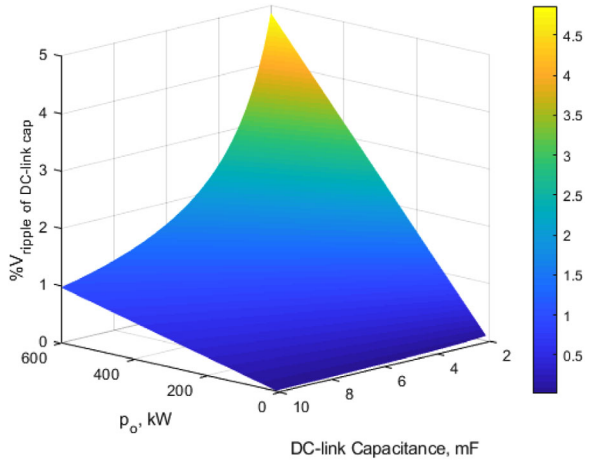


**FIGURE 8** 3D plot of the DC-link capacitors voltage ripple percentage versus the converter output power and the DC-link capacitance

SMs capacitance for the given numerical example.

$$V_{ripple} = \frac{9.375 \times 10^{-4} I_o}{C} \tag{34}$$

$$\% V_{ripple} = \frac{V_{ripple}}{(V_{dc}/N)} \times 100\% \tag{35}$$

Similarly, based on Equation (24), the DC-link capacitor voltage ripple is given by Equations (36) and (37), where Figure 8 shows the 3D plot of the percentage peak-to-peak voltage ripple of the DC-link capacitors versus the output power and the DC-link capacitance.

$$V_{r\,p-p} = \frac{0.81 \times 10^{-6} P_o}{C_s} \tag{36}$$

$$\% V_{r\,p-p} = \frac{V_{r\,p-p}}{(V_{dc}/2)} \times 100\% = \frac{1.62 \times 10^{-8} P_o}{C_s}\% \tag{37}$$

Assuming the proposed converter is delivering a power of 400 kW, where $V_{on} = 2$ V and $R_{on} = 1$ m$\Omega$, while the sum of $t_{on}$ and $t_{off}$ equals 1 $\mu$S, with a switching frequency of 2000 Hz, then the conduction and the switching losses of the first stage can be calculated according to Equations (27) and (29) to be 1.7 and 2 kW, respectively. Also, the conduction and the switching losses of the second stage are calculated according to Equations (31) and (32) to be 1.7 kW and 100 W respectively. Finally, the efficiency is found to be 98.9%.

The switching losses of the second stage MMC are very low due to the low switching frequency of the second stage.

### 4.3 | Limitations of the proposed converter

The limitations of the proposed topology are as follows:

- The output voltage of the proposed converter is limited to only half of the input voltage ($0.5 V_{dc}$).
- The power level of the proposed converter is limited by the size of required DC-link capacitors, as the capacitor size increases with the increase of the converter power level (i.e. bulky DC-link capacitors are needed in high power levels).

These limitations can be avoided by upgrading the converter to the H-bridge front-end converter (i.e. employing two legs instead of one leg HBMMC as a front-end converter) as seen in Figure 3.

### 4.4 | Comparison between the presented approach and other existing modular DC-DC approaches

In this subsection, a comparison has been held between the presented converter and other modular DC-DC converters that exist in the literature [9, 10, 21], assuming few MW power rating and 10 kV/2 kV conversion ratio as shown in Table 1.

Based on Table 1, the proposed converter and the converter presented in [21] have nearly the same concept. However, the proposed converter has a lower number of IGBTs and arm inductors, and a single type of SMs (only HBSMs) are used, hence more simple architecture and control scheme.

## 5 | DESIGN OF THE PRESENTED MODULAR DC-DC CONVERTER PARAMETERS

### 5.1 | SMs capacitance of the HBMMC

With the help of Equation (19), based on the desired SMs capacitor voltage ripple for the given output current level, dc-link voltage level ($V_{dc}$), and swapping time ($T_b$), the proper SM capacitance of the front-end HBMMC can be estimated.

**TABLE 1** Comparison between the presented converter and other modular DC-DC converters assuming a conversion ratio of 10 kV/2 kV

| Points of comparison | The proposed converter | Converter presented in [21] | Converter presented in [9] | Converter presented in [10] |
|---|---|---|---|---|
| **Types of SMs** | **HBSMs** | **HBSMs and FBSMs** | **HBSMs** | **HBSMs** |
| No. of SMs | 32 | HBSMs 18<br>FBSMs 16 | 40 | 60 |
| Voltage of SMs | 1.25 kV | 1.25 kV | 1 kV | 1 kV |
| No. of IGBTs | 64 (1.25 kV) | 100 (1.25 kV) | 80 (1 kV) | 120 (1 kV) |
| DC capacitors | 16 Caps (1.25 kV, pF range) + 16 Caps (1.25 kV, mF range) +2 Caps (5 kV, mF range) | 18 Caps (1.25 kV, $\mu$F range) + 16 Caps (1.25 kV, mF range) +2 Caps (5 kV, mF range) | 40 Caps (1 kV, mF range) | 60 Caps (1 kV, mF range) |
| AC capacitors | — | — | 2 Caps ($\mu$F range) | — |
| Arm inductors | 2 inductors ($\mu$H range) | 2 inductors (mH range), 4 inductors ($\mu$H range) | 8 inductors (mH range) | 8 inductors (mH range) |
| Output filters | $L_f$-filter (mH range) | $L_f$-filter (mH range) | — | — |
| Balancing method | Arm current reversal | Arm interchange concept | AC voltage injection | AC voltage injection |

**TABLE 2** Simulation parameters using MATLAB/SIMULINK software package and OPAL-RT

| Parameters | MATLAB/SIMULINK | OPAL-RT |
|---|---|---|
| $V_{dc}$ | 10 kV | |
| $L_{dc}$ | 10 mH, 0.1 Ω | |
| DC-link cap. | 5 mF | |
| SMs of MMC arm | 4 × 2.5 kV | |
| SMs of bridge arm | 2 × 2.5 kV | |
| MMC SMs Cap. | 5 mF | |
| Bridge SMs Cap. | 10 pF | |
| Inductance/arm | 0.01 mH, 0.1 Ω | |
| DC load | 10 Ω | |
| Low voltage side | 2 kV | |
| L-filter ($L_f$) | 30 mH | |
| Periodic time ($T_b$) | 0.01 s | |
| Switching freq. | 2 kHz | 500 Hz |

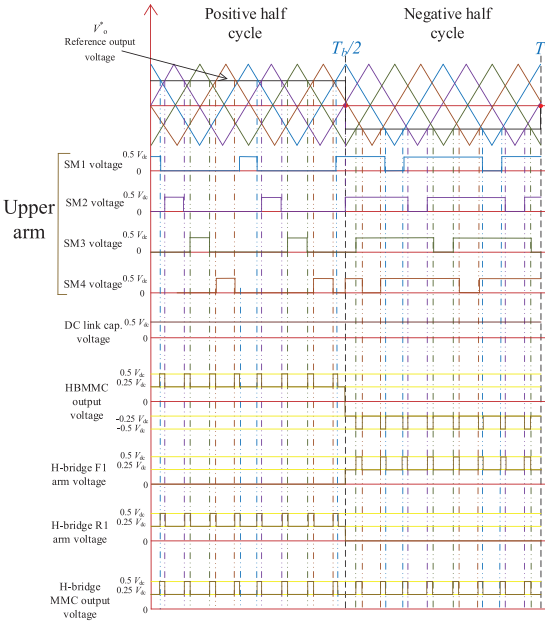


**FIGURE 9** Operational concept of the proposed arm current reversal-based converter

## 5.2 | DC-link capacitors ($C_s$)

With the help of Equation (24), based on the desired voltage ripple of the involved DC-link capacitors for the given output power level, output voltage level ($V_o$), and swapping time ($T_b$), the proper capacitance of DC-link capacitors of the front-end HBMMC can be estimated.

## 5.3 | Arm inductor ($L_a$)

The arm inductor is chosen to satisfy fast steady-state condition after switching from the positive half cycle to the negative half cycle and vice versa. To achieve that, the natural response's periodic time of the LC circuit of HBMMC should be kept much lower than half the swapping time ($T_b$) as in Equation (38).

$$\frac{T_b}{2} \gg 2\pi\sqrt{L_a \times \frac{C}{N}} \tag{38}$$

## 5.4 | Output L-filter ($L_f$)

An output L-filter is connected in series at the output terminals of the converter to ensure a smooth current. To have a smooth output DC current ($I_o$), the L-filter inductance is chosen, such

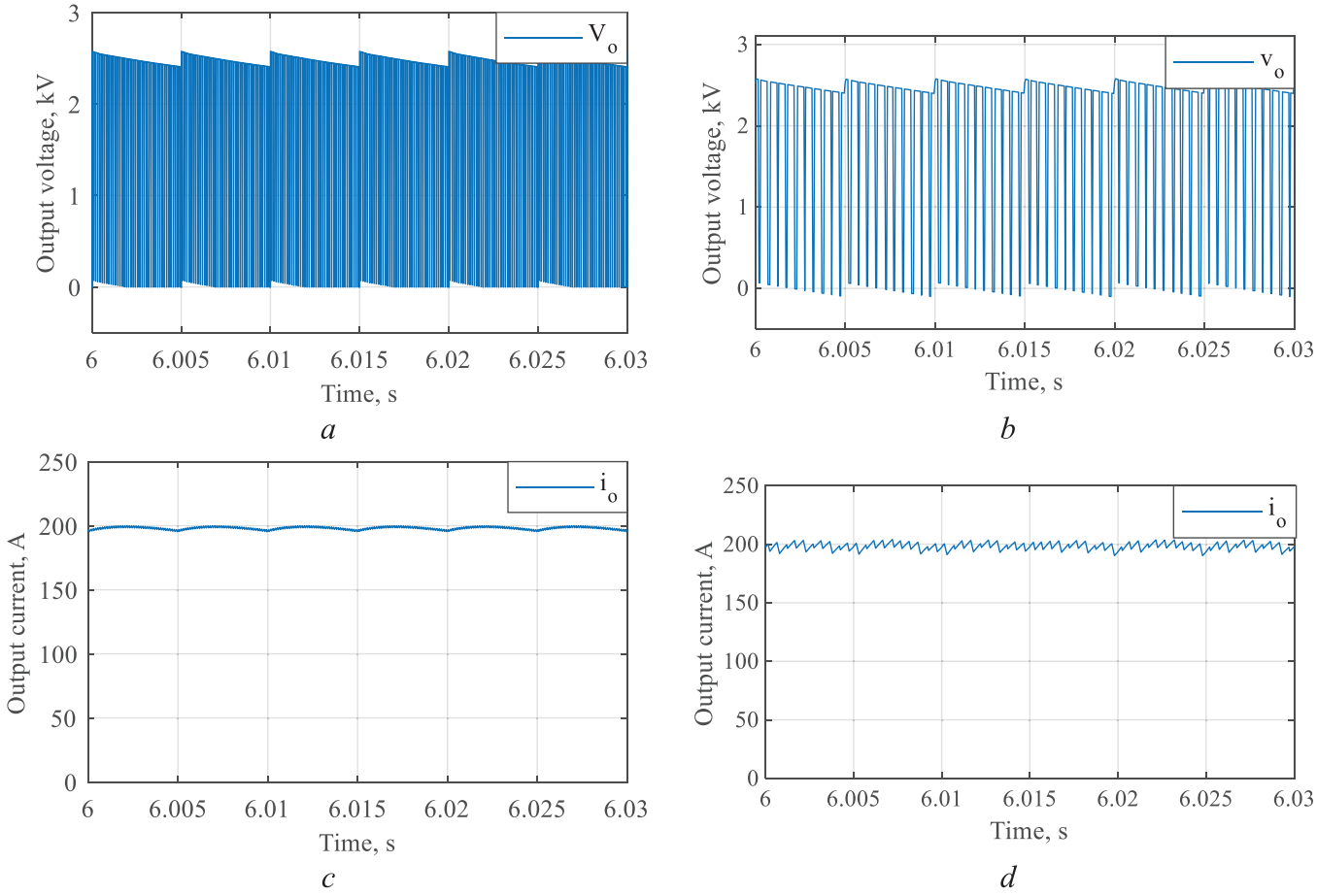


**FIGURE 10** Simulation results case: 1. (a), (b) are the output voltage in the case of MATLAB and OPAL-RT respectively, (c) and (d) are the load current in the case of MATLAB and OPAL-RT respectively

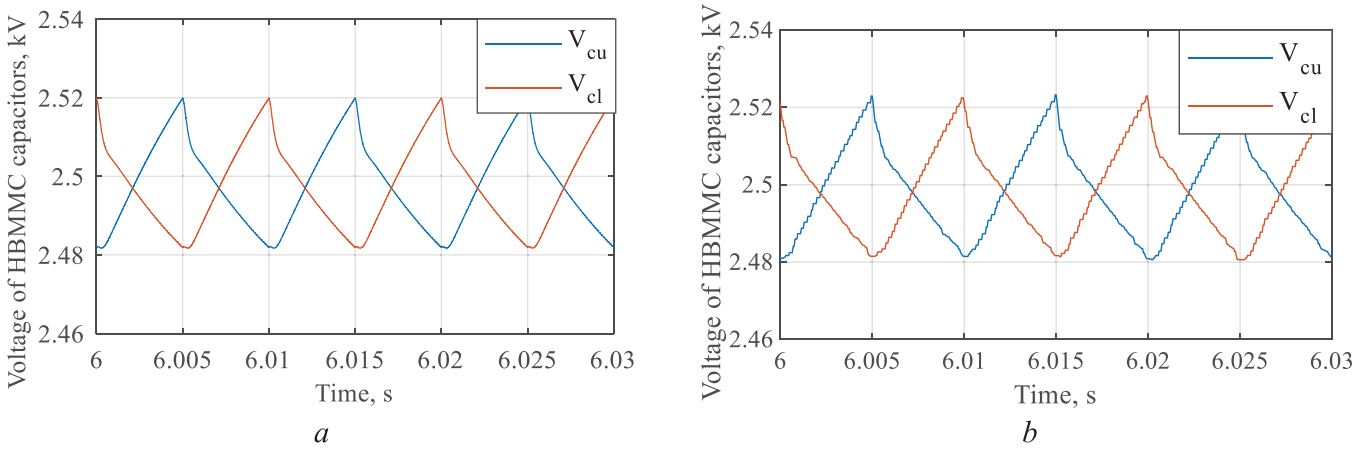


**FIGURE 11** Simulation results case: 1 (Cont.). (a) and (b) HBMMC SMs cap. voltages in the case of MATLAB and OPAL-RT respectively

that the ac component in the output current produced from the swapping frequency is attenuated. For example, if the low voltage side of the converter is a resistive load, then the L-filter inductance should be chosen, such that five times the time constant ($\tau$) is much greater than half the swapping time ($T_b$) as in Equation (39), where $\tau$ is defined as the filter inductance ($L_f$) divided by the load resistance ($R_{Load}$).

$$5\tau \gg \frac{T_b}{2} \rightarrow 5 \times \frac{L_f}{R_{Load}} \gg \frac{T_b}{2}$$

$$\rightarrow L_f \gg 0.1 \times T_b \times R_{Load} \tag{39}$$

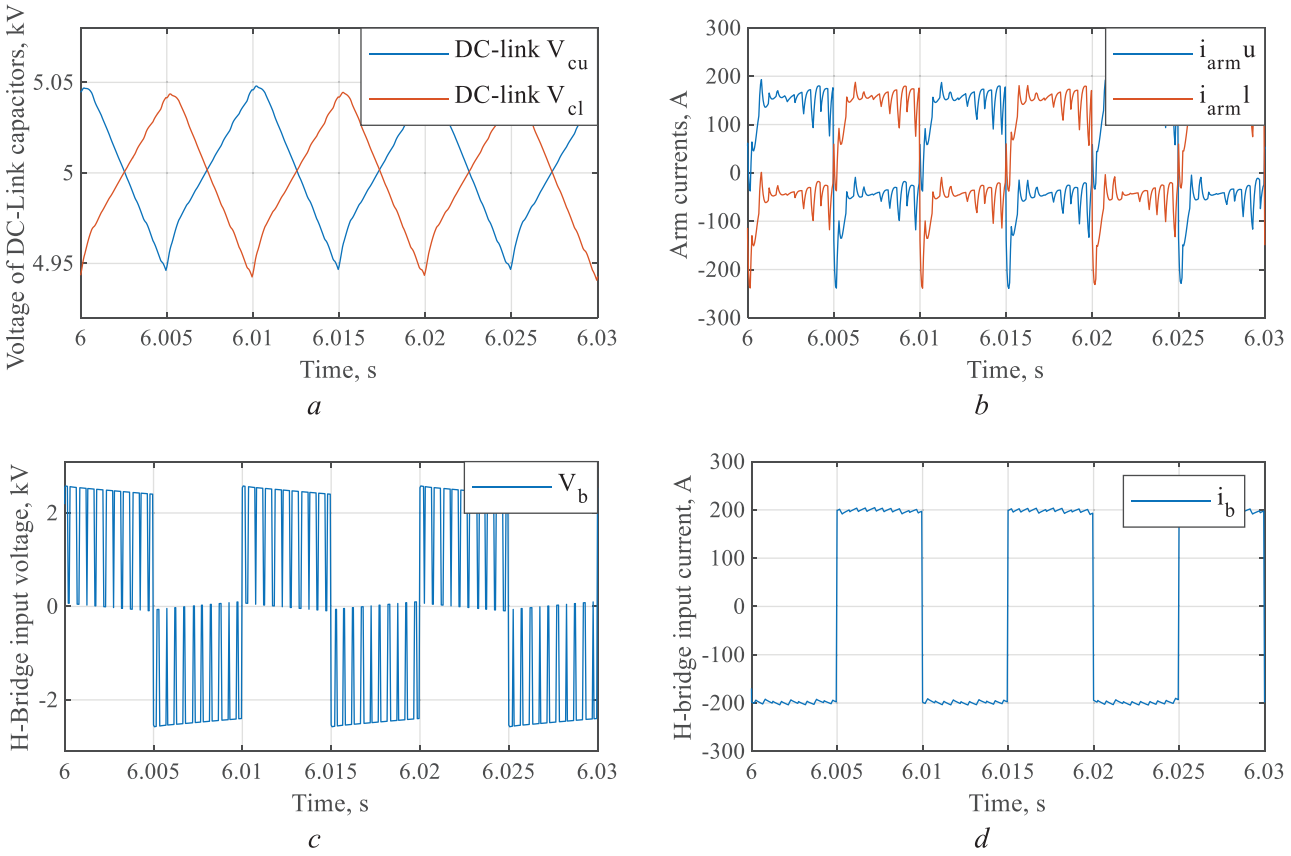


**FIGURE 12** OPAL-RT simulation results case: 1 (Cont.). (a) DC-link capacitor voltages, (b) HBMMC arm current, (c) H-bridge input voltage (output voltage of HBMMC stage), and (d) H-bridge input current (output current of the HBMMC stage)

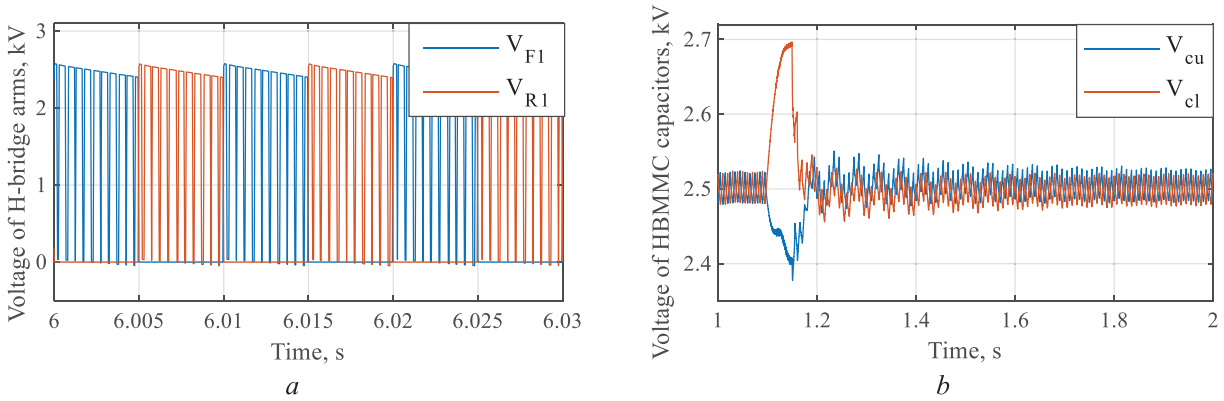


**FIGURE 13** OPAL-RT simulation results case: 1 (Cont.). (a) Voltage of H-bridge arms, and (b) effect of activation/deactivation of the proposed arm reversal control on the capacitor voltages

## 5.5 | SMs capacitors of the H-bridge MMC ($C_b$)

The capacitances of H-bridge MMC at the output stage are chosen to ensure that the output voltage is divided equally among the activated H-bridge MMC SMs, hence no bulky capacitors are needed, i.e. they are used as snubber circuits to clamp the module voltage, not to store the energy to be delivered to the load, which means small capacitances in range of picofarad are sufficient in this stage.

## 5.6 | The swapping period ($T_b$)

As ($T_b$) is decreased at a given peak to peak capacitor voltage ripples, the submodules' capacitance, as well as the DC link

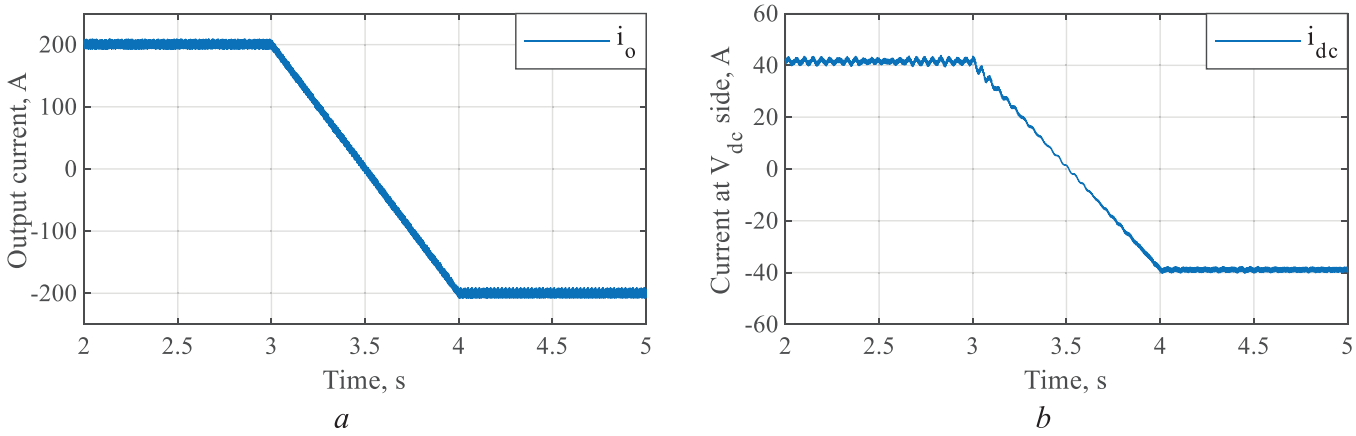


**FIGURE 14** OPAL-RT Simulation results case: 2. (a) Current at the low-voltage side, and (b) current at the $V_{dc}$ side

**TABLE 3** Experimental setup parameters

| Parameter | Value |
|---|---|
| $V_{dc}$ | 200 V |
| No. of SMs/arm | 2 |
| HBMMC SM Cap. | 1 mF |
| DC-Link cap. | 1 mF |
| $L_{dc}$ | 7 mH |
| Inductance/arm | 0.15 mH |
| DC load | 18.5 Ω |
| Output voltage reference | $0.25V_{dc}$ |
| L-filter ($L_f$) | 40 mH |
| Periodic time ($T_b$) | 0.01 s |
| Switching freq. | 2 kHz |

capacitance, decrease, but the switching losses are increased. Therefore, the selection of $T_b$ is based on compromising between the losses in the H-bridge MMC SMs switches and the capacitor size of both the HBMMC SMs and the DC link.

## 6 | SIMULATION

A simulation model has been built for the proposed modular DC-DC converter using both MATLAB/SIMULINK software package and OPAL-RT (OP4510), which is a real-time digital simulator, with a conversion ratio of 5:1 assuming the parameters listed in Table 2. It is worth noting that for $V_{dc}$ = 10 kV, $V_o$ = 2 kV, $T_b$ = 0.01 s, and peak to peak ripple voltage < 2%, Based on Equation (19), the suitable capacitance of the HBMMC SMs should be higher than 4.2 mF, so 5 mF is chosen. Similarly, based on Equation (24) the required DC-link capacitors should be higher than 4 mF, so 5 mF is selected. However, in the case of the H-bridge MMC SMs, a capacitance of 10 pF is chosen. Based on Equation (38), the corresponding arm inductance ($L_a$) should be much less than 0.5 mH. To ensure that and to decrease the $L_a$ d$i$/d$t$ effect, an inductance of 10 $\mu$H is chosen. Finally, based on Equation (39), the output filter inductance ($L_f$) should be higher than 25 mH hence 30 mH is chosen. A carrier frequency of 2 kHz and 0.5 kHz are employed for MATLAB/SIMULINK and OPAL-RT, respectively.

To show the viability of the proposed converter, two cases are considered. In the first case, namely, case 1; a passive DC load is assumed, while in the second case, a DC-link voltage of 2 kV is assumed at the low-voltage side to show the performance of the proposed approach as a DC transformer in DC grids. The cases are presented in detail in the following subsections.

### 6.1 | Case 1: Passive DC load

In this case, a DC load resistance of 10 Ω is considered at the low-voltage side of the converter, while an output L-filter of 30 mH is connected in series with the DC load to ensure a smooth load current. In this case, open-loop control is used for simplicity, where the magnitude of the reference output voltage $|V^*_o|$ is fed to the controller where the reference voltage is compared with multiple carriers using PSC-PWM, and the arm current reversal concept is applied as shown in Figure 9, such that it generates the gate pulses to the involved IGBTs.

It has to be noted that the results of both MATLAB/SIMULINK and OPAL-RT are nearly identical. Figure 10(a) and (b) shows the output voltage at the low-voltage side ($V_o$) in the case of MATLAB and OPAL-RT respectively, where a successful generation of 2 kV average voltage is realized, hence, achieving a successful DC-DC conversion with a bucking conversion ratio of 5:1. Figure 10(c) and (d) shows the load current in the low-voltage side in the case of MATLAB and OPAL-RT respectively, where a load current of 200 A is generated successfully. Figure 11(a) and (b) shows the HBMMC capacitor voltages in the case of MATLAB and OPAL-RT respectively, where the state of the capacitor voltage changes from charging to discharging and vice versa because of the swapping between the positive and negative cycles with $T_b$ = 0.01 s. This results in balanced capacitor voltages with peak-peak ripple voltages of 42 V (1.68%), i.e. less than the defined 2% ripple voltage. Figure 12(a) shows the DC-link

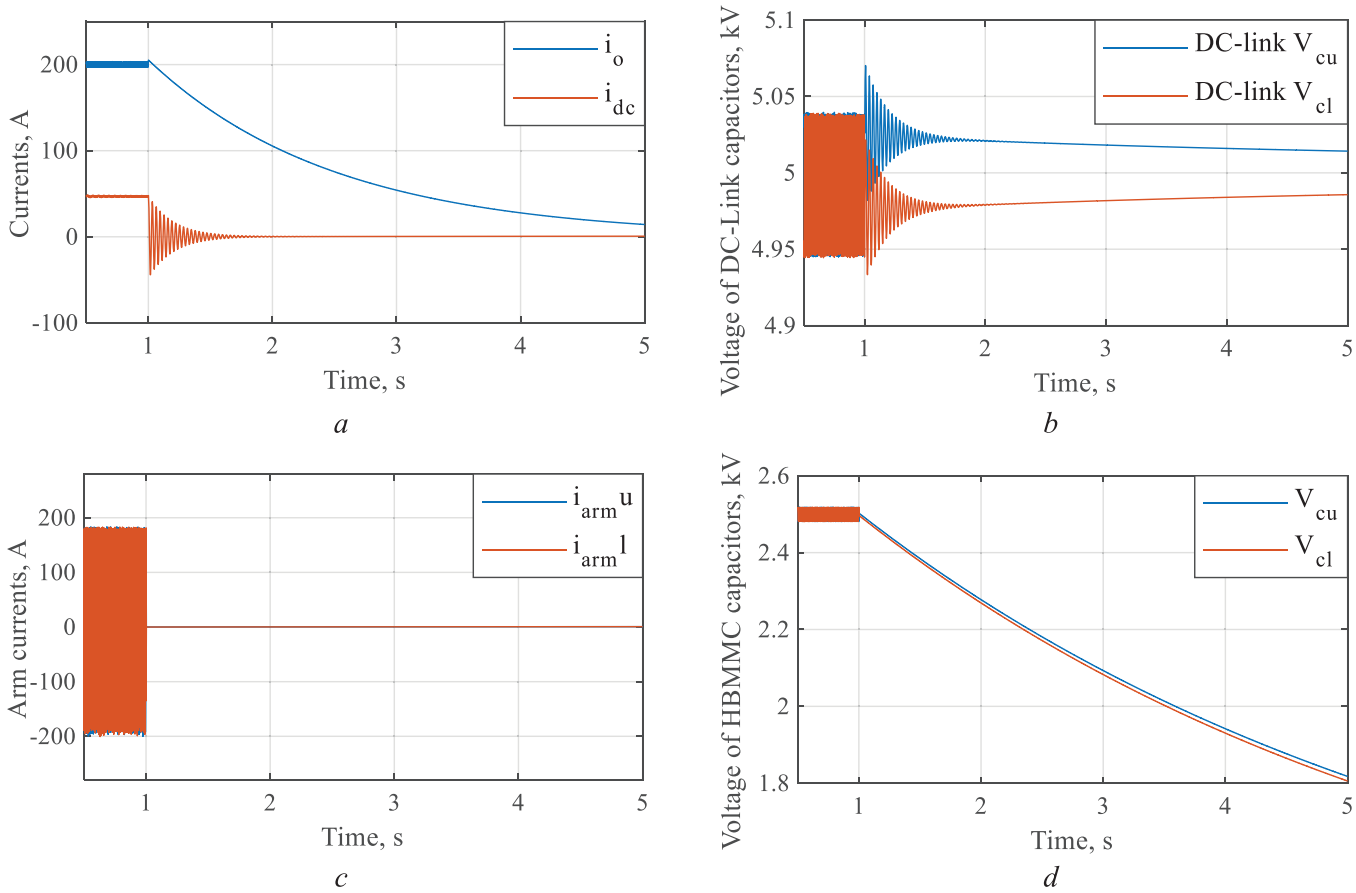


**FIGURE 15** OPAL-RT simulation results during fault at the low-voltage side. (a) Currents at both low-voltage side and high-voltage side, (b) DC-link capacitor voltages, (c) HBMMC arm currents, and (d) HBMMC capacitor voltages

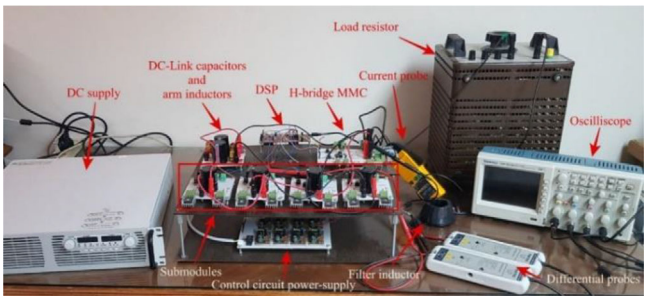


**FIGURE 16** Experimental setup

capacitor voltages extracted from the OPAL-RT real-time simulation, where the charging and the discharging of the capacitors result in a peak to peak ripple voltage of DC-link capacitors of approximately 100 V (2%). Figure 12(b) shows the corresponding HBMMC arm currents, where the arm currents are limited, hence, low current stress operation. Figure 12(c) and (d) shows the H-bridge input voltage and current respectively. The direction of the bridge input voltage and current is reversed in every swapping time, i.e. the arm current reversal concept is applied successfully. The voltages of the H-bridge arms are depicted in Figure 13(a). To show the arm current reversal concept effectiveness, the proposed arm current reversal control is disabled and then enabled. Corresponding to this action, the voltages of the HBMMC SMs capacitors are depicted in Figure 13(b), where the capacitor voltages diverge at the instant of disabling the proposed control then converge again at the instant of enabling it.

## 6.2 | Case 2: DC transformer

The presented modular DC-DC converter in this case is used as a DC transformer, which connects two DC grids of different voltage levels. The high-voltage side is named ($V_{dc}$), while the low-voltage side is named ($V_{DCL}$). As mentioned earlier, the proposed converter configuration allows a bidirectional power flow between the high and the low voltage sides. In this case, closed-loop control is used. By controlling the low voltage side current ($i_o$), the direction of power transfer is determined. The reference value of the low voltage side current ($i^*_o$) is compared with the actual value, and the comparator output error is fed to a proportional-integral (PI) controller to provide the proper output voltage reference magnitude $|V^*_o|$. Then the employed controller generates the suitable gate pulses to the involved switching devices. If the reference current ($i^*_o$) is positive, then the power flows from the high-voltage side to the low-voltage side. However, if the reference current ($i^*_o$) is negative, the power direction is reversed.

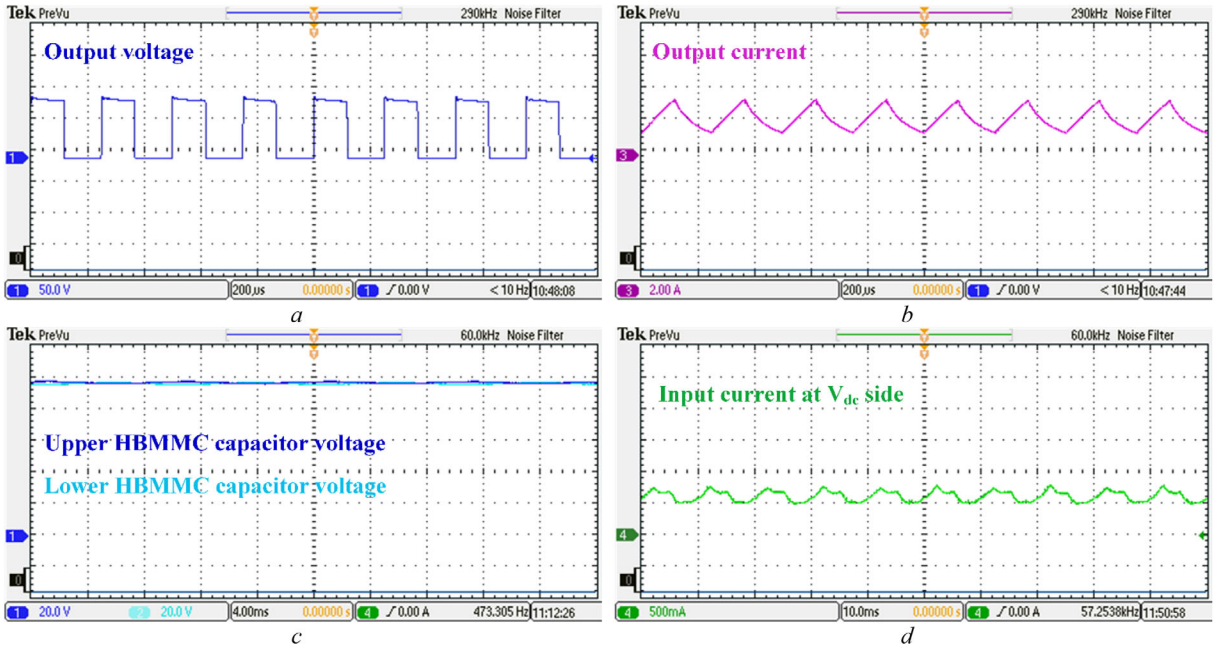


**FIGURE 17** Experimental results with the proposed configuration at $V_o = 0.25V_{dc}$. (a) The output voltage, (b) load current, (c) HBMMC SMs capacitor voltages, and (d) input current at $V_{dc}$ side

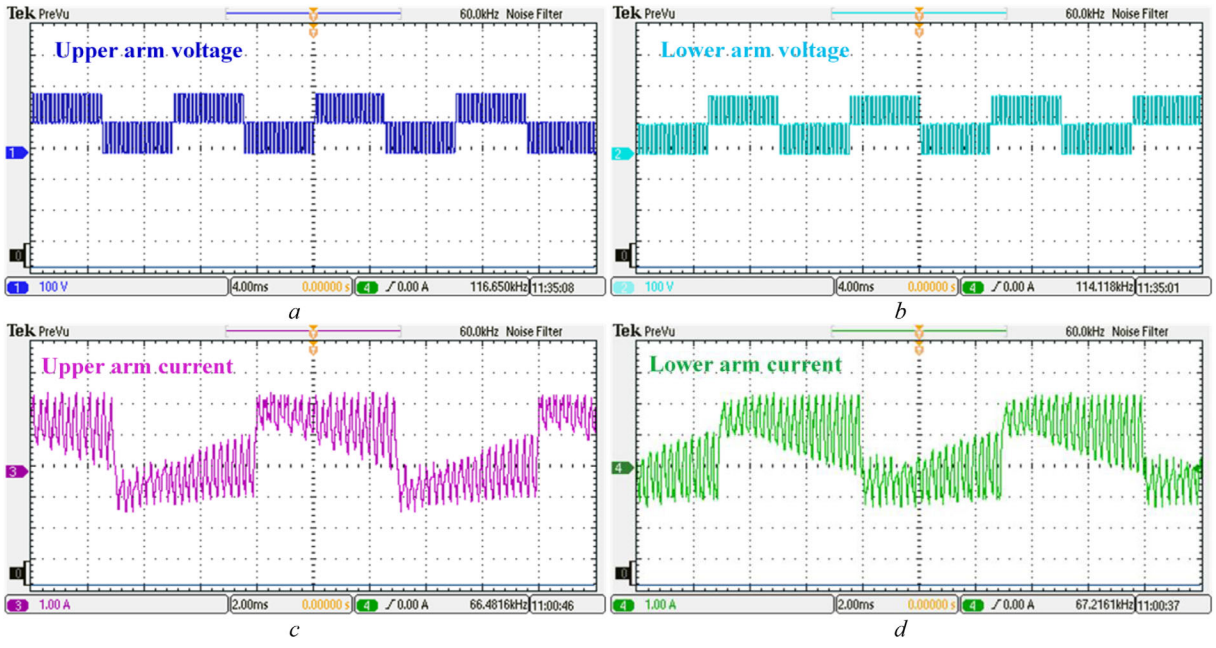


**FIGURE 18** Experimental results with the proposed configuration at $V_o = 0.25V_{dc}$ (Cont.). (a), (b) HBMMC upper and lower arm voltages, respectively, (c) and (d) the HBMMC upper and lower arm currents

To clarify the proposed converter capability of bidirectional power flow, a simulation model has been constructed on OPAL-RT, where the corresponding results are shown in Figure 14, where the output current reference ($i^*_o$) is changed gradually from 200 A to −200 A with the same defined parameters in Table 2.

Figure 14(a) and (b) shows the output current and the input current at the $V_{dc}$ side respectively, where their direction is reversed successfully at the same time. It is worth mentioning that if the output voltage of the converter is higher than the $V_{DCL}$, the output current is in the positive direction and the power flows from the high to the low voltage side. However, if the output voltage is lower than the $V_{DCL}$ then the situation is reversed where the output current is in the negative direction and the power flows from the low to the high voltage side.

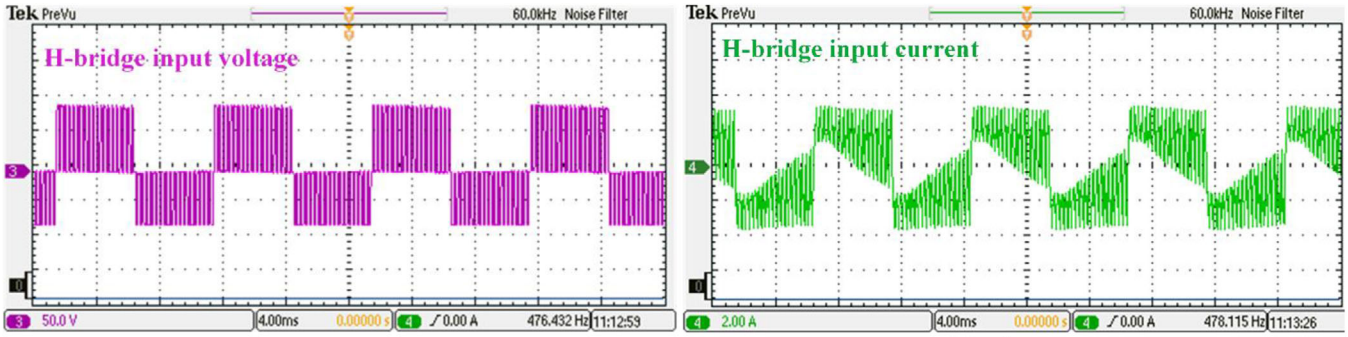


**FIGURE 19** Experimental results with the proposed configuration at $V_o = 0.25V_{dc}$. (a) The H-bridge input voltage (the output voltage of the first stage), and (b) the H-bridge input current (the output current of the first stage)

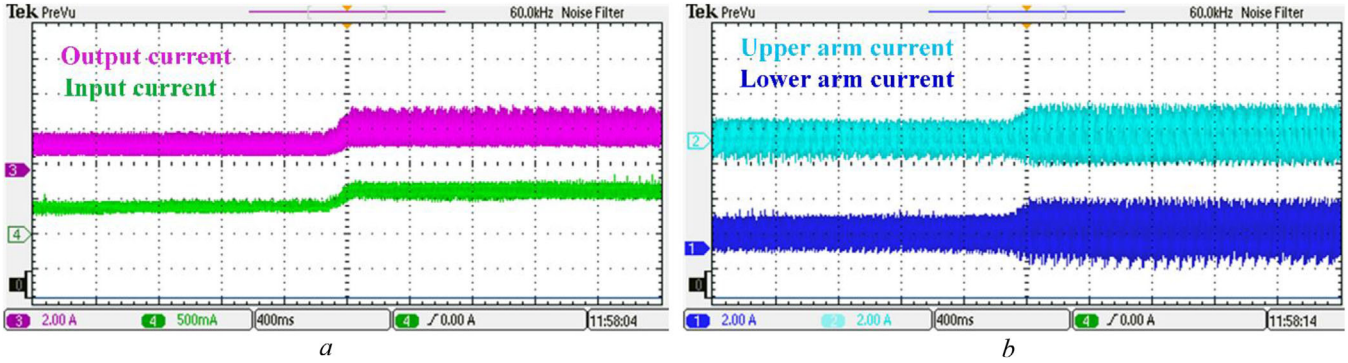


**FIGURE 20** Experimental results with the proposed configuration at $V_o = 0.25V_{dc}$ during a sudden change in the load. (a) The output and input currents, and (b) the upper and lower arm currents

To show the performance of the presented modular DC-DC converter during a DC-fault. A DC-fault has been introduced to the low-voltage side ($V_{DCL} = 0$), while a 10 kV source is connected to the input terminals of the high-voltage side. The fault has been simulated at $t = 1$ s and the gate pulses of all involved switching devices are inhibited after fault detection. The currents at both the low and high voltage sides during the low voltage fault are depicted in Figure 15(a), where both currents decrease to zero without any inrush currents. Hence no need for a circuit breaker at the low voltage side. Figure 15(b) shows the DC link capacitor voltages, which remain almost around their nominal values. The arm currents in the HBMMC decrease to zero, as depicted in Figure 15(c), without any high circulating currents at the instant of the low-voltage fault. The HBMMC capacitor voltages decay slowly as shown in Figure 15(d) due to the parasitic resistance of the converter.

It has to be noted that when the fault is applied to the high-voltage side ($V_{dc} = 0$), while a 2 kV source is connected to the terminals of the low-voltage side, the DC-link capacitors discharge through the fault and resulting in a high inrush current. In addition, after the DC-link capacitors are fully discharged, the series filtering inductance at the high side forces that high current to flow through the arm diodes of the HBMMC. Therefore, a DC circuit breaker is needed at the high voltage side to interrupt the flow of high discharge current due to the dc-side fault at the high-voltage side.

## 7 | EXPERIMENTAL VALIDATION

A small prototype of the presented arm current reversal-based modular DC-DC converter has been implemented, as depicted in Figure 16 with the parameters given in Table 3. For simplicity, the H-bridge MMC is replaced by an H-bridge inverter with 4 IGBTs. Besides, a sensor-less system is used with the PSC-PWM modulation technique. To validate the proposed configuration, an open-loop control approach has been employed, where the reference output voltage magnitude is defined and fed to the controller to provide the suitable gate pulses to the involved switching devices. The corresponding experimental results for an output voltage reference of $0.25V_{dc}$, i.e. a bucking ratio of 4:1, are shown in Figures 17–20, where the DC output voltage is generated successfully with balanced capacitor voltages.

Figure 17(a) and (b) show the output voltage and the output current, respectively, with the proposed arm current reversal-based modular DC-DC converter, where a DC output voltage is generated successfully. Figure 17(c) shows the HBMMC capacitor voltages in the upper and lower arms. The capacitor voltages in both arms charge and discharge in every period, therefore, remain balanced with acceptable voltage ripple. The input current at the $V_{dc}$ side is depicted in Figure 17(d).

Figure 18(a) and (b) shows the internal upper and lower arm voltages of the HBMMC, respectively, while the arm currents in the HBMMC are shown in Figure 18(c) and (d), respectively,

which are bipolar. Figure 19(a) and (b) shows the H-bridge input voltage and current respectively, which are the AC output values of the first stage (HBMMC) before being rectified by the second stage.

To show the experimental dynamic behaviour of the proposed DC-DC converter, a sudden increase in the load current is applied to the converter, where the output current is increased from 1.5 to 2.4 A. The corresponding results of the output and the input currents are depicted in Figure 20(a). Also, the corresponding arm currents are shown in Figure 20(b). Based on the presented experimental results, a DC-DC conversion is achieved successfully with balanced capacitor voltages. An efficiency of 83.5% is measured for the implemented low-voltage experimental setup.

## 8 | CONCLUSION

In this paper, a new arm current reversal-based modular DC-DC converter is presented, which successfully achieves balanced capacitor voltages when operating in DC-DC conversion. The proposed configuration consists of a half-bridge single-phase DC-AC HBSM-based MMC (HBMMC) followed by an H-bridge single-phase AC-DC HBSM-based MMC. The HBMMC is responsible for generating the desired DC output voltage, but only in half of a predetermined period, and its negative value in the other half, where the arm current is reversed every half period. Hence, both the charging and discharging of the capacitors occur in each period. The generated voltage of the first stage is fed to the H-bridge MMC, which acts as a rectifier and generates the desired DC output voltage for the whole period. Therefore, a successful DC-DC conversion is achieved while maintaining balanced capacitor voltages by applying the proposed arm current reversal concept. Detailed illustration of the proposed concept, along with the voltage ripples analysis and passive components design are presented in this paper. The proposed approach provides high DC-DC conversion ratios, bidirectional power flow, low current stresses, and a low number of IGBTs. Finally, simulation and experimental results are demonstrated to confirm the validity of the proposed approach.

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