International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

In-Memory Computing Based Reliable and High Speed Schmitt trigger 10T SRAM cell design

[*1]Mucherla Usha Rani, [2]N. Siva Sankar Reddy, [3]B. Rajendra Naik
[*1]Associate Professor,
ACE Engineering College, Jntuh, Medchal, Hyderabad, 501301, India.
[*]Email: usha.rani1991@gmail.com
[2]Associate Professor,
Vasavi College of Engineering, Osmania University, Hyderabad, 500089, India.
Email: n.sivasankarreddy@staff.vce.ac.in
[3]Dean Student Affairs, Osmania University Hyderabad, 500007, India.

Abstract: Static random access memories (SRAM) are useful building blocks in various applications, including cache memories, integrated data storage systems, and microprocessors. The von Neumann bottleneck difficulties are solved by in-memory computing. It eliminates unnecessary frequent data transfer between memory and processing units simultaneously. In this research, the replica-based 10T SRAM design for in-memory computing (IMC) is designed by adapting the word line control scheme in 14nm CMOS technology. In order to achieve high reading and writing capability, the Schmitt trigger inverter was used for energy-saving and stable use. To speed up the writing process of the design, a single transistor is inserted between the cross-coupled inverters. In addition, to increase the node capacity, the voltage boosting circuitry is emphasized. The adaptive word line control scheme was utilized by integrating the replica column based circuit. The Replica approach regulates signal flow through the core by using a dummy column and a dummy row in RAM. To demonstrate the viability of the suggested design, the simulated outcomes are contrasted with those of existing designs. The various performance metrics examined are Read Static Noise Margin (RSNM), Write (WSNM), Hold (HSNM), Read Access Delay (RAD), Write Access Delay (WAD), Read performance and Write performance the varying supply voltage is evaluated.

Keywords: Static random access memory, voltage booster, Schmitt trigger inverter, word line control, replica column and in memory computing.

I. INTRODUCTION

As technology develops, there is an increasing demand for microprocessors with low power dissipation and higher processing speeds. Consequently, Static Random Access Memory (SRAMs) are manufactured quickly and densely. Maintaining acceptable levels of dynamic power is the first problem since a decrease in VDD causes a quadratic or linear loss in dynamic or static power [1]. Building low-power SRAMs at the nanoscale poses two challenges: power dissipation, the leakage power, and stability. In addition, scaling causes a short-channel effect and leads to drastic performance losses. Therefore, due to scaling, the power consumption in SRAM is higher [2-3].

The sensing amplifier (SA) is affected by random variations brought on by Random Dopant Fluctuations (RDF) because SRAM cells are extremely sensitive to process variations. The access delay and SRAM read yield both significantly suffer from the mismatch in threshold voltages. To reduce power consumption in SRAM cells, the VDD can be slowed down close to the threshold voltage. Minimizing this voltage reduces power dissipation and dynamic power exponentially and quadratically. The supply voltage reduces the signal-to-noise ratio, speed and gain of the SRAM cell, leading to a reduction in stability and performance [4-7]. In conventional 6T SRAM, the static margins are not sufficient due to the intrinsic changes during reading and writing and at low supply voltages. This can affect the process variation as part of the stability analysis. Therefore, various researchers have designed different architectures to improve stability under process variation [8-11].

The existing research shows that the traditional 6T SRAM cells do not offer better reliability. The existing work [12] used the Schmitt trigger (ST) inverter in the SRAM to improve the HSNM and this cell has more RSNM than the 6T. However, this design is compromised due to the low RSNM due to the reading disorder. Then, 7T SRAM cells are used to improve RSNM at low supply voltage. However, these cells consume more power during the reading process [13]. To address this challenge, researchers developed a decoupled 8T memory line [14] during the read process. Hence, it enhanced the RSNM and yield. At low supply voltages, sufficient WM (white border) for 8T cells is still a challenging problem. To solve this problem, WRE8T was developed by reducing the left inverter during writing and increasing the WM [15]. However, at low supply voltages, this design does not have enough RSNM and HSNM.

Initially, 6T SRAM is suitable to design LLC (last level cache), however, the activating multi-rows affects the RSNM. Further, it generates short circuit paths, and it flips states of cells. 8T SRAM decoupled the read and write operations with increased sensing margin and low power consumption. But, 8T SRAM has a thirty percentage area penalty compared to the 6T

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

SRAM. Moreover, 8T SRAM utilizes a single read bit line, and it calculates only AND operation [17]. The Von Neumann bottleneck is an undesirable problem that has recently arisen in application fields including artificial intelligence, machine and deep learning, and search processes. The increased volume of data flow between the CPU and RAM is the factor that has led to this problem. Therefore, due to this, the delay and energy consumption gets increased. In-memory computing (IMC) has evolved as a cutting-edge strategy that has decreased the amount of data exchange between the CPU and the main memory to get around these limitations.

One of the intriguing features of this method is its ability to implement basic logical operations and enable search operations in the memory. SRAM with IMC can be widely used in applications such as pattern matching and neural networks. When the neural networks are trained on large databases, inference calculations are performed over the weights of the layers [16]. Hence, in this work, 10 T SRAM design for IMC is designed. The insights of this research work is listed below:

- To improve the RSNM and capacity of the 10T SRAM design, the modified cross-coupled inverter structures with voltage booster circuit are integrated.
- To extend the 10 T SRAM design for In-Memory Computing by introducing an adaptive word line control. This method will be used to remove the sneaky direct current and the dynamic read disturbance in 10T SRAM based in-memory computing.
- To develop an adaptive word line control scheme based replica column circuit to control the flow of signals and eradicate the short circuit pathway.

The organization of the research paper is as follows: The examples of existing SRAM designs are surveyed in section 2. The proposed design with schematic represnetation is detailed in section 3. Section 4 describes the performance measures and compares them with existing designs. Finally, the research ends with section 5 conclusion.

II. RELATED WORK

Shakouri et al. [18] presented a 10T single-ended SRAM cell with less static power and better stability. ST was used to extend the RSNM and decouple the memory node by integrating additional transistors. It is complex to write 1 into a single-ended SRAM cell. To solve this problem, an additional pMOS transistor and exact capacitive coupling were used. The authors demonstrated the simulation on 10,000 Monto Carlo and proved that the SRAM cell achieved 7.5x, 1.4x and 1.1x performance than the traditional 6T SRAM cell. With a supply voltage of 0.5V, this model consumed less static current and was 1.5 times better than the traditional 6T SRAM cell.

Sha et al. [19] introduced an AS10T (asymmetric 10T) SRAM cell to improve RSNM. The voltage amplifier was then connected for a capacity enhancement. This AS101 model achieved 75.8% better and the soft error rate achieved by the AS10T was 6.41 times and 3.2 times lower than the 6T SRAM cell. Due to its better performance, it can be used for aerospace applications.

Wang et al. [20] presented symmetric 4T2R based CIM (Computing in Memory) SRAM using operations such as XNOR and XOR. Then, the LLU (local logic unit) was combined with an SRAM cell with two surface channel transistors. This design uses only six elements and has better area efficiency. This design was only suitable for XNOR, XOR, NOR and NAND gates and was not implemented for Boolean logic operations.

Xiao et al. [21] designed a 6T SRAM-CIM macro and sub-ranging analog to digital converter (ADC) for AI edge applications. A local processing component with a DAC converter (digital-to-analog converter) supporting AND and XNOR operations was developed. The CIM is designed for MAC (multiply and accumulate) operation to reduce energy costs. The subdomain ADC is designed to support quantizations such as 4-b and 42.24-b for multiple model operations. For the SRAM design, the achieved array area efficiency was 76.6%. For the CIFAR-10 dataset, the achieved classification accuracy was 85.5%, and the accuracy loss was about 1.3%.

Wang et al. [22] presented an IMC model with FS-GDI (Full Swing-Gate Diffusion Input) in 6T SRAM. This model realized the basic Boolean operations and also realized the RCA (Ripple Carry Adder). Furthermore, the authors were shown that the IMC would be impossible without a CPU or an ALU. FS-GDI overcomes the problem of reduced voltage swing but has high static power and low speed. Therefore, IMC was used to improve energy efficiency.

Sachdeva and Tomar [23] presented 10T SRAM with better read and write margin performance. The authors demonstrated reading performance reduction and stability maintenance for fair performance. Various design measures were presented, such as read power, data hold voltage, and cell read voltage. Compared to 6T SRAM, this design achieved a better read and write margin of 8.6% and 16.8%. In addition, the read and write latency has been increased by 1.78x and 2.32x, respectively, compared to the 6T SRAM.

ST-based differential SRAM cell design aids in resolving concerns with the design of basic SRAM cells' reading and writing operations. The ST method is used in this study to increase cell acceptance at low technology levels. The 10T SRAM design has higher leakage than conventional SRAM designs and enhances the circuit's effective power dissipation. Recently, the 10T SRAM cell has gained popularity for stable and low power applications.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

III. PROPOSED METHODOLOGY

In this research, the 10T SRAM design is designed for in-memory computing. First, the modified cross-coupled inverters and voltage booster circuits are inserted into the SRAM cell design to improve the RSNM and capacity of the storage node. Before that, a single transistor is inserted to decouple the storage node from the read bit line. To improve the writing process, the single nMOS transistor is inserted between cross-coupled inverters. In this study, a ST inverter is introduced to address this problem. With the help of the Schmitt trigger inverter, the read tolerance for static noise is increased. Also, inserting a voltage booster circuit helps to easily write "1" without errors. The focus of this research is to develop an improved word line control scheme based on the integration of a replica column, a voltage comparator and a timing controller. The proposed design is shown in Figure (1), and the architecture is comprised of a sensing amplifier and some other peripheral circuits such as a row decoder, a word line (WL) driver, a write driver, a column decoder and pre-charging circuit realization.

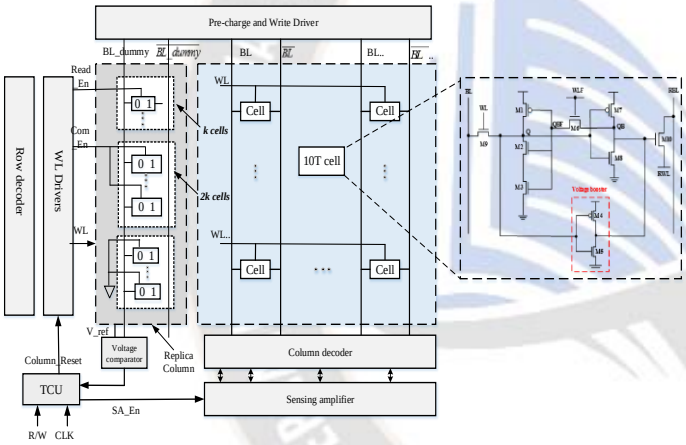

Figure 1: Schematic representation of SRAM design

A. SRAM design based in memory computing

The proposed cell design is emphasized with two main parts, namely Schmitt trigger inverters (M1, M2, M3) and voltage booster (M4, M5). To enhance the write operation, the n-mos transistor, which is named M6, is linked between the cross coupled inverters. The conventional inverters M7 and M8 are placed in the design, and the write and read operations are performed using two n-mos transistors named M9 and M10, respectively. For both the read (R) and write (W) operations, several bitlines, such as RBL, RWL, WL, and WLF, are required. An inverter called a ST has been offered to solve this problem. This construction offers better SNM for SRAM and enhanced inverter performance. The double-length pull-up transistor (M1) and two stack transistors (M2 and M3) are considered to greatly lower the static power consumption. The proposed cell's write operation is carried out through the leftmost bitline (BL). The performance of the read and write abilities is improved by using the read and write access transistors (M9 and M10). The purpose of a voltage booster is to protect an SRAM cell from the effects of a particle impact. The design of the proposed voltage boosted ST 10T cell is demonstrated in Figure (2).

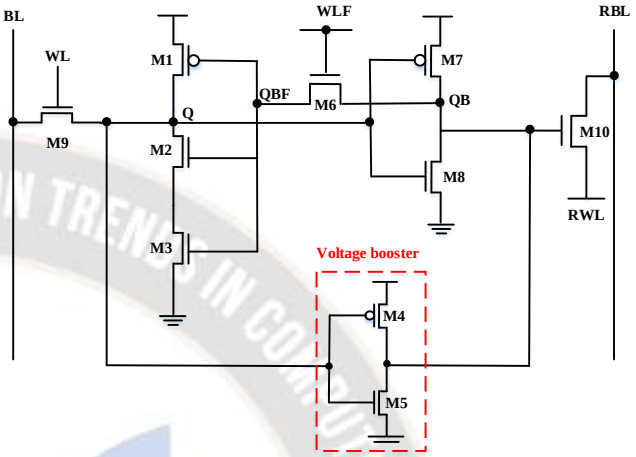

Figure 2: Schematic view of ST10T SRAM

1) Read, Write and hold operation: Once the read operation is engaged to process, WL is grounded, and RBL is pre-charged to VDD. The sensing amplifier finish the read process when Q= "0" and QB= "1", and M10 activates (turns on) discharging RBL. Consequently, RBL stays precharged at VDD value when QB= "0". Data node QB is connected to the gate terminal of the read transistor (M10), and it prevents the charge sharing process between the RBL and the data node QB. To perform the write operation, the BL from the left is used. In addition, the nMOS transistor (M6) is used between QB and the QBF. Write "1" causes the column-based WLF to transition from VDD to ground, decreasing the QBF voltage by ΔV_{QBF} due to capacitive coupling. The voltages of the BL and RBL are at VDD in the hold state. The 10T SRAM cell features a voltage booster circuit that increases both the amount of data that can be accessed simultaneously and the computational stability. The cell operation is shown in Table (1).

TABLE I: CELL OPERATION

Control signals	Write 0	Write 1	Read	Hold
WL	Vdd	Vdd	Gnd	Gnd
BL	Gnd	Vdd	Vdd	Vdd
WLF	Vdd	Gnd	Vdd	Vdd
RWL	Vdd	Vdd	Gnd	Vdd
RBL	Pre-charge	Pre-charge	Pre-charge	Pre-charge

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

2) Inmemory logic operations: The in memory logic AND and OR operations are defined in this section and its illustration is shown in Figure (3). The output may be determined in accordance with the information in storage nodes Q1 and Q2 under AND operation. Initially, in AND operation, the two storage nodes Q1 and Q2 are visible, and to perform row wise AND operation, these can be considered as input with the cases of 00, 01, 10 and 11, respectively. If both Q1 and Q2 are 1, the BL and WL voltages remain elevated due to the fact that the BL and WL paths to the ground are both in the OFF state. If Q1 or Q2 are both 0, however, the bit line bar (BLB) discharges, resulting in output 0, because at least one channel from the BL to the ground is in an ON state. This logic operation's workflow is comparable to a read operation of SRAM. The input for a logic OR operation can be the visible storage nodes QB1 and QB2, which are both involved in the operation. It is evident from Table (2) that in the case of a logic OR operation, the output remains high even if both QB1 and QB2 are 0. When QB1 and QB2 are 0, the output gets discharged. Therefore, IMC with AND and OR operations under different conditions are examined.

TABLE II: IN MEMORY COMPUTING BASED LOGIC AND AND OR OPERATION

Logic AND operation				Logic OR operation			
Q1	**Q2**	**BL**	**WL**	**QB1**	**QB2**	**RBL**	**RWL**
0	**0**	↓	↓	**0**	**0**	—	—
0	**1**	↓	↓	**0**	**1**	↓	↓
1	**0**	↓	↓	**1**	**0**	↓	↓
1	**1**	—	—	**1**	**1**	↓	↓

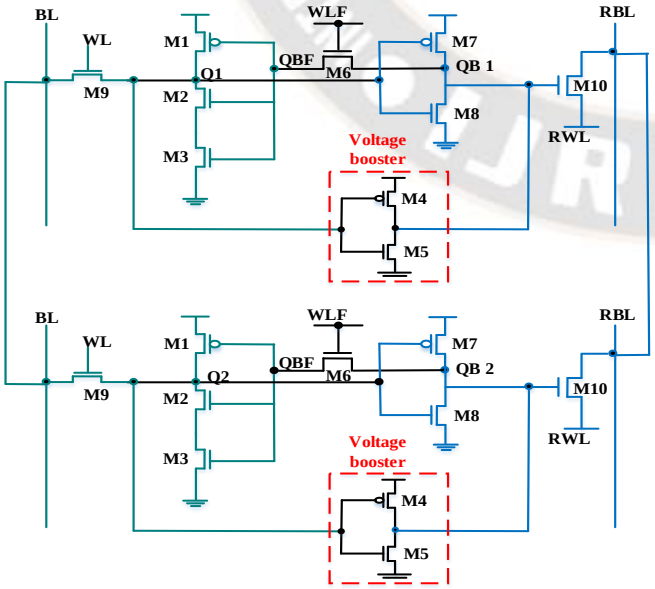

Figure 3: In memory logic design

B. Adaptive wordline control scheme

The enhanced wordline control strategy is introduced for the purpose of eradicating the read disturbance and the sneaky direct current path by maintaining the bitline voltage at a high level. Word lines must be turned on for the right amount of time in order to create a correct voltage difference between BL and $\overline{BL}$. To maintain a high bitline voltage during, wordlines must also be shut off quickly. Therefore, creating a successful wordline control strategy is difficult. When the SRAM is accessed (Start = 1), the Read_En or Com_En control signals will be turned on. The comparator will deliver a control signal (V_out = 1) that will deactivate the chosen wordline (Read_En = 0 or Com_En = 0, and WL[i] = 0), as well as activate the sense amplifier enable signals (SA_En = 1), when the dummy bitline discharges below V_ref. This will terminate the deceptive short circuit path between the two access transistors, thereby preventing further bitline discharge during the computing access. The schematic view of the adaptive word line control scheme is illustrated in Figure (4).

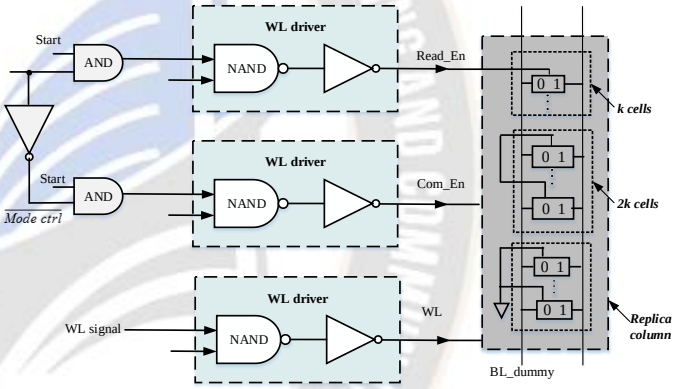

Figure 4: Schematic of wordline control scheme

C. Row decoder/ Column decoder

Typically, the SRAM cell array comprises rows and columns of cells. The AND gate based row decoder is utilized with 2 bit address to activate one of the WL and four AND gates. Additionally, several BLs are activated by the column decoder. However, to activate either the WL or RWL at any given interval, row/column decoders should be adjusted. Finally, each output of the row decoders is connected to a DEMUX based AND gate. Therefore, the schematic view of the row and column decoder is illustrated in Figure (5).

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

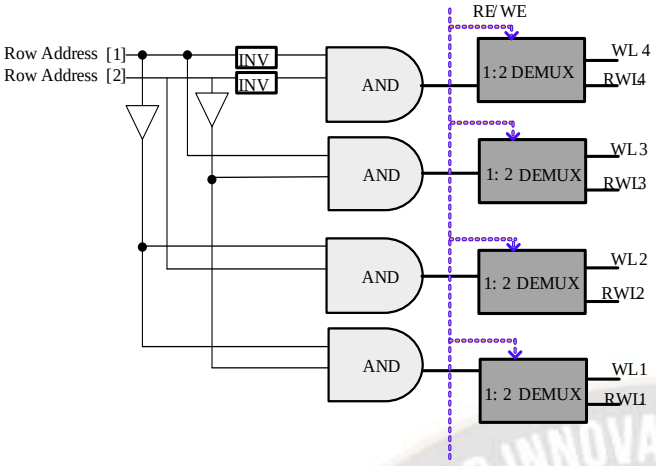

Figure 5: Schematic view of row and column decoder

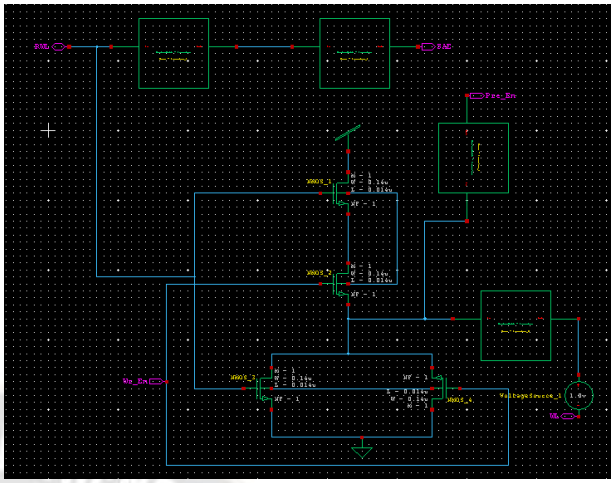

Figure 7: Schematic design of TCU

D. Sensing amplifier (SA) and TCU

The SA is a crucial element in memory architecture. Figure (6) shows the schematic perspective of a latch-type SA. The primary task of the SA is to amplify the analogue differential voltage produced on the bit lines by a read-accessed cell, thereby significantly lowering the time needed for a read operation. To ensure that the proper time sequence is accomplished during read and write operations, the time control unit (TCU) unit is utilized, and it controls the circuit for pre-charge clocking, WL, read wordline (RWL), sensing amplifier, and write enable. To avoid unwanted read/write operations, timing risks must be avoided. By adopting a wordline method or using a voltage slightly higher than the VDD for the wordline, the timing block described in this work and the diagrammatic representation of TCU unit is demonstrated in Figure (7).

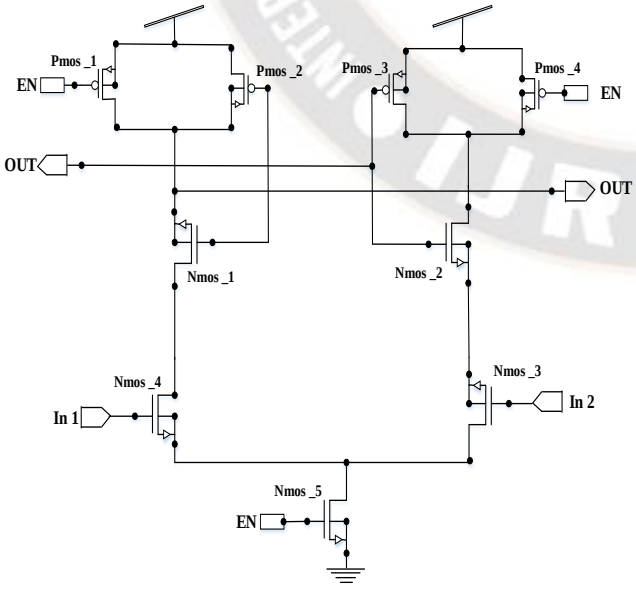

Figure 6: Design of sensing amplifier

E. Pre charging and write driver

One of the crucial parts utilized in SRAM is the pre-charge circuit. SRAM works by charging the bit and bitbar lines to VDD. With the exception of read and write operations, the precharged circuit always allows the bit lines to be charged high. By stacking two NMOS transistors, the write driver produces two pass-transistor AND gates with NMOS T1, T3, and T2, T4 transistors. The NMOS transistors' Q1 and Q2 sources are grounded. The input data enables one of the transistors T1 or T2 when a write enable is present by way of inverters 1 and 2. Additionally, when releasing BL or BLB from the pre-charge level to the ground level, a powerful "0" is applied. The schematic design of pre-charging and write driver is illustrated in Figure (8).

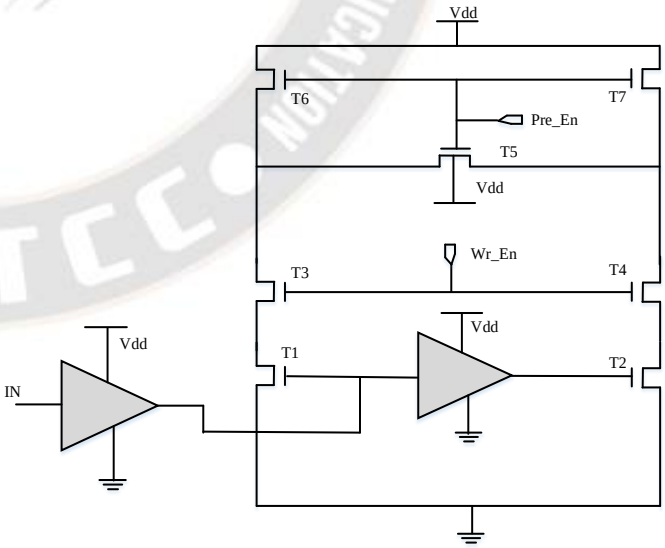

Figure 8: Schematic design of pre-charging and write driver

IV. RESULT AND DISCUSSIONS

In this section, the effectiveness of the proposed cell is determined with respect to the essential parameters such as

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

noise margin analysis, power analysis and delay analysis. However, the SRAM cell is compared with existing designs [24-27] and Tanner EDA Tool 16.0 was used to build the proposed cell. Figure (9) shows the simulated read and write waveform for the intended architecture.

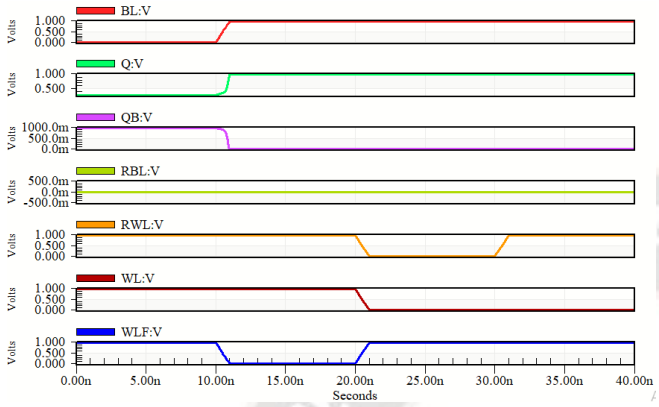

Figure 9: Waveform of the proposed design

A. Evaluation of stability analysis

A statistic called SNM may be used to evaluate the stability of SRAM designs. The standard static strategy, such as the butterfly method or N curve, is described here to estimate the SNM. The stability analysis is classified into three groups namely, RSNM, WSNM, and HSNM. This section contrasts the proposed SNM analysis with popular techniques like 10TRWM and TS14T.

1) RSNM: The ability of an SRAM cell is to maintain the information during the progress of read operation. Less noise might affect the stored data during the reading process. The voltage at node Q can convert VDD from "0" under these biassing circumstances. Then, a voltage transfer curve of QB versus Q is constructed using the data extracted from the tanning tool, illustrated in Figure (10). Compared to previous SRAM designs at a supply voltage of 0.6V, the proposed design exhibits greater read stability by offering a higher RSNM of roughly 265 mV. However, the existing SEDFT10T, TS14T, and HDFWA-PDP designs yield an RSNM of 176mv, 130mV and 230 mV, respectively. The RSNM of the proposed design is illustrated in Figure (10).

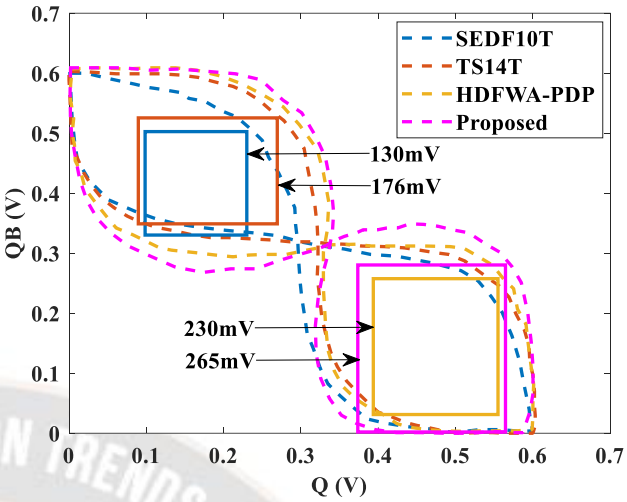

Figure 10: RSNM analysis

2) WSNM: The possibility of a write operation succeeding in an SRAM bit cell is quantified by the WSNM. The WSNM analysis of the proposed model over existing designs with 0.6 V is illustrated in Figure (11). It demonstrates how easy it is for an SRAM bit cell to change the data being saved by bringing the node that is holding the value "1" below the switching threshold voltage of the opposing inverter that is holding the value "0". BLB (Bit line bar) and BL are coupled to VDD, while BL remains connected to the ground during WSNM measurement. This biassing circumstance results in High voltage at node (Q), and node QB can provide the read VTC curve. The write VTC is calculated under these circumstances. The suggested SRAM design exhibits improved write stability compared to current designs like HDFWA-PDP, SEDF10T and TS14T. The proposed design delivers a higher WSNM of roughly 340 mV. SEDFT10T provides a WSNM of about 175 mV, HDFWA-PDP provides a WSNM of 300mV, and TS14T provides a WSNM of 250 mV, demonstrating worst-case write stability.

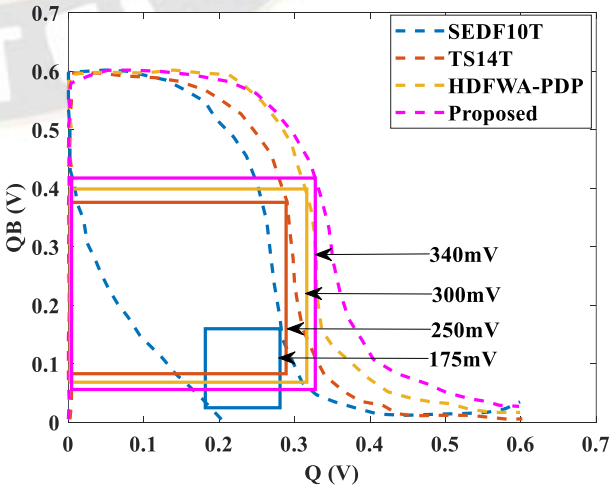

Figure 11: WSNM of the proposed design

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

3) HSNM: Figure (12) shows the HSNM of the suggested design at various supply voltages. The proposed design yields an HSNM of 230mV while the existing design attains a very low value of about 125mV, 180mV and 200mV, respectively.

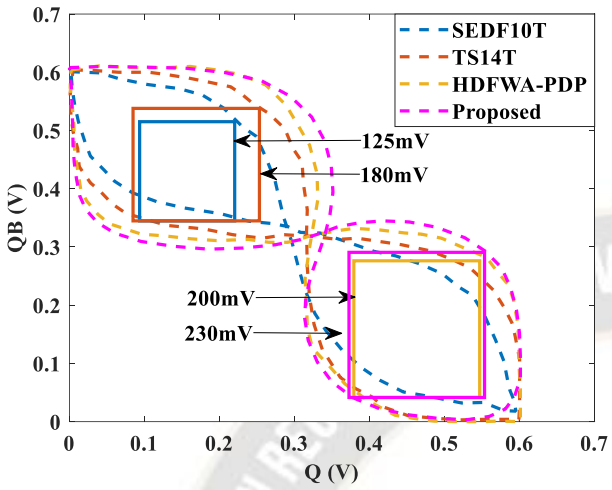

Figure 12: HSNM of the proposed design

B. Performance of delay Vs supply voltage

This section examines the performance analysis of delay in terms of read access delay (RAD) and write access delay (WAD). Therefore, the analysis of RAD and WAD under varying supply voltage are illustrated in Figures (13) and (14), respectively. The read delay judges how quickly a read operation occurs, and the write delay or write access time indicates how quickly the write operation completes to write the data 0 or 1 into memory. This procedure switches the logic Q/QB in the memory cell from 0 to 1 when the Q exceeds 90% of the VDD value. Under this delay analysis, the existing designs such as SEDF10T, SBL9T, TG8T, TS14T and HDFWA-PDP are analysed. The figures show that the proposed design attains less delay due to the adaption of wordline control schemes and in memory computing approaches. From Figure (13) and Figure (14), it is seen that the proposed design yields a very low delay under varying supply voltages.

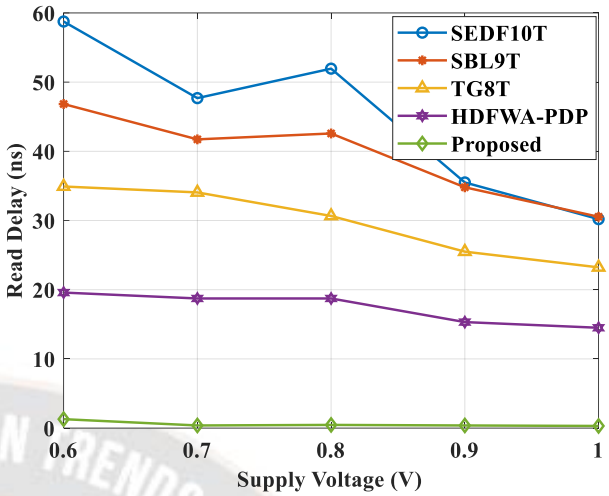

Figure 13: Analysis of Read delay

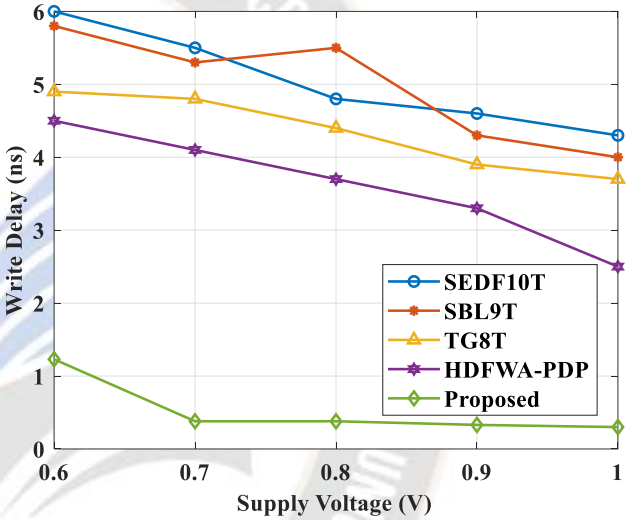

Figure 14: Analysis of Write delay

C. Power analysis Vs Supply voltage

Figures (15) and (16) demonstrate the write power (WP) and read power (RP) consumption of the proposed design by contrasting it with typical existing designs. Table (3) provides a quantitative measurement of RP and WP respectively.

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: *19 August 2023* ***Revised:*** *12 October 2023* ***Accepted:*** *24 October 2023*

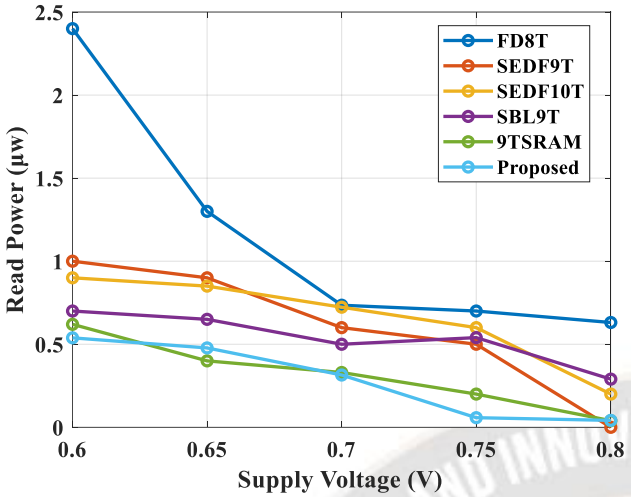

Figure 15: RP analysis

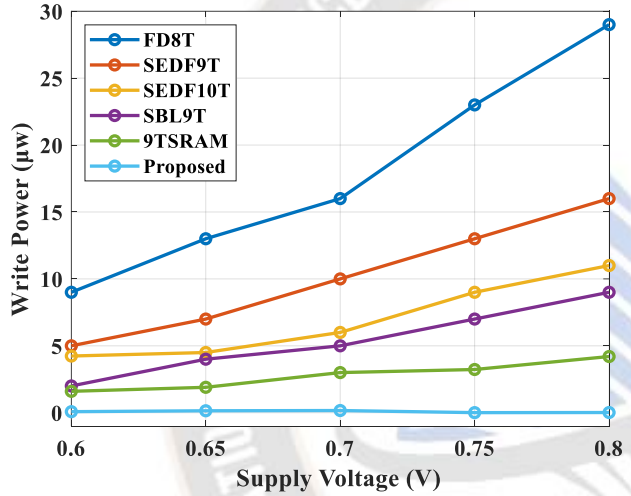

Figure 16: WO analysis

TABLE III: POWER ANALYSIS IN TREMS OF READ AND WRITE POWER

RP(µw)					
Supply Voltage (V)	0.6	0.65	0.7	0.75	0.8
FD8T	2.4	1.3	0.735	0.7	0.631
SEDF9T	1	0.9	0.6	0.5	0
SEDF10T	0.9	0.85	0.723	0.6	0.3
SBL9T	0.7	0.66	0.5	0.54	0.29
9TSRAM	0.62	0.4	0.33	0.2	0.04
Proposed	0.5835	0.47	0.3148	0.0579	0.041
WP(µw)					
Supply Voltage (V)	0.6	0.65	0.7	0.75	0.8
FD8T	9	13	16	23	29
SEDF9T	5	7	10	13	16
SEDF10T	4.237	4.5	6	9	11
SBL9T	2	4	5	7	9
9TSRAM	1.6	1.9	3	3.23	4.2
Proposed	**0.080**	**0.146**	**0.165**	**0.007**	**0.015**

V. CONCLUSION

In this research, the IMC based SRAM design is proposed and implemented in 14nm CMOS technology using the Cadence Virtuoso tool. The Schmitt-trigger inverter was used for low power and steady application to achieve strong read and write capabilities. The cross-coupled inverter structures can be modified by connecting the Schmitt-trigger (ST) inverters with conventional inverters to improve the characteristics of the cross-coupled inverter and offer high static noise margin performance. The voltage booster circuit is placed between the storage nodes of the design in order to increase the node capacitance. The replica column-based circuit had been used in conjunction with the adaptive word line control technique. The replica technique uses a dummy column and row in the RAM to control the signal flow through the core. In order to demonstrate the effectiveness of the suggested design, the performance measurements of margin analysis, delay analysis, and power analysis are investigated and contrasted with existing designs. The design can be implemented with several technologies for the same logic in the future, and the temperature analysis has also been done.

REFERENCES

[1] E. Abbasian, S. Birla, M. Gholipour, “A comprehensive analysis of different SRAM cell topologies in 7-nm FinFET technology”. Silicon, pp.1-12, 2021.

[2] S. Ahmad, N. Alam, M. Hasan, “Pseudo differential multi-cell upset immune robust SRAM cell for ultra-low power applications”. AEU-International Journal of Electronics and Communications, Vol. 83, pp.366-375, 2018.

[3] S. Gupta, K. Gupta, N. Pandey, “A 32-nm subthreshold 7T SRAM bit cell with read assist”. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 25(12) (2017) pp.3473-3483.

[4] R. Manoj Kumar, P.V. Sridevi, “Design of a bit-interleaved low power 10T SRAM cell with enhanced stability”. Journal of Circuits, Systems and Computers, Vol. 30(08), p.2150142, 2021.

[5] N. Eslami, B. Ebrahimi, E. Shakouri, D. Najafi, “A single-ended low leakage and low voltage 10T SRAM cell with high yield”. Analog Integrated Circuits and Signal Processing, Vol. 105(2), pp.263-274, 2020.

[6] D. Mittal, V.K. Tomar, “Performance Evaluation of 6T, 7T, 8T, and 9T SRAM cell Topologies at 90 nm Technology Node”. In 2020 11th International Conference on Computing,

Communication and Networking Technologies (ICCCNT), pp.1-4, 2020. IEEE.

[7] K. Cho, J. Park, T.W. Oh, S.O. Jung, "One-sided schmitt-trigger-based 9T SRAM cell for near-threshold operation". IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 67(5), pp.1551-1561, 2020.

[8] N. Gupta, V. Sharma, A.P. Shah, S. Khan, M. Huebner, S.K. Vishvakarma, "An energy-efficient data-dependent low-power 10T SRAM cell design for LiFi enabled smartstreet lighting system application". International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Vol. 33(6), p.e2766, 2020.

[9] S. Pal, S. Bose, A. Islam, "Design of SRAM cell for low power portable healthcare applications". Microsystem Technologies, 1-12, 2020.

[10] G. Prasad, N. Kumari, B.C. Mandi, M. Ali, "Design and statistical analysis of low power and high speed 10T static random access memory cell". International Journal of Circuit Theory and Applications, Vol. 48(8), pp.1319-1328, 2020.

[11] E. Abbasian, M. Gholipour, "Design of a Schmitt-Trigger-Based 7T SRAM cell for variation resilient Low-Energy consumption and reliable internet of things applications". AEU-International Journal of Electronics and Communications, Vol. 138, p.153899, 2021.

[12] J.P. Kulkarni, K. Kim, K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM". IEEE Journal of Solid-State Circuits, Vol. 42(10), pp.2303-2313, 2007.

[13] M. Ansari, H. Afzali-Kusha, B. Ebrahimi, Z. Navabi, A. Afzali-Kusha, M. Pedram, "A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies". Integration, Vol. 50, pp.91-106, 2015.

[14] S. Gupta, K. Gupta, N. Pandey, "Pentavariate $ V_ {\mathrm {min}} $ Analysis of a Subthreshold 10T SRAM Bit Cell with Variation Tolerant Write and Divided Bit-Line Read". IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 65(10), pp.3326-3337, 2018.

[15] G. Pasandi, S.M. Fakhraie, "An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs". IEEE Transactions on Electron Devices, Vol. 61(7), pp.2357-2363, 2014.

[16] S. Yin, Z. Jiang, J.S. Seo, M. Seok, "XNOR-SRAM: In-memory computing SRAM macro for binary/ternary deep neural networks". IEEE Journal of Solid-State Circuits, Vol. 55(6), pp.1733-1743, 2020.

[17] S. Mittal, G. Verma, B. Kaushik, F.A. Khanday, "A survey of SRAM-based in-memory computing techniques and applications". Journal of Systems Architecture, Vol. 119, p.102276, 2021.

[18] E. Shakouri, B. Ebrahimi, N. Eslami, M. Chahardori, "Single-ended 10T SRAM cell with high yield and low standby power". Circuits, Systems, and Signal Processing, Vol. 40(7), pp.3479-3499, 2021.

[19] A.P. Shah, S.K. Vishvakarma, M, "Hübner. Soft error hardened asymmetric 10T SRAM cell for aerospace applications". Journal of Electronic Testing, Vol. 36(2), pp.255-269, 2020.

[20] F. Wang, J. Li, Z. Zhang, Y. Ding, Y. Xiong, X. Hou, H. Chen, P. Zhou, "Multifunctional computing-in-memory SRAM cells based on two-surface-channel MoS2 transistors". Iscience, Vol. 24(10), p.103138, 2021.

[21] K. Xiao, X. Cui, X. Qiao, Y. Wang, "A 128 Kb DAC-less 6T SRAM computing-in-memory macro with prioritized subranging ADC for AI edge applications". Microelectronics Journal, Vol. 126, p.105506, 2022.

[22] C.C. Wang, N. Sulistiyanto, T.Y. Tsai, Y.H. Chen, "Multifunctional in-memory computation architecture using single-ended disturb-free 6T SRAM". In Advances in Electronics Engineering, pp.49-57, 2020. Springer, Singapore.

[23] A. Sachdeva, V.K. Tomar, "Design of 10T SRAM cell with improved read performance and expanded write margin". IET Circuits, Devices & Systems, Vol. 15(1), pp.42-64, 2021.

[24] D. Anh-Tuan, J. Y. S. Low, J. Y. L. Low, Z.H. Kong, X. Tan, K.S. Yeo, "An 8T differential SRAM with improved noise margin for bit-interleaving in 65 nm CMOS", IEEE Trans. Circuits Syst. I, Reg. Papers, Vol. 58(6), p.1252–1263, 2011. doi: 10.1109/TCSI.2010. 2103154.

[25] M.H. Tu et al, "A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing", IEEE J. Solid-State Circuits, Vol. 47(6) , pp.1469–1482, 2012. doi: 10.1109/JSSC.2012.2187474.

[26] S. Mansore, R. Gamad, "A data-aware write-assist 10T SRAM cell with bit-interleaving capability". Turkish Journal of Electrical Engineering and Computer Sciences Vol. 26(5), pp.2361-2373, 2018.

[27] C. Roy, A. Islam, "Design of low power, variation tolerant single bitline 9T SRAM cell in 16-nm technology in subthreshold region". Microelectronics Reliability Vol. 120, p.114126, 2021.