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# Design and Implementation of Hybrid Multiplier for DSP Applications

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**Abstract**— In recent decades, there has been a consistent reduction in feature sizes in integrated circuit (IC) technology, leading to the need for increased placement of functional circuits on each chip. When it comes to the design of digital circuits, there is a significant focus on hybrid logic. Hybrid logic is highly regarded due to its ability to consume less power while achieving higher efficiency. Hybrid logic circuits have similarities to complementary metal-oxide-semiconductor (CMOS) transistors, yet possess a reduced transistor count while offering enhanced performance and reliability capabilities. This study examines the modeling and implementation hybrid multiplier with of help of hybrid adder. The functionality of adder is determined with the help of hybrid logic producing XOR/XNOR functionalities in single circuit. The proposed hybrid Multiplier, which incorporates a hybrid Adder, has been successfully designed and implemented using CMOS 45nm technology and Mentor Graphics software the hybrid transistor logic multiplier demonstrates a decrease in total delay of 60% compared to CMOS.

**Keywords**-CMOS, XOR/XNOR, IC, hybrid logic.

## I. INTRODUCTION

All The application of Very Large Scale Integration (VLSI) technology has enabled the consolidation of numerous complex devices into a single chip, enabling the deployment of diverse operations and capabilities. The use of analog circuits in complex devices emulated within the digital realm has led to increased power consumption, raising concerns over reliability and cost. Moreover, incorporating nano-scale range systems in the context of very large-scale integration (VLSI) has resulted in many challenges to design resilience. These challenges encompass signal integrity, soft errors, and process unpredictability. Presently, a notable scholarly focus exists on the mitigation of intricacy linked to the execution of cryptography and Digital Signal Processing (DSP) methods. When developing a software program, a critical aspect that significantly influences the effectiveness of its intended operation is the assessment of fundamental limitations, such as mathematical components like adders and multipliers (Smith, 2010; Johnson, 2015). There is a dominant tendency in multiplication that favours increased efficiency, accelerated performance, and reduced expenditure.

The achievement has been facilitated by the rapid increase in the quantity of microchips and processing speed due to advancements in Very Large Scale Integration (VLSI) technology. The issue of excessive energy use surpasses the limitations of dependability and expense. Furthermore, when the system is scaled down to the Nanoscale range, it faces challenges related to design resilience, including signal integrity, soft mistakes, and process unpredictability. Moreover, the concerns about power consumption and durability demonstrate an ongoing trend. The above-described matter has resulted in a complex predicament within information systems design, which is expected to impede future advancements. As per experts in computer systems, it is crucial to consider power consumption and system robustness across all phases of the design process. The meticulous examination of logic types holds significant significance in conceptualising circuit designs, as it directly impacts variables like power consumption, efficiency, and durability. The revision of static CMOS logic is necessary to meet future computing systems' computational requirements. In complementary metal-oxide-semiconductor (CMOS) technology, static and dynamic logic are the primary circuit topologies. The CMOS technology, renowned for its static properties, has notable energy efficiency and robustness. However, it is essential to note that this system exhibits notable performance constraints, mainly when implemented in crucial and extensive contexts. On the other hand, it should be noted that Domino logic has high-speed performance but at the cost of significant power consumption and a deficiency in robustness [3].

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Therefore, developing an enhanced digital logic methodology and architecture encompassing the critical aspects of energy efficiency, high speed, and noise robustness is imperative. Therefore, employing the hybrid logic technique in this study is motivated by its favourable characteristics, including its reduced power consumption and ability to integrate many capabilities with a minimal transistor count effectively. However, due to the decrease in threshold voltage, the adders that rely on this logic encounter a reduced operational speed and increased power consumption. The findings above prompted us to propose an enhanced adder design that achieves its intended functionality without increasing the complexity of the manufacturing process while also requiring a lower quantity of transistors [4]. The present study utilizes hybrid logic techniques to construct adders and multiplier circuits tailored explicitly for implementation in Hybrid Transistor logic systems. Utilizing hybrid logic enables the creation of logic circuits with fewer transistors. Compared to alternative static CMOS circuit designs, a notable quantity of energy is preserved. This thesis undertakes a comparative investigation of hybrid logic adders, multipliers, and related circuits constructed through several logic techniques. Given the adder mentioned above, a new multiplier has been successfully developed.

## II. LITERATURE SURVEY

Venkataramani et al. [5] developed a methodological framework called SALSA, which utilizes approximation circuits to facilitate autonomous logic's methodical and disciplined synthesis. The SALSA technique provides an approximate representation of a circuit that satisfies particular criteria, utilizing a conventional Register Transfer Level (RTL) representation of the circuit and a standardized specification that defines the permissible level of errors in the implementation. The authors have made two noteworthy contributions to their scholarly investigation. The authors have provided a comprehensive conceptual framework for addressing the approximate logic synthesis (ALS) problem. Utilizing this framework facilitates the creation of improved circuit designs by implementing iterative development approaches. A robust correspondence has also been established between the approximate synthesis problem and a closely related logic synthesis problem. This mapping enables the effective utilization of existing logic synthesis capabilities for ALS.

Liu et al. [6] introduced the application of machine learning techniques in developing approximation adders and multipliers. The proposed methodology involves incorporating approximation compressors and reduction circuits with complement values into the design of multipliers. This research paper presents and examines a recently discovered effect component dependent on the multiplier's size. This study aimed to assess the significance of various supplementary elements. The designs that were submitted underwent a thorough assessment, with careful consideration given to their hardware properties and error metrics. The efficacy of the recommended solutions surpasses that of previously published machine learning-based designs. Furthermore, this study encompasses scholarly articles that provide evidence of the practicality of the suggested designs.

In their study, Edavoor et al. (2017) conducted an investigation and put up a conceptual framework for advancing two approximation compressors. The fundamental objective of these compressors was to achieve reduced dimensions, minimized delay, and decreased energy consumption while preserving a degree of precision comparable to that of conventional systems. The concepts above have been accomplished using the 45 nm CMOS technological node. The system's efficiency has been comprehensively evaluated concerning several criteria: area, latency, power consumption, power-delay product (PDP), and accurate output count (AOC). The compressors investigated in this study are utilized to produce 8 × 8 and 16 x 16 Dadda multipliers.

The research conducted by IhsenAlouani et al. [8] examines the concept of approximation computing as a design paradigm for diverse applications that can tolerate a certain degree of precision degradation. Removing limitations within traditional digital design approaches can yield enhanced energy efficiency but at the cost of reduced precision. This research paper introduces a novel architectural design that prioritizes precision and incorporates a heterogeneous block to achieve an approximation of parallel multiplication. Researchers have demonstrated that employing a diverse range of crucial elements in creating multipliers, instead of replicating a singular building block, yields more accurate results, as evidenced by their successful design investigation. This study gives empirical facts that can be used to assess precision, response time, and energy efficiency. Following this, these measures are compared with three previous approximation methodologies. The assessed circuits exhibit diminished output precision relative to the recommended heterogeneous multiplier, which effectively compromises efficiency and energy considerations.

The study by K.M. reveals a significant increase in interest regarding the concept of approximation computation in recent years. The motivation behind this interest arises from the possibility of creating algorithms that include mistake tolerance capabilities, leading to decreased energy consumption, latency, and space utilization. Nevertheless, it is crucial to recognize the inherent compromise regarding precision, as Reddy et al. emphasised (2019). This study presents a novel theoretical

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framework for a new 4-2 compressor approximation. This work presents a novel architectural design for the Dadda Multiplier, intending to enhance the utilization of the proposed compressor and minimize the error function. The results indicate that the compressor described in this study significantly reduces the error rate compared to previously mentioned approximation compressors in the academic literature. Multiple image processing programs assess the effectiveness of the multiplier. The multiplication approach, as described, demonstrates an average structural similarity of 85% when comparing images and their respective source images.

The study by Yi et al. (2010) demonstrated that the Digital Multiplier is essential in numerous Digital Signal Processing (DSP) systems, primarily due to its substantial impact on utilising computational resources. The necessity to account for approximation multipliers arises from the limited tolerance of specific digital signal processing (DSP) approaches towards imprecise calculations to achieve energy tradeoffs. This aspect holds particular significance in contexts where the primary focus is on attaining elevated computational energy efficiency levels. The present research study presents a novel methodology for estimating a 4-2 compressor and integrating it into a circuit designed for an error-resilient multiplier. Upon comparing the operand length of this multiplier to earlier instances with an operand length of around 8 bits, it is evident that utilizing it leads to minimal power consumption per operation while maintaining an equivalent degree of computational precision. Compared to the conventional way of multiplication, this particular methodology demonstrates a reduction of 26.7 percent in the Energy-Delay Product (EDP).

## III. PROPOSED HYBRID MULTIPLIER

Multiplication is a commonly utilized technique in various signal-processing applications, including image processing and encryption. Generating partial products in a multiplier is achieved by employing arrays of AND gates. The main focus is on the aggregation of partial products, which eventually limits the maximum operational velocity of a multiplier. The utilization of the HYBRID Adder is implemented in order to accomplish the aggregation of partial products within the HYBRID multiplier system, as depicted in Figure 1. The multiplier demonstrates three separate phases. The first phase entails employing n2 AND gates to produce a partial product. Adders have been utilized to execute addition operations in the second stage. During the third step, the least significant bits (LSB) undergo rounding, resulting in the outcome (11, 12).

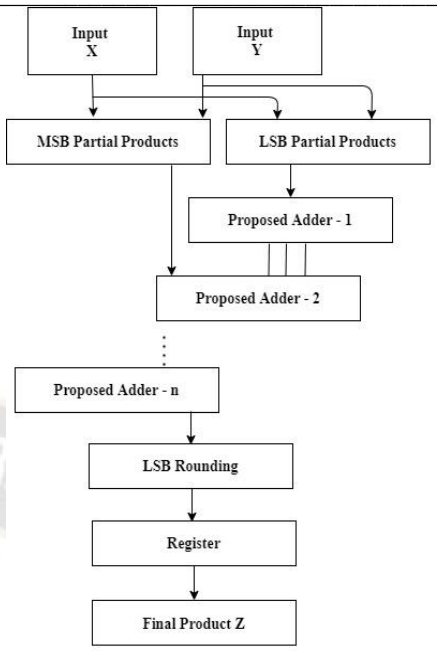


Fig. 1 Flow chart of Hybrid logic multiplier

The proposed hybrid multiplier system employs the hybrid Adder to execute the Summation of partial products. The multiplier is comprised of three discrete stages. The first phase entails employing n2 AND gates to produce a partial result. Adders have been utilized to execute the addition operation in the second stage. During the third phase, the rounding process is applied to the least significant bits (LSB), ultimately leading to the acquisition of the outcome. The circuit, in its entirety, is fabricated using hybrid logic. The employment of the adder design has significantly strengthened the multiplication process.

The Sum of the proposed hybrid adder has been generating the following equation 1.

$$SUM = \overline{(AXORB)}C + (AXORB)\bar{C} \quad \ldots..1$$

The sum outcome generated by the hybrid adder architecture is attained by sequentially linking the hybrid XOR/XNOR and multiplexer modules. The XOR/XNOR operations are performed by the hybrid XOR/XNOR module, which is subsequently followed by a multiplexer. The hybrid XOR/XNOR module comprises transistors M1-M6, while transistors M7 and M8 function as the 2 to 1 multiplexer.

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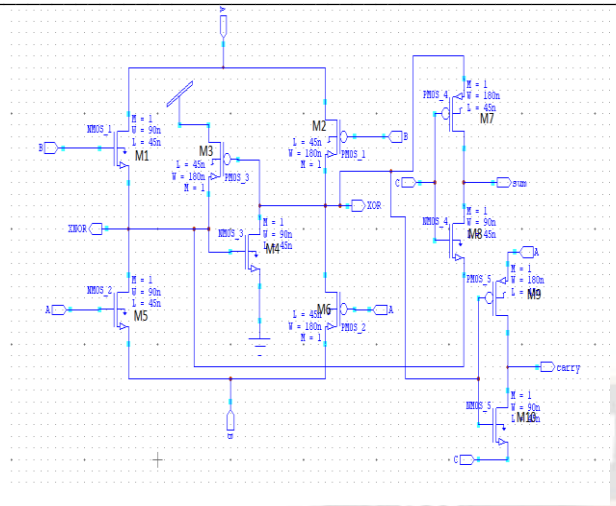


Fig. 2 Proposed HYBRID adder

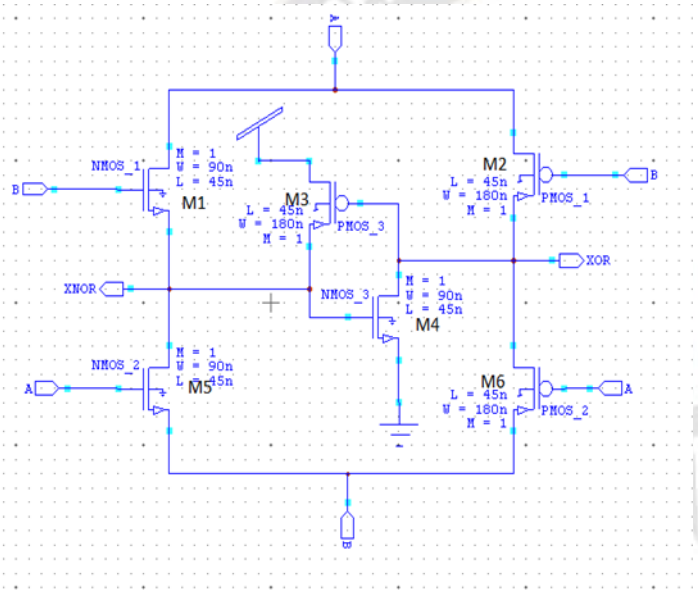


Fig. 3 Proposed Hybrid XOR/XNOR Module

Equation 2 represents the carry generated by the proposed hybrid adder.

$$Carry = A\overline{(AXORB)} + C\ (AXORB)\ldots.2$$

The output signal of the XOR gate, denoted as (A XOR B), serves as the selection input for the multiplexer (MUX). The MUX has two inputs, A and C. The transistors M9 and M10 function as a 2 to 1 multiplexer. The hybrid XOR/XNOR module implemented is seen in Figure 3. Figure 2 illustrates a cross-coupled logic circuit consisting of NMOS and PMOS transistors. The XNOR output can be obtained by employing NMOS logic, while the XOR logic output can be achieved using PMOS logic. The M3 and M4 transistors serve as pass transistors, facilitating the transmission of the pertinent logic output from M1 and M2 and M5 and M6. Figure 3 illustrates a cross-coupled logic circuit consisting of NMOS and PMOS transistors. The XNOR output can be obtained by employing NMOS logic, while the XOR logic output can be achieved using PMOS logic. The M3 and M4 transistors serve as pass transistors, facilitating the transmission of the pertinent logic output from M1 and M2 and M5 and M6. Figure 4 illustrates the conceptualization of a 2x2 multiplier with the suggested hybrid adder design.

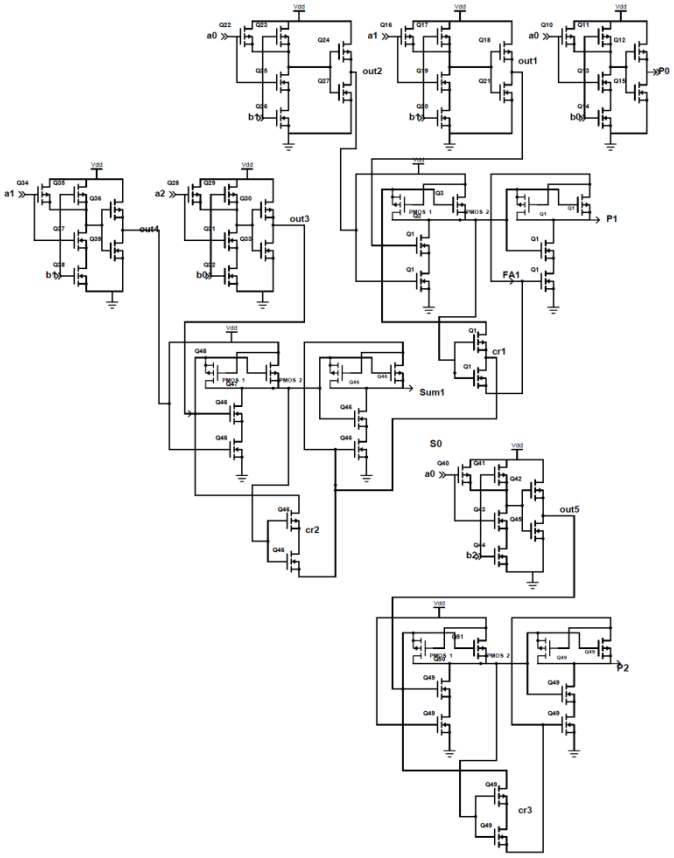


Fig. 4 Proposed HYBRID multiplier based on hybrid adder

## IV. SIMULATION RESULTS

To assess the effectiveness of the recently designed multiplier in the fields of cryptography and digital signal processing (DSP), the implementation of the HYBRID multiplier was carried out using Mentor Graphics EDA tools, with the utilization of CMOS 45nm technology.

The core foundation of the analytical assessment encompasses key performance metrics, including power consumption, latency, and transistor count. The adder circuits used in the experimental study were operated at a frequency of 20 kHz and a temperature of 27 °C to maintain uniformity during the comparing process. Figures 4 and 5 illustrate the demonstrations of the 2x2 multipliers with the typical CMOS adder Hybrid adder.

The simulation analyses the delay, power, and Power Delay Product (PDP) at a supply voltage of 0.8 V, as presented in

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Table 1. The study results suggest that the HYBRID multiplier, as described, demonstrated advantages in terms of delay and power consumption. The Mentor Graphics tools were employed to model the hybrid multiplier circuits implemented using 45 nm technology. The hybrid transistor logic multiplier reduces overall delay by 60% compared to CMOS technology.

The hybrid transistor logic multiplier exhibits a notably reduced average power consumption compared to both CMOS multipliers. The circuitry has been compared with previously produced adders that utilized different approaches. The suggested multiplier aims to overcome the constraints of existing multipliers by lowering circuit complexity and minimizing time delay, improving operational speed. The terms of the resultant product are derived by employing partial products.

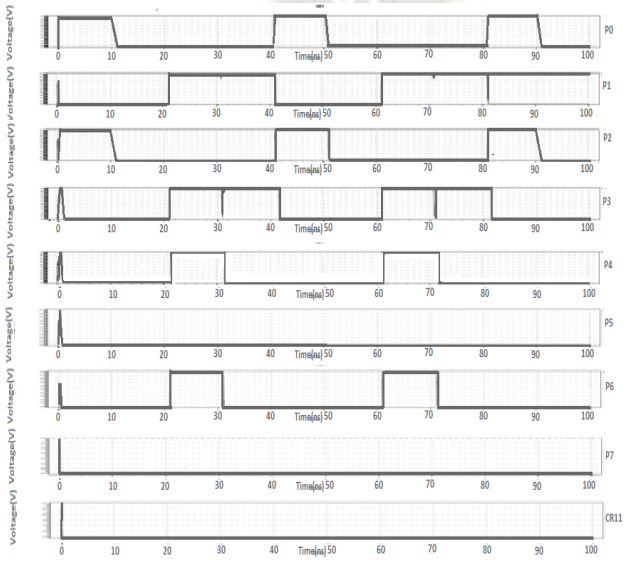


Fig. 4 2x2 multipliers based on conventional CMOS adder

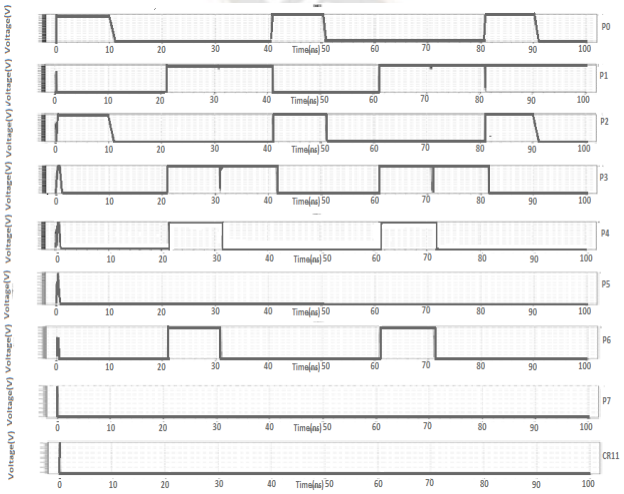


Fig.5 2x2 multipliers based on hybrid adder

Table 1. Comparative Analysis of exiting multipliers w.r.t to proposed HYBRID multipliers

| | Average Power (W) | Delay (ns) |
|---|---|---|
| [17] | 0.1477x10-3 | 72.4 |
| [16] | 0.1475 x10-3 | 72.2 |
| [15] | 0.6080 x10-3 | 73.3 |
| [14] | 0.6740 x10-3 | 72.3 |
| [13] | 0.6791 x10-3 | 72.4 |
| HYBRID Multiplier | 1.96 x10-6 | 47.8 |

## V. CONCLUSION

Many designs have been extensively examined and assessed to develop an effective design capable of fulfilling the growing need for big multipliers in many applications. The hybrid Multiplier integrates a hybrid Adder and has been effectively designed and constructed utilizing CMOS 45nm technology and Mentor Graphics software. The hybrid transistor logic multiplier reduces overall delay by 60% compared to the CMOS multiplier. The hybrid transistor logic multiplier exhibits a notably reduced average power consumption compared to CMOS multipliers. The circuitry has been compared with previously produced adders that utilized different approaches. The hybrid adder design has been used as a replacement for the traditional architecture of adders to improve the performance of multipliers in terms of spatial efficiency and processing speed.

**References:**

[1] Manish Kumar, JonaliNath., (2017) Design of an Energy Efficient 4-2 Compressor, IOP Conf. Series: Materials Science and Engineering, Vol 225.

[2] Jorge Tonfat, Ricardo Reis.,2012. Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN. ln: XXVII SIM - South Symposium on Microelectronics, Latin America 29 Feb.-2 March 2012.

[3] ShimaMehrabi, Reza FaghihMirzaee, ShararehZamanzadeh, Amir hosseinJamalian.,(2017) Multiplication With m:2 and m:3 Compressors: A Comparative Review, Canadian Journal of Electrical and Computer Engineering, vol. 40, issue . 4.

[4] FarnazSabetzadeh, Mohammad HosseinMoaiyeri., (2019) A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication, IEEE Transactions on Circuits And Systems–I: Regular Papers.

[5] Vivek J. Kozhikkottu; AmitSabne; Kaushik Roy; AnandRaghunathan., (2020) Logic Synthesis of Approximate Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems , Volume: 39, Issue:

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10.

[6] Weiqiang Liu; Tingting Zhang; Emma McLarnon; Maire O'Neill; Paolo Montuschi; Fabrizio Lombardi., (2021) Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers, IEEE Transactions on Emerging Topics in Computing , Volume: 9, Issue: 3.

[7] Pranose J. Edavoor; SitharaRaveendran; Amol D. Rahulkar., (2020) Approximate Multiplier Design Using Novel Dual-Stage 4:2 Compressors, IEEE Access, Volume: 8.

[8] IhsenAlouani1 ,Hamzeh Ahangari2 , Ozcan Ozturk2 , and Smail Niar1., (2017) A Novel Heterogeneous Approximate Multiplier for Low Power and High Performance: IEEE Embedded Systems Letters.

[9] Karri Manikantta Reddy, M.H. Vasantha, Y.B. Nithin Kumar, DeveshDwivedi , (2019) Design and analysis of multiplier using approximate 4-2 compressor: International Journal of Electronics and Communications, Volume 107, Pages 89-97.

[10] Xilin Yi, Haoran Pei, Ziji Zhang, Hang Zhou, and Yajuan He., 2019 . Design of an Energy-Efficient Approximate Compressor for Error-Resilient Multiplications.,ln: IEEE Conference.

[11] ANUSHA GORANTLA, DEEPA P., (2017) Design of Approximate Compressors for Multiplication: ACM Journal on Emerging Technologies in Computing Systems, Vol. 13, No. 3, Article 44.

[12] Haoran Pei, Xilin Yi, Hang Zhou, and Yajuan He., (2020) Design of ultra-low power consumption approximate 4-2 compressors based on the compensation characteristic: , : DOI 10.1109/TCSII.2020.3004929.

[13] C.S. Wallace, A suggestion for a fast multiplier. IEEE Trans. Elect. Comput. 13(1), 14–17 (1964).. 39. R.S. Waters, E.E. Swartzlander, A reduced complexity wallace multiplier reduction. IEEE Trans. Comput. 59(8), 1134–1137 (2010).

[14] S. Asif, Y. Kong, Analysis of different architectures of counter based wallace multipliers. In Proceedings of the 2015 Tenth International Conference on Computer Engineering Systems (ICCES), pp 139–144, (2015).

[15] S. Asif, Y. Kong, Design of an algorithmic wallace multiplier using high speed counters. In Proceedings of the 2015 Tenth International Conference on Computer Engineering Systems (ICCES), pp 133–138 (2015). https://doi.org/10.1109/ICCES.2015.7393033

[16] C. Fritz, A. T. Fam. Fast binary counters based on symmetric stacking. IEEE Trans. Very Large Scale Integ. (VLSI) Syst. 25(10):2971–2975 (2017). https://doi.org/10.1109/TVLSI.2017.2723475

[17] Rahman, M.; Afonso, R.; Tennakoon, H.; Sechen, C. Design automation tools and libraries for low power digital design. In Proceedings of the 2010 IEEE Dallas Circuits and Systems Workshop, Richardson, TX, USA, 17–18 October 2010.